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Simulation of Pentacene Organic Metal-Oxide Field Effect Transistors

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Simulation of Pentacene Organic Metal-Oxide Field Effect Transistors

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2003
by
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Taylor University, Indiana, 1996

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Committee Members: Dr. Marc Cahay, Dr. Punit Boolchand
Abstract

The search for lighter and cheaper electronics has recently begun investigating a new group of materials, organic semiconductors, which have not previously been considered for use in charge manipulation and transport in transistors. Recent progress has even begun to steal the spotlight from the current leader in electronics, which is the world of inorganic semiconductors such as silicon and gallium arsenide. This new type of semiconducting material which has drawn increased interest from scientists and engineers is that of organic semiconductors. Historically, organic material has been largely insulating in its nature. But research in recent years has demonstrated the ability to form organic materials whose ability to conduct current can be modified so that semiconducting characteristics can be achieved. In fact, field effect transistors based on charge transport in organic semiconductors have been demonstrated. Recently, organic transistor speeds have become comparable to that of devices based on amorphous silicon. This has peaked interest in the possibility that organic-based transistors could replace amorphous silicon FETs in flat panel displays and other areas of technology. Currently, a wide variety of organic materials are being investigated for use in these transistors.

Because of the early stage of the development of these organic transistors, there has been very little work on computer modeling of the devices. This thesis describes the use of a commercial modeling software package, ATLAS from Silvaco International, to simulate the operation of an insulating gate, field effect transistor (MOSFET) based on the organic semiconductor pentacene. Material properties are drawn from a survey of the published literature and results are compared with measurements reported on experimental, prototype devices. The objective is to develop an understanding of the factors limiting device performance in order to improve the device’s design and operation.
Acknowledgements

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I would like to thank my advisor, Dr. Roenker, for all his support and help in researching and developing the ATLAS simulations in this new and exciting field of research. His encouragement and patience has helped me to complete this project in a constrained time period. He has gone above and beyond the role of just an advisor by helping me at a moments notice and explaining complex concepts to me despite his busy schedule. I’d also like to thank the other members of my advising committer, Dr. Cahay and Dr. Boolchand for not only their participation in the advising committee but also their instruction in the classes I have taken from them.

I would also like to thank my loving wife, Alison, who has encouraged me and enabled me to enroll as a full time student. She has been a real inspiration to me and a wonderful companion in this segment of our life together.

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Chapter 1

1.1 Introduction

In 2000 the Nobel Prize in Chemistry was awarded for developments in new semiconducting materials. However, the three chemists who received this prestigious award were not studying leading edge materials such as silicon and gallium arsenide, but organic semiconductors. Since Alan Heeger, Alan MacDiarmid, and Hideki Shirakawa first began studying how to alter the level of conductivity of polymers in 1976, the interest in conducting polymers has exploded [1,2]. While investigating the chemistry of conducting polymers, Alan Heeger’s group discovered the conductivity of polymers could be controllably altered from that of an insulator.

![Levels of conductivity of several doped organic polymers](image)

Figure 1.1 Levels of conductivity of several doped organic polymers [2].
to semiconducting, to that of a metallic conductor [1]. By carefully controlling chemical reactions, the level of doping in polymers can be changed several orders of magnitude as seen in Figure 1.1. This is a characteristic typical of conventional semiconductors such as silicon. This ability of these polymers to be able to mirror metallic properties when doped high enough prompted them to be nicknamed Synthetic Metals.

The wide range of conductivity of these polymers is a product of their unique structure. Polymers consist of small unit cells containing a hydrogen-carbon configuration, which become chemically bonded together to form a giant molecule or macromolecule. The macromolecule is called a conjugated polymer because of this long, repeating chain. Bonding occurs as the carbon

### Electrical conductivity
- Conductivity approaching that of copper
- Chemical doping induces solubility
- Transparent electrodes, antistatics
- EMI shielding, conducting fibers

### Control of electrochemical potential
- Electrochemical batteries
- Electrochromism and “Smart Windows”
- Light-emitting electrochemical cells

---

**Figure 1.2** Doping methods with regards to applications of conjugated polymer [1].
atoms are brought together to form the backbone of the molecule, but leaves one π-bonded electron weakly bonded \[1\]. The weakly bound electron can then give rise to charge carrier transport in the presence of an electric field, which takes place along the carbon bonded backbone \[1\]. Controlling the conductivity is simply a process of doping the polymer to capture or free more electrons in the macromolecule.

The process of doping conjugated polymers uses much different methods than that employed for inorganic semiconductors such as silicon or gallium arsenide. Chemists control the

![Figure 1.3 Oxidation of emeraldine by HCL. The level of conductivity can be measured by the pH of the solution \[2\].](image)
conductivity through various methods which are a function of the applications as shown in Figure 1.2 [1]. These methods of doping include: oxidation/reduction reactions, electrochemical methods, acid-base reactions or photodoping [1]. Figure 1.3 shows an example of doping by the oxidation of emeraldine by hydrochloric acid (HCL), where emeraldine’s conductivity can be altered through eleven orders of magnitude by a timed exposure to HCL [2]. The conductivity was subsequently determined by measuring the acidity (pH) of the solution. As the HCL combined with the emeraldine, the pH level drops; thereby giving an accurate way to determine the level of the conductivity.

An interesting phenomenon of organic semiconducting polymers is the vast array of available materials that have been reported. Although p-type organic semiconductors were studied and developed first, n-type are now under extensive investigation. Tables 1.1 and 1.2, respectively,

<table>
<thead>
<tr>
<th>Year</th>
<th>Mobility [cm² V⁻¹ s⁻¹]</th>
<th>Material</th>
<th>I₆₀/Iₒff</th>
<th>W/L</th>
</tr>
</thead>
<tbody>
<tr>
<td>1990</td>
<td>2 × 10⁻⁴</td>
<td>PC₆</td>
<td>NR</td>
<td>0.1 cm/50 µm</td>
</tr>
<tr>
<td>1990</td>
<td>1.4 × 10⁻³</td>
<td>PC₆₃₃</td>
<td>NR</td>
<td>0.1 cm/50 µm</td>
</tr>
<tr>
<td>1993</td>
<td>10⁻⁴</td>
<td>C₆₀/C₇₀ 9:1</td>
<td>NR</td>
<td>8 cm/5 µm</td>
</tr>
<tr>
<td>1994</td>
<td>3 × 10⁻⁵</td>
<td>TCNQ</td>
<td>4-450 [a]</td>
<td>10 mm/5 µm</td>
</tr>
<tr>
<td>1995</td>
<td>0.08</td>
<td>C₆₀</td>
<td>10⁶</td>
<td>400</td>
</tr>
<tr>
<td></td>
<td>0.3</td>
<td></td>
<td></td>
<td>22</td>
</tr>
<tr>
<td>1996</td>
<td>1.5 × 10⁻⁵</td>
<td>PTCDI-Ph</td>
<td>NR</td>
<td>0.5 cm/50 µm</td>
</tr>
<tr>
<td>1996</td>
<td>0.003</td>
<td>TCNQ</td>
<td>8 [b]</td>
<td>250 µm/12 µm [b]</td>
</tr>
<tr>
<td>1996</td>
<td>10⁻⁴</td>
<td>NTCDI</td>
<td>10² [b]</td>
<td>250 µm/12 µm [b]</td>
</tr>
<tr>
<td>1996</td>
<td>0.003</td>
<td>NTCDA</td>
<td>10³ [b]</td>
<td>250 µm/12 µm</td>
</tr>
<tr>
<td>1997</td>
<td>10⁻⁴-10⁻⁵</td>
<td>PTCDI</td>
<td>NR [b]</td>
<td>250 µm/12 µm</td>
</tr>
<tr>
<td>1998</td>
<td>0.03</td>
<td>F16CuPc</td>
<td>5 × 10⁴</td>
<td>250 µm/12 µm</td>
</tr>
<tr>
<td>2000</td>
<td>0.06</td>
<td>NTCDI-C₈F</td>
<td>10⁵</td>
<td>1.7</td>
</tr>
<tr>
<td></td>
<td>0.1</td>
<td></td>
<td></td>
<td>1.5</td>
</tr>
<tr>
<td>2000</td>
<td>0.02</td>
<td>DHF-6T</td>
<td>10⁵</td>
<td>1.5 mm/75 µm</td>
</tr>
<tr>
<td></td>
<td>0.5</td>
<td>Pentacene</td>
<td>NR</td>
<td>10-100</td>
</tr>
<tr>
<td>2001</td>
<td>0.6</td>
<td>PTCDI-C₈</td>
<td>10⁵</td>
<td>1500 µm/95 µm</td>
</tr>
</tbody>
</table>
show the progress of MOSFET transistors based on both n and p-type organic semiconductors and how the leading edge materials have changed over the years. Dimitrakopoulos et al. [3] has recently published a comprehensive review of progress into the development of organic semiconductor based transistors.

Table 1.2 Progress of P-type Organic Semiconducting Material [3].

<table>
<thead>
<tr>
<th>Year</th>
<th>Mobility [a] [cm² V⁻¹ s⁻¹]</th>
<th>Material (deposition method) [b]</th>
<th>( I_{on}/I_{off} [\text{c}])</th>
<th>W/L</th>
</tr>
</thead>
<tbody>
<tr>
<td>1964</td>
<td>NR [d]</td>
<td>Cu-phthalocyanine (v) (first demonstration of field effect in small organic molecules)</td>
<td>NR</td>
<td></td>
</tr>
<tr>
<td>1983</td>
<td>NR</td>
<td>Polyacetylene (s) (first demonstration of field effect in polymers)</td>
<td>NR</td>
<td>200</td>
</tr>
<tr>
<td>1984</td>
<td>(1.5 \times 10^{-5})</td>
<td>Merocyanine</td>
<td>NR</td>
<td>7000</td>
</tr>
<tr>
<td>1986</td>
<td>(10^{-5})</td>
<td>Polythiophene (s)</td>
<td>(10^5)</td>
<td>NR</td>
</tr>
<tr>
<td>1988</td>
<td>(10^{-4})</td>
<td>Polyacetylene (s)</td>
<td>750</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(10^{-3})</td>
<td>Phthalocyanine (v)</td>
<td>NR</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td>(10^{-4})</td>
<td>Poly(3-hexylthiophene) (s)</td>
<td>NR</td>
<td>NR</td>
</tr>
<tr>
<td>1989</td>
<td>(10^{-3})</td>
<td>Poly(3-alkythiophene) (s)</td>
<td>NR</td>
<td>NR</td>
</tr>
<tr>
<td></td>
<td>(10^{-3})</td>
<td>(\alpha)-sexithiophene (v)</td>
<td>NR</td>
<td>NR</td>
</tr>
<tr>
<td>1992</td>
<td>(0.027)</td>
<td>(\alpha)-sexithiophene (v)</td>
<td>NR</td>
<td>100</td>
</tr>
<tr>
<td></td>
<td>(2 \times 10^{-3})</td>
<td>Pentacene (v)</td>
<td>NR</td>
<td>NR</td>
</tr>
<tr>
<td>1993</td>
<td>(0.05)</td>
<td>(\alpha)-dihexyl-sexithiophene (v)</td>
<td>NR</td>
<td>100-200</td>
</tr>
<tr>
<td></td>
<td>(0.22\ [e]</td>
<td>Polythiénylènevinyle (s)</td>
<td>NR</td>
<td>1000</td>
</tr>
<tr>
<td>1994</td>
<td>(0.06)</td>
<td>(\alpha)-dihexyl-sexithiophene (v)</td>
<td>NR</td>
<td>50</td>
</tr>
<tr>
<td>1995</td>
<td>(0.03)</td>
<td>(\alpha)-sexithiophene (v)</td>
<td>(&gt;10^6)</td>
<td>21</td>
</tr>
<tr>
<td></td>
<td>(0.03)</td>
<td>Pentacene (v)</td>
<td>140</td>
<td>1000</td>
</tr>
<tr>
<td>1996</td>
<td>(0.02)</td>
<td>Phthalocyanine (v)</td>
<td>(2 \times 10^5)</td>
<td>NR</td>
</tr>
<tr>
<td></td>
<td>(0.045)</td>
<td>Poly(3-hexylthiophene) (s)</td>
<td>340</td>
<td>20.8</td>
</tr>
<tr>
<td></td>
<td>(0.62)</td>
<td>Pentacene (v)</td>
<td>(10^6)</td>
<td>11</td>
</tr>
<tr>
<td>1997</td>
<td>(1.5)</td>
<td>Pentacene (v)</td>
<td>(10^6)</td>
<td>2.5</td>
</tr>
<tr>
<td></td>
<td>(0.13)</td>
<td>(\alpha)-dihexyl-sexithiophene (v)</td>
<td>(&gt;10^4)</td>
<td>7.3</td>
</tr>
<tr>
<td></td>
<td>(0.05)</td>
<td>Bs(dithienothiophene) (v)</td>
<td>(10^6)</td>
<td>500</td>
</tr>
<tr>
<td>1998</td>
<td>(0.1)</td>
<td>Poly(3-hexylthiophene) (s)</td>
<td>(&gt;10^6)</td>
<td>20</td>
</tr>
<tr>
<td></td>
<td>(0.23)</td>
<td>(\alpha)-dihexyl-quaterthiophene (v)</td>
<td>NR</td>
<td>1.5</td>
</tr>
<tr>
<td></td>
<td>(0.15)</td>
<td>Dhexyl-anthradithiophene</td>
<td>NR</td>
<td>1.5</td>
</tr>
<tr>
<td>2000</td>
<td>(0.1)</td>
<td>(\alpha)-dihexyl-quinqueithiophene (s)</td>
<td>NR</td>
<td>NR</td>
</tr>
<tr>
<td></td>
<td>(2.4)</td>
<td>pentacene (v)</td>
<td>(10^6)</td>
<td>10-100</td>
</tr>
</tbody>
</table>
1.2 Organic Semiconducting Device Applications

Extraordinary developments in organic semiconductor research have created a growing interest in commercial applications. Due to the very low carrier mobility (< 1 cm²/V·sec), the suitable applications are low speed, low cost ones such as packaging and electronic flat panel displays [4]. While low cost, these applications have a potentially huge market for themselves. Although the maturity of the research of the charge carrier transport process in inorganic semiconductors (such as silicon and gallium arsenide) has resulted in a dominance of inorganic devices in the market, there is still a considerable opportunity waiting to be tapped by organic semiconductors. Organic based devices are expected to challenge amorphous silicon for markets such as flat panel displays, solar cells and similar applications where low cost is the dominant factor. As evidence of the progress in organic semiconductors in recent years, Figure 1.4 shows the orders of magnitude increase in mobility due to research progress of several organic semiconducting materials. Advances in organic semiconductor research have begun to yield

Figure 1.4  Progress of several leading organic semiconducting materials’ mobilities. [5]
mobilities as high as 2.4 cm$^2$/V$^{-1}$s$^{-1}$ [3]. These reported mobilities have closed the gap between organic semiconductors and amorphous silicon which is currently used as the semiconducting material in flat panel displays.

One of primary commercial targets for organic semiconductors is flat panel displays. Traditionally, these displays currently consist of a matrix of amorphous silicon light emitting diodes. The light they emit passes through a filter which creates the desired colored pixel. In recent years there has been considerable progress in developing organic light emitting diodes so that organic based flat panel displays are being developed. For such displays, transistors are needed to control current flow to individual pixels to turn them on. For organic LED displays, organic–based transistors are needed. In addition, due to the light weight nature of organics, they are attractive to replace the heavier amorphous silicon. Another advantage of organic materials is their mechanical flexibility as demonstrated in Figure 1.5. If flat panel screens can be created with organic light emitting diodes OLED their flexible nature will not limit them to a flat two dimensional display. Currently there are many groups whose main focus is to develop organic-based semiconductor displays. The University of California has developed electroluminescent devices out of indium-tin-oxide through the use of inkjet printing deposition methods on glass

Figure 1.5 Organic PEN circuits demonstrated on a flexible substrate [4].

10
(see Figure 1.6) [6]. Other groups at the University have created dual color displays by combining polymers as seen in Figure 1.7 [7]. Furthermore, flexible arrays of OLEDs on plastic have already been demonstrated by Universal Display Corporation [8].

Organic transistors are also being created and developed for other commercial markets. Many companies such as Bell Labs, are investigating organic transistors for use in memory [9]. A.R. Brown et al. has used pentacene for logic circuits and data storage, and has demonstrated simple nor and nand gates as well as pentacene based ring oscillators [10]. Other uses for pentacene and other organic semiconducting materials include: low cost solar cells [11], ring oscillators [12], logic gates [13], and transistors arrays [12].

![Figure 1.6](image)

**Figure 1.6** Electroluminescence demonstrated by deposition of ITO on glass [6].
One interesting implementation of organics transistors is their use in smart cards and RF tags [13]. Smart cards are similar to credit cards; however, they have a built-in microchip. This microchip can store hard coded information which makes the card unique to the owner. Organics are ideal for smart cards due to their light weight and ability to operate on a flexible substrate. For this same reason they are useful for RF tag technology [14]. RF tags are similar in use to barcodes. However instead of being scanned by a laser, they are excited by an external RF source, which causes them to emit their stored information [15]. If fabrication costs could be sufficiently reduced, these could replace barcodes and help to make inventory and store checkout a more efficient process.

Currently limiting these applications are problems due to the immaturity of the research in organic semiconducting material. Most organics tend to exhibit p-type charge carrier characteristics even when they are not intentionally doped. N-type materials which have been created in labs tend to be unstable and degrade quickly in normal atmospheric conditions [3].

Figure 1.7 Deposition of dual color organic LED [7].
This makes complimentary FET-based circuits difficult to achieve and the creation of microprocessors very unlikely. However, the low cost, flexibility and light weight of the organic semiconductors is continuing to drive a strong interest into their development.

1.3 Introduction to Organic MOSFET Transistors

Considerable research has been directed towards developing organic semiconducting transistors. MOSFET transistors have particularly been targeted for extensive research and fabrication [3]. The physics of charge transport in organic semiconductors has been theoretically and experimentally investigated by a number of researchers [1, 2, 16, 17, 18].

The transport process in organic semiconductors is considerably different from that in silicon and III-V semiconductors where the material has a single crystal structure. For the organic semiconductors, the material typically has a polycrystalline or amorphous structure so that the transport process is more difficult and irregular. Some researchers [3, 16, 18] describe the transport process as one involving hopping between adjacent localized states similar to transport in dielectrics such as silicon oxide at high fields. The transport process has also been described in terms of polarons where the presence of a charge distorts the structure around it [1, 5, 17].

For this work, we will follow an empirical approach starting from the fact that application of an electric field is observed to produce charge transport and flow from which an effective carrier mobility can be extracted. For modeling purposes, the microscopic details of the transport process will be neglected and an effective mobility will be used to describe the charge transport process where the mobility’s value will be taken from experimental reports in the
literature. Similarly, the organic semiconductor will be treated as a classic semiconductor with a well defined bandgap, where again its value will be taken from the experimental reports. While admittedly this is a crude approximation to the physics occurring in the organic semiconductor, it will allow us to begin device modeling as a first approximation to simulating device operation and performance.

Analogous to silicon MOSFETs, for organic MOSFETs operation is established by a flow of charge carriers between the source and drain driven by the source drain bias which is varied by a voltage applied on the gate. The current flow is then governed at low drain biases following the MOSFETs operation by [3],

\[ I_D = \frac{W C_i \mu}{L} \left( V_G - V_T - \frac{V_D}{2} \right) \cdot V_D \] (1.1)

where \( L \) is the length of the channel, \( W \) is the channel width, \( \mu \) is the mobility, \( C_i = \varepsilon_{ox}/t_{ox} \) where \( t_{ox} \) is the gate oxide thickness, \( V_G \) is the gate bias and \( V_D \) is the potential between the source and drain. As the channel width (\( W \)) is increased, more majority carriers are allowed to enter the charge sheet region, so there is an increase in the device current. While the equations are typically the same as those for the silicon MOSFET, the charge carriers and their origin in organic materials are quite different.

Silicon based semiconductors must be subjected to ion implantation or thermal diffusion to control the amount of impurities and to make them n or p-type material. Many organic materials such as pentacene (Pc) naturally contain an imbalance of charge carriers of one kind (see Table 1.1) which negates the need for the doping process. Pentacene in particular contains an abundance of hole charge carriers which categorizes it as a p-type semiconductor. This abundance of positive charge carriers comes from the flaws and nature of the material’s crystal structure. These charge carriers exist as heavy quasi-particles called polarons which will be
discussed in chapter two. N-type organic semiconductors have typically been more difficult to produce (see Table 1.2) and more rapidly degrade [3]. As useful as this inherent doping may appear, it does create a problem. Perfection of the organic crystal must be of high importance in order to achieve maximum order and a high mobility. Furthermore, the material’s conductivity becomes a function of the fabrication process and sample history, which makes it tricky to control and difficult to repeat the process consistently.

Another difference between organic versus inorganic MOSFET transistors is in their voltage operating range. Due to the very low mobilities of carriers in organic semiconductors, larger electric fields are needed to achieve the same current level. In addition, typical organic MOSFETs have larger channel lengths (few µm versus submicron for silicon). As a result, typical organic transistors will operate with a gate voltage range of 0-100V as seen in Figure 1.8.

![Graph](image)

**Figure 1.8** Typical operating range of a organic semiconducting MOS transistors which in this case is pentacene [3].
The same is true of the source to drain voltage. Inorganic transistors such as silicon on the other hand typically operate in the 0-5V range. Organic transistor operating voltages can be dramatically decreased but only at the expense of increasing the size of the channel width or decreasing the length (see equation 1.1). Phillips Research Laboratory has created p-type pentacene transistors that operate from 0-10V [10, 19]. This has been accomplished by increasing the channel width to 10 mm for a channel length of 12 µm (see Figure 1.9). However, integration of an array of 10 mm wide transistors to drive a flat panel display screen might not be feasible. Advances in organic fabrication techniques and a better understanding of the physics of organic transistors will help to optimize their dimensions without losing performance characteristics.

Figure 1.9 Organic MOS transistor IV curves for devices size L=12µm, W=10000µm [10].
A number of different organic materials have been investigated and improved recently. Dimitrakopoulos et al. [3] provides a review of reports before 2002. Table 1.3 shows several of these materials and how they compare to each other.

<table>
<thead>
<tr>
<th>Material</th>
<th>Mobility</th>
<th>Year</th>
<th>L</th>
<th>W</th>
<th>Config.</th>
<th>Deposition</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>6T</td>
<td>2.00E-01</td>
<td>2001</td>
<td>50</td>
<td>1000</td>
<td>Top</td>
<td>Thermal</td>
<td>[20]</td>
</tr>
<tr>
<td>PEDOT</td>
<td>2.00E-02</td>
<td>2000</td>
<td>20</td>
<td>3000</td>
<td>Bottom</td>
<td>Ink Jet</td>
<td>[21]</td>
</tr>
<tr>
<td>PTV</td>
<td>3.00E-04</td>
<td>1998</td>
<td>2</td>
<td>1000</td>
<td>Bottom</td>
<td>Spin Coat</td>
<td>[13]</td>
</tr>
<tr>
<td>PTV</td>
<td>2.00E-02</td>
<td>2002</td>
<td>10</td>
<td>20000</td>
<td>Bottom</td>
<td>Spin Coat</td>
<td>[19]</td>
</tr>
<tr>
<td>PTV</td>
<td>1.00E-04</td>
<td>1997</td>
<td>10</td>
<td>20000</td>
<td>Bottom</td>
<td>Spin Coat</td>
<td>[10]</td>
</tr>
<tr>
<td>Pc</td>
<td>3.00E-02</td>
<td>1997</td>
<td>8</td>
<td>10000</td>
<td>Bottom</td>
<td>Spin Coat</td>
<td>[10]</td>
</tr>
<tr>
<td>Pc</td>
<td>4.00E-01</td>
<td>2000</td>
<td>20</td>
<td>25</td>
<td>Bottom</td>
<td>Thermal</td>
<td>[12]</td>
</tr>
<tr>
<td>Pc</td>
<td>2.20E-01</td>
<td>2000</td>
<td>30</td>
<td>220</td>
<td>Top</td>
<td>Evap. Flash</td>
<td>[22]</td>
</tr>
<tr>
<td>Pc</td>
<td>1.20E+00</td>
<td>2000</td>
<td>20</td>
<td>220</td>
<td>Bottom</td>
<td>Evap. Flash</td>
<td>[22]</td>
</tr>
<tr>
<td>Pc</td>
<td>3.90E-01</td>
<td>2001</td>
<td>100</td>
<td>650</td>
<td>Top</td>
<td>Thermal</td>
<td>[23]</td>
</tr>
<tr>
<td>Pc</td>
<td>2.00E-03</td>
<td>2002</td>
<td>10</td>
<td>20000</td>
<td>Bottom</td>
<td>Spin Coat</td>
<td>[19]</td>
</tr>
<tr>
<td>Pc</td>
<td>1.03E+00</td>
<td>2002</td>
<td>15.4</td>
<td>1000</td>
<td>Top</td>
<td>Thermal</td>
<td>[3]</td>
</tr>
</tbody>
</table>

A measure of the performance can be assessed by their speed or mobility. For pentacene, the hole mobilities reported range from $2.0 \times 10^{-3}$ to 1.2 cm²/V·s. The exact value likely depends on the deposition process, degree of crystallinity and the material purity.

However, there are also device configuration considerations such as the placement of the electrodes that affect device performance. Two simple fabrication methods, bottom and top configurations, for MOSFET transistors have been created to quickly prototype devices. Figure 1.10 shows the device geometry for the bottom and top contact configurations. Virtually all reported organic MOSFETs employ one of these configurations. These designs each have their advantages and disadvantages which will be discussed further in chapter three.
In an effort to reduce costs, it is quite useful to characterize a transistor design prior to its fabrication. Due to the complexity of the charge transport in organic semiconductors this is a difficult undertaking. Typical modeling begins with a basic set of equations that describe charge transport in MOS transistors which will be discussed in chapter three. Most groups will then extract material parameter to fit their data. Other groups such as Meijer et al., use an existing hopping model or develop their own to fit equations to the relative data [19]. Table 1.4 lists the methods several groups have used to model organic MOS transistors. Because of the random

Figure 1.10 Top (a) and bottom (b) contact configurations for the source/drain electrodes in organic MOSFETs [5, 24].
nature of the molecular structure in organics, it is difficult to predict the behavior of future fabricated transistors. That is why this thesis is looking at a commercially available simulator to help understand the devices and predict their behavior.

<table>
<thead>
<tr>
<th>Material</th>
<th>Modeled Characteristics</th>
<th>Model</th>
<th>Method</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pc, PTV, P3HT</td>
<td>Transfer Characteristics</td>
<td>Hopping Model</td>
<td>Numerical</td>
<td>[19]</td>
</tr>
<tr>
<td>Pc</td>
<td>Threshold Voltage</td>
<td>Trapping Model</td>
<td>Numerical</td>
<td>[18]</td>
</tr>
<tr>
<td>6T</td>
<td>IV and Short Channel</td>
<td>Padre</td>
<td>Analytical</td>
<td>[25]</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Unified Charge</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pc</td>
<td>DC Characteristics</td>
<td>Control</td>
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<td>[22]</td>
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<tr>
<td>α-6T</td>
<td>Electrical Characteristics</td>
<td>Transistor Model</td>
<td>Analytical</td>
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<tr>
<td>α-6T</td>
<td>Threshold Voltage</td>
<td>Trapping Model</td>
<td>Analytical</td>
<td>[27]</td>
</tr>
<tr>
<td>Pc</td>
<td>Transfer Characteristics</td>
<td>Transistor Model</td>
<td>Analytical</td>
<td>[3]</td>
</tr>
</tbody>
</table>

1.4 Organic Semiconductor Fabrication Processes

Much of the technology which has been used in the development of organic semiconducting transistors has been borrowed from inorganic MOSFET and MESFET fabrication processes. These include thermal evaporation, optical lithography and lift-off metallization techniques. But in an effort to lower the fabrication costs, engineers have adapted these techniques and developed new ones especially suited for organic transistors. A brief and simplified explanation of organic MOSFET transistor fabrication techniques follows.

1.4.1 Thermal Evaporation of Organic Material

The technique of thermal evaporation has been used by a number of researchers to fabricate organic transistors, which have produced devices with the highest reported mobilities [3, 12, 23]. The purity of the organic material leads to longer diffusion length of the charge
carriers due to less interaction with the lattice which slows down the carriers and the device. Furthermore, impurities in the material tend to chemically combine with the organic semiconducting material which leads to irregularities in the band gap [28]. Therefore, evaporation is carried out under high or ultra high vacuum conditions to remove impurities and increase the quality of the material. Although this does lead to better devices, the expense of the equipment and the process is comparatively high, which has led many research groups to investigate alternative and cheaper methods of fabrication.

1.4.2 Spin Coating and Soft Lithography

Another method of depositing the organic material onto a substrate is spin coating. This method is borrowed from the deposition process for photoresist for the lithography process. In this process the material in its liquid state is deposited onto the wafer which is held by a vacuum to a spindle. After deposition of the liquid, the whole assembly is spun at a high speed (rpm) to obtain the desired final thickness of photoresist or in this case organic semiconducting material. This is a very simple process, but it also requires a subsequent process to pattern the organic material.

A new technology which has reduced the fabrication costs of organic transistors is soft lithography. Currently photolithography is the standard method to pattern the layers for the fabrication of silicon and III-IV transistors. It is begun by spin coating photoresist onto the wafer, exposing it to ultra violet light and developing the exposed or unexposed portions (depending on the type of design). The patterned photoresist then protects portions of the underlying layer from etching or doping. Soft lithography replaces the exposing and developing steps of this photolithography process by patterning the semiconducting material directly. This
The fabrication of a PDMS stamp is accomplished by creating a stamp out of polydimethylsiloxane (PDMS) as shown in Figure 1.11 [29]. The stamp is initially created first using photolithography to pattern the photoresist after which the liquid PDMS is deposited over the pattern. Once the PDMS hardens, it is peeled away and constitutes a master stamp that can be used to pattern organic material over several hundred uses [30]. Figure 1.12 shows a PDMS master stamp created using soft lithography techniques and the pattern it has created in a thin film polymer. Several patterning processes have been developed in conjunction with the use of these PDMS stamps.

One such fabrication process using PDMS stamps is called microcontact printing (µCP) [30]. While the semiconducting material is still in its liquid phase, the stamp is pressed into it. Once it cools off and solidifies, the stamp is removed leaving an impression which is the
A very similar form of this lithography method is called solvent assisted micromolding (SAMIM) [30]. In this process the stamp is first wet with a solvent. This assists the stamping process by dissolving the semiconducting material which comes into contact with the stamp surface. As before, the stamp is peeled away once the semiconducting material has stabilized.

Another useful stamping method is called microtransfer molding (µTM) [30]. In this process the semiconducting material is directly applied to the stamp surface. Once the surface is fully covered, the stamp is inverted onto the substrate surface where the material then solidifies. The stamp can then be peeled away leaving the negative of the pattern.

One final method of fabrication with PDMS is micromolding using capillary action (MIMIC) [30]. This process is quite different from the previous because the dry stamp is first placed onto the bare substrate. Then, the semiconducting material is placed next to an opening in the stamp where capillary action will draw it into the empty channels [29]. Figure 1.13 shows patterns created using the MIMIC soft lithography technique. The unfortunate drawback to this method is the amount of time it takes for the semiconducting material to be drawn into all regions of the stamp.
Soft lithography has been used to make many devices. In many cases it has replaced photolithography steps altogether. Due to the reusable nature of the stamps it has greatly decreased the time necessary to repeat lithography steps in multilayer transistors. Furthermore, the stamps are able to replicate sizes down to 30 nm which is comparable if not better than ultraviolet photolithography processes [30].
Transistors fabricated using spin coat thin films have typically shown smaller mobilities than the evaporated forms of the same materials. For example, for pentacene, mobilities ~0.015 cm²/V·s have been reported for spin coated films [10] versus 2.4 cm²/V·s for single crystals films [3]. The reason for this will be explained further in chapter two.

Figure 1.13 Patterns created using MIMIC soft lithography techniques [29].
1.4.3 Ink Jet Printing

Organic deposition methods have also been borrowed from other technologies. Several groups such as Motorola, Philips Electronics, Plastic Logic and others have been researching the use of modified ink jet printers to pattern organic transistors [9, 32]. In this procedure highly purified organic materials replace the inks in ink-jet printer cartridges (see Figure 1.12). A computer aided drafting (CAD) program is used to design the opposing layers and interconnects of the transistor. Once the computer design is finalized, the printer can then “print” the layers, creating a transistor. A particular advantage of this process is the ability to print directly onto a transparency which acts as the flexible substrate. This exciting technology can allow anybody to quickly prototype a design and develop their own circuits. However, it is limited in scope to current ink-jet technology resolution. The highest resolution printers create droplets which are 1200 x 1200 dpi (dots per inch). This translates to a minimum geometry of 25 x 25 µm which is

![Figure 1.12](image)

Figure 1.12 Use of inkjet printing for semiconducting material deposition [6].
much larger than current cmos based micro processing technology. Furthermore because of the space between the print head and the substrate, there is difficulty in controlling the absolute edge resolution due to some splashing [32]. This creates further limitations on transistor geometries due to the difficulty in controlling the deposition of the material.

1.5 Organization of Thesis

This thesis is divided into five chapters. The first chapter has provided a discussion of the usefulness and current development of organic semiconductors. The second chapter introduces the physical structure as well as the electronic properties of pentacene organic semiconducting material, the material selected for study in this thesis. Analysis of the physical structure gives increased awareness towards optimizing the transistors. Furthermore, crucial modeling parameters, which tend to have various values in published papers, are discussed and appropriate values are identified for use in the device modeling. These are necessary to perform simulations with the Silvaco tools. The third chapter describes the device modeling software and illustrates the results that can be obtained for a typical device. The fourth chapter compares the results of the device modeling with published, experimental results for a series of pentacene-based organic MOSFETs. The last chapter discusses the limitations of the modeling and future directions that could be undertaken to more accurately model these organic MOSFETs and improve their design and performance.
References


Chapter 2

2.1 Introduction to Organic Semiconductors and Pentacene

Organic semiconductors can be organized into two categories. The first is plastics or polymers. The backbone of these materials is based on a repeating chain of hydrogen and carbon in varying configurations with other elements. Much work has been accomplished with these materials, but they have relatively poor mobilities ($10^{-4}$ cm$^2$/V·s$^{-1}$ [1]). The second group is based on short organic molecules called oligomers. Crystals of these materials are held together by weak van der Waal forces. Devices fabricated with these materials have been produced with the highest observed mobilities in organic semiconductors ($2.4$ cm$^2$/V·s$^{-1}$ [2]). However, these devices still do not have speeds comparable to traditional transistors based on inorganic semiconductors, such as silicon MOSFETs. But, the growing curiosity in organic transistors is not driven by an interest in replacing silicon devices, but rather in developing devices for especially low cost applications. Currently, research into the physics of these organic semiconducting devices is still immature but is progressing quickly.

Pentacene is one of the short molecule organic semiconducting materials that has received a great deal of attention [2]. Recent developments have yielded the highest charge carrier mobilities of any organic semiconductor [2]. Pentacene is derived from a group of materials called polyacenes. A characteristic of this group of materials is its structural formation. It begins with a carbon-carbon covalently bonded ring of six carbon atoms called benzene. As shown in Figure 2.1, every other carbon bond in the benzene ring is a double bond. Because carbon has four available electrons for bonding in its outer shell, one is used in a single C-C bond, two in a double C-C bond, and then the final electron is bonded with a dangling hydrogen
atom. Therefore, the final molecule is a ring of six carbons with a hydrogen atom attached to each carbon atom. Pentacene has five benzene rings bonded together (its structure can be seen in Figure 2.1) and therefore, its chemical formula is C_{22}H_{14}.

### 2.2 Physical Properties of Pentacene

The lattice constant of a semiconducting crystal is a very important property to know. In the case of most inorganic semiconductors, the lattice constant is identical in all three directions due to its cubic symmetry. However, Pentacene is a long and narrow molecule and it takes the triclinic crystal structure. Therefore, its structure is described by three separate lattice constants (a,b,c) and three angles (α,β,γ). Table 2.1 shows the lattice constants and other physical properties of the pentacene in the single crystal form.
Ordinarily, the primary concern for knowing the lattice constant of a material is for material deposition onto another material. Inorganic semiconductors such as InGaAs must be epitaxially grown on another material of the same lattice constant, e.g. InP, to avoid formation of crystal defects, which are detrimental to device performance and fabrication yield. Mismatch in the lattice constant causes a strain in the growing layer. This allows for only a thin layer of growth before crystal deformation and defects form, which relaxes the crystal strain. However, when growing a layer of organic semiconducting material, there is no need to be constrained by such rules. Alignment of small molecule organics with another layer is too complex to try to achieve. In practice, thin films of organic semiconductors are amorphous or at best polycrystalline. For this reason lattice matching of organic materials is not of primary concern and leads in practice to organic semiconductor deposition on metal, glass or plastic substrates.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Pentacene $\text{C}<em>{22}\text{H}</em>{14}$</th>
</tr>
</thead>
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<tr>
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</tr>
<tr>
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<tr>
<td>$b$, Å</td>
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<td>$\gamma$, °</td>
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<td>692</td>
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<tr>
<td>$z$</td>
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</tr>
<tr>
<td>$d_{\text{calc}}$, g/cm³</td>
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<tr>
<td>$d_{\text{exp}}$, g/cm³</td>
<td>1.32</td>
</tr>
<tr>
<td>$M$, daltons</td>
<td>278.36</td>
</tr>
</tbody>
</table>

Notations: $a,b,c$, lattice constants; $\alpha, \beta, \gamma$, bond angles; $V$, unit cell volume; $z$, number of molecules in a unit cell; $d$, density; $M$, molecular weight.
However, there are reasons for knowing the lattice constants of a material, which will be discussed shortly.

Bonding between the molecules in an organic semiconductor such as pentacene is a product of the van der Waal forces between the hydrogen atoms, which are dangling on the ends of the benzene rings. Figures 2.2 and 2.3 give a pictorial view of van der Waal forces and molecular bonding. Van der Waal forces are thought to be caused by induced dipole moments between adjacent molecules [4]. These forces are much weaker than the covalent bonds that hold together the atoms in traditional inorganic semiconductors such as GaAs. The bonding energy of van der Waal forces is approximately $10^{-2}$ eV [4], while covalent forces are in the range of 2-4 eV [5]. Van der Waal bonding creates a weaker, less rigid material than covalent forces i.e. amorphous or polycrystalline in structure. These weak forces are the dominant cause of low mobility and other characteristics, to be discussed shortly, which make transistors based on organic materials slow and difficult to model.

Figure 2.2 Depiction of molecular bonding by van der Waal forces [5].
Figure 2.3 Depiction of van der Waal forces in another molecule in the polyacene family, anthracene [5].
2.3 Band Structure

The energy band structure of organic semiconductors is different from that of inorganic, single crystal semiconductors such as silicon and GaAs. This is due to the amorphous structure of the organic semiconductors. It is also a function of the effects of polarons and thermal energy in the lattice [5]. In typical semiconductors, the electrons transition from the valence band to the conduction band once they have obtained enough thermal energy from collisions with phonons. Then they are relatively free to move about the semiconductor under the influence of an applied electric field to form a charge current. However in organic systems, the conduction band of numerous, closely spaced states as in a crystalline inorganic semiconductor such as silicon is replaced with fewer, more discrete excited states. The charge carriers in organic semiconductors are heavy quasi-particles called molecular polarons. Polarons are created when a negatively charged electron is localized by a strong dipole moment in the molecule. These dipole moments are typically the result of a deformation in the molecule as a result of phonon vibrations [5]. It is thought that carriers move in conjunction with these polarons and form a charge current by tunneling through the band gap or by hopping between adjacent sites or nearby molecules [6]. Only at low temperatures will the conduction band-like characteristics of the organic semiconductor be evident due to the lowering of the lattice vibrations. A further discussion of polarons can be found in section 2.6.
In an impurity free lattice the energy gap is controlled by the polaron transitions in the structure [6]. Electrons can possess two states within the confines of the polaron. One is that of the ground or unexcited state and the other that of an excited state. The transition from the ground state to the conduction band or ionic state is called the adiabatic energy gap \( (E_G^{Ad}) \) as shown in Figure 2.4. This is the traditional band gap used to model inorganic semiconductors. Silinish determined the adiabatic energy gap by using the threshold function of intrinsic photoconductivity of pentacene [5]. The second transition is from the excited state to that of the

![Energy band diagram of pentacene](image)

**Figure 2.4** Energy band diagram of pentacene. The left side gives a reference level of the energy gap to the ionized states of the molecule. The right side shows the energy gap relationship to the vacuum level. [5]
ionic state. This is called the optical energy gap \( E_G^{\text{opt}} \) and has been studied by electromodulation techniques by Sebastian et al. \[3\]. According to Figure 2.4, the adiabatic energy gap can be deduced as 2.47 eV while the optical energy gap can be deduced as 2.83 eV.

Energy is needed to create a molecular polaron. This energy originates from the thermal energy in the lattice. The energy \( E_b \) necessary to create a molecular polaron is reflected in the equation (2.1) and can been seen in Figure 2.4 \[5\].

\[
E_b = \frac{E_G^{\text{opt}} - E_G^{\text{Ad}}}{2}
\] (2.1)

In an ideal organic molecule crystal with no thermal lattice energy present, absolute zero temperature, molecular polarons would not exist. However, at finite temperatures molecular polarons exist and are the result of displacement of ions due to the negatively charged electron, i.e. deformations in the molecules created by the presence of a trapped electron. The amount of energy needed to create these deformations which lead to molecular polarons is \( E_b \) \[5\]. This energy is different yet complimentary to the energy band gap. Once the deformations are created and trap an electron, the amount of energy needed to release the trapped electron is the energy band gap. Summarized in Table 2.2 are the energy bandgaps reported in the literature including both theoretically calculated and experimentally measured values.

Sebastian and Weiser have also studied the band gap of pentacene crystals and reported it to be 2.12, 2.27 and 2.34 eV as shown in Table 2.2 \[7\]. The differences arise from the crystallographic direction of the electron transition between the molecules. Pentacene is non-cubic and has three separate lattice constants and therefore, three energy gaps which are associated with these directions. In determining the appropriate energy gap for simulation purposes, the value of 2.25 eV was chosen as an average. Simulations performed with Silvaco
did not show any significant deviation in results between the lowest and the highest values reported for the band gap.

<table>
<thead>
<tr>
<th>Value</th>
<th>Type</th>
<th>Method</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.12</td>
<td>Adiabatic</td>
<td>Measured</td>
</tr>
<tr>
<td>2.27</td>
<td>Adiabatic</td>
<td>Measured</td>
</tr>
<tr>
<td>2.345</td>
<td>Adiabatic</td>
<td>Measured</td>
</tr>
<tr>
<td>2.47</td>
<td>Adiabatic</td>
<td>Measured</td>
</tr>
<tr>
<td>2.46</td>
<td>Adiabatic</td>
<td>Calculated</td>
</tr>
<tr>
<td>2.83</td>
<td>Optical</td>
<td>Measured</td>
</tr>
<tr>
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<td>Calculated</td>
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<tr>
<td>1.85</td>
<td>-</td>
<td>Measured</td>
</tr>
</tbody>
</table>

2.4 Electron Affinity

Another important parameter which can be deduced from the energy band diagram is the electron affinity. The electron affinity is the energy needed for an electron to move from the conduction band to the vacuum level of the molecule. Figure 2.4 shows the electron affinity as the energy difference between $M_p$ and the top reference energy level 0. Usually this value is not of primary importance when modeling MOSFET transistors because there is no need for energy level alignment between materials, i.e. such as when modeling heterojunction bipolar transistors. However, studies have shown that when a metal is deposited above the organic material an energy barrier is formed at the interface [8-11]. Therefore, when modeling bottom contact transistors it is necessary to align the work function of the metal with the electron affinity of the organic semiconducting material in order to determine the height of the barrier at the source and drain contacts. Table 2.3 lists several reported values of pentacene’s electron affinity measured from devices based on deposition of pentacene on different metallic materials. For modeling of
pentacene organic transistors using Silvaco, the value of 2.49 eV was used based on the extensive research performed on pentacene organic semiconductors by Silinish et al. [5].

<table>
<thead>
<tr>
<th>Value (eV)</th>
<th>Method</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.49</td>
<td>Single Crystal Pc Diode</td>
<td>[5]</td>
</tr>
<tr>
<td>3.22</td>
<td>Bandgap alignment with Au</td>
<td>[8]</td>
</tr>
<tr>
<td>3.56</td>
<td>Bandgap alignment with SnS$_2$</td>
<td>[8]</td>
</tr>
</tbody>
</table>

2.5 Electron and Hole Mobilities

The mobility is the electrical determination of the speed and ability of a charge carrier to move inside a semiconducting material in response to an electric field. Organic versus inorganic semiconductor mobilities do not begin to compare. Silicon’s electron mobility is 1500 cm$^2$/V$^{-1}$s$^{-1}$ at low doping levels, while mobilities for holes are much smaller at 800 cm$^2$/V$^{-1}$s$^{-1}$ [8]. By comparison, these mobilities are orders of magnitude larger than the highest value reported for holes in pentacene, which is 2.4 cm$^2$/V$^{-1}$s$^{-1}$. There are many causes for this smaller mobility, but the amorphous nature of the organic material and the weak nature of the van der Waal forces are the primary reasons. At room temperature, there is a certain amount of thermal energy which resides in the lattice and is present in the form of lattice vibrations or phonons. In conventional semiconductors such as silicon, phonons cause scattering of the electrons as they travel through the lattice, thereby decreasing the length of the path between collisions causing redirection of the electrons. Once electrons undergo scattering they lose energy to the collisions, slow down and are deflected from their direction of acceleration opposite the direction of the applied electric
field. As a result, the mobility increases as the lattice thermal energy and temperature are decreased since the density of phonons scales with the temperature. Because the organic semiconductor is held together by weak van der Waal forces instead of covalent forces and the structure of the material is amorphous or polycrystalline, the transport process is less clear and hopping of electrons from one localized site to an adjacent one may be a more accurate description. Research groups at the Institute of Physics and Energetics and Physicalisches Institut have studied the effect of cooling pentacene and other polyacenes to extremely low temperatures [6, 13, 14]. They found that as the temperature decreases, the measured mobility increases with a power dependence $\mu_0 \sim T^{-\eta}$ at low temperatures where $\eta \approx 2.1$, as seen in Figure 2.5. This phenomenon has drawn attention to low temperature organic semiconductors as possible superconductors [2]. The study of the mobility’s temperature dependence may ultimately help to unravel the mechanism of charge transport. However, cooling semiconductor circuits to low temperatures increases their costs dramatically, which negates a primary motivation for developing devices based on these organic semiconductors.
Because organic materials are primarily p-type, the hole mobility is a very important parameter to incorporate into any modeling program. This mobility in organic semiconductors is quite difficult to model and predict because it is a strong function of the fabrication history of the sample. This may be due in part to the irregular nature of the material’s structure. For example, the grain size in polycrystalline thin films will depend strongly on the deposition conditions. Table 2.4 gives several of the values for fabricated pentacene MOSFETs reported by different research teams. Thermally grown pentacene creates a highly structured, single crystal, which therefore has a higher hole mobility [2]. But in practice, spin coating a pentacene precursor
material followed by heating to allow for material conversion will produce a pentacene thin film with a much lower mobility [15]. Even this process of material conversion consists of a trial and error situation to find an optimum annealing time. The method of ink jet printing is expected to produce thin films with a similar mobility to that of spin coating because it results in a similar amorphous material. To further complicate things, the hole mobility has also been observed to be a function of substrate selection [16]. Because of the rigidity and smoothness of a silicon substrate, it allows for much higher mobilities (0.3 – 0.6 cm²/V⁻¹s⁻¹ [16]) than a rougher plastic substrate (10⁻⁴ cm²/V⁻¹s⁻¹ [1]). Silicon will also withstand higher and longer annealing processes than plastic substrates which will ultimately enable higher mobility values.

<table>
<thead>
<tr>
<th>Mobility (cm²/V⁻¹s⁻¹)</th>
<th>Deposition Type</th>
<th>Underlying Material</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.23</td>
<td>Vacuum Deposition</td>
<td>Oxide/SAM</td>
<td>[2]</td>
</tr>
<tr>
<td>0.22-1.2</td>
<td>Thermal Evaporation</td>
<td>Oxide/SAM</td>
<td>[9]</td>
</tr>
<tr>
<td>0.38-0.6</td>
<td>Vacuum Deposition</td>
<td>Oxide</td>
<td>[17]</td>
</tr>
<tr>
<td>0.3-0.6</td>
<td>Thermal Evaporation</td>
<td>Thermal oxide</td>
<td>[16]</td>
</tr>
<tr>
<td>0.25-0.55</td>
<td>Thermal Evaporation</td>
<td>Flat Si₃N₄</td>
<td>[16]</td>
</tr>
<tr>
<td>0.03</td>
<td>Spin Coat</td>
<td>Oxide</td>
<td>[18]</td>
</tr>
<tr>
<td>0.02</td>
<td>Precursor Material</td>
<td>Oxide/Primer</td>
<td>[15]</td>
</tr>
<tr>
<td>10⁻²-10⁻³</td>
<td>Thermal Evaporation</td>
<td>Rough Si₃N₄</td>
<td>[16]</td>
</tr>
<tr>
<td>0.0004</td>
<td>Spin Coat</td>
<td>Oxide</td>
<td>[18]</td>
</tr>
</tbody>
</table>

Electron mobilities in organic materials have been under investigation for only the past ten years compared to almost forty years for p-type materials [2]. Because the research of n-type materials is still in its early stages, there are fewer reported values for electron mobilities. Dimitrakopoulos et al. [2] have reported several lab-created n-type materials and their electron mobilities, which can be seen in Table 1.2 shown previously. Electron mobilities are quickly
approaching reported hole mobilities; even n-type pentacene has been reported to have a mobility of 0.5 cm$^2$/V·s [2].

2.6 Charge Carriers as Polarons

In organic materials charge carriers move as heavy quasi particles called polarons [5]. Polarons are comprised of an electron coupled with an electronic dipole induced in the lattice or molecular structure by the charge repulsion and attraction of the electron with nearby ions. There are two dominant types of polarons in organic semiconductors: small molecular and lattice. Small molecular polarons originate from vibrations in the lattice structure while lattice polarons are caused by much stronger forces such as structural defects and impurities. Electrons are present as an electron cloud surrounding the dipole which together forms a heavy quasi-type particle. Modeling of carrier movement in conjunction with lattice polarons involves describing potential barriers and quantum well traps. When electrons gain sufficient energy, they are released from their dipole partner and can travel in the lattice to an adjacent trap. However, they lose their energy very quickly due to the vibronic nature of the lattice and collisions with phonons. The actual mean free path of an electron in organic semiconductors has been measured to be nearly the same as the lattice constant [7]. This is much different than the case in conventional semiconductors where charge carriers can travel many lattice constants before undergoing a collision. Translation of carriers by this trap and release mechanism in organic semiconductor, leads to the hopping model, which is quite popular in describing transport in organic materials. This model states that electrons hop from one lattice polaron trap (see Figure 2.6) to another instead of freely moving through the semiconductor’s lattice. For amorphous semiconductors, the picture is more complicated. If charge transitions were only based on these
lattice polarons, the mobility would be a function of thermal activation which has been proven to not be the case in pentacene [6, 18]. On the other hand, charge carrier movement involving molecular polarons entails travel by tunneling through the band gap. Silinish suspects that the mobility in organic semiconductors is a combination of transport by both lattice and small molecular polarons [6].

For purposes of this thesis, we will incorporate the extracted mobility reported by each author for simulation of the individual fabricated devices. However, close inspection of Table 2.4 presents an average value of pentacene’s mobility for thermal deposition of pentacene as \( \sim 0.3 \text{ cm}^2/\text{V.s} \). Average values of mobilities using precursor spin coating methods yield values of a magnitude or more lower (i.e. \( \sim 0.03 \text{ cm}^2/\text{V.s} \)).

2.7 Permittivity

The importance of a material’s permittivity can be overlooked at times. The permittivity is a material’s capacitative ability, which can be interpreted to mean a material’s tendency to fit
into one of two categories: conductors or insulators. Insulators tend to have low permittivities while conductors have large values. Semiconductors fall in-between the two extremes. Frequently, the permittivity of a material is stated in terms of its comparison to that of the permittivity of air (8.85E-14 F/cm) [12], i.e. as a relative permittivity. Therefore, silicon dioxide, which is a typical insulator, has a permittivity of 3.8 while silicon’s is 11.8. By comparison, pentacene has been found to have a permittivity of 4 [7], which creates the illusion that it is an insulator. Though it and other organic materials have exhibited insulator qualities in the past, high enough voltages prove they can be categorized with other semiconducting materials.

2.8 Doping

Pentacene and many other organic materials are different from inorganic semiconductors in that they are intrinsically doped. There is no need to submit the material to ion implantation or diffusion because there are already typically enough active acceptor ions to call it a p-type material. N-type material is much more difficult to produce and has a poorer performance, i.e. a lower mobility. The actual origin of these acceptors in p-type organic semiconductors is not known, but could possibly be related to the large effective masses of the material [5]. Measuring the number is acceptors must be done through analysis of fabricated devices since a controlled impurity implanting process is not used to dope them. Shown in Table 2.5 is the range of values reported for the doping level in p-type pentacene.
Brown et al. deduced the acceptor density from the gate voltage at the observed pinch off of the current in MOS devices [21]. From there they used equation (2.2) to determine the acceptor density from the depletion width $W$ and the capacitance $C_i$.

$$ W = \frac{\varepsilon_s}{C_i} \left[ \left( 1 + \frac{2C_i^2V_g}{qN_a\varepsilon_s} \right)^{1/2} - 1 \right] $$

(2.2)

This leads to an acceptor density of $2.0 \times 10^{17}$ cm$^{-3}$.

Yang et al. [20] determined the number of acceptors by creating a 400nm thick pentacene capacitor and measuring its capacitive-voltage (C-V) characteristics. A fit of the data was then used in conjunction with an equivalent circuit model and other data to calculate an acceptor level of $1.7 \times 10^{16}$ cm$^{-3}$ [20]. However, Yang used a permittivity of 6.7 for pentacene to determine the doping level. This is different from the permittivity of 4 which was reported by Silinish [7].

### 2.9 Band Gap Defects

Control of defect formation has long been a concern in inorganic semiconductor material preparation. Organic semiconductors are no strangers to material defects. It has been widely reported that organic semiconductors contain many defects in them that cause extra electronic states within the band gap. For amorphous materials, these defects are more numerous. Structural defects in the lattice can contribute to them, but elemental impurities such as oxygen and nitrogen can also be a primary cause. Determining the energy level and density of the impurities is a particular concern because of its ultimate effects on the band gap and charge
transport. Silinish et al. used thermally modulated space-charge limited current (TM SCLC) methods to measure the defects in pentacene samples [22, 23]. The results of his study are listed in Table 2.6.

<table>
<thead>
<tr>
<th>Energy (eV)</th>
<th>Density (cm⁻³)</th>
<th>Energy (eV)</th>
<th>Density (cm⁻³)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.35±0.05</td>
<td>3X10¹⁴</td>
<td>1.08</td>
<td>9.6X10¹⁴</td>
</tr>
<tr>
<td>0.28±0.05</td>
<td>4X10¹⁴</td>
<td>0.31</td>
<td>6.5X10¹⁵</td>
</tr>
<tr>
<td>0.21±0.03</td>
<td>1X10¹⁵</td>
<td>0.24</td>
<td>4.2X10¹⁵</td>
</tr>
<tr>
<td>0.06±0.02</td>
<td>4X10¹⁵</td>
<td>-0.69</td>
<td>2.6X10¹⁴</td>
</tr>
</tbody>
</table>

Further studies have been performed by Yang et al. [20] who used capacitive methods with deep-level transient spectroscopy (DLTS). Street et al. extrapolated their density values from the Levinsen plots of the threshold voltage of two fabricated pentacene bottom contact MOSFET transistors [17]. Both of these results are also presented in Table 2.6. Both studies show the largest density of defects around 0.25 eV at nearly the same densities. These densities and energies are known to be specific to elemental defects such as oxygen and nitrogen when they combine with pentacene [20].

Frequently, defects are modeled using a Gaussian distribution of defects which is centered at a discrete energy level in the energy bandgap. The probability of finding a defect is much larger at the peak and then tapers off in an exponential fashion at lower and higher. These defect-created extra states in the band gap allow the charge carriers to move by tunneling
through the band gap. But this tunneling decreases our ability to predict the charge current properties of the semiconducting material since the extent of the presence of these defects is frequently unknown. Figure 2.7 shows a representation of these effects in the band gap of the material. Typically, defects are located close to the valence and conduction band edges. However, defects can also reside in the middle of the band gap. Both studies by Silinish [22] and Yang [20] fail to show deep defect levels which are close to the midpoint of the energy band gap. Impart, this is because the resolution of both methods becomes too difficult to discern at deep defect levels.

Figure 2.7  Defects in the energy gap evolving from structural defects and impurities [5].
2.10 Effective Mass of Holes and Electrons

Because of the rather small mobilities of holes in pentacene crystals, it can be anticipated that the effective mass of holes in that material will be quite large. In studies carried out by Silinish, he determined that this was in fact the case and that the effective mass of hole charge carriers was temperature dependent and follows Equation (2.3) [24].

\[ m_{\text{eff}}(T) = m_{\text{eff}}^0 \exp \left( \frac{T}{T_o} \right) \]  

(2.3)

In this equation \( m_{\text{eff}}^0 \) is the effective mass of the hole charge carrier at zero temperature, \( T \) is the operating temperature and \( T_o \) is a characteristic constant. This equation shows the effective mass dramatically increases as the temperature increases. Silinish et al. found the effective mass of hole charge carriers to be approximately 100 to 1000 \( m_o \) in naphthalene organic semiconductors at low to mid temperatures (as seen in Figure 2.8) [5], where \( m_o \) is the free mass of an electron. At room temperature the effective mass of the hole charge carriers reached \( 10^4 m_o \) [5]. The effective mass was measured in the low temperature regime from the saturation drift velocity temperature dependence. While in the high temperature regime, it was determined from microscopic mobility measurements. Although these results are for naphthalene, the structure of this molecule consists of the same benzene rings and is therefore quite similar to pentacene. Therefore, it can be assumed that the effective mass of pentacene positive and negative charge carriers will follow the same basic trends set forth by naphthalene. Because of the strong interest in transistors based on low cost, room temperature organic semiconductors, a value of \( 10^4 m_o \) was chosen to represent the hole effective mass in pentacene for use in the Silvaco simulations for this thesis.
Further analysis of the effective mass can yield the carrier mean free path ($l_o$) using Equation (2.4) [6]

$$m_{\text{eff}}(T) = \frac{3e^2l_o}{a^2k_B} * T^{2n-1}$$  

(2.4)

where $l_o$ is the carrier mean free path, $k_B$ is Boltzmann constant, $e$ is the charge on the electron, $T$ is the operating temperature, $n$ is a material based constant, and $\alpha$ is a constant. As the temperature decreases, the carrier mean free path will increase, thereby increasing the overall mobility of the material (as seen in Figure 2.8). However, at room temperature the carrier mean free path ($l_o$) is on the order of the lattice constants for the pentacene material is listed in Table 2.1 [6].
Because pentacene is traditionally a p-type material, the effective mass of holes is of higher interest for device modeling than that of electrons. However, studies by Silinish have shown negative charge carrier polarons in napththalene to have an even higher effective mass than holes (as seen in Figure 2.9). This could account for their even slower transit time [24]. Typically, values for the electron effective mass are equal or larger than that of holes (i.e. $10^4 m_o$ versus $\sim 10^3 m_o$ for holes).

![Figure 2.9 Effective mass ($m^*$) of negative molecular polaron charge carriers (MP$^-$) in Napthalene organic semiconducting material [5].]

2.11 Effective Density of States

The effective density of states depends on the effective mobility and is an important quantity for device modeling calculations. Therefore, it is important to know this constant before attempting simulations. Furthermore, the effective mass is temperature dependent, similar to the
mobility. Therefore, the appropriate value must be chosen. The effective densities of states for the valence and conduction band are given by,

\[ N_v = 2 \left( \frac{2\pi m_{dh} k_B T}{\hbar^2} \right)^{3/2} \]  \hspace{1cm} (2.5)

\[ N_c = 2 \left( \frac{2\pi m_{de} k_B T}{\hbar^2} \right)^{3/2} M_c \]  \hspace{1cm} (2.6)

where \( m_{dh} \) is the effective mass of holes, \( m_{de} \) the effective mass of electrons and \( M_c \), which is the number of brilloquine zones is chosen to be one [12]. From the determined effective masses chosen above (10^4 \( m_0 \)), the effective density of states for the valence band is \( (N_v) \) and conduction band \( (N_c) \) were calculated at room temperature to be:

\[ N_v = 2.5 \times 10^{25} \text{ cm}^{-3} \]

\[ N_c = 2.5 \times 10^{25} \text{ cm}^{-3} \]

These values are much larger (orders of magnitude) than conventional semiconductors (\( \sim 10^{19} / \text{cm}^3 \)) due to the large effective masses. The much larger \( N_v \) does not mean that there will be an increase in the current density. When this value becomes exceedingly large, the over abundance of hole states can create extra collisions. This can reduce or limit the charge flow in the semiconductor and thus, decreasing the carrier mean free path lowering the mobility.
2.12 Summary of Material Parameters

A summary of pentacene material parameters discussed in the previous sections is listed in Table 2.7. These parameters are the ones incorporated into the simulations for pentacene semiconducting transistors discussed later on in this thesis.

Table 2.7 Summary of material parameters for pentacene.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Pentacene</th>
<th>C\textsubscript{22}H\textsubscript{14}</th>
</tr>
</thead>
<tbody>
<tr>
<td>Crystal Structure</td>
<td>Triclinic</td>
<td>[5]</td>
</tr>
<tr>
<td>Lattice Constants (Å)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>A</td>
<td>7.90</td>
<td>[5]</td>
</tr>
<tr>
<td>B</td>
<td>6.06</td>
<td>[5]</td>
</tr>
<tr>
<td>C</td>
<td>16.01</td>
<td>[5]</td>
</tr>
<tr>
<td>Permittivity</td>
<td>4</td>
<td>[7]</td>
</tr>
<tr>
<td>Energy Band Gap (eV)</td>
<td>2.25</td>
<td>[7]</td>
</tr>
<tr>
<td>Electron Affinity</td>
<td>2.49</td>
<td>[5]</td>
</tr>
<tr>
<td>Intrinsic p-type doping</td>
<td>2X10\textsuperscript{17}</td>
<td>[21]</td>
</tr>
<tr>
<td>Defect Energy (eV) &amp; Densities (cm\textsuperscript{3})</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.35±0.05</td>
<td>3X10\textsuperscript{14}</td>
<td>[22]</td>
</tr>
<tr>
<td>0.28±0.05</td>
<td>4X10\textsuperscript{14}</td>
<td>[22]</td>
</tr>
<tr>
<td>0.21±0.03</td>
<td>1X10\textsuperscript{15}</td>
<td>[22]</td>
</tr>
<tr>
<td>0.06±0.02</td>
<td>4X10\textsuperscript{15}</td>
<td>[22]</td>
</tr>
<tr>
<td>Effective Hole Mass (m\textsubscript{h})</td>
<td>10\textsuperscript{4} m\textsubscript{0}</td>
<td>[6]</td>
</tr>
<tr>
<td>Effective Electron Mass (m\textsubscript{e})</td>
<td>10\textsuperscript{4} m\textsubscript{0}</td>
<td>[6]</td>
</tr>
<tr>
<td>Effective Valence Band Density of States (N\textsubscript{v}) (cm\textsuperscript{3})</td>
<td>2.5X10\textsuperscript{25}</td>
<td></td>
</tr>
<tr>
<td>Effective Conduction Band Density of States (N\textsubscript{c}) (cm\textsuperscript{3})</td>
<td>2.5X10\textsuperscript{25}</td>
<td></td>
</tr>
</tbody>
</table>

The hole mobility is not included in this table because it is a parameter which is strongly dependent on the method of fabrication. For the individual transistor simulations the hole mobility reported in the literature was directly applied to that particular simulation.
2.13 Conclusion

A search of the literature was performed to obtain the material parameters for the pentacene organic semiconducting material and the results summarized in this chapter. Values were reported for the energy band gap, permittivity, effective mass of holes and electrons, lattice constants, electron and hole mobilities and the energy levels and their densities for defects. The effective density of states for the conduction and valence bands were also calculated. Results from incorporating these parameters into the Silvaco simulator and device modeling for p-channel MOSFETs are reported in the following chapter.
References


Chapter 3

3.0 Simulation of Pentacene Organic MOS Transistors and Model Verification

This chapter summarizes the software tools and computer simulations used to model p-channel MOSFETs based on pentacene organic semiconducting material. Reported results from three groups who have fabricated pentacene-based metal-oxide semiconducting field effect (MOSFET) transistors were used to compare with our computer simulations. The authors used various methods to deposit the pentacene material and two different orientations of the physical layout of the device. These deposition methods and design differences will be discussed further in the chapter. The purpose of developing the pentacene-based MOSFET model through comparison with the published experimental results for fabricated transistors is to optimize pentacene organic transistor design by developing a better understanding of the factors limiting the device’s performance.

3.1 Simulation Procedure

The simulator used for this device modeling is Silvaco’s ATLAS (version 3.12.0R) [1]. ATLAS is a general, two-dimensional semiconductor device simulator which incorporates the physics that govern charge carrier transport and applies it to the dimensions of the device being studied. The procedures of an ATLAS simulation are typically divided into three sections: physical structure and mesh specification, device material parameters, and operation requirements. While ATLAS is typically used as a 2-Dimensional simulator (length and thickness), it also incorporates an option which allows the user to specify the third dimension (e.g. channel width for a MOSFET). This is quite useful for organic devices because they
typically are very large in comparison with inorganic devices such as silicon or GaAs. However, some organic devices have widths as large as 20 mm, which would drastically increase the number of nodes or grid points needed and the amount of time consumed to simulate a device in three dimensions [2, 3]. Fortunately, the MOSFET current is directly proportional to the width of the channel. This allows Silvaco to simulate a device with a default width of 1µm and multiply the results by the measured width to achieve the correct current-voltage characteristics.

3.1.1 Device Structure and Mesh Specification

To begin a simulation, the physical structure and dimensions of the device must be defined including the locations of the electrical contacts. Shown in Figure 3.1a is the cross section for a top contact pentacene based MOSFET and (b) a closeup of the channel region. Once the main features, materials, and dimensions are described, the internal regions must be broken down into a mesh. The mesh is comprised of a complex grid of triangles where the simulation entails the calculations of the results at each node (triangle corner). The density of the triangles can vary depending on the complexity of the physics of the region of the device being studied. For instance, the oxide-semiconductor boundary is a common place for carrier accumulation and transport to occur. Therefore, the density of the mesh will be quite high at this location compared to other regions. The bulk region of the substrate is a low activity area and will therefore consist of a lower density mesh. Mesh definition is a function of the program which needs to be optimized. A poorly defined mesh can give inaccurate results, while a mesh which is too dense will increase the run time of the simulation. Furthermore, there is an upper limit to the amount of mesh points which can be defined for the simulation to run. Other mesh considerations will be discussed in the contact resistance section of chapter four. Figure 3.2
shows the user defined mesh for one of the devices which was chosen for simulations from the literature [4]. A zoomed region of the mesh around the source electrode reveals the increased density of the triangles in the semiconducting material compared to that of the oxide.

Figure 3.1  (a) Cross section of a top contact pentacene organic MOSFET in ATLAS and (b) close up of the channel region and source/drain electrodes.
Figure 3.2  (a) Physical mesh of a pentacene MOSFET simulated in ATLAS, and (b) zoom of mesh at source electrode.
3.1.2 Device Physics Equations

The mesh density is important because it defines where the charge carrier densities within the device will be calculated. These charge carrier densities are figured by simultaneously solving the fundamental device equations including [5]: Poisson’s equation, continuity equations for electrons and holes, charge transport equations and defect density equations. The first three equations are the default equations which ATLAS uses to determine the device’s electrical characteristics.

Poisson’s equation determines the electric fields ($\vec{E}$) within the device based on the distribution of charges, both mobile and fixed, within the device as given by Equation (3.1),

$$\nabla \cdot \vec{E} = \frac{\rho(x,y)}{\varepsilon} \quad (3.1)$$

where $\varepsilon$ is the permittivity of the region, and $\rho(x,y)$ is the charge density given by,

$$\rho(x,y) = q[p(x,y) - n(x,y) + N_D^+(x,y) - N_A^-(x,y)] \quad (3.2)$$

where $p(x,y)$ = hole density, $n(x,y)$ = electron density, $N_D^+(x,y)$ = ionized donor density, and $N_A^-(x,y)$ = ionized acceptor density. Wherever a buildup of charge occurs, an electric potential is created which effects the electric field distribution and current flow. In a MOS structure the interface at the oxide and semiconductor is of primary importance. The voltage applied on the gate electrode creates an electric field which attracts the minority or majority carriers. Furthermore, for a MOSFET the voltage potential between the source and drain sets up another electric field along the channel which drives the charge carriers and produces the current flow.
The continuity equations describe the dynamics of charge carrier distribution over time as seen in Equations (3.3) and (3.4). In these equations \( q \) is the magnitude of the charge of an electron, \( n \) is the electron carrier density, \( p \) is the hole carrier density, \( J \) is the respective current density, \( G \) is the respective charge generation rate, and \( R \) is the respective charge recombination rate.

\[
\frac{\partial n}{\partial t} = \frac{1}{q} \nabla \cdot \vec{J}_n + G_n - R_n \quad (3.3)
\]

\[
\frac{\partial p}{\partial t} = \frac{1}{q} \nabla \cdot \vec{J}_p + G_p - R_p \quad (3.4)
\]

For the organic MOSFETs, no optical absorption is present so the generation and recombination terms simplify and the material’s characteristics are described by the minority carrier recombination lifetime. Since the MOSFET is a majority carrier device, the characteristics of the carrier generation and recombination are relatively unimportant.

The physics of organic semiconductors is governed by polaron creation and movement as mentioned in chapter two. Due to the complexity of the charged polaron behavior, the underlying physics of the transport is simplified using one major parameter, an effective carrier mobility. Since we are studying p-channel MOSFETs, which are a majority carrier device, and primarily their static (DC) characteristics, the hole mobility is the most important material parameter. Values for the hole mobility will be used which have been reported from experimental results. Since the mobility depends on the pentacene deposition process and conditions and the device geometry, i.e. top or bottom configuration, different mobilities will be employed for comparison with various devices.
A third important set of equation for describing the device physics are the charge carrier transport given by,

\[ \bar{J}_n = qn\mu_n F + qD_n \nabla n \]  \hspace{1cm} (3.5)

\[ \bar{J}_p = qn\mu_p F + qD_p \nabla p \]  \hspace{1cm} (3.6)

which contain both drift and diffusion components. These equations determine the current density of the charge carriers based on the mobility of the carrier (\(\mu\)), the electric field (E), the carrier densities (\(n, p\)), and the diffusion lengths of the carriers (D). The diffusion length of the carriers is related by Einstein’s relationship to the mobility by,

\[ D_n = \frac{kT}{q} \mu_n \]  \hspace{1cm} (3.7)

\[ D_p = \frac{kT}{q} \mu_p \]  \hspace{1cm} (3.8)

In summary, the ATLAS software simultaneously and self consistently solves Poisson’s equation, the continuity equations, and the current density equations at each node in the two-dimensional mesh for the given device structure and subject to the boundary conditions including the voltages applied at the contacts. Included in the solution is the electron and hole concentrations and the potential at each node. From these, the electric field distribution and the electron and hole current densities are calculated at each node and the terminal currents at the electrodes. Initially we are considering only the static (DC) characteristics of the device. When an ac component is added to the bias at the FET gate, ac currents can be calculated and ac parameters such as the transconductance are also calculated.
3.1.3 Material Parameters for Pentacene

ATLAS treats all semiconducting materials as silicon unless new parameters for the material are specified. This shows the importance of researching the material parameters for the pentacene organic material. Any undefined parameters will be assigned the corresponding default value belonging to silicon. For the pentacene employed in the MOSFETs studied here, these parameters were discussed and listed in chapter two. Table 3.1 restates these values which are incorporated into ATLAS for pentacene. Note that the hole mobility does not appear in the table since its value has been reported to vary considerably depending on the deposition conditions and the device geometry. When comparing the simulation results with reported device characteristics, the experimentally reported value for the mobility will be used in the device modeling.

<table>
<thead>
<tr>
<th>Material Simulation Parameters</th>
<th>Pentacene C$<em>{22}$H$</em>{14}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Permittivity</td>
<td>4 [6]</td>
</tr>
<tr>
<td>Energy Band Gap (eV)</td>
<td>2.25 [6]</td>
</tr>
<tr>
<td>Electron Affinity (eV)</td>
<td>2.49 [7]</td>
</tr>
<tr>
<td>Intrinsic p-type doping</td>
<td>2X10$^{17}$ [2]</td>
</tr>
<tr>
<td>Effective Hole Mass ($m_h$)</td>
<td>10$^4$ $m_e$ [8]</td>
</tr>
<tr>
<td>Effective Electron Mass ($m_e$)</td>
<td>10$^4$ $m_e$ [8]</td>
</tr>
<tr>
<td>Effective Valence band density of states ($N_v$) (cm$^{-3}$)</td>
<td>2.5X10$^{25}$</td>
</tr>
<tr>
<td>Effective Conduction band density of states ($N_c$) (cm$^{-3}$)</td>
<td>2.5X10$^{25}$</td>
</tr>
</tbody>
</table>

3.1.4 Thin Film Transistor Modeling

ATLAS provides a package called TFT (Thin Film Transistor) which allows simulation of devices based on amorphous or polycrystalline materials, such as organics or inorganic
materials such as amorphous silicon. Modeling of such thin film transistors requires that the simulator take into account the high number of defects in the amorphous semiconductor. As the defect level rises within a semiconductor, the current becomes drastically affected. This is because the defects disrupt the diffusion process and reduce the diffusion length of the charge carriers by trapping them. These traps correspond to localized energy levels within the semiconductor bandgap. For an amorphous semiconductor, they can exist with various (continuous range of) energy levels, densities and capture cross sections. To model this, Silvaco uses a distribution of defect states \( g(E) \) in the energy bandgap of the organic semiconducting material [1]. This density of states is described using a combination of gaussian distributions for midgap states and exponential decaying band tail states. It can be described using a sum of four distributions: gaussian donor \( (g_{GD}(E)) \), gaussian acceptor \( (g_{GA}(E)) \), conduction band donor tail states \( (g_{TD}(E)) \), and valence band acceptor tail states \( (g_{TA}(E)) \) as given by [1],

\[
g(E) = g_{TA}(E) + g_{TD}(E) + g_{GA}(E) + g_{GD}(E)
\]  

Silinsh et al. [9] and Yang et al. [10] have studied the distribution of defects within pentacene material and found it to be p-type with several gaussian acceptor-like distributions of states. Their studies have shown that there are no significant tail states or gaussian donor states. Therefore, the density of states given by (3.9) can be expressed as simply a gaussian distribution of states as shown in Equation (3.10). In this equation \( NGA \) is the total density of acceptor traps, \( E \) is the energy field, \( EGA \) is the central energy level of the defects, and \( WGA \) is the distribution width or decay energy of the trap.
\[
g(E) = g(E)_{GA} = N_{GA} \exp \left[ -\frac{(E - E_{GA})}{W_{GA}} \right]
\]  

(3.10)

In general, the effects of these defect traps is to trap electrons and holes and modify the density of electrons in the conduction band and holes in the valence band. The total density of trapped electrons \( n_T \) and trapped holes \( p_T \) is given by [1],

\[
n_T = n_{TA} + n_{GA}
\]

(3.11)
\[
p_T = p_{TD} + p_{GD}
\]

(3.12)

These equations also become simplified since only gaussian acceptor traps were reported in the pentacene material [7, 10]. So \( n_T = n_{GA}; n_{TA} = 0 \) and \( p_T = p_{GD} = p_{TD} = 0 \). Therefore, the only parameter left in the trap density equation is \( n_{GA} \), an acceptor-like trap concentration. An acceptor-like trap is one which is electrically neutral when empty, but negatively charged when filled (electron captured). Hence, it operates as a hole trap, capturing holes from the valence band making them immobile, or releasing them to the valence band where they become mobile. This \( n_{GA} \) is related to the probability of trap occupation \( f_{TGA} \) which is a function of its position in the energy gap and the electronic cross section of the trap and is expressed by,

\[
n_{GA} = \int_{E_v}^{E_c} g_{GA}(E) \cdot f_{TGA}(E, n, p) dE
\]

(3.13)

where \( g_{GA}(E) \) is the density of the acceptor-like traps given by (3.10). The probability of the traps occupation, \( f_{TGA}(E, n, p) \), is a function of the energy, the electron and hole carrier
concentrations as well as a function of its electron and hole capture cross sections as shown in Equation 3.14.

\[
f_{\text{fck}}(E, n, p) = \frac{v_n SIGGAE \cdot n + v_p SIGGAH \cdot n_i \exp \left[ \frac{E_j - E}{kT} \right]}{v_n SIGGAE \left( n + n_i \exp \left[ \frac{E - E_j}{kT} \right] \right) + v_p SIGGAH \left( p + n_i \exp \left[ \frac{E_j - E}{kT} \right] \right)}
\]  

Equation 3.14

In this equation \( SIGGAE \) is the cross section for capture of an electron by the acceptor trap, \( SIGGAH \) is the cross section of a hole by the acceptor trap, \( n_i \) is the intrinsic carrier concentration, \( n \) is the electron concentration, \( p \) is the hole concentration, and \( v_n \) and \( v_p \) are the electron and hole thermal velocities.

The parameters reported for pentacene for these equations are listed in Table 3.2. The electron and hole capture cross section values have not been reported in the literature for pentacene so the values reported for silicon have been used [11]. Electron acceptor capture cross sections employed was taken to be 1X10\(^{-16}\) cm\(^{-2}\) while that for holes was taken as 1X10\(^{-14}\) cm\(^{-2}\). For those variables in the equations where there was no reported value in the literature, the default values of silicon have been employed. Because each energy level has a separate density associated with it the equations mentioned in this section were applied to each distribution and then summed together by the thin film module of ATLAS.

Silinish et al. [9, 12] have reported four acceptor-like traps in pentacene. Recently, Yang et al. [10] have also reported measurements of donor-like trap levels and densities in pentacene. A trend in peak energies and densities can be seen in the reported values from the literature. It is likely that the differences which do exist result from differences in material fabrication methods.
Furthermore, the results published by Street et al. [13] were not as thorough as those reported by Silinish. The latest values reported by Silinish et al. [9] were used in the organic pentacene MOSFET simulation.

Table 3.2 Defect Trapping States in Pentacene

<table>
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<tbody>
<tr>
<td>Energy (eV)</td>
<td>Density (cm$^{-3}$)</td>
</tr>
<tr>
<td>0.35±0.05</td>
<td>3x10$^{14}$</td>
</tr>
<tr>
<td>0.28±0.05</td>
<td>4x10$^{14}$</td>
</tr>
<tr>
<td>0.21±0.03</td>
<td>1x10$^{15}$</td>
</tr>
<tr>
<td>0.06±0.02</td>
<td>4x10$^{15}$</td>
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<tbody>
<tr>
<td>Energy (eV)</td>
<td>Density (cm$^{-3}$)</td>
</tr>
<tr>
<td>0.47±0.02</td>
<td>7x10$^{14}$-2x10$^{15}$</td>
</tr>
<tr>
<td>0.28±0.02</td>
<td>1x10$^{14}$-1x10$^{15}$</td>
</tr>
<tr>
<td>0.23±0.02</td>
<td>(4.1 ± 3)x10$^{14}$</td>
</tr>
<tr>
<td>0.11±0.02</td>
<td>(5.3 ± 2)x10$^{14}$</td>
</tr>
</tbody>
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3.2 MOSFET Device Structure Considerations: Bottom Contact or Top Contact

The key region which defines a MOS structure is the oxide. In silicon devices, the oxide can be grown at ~800°C from the existing semiconducting material to make silicon dioxide. However, organic semiconducting materials do not have the convenience of a native oxide (one that can be grown from the existing material as in the case of silicon). Other inorganic semiconductors such as GaAs and InP can have an oxide thermally deposited or sputtered on top of the semiconducting channel material at ~400°C, which is easily withstandable by inorganic materials. Organic materials, on the other hand, are very susceptible to degradation at high temperatures. A highly ordered vacuum deposited organic semiconductor could easily become
amorphous, oxidized or decompose if exposed to the high temperature process of oxide deposition. Furthermore, the deposition of a high energy oxide could allow it to chemically bond with the organic material creating a large amount of electrical defects [10].

To solve this problem electrical engineers have established two types of configurations for organic MOS transistors. Figure 3.3 shows the physical cross sections of these two device configuration. Both begin with a highly doped silicon substrate which acts as the gate. Because the gate is on the bottom of the device it allows a layer of oxide to be thermally grown at high temperature before the organic semiconducting material is deposited. Once the oxide is grown on the gate/substrate, the organic material is deposited on top. This can be accomplished through low temperature (~140°C) or even room temperature thermal deposition (evaporation), spin coating or ink-jet printing as mentioned in chapter one. The process which differentiates the two

---

Figure 3.3  (a) Bottom contact MOS configuration, (b) top contact MOS configuration. [4]
configurations is the location of the source/drain electrodes. If the metal is deposited initially on the oxide below the organic semiconducting material, it is called a bottom contact configuration (Figure 3.3a). If the source/drain electrodes are deposited on top of the organic semiconductor, it is called a top contact configuration (Figure 3.3b).

Both top and bottom contact configurations have physical and electrical advantages and disadvantages. The most obvious advantage to a top contact configuration over a bottom configuration is the accessibility to probing of the source and drain electrodes. By contrast, because bottom contacts are below the semiconductor, for the bottom contact configuration the metal will need to be connected through vias in order to make electrical contact. This can lead to additional parasitic resistances and capacitances associated with the contact lines. However, there is another electrical problem with the bottom contact compared with top contact configuration. When metal is deposited on top of an organic material, it tends to diffuse into it creating an ohmic contact [14]. This makes the source/drain contacts better (lower resistance), which is an advantage of the top contact configuration. However, when an organic is deposited on top of a metal, it doesn’t allow the same diffusion and creates a Schottky (rectifying) contact between the electrodes and the organic semiconducting material [14]. This is a disadvantage for the bottom contact configuration. Both device configurations will be considered in the ATLAS simulations and will be discussed further in the next chapter.
3.3 Modeling Verification

To help determine whether a device simulation is working according to the MOSFET model presented in chapter one, it is necessary to verify the electrical characteristics. ATLAS can generate many different plots to help better understand the physics of the device including: dc current-voltage characteristics, conduction band and valence band bending, hole and electron concentration profiles, transconductance, and frequency response are just a few.

The simplest plot to generate is created by first ramping the gate voltage and then sweeping the drain voltage for each value of the gate voltage. Doing this will generate the basic electrical output characteristics \( I_D (V_{GS}, V_{DS}) \), which is used to set the operating point of the MOSFET transistor. Figure 3.4 shows the current versus drain voltage (IV curve) plot for a pentacene MOSFET transistor. The material parameters discussed and summarized in chapter two were incorporated into ATLAS to generate these electrical characteristics. For these simulations discussed in this chapter, the pentacene MOSFET is a top contact structure where the gate length = 30 µm, gate width = 220 µm, the hole concentration \( N_A = 1.0\times10^{17}/\text{cm}^3 \) and the hole mobility was taken as 1.2 cm²/Vs as reported by Necliudov et al. [4]. The device appears to behave according to the MOSFET theory, having both a linear and saturation region. However, other plots are necessary to determine if the device is working properly.
Useful values such as the threshold voltage can be extrapolated from the drain current versus the gate voltage plot. This is simulated in ATLAS in the same manor as the drain current vs. drain voltage characteristics accept the drain voltage is ramped before the gate voltage. Figure 3.5 shows a linear plot of the drain current versus the gate voltage. From this graph the threshold voltage can be obtained by adding a linear fit to the plot and then extrapolating the x-intercept. The value of the gate voltage extrapolated from the x-intercept of the graph shows the threshold voltage for this device to reside at 3.8 volts. The device dimensions and mobility were taken from that reported in the literature by Necliudov et al. [4]. They reported a threshold voltage of 5 volts for their pentacene MOSFET. Although the ATLAS device’s threshold voltage was slightly lower than that reported in the literature, the Figure 3.5 shows some current flow occurring until 5V is applied to the gate electrode. In this case it is difficult to achieve high...
precision when extrapolating the threshold voltage because a tangent line to the graph could result in several values of the threshold voltage. However, inspection of the graph and device’s ability to conduct until 5 volts is applied to the gate electrode proves that the ATLAS simulation is in good agreement with the literature.

Figure 3.5 shows a plot of the logarithmic characteristic of the same data. The subthreshold roll off can be seen below the threshold voltage of 3.8V, where we define the threshold voltage here as the voltage of the gate electrode when current drops to $10^{-2}$ µA. This data shows the device to be completely turned off at 5 volts. Also, the slope of the subthreshold region drops at a rate of $2.9 \times 10^{-4}$ µA/V.
If the device is to be used in an AC situation, it is necessary to investigate and understand the frequency response of the pentacene MOSFET. Even though organic MOSFET transistors are not suitable for high frequency applications like inorganic transistors such as silicon and gallium arsenide, they still have good low frequency response. ATLAS can model this by superimposing an ac signal on the gate and ramping the frequency on the gate signal for various values of the dc gate or drain voltage. Figure 3.7 shows the transconductance versus the gate voltage for the pentacene MOSFET for several frequencies. Due to the device’s low hole mobility and large size, the transconductance degrades rapidly as the frequency goes up. Measuring the transconductance gives an accurate way to measure the ac device performance. This device has a maximum transconductance for any given frequency at \( V_G \approx 20 \text{V} \).

![Figure 3.6](image_url)  

**Figure 3.6**  Plot of the logarithm of drain current versus gate voltage.
If the device is going to be used in its higher frequency range, then a plot of the ac current gain versus the frequency will give the maximum frequency of operation or the cutoff frequency $f_T$. Figure 3.8 shows the frequency response of this pentacene MOSFET. The gain begins to drop quite quickly above a few kHz, showing the difficulty in implementing the device in a high speed application. However, the cutoff frequency can be extrapolated from the graph to be $\sim 100$ kHz for $V_G = -60V$. Because the graph shows the cutoff frequency is a function of the gate voltage, a device of this type would be suited for operating frequencies below 10 kHz. There are plenty of applications for a device with this $f_T$ as were mentioned in chapter one.

Figure 3.7  Transconductance versus gate voltage for a pentacene MOSFET.
3.4 Modeling Charge Carrier Characteristics

ATLAS also provides several means to confirm the proper behavior of the charge carriers. This is not only helpful in checking for the correct device physics, but also for developing insight into the device’s operation and for pursuing further optimization of the device.

In theory because this is a p-type, depletion MOSFET device and the channel is inherently doped p-type, the majority carriers are available in the channel for no gate bias to carry the current between the source and drain electrodes at zero gate voltage bias when a potential is supplied between the source and drain. Once a positive potential is applied to the gate, a depletion region will then begin to form at the semiconductor/oxide interface. When the
potential on the gate is large enough, the depletion region should have expanded throughout the semiconductor and turned off the device. This is similar in operation to a depletion mode MOSFET. ATLAS provides a physical structural file which can show the currents in the device. Figure 3.9 provides a picture of the hole charge carrier transport for a cross section of the MOSFET when the transistor gate bias voltage is near zero bias. The gate bias voltage is set at -1V and drain bias voltage is fixed at -20V. The holes are injected at the source electrode and are accelerated by the negative potential at the drain to a current density of ~9.31 A/cm². This is

Figure 3.9 Hole current in a pentacene organic transistor in the accumulation mode of operation.
evident due to the increasing size of the arrows near the drain electrode. As the gate voltage is positively increased, the carriers begin to be pushed away from the semiconductor/oxide interface since the gate electrode is at the bottom and the channel region is pinched. Figure 3.10

Figure 3.10 Formation of depletion layer in pentacene organic transistor during inversion mode of operation.

indicates the density of the hole current in the pentacene organic semiconducting material at a gate bias voltage of 5V and a drain bias voltage of -20V. In this mode of operation, the current is almost completely shut off and the holes in the conducting channel have been squeezed into the region near the top surface. It can be seen from the figure that the hole current is extremely
small (< 0.301 A/cm²) compared to the $V_G \sim 0$V operating current (9.31 A/cm²). Therefore, the model of the hole current from ATLAS shows the pentacene organic MOSFET to be operating as a depletion type transistor.

To further show the agreement of the simulations with the depletion MOSFET theory of operation, examination of the effects to the bandgap and the hole concentration in the pentacene organic semiconductor under the gate is a necessity. ATLAS is able to take a cross section of the device at a user specified location in the structural file and plot the bandgap, hole concentration and other electrical parameters. Figure 3.11 shows the bandgap for a cross section under the gate of the pentacene MOSFET for several negative gate biases (hole accumulation). As the gate bias increases the bandgap also increases in potential energy. Furthermore, a slight bend upwards at

Figure 3.11  Cross section of the pentacene organic semiconductor under the gate showing the band bending of the energy band gap in the inversion mode of operation.
the oxide/semiconductor interface shows the trend of hole accumulation.

Figure 3.12 shows the amount of band bending which occurs as the channel is depleted of charge carriers and slowly turned off. The amount of negative band bending shows the positive hole carriers are being pushed away from the oxide interface region as seen in Figure 3.10. Therefore, the physical picture of the structure and the electrical picture of the bandgap agree.

Further analysis can be performed on the pentacene MOSFET by examining the hole concentration in the semiconductor. By taking a cross section under the gate, ATLAS can plot the hole concentration through the pentacene semiconducting material at different gate and drain biases. Figure 3.13 shows the effect of the increasingly positive gate bias on the hole concentration. As the gate voltage increases in the positive direction, the hole concentration is

---

**Figure 3.12** Cross section of pentacene organic transistor showing the band bending of the energy band gap in the accumulation mode of operation.
reduced several orders of magnitude from $1 \times 10^{16}$ cm$^{-3}$ for the gate voltage negative to $1 \times 10^{-5}$ cm$^{-3}$ when the MOSFET is completely turned off. This picture of the hole concentration also agrees with the depletion mode of operation for this pentacene organic MOSFET.

3.5 Conclusion

The output graphs and figures generated by ATLAS including the electrical characteristics, bandgap bending, and the hole concentrations agree with the depletion MOSFET theory. For a positive gate bias the holes near the oxide interface are driven out of the pentacene semiconducting material, as shown in Figure 3.13 which is evident from the downwards bending of the bandgap seen in Figure 3.12. As the gate bias is turned off and reverses polarity, holes are

Figure 3.13 Hole concentration for increasingly negative gate bias at the semiconductor/oxide interface.
reintroduced into the semiconducting material. This collection of holes is then accelerated by the lateral bias applied between the source and drain electrodes. The next section of this thesis will compare ATLAS simulation results to fabricated transistors from the literature.
References


crystals by method of thermally modulated space-charge limited current”, Acta Physica


electronic structures at organic/metal and organic/organic interfaces”, Advanced
Chapter 4

4.0 ATLAS Simulations

To begin the simulation study of pentacene organic semiconducting transistors, three authors who have reported experimental results, were chosen to verify the model which will be created using Silvaco’s ATLAS tools. By comparing the results from the simulator with the results from the three authors, the model for pentacene can be verified and refined. Initial results of the ATLAS simulator showed a trend towards higher currents than reported in the literature. After careful consideration of the material parameters, it was determined the inherent doping concentration seemed the most appropriate to be the parameter which could be varied. This was due to the fact that the doping level in organic semiconductors is highly variable, frequently unmeasured and depends on the material deposition methods and device configurations i.e. top or bottom contact. Therefore, in each case the doping value was determined by matching the reported values of the threshold voltage or the plot of the drain current versus the drain voltage for the devices. This helped to achieve more agreeable results.

4.1 Modeling the Contact Resistance and Schottky Barrier at the Electrodes

The importance of the interface at the source and drain electrodes with the organic semiconducting materials has prompted much research. The small currents seen in organic MOSFETS could very likely be limited not only by the amorphic nature of the material, but also the interface at the source and drain contacts. Many groups have been studying the nature of
these contacts to determine the physical nature. Baldo and Forest have studied the interface of metals with the organic material Alq₃ [1]. Their studies suggest that contact issues must be resolved before modeling of the semiconductor can be undertaken. Their research has shown that the electrons are injection limited at the cathode due to dipole fields caused by interfacial layers. Antoniadis et al. has also seen similar injection limited interfaces but this time for hole charge carriers [2]. Their study of organic LEDs has shown the current drive in organic LEDs is also limited by Schottky like barriers at the contacts. Ishii and Seki have also seen an interfacial electric dipole layer which effectively causes a shift in the vacuum layer of organic materials as seen in Figure 4.1 [3]. Their studies involved the organic semiconductors ZnTPP, H₂TPP and H₂T(4-Py)P instead of pentacene, but the concept of the vacuum shift and the interfacial layers can be broadened to fit all organic/metal interfaces. Further studies by Wolf et al. have also

![Figure 4.1](image-url)

**Figure 4.1** (a) Shows the presence of a barrier at the organic semiconductor/metal interface and (b) the effective lowering of the organic workfunction which results from this barrier [3].
shown a potential barrier to exist at the metal/organic semiconductor interface producing a Schottky-like current voltage behavior [4,5].

The existence of a barrier at the interface of the organic semiconductor and a metal has also been proven to exist by Seshadri et al. who used atomic force microscopy (AFM) experimental measurements across the channel region of an organic MOSFET made of 6T (sexithiophene) [6]. As the probe tip was scanned across the surface of the device, a large potential drop could be seen at the source and drain electrodes. Figure 4.2 shows a schematic cross section of the setup and the magnitude of the voltage drop at the source and drain contacts. Further experiments showed that the contact interface was much more complicated as they were experimentally measured to be a function of the drain voltage ($V_D$) and the gate voltage ($V_G$) [6]. The problem with the large contact resistance arises as the channel length decreases. Then the contact resistance can become orders of magnitude larger than that of the channel resistance and effectively limit the current [1].
In order to increase the accuracy of the simulations shown earlier, the contact resistance of the source and drain electrodes must be incorporated into the Silvaco model. This is true for both the top and bottom contact configurations. The bottom contact configuration must also have a parameter added to compensate for a Schottky barrier which is formed at the source/drain electrodes at the interface with the organic semiconducting layer [7]. This is due to the lack of sufficiently high doping in the semiconductor to form low resistance, tunneling contacts, and the
diffusion of the gold electrodes into the semiconducting material. Necliudov et al. proposed the transistor models for the top and bottom contact structures including the source/drain contact resistances and the Schottky barrier as seen in Figure 4.3. In this case the resistors $R_S$ and $R_D$ are incorporated to model more than the parasitic resistances associated with metal contacts. They used lumped parameters which encompass all resistances at the source and drain electrodes including the large contact resistances mentioned earlier. The diodes are incorporated to model the energy barrier which has been proven to exist at the metal organic interfaces in bottom contact MOSFETs [3, 6]. An anti-parallel diode was also added to the model to accommodate for symmetry and model small amounts of leakage currents yet have negligible effects to the circuit [1].

![Diagram of top contact MOS transistor](image)

![Diagram of bottom contact MOS transistor](image)

Figure 4.3 (a) Model of the top contact MOS transistor for ATLAS simulations, and (b) model of the bottom contact MOS transistor model including the contact resistances $R_S$ and $R_D$ as well as the Schottky barriers at the electrodes [7].
In ATLAS the contact resistances ($R_S$ and $R_D$) are added as lumped parameters at the electrodes [8]. However, the Schottky barriers are not quite as simple to add to the simulation. To apply a Schottky barrier to an electrode, a work function must be assigned to the contacts [8]. The barrier height ($\Phi_{bh}$) can then be determined by,

$$
\Phi_{bh} = \left(E_G + \chi_{pc}\right) - \Phi_m
$$

(3.1)

where $E_G$ is the energy gap of pentacene (2.25 eV [9]), $\chi_{pc}$ is the pentacene electron affinity (2.49 eV [10]), and $\Phi_m$ is the work function of the metal incorporated into ATLAS (4.15 eV). This produces an energy barrier of 0.60 eV which is very similar to the 0.65 eV barrier reported by Necliudov et al. [7].

To further enhance the energy band picture at the interface, the Fermi level was calculated in order to determine the amount of band bending in the pentacene organic semiconductor at the metal interfaces. The work function ($\Phi_{pc}$) and band bending ($\Delta\Phi$) were determined by,

$$
\Phi_{pc} = \chi_{pc} + E_G - E_{fpc}
$$

(3.1)

$$
\Delta\Phi = \Phi_{pc} - \Phi_m
$$

(3.2)

where $\chi_{pc}$ is the electron affinity of pentacene, $E_G$ is the band gap, and $E_{fpc}$ is the Fermi level energy measured relative to the valence band, and $\Phi_m$ is the work function of the metal. Both the electron affinity and energy gap of pentacene were reported in section 2.12 as 2.49 eV and 2.25 eV, respectively [9, 10], and the work function of the gold electrodes was experimentally determined to be 4.15 eV from the ATLAS simulations. The Fermi level is a function of the intrinsic doping level and has been calculated to be 0.516 eV above the valence band by,
where $E_i$ is the midpoint of the energy gap, $N_A$ is the intrinsic doping level (2X10$^{17}$ cm$^{-3}$ [11]), $n_i$ is the intrinsic carrier concentration, $N_C$ is the conduction band density of states calculated in
section 2.11 \((2.5 \times 10^{25} \text{ cm}^{-3})\), \(N_f\) is the valence band density of states calculated in section 2.11 \((2.5 \times 10^{25} \text{ cm}^{-3})\), \(k\) is Boltzman’s constant, and \(T\) is the temperature. Figure 4.4 shows the alignment of the metallic electrode’s Fermi level with the energy band structure of the pentacene semiconductor at the source and drain before contact and at thermal equilibrium. Due to the difference in the work function of the two materials, an energy barrier forms blocking the transport of holes. Using the above equations, the workfunction of pentacene \((\Phi_{pc})\) was calculated to be 4.23 eV. The workfunction of the metal in ATLAS was adjusted to be lower than that of the pentacene to form the hole barrier based on previous reports of Schottky-like contacts [7]. The height of the barrier for the bottom contact structures was determined using the ATLAS tools and will be discussed later on in this chapter.

4.2 ATLAS Results Compared to Necliu dov et al. Top Contact Structure

P.V. Necliu dov et al. presents the most comprehensive experimental study of the properties of pentacene MOS transistors [7]. At Renssalaer Polytechnic Institute they have extensively studied pentacene organic MOSFETs by fabricating both bottom and top contact configurations. Furthermore, they have developed computer simulations to match their data and created an equivalent circuit for modeling purposes.

The first physical configuration studied was the top contact configuration as shown in Figure 4.5. The length and width of the device was 30 µm and 220 µm, respectively. The insulating oxide thickness was 250 nm while the deposited pentacene thickness was 50 nm [7]. Deposition of the material was accomplished by flash evaporation of the pentacene onto the substrate which was held at a temperature between 20° and 160° C [12]. Furthermore, the self-
assembling agent octadecyltrichlorosilane (OTS) was deposited by evaporation between the oxide and semiconducting layer [7]. This was done to improve the mobility and overall performance [7]. Gold source and drain electrodes were deposited through a shadow mask. The mobility for this device was experimentally measured to be 0.22 cm²/V-s.

Since Necliudov et al. [7] did not report or measure the pentacene’s doping level, in order to find the correct value for the inherent doping, the threshold voltage was obtained from the reported experimental $I_D-V_G$ characteristics by extrapolating the drain current to zero for low values of the drain voltage in the linear region of the drain current versus the gate voltage plot as shown in Figure 4.6a. Necliudov et al. reported a threshold voltage of 5V for their top contact device [7]. At a doping value of $1.2 \times 10^{17} \text{ cm}^{-3}$ the ATLAS simulations of the $I_D$ versus $V_G$ plot produce a threshold voltage $V_{\text{TH}} = 5V$ shown by Figure 4.6a. This value of the doping is similar in magnitude to that measured by Brown et al. [11]. To double check the threshold voltage results, the square root of the drain current versus the gate voltage for high values of the drain voltage were used to extrapolate the x-intercept as seen in Figure 4.6b. Values of the drain voltage were plotted at -30V and -20V to check for differentiating values in the linear region. This plot shows the threshold residing at 7V which is similar to the low drain voltage plot.

Figure 4.5 Cross section of top contact pentacene organic MOSFET for simulation comparison to Necliudov et al. [7]. The x to y scale one to five.
difference in voltage could be contributed to the variability of positioning a tangent line to the simulated low drain voltage plot in Figure 4.6a.

Once the value of the inherent p-type doping had been determined, the dc I-V characteristics for the device were simulated as described in chapter three. An initial resistance of $1 \times 10^5$ ohms was added to the resistance of the source and drain electrodes to model the

![Figure 4.6](image)

Figure 4.6  Threshold voltage extraction from the (a) linear plot of the drain current versus the gate voltage and (b) the square root of the drain current at high values of $V_D$ in ATLAS.
contact resistance. From this initial guess, for each value of the gate voltage the I-V characteristics were simulated separately and the contact resistance adjusted to match to the published dc characteristics of the pentacene organic MOSFET. This was necessary because Necliudov et al. determined that the contact resistance at the source and drain electrodes was not a constant but a function of the gate voltage [13]. Figure 4.7a shows the experimentally determined values of the contact resistance as a function of the gate voltage for a 1200 µm wide device and (b) the total contact resistance versus the gate voltage of the simulated ATLAS device whose width was 220 µm. The simulated data, although larger in size, does follow the same trend as the experimental. This data was then incorporated into ATLAS model in order to simulate the dc $I_D$-$V_D$, $V_G$ characteristics. Figure 4.8a shows the published data for the drain current versus the drain voltage [7] and (b) the simulated dc characteristics by ATLAS of a pentacene top contact MOSFET with the same structure. The graphs show very good agreement between the fabricated transistor and the simulated data after the fitting the simulated data by altering the contact resistance for each gate bias.
From the graph of $I_D$ versus $V_D$ (Figure 4.8) several important characteristics can be extrapolated. The first is the transconductance ($g_m$) which is the change in the drain current per change in gate voltage or $\Delta I_D/\Delta V_G$. This is measured at a large value of $V_D$ so the maximum $g_m$ is obtained for the MOSFET. Figure 4.9 shows the transconductance as a function of the gate voltage for both the experimental and simulated pentacene MOSFET. Both increase linearly with the gate voltage as expected since the drain current in the saturation region varies gradually.

Figure 4.7  (a) Total contact resistance as a function of gate voltage from a fabricated pentacene MOSFET ($W=1200$ µm) [13], and (b) simulated results from a similar top contact device ($W=220$ µm).
with the gate voltage. Typically, the transconductance for long channel (>1 µm) inorganic MOSFETs such as silicon is a constant as a function of drain bias and non-linear for short channel (< 1 µm) device [14]. However, this pentacene organic MOSFET shows non-linear or short channel behavior, which arises from the large contact resistances at the source and drain, since the drain current does not saturate until very large drain biases are reached (>50V).

Another parameter which can be extracted from Figure 4.8 is the source drain resistance or $R_D$. This is derived from the slope ($\Delta I_D/\Delta V_D$) of the I-V curves in the linear region of the
This is also a function of the gate voltage in both the experimental and simulated measurements as seen in Figure 4.10. This shows that as the gate voltage increases, the resistance in the channel decreases. Therefore, the device will eventually be limited by the contact resistance at the source and drain as the channel resistance decreases due to the increasing gate voltage.

The last electrical parameter extracted from the drain current versus drain voltage plot was the output conductance. This is a measure of the flatness of the lines in the saturation region of the $I_D$ versus $V_D$ graph. If the conductance is high, the transistor will not be able to drive a large resistive load on the output. The output conductance of the experimental device was measured from the graph to be $3 \times 10^{-2}$ $\mu$A/V at a gate voltage of -50V. The same characteristic measured at a gate voltage of -50V from the simulated data was $6.01 \times 10^{-2}$ $\mu$A/V which is twice as high. This difference in slope could easily be contributed by the difficulty in extrapolating the data from the published graph.

Figure 4.9 Plot of the transconductance versus the gate voltage for the fabricated pentacene MOSFET [17] and the simulated device with the same structure.
The results of the contact resistance for the source and drain electrodes determined previously were also incorporated in the simulations to evaluate the plot of the log of the drain current versus the gate voltage for the subthreshold region. Figure 4.11a shows the published experimental results for the same pentacene based transistor [7], compared to the simulated results obtained by using ATLAS. The gate voltage region of the two transistors is nearly the same in the negative gate voltage region. However, the simulated device has a much steeper subthreshold roll off slope. The subthreshold rolloff slope of the fabricated device was calculated to be $4.5 \times 10^{-3}$ $\mu$m/V and the simulated MOSFET’s slope was determined to be $9 \times 10^{-3}$ $\mu$m/V. Furthermore, the fabricated device shows a much higher current when the gate voltage is at its largest ($V_G \approx -40$V). It is most likely that the ATLAS simulation cannot model all of the leakage currents which are present in the real device, but this region is relatively unimportant.
Figure 4.7  (a) Fabricated MOSFET drain current versus gate voltage [7] and (b) simulated results in ATLAS of a pentacene MOSFET of the same structure.
4.3 ATLAS Results Compared to Knipp et al. Top Contact Structure

A team at Xerox PARC has chosen the more expensive route of thermal vapor deposition to grow their layer of pentacene semiconducting material [15, 16, 17]. The advantage of this technique is a higher purity crystalline structure which ultimately improves the mobility. Furthermore, they were studying the effects of the interface roughness with the dielectric on the mobility. The grain size of the thermally deposited pentacene was 0.1-0.2 um while the underlying roughness of the dielectric was 0.15 nm [15]. The mobility measured from their fabricated MOSFET was 0.39 cm²/V·s⁻¹ [15] while the length and width of this transistor was 100 µm and 650 µm. The thermal oxide was 100nm thick while the thickness of the deposited pentacene was 70 nm [15]. Knipp’s group chose a top contact configuration as seen in Figure 4.12 for their study.

The process of simulating this transistor was different from earlier methods mentioned because the threshold voltage was not reported. Therefore, a best fit of the drain current versus the drain voltage plot was attempted by varying the doping. Once the doping value was determined, the contact resistance was added and each value of the gate voltage was simulated.
separately due to varying values of the contact resistance with gate bias as seen in the previous section. The results of the ATLAS simulator compared to the fabricated pentacene MOSFET can be seen in Figure 4.13. The inherent doping used to achieve these dc characteristics was $2 \times 10^{17} \text{ cm}^{-3}$ as reported by Brown et al. [11]. As can be seen from the Figure 4.13, the saturation region matches well to the fabricated device, but the linear region of the simulated MOSFET has a smaller slope. Also, the drain current produced by the simulator for a gate voltage above -25V was smaller than the fabricated device’s even before adding the contact resistance to the simulation. A fit to the experimental gate voltage at -30V would have needed a doping value above $4 \times 10^{17} \text{ cm}^{-3}$ which would have resulted in extremely large contact resistances for the gate voltages less than -30V. Therefore, this value of the gate voltage was eliminated from the ATLAS graph in Figure 4.13b.
The contact resistances reported and extracted by fitting the $I_D$ ($V_{DS}$, $V_{GS}$) curves, can be seen as a function of the gate voltage in Figure 4.14. The same trend, which was seen in the previous section for a contact top contact ATLAS simulations, is also seen here, i.e. as the gate voltage increases, the contact resistance decreases at a rapid rate. Once again the simulated
contact resistance is about an order of magnitude different than the published data [13]. This may be due to the approximate nature of the fit of the simulated I-V characteristics to the experimental results.

Similar parameter extractions were performed on the drain current versus drain voltage

![Figure 4.14](image)

(a) Total contact resistance multiplied by the width versus gate voltage for a pentacene MOSFET (W=1200µm) [13] and (b) the corresponding graphical results for the same device structure simulated in ATLAS (W=650µm).
plot as described in the previous section. The transconductance of this top contact device was measured at a drain voltage of -40V and is seen in Figure 4.15. The simulated data only has two data points because of the problems with the simulations at a gate voltage of -30V. However, the data is in good agreement for the transconductance at a gate voltage of -15 and -20V. Again, the transconductance increases linearly with gate voltage as expected.

The channel resistance ($R_D$) was extracted from the drain current versus the drain voltage plot at low $V_{DS}$ (-5V) and is seen in Figure 4.16 for both the experimental data and the simulated data. The data extrapolated for both devices compares very well.

The output conductance which is the reciprocal of the output resistance was measured for both the experimental and the simulated pentacene MOSFET. At a gate voltage of -25V, from the experimental results the output conductance was found to be $2.5 \times 10^{-2} \ \mu A/V$; the simulated output conductance was found to be nearly the same at $2.8 \times 10^{-2} \ \mu A/V$.

A simulated plot of the drain current versus the gate voltage was unobtainable due to

![Figure 4.15](image)

Figure 4.15 Plot of the transconductance versus the gate voltage for the fabricated pentacene MOSFET [15] and the simulated device with the same structure.
convergence errors in the ATLAS simulations possibly due to the long channel length of this device. However, the threshold of this device could be determined from plots generated from the simulation of the drain current versus the gate voltage for small values of the drain voltage as seen in Figure 4.17(a). It is also determined as shown in Figure 4.17(b) from the plot of the square root of the drain current versus the gate voltage at large values of the drain voltage. These were obtainable because the subthreshold region is a not a strong function of the contact resistance as determined from ATLAS simulations. Therefore, the convergence problems could be avoided in this simulation by neglecting the contact resistance all together. Figure 4.17 shows extracted threshold voltages of (a) 7.5 V and (b) 8.5 V from the ATLAS simulations. An experimentally determined threshold voltage was not reported by Knipp et al. for this device [15].

Figure 4.16  Plot of the channel resistance versus the gate voltage for the fabricated pentacene MOSFET [15] and the simulated device with the same structure for a $V_{DS} = -5V$. 
Figure 4.17  Threshold voltage extractions from ATLAS simulations of the (a) drain current versus the gate voltage at $V_D = -1V$ and (b) the square root of the drain current at $V_D = -25V$ for a top contact pentacene MOSFET similar in structure to Knipp et al. [15].
4.4 ATLAS Results Compared to Brown et al. Bottom Contact Structure

Brown et al. [11] fabricated organic semiconducting pentacene transistors using spin coating techniques. The difficulty of using the spin coating technique for pentacene is it does not have a usable liquid form. Therefore, several authors including Brown have discovered precursor materials [11, 18]. Precursor materials are similar to the desired material, but they have an additional side chain to the molecule, and can be used in spin coating. When the material is heated, the side chain is released leaving behind the desired material, which in this case is pentacene. Figure 4.18 shows this process for pentacene and its precursor. The disadvantage of this process is the mobility of the pentacene is a function of the temperature and time the material is allowed to convert from its precursor [11]. Figure 4.19 shows the conversion temperature and how it affects the mobility and conductivity of the final material. Another effect of the heating is the thinning of the semiconducting layer. The original thickness of the deposited pentacene-precursor layer was 100 nm. After 20 minutes of heating in a low vacuum chamber (10^{-2} Torr), the material was reduced to a thickness of 70 nm [11].

![Diagram showing the conversion of precursor to pentacene](image)

Figure 4.18  Pentacene and its precursor material [11].
The p-type transistor reported by Brown et al. [11] incorporating spin coating pentacene used a lightly doped silicon wafer as the substrate. The gate material was created from a layer of heavily doped polysilicon. Deposited above this was a 100 nm layer of silicon dioxide which was grown using chemical vapor deposition (CVD) [11]. Deposition was used to form the 200 nm gold contacts, the length and width of which were 12 µm and 10 mm [11] as seen in Figure 4.20. The reason for creating such a large transistor width was to minimize the operating voltages [11]. This enormous width allowed the transistor to operate in a voltage range of 0-10 volts. To finish the transistor fabrication, Brown et al. [11] spin coated the precursor material above the contacts creating a bottom contact configuration described in Section 3.2. The mobility reported for the fabricated transistor by Brown et al. was $4 \times 10^{-3} \text{ cm}^2/\text{V-s}$ [11]. This low mobility was attributed to incomplete step coverage of the pentacene precursor material [11].
The value of the inherent doping reported originally by Brown et al. [11] \((2 \times 10^{17} \text{ cm}^{-3})\) was determined to be too large from our initial simulations since it could have implied a negative contact resistance. A new value of \(5 \times 10^{16} \text{ cm}^{-3}\) was determined to give a better fit of the simulations with the experimental results. Necliudov et al. experimentally determined the contact resistance in bottom contact devices to be a constant [7, 13]. Therefore, a constant contact resistance of \(1 \times 10^4\) ohms was chosen causing the barrier height to become the key fitting factor. Figure 4.21 shows simulations in ATLAS which were used to determine the proper metal workfunction which would produce the best fit of the drain current versus the drain voltage. A barrier height below 0.51 eV produced little if no change in the dc characteristics while a barrier height greater than 0.74 eV almost cut off the current completely. Therefore, an intermediate barrier height of 0.61 eV, which was equivalent to a metallic workfunction of 4.15 eV, was chosen to give the best fit. The results of the dc characteristic \(I_D\) versus \(V_D\) simulations are shown in Figure 4.22.

Figure 4.20 Physical cross section of pentacene MOSFET fabricated by Brown et al. [11]. The x to y ratio is one to five.
The same parameters extracted in the previous sections from the $I_D$ versus $V_D$ were also extracted from the experimental and simulated data for this device. A plot of the comparison of the transconductance versus the gate voltage at a drain voltage of -10V for the experimental and simulated data is shown in Figure 4.23. Unlike the previously studied devices, this graph shows a much different trend in the transconductance of the fabricated and simulated MOSFET. The fabricated device shows characteristics similar to that of a short channel MOSFET which exhibits a non-linearity in the transconductance. The simulated device shows more of a long channel characteristic by exhibiting a linear transconductance. Therefore, this plot shows a big difference in the electrical characteristics of the two devices.

A plot of the channel resistance in the linear region of operation shows much better agreement of the experimental and simulated data than the transconductance plot as can be seen
in Figure 4.24. The channel resistance was measured at a drain voltage of -1V for both devices. The crudeness of the experimental device’s curve can be attributed to the difficulty of extracting data from the published plot of the drain current versus the drain voltage.
The output conductance was measured at a gate voltage of -9V due to the lack of a saturation region formation at -10V in the experimental data. The experimental data showed an output conductance of 1.7 µA/V while the simulated device showed a slightly smaller value at 1.1 µA/V.

A comparison of the log drain current versus the gate voltage for the experimental device by Brown et al. [11] and the same device simulated in ATLAS can be seen in Figure 4.25. The magnitude of the currents in the negative gate voltage region show good comparison. However, the subthreshold rolloff of the experimental device is much more gradual than that of the simulated device. Measurements of the slope between a drain current of 1X10^{-7} A and 1X10^{-8} A produces a slope of 3.2X10^{-2} µA/V for the experimental data and a slope of 4.4X10^{-2} µA/V for the simulated data. The slope becomes much steeper as the gate voltage becomes more positive.
for the simulated pentacene MOSFET, but this difference can be attributed to the difficulty in simulating this region due to the effects of surface currents and other parasitics in the device.

The threshold voltage can be extracted for the drain current versus the gate voltage for small values of the drain voltage. At a drain voltage of -2V the threshold voltage is extracted from the x-intercept to be 3.2 V as seen in Figure 4.26a. The square root of the drain current versus the gate voltage for a large value of the drain voltage produces a similar threshold voltage of 3.4 V for this device as seen in Figure 4.26b. Brown et al. [11] did not report a value of the threshold voltage to compare to the simulated data.

Figure 4.24  Plot of the experimental [11] and simulated channel resistance in the linear region of operation versus the gate voltage for a pentacene MOSFET.
Figure 4.25  (a) Experimental drain current versus gate voltage plot of a fabricated pentacene MOSFET [11], and (b) the plot of the simulated structure in ATLAS.
Figure 4.26  Threshold voltage from the (a) plot of the drain current versus the gate voltage and (b) the square root of the drain current versus the gate voltage.
4.5 ATLAS Results Compared to Necliudov et al. Bottom Contact Structure

Necliudov et al. [7] also studied a pentacene MOSFET for the bottom contact configuration. The gate length and width of this device was 20 µm and 220 µm. The insulating oxide thickness was 290 nm while the pentacene thickness was 50 nm [7] as seen in Figure 4.27. The same self-assembling agent was deposited between the oxide and semiconducting layer as

![Cross section of a pentacene MOSFET fabricated by Necliudov et al. [7]. The x to y ratio is one to five.](image)

for the previous device, and the pentacene was deposited in the same manner described for the top contact device in section 4.2. The mobility was experimentally determined to be 1.2 cm²/V-s.

This time a higher value of the doping $(3.5 \times 10^{17} \text{ cm}^{-3})$ was needed for the simulation because the simulated $I_D$ versus $V_G$ plot came close to matching up with the experimental at a doping value of $2 \times 10^{17} \text{ cm}^{-3}$ [11] without the addition of any contact resistance or the inclusion of the barrier height adjustment to the simulation. Because it is a bottom contact device the contact resistance was not expected to be a function of the gate voltage and, therefore the contact resistance was introduced into the simulation as a constant. The contact resistance was chosen to
be $1 \times 10^4$ ohms for the source and drain, and the barrier height was chosen to be 0.59 eV as in the simulations in the previous section. The results of the ATLAS simulations versus the experimental results for the $I_D$ versus $V_D$ can be seen in Figure 4.28. A first look at Figure 4.28 shows good comparison of both the linear and saturation regions of operation for the bottom

![Diagram](image)

Figure 4.28  (a) Plot of drain current versus drain voltage for a fabricated pentacene MOSFET [7], and (b) the simulated results of a similar device structure using ATLAS.
contact pentacene MOSFET. To obtain a better comparison of the experimental and simulated device, a look at the transconductance, channel resistance, and output conductance were examined.

The transconductance was measured for both the published experimental data and the simulated data at a drain voltage of -60V and can be seen as a function of the gate voltage in Figure 4.29. The two devices show opposite trends in the transconductance. In the experimental transistor, a minimum transconductance is reached at $V_G = -30V$ and the simulated transistor shows a maximum at the same negative gate voltage. However, both have an upward trend with larger gate voltages.

The channel resistance was also extracted from the slope of the linear region of operation for both the experimental and simulated MOSFET. Figure 4.30 shows the channel resistance which was measured at a drain voltage of -10V. Unlike the comparison of the transconductance,
the channel resistance shows good agreement of the slopes from the linear region.

The output conductance was not able to be obtained for this device. Neither the simulated nor the experimental pentacene MOSFET showed signs of a measurable saturation region at higher gate voltages. In order to obtain this saturation region both transistors would have needed to have been operated to higher drain voltages.

A comparison of the drain current versus the gate voltage for both the experimental and simulated transistor can be seen in Figure 4.31. The simulated device was operated at a gate voltage maximum of -30V because the ATLAS simulator had convergence problems above that voltage when the contact resistances were added. These graphs show good comparison in the negative gate voltage region, but poor subthreshold comparison. The fabricated device has a much lower off current and reaches the point of channel depletion much earlier than the

![Graph](image)

**Figure 4.30** Comparison of the channel resistance of a fabricated pentacene MOSFET [7] and a simulated one of the same structure.
simulated device. However, the measured subthreshold roll off were found to be in reasonable agreement with 1 μA for the experimental device 0.18 μA/V and 0.16 μA/V for the simulated device.

The threshold voltage of this pentacene MOSFET was reported to be 13V by Necliudov

Figure 4.31 (a) Drain current versus the gate voltage of a fabricated pentacene MOSFET [7] and (b) a simulated one of a similar structure in ATLAS.
et al. [7]. To determine the threshold voltage of the bottom contact simulated device, plots were made of the drain current versus the gate voltage at \( V_D = -2V \) and the square root of the drain current versus the gate voltage at \( V_D = -30V \) for a bottom contact pentacene MOSFET similar in structure to Necliudov et al. [7].

Figure 4.32 Threshold voltage extractions from ATLAS simulations of the (a) drain current versus the gate voltage at \( V_D = -2V \) and (b) the square root of the drain current at \( V_D = -30V \) for a bottom contact pentacene MOSFET similar in structure to Necliudov et al. [7].

To determine the threshold voltage of the bottom contact simulated device, plots were made of the drain current versus the gate voltage at \( V_D = -2V \) and the square root of the drain current versus the gate voltage at \( V_D = -30V \). The results of the ATLAS simulation can be seen in Figure 4.32. A much higher threshold of 24 volts (versus the experimental 13V) was extracted from the x-intercept of both graphs. This could be attributed to the higher doping concentration which was incorporated in the simulation to fit the plot of the drain current versus the drain voltage. However, the threshold voltage is not a function of the contact resistance or the
formation of a Schottky barrier as simulations performed using ATLAS proved that this was not a function of these variables. Also the effects of the self assembling mono layer (OTS) are unclear.

4.6 Conclusion

In this chapter we compared the results of Silvaco simulations with those of three experimental reports. In general, the ATLAS simulations showed good agreement with the published data of fabricated pentacene MOSFETs. The simulated top contact structures needed higher contact resistances by an order of magnitude than the published, but then produced very similar trends. The bottom contact devices both used a contact resistance of $1 \times 10^4$ ohms and a barrier height of 0.59 eV to produce graphical results similar to the published data. The only major difference occurred in the top contact device by Knipp et al. [15]. The gate voltages above -25V produced very different drain currents and were therefore left out of the simulation data. However, the simulations proved that ATLAS can be used for modeling organic MOSFETs such as pentacene-based devices. Further experimental study is needed to more completely understand the nature of the metal organic semiconductor contacts since the contact resistance of these interfaces can dominate over the channel resistance in organic-based MOSFETs, which is unlike the case in traditional silicon MOSFETs.
References


Chapter 5

5.0 Conclusion

The past couple decades have seen an ever increasing interest in organic semiconducting devices towards an expanding commercial market. The purpose of this thesis was to show the usefulness of a commercial semiconducting device simulator package called Silvaco to model the dc and ac characteristics of a pentacene organic semiconductor-based MOSFET. Creation of a pentacene semiconductor material model could potentially offset expensive fabrication costs for device development.

Because of the complexity of the physics of the motion of the charge carriers through the organic semiconducting material involving polaron charge carriers, a constant effective mobility model was used to approximate charge movement to simplify the device physics for use in device modeling using ATLAS [1]. Other material parameters for pentacene were extracted from the literature and incorporated into the semiconductor material model in the ATLAS simulator. The primary parameters such as energy gap, electron affinity, and permittivity were extracted from publications by Silinish et al. and Sebastian et al. [2, 3]. The inherent doping of the pentacene was assumed to be 2X10^{17} \text{ cm}^{-3} as measured Brown et al. [4] and was later used as a vital fitting parameter for the dc characteristics since it was not independently measured for the MOSFETs reported.

Recent publications of fabricated pentacene MOSFETs from several research groups were used for comparison with the ATLAS simulation results. The fabricated MOSFETs from the publications were both top and bottom contact structure and had pentacene material deposition methods ranging from orderly thermal deposition to amorphous like spin coating
deposition. The complexity of the simulations was increased by the difficulty associated with modeling hole injection barriers, which have been reported to exist at the source and drain electrodes [5, 6]. Lumped series resistances and Schottky barriers at the source and drain contacts were incorporated in the simulations to model these injection barriers and to increase the accuracy of the simulation results. The final ATLAS simulations showed reasonably good comparison to the experimental published data for both top and bottom contact structures and multiple deposition methods. This thesis represents one of the earliest attempts to model the operation of the organic semiconductor based MOSFETs.

5.1 Future Work

To increase the current density of the pentacene MOSFETs, the fabricated transistors were designed with extremely large gate widths, i.e. 10 mm [4]. Due to the limitations of the number of nodes available and the amount of time necessary to execute a three dimensional simulation, two dimensional simulations were developed with a width of one micron and then scaled by the published width. Future projects could incorporate a third dimension to increase the accuracy of this thesis’ results.

Furthermore, the mobility has been determined to be a function of both the gate voltage and temperature [1]. The experimental fitting parameters and mobility model could be incorporated into the C code, which is the basic building block of the ATLAS simulator. This will provide a better means of modeling the mobility and understanding the device physics.

Finally, further validation of the ATLAS model could be accomplished by fabricating a pentacene MOSFET at the University of Cincinnati and comparing the results to the simulated
device of the same design. In particular, detailed study of the nature of the charge injection at the metal-semiconductor contacts is needed to enable better simulation of the current-voltage characteristics of experimental MOSFETs. A particularly interesting study would use a three tiered structure at the source/drain contacts consisting of a layer of gold followed by a layer of a highly conducting polymer on top of the pentacene organic semiconductor. It might be possible to reduce the bottlenecking of the hole charge current which occurs at the source/drain electrodes by using an amorphous material such as a highly conducting polymer to interface with the amorphous organic semiconductor.
References


