A Dissertation

entitled

Analysis and Loss Estimation of Different Multilevel DC-DC Converter Modules
and Different Proposed Multilevel DC-DC Converter Systems

by

Sandeep Patil

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Dr. Vijay Devabhaktuni, Committee Chair
Dr. Srinivasa Vemuru, Committee Member
Dr. Mohammed Niamat, Committee Member

Dr. Patricia R. Komuniecki, Dean
College of Graduate Studies

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A multilevel DC-DC converter converts a DC source from one voltage level to another level. DC-DC converters are important in portable devices like cell phones, laptops, etc, as well as in applications such as electric vehicles, which have subcircuits operating at voltages different from the supply voltage. In this thesis, two new multilevel DC-DC converter system modules: one-to-many topology and cascaded topology are presented. Comparisons are made for the proposed multilevel DC-DC converter systems along with the existing multilevel DC-DC converter system. The comparisons are made in the terms of range of the output voltage, maximum output voltage, number of steps of output voltages, number of switches operated for any given output voltage, and the ripples in the output voltage. Among all the proposed converter system topologies, cascaded topology with even number of modules turned out to be more efficient in terms of maximum output voltage and number of steps of output voltages.

Two new different multilevel DC-DC converter modules are presented in this thesis. However only one of them facilitates the implementation of cascaded topology of DC-DC converters and decrease the transition currents, while other just decrease the transition currents. Comparisons are based on different losses during the circuit operation, ripple voltages, and efficiency. One of the proposed converter modules
limits the transient currents significantly over existing converters during the output
voltage transition in multilevel DC-DC converter topologies for a given transition
time. Though the efficiencies of the proposed modules are slightly less (< 1%) than
the existing converter modules they facilitate the implementation of cascading con-
verters. Also the reduction in the transition currents can potentially increase the life
of the converter modules.
This thesis is dedicated to my parents Mruthyunjaya Patil and Vijaya Gowri Patil, and my brother Pradeep Patil.
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<td>Electro Magnetic Interference</td>
</tr>
<tr>
<td>LTspice</td>
<td>Linear Technology Simulation Program with Integrated Circuit Emphasis</td>
</tr>
<tr>
<td>DC</td>
<td>Direct Current</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal Oxide Semiconductor Field-Effect Transistor</td>
</tr>
<tr>
<td>NMOS</td>
<td>N-Type Metal Oxide Semiconductor</td>
</tr>
<tr>
<td>IPB025N10N3</td>
<td>Infineon Power Transistor B025N10N3</td>
</tr>
<tr>
<td>ESL</td>
<td>Equivalent Series Inductance</td>
</tr>
<tr>
<td>IGBT</td>
<td>Insulated-Gate Bipolar Transistor</td>
</tr>
<tr>
<td>MMCCC</td>
<td>Multilevel Modular Capacitor Clamped DC-DC Converter</td>
</tr>
<tr>
<td>FCMDC</td>
<td>Flying Capacitor Multilevel DC-DC Converter</td>
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\[ \Delta \] Difference operator for the output voltage
\[ \Sigma \] Summation of a sequence of numbers
\[ C \] Capacitance
\[ L \] Inductance
\[ S \] Switch
Chapter 1

Introduction

This chapter is organized into four sections. The first section presents the problem statement of this thesis. The second section presents the previous work done on this research topic. The third section presents the proposed research approach followed by fourth section which presents the organization of this thesis.

1.1 Problem Statement

Over the last decade power conversion devices have attracted a great deal of attention. One such power supply device is the multilevel DC-DC converter. Multilevel converter systems are used to transform low level DC voltages to multiple high level DC voltages. Multilevel converters are used in power conversion applications due to advantages such as low EMI, low voltage stress on devices, and less harmonic distortion [1] [2]. Obtaining high power density and high efficiency has become a major problem in most of the power electronics circuits because magnetic components become bulky and the losses by the magnetic components make them less efficient [3]. The main advantage of the multilevel DC-DC converters is that they are transformer-less [4] and can either reduce or eliminate magnetic components. This reduces the size and the cost of implementation of the converter [5]. The main driving force for DC-DC converters is a constant demand for small, light, and high efficiency power.
supplies. These power electronic converters have increased use in hybrid automobile industry and fuel cell vehicular power systems [6] [7] [8].

However there are certain disadvantages with the multilevel DC-DC converters. The existing converters have limited steps or levels of output voltages. There is a need to further increase the number of steps of output voltages and to increase the maximum output voltage to even larger output voltages than the existing multilevel converters [9].

The goals of this research work are as follows:

• To develop different improvised multilevel DC-DC converter modules that decrease transition time, reduce transition currents, and increase the life of the converter module.

• To make an estimate of operational and transition losses in multilevel DC-DC converter modules.

• To develop different multilevel DC-DC converter systems that can output a wide range of output voltages.

1.2 Literature Review

The research on multilevel converters concept has started since 1975 [10]. However, the concept of multilevel converters began with three level converters. Many multilevel converter topologies have been developed later [10 - 13][14]. Significant developments in this area include the flying capacitor multilevel DC-DC converter (FCMDC) [15][16], multilevel modular capacitor clamped DC-DC converter (MMCCC) [16], high frequency multilevel DC-DC boost converter, and diode clamped multilevel converter [17]. In FCDMC topology, there are capacitor charge unbalance issues and voltage stress is not equal in all the switches. In MMCCC topology, there
are more transistor switches being operated to obtain the same conversion ratio. The high frequency and diode clamped multilevel converters mainly concentrate on the reduction of chip size, and control and modulation schemes, respectively.

Other efforts were focused on the elimination of inductors to avoid losses and to perform steady state analysis of the converters [18][19]. However, all these converters supply very limited increase of output voltages [20][21]. Hence, there is a need to develop converters that can generate larger output voltages and more steps of output voltage using a single voltage source.

With the increase in the use of multilevel DC-DC converters in the automotive industry [22][23], fuel cells [24], and photovoltaic cells [10][25], there is a need to improve the performance of the converters [26-30]. Multilevel converters are also used to interface energy systems [31][32]. In these applications, the multilevel DC-DC converters are advantageous because they are bidirectional in nature. The capability of bilateral power flow providing the functionality of two unidirectional converters in a single unit makes this compact with less use of magnetic components. This feature makes them distinct from other traditional DC-DC converters.

1.3 Proposed Research Approach

This section of this chapter presents the research approach followed to address some stated disadvantages from the prior section.

In the first phase of this research, two new multilevel DC-DC converter system topologies, one-to-many topology and cascaded topology of multilevel DC-DC converters, are presented. Several possible implementations of cascaded topologies are presented that use odd and even number of converter modules. All the topologies presented can increase the range of output voltage levels and with different number of voltage steps within the voltage range. Several formulations and generalizations
are developed for the output voltage levels, number of steps of output voltages, the switching configurations with minimum number of switches operated to obtain any given output voltage level, and voltage ripples.

Converter modules are the critical components of the two new multilevel converter systems that are proposed. In the second phase of this research, two new topologies of multilevel DC-DC converter modules are presented. One of the proposed multilevel converters facilitates the implementation of cascaded topology of multilevel converters by overcoming the problems with the switching patterns. Both modules reduce the transition currents that can increase the life span of the converter module but they use two more switches.

For an efficient operation of any power conversion module, there is a need to decrease the power losses. Therefore, the sources of these losses must be understood and analyzed to study the impact of circuit configuration on these losses. Hence, in the third phase of this thesis, the losses that occur in the operation of multilevel DC-DC power conversion module are studied. Another factor that is important in the operation of DC-DC converter is the response of the system to changes in voltage levels, i.e., the transition currents during transition of the output voltage. The two new topologies decrease the transient currents during the voltage transitions.

1.4 Thesis Organization

The rest of the thesis is organized as follows:

Chapter 2 presents the two new multilevel DC-DC converter system topologies along with the existing general multilevel DC-DC converter system. Chapter 3 presents different performance criteria comparisons for each converter system topology such as range of output voltage, number of steps of output voltages, voltage ripples, and the minimum number of switches operated for a given output voltage.
Chapter 4 presents the two new multilevel DC-DC converter modules along with the existing general multilevel DC-DC converter. Chapter 5 presents the different operational and transition losses of the proposed and existing multilevel DC-DC converter modules. Chapter 6 presents the implementation of the cascaded topology of the converter modules. Finally, Chapter 7 gives the conclusions and future extensions to this research project.
Chapter 2

Different Multilevel DC-DC Converter System Topologies

2.1 Introduction

The description and the operation of a basic multilevel DC-DC module is presented in the second section. This module can be used to build some of the multilevel DC-DC converter systems presented in this chapter. This multilevel DC-DC converter module was proposed by Peng et al in 2004 [2]. In the later sections of the chapter, the converter module is used in the implementation of the multilevel DC-DC converter system topologies including two new topologies [2]. The advantages of the new proposed multilevel converter systems are that they have large number of output voltage levels and maximum output voltages when compared to the existing converter systems.

The primary concept of multilevel converters is to achieve higher and multiple levels of voltages by using a set of power semiconductor devices with one or several DC sources. The minimal use of magnetic components is targeted due to the need of compact converters. Multilevel topologies have several advantages such as low output voltage distortion frequency and they can be operated at both fundamental switching
and high frequency switching [33] in high voltage applications like large electric drives, dynamic voltage restorers, reactive power compensations, and FACTS devices.

## 2.2 The Description and Operation of Basic DC-DC Converter Module Design

The multilevel DC-DC converter module proposed by Peng et al, shown in the Figure 2-1, consists of a battery source, four switches (S1, S2, S3, S4), and two capacitors which operate in three switching states (state1, state2, state3). These states are based on the sequence of different switching patterns applied to the switches.

![General Multilevel DC-DC Converter Module](image)

**Figure 2-1: General Multilevel DC-DC Converter Module**

By operating in these three states the converter module is able to output two
voltages: $V_{in}$ and $2V_{in}$, where $V_{in}$ is the input voltage given to the converter module. When the converter is operated in switching state1, the switches S1 and S4 are ON while the switches S2 and S3 are OFF. With the switches S1 and S4 being closed, the combined voltage across the capacitors C1 and C2 is $V_{in}$. The operation of the converter module in state1 with the path for the current flow is shown in the Figure 2-2.

![Multilevel DC-DC Converter Module Operating in State1](image)

Figure 2-2: Multilevel DC-DC Converter Module Operating in State1

When the converter is operated in switching state2, the switches S1 and S3 are ON and S2 and S4 are OFF. During this state the capacitor C1 is charged to $V_{in}$. 
The operation of switches and the flow of current in the converter module in state2 is shown in the Figure 2-3.

![Multilevel DC-DC Converter Module Operating in State2](image)

When the converter is operated in switching state3, switches S2 and S4 are ON and switches S1 and S3 are OFF. The flow of current in the converter module in state3 is shown in Figure 2-4. The capacitor C2 is charged to $V_{in}$ in state3.
By switching between state2 and state3 at a relatively high frequency with a 50% duty cycle, a $2V_{in}$ output voltage is obtained since the capacitors $C1$ and $C2$ are charged to $V_{in}$ in state2 and state3, respectively. Thus, the multilevel DC-DC converter module is able to output two voltages: $V_{in}$ and $2V_{in}$. When the switches (MOSFETs or IGBTs with freewheeling diodes) are turned on, the current can flow in either direction, so the converter is a bidirectional converter.

During the steady state operation, the difference of the voltage between the capacitors being charged/discharged and the battery is very small; therefore, the current
through the switches is limited. However, there is a large voltage difference during
the transition of the output voltage from $V_{in}$ to $2V_{in}$ or vice versa, which can result
in large transient currents. In order to limit these large currents during the voltage
transition, a very small inductance can be added in the circuit. The parasitic induct-
tance of the cable and the equivalent series inductance (ESL) of the capacitor can
sometimes limit the transition currents to some extent.

Further reduction can be made through the use of the control signals during output
voltage transition from $V_{in}$ to $2V_{in}$ and the control signals during output voltage
transition from $2V_{in}$ to $V_{in}$ are as shown in Figure 2-5 and Figure 2-6 respectively.
The control signals for the switches S1, S2 and switches S3, S4 are complementary
in nature while outputting $V_{in}$ output voltage. The duty cycle is changed slowly so
that switches S1 and S3 are ON at the same time while S2 and S4 are OFF and vice
versa.

Figure 2-5: Control Signals During Output Voltage Transition from $V_{in}$ to
$2V_{in}$
2.3 General Multilevel DC-DC Converter System Topology

The general multilevel DC-DC converter system topology is comprised of N converter modules. Each converter module can have an individual isolated voltage source as shown in Figure 2-7. Typically all the converter modules are of the same ratings. The outputs of the converter modules are connected in series to provide the system output voltage as shown in Figure 2-7.

The output voltage of this topology is the sum of the individual converter modules in the converter system. The output of each converter is independent of other converter modules in the topology. As the number of converter modules in this topology increase the output voltage appears to be almost continuous [2].
2.4 One-to-Many Topology

In the proposed one-to-many topology, the output of a single converter module in the first stage provides the input to a number of converter modules in the next stage as shown in Figure 2-8. All the outputs of the converter modules in the second stage are connected in series and fed to the DC bus to obtain different steps of output voltages. Though the converter modules considered are identical in operation, the ratings of the converter modules change from the first stage to the second stage as the current levels change. The maximum output voltage as well as the number of
steps of output voltages is more in this case when compared to general multilevel DC-DC converter system.

![One-to-Many Topology of Multilevel DC-DC Converters](image)

**Figure 2-8: One-to-Many Topology of Multilevel DC-DC Converters**

### 2.5 Cascaded Topology

In the cascaded topology, different converter modules are arranged in the multiple stages in a cascaded arrangement as shown in Figure 2-9. In this topology each converter module typically drives two converter modules in the next stage. All the converter modules in the last stage are connected in series. Summing the output
voltages of all converter modules in the last stage produces the system output voltage. Converter modules with different switch ratings are chosen in each stage for optimal performance.

Figure 2-9: Cascaded Topology of Multilevel DC-DC Converter Modules

To obtain a given output voltage level, there are multiple switching combinations possible for the intermediate and final stage converter modules. Since the switch losses are one of the significant losses in the converter module operation, the selection of a switching combination with minimum number of operating switches yields better
2.5.1 General Cascaded System Topology

In a general cascaded topology shown in Figure 2-9, there are an odd number of converter modules. However, with minor modifications to this standard cascaded topology, three different multilevel DC-DC cascaded system topologies that have an even number of converters are proposed by adding one additional converter module to the general cascaded topology. The cascaded topology with an even number of converter modules is dependent on the placement of the additional converter module to the standard cascaded topology. This placement can improve the number of voltage levels, the range of output voltages or reduce the output voltage ripple. The three even cascaded converter topologies are detailed in this section.

2.5.2 General Cascaded System Topology with Even Number of Converter Modules with Additional Module in the Last Stage

In the first even number cascade topology shown in Figure 2-10, the additional converter module is connected to the output of a converter module in the stage just before the last stage. This arrangement increases the range of the output voltage and increases the number of steps of output voltages.
2.5.3 General Cascaded System Topology with Even Number of Converter Modules and the Additional Module Driven by Individual Voltage Source

For a cascaded topology with an even number of converter modules, the additional converter module can also be connected in series in the last stage with an individual
voltage source as shown in Figure 2-11. This arrangement may need another voltage source or it can be driven by the same voltage source that drives the whole cascaded system.

Figure 2-11: Cascaded topology of Multilevel DC-DC Converter Modules with Even Number of Converter Modules and the Additional Module Driven by Individual Voltage Source
2.5.4 General Cascaded System Topology with Even Number of Converter Modules with Additional Module in First Stage

Another cascaded topology with an even number of converter modules, shown in Figure 2-12, has the added converter module in the first stage, i.e. in the first stage each converter module drives only one converter module breaking the basic rule of the cascaded system that each converter drives the other two converters in the next stage.

Figure 2-12: Cascaded Topology of Multilevel DC-DC Converter Modules with Even Number of Converter Modules with Additional Module in First Stage
2.6 Summary

This chapter presents different topologies of multilevel converters. Two new topologies, namely, one-to-many topology and cascaded topology, were presented along with the existing general multilevel DC-DC converter system topology. In addition, multiple implementations of cascaded topologies with an even number of converter modules were presented.
Chapter 3

Comparisons of Multilevel DC-DC Converter Systems

3.1 Introduction

This chapter presents the comparisons of different implementations of multilevel DC-DC converter systems in terms of the following performance criteria: minimum output voltage, maximum output voltage, number of possible steps of output voltages, minimum number of switches operated for a given output voltage, and ripple voltages.

3.2 Comparisons of Different Multilevel DC-DC Converter Systems

Several generalizations and formulations are derived for each topology to make comparisons of each converter system topology in order to determine which converter is better to use for a given set of requirements.
3.2.1 General Topology

The maximum voltage for a general multilevel DC-DC converter topology [2] comprising of N converter modules is obtained when each module can output its maximum voltage of $2V_{in}$. So, the maximum output voltage is $2NV_{in}$.

On the other hand, each module can have a minimum output voltage of $V_{in}$. If each module is operating at the minimum voltage, the output voltage will have its least value. Therefore, the minimum output voltage is $NV_{in}$.

Therefore, the range of output voltage falls between the output voltages $[NV_{in}, 2NV_{in}]$.

The number of steps of output voltages within this range of values is $N+1$ as all the voltages from $NV_{in}$ and $2NV_{in}$ with integer values of $N$ are possible.

In a converter module, to generate an output of $V_{in}$, the switches S1 and S4 are ON and the switches S2 and S3 are OFF. There is no switching taking place in this state. However, to generate the output voltage of $2V_{in}$, all the switches S1, S2, S3, and S4 in the converter module are operated (although not simultaneously). For the converter system to output any voltage $XV_{in}$, the number of switches operated within the converter modules is $2X$, where

$$2NV_{in} \geq XV_{in} \geq NV_{in} \quad (3.1)$$

During the operation of the converter module, the capacitors within the module supply current to the load. As the capacitors discharge, there will be voltage ripples generated. Of the N modules present, to generate a voltage of $XgV_{in}$, $(Xg-N)$ are operating with output voltage of $2V_{in}$, while the rest $(2N-Xg)$ are operating with an output voltage of $V_{in}$. The ripple voltage generated depends on whether the converter module is operating at output voltage level of $V_{in}$ or $2V_{in}$. If $\Delta V_{2V_{in}}$ is the ripple voltage for a given converter module while it is operating at $2V_{in}$ and $\Delta V_{V_{in}}$ is
the ripple voltage for the converter module while the output voltage is $V_{in}$, then the ripple voltage is given by

$$V_{ripple} = (X_g - N)\Delta V_{2V_{in}} + (2N - X_g)\Delta V_{V_{in}}$$

(3.2)

Consider a general topology with three, five, seven, and ten converter modules and the input voltage of 1V. All the results from the formulations are presented in a tabular form in Table 3.1.

Table 3.1: Critical Parameters for a General Cascaded Topology with Different Number of Converter Modules

<table>
<thead>
<tr>
<th>Number of Converter modules</th>
<th>Number of steps of possible output voltages</th>
<th>Maximum output voltage</th>
<th>Minimum output voltage</th>
<th>Output voltages obtained</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>4</td>
<td>6V</td>
<td>3V</td>
<td>3V,4V,5V,6V</td>
</tr>
<tr>
<td>4</td>
<td>5</td>
<td>8V</td>
<td>4V</td>
<td>4V,5V,6V,7V,8V</td>
</tr>
<tr>
<td>7</td>
<td>8</td>
<td>14V</td>
<td>7V</td>
<td>7V,8V,9V,10V,11V,12V,13V,14V</td>
</tr>
<tr>
<td>10</td>
<td>11</td>
<td>20V</td>
<td>10V</td>
<td>10V,11V,12V,13V,14V,15V,16V,17V,18V,19V,20V</td>
</tr>
</tbody>
</table>

3.2.2 One-to-Many Topology

For the one-to-many topology made of $N$ converter modules, there will be $(N-1)$ modules at the second output stage. These modules are driven by one module from the first level that can output either $V_{in}$ or $2V_{in}$. Similarly, the modules in the output stage can take the resultant voltage (either $V_{in}$ or $2V_{in}$) and scale it by a factor of 1.
or 2. Therefore, the output stage converter modules can have output voltages of $V_{in}$, $2V_{in}$, or $4V_{in}$. Thus the maximum output voltage is given as $4(N-1)V_{in}$.

The minimum output voltage in one-to-many topology with N multilevel DC-DC converter modules is given by $(N-1)V_{in}$.

The range of output voltages is given by $[(N-1)V_{in}, 4(N-1)V_{in}]$

Since each of the $(N-1)$ converter modules can deliver two possible values of output voltage, and the input presented to these modules is either $V_{in}$ or $2V_{in}$, the number of possible steps within the range of the output voltage is determined based on the output state of the converter module in the first stage. All voltages in increments of $V_{in}$ within the range of $(N-1)V_{in}$ to $2(N-1)V_{in}$ are possible with the output voltage of first stage converter being $V_{in}$. If the output voltage of the first stage is $2V_{in}$ then additional steps in increments of $2V_{in}$ in the voltage range are possible in the voltage range from $(2N)V_{in}$ to $4(N-1)V_{in}$.

The steps in increment of $V_{in}$ for the output is given within the output voltage range as specified in eqn 3.3.

$$2(N - 1)V_{in} \geq V_{out} \geq (N - 1)V_{in} \quad (3.3)$$

Similarly, the steps in increments of $2V_{in}$ are valid for the voltage range as specified below.

$$4(N - 1)V_{in} \geq V_{out} \geq 2NV_{in} \quad (3.4)$$

The total number of steps of output voltages for one-to-many topology with N number of converter modules is given by sum of steps $(N+N-1)= 2N-1$.

For the output voltage range specified in equation 3.3, the first stage converter module has a output voltage of $V_{in}$, and the number of switches operated for any
given output voltage $XV_{in}$ is given by $2X+2$, where

$$2(N - 1)V_{in} \geq XV_{in} \geq (N - 1)V_{in} \quad (3.5)$$

The number of switches operated for any given output voltage $XV_{in}$ is given by $X+4$. Note that the output voltage changes in increments of $2V_{in}$ in this range of output voltage values.

$$4(N - 1)V_{in} \geq XV_{in} \geq 2NV_{in} \quad (3.6)$$

Of the N modules present, to generate a voltage of $X_gV_{in}$, $(X_g-N-1)$ switches are operating with output voltage of $2V_{in}$, while the rest $(2(N-1)-X_g)$ are operating with an output voltage of $V_{in}$. The ripple voltage generated depends on whether the converter module is operating at output voltage level of $V_{in}$ or $2V_{in}$. If $\Delta V_{2V_{in}}$ is the ripple voltage for a given converter module while it is operating at $2V_{in}$ and $\Delta V_{V_{in}}$ is the ripple voltage for the converter module while the output voltage is $V_{in}$, then the given output voltage $X_gV_{in}$ is given by

$$V_{\text{ripple}} = (X_g - N - 1)\Delta V_{2V_{in}} + (2(N - 1) - X_g)\Delta V_{V_{in}} \quad (3.7)$$

Table 3.2 presents the different performance criteria for a one-to-many topology that uses three, four, and seven converter modules respectively.
Table 3.2: Comparison of One–to–Many Topology with 3, 4, and 7 Converter Modules

<table>
<thead>
<tr>
<th>Number of Converter modules</th>
<th>Number of steps of possible output voltages</th>
<th>Maximum output voltage</th>
<th>Minimum output voltage</th>
<th>Output voltages obtained</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>5</td>
<td>8V</td>
<td>2V</td>
<td>2V,3V,4V,6V,8V</td>
</tr>
<tr>
<td>4</td>
<td>7</td>
<td>12V</td>
<td>3V</td>
<td>3V,4V,5V,6V,8V,10V,12V</td>
</tr>
<tr>
<td>7</td>
<td>13</td>
<td>24V</td>
<td>6V</td>
<td>6V,7V,8V,9V,10V,11V,12V,13V,14V,16V,18V,20V,22V,24V</td>
</tr>
</tbody>
</table>

3.2.3 Cascaded Topology

A cascaded topology comprises of multiple stages of converter modules that are connected together as explained in Chapter 2. Let us consider a cascaded topology with L number of levels. The number of converter modules in any given level i is given by $2^{i-1}$, where $i \leq L$. The total number of converter modules in the cascaded topology with L number of levels is given by

$$N = \sum 2^{i-1} = 2^L - 1$$

The modules in the final stage are connected in series to generate the output voltage. The minimum voltage that is obtained is when all these modules have an output voltage of $V_{in}$. Since the $L^{th}$ stage is the final stage, it consists of $2^{L-1}$ modules. Therefore, the minimum output voltage for a cascaded topology with L number of stages is $2^{L-1}V_{in}$.

The largest possible voltage of a module is obtained if every module in the path
from the input source to the final stage is increasing the voltage by a factor of 2. Since there are \((L-1)\) stages, the maximum possible voltage for a module in \(L^{th}\) stage is \(2^L V_{in}\). The maximum output voltage for any general cascaded topology is obtained when all the modules in \(L^{th}\) stage have the maximum possible voltage. Therefore, the maximum voltage is \(2^{2L-1}V_{in}\).

The range of output voltage is given by \([2^{L-1}V_{in}, 2^{2L-1}V_{in}]\)

To determine the number of steps of output voltages for any general cascaded topology with \(L\) number of levels, a MATLAB code was developed because same output voltage can be obtained in many combinations. This program finds different possible output voltages for any number of levels for a cascaded topology is presented in Appendix A.

As the number of stages increases, the voltage ripples keeps on adding up in each stage. This sets a practical limit to the number of possible cascaded stages that can be used.

The prior cascaded multilevel system analyses are for the odd number of converter modules. However, in cascaded topology with even number of converter modules, the basic rule of cascading is ruled out.

The cascaded topology with added converter module in the last stage driven by the converter module in the prior stage is capable of generating maximum range of output voltage when compared to all other even cascaded topologies. The maximum output voltage this cascaded topology can generate is \([(2^{2L-1} + 2^{L-1})V_{in}]\).

The cascaded topology with an even number of converter modules with the added converter module in the last stage driven by an individual voltage source is capable of outputting maximum steps of output voltages. For this topology, the maximum output voltage is \(2^{2L-1}V_{in} + 2V_{in}\).

The cascaded topology with the last converter module in the first level will have reduced ripple voltage compared to other cascaded even topologies.
The MATLAB code in Appendix A finds the total number of converter modules of by summing the modules in each of the stages. To obtain the output voltage, there are two conditions tested for each converter operation:

1. When switches S1 and S4 are set ON and S2 and S3 are set OFF i.e. when converter module output is $V_{in}$ a variable S is assigned a value of 0.

2. When switches S1, S2, S3 and S4 are operated to output twice the input voltage the variable S is assigned a value of 1.

All the values of variable S for individual converter modules in each case are stored in a matrix. Based on the value of the S for each converter module in the cascaded topology, the output voltage is evaluated from the first stage to the final stage. The evaluated output voltages of the converters in the last stage are added to obtain the system output voltage. The number of switches that are operated in the converter module are also updated to two switches when S is 0 and four switches when S is 1. The MATLAB code can produce all the possible outcomes given number of levels L.

For example, let us consider a general cascaded topology with 2 and 3 levels and the input voltage to the converter modules as $V_{in}$. The voltages that are possible for a 2 level general cascaded topology are as shown in Table 3.3. The voltages that are possible for a 3 level general cascaded topology are as shown in Table 3.4.
Table 3.3: Combination of Output Voltages and Minimum Number of
Switches Operated for 2-stage General Cascaded Topology

<table>
<thead>
<tr>
<th>Output voltage</th>
<th>Different Combination of voltages</th>
<th>Minimum Number of Switches Operated for the Output Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>$2V_{in}$</td>
<td>(1,1)</td>
<td>6</td>
</tr>
<tr>
<td>$3V_{in}$</td>
<td>(1,2)</td>
<td>8</td>
</tr>
<tr>
<td>$4V_{in}$</td>
<td>(2,2)</td>
<td>8</td>
</tr>
<tr>
<td>$6V_{in}$</td>
<td>(2,4)</td>
<td>10</td>
</tr>
<tr>
<td>$8V_{in}$</td>
<td>(4,4)</td>
<td>12</td>
</tr>
</tbody>
</table>

### 3.3 Results and Discussions

The results of the code implemented in MATLAB with the number of stages being 2, 3 and 4 are shown in the Table 3.5 for an input voltage of 1V. The code presents the values of maximum output voltage, minimum output voltage, number of steps of output voltages, all the possible voltages for the given cascaded topology with given number of stages and number of switches operated for outputting any given possible voltage. Table 3.6 presents the steps of output voltages, maximum and minimum output voltages, and different possible voltages for the different cascaded systems with even number of converter modules for two stages. Among all the cascaded converter systems with even number of converter modules, the converter system with the last added module in its last stage has maximum output voltage and the converter system with the additional module with individual voltage source has maximum number of
steps of output voltage respectively.

As the number of stages of cascaded topology increase, complexity of the system increases at a faster rate. Another disadvantage of the multilevel converter topologies is that they need semiconductor devices with significantly different blocking voltages at each stage. They also have complex control schemes and a large number of gate driver circuits. Also, as the number of stages increase, there is a corresponding increase to the ripples in the output voltage.

3.4 Summary

In this chapter comparisons were made for different converter system topologies. The cascaded topology has more possible output voltages and range of output voltage over general multilevel and one-to-many topologies for the same number of converter modules.
Table 3.4: Combination of Output Voltages for Converters in Last Stage and Minimum Number of Switches Operated for 3-stage Cascaded Topology

<table>
<thead>
<tr>
<th>Output voltage</th>
<th>Different Combination of Output Voltages for Converters in Last Stage</th>
<th>Minimum Number of Switches Operated for the Output Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>$4V_{in}$</td>
<td>(1,1,1,1)</td>
<td>14</td>
</tr>
<tr>
<td>$5V_{in}$</td>
<td>(1,1,1,2)</td>
<td>16</td>
</tr>
<tr>
<td>$6V_{in}$</td>
<td>(1,1,2,2)</td>
<td>18</td>
</tr>
<tr>
<td>$7V_{in}$</td>
<td>(1,2,2,2)</td>
<td>18</td>
</tr>
<tr>
<td>$8V_{in}$</td>
<td>(1,1,2,4)</td>
<td>18</td>
</tr>
<tr>
<td>$9V_{in}$</td>
<td>(1,2,2,4)</td>
<td>20</td>
</tr>
<tr>
<td>$10V_{in}$</td>
<td>(1,1,4,2),(2,2,2,4)</td>
<td>18</td>
</tr>
<tr>
<td>$11V_{in}$</td>
<td>(1,2,4,4)</td>
<td>22</td>
</tr>
<tr>
<td>$12V_{in}$</td>
<td>(2,2,4,4)</td>
<td>18</td>
</tr>
<tr>
<td>$14V_{in}$</td>
<td>(2,4,4,4)</td>
<td>20</td>
</tr>
<tr>
<td>$16V_{in}$</td>
<td>(4,4,4,4),(2,2,4,8)</td>
<td>20</td>
</tr>
<tr>
<td>$18V_{in}$</td>
<td>(2,4,4,8)</td>
<td>18</td>
</tr>
<tr>
<td>$20V_{in}$</td>
<td>(2,2,8,8),(4,4,4,8)</td>
<td>22</td>
</tr>
<tr>
<td>$22V_{in}$</td>
<td>(2,4,8,8)</td>
<td>24</td>
</tr>
<tr>
<td>$24V_{in}$</td>
<td>(4,4,8,8)</td>
<td>24</td>
</tr>
<tr>
<td>$28V_{in}$</td>
<td>(4,8,8,8)</td>
<td>26</td>
</tr>
<tr>
<td>$32V_{in}$</td>
<td>(8,8,8,8)</td>
<td>28</td>
</tr>
</tbody>
</table>
Table 3.5: Critical Parameters for Different Level Implementation of General Cascaded Topology

<table>
<thead>
<tr>
<th>Number of Stages Implemented</th>
<th>Number of Steps of Possible Output voltages</th>
<th>Maximum Output Voltage</th>
<th>Minimum Output Voltage</th>
<th>Number of Converter Modules</th>
<th>Output voltages Obtained</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>5</td>
<td>8V</td>
<td>2V</td>
<td>3</td>
<td>2V,3V,4V,6V,8V</td>
</tr>
<tr>
<td>3</td>
<td>17</td>
<td>32V</td>
<td>4V</td>
<td>7</td>
<td>4V,5V,6V,7V,8V,9V,10V,11V,12V,14V,16V,18V,20V,22V,24V,28V,32V</td>
</tr>
</tbody>
</table>
Table 3.6: Critical Parameters for 2-stage Implementation of Converter Systems with Even Number of Modules

<table>
<thead>
<tr>
<th>Type</th>
<th>Number of steps of possible output voltages</th>
<th>Maximum output voltage</th>
<th>Minimum output voltage</th>
<th>Output voltages obtained</th>
</tr>
</thead>
<tbody>
<tr>
<td>last converter modules in the last stage</td>
<td>7</td>
<td>12V</td>
<td>3V</td>
<td>3V,4V,5V,6V,8V,10V,12V</td>
</tr>
<tr>
<td>last converter module with the individual voltage source</td>
<td>9</td>
<td>10V</td>
<td>2V</td>
<td>2V,3V,4V,5V,6V,7V,8V,9V,10V</td>
</tr>
<tr>
<td>last converter modules in the first stage</td>
<td>7</td>
<td>8V</td>
<td>2V</td>
<td>2V,3V,4V,5V,6V,7V,8V</td>
</tr>
</tbody>
</table>
Chapter 4

Different Multilevel DC-DC Converter Modules

4.1 Introduction

In this chapter two new modified multilevel DC-DC converter modules are presented. The converter modules decrease the transition currents during the output voltage transition from one level to the other for a given transition cycle. One of the presented multilevel converter modules facilitates the implementation of the cascaded converter system topologies of the previous chapter.

4.2 Problem Statement

There are several problems with switching patterns in the implementation of the cascaded topology of multilevel DC-DC converter modules. The cascaded multilevel converters provide superior performance in terms on voltage range and number of voltage levels as compared to other implementations [10]. The converter module from [5] will not provide the needed isolation to implement cascaded multilevel topologies. For example, consider the cascaded configuration shown in Figure 4–1. Let the module
in the first stage and have the drives two modules in the second stage. Both the modules driven are parallel in connection and have the same return path for the current i.e. when the current flows in the first converter module as shown in the Figure 4-1, the same return current flow is expected even in the second module driven as they are connected in parallel. If the first driven converter module outputs $4V_{in}$, the second driven can not output $2V_{in}$. Hence, there is a problem in obtaining desired output voltage and which can be served by employing a switch by isolation from one stage to the other.

![Diagram of cascaded topology](image)

Figure 4-1: Problems with Switching Patterns in the Implementation of Cascaded Topology using the General Converter Module

Due to this switching pattern desired output voltage cannot be achieved. The new
topologies presented in this paper overcome the problems with this switching pattern. The switching pattern problems in the implementation of cascaded system topology using basic converter module is as shown in the Figure4 -1. The two topologies presented to over this switching pattern problems.

4.3 General Multilevel DC-DC Converter Topology

This is the same module discussed in the previous chapters but includes the parasitic inductances of the cable and the equivalent series inductance (ESL) of the capacitor.

![General Multilevel DC-DC Converter Module](image)

Figure 4-2: General Multilevel DC-DC Converter Module

These inductors are included to model the impact of the parasitic inductances on
the transient currents when the switches are operated during the transition of the module output voltage from one level to another.

4.4 Multilevel DC-DC Converter Module with Switches in Series with Capacitors

In the first new topology of multilevel DC-DC converter module, two additional switches are added to the converter module as shown in Figure 4-3. The first switch, S5, is added in series with the capacitor C1, switch S1, and switch S3. The second switch, S6, is added in series with switches S2 and S4 as shown in Figure 4-3.

![Figure 4-3: Multilevel DC-DC Converter Module with Switches in Series with Capacitors](image-url)
During the transition between the two voltage levels, switches S5 and S6 are OFF as shown in the control signals in Figures 4-5 and 4-6. Then the charged capacitors will deliver the current to the load. Since it is possible for the load to be not connected directly to the input voltage sources and/or to the stages prior to the output stages, there is better control of the operation of the converter modules. As no current flows directly from the input source to the load, its current needs are served by the capacitors. The transient currents are also reduced during the switching between voltage levels. Hence, the life span of the converter module potentially increases compared to the Pengs multilevel DC-DC converter.

4.5 Multilevel DC-DC Converter Module with Switches before Capacitors

The second topology of multilevel DC-DC converter module presented has two additional switches as shown in Figure 4-4. The first switch, S5, is added in series with the capacitor C1, switch S1, and switch S3, and the second switch, S6, is added in series with switches S2 and S4.

During the transition of the output voltage, the capacitors are being disconnected from being charged i.e., two switches S5 and S6 are in OFF mode such that the capacitors are disconnected from being charged. During this time, the input directly supplies the current to the load. The switches S5 and S6 are in the ON state as long as the converter module operates with a constant output voltage (either at $V_{in}$ or $2V_{in}$) and they are maintained in the OFF state when the transition takes place from $2V_{in}$ to $V_{in}$ and vice versa.
The control signals during output transition from $V_{in}$ to $2V_{in}$ are shown in Figure 4-5 and from $2V_{in}$ to $V_{in}$ are shown in Figure 4-6 respectively. The control signals for the four switches from S1 to S4 are similar for all three topologies. For the topologies presented, the switches S5 and S6 are OFF during the transition period and are ON during the steady output condition. Thus, it facilitates reduction of transient currents and the transient times.

The main advantage of the two proposed topologies is that for the same transition times of the control signals, they have a considerable reduction in transient currents when compared to the existing converter module. Since there is significant reduction in transition currents, the lifetime of the new converters is expected to improve. When the switches S5 and S6 are OFF during the transition time, the input voltage directly
supplies the current to the load. Thus, this topology is not suited for implementing cascaded multilevel converters.

Figure 4-5: Control Signals During the Transition from $V_{in}$ to $2V_{in}$ for New Topologies

Figure 4-6: Control Signals During the Transition from $2V_{in}$ to $V_{in}$ for New Topologies
The control signals for the switches S1, S2, S3, and S4 are gradually changed in order to make the switches S1 and S3 ON and switches S2 and S4 OFF at the same time and vice versa. Once the duty cycle of 50% is obtained, the capacitors C1 and C2 can be charged alternatively to obtain $2V_{in}$ output voltage. In these topologies, the switches S5 and S6 are in the OFF position as long as the transition is taking place.

4.6 Summary

Two new topologies of multilevel DC-DC converter modules which facilitate the implementation of the cascaded and/or one-to-many topology of the multilevel converters were presented in this chapter. One of the two multilevel converter modules presented in this chapter not only facilitates the implementation of the cascaded converter system module implementation, but decrease the transient currents during the transition of output voltage from one voltage level to the other. The other converter module only decreases the transient currents during output voltage transition.
Chapter 5

Simulation Results of Operational and Transition Losses in Multilevel Converter Modules

In this chapter the comparison of the different losses in the operation of three topologies of multilevel DC-DC converter modules is presented. The output waveforms for each case during transition of the output voltage between the voltage levels, and during the steady state output voltage at $V_{in}$ and $2V_{in}$ are presented. The results are presented for both current load and resistive load for all converter modules.

5.1 Introduction

In this section, the comparisons of the different losses in the operation of three different topologies of multilevel DC-DC converter modules are presented. Along with the losses the output waveforms for each case during transition of the output voltage, steady state output voltage while outputting $2V_{in}$, steady state output voltage while outputting $V_{in}$ for both current load and resistive load are presented.
5.2 Different Operational Losses in a DC-DC Converter Modules

There are different losses that occur during the operation of a converter module. The losses considered are switch losses, switching losses, diode losses, transition losses, and capacitor charging and discharging losses. The impact of the ripples in the output voltage is also studied.

5.2.1 Switching Losses

The losses that occur during the switching of the transistor are the switching losses i.e., at the instance when the transistor switch is turned ON or OFF. The switching losses can be neglected for very low frequencies but are not negligible at high frequencies. Power losses at high frequency are managed by bigger, thermal optimized semiconductors and heat sink or using optimum component technology [35]. In state1, while the output voltage is $V_{in}$, only two (four for the proposed converter modules) switches are operated, whereas in the case of the output voltage of $2V_{in}$ all the switches in the converter module are operated at a high frequency switching between state2 and state3. Therefore, the switching losses are significantly more while output is $2V_{in}$ rather than $V_{in}$.

5.2.2 Switch Losses

The conduction or leakage losses occur in the transistor switch operating is either in ON mode or OFF mode is the switch loss. The main contribution is due to the losses from the drain-source resistance of the transistor while it is conducting current. Conduction loss in the converter module can be significantly reduced by using switches with small on-state resistance.
Typically, the combination of switching and switch losses account for more than 70% of the total power losses in the converter module.

5.2.3 Diode Losses

The voltage drop across the diode is primarily responsible for the losses in the diode during conduction. In addition, the diode reverse recovery mechanism results in power loss. Typically, the diode losses account to less than .5% of the total losses in a converter module.

5.2.4 Capacitor Charging and Discharging Losses

The losses are caused during the charging and discharging of the capacitor. These losses are primarily due to non-idealities in the capacitor components. The capacitor losses contribute to less than 1% of the total losses.

Since the stored charge in the capacitor maintains the output voltage when the input source is not directly connected to the output current, there are small variations or ripples in the output voltage. These ripple voltages contribute to the distortion in the output voltage and must be reduced. The ripples in the output waveform are affected by the load on the DC-DC converter. As the load increases, the voltage ripples increase and vice versa.

5.2.5 Transition Losses

The losses that occur during the transition in a converter operation from one voltage level to another voltage level are known as transition losses. Since the DC-DC converter modules can output two voltages $V_{in}$ and $2V_{in}$, the transition losses are only between these levels, i.e., during the transition from $V_{in}$ to $2V_{in}$ and from $2V_{in}$ to $V_{in}$. Due to the high transient currents when transitioning the output voltage
from $V_{in}$ to $2V_{in}$, a small inductor can be added to the converter module to reduce transient currents and transient losses. The transition losses contribute around 30% of the total losses.

The longer the transition in switching from one level to next, the larger the transition power loss. Large transition currents also create distortions in the output waveform. Therefore, reducing transient currents during switching and reducing transition time is an important criterion in the design of the DC-DC converters. The voltage ripples do not count under the losses but voltage ripples cause distortions in the output voltage, which results in fluctuating output voltage.

### 5.3 Comparison of SPICE Implemented Results of the Different Multilevel DC-DC Converter Modules

The converter module proposed by Peng is referred to as topology1, the new converter topology with switches in series is referred to as topology2, and the new topology with switches before capacitors is referred to as topology3 in further discussions in this chapter. Circuit simulations of the three topologies have been performed to study the losses during the operation for 250W multilevel DC-DC converter topologies. The switches used are power MOSFET module IPB025N10N3, and 20 mF capacitors are used for both C1 and C2. The loads used are .4 ohms for the resistive load and 25A for the current load. The topology1 converter module has four NMOS transistor switches whereas topology2 and topology3 have six NMOS transistors each. The specifications of the diodes and the transistors used to build the converter module are presented in the Appendix B. Comparison of all the losses calculated from the output waveforms of the simulations of each converter topology are presented in the Tables 5.1 and 5.2.
for outputting $2V_{in}$ and $V_{in}$ respectively for the current load. Similarly in Tables 5.3 and 5.4 compare the different topologies for outputting $V_{in}$ and $2V_{in}$ respectively for the resistive load.

The switching losses in topology2 and topology3 are high compared to topology1 because of the presence of the two extra switches. The transition losses are reduced but the overall power loss is more in the two new topologies. The difference in efficiency is less than 1% for topology3 as compared to topology1. The efficiency reduces between 1-3% for topology2 as compared to topology1. As expected, the ripple voltage of topology3 is significantly larger than topology1 or topology2 because the capacitors are disconnected from the load and cannot compensate for the voltage variations due to transient current surges.

Taking the transition time during switching of voltage levels and the transient current surges into consideration, topology3 is better than topology2 and topology1 in that order.

The simulation results for the current load of each topology are presented as the diagrams show in Figure 5-1 through Figure 5-15. The diagrams show the steady state waveforms when outputting $V_{in}$, and $2V_{in}$, the transition from outputting $V_{in}$ to $2V_{in}$, the transition from $2V_{in}$ to $V_{in}$ and the transient currents. The Figures 5-1 through 5-5 provide the information for the steady state output voltage, output voltage transition, and transient currents for topology1. The Figure 5-6 through 5-10 provides the steady state output voltage, output voltage transition and transient currents for topology2. The Figure 5-11 through 5-15 provides the steady state output voltage, output voltage transition and transient currents for topology3.

The transient currents are very high in topology1 when compared to topology2 and topology3 and this can be inferred from the simulation diagrams. The transient current is constantly high in topology1, whereas in topology2 and topology3 we have reduced transient currents. All losses are almost the same for topology1 and topology3.
when the output voltage is $V_{in}$ because the switches S5 and S6 are open during the transition and the load is directly connected to the input source. So there are no switching and switch losses for these switches. During transition for topology 2, when switches S5 and S6 are open, the capacitors provide current to the load and hence, the losses are more in this topology compared to others.

Table 5.1 presents different losses for the current load for all the topologies while the output voltage is $2V_{in}$. The output voltage is better for topology 1 when compared to topology 2 and topology 3 as there are two more switches involved in topology 2 and topology 3. Switching losses contribute major losses and it is high in topology 2 when compared to the other two topologies as the switching operation is more in topology 2 than the other two converter modules. The diode losses are negligible.

Table 5.1: Comparison of Different Losses in Three Different Topologies for Outputting $2V_{in}$ for Current Load

<table>
<thead>
<tr>
<th>No</th>
<th>Types of Losses</th>
<th>Topology 1</th>
<th>Topology 2</th>
<th>Topology 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Output Voltage (Avg)</td>
<td>9.3391V</td>
<td>9.2054V</td>
<td>9.2412V</td>
</tr>
<tr>
<td>2</td>
<td>Switch and Switching Losses</td>
<td>10.057W</td>
<td>14.8005W</td>
<td>12.508W</td>
</tr>
<tr>
<td>3</td>
<td>Capacitor Charging and Discharging Losses</td>
<td>.635mW</td>
<td>.631mW</td>
<td>.633mW</td>
</tr>
<tr>
<td>4</td>
<td>Diode Losses</td>
<td>218.26uW</td>
<td>36.54uW</td>
<td>225.43uW</td>
</tr>
<tr>
<td>5</td>
<td>Voltage Ripples</td>
<td>10.1mV</td>
<td>6.98mV</td>
<td>480mV</td>
</tr>
<tr>
<td>6</td>
<td>Total Losses</td>
<td>16.34W</td>
<td>19.82W</td>
<td>18.8W</td>
</tr>
<tr>
<td>7</td>
<td>Efficiency</td>
<td>93.45%</td>
<td>92.07%</td>
<td>92.47%</td>
</tr>
</tbody>
</table>
Table 5.2: Comparison of Different Losses in Three Different Topologies for Outputting $V_{in}$ for Current Load

<table>
<thead>
<tr>
<th>No</th>
<th>Types of Losses</th>
<th>Topology 1</th>
<th>Topology 2</th>
<th>Topology 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Output Voltage (Avg)</td>
<td>4.8527V</td>
<td>4.7303V</td>
<td>4.8526V</td>
</tr>
<tr>
<td>2</td>
<td>Switch and Switching Losses</td>
<td>2.433W</td>
<td>4.866W</td>
<td>2.433W</td>
</tr>
<tr>
<td>3</td>
<td>Capacitor Charging and Discharging Losses</td>
<td>.635mW</td>
<td>.631mW</td>
<td>.633mW</td>
</tr>
<tr>
<td>4</td>
<td>Diode Losses</td>
<td>16.525pW</td>
<td>12.525pW</td>
<td>101pW</td>
</tr>
<tr>
<td>5</td>
<td>Voltage Ripples</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>6</td>
<td>Total Losses</td>
<td>3.68W</td>
<td>6.74W</td>
<td>3.68W</td>
</tr>
<tr>
<td>7</td>
<td>Efficiency</td>
<td>97.056%</td>
<td>94.608%</td>
<td>97.056%</td>
</tr>
</tbody>
</table>

Table 5.2 presents different losses for the current load for all the topologies, while the output is $V_{in}$. However the output voltage is closer to the input voltage for topology 1 when compared to topology 2 and topology 3 as there are two more switches involved in these topologies. Switching losses contribute major losses and it is high in topology 2 when compared to other two topologies as switching operation is more in topology 2 than other two topologies.

There are small voltage ripples in all the topologies while output voltage is $V_{in}$, as the output voltage keeps on building up constantly. As the input source directly supplies the power to the load the voltage keeps on building across the capacitances as long as the switches S1 and S4 are in ON position i.e. while the converter modules are outputting $V_{in}$. 

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Table 5.3: Comparison of Different Losses in Three Different Topologies while Outputting $2V_{in}$ for Resistive Load

<table>
<thead>
<tr>
<th>No</th>
<th>Types of Losses</th>
<th>Topology 1</th>
<th>Topology 2</th>
<th>Topology 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Output Voltage(Avg)</td>
<td>9.391V</td>
<td>9.2638V</td>
<td>9.2946V</td>
</tr>
<tr>
<td>2</td>
<td>Switch and Switching Losses</td>
<td>8.858W</td>
<td>12.727W</td>
<td>10.874W</td>
</tr>
<tr>
<td>3</td>
<td>Capacitor Charging and Discharging Losses</td>
<td>.559mW</td>
<td>.541mW</td>
<td>.547mW</td>
</tr>
<tr>
<td>4</td>
<td>Diode Losses</td>
<td>174.92uW</td>
<td>31.3uW</td>
<td>174.76uW</td>
</tr>
<tr>
<td>5</td>
<td>Voltage Ripples</td>
<td>9.8mV</td>
<td>6.35mV</td>
<td>431mV</td>
</tr>
<tr>
<td>6</td>
<td>Total Losses</td>
<td>14.39W</td>
<td>17.01W</td>
<td>16.25W</td>
</tr>
<tr>
<td>7</td>
<td>Efficiency</td>
<td>93.85%</td>
<td>92.65%</td>
<td>93%</td>
</tr>
</tbody>
</table>

Tables 5.3 and 5.4 presents the output voltage, losses, ripples and efficiency for all the three topologies, while the output voltage is $2V_{in}$ and $V_{in}$, respectively, for a resistive load. The output voltage in topology1 is higher compared to other two topologies, as there are two more switches operated in those topologies. Similarly, the same is reflected in comparison of switch and switching losses, as they comprise more than 70% of the losses, these losses are less in topology1 when compared to topologies 2 and 3. The diode losses are negligible and capacitor charging and discharging losses are not significant for all topologies.

The voltage ripples are minimal for all the topologies while the output voltage is $V_{in}$ as the voltage keeps on building up constantly. As the input source directly supplies the power to the load the voltage keeps on building across the capacitances as long as the switches S1 and S4 are in ON position i.e. while the converter modules output is $V_{in}$. The efficiency of topology1 is higher compared to topology2 and
topology3 as there are two more switches operated in topology2 and topology3.

Table 5.4: Comparison of Different Losses in Three Different Topologies for Outputting $V_{in}$ for Resistive Load

<table>
<thead>
<tr>
<th>No</th>
<th>Types of Losses</th>
<th>Topology 1</th>
<th>Topology 2</th>
<th>Topology 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Output Voltage (Avg)</td>
<td>4.9274V</td>
<td>4.8687V</td>
<td>4.927V</td>
</tr>
<tr>
<td>2</td>
<td>Switch and Switching Losses</td>
<td>590.91mW</td>
<td>1.1539mW</td>
<td>591mW</td>
</tr>
<tr>
<td>3</td>
<td>Capacitor Charging and Discharging Losses</td>
<td>.635W</td>
<td>.631mW</td>
<td>.633mW</td>
</tr>
<tr>
<td>4</td>
<td>Diode Losses</td>
<td>16.73pW</td>
<td>28.34pW</td>
<td>49.71pW</td>
</tr>
<tr>
<td>5</td>
<td>Voltage Ripples</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>6</td>
<td>Total Losses</td>
<td>.894W</td>
<td>1.599W</td>
<td>.894W</td>
</tr>
<tr>
<td>7</td>
<td>Efficiency</td>
<td>98.54%</td>
<td>97.37%</td>
<td>98.54%</td>
</tr>
</tbody>
</table>

The efficiencies are higher in case of outputting $V_{in}$ than outputting $2V_{in}$. This is because while outputting $V_{in}$ there are only two switches involved in the conversion and while outputting $2V_{in}$ there are four switches involved in the conversion process. Since, switch and switching losses contribute the major share of losses the efficiencies are lower in case of outputting $2V_{in}$ than outputting $V_{in}$.
Figure 5-1: Steady State Output Voltage Waveform While Outputting $2V_{in}$ with Current Load for Topology1

Figure 5-2: Steady State Output Voltage Waveform While Outputting $V_{in}$ with Current Load for Topology1

Figures 5-1 and 5-2 are the output waveforms showing the steady state output waveforms for topology1. The steady state output waveforms shown in the figures
are outputting $2V_{in}$ and $V_{in}$ respectively. There are slight distortions in the steady state output voltage waveform while output is $2V_{in}$ and there are no distortions in the waveform while output is $V_{in}$. These distortions are the voltage ripples and these are caused by to the alternate switching of the switches to charge each capacitor. While one capacitor is being charged, there is a slight drop in voltage across the other capacitor. While output is $V_{in}$, only two switches are operated and the voltage keeps on building up constantly. So, there are no voltage ripples while outputting $V_{in}$.

![Figure 5-3: Output Voltage Transition from $V_{in}$ to $2V_{in}$ with a Current Load for Topology1](image)

Figures 5-3 and 5-4 are the output waveforms for the output voltage transition for the topology1 presented. The figures are the output voltage transition from $V_{in}$ to $2V_{in}$ and from $2V_{in}$ to $V_{in}$ respectively. As the duty cycle is changed for the voltage transition to take place there is a gradual change in the output voltage accordingly i.e. the voltage builds during the transition from $V_{in}$ to $2V_{in}$ and voltage drops during the transition from $2V_{in}$ to $V_{in}$.
Figure 5-4: Output Voltage Transition from $2V_{in}$ to $V_{in}$ with a Current Load for Topology1

Figure 5-5: Transient Current During the Transition of Output Voltage with a Current Load for Topology1

Figure 5-5 shows the transient currents during the transition of the output voltage
from $2V_{in}$ to $V_{in}$. The maximum transient currents are around 800A for a period of time due to the transitions of the output voltage.

![Graph of steady state output voltage waveform](image)

Figure 5-6: Steady State Output Voltage Waveform While Outputting $2V_{in}$ with Current Load for Topology2

Figures 5-6 and 5-7 show the steady state output voltage waveforms for the topology2 for a current load, for output voltages of $2V_{in}$ and $V_{in}$, respectively. The reason for the voltage ripples is same as above explained for the topology1 and the output voltage is less compared to the topology1 because the there are two more switches involved during the conversion process in both the topology2 and topology3.
Figure 5-7: Steady State Output Voltage Waveform While Outputting $V_{in}$ with Current Load for Topology2

Figure 5-8: Output Voltage Transition from $V_{in}$ to $2V_{in}$ with a Current Load for Topology2
Figures 5-8 and 5-9 are the output waveforms for the output voltage transition for the topology 2 with a current load, from $V_{in}$ to $2V_{in}$, and from $2V_{in}$ to $V_{in}$, respectively. The voltage builds up during the transition from $V_{in}$ to $2V_{in}$ and drops during transition from $2V_{in}$ to $V_{in}$. As the duty cycle of switching transitions is changed gradually, the abnormalities in the output voltage are reduced as shown in figures 5-8 and 5-9.
Figure 5-10: Transient Current During the Transition of Output Voltage with a Current Load for Topology2

Figure 5-10 shows the transient currents during the transition of the output voltage from $2V_{in}$ to $V_{in}$ for the topology2. The maximum transient currents are reduced to 150A when compared to the transient currents of the topology1. For the most of the time during the transition the transition current is almost zero. As there are smaller transient currents compared to the topology1 the life expectancy of the converter is increased. The peak in the transition current is due to the sudden switching of switches S5 and S6 to the ON position but quickly reduces to a smaller value.
Figure 5-11: Steady State Output Voltage Waveform While Outputting $2V_{in}$ with Current Load for Topology3

Figure 5-12: Steady State Output Voltage Waveform While Outputting $V_{in}$ with Current Load for Topology3
Figures 5-11 and 5-12 are the waveforms showing the steady state output voltage for the topology3 for a current load. The figures show the output waveform while outputting $2V_{in}$ and $V_{in}$ respectively.

Figure 5-13: Output Voltage Transition from $V_{in}$ to $2V_{in}$ with a Current Load for Topology3

Figure 5-14: Output Voltage Transition from $2V_{in}$ to $V_{in}$ with a Current Load for Topology3
Figures 5-13 and 5-14 are the output voltage waveforms during the transition from $V_{in}$ to $2V_{in}$ and from $2V_{in}$ to $V_{in}$ respectively for the topology3. There is a lot of distortions during the output voltage transition because the input voltage source directly supplies the power to the load during the transition.

Figure 5-15 shows the transient currents during the transition of the output voltage from $2V_{in}$ to $V_{in}$. The maximum transient currents are reduced to 350A when compared to the transient currents of the topology1. As there are less transient currents compared to the topology1, the life expectancy of the converter is expected to be increased. Similar to topology2, the peak currents during the transition is due to switching but quickly reduces to small values.

5.4 Results and Discussion

This chapter presents two new topologies that improve the transition time during switching of voltages in multilevel converters. The losses incurred in the operation
of different multilevel DC-DC converter modules are studied with both resistive and current loads. The comparison of losses in different switching modes were also presented. From the comparisons it can be inferred that the topology1 is better in terms of output voltages and efficiency as there are two more added switches in the other two topologies. Adding two new transistor switches increase the switching losses and reduces the efficiency by about 1-2% but they also decrease the transition losses and transition currents. The new topologies also make it easier to implement cascaded system topology converters.
Chapter 6

Implementation of Cascaded Topology of Multilevel Converter Modules

6.1 Introduction

This section presents the implementation of the cascaded topology of multilevel DC-DC converter modules for two stages.

6.2 Description and Operation

To implement a two-stage cascaded topology of multilevel converter modules 15 transistor switches are used. Power MOS transistors, Infineon IPB12348018, are used in the simulation along with four 10 mf capacitors and two 100 mf capacitors. As the number of stages increase the capacitor ratings have to be increased as they have to drive the converter modules in the next stage. During this operation, the capacitors in the first stage are being charged to the $2V_{in}$ output voltage.

Once the capacitors accumulate the desired charge, they are disconnected from
being charged with the help of two transistor switches and these capacitors are used to charge the capacitors in the next stage.

The switches connecting the stage 1 and stage 2 are OFF as long as the capacitors in the first stage charges and are in ON position once the capacitors in the stage 1 drive the modules in the stage 2. The capacitors in the stage 1 need to be charged more often i.e. the capacitors in the stage 1 are charged four times the frequency the capacitors are charged in the stage 2. Thus, continuing the procedure over a period of time the voltage builds up across the capacitors in the stage 2. Thus, the output of each individual module in the stage 2 can be upto $4V_{in}$. By adding the output voltages of both converter modules in the stage 2 an output of $8V_{in}$ is obtained which is the maximum output possible for a cascaded topology with 2 stages. The circuit diagram of the cascaded implementation of a multilevel DC-DC converter modules for two stages is as shown in the Figure 6-1. However there are certain problems obtaining the maximum output voltage proposed in the previous chapters.

The $4V_{in}$ output for the converter modules in the second level can be obtained. However, there are certain problems in summing up the $4V_{in}$ output voltages obtained at the converter modules in the second stage. The node connecting capacitor C4 and switch S11 is ground with respect to the node connecting capacitor C3 and switch S8. The node connecting capacitor C6 and switch S16 is ground with respect to the node connecting capacitor C5 and switch S13. While trying to connect the nodes at capacitors C4 and C5 there is problem of shorting the ground. Hence, desired $8V_{in}$ output is not obtained. However, the future work would be to modify the circuit so that summing up the output voltages of the converter modules is possible in the second level.

Though the topology2 converter modules are used in all the stages, it is not necessary to use the topology2 converter modules in the final stage as it drives no further stages. This arrangement can reduce the number of transistor switches used
6.3 Discussion

This section of this chapter presents the implementation of cascaded topology of multilevel DC-DC converters in SPICE. The cascaded topology implemented is for a rating of 400W. The battery used in this implementation is 5V. The maximum desired output voltage is 40V. The obtained output voltage of the each converter module in the second stage is 20V. However, the future work would be summing up the output voltages of the converter modules in the second level.
Figure 6-1: Implementation of the Cascaded Topology of Two Levels using Multilevel DC-DC Converter Modules
Chapter 7

Conclusions and Future Work

7.1 Conclusions

This thesis presents theoretical results to compare new multilevel DC-DC converter system topologies to the existing multilevel DC-DC converter system module in terms of number of steps of output voltages, maximum output voltage, and minimum number of operating switches required for a given output voltage. Different models of cascaded topology with odd and even number of converter modules were presented and compared for their advantages and disadvantages. Of these, cascaded topology presents significant advantages compared to other topologies. The future work aims to look into the different losses with the multilevel topology and perform a theoretical framework for the ripple analysis of the output voltage under different types of loading conditions.

In this research, two new converter modules were presented which reduce the transition currents during the output voltage transition. Among the two presented topologies one of them facilitate the implementation of the cascaded topology of multilevel converters more efficiently over the other. As the transition losses are reduced by these converter modules presented, the life of the converter module also potentially increases. Comparison of different losses during the operation of these
converter topologies is also presented.

### 7.2 Future Work

The hardware implementation of the multilevel DC-DC converter system topologies is a potential extension of this work. The converter modules were analyzed and simulated when they were operated in ideal conditions. However, in the actual implementation of these converter modules, losses have to be considered to find the optimum number of converter modules to implement the one-to-many topology and/or cascaded topology. An extension of the proposed models to accommodate larger input voltages can result in multilevel converters suitable for industrial and power applications.
References


Appendix A

Source Code for Generalizations of the Cascaded System Topology

clc;
clear all;
close all;
l=input('enter the level:\n');
v=input('Intial Input voltage:\n');
m=power(2,l)-1;

b=zeros(127,1);
m1=((2^(l+1)-1));
a=zeros(m1,1);
n=(2^n)-1;
um=(2^n)-1;
b=zeros(num+1,1);
swc=zeros(num+1,2);
for f=1:m1
  a(f,1)=v;
end
```matlab
end
    sum=0;
    x=0;
    y=0;
    sc=0;
    s1=(0:num);

    s=de2bi(s1);
    for z=1:(num+1)

        for i=1:m
            x =2*i;
            y =(2*i)+1;

            if(s(z,i)==0)
                a(x,1)=a(i,1)*1;
                a(y,1)=a(i,1)*1;
                sc=sc+2;
            end
            if(s(z,i)==1)
                a(x,1)=a(i,1)*2;
                a(y,1)=a(i,1)*2;
                sc=sc+4;
            end
        end
    p=power(2,l);
    q=power(2,l+1)-1;
end
```
for j=p:q
    sum=sum+a(j,1);
end

tsum=sum/2;
b(z,1)=tsum;
swc(z,1)=tsum;
swc(z,2)=sc;
sum=0;
sc=0;
end
fswc=sort(swc);
g=unique(b,'rows');
c=length(g);
disp('possible outcomes');
disp(g);
disp('count of steps of voltages');
disp(c);
xlswrite('fvoltagesandswitches',fswc);
Appendix B

B.1 Specifications of the Diode used in the model

B.1.1 Features

N–Channel, Normal level

Excellent gate charge $XR_{DS[on]}$ product (FOM)

Extremely low on-resistance $R_{DS[on]}$

175 degrees Celcius operating temperature

Pb-free lead plating; RoHS compliant
Table B.1: The Specifications of the Transistor Switch used to build the Converter Module

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Continuous Drain Current</td>
<td>$T_c=25 \text{ degrees C}$</td>
<td>180</td>
<td>A</td>
</tr>
<tr>
<td>Continuous Drain Current</td>
<td>$T_c=100 \text{ degrees C}$</td>
<td>167</td>
<td>A</td>
</tr>
<tr>
<td>Pulse Drain Current</td>
<td>$T_c=25 \text{ degrees C}$</td>
<td>720</td>
<td>A</td>
</tr>
<tr>
<td>Avalanche Energy, Single Pulse</td>
<td>$I_D=100\text{A}$, $R_{GS}=25\text{ohm C}$</td>
<td>1000</td>
<td>mj</td>
</tr>
<tr>
<td>Gate Source Voltage</td>
<td></td>
<td>+20 or -20</td>
<td>V</td>
</tr>
<tr>
<td>Operating and storage temperature</td>
<td></td>
<td>-55.....175</td>
<td>C</td>
</tr>
</tbody>
</table>