A Thesis

entitled

NiOₓ Based Resistive Random Access Memories

by

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In present flash memory devices, data is stored by injecting hot electrons or charge through tunnel oxide. This will result into degradation of oxide and the problem would amplify with the scaling of the dielectric. According to International Technology Roadmap for Semiconductors (ITRS) the continuous scaling of the oxide thickness beyond 16 nm node technology may result into unwanted data loss and high leakage current. Hence, new ways of data storage are being explored, resistive random access memory (RRAM) being one of them. A RRAM device is a two-terminal metal insulator metal (MIM) structure having the potential to scale up to 8 nm generation technology. It is non-volatile and can store data in form of both low resistance state (LRS) and high resistance state (HRS). The other incentives are its low operating voltage, high endurance and integration in crossbar arrays. NiO$_x$ promises to be a strong candidate for future non-volatile memory devices and it still needs a better understanding of the physical mechanism behind the ability to switch between two resistive states. This thesis is focused to study the impact of different metal electrode on NiO$_x$ based RRAM devices with high percentage (20%) of O$_2$. RRAM device performance with Al and Ru electrodes was studied. Switching characteristics indicated that Al based electrodes lead to the
device failure due to formation Al₂O₃ on NiOₓ. On the other hand, devices with Ru electrodes demonstrated switching with SET/RESET voltages of less than ±2 V. Moreover, the conduction mechanism responsible for switching mechanism is also reported.
To my parents, sisters and best friend Raju.
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Introduction to Memory Technology

Today’s semiconductor memory market can be broadly classified into two main groups: Volatile memories and Nonvolatile memories.

Volatile memories are divided into Dynamic Random Access Memory (DRAM) and Static Random Access Memory (SRAM). DRAM stores data in the presence or absence of charge in the capacitor. The charge stored in the capacitor decays with time and hence, the DRAM needs to be refreshed periodically. However they are dense and have low cost. On the other hand, the SRAM does not need to be refreshed and has higher speed but comes with a low density. Furthermore, the major disadvantage of DRAM and SRAM is their inability to retain data when the power is turned off and this brings nonvolatile memories into the picture [1].

1.1 Overview of Nonvolatile Memories

The nonvolatile memories like Erasable Programmable Read Only Memory (EPROM), Electrically Erasable PROM (EEPROM) or Flash have the capability to retain the data even without power supply. The data retention time is around 100 ms in DRAM
while it is 10 years for a flash memory. The Fig 1-1 indicates market share for different memory technologies (both volatile and non-volatile), “Flash memory” being one of the dominant players.

![Figure 1-1 Current Market for Memory Technology, DRAM and Flash dominates [2].](image)

1.2 Flash Memory

Flash memory is a combination of both EPROM and EEPROM. Flash memory’s ability of erasing a large portion of memory at a given time is what leads to its name. In EEPROM each byte is erased one at a time and hence it is different from flash. A flash memory cell constitutes of a transistor with a floating gate, analogous to an EPROM cell. However, there are some differences in technology and geometry between flash memory cells and EPROMs. In particular, the thinner gate oxide between the silicon and the floating gate and also the source and drain diffusions for flash memory technology [3].
1.2.1 Working Principle of Flash Memory

When a conventional MOSFET’s gate is modified such that temporary storage of charge inside the gate is possible, the new structure becomes a nonvolatile memory. A typical structure of a Flash memory cell is shown in Fig. 1-2 where the top gate is called the “control gate” (CG) and the isolated gate between the oxides is called the “floating gate” (FG). This FG is sandwiched between CG and MOS channel [4] where the \( I_D-V_G \) (Drain Current-Gate Voltage) characteristic changes with the amount of charge stored in the FG as shown in Fig. 1-3 [5]. The change in the \( V_T \) can be denoted by simple electrical analysis given by

\[
V_T = V_{T0} - Q/C_2
\]  

(1)

Where \( V_{T0} \) is the threshold voltage with no charge trapped in the FG, \( Q \) is the charge trapped in FG and \( C_2 \) is the FG/CG capacitance.

Figure 1- 2 Structure and \( I_D-V_G \) characteristic of Flash memory.
1.2.2 Write and Erase Operation

The Flash memory cell’s default logic equivalent is binary state of “1”. It can be SET or programmed to “0” by a phenomenon commonly known as tunneling or hot electron injection. The electrons traveling from source to drain are forced to tunnel through the oxide by applying a high voltage at CG and consequently trapped by the FG. The programming steps are illustrated in Fig.1-3 (a). When a high bias of ~ 10 V is applied to the CG, the electrons in the channel gain high energy and they are injected through tunnel oxide to the FG as illustrated in Fig. 1-3 (a). The Flash memory cell is then said to be SET or programmed to the binary state “0” [5]. The electrons trapped in the FG are tunneled out by applying high a negative bias to CG. In this way, the memory cell can be again RESET back to “1”. The erase mechanism is illustrated in Fig. 1-3 (b) where $V_G$ is gate voltage, $V_S$ is source voltage and $V_D$ is drain voltage.

![Figure 1-3](image_url)  
Figure 1-3 Physical mechanism of (a) write by hot carrier injection and (b) tunneling.
1.2.3 Reliability Issues of Flash Memory

Even after having features like high mass storage, portability, non-volatility and small cell size there are some issues which makes it difficult to go further in future. Hence there is a need for a universal memory device to have features like non-volatility with long retention time, high speed of operation, low power consumption, high chip density, and scalable beyond 16 nm without any data loss. This section deals with the reliability issues which limit the progress of this technology [6].

1.2.3.1 Scalability Issue of the Oxide

Technology node starting from 45 nm and beyond, the flash memory is expected to face serious scaling issues [7]. In principle it is impossible to fabricate oxides with no defects because at given temperature there is an equilibrium amount of point defects. When there is a defect in the tunnel oxide, electrons stored in the FG can leak out through trap assisted tunneling mechanism [8]. The tunnel oxide should be thick enough to avoid electrons tunneling through disconnected defects as shown in Fig. 1-4 a and 1-4 b. A single defect in the oxide is inadequate to provide a leakage path in a thick oxide. Even several defects may not cause tunneling if they are not within reach of one another but oxide thickness less than 8 nm is prone to trap-assisted leakage as depicted by percolation model [8].
Figure 1- 4 Trap-assisted tunneling shown by percolation model. (a) Single defect in a thin tunnel oxide can cause leakage. The red circle represents the typical distance an electron may tunnel. (b) For a thick oxide a single defect is inadequate to cause tunneling. The efficiency of writing/erasing via tunneling or hot carrier injection is degraded by the interface traps generated in the tunnel oxide, so the scaling of dielectric thickness at the same reliability is possible only if the defect density is accordingly reduced. [D. Ielmini et al].

1.2.3.2 High Operational Voltage

A flash memory requires very high voltage for its unique features like able to write, erase and read data (especially write and erase). However, this may lead to unintentional data loss from the cell [9].

1.2.3.3 Endurance of Flash Memory Cell

Another major issue related with flash memory technology is the tunneling mechanism required for programming and erasing data from the flash memory cell. The most significant aspect governing the reliability of flash memory is the quality of tunnel oxide, both in terms of intrinsic properties and defect density [10]. The tunneling of the
hot electrons from the channel to the FG through the tunnel oxide layer leads to damage of the oxide. This in turn reduces the number of write/erase cycle of the memory cell.

1.2.3.4 Access Time Limitation

One important short-coming of the flash memory is that, even though it can read and program each byte individually in a random access manner, it can only erase one block at a time. This usually sets all bits in the block to logic “1”. To erase a block of memory it takes on the order of 1–2 ms per block, and programming an erased flash needs around 200–300 µs [11]. Additionally, flash memory (specifically NOR flash) can only provide random-access read and programming operations, but not random rewrite or erase operations [12]. In Fig. 1-5 it shows the time required to program decreases with number of times write cycles while the erase time increases with number of cycles of erase operations.

![Figure 1-5 Latency in write and erase cycles after several iterations of tunneling through the oxide.](image)

Hence, tremendous amount of research is going on in search of a universal memory, which merges the high-speed performance of existing DRAM with the non-
volatility of Flash. The memory must be able to overcome the issues which present memory technology is facing (scalability, endurance, high operating voltage) to become the next alternative memory [13]. One of the emerging memories which have the potential to replace FLASH is Resistive Random Access Memory (RRAM). The table below from ITRS shows the comparison of Flash with projected potential of a fully scaled RRAM. According to the data projected for RRAM, it has the ability to scale beyond 10 nm technology node and has extremely high write/erase speed unlike flash memory with many more incentives like high endurance, low operating voltage are few to mention.

Table 1. 1 Comparison of performance parameters for fully scaled RRAM with flash.

<table>
<thead>
<tr>
<th></th>
<th>NAND FLASH</th>
<th>RRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum F-Scaling</td>
<td>16 nm</td>
<td>5-10 nm</td>
</tr>
<tr>
<td>Multi-level</td>
<td>3-bits/cell</td>
<td>Yes</td>
</tr>
<tr>
<td>Write/Erase Voltage</td>
<td>18-20 V</td>
<td>&lt; 0.5 V</td>
</tr>
<tr>
<td>Read Voltage</td>
<td>0.1-0.5 V</td>
<td>&lt; 0.2 V</td>
</tr>
<tr>
<td>Write/Erase Time</td>
<td>&gt; 10 µs</td>
<td>&lt; 5 ns</td>
</tr>
<tr>
<td>Read Speed</td>
<td>15-50 ms</td>
<td>&lt; 10 ns</td>
</tr>
<tr>
<td>Retention Time</td>
<td>10 years</td>
<td>10 years</td>
</tr>
<tr>
<td>Endurance Cycles</td>
<td>$10^4$-$10^5$</td>
<td>$10^{16}$</td>
</tr>
</tbody>
</table>
Chapter 2

Research Motivation

The universal nonvolatile memory must exhibit features like high density, low cost, high performance, low power, greater endurance and retention [14]. The contemporary Si-based flash memories are among the most popular nonvolatile memories because of their high density and low cost of fabrication. However, it suffers from serious reliability issues like future scaling, i.e. the continuous escalation in the density is anticipated to run into physical limitations (beyond 16 nm node). In addition, it suffers from low endurance, low write/erase speed and high operating voltages. To overcome these challenges numerous alternative memory technologies are being explored. “Resistive Random Access Memory” (RRAM) has sought most attention out of many emerging memory devices. The ITRS has projected that it has potential to scale up to 8 nm, has higher speed for read/write operations (~5 ns), and higher number of write cycles ($>10^{16}$). In this thesis, two of the major problems encountered in flash memory and its solution by RRAM to overcome these problems have been brought into focus.

- High Operational Voltage.
- Scaling Limitation.
Furthermore, switching characteristics at very low voltages (~±1.5 V) are reported with higher percentage of O\(_2\) in NiO\(_x\). Higher percentage of O\(_2\) would make NiO\(_x\) less leaky and would allow for further scaling of the dielectric. Also, the switching behavior, mechanisms of failure, and conduction mechanism in NiO\(_x\) based RRAM devices are discussed.

### 2.1 Resistive Random Access Memory

A RRAM is a 2-terminal metal-insulator-metal capacitor with the ability to store data in the form of resistance across the insulator layer. The insulator layer is composed of transition metal oxides (TMO) sandwiched between two metal (possibly different and inert) electrodes. RRAM can be categorized on the basis of switching mechanisms responsible to alter the resistance of the insulator layer from a low resistance state (LRS) to a high resistance state (HRS) and vice-versa. Primarily, the physical mechanism can be broadly divided into “thermal, electrical or ion-migration-based” switching mechanisms. The ion-migration based mechanisms are related to redox processes which cause the change in the resistance of the insulator layer. The ion-migration can be further subdivided into cation migration and anion migration induced switching. In TMO, generally oxygen vacancies (Vo\(^{2+}\)) are more mobile than cations and hence, most ion-migrated based switching is induced by anion migration. Ionic-migration based switching is mostly results in bipolar switching [15]. Various TMOs have been investigated for resistive switching capability [16]-[21]. Of the several TMOs studied so far, NiO\(_x\) promises to be a strong candidate for future. NiO\(_x\) based RRAMs show switching due to presence of Ni vacancies (V\(_{\text{Ni}}^{2+}\)) or O\(^{2-}\) anions. [22]. The p-type doping in NiO\(_x\) has been widely
explained due to the presence of Ni vacancies, as governed by the following relation [23] [24].

\[ 2Ni + 2O_2 \rightarrow 2NiO + 2V_{\text{Ni}}^{2-} \]  

(2)

Fig. 2-1 shows the formation of conducting filament across the NiO\(_x\) insulator layer due to migration of V\(_{\text{Ni}}^{2-}\), on application of positive bias to the Pt (TE) [H. D. Lee and Y. Nishi]. The switching to the LRS state is typically reported as a limited, filamentary effect instead of uniformly dispersed across the entire NiO\(_x\) layer. This leads to the resistance of the device at LRS independent of the area of the device.

On the other hand, the thermal effect shows a unipolar characteristic. An initial voltage-induced breakdown of the insulator layer is done (electroforming), to generate a conductive filament across the layer, where the material in the filament is modified due to joule heating [15]. The material of the filament can either be metals diffused from the electrodes or decomposed insulator material like sub-oxides [25]. The filament is ruptured thermally due to high power density hence switching the device back to HRS. It has also been reported that by increasing the compliance current a bipolar switching mechanism can be converted into unipolar mechanism [26].
Although numerous studies have been reported for switching on NiO$_x$ based RRAM, its repeatability, durability, and mechanisms of failure still needs to be understood. From previous studies it has been demonstrated that high percentage of O$_2$ (in Ar/O$_2$ gas mixture) in NiO$_x$ layer would lead to a monostable switching and hence a low O$_2$ percentage is required for bistable switching [27], [28] as shown in Fig. 2-2. According to their studies the current at LRS is from the “electrons mediated by the empty states of metallic Ni$^{2+}$ defects”. More V$_{\text{Ni}^{2-}}$ leads to reduction in metallic Ni$^{2+}$ defects which in turn reduces the number of trapping sites and hence makes the ON state unstable. In other words, the empty states are filled by more number of V$_{\text{Ni}^{2-}}$ and hence do not contribute to conduction.

Figure 2-2 (a) Bistable switching with 3% O$_2$ and (b) Monostable switching with high (~20%) O$_2$. 


Chapter 3

Fabrication Process of RRAM

The first half of this chapter deals with a detailed process flow adopted for the method of fabrication of the NiO$_x$ based RRAMs. The second half of the chapter will deal with the typical measurement techniques and characterization process of the devices. In general, a sample (MIM capacitor) will constitute of more than 100 devices. The table below demonstrates the number of experiments runs and samples fabricated. Out of all the samples fabricated, only two samples showed resistive switching, namely Ni/NiO/Al 1 and Ru/NiO/Ru/W 2.

Table 3 1 List of samples and fabrication parameters.

<table>
<thead>
<tr>
<th>SAMPLE ID</th>
<th>TE</th>
<th>BE</th>
<th>O$_2$/Ar (sccm)</th>
<th>$T_{ox}$ (Å)</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>W/NiO/W 1</td>
<td>W</td>
<td>W</td>
<td>2.4:9.6</td>
<td>9252</td>
<td>No switching due to too thick of dielectric to electroform the NiOx.</td>
</tr>
<tr>
<td>W/NiO/W 2</td>
<td>W</td>
<td>W</td>
<td>2.4:9.6</td>
<td>250</td>
<td>Dielectric too leaky, current not scaling with area.</td>
</tr>
<tr>
<td>Composition</td>
<td>BE</td>
<td>TE</td>
<td>T</td>
<td>1200°C</td>
<td>Result</td>
</tr>
<tr>
<td>--------------</td>
<td>-----</td>
<td>----</td>
<td>---</td>
<td>--------</td>
<td>------------------------------------------------------------------------</td>
</tr>
<tr>
<td>Ni/NiO/Al 1</td>
<td>Al</td>
<td>Ni</td>
<td>2.4:9.6</td>
<td>Showed resistive switching. Failed after few switching cycles due to oxidation of Al.</td>
<td></td>
</tr>
<tr>
<td>Ru/NiO/Ru 1</td>
<td>Ru</td>
<td>Ru</td>
<td>2.4:9.6</td>
<td>Failed in fabrication due to problem in Ru etching.</td>
<td></td>
</tr>
<tr>
<td>Ru/NiO/Ru/W 2</td>
<td>Ru</td>
<td>Ru</td>
<td>2.4:9.6</td>
<td>Showed resistive switching, W helped in adhesion of Ru to photoresist.</td>
<td></td>
</tr>
<tr>
<td>Ru/NiO/Ru/W 3</td>
<td>Ru</td>
<td>Ru</td>
<td>1.2:10.8</td>
<td>Showed volatile memory switching, due to oxidation of W. Here, photoresist was removed before etching Ru.</td>
<td></td>
</tr>
<tr>
<td>Ni/G/NiO/Ru</td>
<td>Ru</td>
<td>G</td>
<td>2.4:9.6</td>
<td>Testing showed that metal was not etched uniformly throughout the sample causing short circuit.</td>
<td></td>
</tr>
</tbody>
</table>


### 3.1 Process Flow in Details

**Step 1: Wafer Labeling**

First a p-type Si substrate was taken and the name of the sample was scribed at the back (non-shining part). Generally, the naming was done as metal (BE)/metal oxide/metal (TE) followed by a number to represent the sample number.

**Step 2: Cleaning and Surface Treatment**

The wafer was cleaned by dipping it in 2% of HF (Hydrofluoric) acid for 10s then followed by 2 minutes de-ionized (DI) water rinse.

**Step 3: Deposition of BE**
The deposition of BE depends on the type of metal chosen. The experiments performed dealt with different types of metals. The deposition parameters for BE are shown in Table 3.1:

Table 3.2 Deposition parameters for BE.

<table>
<thead>
<tr>
<th>Sample ID</th>
<th>BE</th>
<th>Tox (nm)</th>
<th>Deposition Method/Temp</th>
<th>Adhesion layer</th>
</tr>
</thead>
<tbody>
<tr>
<td>W/NiO/W 1</td>
<td>W</td>
<td>100</td>
<td>Sputtering/RT</td>
<td>NA</td>
</tr>
<tr>
<td>W/NiO/W 2</td>
<td>W</td>
<td>100</td>
<td>Sputtering/RT</td>
<td>NA</td>
</tr>
<tr>
<td>Ni/NiO/Al 1</td>
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<td>100</td>
<td>Sputtering/RT</td>
<td>NA</td>
</tr>
<tr>
<td>Ru/NiO/Ru 1</td>
<td>Ru</td>
<td>100</td>
<td>Sputtering/RT</td>
<td>Titanium</td>
</tr>
<tr>
<td>Ru/NiO/Ru/W 2</td>
<td>Ru</td>
<td>100</td>
<td>Sputtering/RT</td>
<td>Titanium</td>
</tr>
<tr>
<td>Ru/NiO/Ru/W 3</td>
<td>Ru</td>
<td>100</td>
<td>Sputtering/RT</td>
<td>Titanium</td>
</tr>
<tr>
<td>Ni/G/NiO/Ru/W</td>
<td>G</td>
<td>Unknown</td>
<td>*MOCVD/ ~900°C</td>
<td>G deposited on Ni</td>
</tr>
</tbody>
</table>

*MOCVD: Metal Organic Chemical Vapor Deposition. The entire fabrication process of Graphen is discussed in Appendix D.

Step 4: Deposition of NiO$_x$

A shadow mask was put on top of BE before depositing the oxide layer. It partially covered the BE and hence helped in probing. NiO$_x$ was deposited by reactive RF magnetron sputtering on Ni in an O$_2$ environment. A mixture of O$_2$ and Ar gas was flown at 5 mTorr working pressure. The deposition rate for NiO$_x$ at a power of 200 W and a temperature of 300 °C, was found to be 77 A/min.
Figure 3-1 Sputtering tool at University of Toledo clean room for thin film depositions.

**Step 5: Deposition of TE**

TE was deposited using sputtering metal, generally at room temperature. The thickness to be sputtered varied from experiment to experiment.

<table>
<thead>
<tr>
<th>Sample ID</th>
<th>TE</th>
<th>Tox (nm)</th>
<th>Hardmasks</th>
</tr>
</thead>
<tbody>
<tr>
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<td>100</td>
<td>NA</td>
</tr>
<tr>
<td>W/NiO/W 2</td>
<td>W</td>
<td>100</td>
<td>NA</td>
</tr>
<tr>
<td>Ni/NiO/Al 1</td>
<td>Al</td>
<td>100</td>
<td>NA</td>
</tr>
<tr>
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<td>Ru</td>
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<td>10</td>
<td>W</td>
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<td>Ru/NiO/Ru/W 3</td>
<td>Ru</td>
<td>10</td>
<td>W</td>
</tr>
<tr>
<td>Ni/G/NiO/Ru/W</td>
<td>Ru</td>
<td>10</td>
<td>W</td>
</tr>
</tbody>
</table>
Step 6: Prebake

The sample was then heated on a hot plate for 5 minutes at 115 °C. Then it was left to cool down for 5 minutes before proceeding to the next step. This step ensured that there was no moisture left on the sample before it was ready to be spin coated.

Step 7: Spin coating Photoresist

The sample was placed on the chuck of a spinner and a chemical (primer) was put on it. The primer was spread at the speed of 300 rpm for 5 s and then spun for 30 s at a spin speed of 3000 rpm. Thereafter, photoresist was applied. The photoresist was first spread at 500 rpm for 10 s and then the spin speed was increased to 4000 rpm for 60 s. Both primer and photoresist were first spread slowly such that they uniformly cover the entire wafer.

Step 8: Soft Bake

After the sample was spin-coated, it was heated for 1 minute on the hot plate at 115 °C and was allowed to cool for 5 minutes.

Figure 3-2 Mask Aligner used for photolithography in University of Toledo clean room.
Step 9: Photolithography to Pattern Electrodes

The sample was placed on the mask aligner with a mask on it and then it was exposed to UV rays for 15 s. The intensity of the exposed UV ray was 20 mW/cm². The part of photoresist which was exposed to UV rays changes its composition, such that it becomes soluble in the developer.

Step 10: Develop Photoresist

The sample was then dipped into the developer. The developer removed all the soluble photoresist leaving behind the unexposed photoresist as it was. Thereafter, the device pattern was well defined.

The patterning of electrode can be classified into two:

(a) Lift off Technique

The lift off technique was used when the TE was deposited after completing Steps 6 through 9. After that, Step 5 was conducted, followed by Step 10.

(b) Etching Technique

The etching technique was used after all the Steps from 5 through 10 were completed. After etching was successfully completed, the remaining photoresist (on the TE) was removed by dipping the sample into the PG remover.
Chapter 4

Device Characterizations and Switching of Ni/NiO$_x$/Al RRAMs

In this chapter the device characterization of Ni/NiO$_x$/Al samples are discussed. The first half deals with the measurement techniques to characterize Ni/NiO/Al samples. The second half deals with results and discussion of the data obtained from measurement. All the I-V characteristics of the virgin devices, switching mechanism of the devices, failure mechanisms are discussed in detail. Various parameters including the content of O$_2$ in NiO$_x$ films, applied voltage bias, frequency of the applied bias, work function of the metal electrodes, and free energy for oxidation of the electrodes were analysed for understanding the possible reasons of failure and unpredictability. C-V curve analyses were performed to gain a better understanding of the physics behind this mechanism.
4.1 Overview

The samples were probed in a Lakeshore cryogenic probe station and all of the electrical measurements were obtained by using a Keithley 4200 semiconductor characterization system as shown in Fig. 4-1 (a). The voltage bias was applied on the TE electrode while the BE electrode was grounded in all our measurements as shown in Fig. 4-1 (b). The initial J-V curves in positive and negative bias indicated symmetric behavior in spite of a significant difference in the vacuum work functions of Al and Ni. The Capacitance-Voltage (C-V) characterizations indicated NiO$_x$ to be a p-type semiconductor with acceptor doping density between $6 \times 10^{18}$ cm$^{-3}$ ~ $5 \times 10^{20}$ cm$^{-3}$. Switching behavior was observed after electroforming the devices. The devices failed after multiple switching cycles by switching into a relatively low conductive state. The mechanism of failure was attributed to the formation of Al$_2$O$_3$ due to a slow oxidation of Al electrodes with repeated cycles.

![Figure 4-1](image_url)

Figure 4-1 (a) Probe Station at UT Nano-laboratory for device characterization, (b) Stack of Al (TE)/NiO$_x$/ Ni (BE) RRAM.
4.2 Analysis of Ni/NiOx/Al RRAM

In this section the switching behaviour and mechanisms of failure in NiO\textsubscript{x} based RRAM devices are discussed. In the analysis, various parameters including the content of O\textsubscript{2} in NiO\textsubscript{x} films, applied voltage bias, frequency of the applied bias, work function of the metal electrodes, and free energy for oxidation of the electrodes were analysed for understanding the possible reasons of failure and unpredictability. C-V curve analyses were performed to gain a better understanding of the interface between the TE and NiO\textsubscript{x} layer.

The current density-voltage (J-V) curves of as-fabricated virgin devices of 100 \(\mu\text{m} \times 100 \mu\text{m}\) and 200 \(\mu\text{m} \times 200 \mu\text{m}\) are shown in Fig. 4-2. The J showed an excellent scaling with the area of the devices and was repeatable across the wafer. In spite of a considerable difference in the vacuum work functions of Al and Ni, the J-V characteristics showed symmetric behavior. The barrier heights were extracted from I-V curves of the virgin devices by J-V extrapolation method and were found to be approximately 0.65 eV for all devices. This implied that voltage bias was needed to change the interface contacts from Schottky to Ohmic, such that most of the voltage drop would be across the dielectric and not at the interface. Also, the conductivity of the devices was found to be low from these curves.
Figure 4-2 Current density vs. voltage characteristics of virgin devices of 200 µm and 100 µm devices. The inset shows the forming current density vs. voltage characteristic. Both the device sizes, i.e. 200 µm and 100 µm need a high voltage of 20 V to form.

To gain a better understanding of the Al/NiO\textsubscript{x} interface, C-V measurements were carried out on virgin devices. Fig. 4-3 shows C-V sweeps between -10 V to 10 V on various devices across the wafer. All C-Vs were performed at an a.c. frequency of 1MHz at room temperature. A typical n/p junction characteristic can be observed where Al serves as n-type electrode and NiO\textsubscript{x} serves the p-type semiconductor. In positive bias sweep (0 to ~6.7 V) when the diode is reverse biased, decrease in the capacitance can be observed due to an increase in the depletion width in NiO\textsubscript{x}. At around 6.8 V, a slight increase in the capacitance can be observed which could be due to the generation of electrons in depleted NiO\textsubscript{x} through thermal excitation.
Figure 4- 3 The capacitance per unit area (F/cm$^2$) versus voltage (V) curve shows a p-type C-V profile for a voltage range of -10 V to 10 V at 1 MHz for all the device sizes.

Fig. 4- 4 shows $1/C^2$ vs. V plot in depletion. Four distinct regions can be clearly defined based on the slope of the curve. The region-1 corresponds to 0 to ~1.3 V with a positive slope of $5 \times 10^{18}$ F$^{-2}$ V$^{-1}$, region-2 corresponds to 1.4 to 2.3 V with positive slope of $8 \times 10^{18}$ F$^{-2}$ V$^{-1}$, and region-3 corresponds to 2.4 V~6.0 V with a positive slope of $4 \times 10^{18}$ F$^{-2}$ V$^{-1}$. The slope becomes negative in region-4 indicating a change in the type of carriers which was attributed to the generation of thermal electrons in the depletion region of NiO$_x$. 
Figure 4- 4 Shows $1/C^2 (F^2)$ vs. voltage (V) plot in depletion.

Fig. 4- 5 shows doping density vs. voltage plot that was extracted from these $1/C^2$-V plots using a dielectric constant of 10 for NiO$_x$ [29]. A relatively low dielectric constant was used due to a high O$_2$ content in our films that was expected from the deposition condition [30]. An acceptor doping density between $6 \times 10^{18}$ cm$^{-3}$ to $5 \times 10^{20}$ cm$^{-3}$ was observed. At voltages lower than 0 V (i.e. negative bias) the capacitance value starts to increase. This increase can be attributed to the reduction in the depletion width due to a gradual accumulation of holes at Al/NiO$_x$ interface. The C-V characteristics clearly indicated the p-type doping in NiO$_x$. 
Figure 4-5 shows doping density vs. voltage plot that was extracted from these $1/C^2$-V plots using a dielectric constant of 10 for NiO$_x$.

After the devices were formed, testing was done by applying voltage sweeps from 0 V up to ±5 V. Fig. 4-6 illustrates the switching of a 200 µm device where the numbers indicate the sequence of switching and arrows indicate the direction of bias applied. The device started to switch with a SET voltage in the -3 V to -3.5 V range and a RESET voltage of 3 V. $R_{on}/R_{off}$ ratio of order 10 was achievable. However the device then experienced a sudden drop in conductance. The device then remained in low conductance state even after applying higher bias of 4.5 V and -5 V.
Figure 4-6 Shows the switching pattern of a 200 µm device after forming. A SET voltage -3 V and RESET voltage of 3 V was achieved.

To investigate the cause of failure, C-V measurement was conducted on the failed devices and it was found that the capacitance of the failed device was less than the capacitance of virgin device as shown in Fig. 4-7. This reduction in the capacitance was attributed to the formation of a thin layer of Al₂O₃ at NiOₓ/Al₂O₃ interface. Assuming a continuous layer of Al₂O₃, the capacitance of the failed device can be modeled using Eq.’s (3) and (4).

\[
\frac{1}{C_{\text{failed}}} = \frac{1}{C_{\text{NiO}}} + \frac{1}{C_{\text{Al}_2\text{O}_3}} \quad (3)
\]

\[
C_{\text{Al}_2\text{O}_3} = \xi A/\varepsilon_{\text{ex}} \quad (4)
\]
where \( C_{\text{failed}} \) = capacitance of the failed device in low conductive state, \( C_{\text{NiO}} \) = capacitance of the virgin device, \( C_{\text{Al}_2\text{O}_3} \) = capacitance of the \( \text{Al}_2\text{O}_3 \) layer formed, \( \xi_o \) = dielectric constant of \( \text{Al}_2\text{O}_3 \sim 10 \) [31], \( \xi_r = 8.854 \times 10^{-14} \text{ F/cm}^2 \), \( A \) = area of \( \text{Al}_2\text{O}_3 \) layer (200 \( \mu \text{m} \) x 200 \( \mu \text{m} \)), \( t_{ox} \) = thickness of \( \text{Al}_2\text{O}_3 \) layer. Using these equations, the thickness of \( \text{Al}_2\text{O}_3 \) was calculated to be 38.2 nm. However, we believe that this layer could be discontinuous and may appear only at the certain regions of the interface.

![Graph showing capacitance density versus voltage](image)

Figure 4-7 A reduction in the capacitance density can be observed in failed device as compared to the virgin device.

This phenomenon was explained by formation of \( \text{Al}_2\text{O}_3 \) layer due to oxidation of the TE (Al). When a negative bias is applied, the holes are pushed back and the thermally generated electrons are trapped in \( V_o^{2+} \). When a positive bias is applied to Al (TE), the holes are accumulating near Al/NiO\(_x\) interface hence lowering the depletion width, which
sets the device however due to low free energy formation of oxide of Al [32], Al₂O₃ is getting formed and that leads to failure of the device as illustrated in Fig. 4-8 (a) and (b) respectively.

![Diagram](image)

Figure 4- 8 Illustrates the switching mechanism of a Al/NiOₓ/Ni. Thermally generated electrons are trapped by the Vo²⁺. (b) Illustrates the failure mechanism of the Al/NiOₓ/Ni structure due to formation of Al₂O₃ layer.
Chapter 5

Device Characterizations and Switching of Ru/NiOx/Ru/W RRAMs

5.1 Ru/NiOx/Ru Based RRAMs

In this chapter the results obtained from the characterization of the successfully fabricated Ru/NiOx/Ru/W devices are discussed. The first half deals with motivation of fabricating this sample and challenges faced during its fabrication. The second half deals with results and discussion after the characterization of Ru/NiOx/Ru/W devices. All the I-V characteristics of the virgin devices, switching mechanism of the devices, are discussed in detail.

5.1.1 Motivation

Failure of Ni/NiOx/Al RRAM motivated for trying another metal electrode on NiOx. The reasons and analysis of failure will be discussed in details in the next section. Fundamentally, Al which has low free energy of oxidation tends to get oxidized and hence results in failure of the device. In this experiment bipolar switching and
hence results in failure of the device. In Ru/NiOx/Ru/W sample bipolar and bistable characteristics with high percentage (20%) of O$_2$ in NiO$_x$ were studied. Switching characteristics indicated higher number of SET/RESET cycles without failing unlike Ni/NiO$_x$/Al sample. Furthermore, the SET or RESET voltages less than ±2 V were achieved. Higher percentage of O$_2$ in NiO$_x$ would make NiO$_x$ less leaky and would allow further scaling of the dielectric.

5.1.2 Fabrication Challenges

Ru deposited as TE of 200 µm x 200 µm area was patterned using etching. W was used as a hard mask on top of Ru (TE), which eased the etching of Ru. The samples were probed in a Lakeshore cryogenic probe station and all of the electrical measurements were obtained by using a Keithley 4200 semiconductor characterization system. All the electrical measurements were done by applying positive bias to the TE as shown in Fig. 5-1.

![Figure 5-1 Stack of Ru (TE)/ NiO$_x$/ Ru (BE) with W used as hard mask.](image)

31
Etching of Ru was not successful for the first few devices fabricated. The etchant for Ru was ceric ammonium nitric acid which would also slowly etch Ni. Moreover, Ru has known to have adhesion issues. Hence, an extra layer of (W) was added on top of Ru, such that the photoresist sticks well to the stack. After depositing all the layers, the stack was ready for the photolithography and then eventually W and Ru were etched. This lead to successful fabrication of devices using Ru electrodes. However, ceric ammonium nitric acid can also slowly oxidize the photoresist and hence for some of the devices PG remover could not do an excellent job of removing photoresist from the TEs.

5.2 Analysis of Ru/NiOx/Ru/W RRAMs

The dielectric (NiOₙ) can be scaled further only if dielectric is less conductive, which can be done by increasing the O₂ content in NiOₙ as it reduces the amount of metallic Ni. Consequently, the roles of metal electrodes on NiOₙ based RRAM becomes more important as they would decide the switching at low voltages, repeatability, high $R_{on}/R_{off}$ ratios. In this section, repeatable switching for Ru (TE)/NiOₓ/Ru (BE) structure at a voltage ~ (±1.0 V to ±1.5 V) with high percentage of O₂ (20% of O₂/Ar mixture) was observed.

The initial I-V curves of the virgin devices were repeatable as shown in Fig. 5-2. The barrier heights were extracted from the I-V curves and found out to be 0.5 eV for Ru/NiOₓ/Ru. This implied that voltage bias was needed to change the interface contacts from Schottky to Ohmic, such that most of the voltage drop would be across the dielectric
and not at the interface. This indicated that the work function of the metal does not dominate the choice of the TE but the free energy of oxidation of metal does.

Figure 5-2 Initial I-V curves for Ru/NiO$_x$/Ru of 200 µm x 200 µm area.

Figure 5-3 Repetitive switching cycles for Ru/NiO$_x$/Ru of 200 µm x 200 µm and inset shows the forming of device.
However, the BE seems to be more conductive than the TE. The potential reason behind it could be trapping of some of the O\(^{2-}\) atoms from NiO\(_x\) by Ru (BE) electrode while depositing NiO\(_x\) layer at 300 °C to form a very thin layer of RuO\(_2\). Moreover, RuO\(_2\) is considered to be a conducting MO\(_x\) by ITRS [33]. The devices were electroformed by applying a positive bias on TE with a compliance limit SET at 5 mA. After the device hits compliance, 5 mA current started to flow across the device even at low voltage (~1.5 V) as shown in the inset of Fig. 5-3. Repetitive switching cycles (~20 cycles) were observed in the region of ±1.5 V for Ru/NiO\(_x\)/Ru even with high percentage of O\(_2\) flown in NiO\(_x\) layer, as evident from Fig. 5-3 where the numbers indicate the sequence of switching and the arrows indicate the direction.

![Diagram of switching mechanism](image)

**Figure 5-4** Switching mechanism using filament based model of NiO\(_x\) based RRAM for [(a) and (b)] Ru/NiO\(_x\)/Ru structure and (c) Pt/NiO\(_x\)/Pt structure. Positive bias applied to TE of [(a) and (c)].

Fig. 5-4 illustrates the switching mechanism of Ru/NiO\(_x\)/Ru structure with high O\(^{2-}\) content. In Fig. 5-4 (a) when a positive bias was applied to the TE, the extra O\(^{2-}\) atoms or the V\(_{Ni}^{2-}\) got attracted towards the TE creating oxygen vacancies (Vo\(^{2+}\)). However, the O\(^{2-}\) atoms which were trapped by the BE could not be moved. This created
a smaller size cone shaped conducting filament giving a distinct state of conductance LRS. The device was switched back to HRS by applying a negative bias which pushed the O$^{2-}$ atoms back and hence ruptured the filament as shown in Fig. 5-4 (b). Since, free energy of oxide formation for RuO$_2$ is more negative than free energy of oxide formation for PtO, so oxide formation for Ru will be more favorable than oxide formation of Pt [37], [38]. Hence less/no O$^{2-}$ atoms would be trapped to the BE (at 300 °C) for Pt/NiO$_x$/Pt structure as illustrated in Fig. 5-4 (c). Either there will be no place to move the O$^{2-}$ atoms to create V$_{o^{2+}}$ or there can be a slight movement but it cannot be distinguished between two different states of conductance. Moreover, the TE of Pt will attract less O$^{2-}$ atoms compared to Ru as TE, which will add on to a lesser amount of movement of O$^{2-}$ atoms in Pt/NiO$_x$/Pt. Consequently, giving rise to a monostable type of switching. Hence, NiO$_x$ with high percentage of O$^{2-}$ cannot give a bistable switching with Pt as its BE where as Ru/NiO$_x$/Ru can.

The compliance limit of the current played a vital role in the formation of filament area in Ru/NiO$_x$/Ru structure. To prove this, switching tests were performed on 500 µm x 500 µm device areas by electroforming the devices using different compliance levels. The initial I-Vs showed excellent scaling with area for 200 µm x 200 µm and 500 µm x 500 µm as shown in Fig. 5-5 (a). As the initial current for larger area devices has higher current, the compliance limit for electroforming was raised from 5 mA. The compliance limit was first SET to 30 mA for electroforming. Then the conductance of the device was increased; however, it could not be RESET back due to formation of large area filament. The same case was observed with a compliance limit of 20 mA. Finally, a compliance
level of 10 mA showed repeatable switching as it was observed for 200 µm x 200 µm area size devices as evident from Fig. 5-5 (b)

![Graph](image)

Figure 5- 5 For Ru/NiOₓ/Ru of 500 µm x 500 µm area (a) Initial I-V curves and (b) switching with 30 mA, 20 mA and 10 mA compliance level. The device with 10 mA compliance while electroforming showed repeatable switching

. Also, the Ru/NiOₓ/Ru structure also showed a stable \( R_{on}/R_{off} \) ratio as evident from Fig. 5-6. For Pt/NiOₓ/Pt, a sacrificial layer of Ni on top of Pt (BE) can reduce the size of the conducting filament as shown in Fig. 5-7 and consequently reduce the RESET
current. However, in our case (Ru/NiOx/Ru), the size of the filament is reduced by the BE itself and can be controlled by changing the compliance limit. In the illustration it shows that in Fig. 5-7 (a) larger filament is formed as compared to the Fig. 5-7 (b) Pt/NiOx/Pt with the Ni interfacial layer. However, in Fig. 5-7 (a) very large filament is formed due to low free energy of oxidation of (Al, Ta and Ni) TE.

Figure 5-6 A stable $R_{\text{on}}/R_{\text{off}}$ ratio of Ru/NiOx/Ru stack.
Figure 5-7 Conducting filament model for Pt/ NiO\textsubscript{x}/Pt structure (a) with Al as interfacial layer resulting in high RESET current. (b) Ni as interfacial layer to reduce the RESET current [39].

However, in case of (Ru/NiO\textsubscript{x}/Ru), the size of the filament is reduced by the BE itself and can be controlled by changing the forming current. Moreover, the SET current was dependent on area of the device whereas the RESET current was independent as shown in Fig. 5-8 (a) and 5-8 (b). The SET current for our devices were higher as compared to the SET current for devices reported in literature due to their smaller area devices. The RESET current was observed to depend on the area of the filament formed and which in turn was dependent on the current at which the device was formed as evident from Fig. 5-8 (c).
Figure 5- 8 (a) HRS current density for 200 µm x 200 µm and 500 µm x 500 µm device for Ru/NiO/Ru.

Figure 5- 8 (b) LRS current density for 200 µm x 200 µm and 500 µm x 500 µm device for Ru/NiO/Ru.
Figure 5-8 (c) Filament area \( (A_{LRS}) \) increases with increase in forming current. \( R_0 \) and \( A_0 \) are the resistance and area of 100 µm x 100 µm device at 5 mA forming current respectively.

The resistive state of the device in the LRS was modeled by the resistance \( (R) \) of the conductive filament in the LRS using the Eq. (5). This model assumes that only one filament is responsible for switching the device from the HRS to the LRS and the filament extends from the BE to the TE.

\[
R = \frac{\rho l}{A} \quad (5)
\]

where \( \rho \) is the resistivity, \( l \) is the thickness of the dielectric and \( A \) is the area of the filament. If \( R_o \) and \( A_o \) are considered as the resistance and area of the filament in a 100 µm x 100 µm device area with a 5 mA forming current, then the other LRS of the device \( (R_{LRS}) \) obtained with different forming currents can be correlated with the corresponding filament area \( (A_{LRS}) \) using Eq. (6).
\[ \frac{R_0}{R_{LRS}} = \frac{A_{LRS}}{A_0} \]  

Using this relation, the \( A_{LRS}/A_0 \) ratio is plotted in Fig. 5-8 (c). It is evident from Fig. 5-8 (c) that the area of the filament increased with increasing forming current, decreasing its resistance (\( R_{LRS} \)). Furthermore, \( A_{LRS} \) is independent of the size of the device and depends primarily on the forming current through the device. In light of these observations, it is possible to achieve a better LRS/HRS ratio in deep submicron devices where the LRS current will be governed by the dimension and morphology of the filament while HRS current can be significantly scaled down due to the reduced dimensions of the device.
Chapter 6

Mechanism of Conduction in NiOx RRAMs

6.1 Background

In this section, the conduction mechanism at different resistive states has been reported, most importantly at LRS and HRS. As from previous chapters it has been shown that conduction of NiO is filamentary in nature and hence it becomes extremely critical to have full control over its formation and dissolution. One of the major hurdles for scalability of RRAM devices is the “high RESET current”. In order to reduce the RESET current, the size of the filament formed at LRS is being reduced. However, reduction in the size of the filament at LRS decreases the stability of the filament [40]. To address all such problems it has become very vital to know the mechanism of conduction in NiOx RRAMs especially through filament (LRS). The mechanism of charge conduction in NiOx based RRAM is highly debatable and widely in research. According to present studies it has been shown that NiOx with bipolar switching (Pt as TE and SrRuO3 as BE) at LRS tends to fit “ohmic” conduction mechanism. Ohmic contacts were observed between Pt/NiOx and NiOx/SrRuO3 interfaces [41]. However for HRS it fitted
the thermionic emission conduction mechanism. The potential reason given for this was lowering of acceptor density which resulted in an increase in schottky barrier.

6.2 Conduction Mechanism in Ru/NiOx/Ru RRAMs

Temperature dependent measurements have been performed for 200 µm x 200 µm area devices for Ru/NiOx/Ru at temperatures ranging from 100 K-335 K. The data collected were fitted to different transport mechanisms like F-P emission, thermionic-field emission, ohmic, ionic, and trap-assisted-tunneling to determine the dominant conduction mechanism. At LRS, the I-V at different temperatures fitted the “ionic conduction mechanism” very well as shown in Fig. 6-1. The equation used for ionic conduction mechanism for the curve fitting is as follows:

Ionic mechanism for LRS:

\[ I \propto \frac{1}{T} \exp\left(-\frac{E_a}{KT}\right) \]  

(7)
The most important factor which decides ionic conduction is the ease with which it can jump or travel to neighboring site. This is termed as the activation energy. The activation energy ($E_a$) was calculated to be 0.03 eV which is quite low for ion-migration to take place. According to the data obtained through cryogenic measurement, the nature of the filament is semiconductor-like as the resistance is decreasing with increase in temperature. From the C-V analysis the acceptor doping density in as-deposited NiO$_x$ was calculated to be of order $10^{20}$ cm$^{-3}$. It can be inferred that O$^{2-}$ ion migration through Ni filament falls in the category of type II ionic conductors, which are generally good ionic conductors at room temperature and fast ionic conductors at high temperatures [42]. Also, lower $E_a$ of 0.03 eV supports that ionic conduction should be fast enough. However, the resistance will start to increase with temperature beyond the critical temperature of 355 K (the maximum point ionic-conduction curve). The data was also

Figure 6-1 Conduction Mechanism at LRS with ionic conduction fit.
analysed by Ohmic conduction mechanism fitting as shown in Fig. 6-2. As evident from $R^2$ values of the fitting, ionic conduction shows better fitting than Ohmic conduction. Therefore, the dominant conduction mechanism through Ni filament was attributed to be ionic over ohmic, which is in contrast with some literature where ohmic conduction was observed. However, those reports are with Pt (TE), SrRuO$_3$ (BE) and with different composition of NiO$_x$ while my data is with Ru electrodes. Therefore, an open question lies in the understanding if the as-deposited composition of NiO$_x$ or the choice of electrodes plays any role in governing the mechanism of conduction in LRS after the filament is formed. Following equation was used for ohmic fitting:

$$I \propto \exp(1/T)$$  \hspace{1cm} (8)

![Figure 6-2 Conduction Mechanism at LRS with ohmic conduction fit at 0.3 V.](image)
On the other hand, in HRS, the I-V at different temperatures displayed excellent fitting for “thermionic field emission” mechanism as shown in Fig. 6-4. During the RESET of the device, the O$^{2-}$ atoms (holes in this case) will be pushed away from the TE creating a Schottky barrier. Considering Ru workfunction (4.6 eV), electron affinity of NiO (1.4 eV) and Fermi level of NiO at 5 eV [43], the barrier height was found to be 0.4 eV. Moreover, the barrier height extracted from the curve fitting was found to be 0.24 eV at HRS. I-V for virgin device fitted for voltage dependent conduction mechanism at room temperature displayed excellent fitting for F-P and thermionic emission, as shown in Fig. 6-3. The extracted barrier height was found to be 0.5 eV from the curve fitting.

Thermionic field emission mechanism for HRS:

\[
I \propto T^2 \exp(1/T)
\]  \hspace{1cm} (9)

F-P emission for VRS at room temperature:

\[
I \propto V \exp(\sqrt{V})
\]  \hspace{1cm} (10)
Figure 6- 3 Conduction Mechanism at HRS with thermionic field emission conduction fit.

Figure 6- 4 Voltage dependent conduction mechanism for F-P emission fitting at VRS.
Figure 6-5 VRS voltage dependent conduction mechanism for thermionic mechanism.

The following table 6.1 summarizes the dominant mechanism of conduction at various resistive states (VRS, LRS and HRS) along with respective parameters being extracted.

Table 6.1 Summary of Conduction Mechanism dominant at different resistive states.

<table>
<thead>
<tr>
<th>Resistance States</th>
<th>Dominant Conduction Mechanism</th>
<th>Extracted Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>VRS</td>
<td>Thermionic and F-P emission</td>
<td>$\Phi_b = 0.5$ eV</td>
</tr>
<tr>
<td>LRS</td>
<td>Ionic conduction</td>
<td>$E_a = 0.03$ eV</td>
</tr>
<tr>
<td>HRS</td>
<td>Thermionic Field Emission</td>
<td>$\Phi_b = 0.24$ eV</td>
</tr>
</tbody>
</table>

$\Phi_b$ is barrier height, $E_a$ is activation energy
Chapter 7

Conclusions and Future Work

7.1 Conclusions

The fundamental properties of NiO$_x$ based RRAM devices with Al, Ru as TE and Ni and Ru as BE were studied respectively. The NiO$_x$ deposition was performed in a relatively high oxygen (20% oxygen in Ar by flow rate) environment.

For Ni/NiO$_x$/Al the initial J-V curves in positive and negative bias indicated symmetric behavior in spite of a significant difference in the vacuum work functions of Al and Ni. The C-V characterizations indicated NiO$_x$ to be a p-type semiconductor with acceptor doping density between $6 \times 10^{18}$ cm$^{-3}$ to $5 \times 10^{20}$ cm$^{-3}$. Switching behavior was observed after electroforming the devices. The devices failed after multiple switching cycles by switching into a relatively low conductive state. The mechanism of failure was attributed to the formation of Al$_2$O$_3$ due to a slow oxidation of Al electrodes with repeated cycles. So TE with low affinity for O$_2$ was chosen i.e Ru.

To conclude for Ru/NiO$_x$/Ru stack, NiO$_x$ based resistive RAMs with higher percentage of O$^{2-}$ atoms can show bistable and repetitive switching with Ru as its BE.
NiO$_x$ with high O$^{2-}$ atoms make it less leaky and hence would allow further scaling of the dielectric thickness. Also by optimizing the compliance level, the size of conducting filament can be controlled. The area of the filament was shown to be dependent primarily on the compliance current during the forming process and independent of the device area. Conversely, HRS current density was shown to be uniform across the device indicating that it can be reduced by scaling down the size of the device. In light of these observations, we believe that a better LRS/HRS ratio can be achieved as the device dimension is scaled down into the deep submicron regime.

### 7.2 Future Work

There is no end in improvising any research output, so it is with this. The $R_{on}/R_{off}$ can be improved by experimenting with different electrode at the bottom after knowing that bistable switching is possible with Ru as TE. Switching speed analysis, durability test needs to be performed in these devices for comparison with other emerging memory devices. The routes to reduce the reset current needs to be investigate. Also, the role of electrodes and composition of NiO$_x$ in switching performance needs further understanding.

A Ru/NiO$_x$/Graphene stack was prepared whose process flow is described in the Appendix. D Graphene electrode has the potential to reduce the switching voltage [43] and hence reduce the power consumption. Moreover, it is transparent [44] and flexible [45] material too. Its tremendous mobility [46] can also benefit the RRAM technology with high speed switching possibly by providing low sheet resistance electrodes.
References


MOSFET with Ti/HfO\textsubscript{2} high-k dielectric,” *Microelectronic Engineering Journal*, vol. 88, pp 1309-1311, 2011.


Appendix A

Statistics of Ni/NiOₓ/Al devices failure

Table A. 1 Switching analysis for 200 µm devices.

<table>
<thead>
<tr>
<th>Device #</th>
<th>Stuck in State</th>
<th>Current Level (A)</th>
<th>Voltage (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>High</td>
<td>Hits compliance</td>
<td>-3</td>
</tr>
<tr>
<td>2</td>
<td>Low</td>
<td>10E-7</td>
<td>1.5</td>
</tr>
<tr>
<td>3</td>
<td>Low</td>
<td>10E-2</td>
<td>2.5</td>
</tr>
<tr>
<td>4</td>
<td>High</td>
<td>Hits compliance</td>
<td>-5</td>
</tr>
<tr>
<td>5</td>
<td>Low</td>
<td>10E-3</td>
<td>3.5</td>
</tr>
</tbody>
</table>

Table A. 2 Switching analysis for 100 µm devices.

<table>
<thead>
<tr>
<th>Device #</th>
<th>Stuck in State</th>
<th>Current Level (A)</th>
<th>Voltage (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>High</td>
<td>Hits compliance</td>
<td>2</td>
</tr>
<tr>
<td>2</td>
<td>Low</td>
<td>10E-3</td>
<td>-4</td>
</tr>
<tr>
<td>3</td>
<td>Low</td>
<td>10E-4</td>
<td>3</td>
</tr>
<tr>
<td>4</td>
<td>Low</td>
<td>10E-4</td>
<td>-4</td>
</tr>
<tr>
<td>5</td>
<td>High</td>
<td>Hits Compliance</td>
<td>3</td>
</tr>
</tbody>
</table>
Table A. 3 Switching analysis for 50 µm devices.

<table>
<thead>
<tr>
<th>Device #</th>
<th>Stuck in State</th>
<th>Current Level (A)</th>
<th>Voltage (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>High</td>
<td>Hits compliance</td>
<td>3</td>
</tr>
<tr>
<td>2</td>
<td>High</td>
<td>Hits compliance</td>
<td>3</td>
</tr>
<tr>
<td>3</td>
<td>High</td>
<td>Hits compliance</td>
<td>-3</td>
</tr>
<tr>
<td>4</td>
<td>Low</td>
<td>10E-3</td>
<td>-1.5</td>
</tr>
</tbody>
</table>
Appendix B

Repeatable Devices for Ru/NiOₓ/Ru Switching

Figure B- 1 200 µm device 1 showing switching cycles.
Figure B-2 200 µm device 2 showing switching cycles.

Figure B-3 200 µm device 3 showing cycles.
Appendix C

Charge Transport Mechanism in High-k Dielectric Based MOS Capacitors

C.1 Introduction

Gate leakage current is becoming the bottleneck in designing of the high speed and low power consumption devices due to continuous scaling of the dielectric thickness of SiO$_2$ [33]. To ensure Moore’s Law remains valid in the next decade, leading integrated circuits (ICs) manufacturers are now making a breakthrough by replacing the long standing SiO$_2$ and polysilicon [34] gate with high-k dielectrics like HfO$_2$, Al$_2$O$_3$, TiO$_2$, and with a metal gate like Ti, W, Pt etc. respectively [35], [36]. The reason for replacement of poly-silicon gate with that of metal gate is to avoid high threshold voltages which arise due to Fermi-level pinning along with degradation of channel carrier mobility [37] - [39]. Fermi level pinning is nothing but inability to entirely move the Fermi level ($E_F$) across Si band gap [40], [41].

However, in poly-Si/HfO$_2$ interface (metal induced gap states) MIGS are more in number and die less swiftly as compared to SiO$_2$. Hence, a larger alteration in work
function would be needed to oscillate $E_F$ across the Si band gap [42]. High-k based dielectric helps in maintaining the same capacitance as that of SiO$_2$ dielectric but with a thinner material layer [43]. In spite of significant research progress in this area [44], the mechanism of charge transport responsible for the gate leakage current and its dependence on the gate dielectrics and metal electrodes is not well-understood. To address this problem, in this chapter, the charge conduction mechanism of gate leakage current in different high-k dielectric based MOS capacitors with metal electrodes on top, have been reported. Temperature dependent measurements were made to compare the charge transport mechanism of atomic layer deposited (ALD) HfO$_2$ based MOS capacitor with that of ALD Al$_2$O$_3$ based MOS capacitor with Ti and W electrodes. In addition to that, temperature dependent measurements were made to compare the charge transport mechanism of atomic layer deposited (ALD) HfO$_2$ based MOS capacitor with that of Al$_2$O$_3$ based MOS capacitor with Ti and W electrodes. I-V curves were fitted for different conduction mechanisms at different temperatures and voltage ranges [45]. A neural network method of modeling has been employed to ease the duplication of same sample by avoiding calculating parameters like effective mass of electron, material specific parameters, which reduces the cost of fabrication and increases the speed of data acquisition.

C.2 Background

The reduction of the gate dielectric thickness is one of the core reasons for increase in gate leakage current of MOS device [46]. To minimize this gate leakage current, many high-k gate dielectrics have been recommended to substitute SiO$_2$ in MOS structure with
effective oxide thickness (EOT) lower than 1.5 nm [47]. To study the interface better, temperature dependent measurements is one of the most important methods to determine the charge transport mechanism of the gate leakage current. Temperature dependent study was performed on Ta$_2$O$_5$ and TiO$_2$ films to determine their conduction mechanisms and to verify whether the gate leakage current is supportable at high temperatures for either of these high-k dielectrics. From studies it was found that in Ta$_2$O$_5$, I-V curves showed stronger temperature dependence than in TiO$_2$ samples [48], [49]. The chief reason was a lower electron barrier height in Ta$_2$O$_5$, which resulted in Schottky emission to dominate the charge conduction mechanism. On the contrary, the TiO$_2$ sample demonstrated tunneling as the dominant conduction mechanism in the high-field region, and F-P conduction in the low-field region. In literature it was reported that, for HfO$_2$ dielectric, a high work function metal (Pt) would be responsible for F-P emission conduction mechanism [50]. This is because the Schottky barrier height would be larger than the energy level of the traps. However, for an Al electrode, Schottky emission dominated the conduction mechanism of gate leakage current. On the other hand, it has been proved that, Al$_2$O$_3$ dielectric based MOS capacitor with Al electrodes showed F-P emission to be dominating charge transport mechanism at Al/Al$_2$O$_3$ interface [51]. In spite of these available researches, a rigorous comparison was needed to identify which conduction mechanism dominates at which voltage level and temperature range for a specific metal/dielectric interface. Temperature dependent comparison has been made at different voltage range to identify the dominant current conduction mechanism. In addition, a neural network model based on Quasi-Newton algorithm was employed for ease of sample reproduction by avoiding extracting parameters like barrier height, effective mass
from equations which are labor intensive and time consuming processes. Neural network’s potential to learn quickly for building convincing solutions to unformulated problems, manage computationally expensive models, deliver fast interpolative analysis, and attaining very precise functional relationships between data sets are its major advantages [52]. It is a well-established method for various process modelings such as the molecular beam epitaxy and plasma-enhanced chemical vapor deposition processes in semiconductor industry [53]. In literature, modeling of semiconductor process device characteristics was done in both the forward and inverse direction [54]. A multilayer perceptron neural network (MLPNN) was used for development of model. In the forward direction, data obtained from the characteristics of earlier fabrication processing points were used as input to a MLPNN, and the last characteristic values were modeled. On the other hand, for inverse modeling, final DC device characteristics measurements of total wafer were used as input to an MLPNN, and in-process characteristic data were modeled. This method eliminates the necessity to statistically describe parametric deviation across a wafer. Modeling of gate leakage current is implemented for reducing the non-uniformity in fabrication process and collect additional data without fabricating the samples again.

C.3 Experimental

HfO$_2$ and Al$_2$O$_3$ dielectric films were deposited on p-type Si wafers by ALD process at 300 °C. The thicknesses for both of the dielectrics were measured to be ~60 Å using ellipsometer. W and Ti metals of 1000 Å were deposited by RF sputtering and the gate electrodes were formed by the liftoff technique on all four devices, namely Al$_2$O$_3$/Ti,
Al₂O₃/W, HfO₂/Ti, and HfO₂/W. The back contact was formed by depositing 1000 Å of Al on the backside of the samples by RF magnetron sputtering followed by a rapid thermal annealing (RTA) in N₂ environment at 600 ºC for 5 minutes to achieve a low resistance ohmic contact.

The modeling of the collected data (gate leakage current) was done using feed forward neural network which constitutes of an input layer, a hidden layer and an output layer. Each layer comprises of several elements called neurons, where the input layer is a relay function, hidden layer is sigmoid function and output layer is linear function of hidden neurons. Each neuron in a layer has an input from previous layer and a constant (called bias) while its output is forwarded to the next layer. The inputs and outputs of the neuron are multiplied by a factor called weights. This feed forward neural network develops a model from the training data supplied. The network is said to be feed forward because each component/element in a layer receives inputs only from the components/elements in the previous layer. The modeling was done by covering the entire temperature points lying in the range of 300 K – 400 K using Quasi-Newton algorithm. Firstly the data set available from experiment was randomized and then segregated into two sections, namely training data set and validation data set. Voltage (-4 V to 4 V) and temperature (300 K, 350 K, 400 K) were taken as the two inputs for the neural network and current (corresponding to the voltage range) as the output. Out of the total data points, 80% were taken to train the neural network and 20% for validating the results. Neural network approach was taken for modeling because the same or additional results can be obtained again without revisiting the whole process of fabrication and
testing. This model will increase the uniformity in fabrication, simplify the data acquisition process and hence increase the future yield.

C.4 Results and Discussions

The samples were probed in the Lakeshore cryogenic probe station and I-V characteristics were obtained by Keithley 4200 Semiconductor Characterization System. The room temperature measurements of gate leakage current for all four samples are shown in Fig. C-1(a). Currents for both devices with Ti electrodes resulted in much lower currents than those with W electrodes.

![Figure C-6](image)

Figure C-6 (a) I-V measurements for HfO₂/W, HfO₂/Ti, Al₂O₃/W, and Al₂O₃/Ti at room temperature.

Temperature dependent studies of gate leakage current were performed for all four devices. The range of temperature, for which, gate leakage currents were measured was from 120 K to 400 K as shown in Fig. C-1(b), with an applied voltage of -4 V. At
temperatures below 250 K, tunneling mechanism dominates as the primary conduction mechanism for all four devices as evident from Fig. C-1(b).

![Graph](image)

Figure C-1 (b) Gate leakage current vs 1000/T for Al₂O₃ and HfO₂ based MOS Capacitors with W and Ti electrodes.

For temperatures at and above room temperature, any of the three, i.e., F-P, Schottky emission and tunneling mechanism may dominate depending upon the voltage range. The processes are not completely independent of each other. It can be observed from Fig. C-1(b) that at higher temperatures, W based samples is showing much higher current than those of Ti based samples. For samples using W electrodes, it is observed that both F-P emission and tunneling mechanism are dominating at the same time. However, for samples using Ti electrodes, tunneling mechanism is dominant at low temperatures only. I-V curves for all the four samples were fitted at 300 K, 350 K, and 400 K employing the following equations [55], [56]:

F-P Emission:
\[ J \propto E \exp(-q(\phi_b - \sqrt{(qE/\pi\xi)/K}) \]  

where \( J \) is current density, \( E \) is electric field of the insulator, \( \phi_b \) is barrier height, \( \xi \) is dielectric permittivity.

Schottky Emission:

\[ J = A T^2 \exp(-q(\phi_b - \sqrt{(qE/\pi\xi)/K}) \]  

where \( A \) is effective Richardson constant.

Tunneling:

\[ J \propto E^2 \exp(-(4\sqrt{2m(q\phi_b)^3/3})/3qhE) \]  

For temperatures above room temperature (300 K, 350 K, 400 K), the observation is split into two cases. Case 1 deals with all the samples in high field region (-1.5 V to -4 V) and Case 2 deals with all the samples in low field region (-0.005 V to -1.5 V).
Figure C-7 (a) Schottky emission curve fit for Al$_2$O$_3$/Ti samples [$-\ln(J/(AT^2))$ vs $E^{1/2}$ (V/cm)$^{1/2}$] for Al$_2$O$_3$/Ti at high field at temperatures of 300 K, 350 K and 400 K.

Figure C-2 (b) F-P emission curve fitting [$-\ln(J/E)$ (A/V*cm) Vs $E^{1/2}$ (V/cm)$^{1/2}$] for Al$_2$O$_3$/W and HfO$_2$/Ti at low and high fields at temperatures of 300 K, 350 K and 400 K.
In case 1 the I-V curve for sample 1 (Al$_2$O$_3$/Ti) fits the Schottky emission model well in this region and a barrier height of 0.59 eV was extracted as shown in Fig. C-2 (a). On the contrary, for sample 2 (Al$_2$O$_3$/W), F-P emission seems to dominate in this region. This is logical, since for W, Schottky barrier becomes too large for Schottky emission to dominate. A barrier height of 0.356 eV was extracted from the curve fitting as shown in Fig. C-2 (b). For sample 3 (HfO$_2$/Ti), it fits the F-P conduction mode extremely well. The calculated Schottky barrier turns out to be greater than the extracted F-P barrier height of 0.58 eV.

![Figure C-8](image)

Figure C-8 (a) Curve fitting for F-P emission [–ln(J/E) (A/Vcm) Vs E$^{1/2}$ (V/cm)$^{1/2}$] and tunnelling [–ln(J/E$^2$) Vs 1/E] for HfO$_2$/W at high field at temperatures of 300 K, 350 K and 400 K.
Figure C-3 (b) F-P emission curve fit [\(-\ln(J/E) (A/V\cdot cm) vs E^{1/2} (V/cm)^{1/2}\)] for Al$_2$O$_3$/Ti sample at low field.

Therefore, at high electric fields F-P emission seems to dominate the conduction mode as shown in Fig. C-3 (a). From Fig. C-1(b), it can be interpreted that the current for sample 4 (HfO$_2$/W), is almost constant, but high relative to sample 1 and sample 3. The reason could be that, at high electric field the I-V curve fits well both in tunnelling and F-P conduction mechanism. Again it is interesting to note from Fig.C-3 (a) that, the curves are not perfectly overlapping for tunnelling mechanism. This is due to the facts that charge conduction mode is not independent. Barrier heights of 0.24 eV and 0.27 eV were extracted for tunnelling and F-P emission respectively.

Now in case 2 at low electric field, for the sample 1, the extracted barrier height of 0.53 eV for F-P emission was lesser than that of Schottky-emission barrier height as shown in Fig.C-3 (b). Therefore, F-P emission seems to dominate at low field for sample 1. Same as in case 1, the calculated Schottky barrier turns out to be greater than the
extracted F-P barrier height of 0.58 eV. Hence, from case 1 and case 2 for sample 2 and sample 3, F-P emission dominates in both the regions as evident from Fig. C-2 (b). However, for sample 4 at low field, Schottky emission acts as the dominant charge conducting mode at low electric field. A barrier height of 0.49 eV was extracted from the curve fitting as shown in Fig. C-4.

![Figure C-9 Curve fitting for Schottky emission](image)

**Figure C-9 Curve fitting for Schottky emission** $[-\ln(J/(AT^2))$ Vs $E^{1/2}$ $(V/cm)^{1/2}$] for HfO$_2$/W at low field at temperatures of 300 K, 350 K and 400 K.

Thereafter, the modeling of the data was done for all four samples using neural network to cover entire temperature points lying in the range of 300 K – 400 K for voltage ranging from -4 V to 4 V. Fig.C-5 shows the actual output current and neural model output current for all the samples. It can be easily observed that the model followed the experimental set of data very closely. Fig.C-5 demonstrated excellent modeling capabilities due to very low percentage of error. Once modeling is done, the current can be
accurately calculated using this model for any given temperature range which will be beneficial in reproducing the result without actually fabricating the device again. Hence, the model is cost effective and helps in speeding the entire process of fabrication and testing of devices. On the contrary, the already established equations like F-P emission, tunneling etc. require defining number of parameters like effective mass or barrier height, before calculating the output current. In this way, just by feeding the trained neural network with two inputs (voltage and temperature); the required output (current) can be easily established. This model in future would also help in comparing with different high-k or different metal gate based MOS capacitors as reproducing data will be very easy.
C.5 Conclusions

The series of experiments showed the method of conduction for different combinations of high-k dielectrics with both low (Ti: 4.3 eV) and mid-gap (W: 4.8 eV) work function metals. The mode of conduction consisted of a combination of F-P emission, Schottky emission, and tunneling, with each mechanism dominating according to the applied bias and temperature. At low temperatures tunneling remains as the dominant mode of conduction. However, at higher temperatures and in low field, mainly F-P emission is dominating the mode of conduction except for HfO$_2$/W sample. For
Al₂O₃ samples, in low field, the conduction mechanism is independent of electrodes being used unlike in high fields. However, for HfO₂ samples, the conduction mechanism is governed both by dielectrics and electrodes for the entire voltage range. Therefore, it is critical to fully understand the consequences in selecting the materials, as device performance could be drastically altered.
Appendix D

Fabrication of Graphene

Graphene is a building unit of graphite. It has extremely high carrier mobility exceeding 200,000 cm\(^2\) V\(^{-1}\) s\(^{-1}\) [57]. The high transparency and flexibility of graphene due to its one atomic thickness can be extremely beneficial for electrodes. Graphene has already been in research to be used in resistive RAM technology. It has been demonstrated that graphene can lower the SET and RESET voltage of a RRAM when used as BE. In this section, the method of fabricating graphene using Metal-Organic Chemical Vapour Deposition (MOCVD) has been discussed.

Following Fig.D-1 shows the steps involved in the process of fabricating graphene. Firstly, on a clean p-type Si substrate a minimum of 1000 Å of Ni was deposited in sputtering system. A thicker Ni would ensure a thicker layer of graphene to be deposited on top of it. After deposition of Ni, the sample was loaded into the MOCVD. There the temperature was elevated to 900 °C and Ar: H\(_2\) (150:125) gas mix was flown into the chamber for 20 mins. The flow rate of the mix was 195 sccm. Thereafter, the flow of Ar was stopped and a CH\(_4\): H\(_2\) mix of ratio 1: 25 were flown into the chamber of MOCVD at the rate of 195 sccm at a constant temperature of 900 °C.
After 20 mins, the temperature was gradually dropped at rate of 5 °C/min until 600 °C and the sample was gradually cooled in the presence of same CH₄ and H₂ gas mix. Subsequently, the gas flow was stopped and only Ar was flown into the chamber for almost 70 min. The sample was then allowed to get cool down to room temperature overnight in the chamber. All the gases were turned off at this time.

Figure D-1 Steps for fabrication of graphene.
Figure D-2 Temperature vs. Time characteristics for fabrication of graphene in MOCVD.
Figure D- 3 Image of Graphene on Ni.
Appendix E

Simulation of GaSb Based MOSFET

Due to constant scaling of the dielectric (SiO$_2$) in the conventional MOSFET structure, huge increase in OFF state current is observed. Therefore SiO$_2$ is being replaced by high-K materials like HfO$_2$. However, the interface of HfO$_2$/Si cannot outshine the exceptional properties of SiO$_2$ and the SiO$_2$/Si (100) interface such as low-defect densities, thermal stability, and excellent uniformity over large area etc. Hence, Si are now being replaced by III-V materials which has very high carrier mobility. Moreover, direct bandgaps in III–V materials which are unavailable in Si- and Ge-based materials, has provided enormous opportunities of fresh device architectures, consequently leading to high-performance integrated circuits. This work mainly focuses on building of p-mosfet using high-k material on III-V substrate (GaSb) [56].
Figure E-1 Structure of p-MOS, Channel length= 100nm, Source/drain depth= 30 nm, tox= 10nm.

Models used to get the simulation results for GaSb based device are also used for Si and Ge based devices, as Si and Ge are well known and well understood materials.

Figure E-2 Drain Current (I_d) vs. (V_d) Drain Voltage for SHI Model for Si/HfO_2.
Figure E-3 Drain Current ($I_d$) vs. Drain Voltage ($V_d$) for Watt Model for Si/HfO$_2$.

Figure E-4 Current ($I_d$) vs. Drain Voltage ($V_d$) for GaSb SHI model.
Table E. 1 Current per unit length for Si, Ge and GaSb for two different models.

<table>
<thead>
<tr>
<th>Material</th>
<th>$I_d$ for Model 1 (SURFMOB(Watt Model))</th>
<th>$I_d$ for Model 2 (SHI (Shirahata Model))</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>.005 A/µm</td>
<td>.0028 A/µm</td>
</tr>
<tr>
<td>Ge</td>
<td>.018 A/µm</td>
<td>.012 A/µm</td>
</tr>
<tr>
<td>GaSb</td>
<td>.02 A/µm</td>
<td>.01 A/µm</td>
</tr>
</tbody>
</table>

The name of the simulator is Silvaco and the inversion layer models used from ATLAS are SHIRAHATA model and WATT model. These models were again compared with a model in literature which is also an ATLAS model. The figures illustrate two different models for Si and GaSb. It is evident from both the models that, GaSb based MOSFET is giving higher current as compared to Si based MOSFET. The models were
also compared with Ge based MOSFETs and from those results it can be concluded that GaSb gives the highest current.