Investigation of growth parameters for as-grown 2D materials-based devices

A Thesis Presented to The Honors Tutorial College, Ohio University

In Partial Fulfillment of the Requirements for Graduation from the Honors Tutorial College with the degree of Bachelor of Science in Physics

By Miles Lindquist

April 2017
Investigation of growth parameters for as-grown 2D materials-based devices

Miles T. Lindquist¹, Shrouq H. Aleithan¹, Sudiksha Khadka¹, Martin E. Kordesch¹ and Eric Stinaff¹

¹Department of Physics and Astronomy, Nanoscale and Quantum Phenomena Institute, Ohio University, Athens, Ohio, OH 45701, USA

ABSTRACT

We investigate the effects of temperature, flow-rate, and growth time for a novel chemical vapor deposition process for producing self-contacted two-dimensional materials-based devices. For a specific set of growth parameters, a lateral thin film extending from the molybdenum pattern is found to monotonically increase in width with increasing growth time. We also observe indications that with an increased reactant delivery rate the film begins to show vertical growth at the expense of the lateral growth. These results will help advance a comprehensive process for the scalable production of as-grown, complex, two-dimensional materials-based device architectures.

INTRODUCTION

Of recent interest in the field of material science is the family of monolayer transition metal dichalcogenides (TMDs). These layered compounds are composed of two chalcogen (S, Se, Te) atoms covalently bonded to one transition metal (Ti, W, Mo, etc.) atom in two dimensional (2D) layers, with each layer of bonded molecules held together by relatively weak van der Waals forces [1,2]. Molybdenum disulfide (MoS₂),
one of the most studied TMDs, has a direct band gap of 1.8 eV in its monolayer limit, which, along with large absorption, strong room-temperature emission, non-linear response, and optical control of spin and valley degrees of freedom [2-5], makes MoS$_2$ an excellent candidate for ultrasensitive photo detectors [6], valleytronics [7], and energy harvesting devices [8]. Monolayer MoS$_2$ is also attractive to manufacturers of digital electronics because of its very high ON/OFF ratio ($>10^7$) [9], good mobility [2,9], excellent thermal properties [5], and ability to form heterostructures with other 2D materials [2]. However, the ability to controllably process material into working devices with any scalability is still one of the largest impediments in the field.

Since their discovery, the methods for monolayer TMD device production remain both difficult to scale and reproduce. Mechanical exfoliation of bulk crystals, in addition to being difficult and time consuming to perform, results in peeled flakes with varying numbers of layer. Early utilization of chemical vapor deposition (CVD) could produce substantial numbers of large, monolayer, single-crystals. However, due to random nucleation, the location, number, and size of the crystals grown is not strictly controllable. Several studies have reported success in the growth of templated as well as continuous thin films on large substrates via CVD for example by seeding the substrate with aromatic molecules, such as reduced graphene oxide (r-GO), perylene-3,4,9,10-tetracarboxylic acid tetrapotassium salt (PTAS) and perylene-3,4,9,10-tetracarboxylic dianhydride (PTCDA), which has been found to produce high-quality, large-area, monolayer growth on a variety of substrates [10-21]. Though the resulting material is typically polycrystalline, and it remains a challenge to alleviate layer thickness fluctuations, these techniques represent promising routes to providing a starting point for
device manufacturing. Another hurdle to scalable device production is patterning and contacting the material. This typically involves using a combination of etching, transfer, lithography and metal deposition. Each of these steps may introduce variability and/or damage to the material, and therefore often require further processing in order to obtain reasonable metal-semiconductor contacts and device performance. Here we report on the optimization of an original process where we begin with lithographically defined metallic patterns around which 2D material is grown, forming self-contacted as-grown device structures in a single step.

This process is based on a typical CVD reaction involving chalcogen and transition metal oxide based precursors. When utilizing an oxide precursor, growth of MoS$_2$ via chemical vapor deposition relies on the reduction of MoO$_3$ to the suboxide MoO$_{3-x}$, followed by the replacement of oxygen by vaporized sulfur. This multi-step reaction is shown in Equations 1 and 2 below [22].

$$MoO_3 + \frac{x}{2} S \rightarrow MoO_{3-x} + \frac{x}{2} SO_2$$  \hspace{1cm} (1)

$$MoO_{3-x} + \frac{(7-x)}{2} S \rightarrow MoS_2 + \frac{(3-x)}{2} SO_2$$  \hspace{1cm} (2)

Interaction between the initial reactants in Equation 1 take place after both are heated from their solid form, after which an inert gas delivers the reactants to each other. It is theorized that there are two possible, and perhaps simultaneous deposition scenarios taking place, one in which the MoO$_{3-x}$ suboxide adsorbs on the substrate prior to their sulfurization, and another in which the suboxide vapor and sulfur vapor react while being delivered to finally adsorb and nucleate on the substrate. While the exact ratio is difficult to predict, the relative prevalence of both processes is affected by the temperature and
location of the substrate and reactants [23]. Presumably, it is also affected by the rate at which the reactants are delivered to each other and the substrate.

Given the complex and novel nature of monolayer MoS$_2$ growth via CVD, the precision required to reproduce results in a process governed by fluid dynamics, and the atomically thin scale of the final products, it is often challenging to identify and determine the essential parameters involved in monolayer growth. In this paper, to advance the development of a repeatable and scalable production method of monolayer MoS$_2$, we examine the effect of critical parameters such as time, temperature, and flow rate on the deterministic growth of monolayer films seeded off a Mo metal pattern produced via photolithography [24].

**EXPERIMENT**

Patterned samples were produced via UV lithography on p-doped Si wafers with a 5 kÅ thick oxide layer. A basic lift-off lithography process was performed using a home-built system with AZ 5214e negative resist, exposed to a 365 nm LED array. Post development, resist-coated samples typically had excess undeveloped resist within the non-exposed areas which was cleaned with an AC plasma exchange system. Using a Denton Vacuum DV-502A DC sputtering system, a 160 ± 10 nm layer thick film of molybdenum was deposited and the photoresist was removed leaving behind the desired metallic patterns which were cleaned using DI water, acetone and isopropanol.

The general CVD procedure used is similar to that described by C. Cong, et al. [12], as well as Khadka, S., et al. [24], with the modification that the patterned substrate and the MoO$_3$ precursor were located at different positions within the furnace, similar to
typical low-pressure CVD techniques [23]. This allowed for some degree of independent control over the reactant temperatures.

Figure 1. a, Schematic diagram of the CVD setup. b, Temperature profile of furnace at temperature of 750 °C. The red diamond and blue square indicate the sample and oxide precursor positions respectively.

The growth was performed using a Thermolyne 21100 Tube Furnace heated to 750 °C with an open-open two-inch diameter quartz tube containing an open-closed one-inch diameter quartz tube 60.7 cm in length (Figure 1a). Inside the smaller quartz tube, the substrate was placed with the pattern facing up on a graphite platform toward the downstream end of the furnace, 8.7 cm left of the center. Another graphite platform with 7-8 mg of molybdenum trioxide (MoO₃) powder was placed 6.3 cm right of the furnace’s center. A boron nitride boat containing 150 mg of sulfur powder was placed 32 cm right of the center of the furnace. For all growth trials the furnace was set to 600 °C at an approximate ramp rate of 54 °C/min for 15 minutes, then to 750 °C at a rate of approximately 29 °C/min for 20 minutes. During this time, a small (<0.010 LPM) flow of argon was sent through the larger quartz tube. To melt the sulfur powder, an Atten Instruments 850B heat gun was placed in direct contact with the outer quartz tube underneath the boron nitride boat. With the heater’s filament set to 480 °C the sulfur would melt within one minute, after which the flow of argon was increased to 0.09 LPM. The melting of the sulfur was used as the starting point of the growth time. For the trials described below the amount of time that the sulfur was heated was varied after which, the
heat gun was removed and the furnace was turned off to cool naturally. During cooldown, the flow is kept at 0.09 LPM until the removal of the sample.

RESULTS AND DISCUSSION

A representative area from the first sample, with a growth time of 20 min, is analyzed in detail in Figure 2. The contrast on the optical image, Fig. 1a, indicated a uniform thin film growth extending 6 µm laterally out from the molybdenum metal. The photoluminescence (PL) spectra, Figure 2d, shows the characteristic excitonic states, A and B, derived from the spin-orbit split valence band and the degenerate conduction band [1]. The low energy A exciton is typically the most intense peak, centered around 660 nm, and shows a six-fold increase in intensity when comparing few-layer to mono-layer (Fig. 2d), comparable to typical exfoliated material [1,25]. As a final confirmation, Figure 2c and 2e display the difference in wavenumbers between the \( E_{2g}^1 \) and \( A_{1g} \) lines in the Raman spectra, which show an absolute separation of 20 to 21 cm\(^{-1}\) for the monolayer regions, consistent with previous CVD grown material [26]. Near the metal patterns the
growth appears mostly multi-layer and as the film extends out the majority is comprised of monolayer material.

Figure 2. Optical analysis of MoS$_2$ grown on a molybdenum pattern. a, Optical image of the as-grown sample showing a continuous uniform film around the edge of the Mo pattern. b and c, Photoluminescence map and Raman analysis map, respectively. The scale bars in a-c are 5µm. The brightness of the PL map is proportional to the integrated intensity between 550 to 750 nm, while the color scale on the Raman map indicates the separation between the $E_{2g}^1$ and $A_{1g}$ in wavenumbers. d and e, Photoluminescence and Raman spectra from the regions indicated with the black and red circles. From these spectra it can be seen that the increase in PL intensity correlates with a decrease in the Raman peak separation, as expected.

To determine the effect of growth time, defined as the time elapsed from the melting of the sulfur to the point where the heat gun was removed, on the lateral extent and quality of material grown we conducted multiple trials in which all other parameters were nominally held constant. The amount of sulfur used in each trial was also held constant (150 mg) and only in the 40 minute growth time trial was the material completely consumed. Therefore, the rate of sulfur delivery should be the similar in all trials with only the total amount delivered varying. The results of a sequence of growths, done over four separate days, are shown in Figure 3a-d.
Qualitatively, we observe uniform thin film growth from the metal pattern out to the film’s edge in the 20 and 30 minute growths. Along the outside edge of the material for the 25 and 40 minute growths, we can identify multi-layer growth. While it is difficult to ascertain the definite cause of this deviation in growth, we hypothesize that the increase in vertical growth on the edge is a result of an increased rate of reactant delivery. This is supported by a result from a separate 30 minute growth shown in Figure 4c in which the BN boat was not level and the sulfur flowed towards the furnace after melting. This increased the overall temperature the sulfur was subject to and therefore increased the sulfur delivery rate, which was confirmed by the observation that all 150 mg of the sulfur was consumed within the 30 minutes. From this trial, we see a decrease in lateral growth, and a considerable increase in vertical growth, emphasizing the importance of
multiple parameters on the overall growth process. For example, when the vaporization rate of the sulfur is well controlled, the growth time functions as a good measure of the total sulfur delivered as well as reaction time inside the furnace. Whereas, the result in Figure 4c, from the increased rate of sulfur melting, indicates that the rate of reactant delivery must be kept in careful equilibrium with the time allowed for reaction. Similarly, it is likely that variability in the argon flow inside the chamber may also significantly affect the delivery rate of the reactants, leading to variations in the growth rate.

The average lateral extent of growth for the sequence is plotted in Figure 3e indicating a linear dependence on time, with a growth rate of about 0.3 \( \mu \)m/min, within this range. Though a monotonic increase of lateral size with time, within a certain window, may not be surprising, it is very likely that the rate and functional dependence of the growth is highly susceptible to variations in other parameters such as temperature and argon flow rate. We also note that with growth times of less than 15 minutes we found no growth, indicating that there may be a rapid onset of growth which then slows to a constant rate. It is also expected that the maximum extent of the growth will be effectively limited by the onset of multi-layer growth on the monolayer material. In Figure 3e, we have plotted the lateral growth from three additional growths of 18, 20, and 30 minutes in which the sulfur delivery rate was markedly increased due to either increased temperature or gas flow rate. These points follow a linear trend, but, as with the example in Figure 4c, indicate a decrease in the extent of lateral growth at the expense of vertical growth as compared to the original time series with a lower delivery rate.
Figure 4. a-c, Results from an 18 minute, 20 minute, and 30 minute growth, respectively. The reactant delivery rates were higher than the series in Figure 3 resulting in decreased lateral growth and increased vertical growth. We note that the pattern grown on in Figure 4a and b is a different pattern than c, owing to the increased width of the bulk Mo metal. Scale bars are 4 µm.

We note that the results from our growth technique also depend on the temperature of the substrate and chamber. In Figure 5a and b, we see two separate growth results from our previously used single-zone technique (described at length in Khadka, et al.) in which the patterned substrate and MoO₃ powder are in contact with each other and placed in the center of the furnace set to 600 °C and 780 °C respectively. The significant difference between the extent of surrounding growth indicates that growth is more readily achieved at temperatures above 600 °C. The dark color and jagged edges of the sample in Figure 5b also indicate a high degree of sulfurization of the bulk molybdenum.

Figure 5. a, Example of growth at 600 °C with bulk Mo intact and low growth yield. b, Example of growth at 780 °C showing severe sulfurization of the metal pads and a large increase in lateral growth.
CONCLUSIONS

As is typically the case with CVD, the parameter space for growth is large and complex and the need for precision control is often essential for successful growth. Even though our system is relatively basic, our results indicate that the use of bulk metallic patterns to nucleate and assist the material growth aids in the reproducibility and robustness of the growth process, in addition to providing as-grown electrical contact to the material. We have shown that for a specific set of parameters, control over the lateral size of the material may be achieved. We are currently in the process of upgrading our system to provide tighter control over relevant variables. For example, the addition of a mass flow controller will allow for precise control of the inert gas flow and therefore the reactant delivery. We are also investigating materials placement and configuration to optimize the delivery of the reactants to the patterned substrate. A better understanding of the fluid dynamics within the chamber, for example using titanium dioxide (TiO$_2$) smoke to track the movement of the gas flow may assist in this optimization [27].

Another significant limitation of our current setup is the dependence on the non-uniform heat profile to provide multi-zone capabilities. We are constructing a furnace with true multi-zone heating, allowing for independent control of the reactant and substrate temperatures, ramp-rates, and growth time. In addition to these experimental improvements, we will utilize emerging theoretical results to guide our parameter optimization, for example to minimize the Gibbs free energy in the system to reach thermodynamic equilibrium [27].

We have presented results from an investigation into relevant parameters for controllable lateral growth of monolayer MoS$_2$ around bulk metallic patterns. These
results indicate the temperature, reactant delivery rate, and overall growth time all contribute to the extent, thickness, and overall quality of the film growth. The ability to control the extent of the film growth is essential for the fabrication of arbitrary device geometries, and with continued refinements, as presented here, this general process for creating as-grown two-dimensional materials-based devices may provide a path to produce complex device structures and wafer scale circuits with broad implications for basic research and industrial applications.

ACKNOWLEDGMENTS

This work was supported by the Ohio University Innovation Strategy as well as the Ohio University CMSS and NQPI programs. The authors would like to thank Prof. Hugh Richardson for access to, and assistance with, the Witec system.
REFERENCES


Kordesch, and E. Stinaff, Advanced Materials Interfaces 1600599 (2016).
25. A. Splendiani, L. Sun, Y. Zhang, T. Li, J. Kim, C.-Y. Chim, G. Galli, and F. Wang,
27. H.O. Pierson and H.O. Pierson, Handbook of Chemical Vapor Deposition, 2nd ed
LITERATURE REVIEW

Since its midcentury invention and the identification of its utility in the production of computer components, the transistor has been aggressively miniaturized in an effort to increase computing power by decreasing the size of the components. This has led to an enormous amount of research into the most scalable, consistent, and cost-effective methods of producing microscopic circuits on a substrate. The most prevalent method in use has been the process of photolithography. It has been optimized to such a high level that the mass production of billions of nanoscale transistors on a single integrated circuit is possible [1]. However, the miniaturization process can only go so far, quantum mechanical restraints restrict the size of the features to a level that is quickly being approached [2,3]. This limit of production calls for a novel approach. Research has recently identified two-dimensional transition-metal dichalcogenides (TMD), most notably MoS$_2$ and WS$_2$, to be a promising solution. These nanoscale crystals are only one atomic layer thick, and display desirable semiconducting properties for use in future digital electronics. However, their mode of production is an issue, due to a lack of scalability. Fortunately, chemical vapor deposition, a method of thin film deposition commonly used in semiconductor production, has shown promise in the mass production of monolayer TMD crystals, though many challenges lie ahead [4]. In this literature review, we will review the theory behind semiconductors and transistors, the current and future construction of nanoscale transistors, the process of photolithography and the steps that led to the sophisticated lithographic procedures used today. Following that, we will review the properties, potential applications, and characterization methods of two-dimensional transition-metal dichalcogenides. Finally, we will review chemical vapor
deposition and its use in the production of integrated circuits, as well as its use as a scalable method of TMD crystal production.

**TRANSISTORS**

Modern computing, and consequently much of the modern world, heavily utilizes the semiconductor. Semiconducting materials, as the name implies, are the middle ground between conducting materials and insulating materials. Conductivity in solids are modeled by two energy bands, the valence band and the conduction band. Valence electrons are the outermost electrons of an atom, the electrons that participate in covalent bonds with other atoms in compounds. At 0 K (absolute zero), the valence electrons are all contained in the valence band. When the electrons gain enough energy via the inevitable heating of a solid at 0 K, these electrons will become energized and break from their covalent bonds. In a conductive metal, the energy gap between the valence and conduction bands (referred to as a “band gap”) tends to be very small, or the bands themselves will overlap, indicating that the material has a low electrical resistivity. Semiconductors have a small (1-2 eV), non-zero band gap that requires an energy input to cross. Insulators, materials with a high resistivity, have a larger band gap (>3.5 eV), preventing any significant flow of electrons [5]. It is also important to note that the population of charge carriers in each band is a major contributor to the conductivity of a solid. In conductors, the valence band can either be partially filled due to low amount of valence electrons, or a full valence band and a conduction band will overlap, partially filling the conduction band. This allows for the free movement of electrons: conduction. Insulators instead have a valence band completely full of bonded valence electrons and a completely empty conduction band which, along with its large band gap, prevents any
significant amount of charge carriers to move. Semiconductors exist on the edge of this dichotomy; the small band gap will allow electrons to move from the valence to the conduction band much more readily than an insulator, allowing for conduction, albeit after a larger energy input than a conductor [5].

When an electron (negatively charged) moves from the valence band to the conduction band it leaves behind an empty state in the valence band. If a remaining valence electron in the valence band gains enough energy, it can move into this empty state, then into other empty states. Movement of an electron between empty states can also be described as the movement of a positive charge in the opposite direction, this so-called positive charge is referred to as a “hole” and is the second charge carrier in the conducting of electricity within semi-conductors [5]. Most circuits use doped semiconductors, compounds that contain a low percentage of another element that allow for increased control over the semiconducting properties of the majority element. Doping is a technique that takes advantage of the differing amount of valence electrons between groups (columns) on the periodic table. For example, germanium (Ge) has four valence electrons, while arsenide (As) has five valence electrons. Bonding an arsenic atom to a gallium lattice would result in one loosely bonded electron that can be excited to the conduction band with much less energy input leaving only a slightly positive impurity in the material. A semiconductor with excess electrons is referred to as n-type (negative-type). A p-type (positive-type) semiconductor would be an atom with less valence electrons in a lattice with an element with more valence electrons. For example, a boron (three valence electrons) atom in a silicon (four valence electrons) lattice would result in
a lack of a bond that another valence electron, given a requisite increase in energy, could fill. [5].

The transistor, a device consisting of joined n-p-n or p-n-p semiconductors, is used in modern computing hardware as a current- or voltage-controlled switch. Attached to each section of the transistor is a lead. On the n-doped (or p-doped in a p-n-p semiconductor) are the emitter and collector leads, the oppositely doped section is attached to the base lead.

Electrons flow from the emitter to the collector. In forward-active mode, the current flows as seen in Figure 1. The voltage difference between the collector and base voltage forms an electric field that pulls the electron towards the base. These electrons will diffuse across the base, where they are then picked up by the electric field from the potential difference between the base and collector. The successful movement of electrons from emitter to collector results in current flowing through the circuit. If there is no voltage difference between the base and the either of the other nodes, no electric field is created and no current flows [5]. Extrapolating to a much higher order of magnitude, an array

Figure 1 – Simple diagram of n-p-n bipolar transistor operating in forward-active mode. Note that the current displayed is the archaic (but accepted) movement of positive charge. Movement of electrons are simply in the opposite direction of what is displayed [5].

Figure 2 – Graph of ideal minority charge carrier distribution of bipolar transistor seen in Figure 1. The negative linear slope $n_e(x)$ shows the diffusion of electrons from the emitter side of the base to the collector side [5].
of billions of open-closed switches allows for the representation of number or letter values as series of ones and zeroes (the open-closed binary state we see in our transistor).

We will next examine the operation of a metal-oxide-semiconductor field-effect transistor (MOSFET). The transistors in the integrated circuits in most of today’s electronics are MOSFETs. Field-effect transistors take advantage of the attractive force between positive and negatively charged particles, and the field that forms between them at a distance. MOSFETs are composed of three components: the conducting metal that connects to the rest of the circuit, an electrically insulating oxide that is deposited between the gate and the third component, the doped semiconducting substrate. This semiconducting substrate also has regions of the opposite doping near the source and drain leads. The flow of charge carriers through the transistor depends entirely on the voltage difference between the gate node and the source node. If the gate node is not connected to a power source that will provide a potential difference, the voltage difference (\(V_{GS}\)) is zero and there is no electric field between the metal gate and the semiconducting substrate. As \(V_{GS}\) is raised, there is an isolation of positive charge on the gate (electrons will become attracted to the positive end of the power source the gate is connected to), leading to a net positive charge attracting negative charges on the substrate. Once this threshold is passed, the depletion region (region of excess negative charge) surrounding the junction between the n and p-doped sections of the substrate will merge with the excess negative charges below the

---

**Figure 3 - Cross-sectional diagram of a n-channel MOSFET.** Electrons are the majority charge carriers in nMOSFETs. Depletion regions of electron concentration will form around the regions labeled n+ that eventually connect once electrons move towards the channel region below the gate [1].
oxide layer, forming a region of negative charge in which current can flow between the source and drain nodes. The insulating oxide layer separating the gate and substrate prevents any current from entering the node. In this manner, we can see how the MOSFET performs its switching operation [1].

With the examination of the state of switching transistors in today’s electronics, we will move onto how researchers have used two-dimensional TMDs to perform the same duty. Radisavljevic, B., et al. constructed a FET with monolayer MoS$_2$ on a SiO$_2$ substrate, using hafnium oxide as a gate dielectric between the MoS$_2$ and the top gate. The monolayer MoS$_2$ channel was 6.5 Å thick and the transistor showed mobility values around 200 cm$^2$ V$^{-1}$ s$^{-1}$, and an ON/OFF ratio of $10^8$. This outperforms the goals that the authors noted for transistor materials replacing silicon. The authors show that they can readily control the density of the charge carriers by grounding the substrate’s back-gate ($V_{BG} = 0$ V), and just applying a voltage to the top gate [6].

Another form of device construction that has been seen in research is an FET with no top gate, seen in Figure 5. These devices simply flip the geometry of the MOSFET, with the substrate acting as the gate, and the TMD film as the doped substrate. Das, S., et
al. use this device geometry to examine the contact between MoS\(_2\) and various metals deposited to function as the source and drain leads. They dispute the observed ohmic (low, non-varying resistance) nature of the contacts between the gold and MoS\(_2\) in devices like Radisavljevic, B., et al.’s, claiming that the contacts are affected by a Schottky barrier, a rectifying layer present between metal and doped semiconductors that requires a significantly large voltage bias to let current through [1]. They say that applying a high gate-source voltage could lead one to conclude that there is no Schottky barrier due to an influx of electrons flowing due thermally assisted tunneling. Platinum (Pt), nickel (Ni), titanium (Ti) and scandium (Sc) were found to have Schottky barrier heights of 230, 150, 50 and 30 meV, respectively. A plot showing the effect these Schottky barriers have on the current flowing through the transistor once switched on shows the dramatic effect that a high Schottky barrier can have on the operation of a transistor. Consequently, Das, S., et al. measured mobility values of 21, 36, 125, and 184 cm\(^2\) V\(^{-1}\) s\(^{-1}\) for Pt, Ni, Ti, and Sc, another indicator of a severe drop off in the performance of MoS\(_2\) transistors due to Schottky barriers [7].

*Figure 5* – Plot of current flowing through the transistor as a function of gate voltage applied once the threshold voltage is reached for contacts between various metals and MoS\(_2\). Inset shows current flowing through the transistor as a function of voltage difference between the drain and source nodes [7].
In an effort to bypass the Schottky barrier, researchers have developed new methods of contacting leads to TMDs that better resemble an ohmic contact. Chuang, H.-J., et al. investigated the merits of using “2D-2D contacts”, where the semiconducting TMD channel of the transistor is contacted vertically by another degenerately (highly) doped two dimensional 2D film. Degenerately doped semiconductors are so highly doped that they begin to adopt metallic electrical characteristics, which avoids the Schottky barrier between the metallic source and drain leads, while maintaining the geometry and composition necessary for van der Waals bonding between the TMDs. The specific device architecture is seen in Figure 7. In the case of MoS$_2$ the researchers used degenerately p-doped molybdenum dioxide (Nb$_{0.005}$Mo$_{0.995}$S$_2$) and non-doped MoS$_2$. To test if there is a Schottky barrier present, they tested the sample at a temperature of 5 K as opposed to the room temperature of 300 K. They found that the conductivity increased by a factor of approximately 13, indicating that there is no drop in current from a lack of thermally assisted tunneling that would be present in a contact with a Schottky barrier [8].

While transistors on their own are a useful electronic component in circuits, their utility becomes immensely invaluable in large numbers functioning as switches in digital electronics. By this metric, the success of a semiconducting material in the modern world
is based entirely on the success of a technique that can reliably produce it in large numbers on the nanoscale.

**PHOTOLITHOGRAPHY**

Photolithography is a process that allows for the selective coating of specific areas on a flat, planar surface. In today’s world, it is utilized to create the nanoscale components found on integrated circuits. This is achieved through the use of a photosensitive chemical commonly referred to as photoresist (or “resist”, for short), a mask with opaque patterns, a source of high frequency (typically ultraviolet) light, and a substrate. In a basic process, the resist will be spun on the substrate to coat the surface with a thin film of approximately 1-2 µm. The coated substrate is then placed under the mask where it will be selectively exposed to ultraviolet (UV) light that alters the characteristics of the resist, most notably its solubility in the presence of specific developers [9]. There are two kinds of photoresists used, negative and positive. Positive resists simply become soluble when exposed to UV light, resulting in the area exposed dissolving when developed. The result of photolithography with a positive resist will be a photoresist replica of the opaque section of the mask. The exposed polymers of negative resist crosslink to become insoluble and non-photosensitive when heated after the initial UV exposure. Exposing the entire substrate to UV light will then make the initially unexposed portion soluble. The

![Diagram showing basic photolithographic process with positive tone resist and metal deposition](image-url)
ultimate step in this process is the developing phase, where the resist is selectively dissolved based on the resist’s processing, resulting in a preferentially coated substrate. Photolithography with a negative resist will result in a hole in the resist film shaped like the opaque section of the mask [10].

The origins of photolithography can be traced back to the seventeenth century, when the French inventor Nicéphore Niépce, famously known as the inventor of photography, transferred an image on oiled paper to a glass plate coated with asphalt-lavender oil solution which hardened in the regions exposed to more sun. The shaded areas were softer and more readily washed away by turpentine and lavender oil. A process similar to his was optimized to produce circuit boards in the 1940s, leading to the production of integrated circuits on silicon wafers twenty years later. Since its introduction to the semiconductor industry in the latter half of the 20th century, the process of photolithography has been improved upon to produce ever-shrinking features on a substrate allowing for more transistors on a single processor, upholding the prophetic Moore’s Law, initially proposed in 1965 [9].

Improvements have been made in every aspect of the process with the same express goal: making the smallest features possible. Evidence of this improvement can be seen when reading Thompson, L.F., et al.’s 1976 paper that proposes polymer resists capable of producing features at as small as 1 μm. Contrasting this with Goethals, A.M., et al.’s 2003 paper where the proposed resist will be capable of features as small as 65 nm, we see that in less than thirty years, the sizes have shrunk by a factor of 15 [11,12]. The approaches that led to these improvements varied, and were applied based on the potential scalability and benefit of their application.
One of the more obvious approaches to increase the resolution of the patterns was to use light with a smaller wavelength. Near ultraviolet light (UV) has the largest wavelength which ranges from 350 nm to 500 nm. Deep ultraviolet light (DUV) is in the middle of the spectrum at 150 nm to 300 nm and extreme ultraviolet light (EUV), also referred to as soft x-rays, is the highest frequency (smallest wavelength) light used, with a wavelength of 10-14 nm. Light with a wavelength smaller than EUV are classified as x-rays, and are used in a separate technique known as x-ray lithography. However, complications arise as one increases the frequency of the light. For example, the intensity of the light emitted from sources capable of producing higher frequency light tends to be lower, and the additional optical components required to focus this light will absorb more of the light that passes through them, resulting in the need for sophisticated reflection systems as well as a need for a resist more sensitive to light. Obstacles such as this make the prospect of using EUV lithography on an industrial scale a difficult task [9,13]. Challenges in introducing shorter wavelength light are outlined by Goethals, A.M., et al. who are interested in achieving device resolution of 65 nm. They identified prior issues with the CaF$_2$ material used in the lithography system’s lens, as well as currently unsolved issues such as resist shrinkage or line-edge roughness seen in Figure 9.

Even with the challenges of using higher frequency light overcome, the size of the smallest features one can hope to produce using just ultraviolet light is roughly equal to

![Resist A and Resist B](image-url)
the value of the wavelength (known as the diffraction limit), resulting in a very clear limit of production when restricted to lower frequency light [9]. To bypass this limitation, less direct steps must be taken. Increased research devoted to pushing forward photomask technology has resulted in optically sophisticated masks that allow for increased resolution such as the phase-shifting mask [9]. The concept of a phase-shifting mask, a specially designed mask selectively covered by a thin, transparent film that shifts the phase of the light passing through it, was shown to have a 40\% increase in resolution in 1982 by Levenson, et al. This technique of resolution improvement relies on the mechanism of diffraction and phase-difference interference. It is seen in in Fig. 10a on the “I at Wafer” diagram that the number of photons reaching the point between the two apertures shown on the second line down is significant. This is due to the diffraction, or bending, of waves as they pass through an opening. Light waves from adjacent apertures will constructively interfere with each other where their waveforms line up, creating an even larger wave, represented by the aforementioned peak. Shifting the phase of the light passing through one of these apertures results in the destructive interference of the coinciding light waves (effectively the peaks of one waveform lines up with the troughs of the other wavelength), resulting in a complete cancellation of the wave. This is evident in the bottom line of Fig. 10b, where two distinct peaks are shown. These two peaks correspond to the light that is...
reaching the exposed sections of resist, whereas the trough has now become a section that is not exposed to light, i.e.: the trough is now a smaller feature that was unachievable with a simple photomask [14].

Advances in mask technology also allowed for increased efficiency in the production of specific features. The development of gray-tone masks allowed for single step production of 3D shaping of deposited features, allowing one to adjust the height profile of the pattern, not just its two-dimensional shape on the substrate. This is achieved by selectively changing the opacity of the metal plating on the mask via adjusting the density of small holes in the metallic portion of the mask. A higher density of holes will allow for more light to be let through, but will not transfer to the resist due to the resolution limitations of the light [15].

In the most recent years, the semiconductor industry has been using immersion lithography in to produce 20 nm logic gates on their processors. Immersion lithography instead uses the higher index of refraction of water or any other immersion liquid to increase the resolution of the lithographic features. It is predicted that Intel will move to EUV lithography in the next generation of their devices [16,17].
As of April 2016, Intel has shipped microprocessors featuring transistor gates made from silicon at a resolution of 14 nm. As the size of the transistor gate decreases past 7 nm, quantum tunneling effects become prevalent, indicating the need for new technologies such as transistors made from two-dimensional TMDs [3,18].

**TRANSITION METAL DICHALCOGENIDES**

Following the discovery of the monolayer variant of graphite, graphene, and its exotic electronic properties, the scientific community was interested in possibilities of its use in electronics. Unfortunately, the new material fell short in its application digital electronics due to its extremely small band gap of <200 meV. This lack of a band gap makes it impossible to switch the current on or off in a transistor, preventing any potential utility in the construction of digital electronics [19]. Since then, much research has gone into the alternative monolayer semiconducting materials, most notably transition metal dichalcogenides such as MoS$_2$ and WS$_2$ [4].

Monolayer MoS$_2$ was first prepared, among other materials, via mechanical exfoliation by Novoselov, K.S., et al. and was found to be a stable material that acted as a highly-doped semiconductor when isolated to a single layer. Further research by Mak, K. F. et al. showed a 1.9 eV direct band gap for monolayer MoS$_2$, and an inverse relationship (seen in Figure 12) between the size of the band gap and the thickness of the crystal [20,21].

*Figure 12 - Graph showing the band gap of two-dimensional MoS$_2$ as a function of layer number [21].*
Two-dimensional TMDs are considered to be key components for the next generation of electronics due to their excellent electronic properties, unique physical characteristics, and low material cost. For example, MoS$_2$ has a high ON/OFF current ratio of about $10^8$, indicating that there is a 100-million-fold difference between the current that flows through the transistor in its on and off states [4]. The large band gap, ON/OFF current ratio, as well as a high thermal stability makes MoS$_2$ suited to switching, in this case as a logic gate in an integrated circuit [22]. It is the charge carrier mobility of MoS$_2$ with a high-κ gate dielectric (around 200 cm$^2$ V$^{-1}$ s$^{-1}$) that places it at the similar performance level of silicon and as a viable candidate for use in low power electronics [22,23]

Monolayer MoS$_2$ is particularly well suited for use in optoelectronics due to its direct band gap of 1.9 eV. The direct band gap allows for the absorption and emission of photons, owing to its very high photoluminescence. This is in direct contrast to MoS$_2$’s bulk form that has an indirect band gap of 1.2 eV. Flexible photovoltaic cells made from organic compounds deviate wildly from the Shockley-Queisser limit, the maximum theoretical limit of the efficiency of a single-junction solar cell (see Figure 13). We see also that the band gap (1.9 eV for MoS$_2$) of monolayer

![Figure 13 - Comparison of various materials used in solar panels by band gap and field effect mobility [4].](image-url)
TMDs trend closer to the band gap of the Shockley-Queisser limit (1.3 eV), showing promise as a replacement or supplement for flexible organic solar cells [4].

LEDs using two-dimensional TMDs have also been considered, but progress is hindered by the lack of any known method capable of doping the flakes to tune the color of the light emitted [4]. Additionally, there has been consideration of using TMDs for thin, flexible electronics. However, this would require the use of a plastic substrate that would melt in the high temperatures required for the CVD growth of TMDs. While the prospect of flexible electronics is exciting, this hurdle seems to have stopped research in that area [4].

The atomic-scale dimensions of TMD flakes require the use of sophisticated classification techniques. With the correct color substrate providing contrast, TMD crystals are visible with an optical microscope. To determine the thickness, composition and photoactivity of the flakes, atomic-force microscopy, photoluminescence measuring, and Raman spectroscopy are used.

Raman spectroscopy measures the excitation of molecular bonds from a laser. The photons’ energy from the laser are then shifted up or down because of its inelastic interaction with the compound, then is collected by a detector. The technique is fairly ubiquitous as a chemical

Figure 14 - Raman spectra comparing peaks of differently layered MoS2 [24].
identifier, so we will see how it applies to the characterization of MoS\(_2\) of various layers. Figure 14 shows a Raman spectra of a mechanically exfoliated MoS\(_2\) flake with varying layers. The flake has been excited by a 488 nm laser under atmospheric conditions. An obvious trend is seen as the layers of MoS\(_2\) increases, the A\(_{1g}\) peak blueshifts and the E\(_{2g}\) peak redshifts. The redshifting and blueshifting of the peaks indicates a loosening and tightening of the bonds between atoms, respectively. These layer-dependent shifts in the Raman peaks indicate that the stacking of the flakes impacts the vibrational modes of MoS\(_2\) in different ways. Adding more layers to the flake suppresses the A\(_{1g}\) bond, but causes the E\(_{2g}\) peak to loosen. This effect is consistent with other flakes, such as the flake seen in Fig. 13 [24]. Photoluminescence intensity is also used as a method of TMD characterization. The intensity of the 1.9 eV peak seen in Figure 16 decreases by a factor of 10\(^4\) from monolayer to bulk MoS\(_2\). While these layer-dependent shifts in the attributes of TMDs can be undesirable, there has been research into using the differing band gaps of variably layered MoS\(_2\) samples for increased responsivity to different wavelengths of light. For example, triple-layer MoS\(_2\) has a band gap of 1.35 eV, which makes the sample suited to detecting red light. In contrast, monolayer MoS\(_2\)’s 1.9 eV band gap makes the sample better suited for detection of ultraviolet light. Of course, these few-layer films have reduced photoluminescence,
charge carrier mobility, and lower ON/OFF ratios, but the increased responsivity to specific frequencies of light increases optoelectronic versatility, in spite of any drops in performance [19].

Before these two-dimensional crystals can be introduced to electronics, methods of mass production must first be identified. The dimensionality of the crystals presents significant challenges, as the desired properties of monolayers diminish significantly as the number of layers increase. Mechanical exfoliation of atomic layers from bulk crystals is typically the method used by researchers to produce single active components for testing. This method is not suited for mass production due to the impossibility of exfoliating and depositing the billions of flakes needed for the transistors needed in today’s electronics. Chemical vapor deposition has been considered a much more promising method of producing large sheets or many flakes of monolayer TMD crystals on a substrate [25].

**CHEMICAL VAPOR DEPOSITION**

The process of chemical vapor deposition has its roots in nineteenth century research. In 1895, a researcher by the name of Wöhler first utilized WCl$_6$ and hydrogen carrier gas to deposit a layer of tungsten metal [26]. In a manner similar to photolithography, this process was then adapted then utilized by the semiconductor industry depositing thin films of materials such as polysilicon, silicon dioxide, or silicon...
nitride [1]. While there are many variants, the basic process in the context of semiconductor production has stayed the same: a solid substrate is placed in a heated or evacuated chamber which then has a volatile gas precursor pumped into it, the gas condenses onto the much cooler substrate, which then cools to produce a film on the surface of the substrate. This process is outlined in Figure 17.

Most chemical vapor deposition processes are endothermic; they require an activation energy. This activation energy can be supplied in many different ways, allowing for a number of variants of the basic process. The most common and accessible method for many is traditional heating via thermal radiation via a furnace, direct heating of the substrate holder, etc. [26].

Reaction chambers can be classified as hot-wall or cold-wall. Hot-wall CVD reactions take place in furnaces heated via electric resistance, heating the entire chamber. These processes provide an environment conducive to deposition throughout the chamber, resulting in the entire inside of the chamber also being deposited. Cold-wall reaction chambers typically only heat the substrate locally via inductive heating, the surrounding gas in the chamber is relatively cooler. This method is useful in the fact that the precursors that condense on the cold walls will not be heated in subsequent growths, and will therefore not contribute to deposition on the substrate [27].
However, simply heating the chamber or substrate may not be the best choice when working with certain metals. For example, if a substrate has had aluminum (which has a melting point of about 600 °C) deposited on it, it will need to be coated with another metal to prevent corrosion. One choice would be to coat the substrate with silicon dioxide at a chamber temperature of 400 °C. Silicon nitride, on the other hand, is more effective at passivating, but requires a chamber temperature of 900 °C using conventional methods. To produce a more robust circuit, another method of energy input must be used. This particular problem can be solved by utilizing plasma. Using the highly reactive and energetic charged particles in the plasma to deposit the film, deposition of silicon nitride could be achieved when the substrate was at a temperature of 350 °C [28].

While energy input for CVD can be supplied in many ways, the pressure inside of the chamber can also be varied. Pressure can vary from no vacuum used: the pressure inside is “atmospheric”, to high vacuum systems with an internal pressure on the order of $10^{-5}$ Torr. Setups at atmospheric pressure are typically the simplest and cheapest to use, but tend to deposit less uniform films with more impurities than the films grown in vacuum [27]. The aforementioned example of passivating circuits via deposition of silicon dioxide usually happens at atmospheric pressure in a cold-wall reactor whereas the doped silicon deposited for semiconductors are typically deposited in a hot-wall system at pressures around 1 Torr [27].

Given CVD’s long history of depositing thin films for the semiconductor industry, it seems only fitting that the technique is useful in the proposed next generation of semiconductor production. In the context of producing MoS$_2$ films via chemical vapor deposition, a two-step chemical reaction must take place, the molybdenum trioxide
(MoO₃) precursor must first be reduced, then sulfurized. The heat of the furnace is meant to not only vaporize the solid MoO₃, but also to help reduce the MoO₃ to MoO₂. When exposed to temperatures of 600 °C and 730 °C for one hour, Spevack and McIntyre found only MoO₃ and MoO₂ left in their samples, indicating that these temperatures are suitable for fully reducing MoO₃ past any intermediate reduced compounds [29]. Sulfur will also act as a reducing agent in these growths. Once reduced and in vapor form, the suboxide MoO₂ will be transported to the substrate via the carrier gas. Introduction of additional sulfur at this stage increases the rate at which the suboxide sulfurizes [30].

Lee, Y. H., et al., among other researchers, have used CVD to deposit atomically thin flakes of transition-metal dichalcogenides on a silicon substrate coated with reduced graphene oxide using a traditional form of CVD that included two specific powders: molybdenum trioxide (MoO₃) and sulfur. In his method, a silicon or silicon dioxide substrate was mounted on top of a boat containing 0.4 grams of MoO₃ powder. Placed on another boat in the chamber was 0.8 grams of sulfur powder. A flow of nitrogen was introduced, and the furnace was heated to 650 °C. At this temperature, the sulfur powder has vaporized, and the MoO₃ has reduced to a suboxide film that further reacts with the sulfur powder to spread out as a thin layer of MoS₂. Lee and his co-authors contend that their technique is consistent and reproducible when using their experimental conditions. They also note that this same technique can be adapted to produce other transition-metal-
sulfide two-dimensional films. Techniques similar to Lee’s have been adopted due to the relative ease of use in comparison to the alternative: mechanical exfoliation [25].

However, there are drawbacks to using CVD to grow monolayer TMD flakes. CVD-grown monolayer flakes have been shown to have a charge carrier mobility an order of magnitude lower than mechanically-exfoliated flakes. Significant research will need to be conducted to resolve this ten-fold decrease in electron-hole momentum, as well as other similar problems [4].

By itself, chemical vapor deposition functions as a process that can synthesize monolayer TMD crystals and/or films. However, the synthesis of these crystals is the means to an end. For the films to be used as active components, they must be further processed via photolithography to produce integrated circuits. The unpredictable location and thickness of the crystals produced via chemical vapor deposition on a blank substrate limits its use in industrial processes that rely on rapid and repeatable results. As mentioned before, there are many ways to augment standard chemical vapor deposition processes to better suit one’s needs. Other researchers have noticed CVD-grown MoS_2’s tendency to grow around topological features on the substrate, such as debris or scratches. Researchers have used many different approaches when preparing seeded TMD growth. Lee, Y. H., et al., the researchers who used the previously described method, spun reduced graphene oxide on their substrate prior to growth. They found that in highly concentrated seeding areas, this method has
produced films on the order of 2 mm. There are also protocols in which a thin layer (a height on the order of a few nanometers) of metal is deposited on the substrate before growing. During the growth, the metallic layer is consumed and a film of MoS$_2$ is left behind [31]. A similar process is also used with thicker patterns about ten times the height. With a thicker pattern, the deposited metal will not be completely consumed during the growth process, instead the monolayer film will grow off the remaining pattern [32]. These two techniques both produce films that are grown in desired locations as well as being much larger than the individual flakes grown on a blank substrate, showing much more potential for scalability than the conventional deposition process on a blank substrate.

The results found in Najmaei, S., et al. seen in Figure 19 show the successful growth of joined, large scale MoS$_2$ film off an array of SiO$_2$ pillars. The synthesis method put forward in Khadka, S., et al. and continued in the accompanying manuscript is based off this idea of seeding TMD growth via bulk metallic patterns. However, instead of using an electrically insulating material such as SiO$_2$, we use the corresponding transition metal (molybdenum in this case) of the TMD. This allows us to produce devices with no need for additional photolithography post-growth, reducing the chance of contamination or damage to the grown TMD. Given the maturity of photolithography as an industrial process, an optimized version of our method combined with adjusted mask designs seems like it could be a valid path to mass production [33].

**METHOD DEVELOPMENT**

As is the case with most research, the first incarnation of any experimental method is typically not the most optimal. The CVD method described in the
accompanying manuscript has been heavily augmented since its inception. In the manuscript, the reactants in our experimental setup are in three separate locations; the substrate (facing upwards), MoO₃ powder, and sulfur powder all have specific locations in each section of the tube. However, in the earlier paper by Khadka, et al., the reactants are arranged into two separate zones: the substrate is laid face down on the MoO₃ powder in the center of the furnace, with the sulfur powder further upstream. This process was used by both Sudiksha Khadka and Shrouq Aleithan prior to my involvement. Placing both the substrate and oxide powder in the center of the furnace limited the maximum temperature that the furnace could be raised to, as the metal patterns tend to sulfurize more quickly at higher temperatures. Additionally, removing physical contact between the oxide powder and substrate removed the bulk growth that often surrounded the point of contact between the two, quieting any concerns that the location of the contact point might influence the uniformity or location of growth on the substrate. The methodology of the three-zone method was first introduced by Shrouq Aleithan in the group. Further optimization of the three-zone growth process was also performed by both her and myself. We will also be making improvements to the growth process such as introducing pressure regulators and mass flow controllers to our setup to keep the argon flow more consistent.

The photolithographic procedure we are performing is relatively basic in comparison to more industrialized processes described earlier. We are performing simple contact lithography with a chrome-on-glass (soda-lime) mask. The resist is a negative AZ 5214e photoresist spin coated on to SiO₂ substrate at a thickness of approximately 1.6 µm. Length of exposure, heating and development processes depend on the freshness of
the resist used. The research group’s method of performing photolithography has, as of late, needed no further optimization, other than occasional process tweaks to contend with post-expiration date resist. The method was initially developed by Helen Cothrel, then later optimized by myself to achieve a high percentage of yield.

Sudiksha and Shrouq are currently working towards the identification of the contact properties of our as-grown devices. We believe that, since the films are seeded off the metallic contacts as opposed to being deposited on top of the film, there is a likelihood of ohmic or ohmic-like contact between metal and semiconductor. We are currently working through complications in the process, so we will not make any conclusions about the nature of the contacts of our as-grown devices.

CONCLUSION

The ever-present goal of increased miniaturization of the integrated circuit has resulted in constant innovations in photolithography that reduced feature size from several micrometers to the current commercial limit of 14 nanometers [18]. Innovations in photolithography include the utilization of various optical properties such as destructive interference in the use of phase shift masks, or taking advantage of the higher refractive index of water in immersion lithography. Chemical vapor deposition has been used has been used in numerous semiconductor fabrication processes as a thin film deposition technique, and has also proved to have continuing use in as a potential method of production of two-dimensional TMDs, an atomically thin class of materials that have shown promise in next-generation semiconductors. TMDs like MoS$_2$, for example, not only perform well as semiconductors with a high ON/OFF ratio of $10^8$ and charge carrier mobility up to 200 cm$^2$ V$^{-1}$ s$^{-1}$, but monolayer samples of MoS$_2$ have a direct band gap,
allowing for the absorption and emission of photons, making them useful in optoelectronics such as photodetectors or photovoltaic cells [4]. However, as cheap as the mechanical exfoliation of bulk MoS₂ is, it does not seem to be a scalable method of monolayer synthesis. Numerous studies have grown films of monolayer TMDs via chemical vapor deposition at a higher rate of consistency and larger scale than mechanical exfoliation. Certain studies have made note of the preferential growth of TMD growth off topological features, allowing for preferential growth of monolayer films [32]. In the accompanying manuscript, we have introduced a method of seeding growth off MoS₂ off bulk molybdenum to create as-grown devices with the intention of developing a scalable and more efficient method of monolayer MoS₂ circuit production. While we have not finalized the method of growth, we have created functioning devices with this method of growth and are in the midst of testing and characterizing grown devices.
REFERENCES


2. *Intel launches first Broadwell Processors, CPU-World (2014)*


17. Intel to extend immersion to 11 nm, EETimes (2010).

18. Intel ISSCC: 14nm all figured out, 10nm is on track, Moore’s Law still alive and kicking, WCCFtech (2015).


26. A.C. Jones and M.L. Hitchman, Overview of Chemical Vapor Deposition, (Royal Society of Chemistry, 2009)


