Injection Locked Synchronous Oscillators (SOs) and Reference Injected Phase-Locked Loops (PLL-RIs)

Dissertation

Presented in Partial Fulfillment of the Requirements for the Degree Doctor of Philosophy in the Graduate School of The Ohio State University

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2017

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Abstract

Synchronization plays an important and fundamental role as the timing basis in digital, analog, and RF integrated circuits (ICs), where Phase-Locked Loops (PLLs) find their versatile applications. The noise sources in a traditional PLL are mainly divided into two groups: noise before the low-pass loop filter such as the noise in the reference signal, Frequency Divider (FD), Phase Frequency Detector/Charge Pump (PFD/CP); and noise after the filter such as the Voltage Controlled Oscillator (VCO) noise and the loop filter noise. The output phase noise of the PLL is the combined contribution from these two equally important in-band and out-band noise sources. This research studies the effect of the synchronization in the PLL on the decoupling of the 3dB bandwidths for different noise sources to achieve an optimum phase noise and improved locking behavior with an attenuated reference signal injection (RI) into a ring-type delay-line Voltage Controlled Synchronous Oscillator (VCSO).

This dissertation begins with the development of a generalized phase model for both LC-type and ring-type VCSOs. Next, the relationship between the device baseband noise (flicker and thermal noise) and a ring-type oscillator’s phase noise is derived. In addition, noise shaping functions are introduced to describe signal injection into the VCSO to achieve suppression of the oscillator in-band phase noise. Then, the transient and steady-state behavior of a Charge-Pump PLL-RI are explained with nonlinear differential equations and the phase-plane method. The nonlinear
phase equation is linearized for the small-signal condition and the s-domain noise transfer functions as well as noise bandwidths are derived for different noise sources in the major components of the PLL-RI. The effect of the loop parameters and the injection strength on the output phase noise, loop settling time, and lock in range is analyzed. The analysis is verified by the SPICE simulation and experimental results from a Charge-Pump PLL-RI using a 1GHz VCSO in GlobalFoundries 130nm standard CMOS technology.

The designed VCSO occupies a core area of 0.005 mm$^2$, and operates from 0.5GHz to 1.7GHz. The PLL-RI, for first-harmonic locking applications, has a core area of 0.02 mm$^2$ and consumes 2.6mW power. When a 30dB attenuation is applied, phase noise at 1MHz and 10MHz offset are reduced from -118.8dBc/Hz (PLL) to -121.9dBc/Hz (PLL-RI), and -102.3dBc/Hz (PLL) to -128.3dBc/Hz (PLL-RI), respectively, with an integrated RMS jitter from 10KHz to 30MHz of 1.55ps. Finally, another application of the PLL-RI as an integer-N frequency synthesizer is studied and tested. The PLL-RI based frequency synthesizer with the ring-type VCSO achieves comparable noise performance with LC type PLLs, but uses a much smaller chip area and features lower power consumption.

To summarize, this dissertation has thoroughly evaluated an oscillator and a PLL under small signal injection. Compared with the traditional PLL, the all-CMOS PLL-RI offers faster settling time, wider lock in range, and ability to decouple 3dB bandwidths for different noise sources to achieve an optimum noise performance. The applications of PLL-RIs can be extended to analog, digital, and RF systems for different timing schemes.
To my parents, Zhenya Lei and Chunhua Liu,

my husband, Hao Ying,

and my daughter, Avery Lei Ying
Acknowledgments

During my graduate study and research at the Ohio State University, I have been so lucky and blessed to meet and collaborate with so many people who are helpful and supportive. It would have been impossible for me to complete this work if I had not received these support and encouragement. They deserve my warmest gratitude and thankfulness. In particular, I would like to thank the following people:

• My advisor and mentor, professor Marvin H. White, who deserves my deepest gratitude. I thank him for introducing and inspiring me to this interesting research. I thank him for his wisdom, guidance, encouragement, and endless support on both my research and my personal life. It has been an honor, a privilege and a pleasure for me to work with him and to learn from him. I have benefited tremendously from his profound knowledge in semiconductors, electronics, and mathematics, his insight into the future technology, and his never-ceasing energy and enthusiasm in the research and teaching. The invaluable discussions and talks with him have deeply made and will continue to make an impact in my life. I will miss the wonderful evenings when he and Mrs. White invited my family to dinner at his house.

• Professor Waleed Khalil, for his precious time serving on my candidacy exam and final exam committees, and providing valuable advices on my research and dissertation. I would like to thank him and his group for providing on-chip test system and RF measurement equipment at OSU ElectroScience Laboratory. I would also like to extend my appreciation to him for the valuable courses I took with him.
• Professor Steven Bibyk, for taking time serving on my candidacy and final exam committees, and providing me with constructive comments. I am also very grateful for his help when I was his TA. He made my first teaching experience unforgeable.

• Professor Mohammed Ismail Elnaggar, for introducing me to the world of integrated circuits. The one-year life and research experience under his guidance and support at Khalifa University in United Arab Emirate is fruitful and memorable.

• Professor Jin-Fa Lee, my Master’s advisor, for teaching me the importance of mathematics and a passionate attitude in the science study.

• NSF ECCS Division, for the continued funding support for my research.

• Ms. Tricia Toothman for her heart-warming encouragement and administrative assistance throughout my graduate study.

• My colleagues and friends at OSU and previous schools for their help and friendship: Vivek Sriram, Hyram Liang, Dr. Salma Elabd, Shahriar Rashid, Dr. Jue Wang, Cagdas Gunes, Ramy Tantawy, Hao Yang, Dr. Lixia Yang, Dr. Jiangong Wei, Liang Yue, Dr. Zhen Peng, Dr. Xiaochuan Wang, Yuanhong Zhao, Xin Chen, Yangjing Wang, Shanshan Xu, Jin Li, and many more others.

• My entire family, especially my parents Zhenya Lei and Chunhua Liu for their unconditional support throughout my life. “The higher you stand, the further you see” is the idea behind their education on me. I am forever grateful to them. I am also grateful to my parents-in-law who treat me like their own daughter. I want to thank Hao Ying, my dear husband and best friend, for always being with me, patiently and supportively. Finally, I want to thank my beloved daughter Avery Lei Ying, whose lovely face colors my life. This dissertation is dedicated to them.

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### Fields of Study

Major Field: Electrical and Computer Engineering
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Chapter 1: Introduction

1.1 Research Motivation

The invention of the first transistor in the year 1947 [1] is the starting point of the upcoming huge revolution in electronics. More than one decade later, the introductions of the first integrated circuit (IC) [2] and CMOS devices [3] have revolutionized the semiconductor industry and the world of electronics. Computers, mobile phones, and other electronics are now inextricable parts of the structure of modern societies, made possible by the small size and low cost of CMOS ICs. In 1965, Gordon Moore, the co-founder of Intel Corp., noted that the number of transistors on a chip doubled every 18 to 24 months [4]. Shown in Figure 1.1, in the next about half a century, this so-called “Moore’s Law” came to be widely accepted as an evolving target for the industry. In over forty years, IC technology has evolved from producing simple chips with only a few transistors, to complex microprocessors comprising more than one billion transistors. Figure 1.2 shows the first Intel microprocessor 4004 which was created in 1971 with 2300 transistors to form a 4-bit adder, an accumulator, and 16 registers clocked at a frequency of 108KHz in 10µm CMOS process, and the recent Intel Quad-core Skylake in 2015 which contains 1.7 billion transistors and clocked at a frequency of 4.2GHz in 14nm Tri-Gate CMOS process. The technology scaling will
Figure 1.1: Technology scaling in industry following Moore’s Law [5]

Figure 1.2: Intel (a) 4004 in 10-um CMOS process (1971) (b) Skylake in 14-nm Tri-Gate CMOS process (2015)
continue at least in the next 5 years with gate lengths approaching sub-10nm and may reach saturation at some point in the future. The aggressive technology scaling on one hand has great impact on increasing integration density, speed, and performance of the ICs; however, on the other hand, creates new design challenges in the implementation of integrated high-speed communication systems which operate at gigabits per second rate, such as to minimize the cost and decrease power consumption while maintaining the speed and bit error rate (BER) of the system. The performance metrics is directly related to the timing scheme of the system. All modern communication systems require a stable periodic signal to provide the timing basis for functions such as sampling clock in analog data converters; clock synchronization, clock and data recovery, clock multiplication and division in high speed digital I/Os; and frequency synthesis in local oscillator (LO) for RF applications.

Synchronous clocking circuits, with their primary impact on modern practical computing systems, have been a significant contributor to the overall advancement of communication technologies. It is typical in synchronous circuits to use a reference clock signal in a feedback control loop to stabilize both frequency and phase, resulting in a phase-locked loop (PLL) architecture. Due to the rapid growth of the CMOS technology, high-frequency, high-speed, low-noise and low-cost PLLs have become crucial elements in a variety of communication applications, such as clock synchronization, skew cancellation, duty cycle correction, clock and data recovery, clock generation, frequency/phase modulation and demodulation, frequency synthesis, etc. Timing uncertainty impacts the performance of all these applications. Any timing jitter in PLLs significantly degrades the performance of the systems, especially when the operating frequency increases. Jitter is due to both intrinsic random device...
noise (Random Jitter RJ) such as thermal noise and low frequency noise (LFN), and deterministic noise (Deterministic Jitter DJ) such as supply/substrate noise.

For a typical PLL, the input reference noise, Phase Detector (PD) noise, and Frequency Divider (FD) noise are shaped by low pass transfer functions, and the Voltage Controlled Oscillator (VCO) noise and Loop Filter (LF) noise are shaped by high pass transfer functions when they are presented at the output, so generally speaking, an optimal noise performance can be obtained by proper selecting the loop bandwidth. However, as the VCO frequency increases, its noise begins to dominate and becomes more difficult to suppress. [6] showed that when the VCO frequency is raised up by a factor of N, the PLL loop bandwidth has to increase by a factor of $N^2$ for them to contribute the same jitter performance to the PLLs. To quantify this issue, we assume the PLL migrates from one standard to another which runs $N$ times faster ($\omega_{o2}/\omega_{o1} = N$), and the two VCOs inside the PLLs have identical quality factor $Q$. A simple Leeson’s phase noise model gives the oscillator output phase noise $L$ at an offset frequency ($\Delta \omega_{os}$) [7]:

$$L(\Delta \omega_{os}) = 10 \log \frac{|N_{out}|^2_{phase}}{P_{sig}} = 10 \log \left( \frac{|N_{in}|^2}{2P_{sig}} \frac{1}{4Q^2} \left( \frac{\omega_o}{\Delta \omega_{os}} \right)^2 \right)$$  \hspace{1cm} (1.1)

where $N_{in}$, $P_{sig}$, $Q$ and $\omega_o$ are the input noise voltage, signal power, resonator quality factor, and the oscillator free running frequency, respectively. Therefore, in the above example, according to Leeson’s model, the phase noises of the two VCOs are separated by $20 \log N$ dB. On the other hand, the RMS phase jitter is given by integrating the phase noise [8]:

$$J_{rms}^2 \text{ (phase)} = 2 \left( \frac{1}{2\pi f_o} \right)^2 \int_0^\infty 10 \frac{\pi}{f} df$$  \hspace{1cm} (1.2)
Normalizing it to one clock period:

\[ J_{\text{rms}}^2 \text{ (normalize)} = 2 \int_0^\infty 10^{L_{\text{rms}}} df \] (1.3)

Therefore, in order for the two VCOs to contribute the same jitter performance, i.e. the same normalized jitter, since VCO noise is high pass filtered, we need to have

\[ 10^{L_{\text{1}}}BW_1 = 10^{L_{\text{2}}}BW_2 \] (1.4)

Combining Equations (1.1) and (1.4), we obtain

\[ \frac{BW_1}{BW_2} = N^2 \] (1.5)

Of course we could use a wider bandwidth to suppress more VCO noise; however, some applications require a narrow loop bandwidth [9]. Moreover, loop stability may be affected and more low pass filtered noise such as PD noise and input noise will be included. This is especially a challenge in today’s nano-scaled processes where the LFN, which arises from the random capture and release of electrons by traps located in and near the gate dielectric, is of concern, especially in high-K dielectrics with large number of traps [10]. LFN in the device baseband affects the oscillating frequency and dominates the measured phase noise up to an offset of 1MHz [8]. If we consider these challenges, then new methodologies are needed to overcome these limitations. The driving force in almost all PLLs is an oscillator, therefore, a good understanding of oscillation-based phenomena, such as the injection locking – which is a very useful and interesting phenomenon that happens in numerous physical systems especially in electronic oscillators, and relatively new in the context of on-chip applications – can be helpful in solving these problems.
1.2 Injection Locked Oscillators

Injection locking is also known as frequency entrainment or synchronization, and it can be observed in our lives. For example, the pendulums of two clocks on the same wall will move in unison if they are hung close to each other [11]. Another example we can observe is that in summer, as night falls, the fireflies are sensitive to one another’s behavior. After some time all fireflies within a certain area like on the same tree begin to flash simultaneously in a burst. In electronics, injection pulling and locking also play very important roles. The injection locking technique, characterized by its simple structure and low noise performance in an oscillator design, has been investigated by researchers. By comparing the oscillator with a high stability reference signal source, injection locking will cause the oscillator to be phase locked to the reference source. Van Der Pol [12] in 1934 first introduced the injection of an external signal to an oscillator to control its frequency; however, the signal level was large and tended to ‘quench’ the output amplitude. Adler [13] in 1946 developed a small signal model for the tracking and non-tracking characteristics of the injection locking phenomena where signal injection was at low levels to modulate the phase, but not to ‘quench’ the amplitude of the oscillator output. Adler’s work provided a strong foundation for the subsequent work on injection-locked oscillators [14–17]. In particular, Armand [14] in 1969 provided the spectrum of a driven but unlocked injection locked oscillator. Runge [15] in 1976 developed a reference injected (RI), discrete component, PLL with an analog multiplier PD and LC oscillator for use in Undersea Lightwave Systems, which have been in use since 1988 in the Atlantic Ocean and 1989 in the Pacific Ocean. Uzunoglu and White [16] in late 1980s studied the low-level operation of a Synchronous Oscillator (SO). Owing to these pioneering works,
injection-locked oscillators opened the applications of amplifiers [18–20], frequency dividers [21], clock multipliers [22], quadrature signal generators [23, 24], coherent phase-locked synchronous oscillators (CPSOs) [17,25], clock recovering [26], frequency demodulators [27–29], self-oscillating mixers [30], optical injection locking loops [31, 32], RF spectrum sensors [33], etc. This research has the root of Runge’s method of reference injecting the PLL, and explored the full potential of his method to improve the noise and settling performance of Charge-Pump PLLs in an integrated CMOS circuit technology.

However, unlike injection locking which is sometimes deliberately used in oscillators, injection pulling is most of time unwanted. For example, as is shown in Figure 1.3 [11], in the broadband transceiver, the two oscillators in the transmitter an receiver may pull each other as a result of coupling through the substrate. Similarly,
the high swing broadband data at the output of the transmitter may pull bother oscil-
cillators as it contains substantial energy in the vicinity of their oscillation frequency.
Another example of undesirable pulling is that the Power Amplifier (PA) output in
an RF transceiver contains large spectral components in the vicinity of local oscillator
frequency. Leaking through the package and the substrate to the VCO is troublesome
and will cause pulling.

1.3 Low Frequency Noise (LFN) in MOSFET

In solid state devices, noise appears as current or voltage fluctuations, which can
arise from several sources. The inherent noise of electronic devices affects many as-
pects of electronic systems. For example, the signal-to-noise ratio (SNR) sets the
minimum detectable power of a communication system. In addition, noise gener-
ated in electronic devices greatly affects the performance of communication systems.
In oscillators, low frequency baseband device noise is up-converted to the high fre-
quency region as phase noise. In receivers, local oscillator phase noise introduces the
reciprocal mixing with the presence of a strong nearby interfere and also limits the
signal to noise ratio (SNR) for FM/PM signal; in transmitters, a substantial phase
noise will corrupt nearby receivers and also affects the bit error rate (BER) in a PSK
transmission system.

Generally speaking, the noise in MOSFET devices can be classified into two cat-
egories: thermal noise, and 1/f (flicker or low frequency) noise. Thermal noise is
created by random motion of charge carriers due to the thermal excitation. A sim-
ple thermal noise model for long channel MOSFET gives the mean-square value of
$\overline{i^2_{\text{thermal}}} = 4kT \frac{2}{3} g_m$  \hspace{1cm} (1.6)

1/f noise, also called low frequency noise (LFN), is the dominant noise in the
low frequency range and its current or voltage power spectral density (PSD) $S(f)$
is inversely proportional to the measurement frequency with a constant $f^{A_f}$, where
$A_f$ is approximately equal to 1, as is shown in Fig. 1.4(a). The origin of 1/f noise
has been studied over the years. This noise is usually associated with the randomly
trapping and releasing of charge carriers by the extra energy states at the gate oxide
and silicon substrate interface due to the imperfection of a fabrication process [34,36].
The simplest way to obtain 1/f characteristics is to superpose many different spectra
of generation recombination noise, where free carriers are randomly trapped and
released by centers with different life times. In circuit design, the historical method
of treating this noise is to refer the MOSFET drain current noise PSD, back to the input voltage PSD in series with the gate electrode by dividing it with \( g_m^2 \) where \( g_m \) is the transconductance of the MOSFET:

\[
\frac{v^2_{ng}}{\Delta f \mid 1/f} = \frac{K_f}{fA_f} \frac{1}{WLC_{ox}^2}
\]

(1.7)

where \( K_f \) and \( A_f \) are fitting parameters [37]. Surface channel MOSFETs show a large noise at low frequencies, which makes the study of LFN very important [38]. Also, LFN is increasing with the reduction of device dimensions and as such is becoming a real problem for devices fabricated in nanoscale. Combine the LFN PSD with the thermal noise PSD, the LFN noise corner frequency \( f_{cor} \) can be found, as shown in Figure 1.4(a). For the \( f < f_{cor} \), the LFN of drain current is the dominant component; and for \( f > f_{cor} \), the thermal noise of the drain current is prevailing. The typical values of \( f_{cor} \) in MOSFETs could be even larger than 10MHz [36]. Therefore, LFN is a very critical noise source for circuit design. Mixer LFN degrades signal-to-noise ratio (SNR), and as a consequence the overall noise figure of the receiver suffers. It is also an important electrical feature of scaled MOSFETs as it affects the front-end noise performance of RF low-noise amplifiers (LNAs) and spectral purity of RF oscillators, which impacts the phase noise and bit-error rate (BER) performance. In addition, 1/f noise affects LNAs at baseband, such as pre-amplifiers for sensor-based electronics like solid-state imagers and bioelectronics. Fig. 1.4(b) illustrates measurements [35] of a high-K NMOS device displaying a low-frequency, 1/f type noise spectrum in these devices. Although high-K films are thin and the existing high trap density does not drastically perturb the device threshold voltage, the presence of these traps influences the noise behavior of the scaled MOSFETs. In addition to the emission and capture of
inversion layer carriers by traps in the interracial region, there are also considerations
for trap occupancy due to the fluctuations in carrier density and mobility [38–40].

1.4 Scope of the Dissertation

This dissertation is composed of five chapters, and is organized as follows:

- Chapter 1 gives the motivation and a brief overview of the related research.

- Chapter 2 presents a detailed analysis on the injection locked synchronous oscil-
  lators (SOs) with a focus on the system dynamics and phase noise.

- Chapter 3 characterizes the device used in the circuit design, and presents meth-
  ods to up-convert device baseband noise to oscillator high frequency phase noise.

- Chapter 4 presents the idea of Reference Injection Locked Phase-Locked Loops
  (PLL-RIs). The functionality and components of the proposed PLL-RI are
described.

- Chapter 5 concludes this dissertation and provides suggestions for future work.

In addition, the detailed derivation of the system dynamic for an astable multi-
vibrator based discrete-type SO is included in Appendix A. Appendix B documents
the chip description and measurement operations presented in Chapters 2, 3 and 4.
Relationship between timing jitter and phase noise is given in Appendix C. Finally,
Appendix D summarizes the Fourier components of a pulse waveform.
Chapter 2: Injection Locked Synchronous Oscillators (SOs)

The injection locking technique, characterized by its simple structure and low noise performance in an oscillator design, has been investigated by many researchers. By comparing the oscillator with a high stability reference signal source, injection locking will cause the oscillator to be phase locked to the reference source. Van Der Pol [12] in 1934 first introduced the injection of an external signal to an oscillator to control its frequency; however, the signal level was large and tended to ‘quench’ the output amplitude. In 1946, Adler [13] developed a small signal model for the tracking and non-tracking characteristics of the injection locking phenomena where signal injection was at low levels to only modulate the phase, but not to ‘quench’ the amplitude of the oscillator output. Adler’s work provided a strong foundation for the subsequent work on injection-locked oscillators [14–16,22]. In particular, Armond [14] in 1969 derived the spectrum of a driven but unlocked SO. Injection locking is used widely in injection-locked clock multipliers (ILCMs) to achieve superior phase noise over a Phase-Locked Loop (PLL) [22]. In 1976, Runge [15] developed a reference injected (RI), discrete component, PLL for use in Undersea Lightwave Systems. In the last few years, there have been many work in the literature on the injection locked oscillators. Razavi [11] reexamined injection puling and locking effect in oscillators; Lee [21] proposed injection locked frequency dividers. Although a great effort has
been made on characterizing the pulling and locking effect of the oscillators, what is missing, however, is to achieve a generalized locking equation and a generalized phase shaping equation for different types of on-chip oscillators such as LC-type and ring-type oscillators, and study the frequency response of the oscillator under injection.

In this chapter, we will first briefly go over the fundamentals in the oscillators, then give the classification of injection locked Synchronous Oscillators (SOs). Section 2.3 thoroughly studies the system dynamics of a SO and derives a generalized SO phase model for LC-type SOs, ring-type SOs, and discrete-type SOs. The phase noise is analyzed in the SO system. A ring-type SO with voltage control capability (VCSO) is implemented with 130nm CMOS technology, and tested to validate the theory. The same VCSO will be used in Chapter 4 to improve the performance of PLLs in the integrated CMOS circuit technology.

2.1 Oscillator Basics

An oscillator is an autonomous circuit that converts DC power into a periodic waveform. Usually the waveform is in the form of sinusoidal or square wave. It is a pretty exciting topic to study because it is different from the other types of circuits. An oscillator is “alive” in some ways since once the power is turned on, it starts.
to create a periodical signal on its own. There is no input signal, but there is an output, therefore an oscillator is a highly nonlinear circuit. Oscillator circuits entail a self-sustaining mechanism that allows their own noise to grow and eventually become oscillating signals. There are different views of oscillators. As we know, a feedback system under certain criteria has a potential to oscillate. Shown in Figure 2.1 is a simple linear feedback system, with an overall transfer function

\[
\frac{Y(s)}{X(s)} = \frac{H(s)}{1 - H(s)}
\]  

(2.1)

If the denominator is equal to 0, then a self sustaining mechanism will arise. In other words, if at some frequency, \(H(s)\) is equal to 1, then the closed loop gain will approach infinity at that particular frequency. To summarize, for the oscillation to begin, a loop gain of unity or greater is necessary, and there should be no phase shift. If we have a negative feedback, the phase shift needs to be equal to 180°. These two conditions (necessary but not sufficient) are called Barkhausen criteria for oscillation [34]:

\[
\begin{aligned}
|H(s)| &\geq 1 \\
\angle H(s) & = 0^\circ
\end{aligned}
\]  

(2.2)

The closed loop poles of the above system lie in the imaginary axis if \(H\) is equal to 1, and if \(H > 1\), the closed-loop poles become complex and lie in the right half plane. In practice, the poles will finally move to the imaginary axis because of the nonlinearity in the signal path. In on-chip circuit implementations, in order to ensure the oscillation in the presence of temperature and process variation, the loop gain should chosen to be more than 2-3 [34].

The above feedback model is known as the “two-port” model because the feedback loop is closed around a two-port network. Another perspective is the so called “one-port” model where the oscillator is treated as two one-port networks connected to
Figure 2.2: One-port model of oscillators

each other [41], as is shown in Figure 2.2. Suppose the resonator is a simple parallel RLC tank. The tank by itself cannot oscillate indefinitely because the stored energy is dissipated in the parallel resistor $R_p$ every cycle. In the steady state, the losses in the tank due to conductance $G_p = \frac{1}{R_p}$ are balanced by the power drawn from the active device through the negative conductance $-G_p$. The two models of Figure 2.1 and Figure 2.2 are equivalent most of the time. In CMOS technology, oscillators are typically implemented in two different types, known as “LC-type oscillators” with resonators and “delay-line ring-type oscillators” without resonators. Almost all of these oscillators can be explained by both one-port and two-port models. Normally we want to control the output frequency of the oscillator by a voltage signal, and thus, this type of oscillators is called Voltage Controlled Oscillators (VCO). In the following subsections, a brief overview of LC-type VCOs and Ring-type VCOs is presented.

2.1.1 LC-type VCO

The implementation of LC oscillators is based on the properties of RLC resonant circuits. The resonator is implemented by a parallel LC resonator shown in Figure 2.3(a). This LC resonator with parasitics can be transformed to a parallel RLC
Figure 2.3: LC resonator and its equivalent circuit

circuit as shown in Figure 2.3(b) with

\[
L_p \approx L_s \quad (2.3)
\]

\[
C_p \approx C_s \quad (2.4)
\]

\[
R_p \approx R_{L,s}Q_{L,s}^2/R_{C,s}Q_{C,s}^2 \quad (2.5)
\]

where we assume quality factors \( Q_{L,s} = \frac{\omega L_s}{R_{L,s}} \) and \( Q_{C,s} = \frac{1}{\omega R_{C,s}C_s} \) are much greater than 1. The frequency dependent equivalent impedance can then be found:

\[
Z_{in}(\omega) = \sqrt{\frac{\omega^2 R^2 L^2}{\omega^2 L^2 + R^2 (\omega^2 L C - 1)^2}} \quad (2.6)
\]

where we find when \( \omega_0 = \frac{1}{\sqrt{LC}} \), the impedance of the inductor and the capacitor cancels each other, so the resonator is pure resistive and the total phase shift is \( 0^\circ \).

According to the Barkhausen’s oscillation criteria, based on the two-port model, in order to have oscillation, this LC resonator should be involved in a feedback loop with an active circuitry to generate a total phase shift of \( 0^\circ \) and a gain larger than unity.

Most discrete RF LC oscillators incorporates only one active device to minimize the noise and the cost. As is mentioned earlier, at resonance, the tank offers no phase
shift. Thus, in order for the oscillator to achieve a total phase of zero, the feedback signal needs to return to the source of the transistor. If the drain voltage is directly applied at the source, the resistive loading of $\frac{1}{g_m}$ seen at the source dramatically reduces the Q of the tank, decreasing the loop gain to be below unity and preventing the oscillation. For this reason, the emitter impedance must be transformed to a higher value before it appears in parallel with the resonator. This common gate topology with impedance transformer is the basic idea in a number of oscillators, such as Colpitts Oscillators, Hartley oscillators, and Clapp Oscillators [41].

The one-port representation, which tells us the active circuitry needs to generate a negative resistance that cancels the parasitic resistance inside the resonator, is also valid to the above mentioned oscillator topologies, providing more insight into the behavior of the circuits [41]. Take the Colpitts oscillator, shown in Figure 2.4(a) as an example. Consider the one-port circuit shown in Figure 2.4(b), the impedance looking into the gate and drain can be found as [41]

$$Z_{in}(\omega) = -\frac{g_m}{\omega^2 C_1 C_2} + \frac{1}{j\omega C_1} + \frac{1}{j\omega C_2}$$  \hspace{1cm} (2.7)

which contains a negative real impedance of $-\frac{g_m}{\omega^2 C_1 C_2}$, indicating the circuit can oscillator if an inductor is placed between the drain and the gate [Figure 2.4(c)].

Another commonly used oscillator topology in IC technology is to put the RLC resonator circuit in Figure 2.3 as load for a common source amplifier and use two cascaded amplifiers inside a feedback loop to achieve a total 360° phase shift, as is shown in Figure 2.5(a). In such a circuit, choosing a proper voltage gain for the amplifiers guarantees the oscillation. This is the so called “Cross-Coupled LC Oscillator”, shown in Figure 2.5(b), where the cross-coupled transistors behave as a negative resistance and have $R_{m} = -\frac{2}{g_m}$. The condition for this circuit to oscillate is
we need to have net negative resistance which means $G_{\text{in}}$ needs to be larger than the tank parasitic conductance $G_p$, giving $|G_{\text{in}}| = \frac{g_m}{2} \geq G_p = \frac{1}{R_p}$. Typically, $\frac{g_m}{2}$ is set 2-3 times higher than $\frac{1}{R_p}$ to guarantee oscillation.

Since the oscillation frequency of LC oscillator is equal to $\omega_o = \frac{1}{\sqrt{LC}}$, suggesting that only the inductor and capacitor values can be varied to tune the frequency. Normally it is difficult to vary the value of monolithic inductors, therefore varactors are used to tune the oscillator frequency.

There are several types of varactors. A reverse-biased diode can serve as a varactor, but with a poor quality factor $Q$ and a narrow tuning frequency range [42]. Readily available in any CMOS process, the MOS transistor itself can serve as a varactor. With Drain, Source and Bulk (D, S, B) connected together, a P/N-MOS varactor has a capacitance value dependent on the gate-to-bulk voltage, but it has a narrow tuning range as well. If the transistor can be ensured not to enter the accumulation
Figure 2.5: Cross-Coupled LC Oscillator (a) two cascaded common source amplifiers (b) equivalent circuit of (a)

region for a wide range of gate voltage, an almost monotonic MOS varactor can be realized, and is called inversion-mode MOS, I-MOS [42] where the connection between D-S-B is removed, and B is connected to the highest/lowest DC voltage available in the circuit. A more attractive alternative is to use PMOS in the depletion and accumulation regions only and form an accumulation-mode MOS capacitor, A-MOS [42]. Figure 2.6 compares the tuning characteristics of the P/N-MOS with (a) I-MOS and (b) A-MOS, and A-MOS offers the highest voltage tuning range and quality factor Q, although sometimes its model is not supported by foundries.

LC-type VCOs have some other limitations: monolithically integrated high quality inductors are one of the most difficult elements in circuit design and require special processes; and the passive components used in the LC resonator take a large area. While with these disadvantages, LC-type VCO is still widely used in wireless communications, especially cellular applications for their stringent noise requirement.
Figure 2.6: Tuning characteristics of varactors (a) I-MOS and P/N-MOS (b) A-MOS and P/N-MOS [42]
2.1.2 Delay-line Ring-type VCO

The ring-type oscillator consists of a number of gain stages in a loop to provide enough loop gain and needed phase delay (shift), therefore, it is also called a delay-line oscillator. It is very compact and easy to integrate. Ring-type oscillators are one of the most widely manufactured circuits. Foundries use ring oscillators to monitor the production yield of wafers and automatically measure the oscillation frequency to decide which wafers are acceptable and which have to be discarded. Shown in Figure 2.7, a simple example of a delay-line ring-type oscillator has the delay stage as a single stage common-source amplifier, and odd number of delay stages ($N \geq 3$). Shown in Figure 2.8(a) and (b), a single or two-stage single-ended oscillator does not oscillate because it cannot provide a phase shift of 360° or equivalent 0°. Therefore, for a single-ended delay-line ring-type oscillator to oscillate, $N$ has to be an odd number and has to be equal to or greater than 3. Take $N = 3$ as an example, since all stages are identical, there are three same poles ($\omega_{p1} = \omega_{p2} = \omega_{p3} = \omega_p$) at the output.
of each stage. The total phase shift around the loop, $\phi$, equals to $-315^\circ$ at $\omega = \omega_p$ and $-450^\circ$ at $\omega = \infty$. Therefore, $\phi$ will reach $-360^\circ$ at some certain frequency which is less than infinity, where the loop gain can still be greater than or equal to unity.

The number $N$ of total delay stages and the delay time $t_d$ associated with each delay stage determine the oscillating frequency:

$$\omega_o = \frac{1}{2Nt_d} \tag{2.8}$$

Define the delay time as the time it takes the output to reach the 50% point in its transition gives

$$t_d = \frac{1}{2} C \int_0^{V_o} \frac{1}{I} dV = \frac{CV_o}{2I_{av}} \tag{2.9}$$

where we assume the output of each delay stage charges between 0 and $V_o$, and in each cycle, a constant current $I_{av}$ charges or discharges capacitor in each node. According
to Equation (2.8), the frequency tuning in ring-type oscillators can be achieved by adjusting $t_d$, which is controlled by the average current. Since the oscillator is tuned by a current instead of voltage, a ring-type oscillator usually has a wide tuning range.

### 2.1.3 Oscillator Phase Noise

Same as the other analog circuits, oscillators are susceptible to noise. Noise can influence both the frequency and the amplitude of the oscillator output signal, however, in most cases, the disturbance in the output amplitude is unimportant, and only the random deviation of the frequency is considered. The latter is known as the phase noise. There are many ways to understand the phase noise. We can think it as the period of the oscillation is not actually constant, and there is some jitter. In other words, the oscillation period changes in a random way. Another way to see the phase noise is to plot the power spectrum of the oscillator output. For a perfect oscillator, we can observe a delta function at the resonant frequency. All the energy concentrates on one frequency. However, for real oscillators, the spectrum exhibits phase noise “skirts” around the center frequency, as shown in Figure 2.9.
Phase noise is a very important concept in RF systems. Shown in Figure 2.10(a), in the transmitter path, a powerful nearby transmitter with substantial phase noise can corrupt the wanted signal by the phase noise tail of the transmitter. In the receiver path, a noisy Local Oscillator (LO) signal with substantial phase noise introduces the problem of reciprocal mixing: when the desired signal with a large nearby interferer mixed with the LO output, the down-converted band consists of two overlapping spectra, with the desired signal suffering from significant noise due to the tail of the interferer. Therefore, the output spectrum of the LO must be extremely sharp with a very low phase noise [41].

The inherent oscillator noise is in the oscillation signal path. Consider the feedback model in Figure 2.1, when noise $X(s)$ is applied into the oscillator, the noise transfer function is the same as the signal transfer function in Equation (2.1). For small $\Delta \omega$ near $\omega_o$, and $\omega = \omega_o + \Delta \omega$, according to Taylor expansion:

$$H(j\omega) = H(j\omega_o) + \Delta \omega \frac{dH(j\omega)}{d\omega} = 1 + \Delta \omega \frac{dH(j\omega)}{d\omega}$$  \hspace{1cm} (2.10)
Therefore, the closed loop noise transfer function can be found:

\[
\left| \frac{Y(j\omega)}{X(j\omega)} \right|^2 = \left| \frac{H(j\omega)}{1 - H(j\omega)} \right|^2 \approx \frac{1}{(\Delta\omega)^2} \left| \frac{dH(j\omega)}{d\omega} \right|^2
\]  

(2.11)

Writing \( H(j\omega) \) in the polar form, \( H(j\omega) = |H|e^{j\phi} \), we have

\[
\left| \frac{dH(j\omega)}{d\omega} \right|^2 = \left| \frac{d|H|}{d\omega} \right|^2 + |H|^2 \left| \frac{d\phi}{d\omega} \right|^2 \approx |H|^2 \left| \frac{d\phi}{d\omega} \right|^2
\]

(2.12)

since at resonance, the phase change is much higher than magnitude change. The open-loop quality factor \( Q \) is a measure of how much the closed-loop system opposes variation in the frequency of oscillation [41], and is defined as

\[
Q = \frac{\omega_o}{2} \left| \frac{d\phi(\omega)}{d\omega} \right| \bigg|_{\omega = \omega_o}
\]

(2.13)

Substitute Equations (2.12) and (2.13) to Equation (2.11), we have

\[
\left| \frac{Y(j\omega)}{X(j\omega)} \right|^2 = \frac{1}{4Q^2} \left( \frac{\omega_o}{\Delta\omega} \right)^2
\]

(2.14)

Note that \( |Y(j\omega)|^2 \) contains the effect of noise on both the amplitude and the phase of the carrier, and the noise on the phase is typically half of the value, giving that

\[
|N_{out}|_{\text{phase}}^2 = \frac{1}{2} |Y(j\omega)|^2 = \frac{1}{2} \frac{1}{4Q^2} \left( \frac{\omega_o}{\Delta\omega} \right)^2 |N_{in}|^2
\]

(2.15)

where \( |N_{in}|^2 = |X|^2 \) is the input noise power. Phase noise is defined as the single sideband noise power at a frequency offset \( \Delta\omega_{os} \) relative to carrier power with a measurement bandwidth of 1Hz [34]:

\[
L(\Delta\omega_{os}) = 10 \log \left( \frac{P_{SSB}(\omega_o + \Delta\omega_{os}, 2\pi)}{P_{sig}} \right) \text{ dBc/Hz}
\]

(2.16)

Substitute Equation (2.15) into (2.17), we can derive the Leeson’s Model [7], which is one of the earliest models for the phase noise of oscillators:

\[
L(\Delta\omega_{os}) = 10 \log \left( \frac{|N_{out}|_{\text{phase}}^2}{P_{sig}} \right) = 10 \log \left( \frac{|N_{in}|^2}{2P_{sig}} \frac{1}{4Q^2} \left( \frac{\omega_o}{\Delta\omega_{os}} \right)^2 \right)
\]

(2.17)
Equation (2.17) shows the dependence of the output phase noise on the oscillating frequency $\omega_o$, the quality factor $Q$, and the offset frequency $\Delta\omega_{os}$. Since we only consider the white noise, and make simplification assumptions, there are some differences between the spectrum predicted by Equation (2.17) and what one typically measures in practice. The dashed line in Figure 2.11 plots Equation (2.17), whereas the solid line plots the real world phase noise spectra which not only processes a region where the phase noise is proportional to $1/f^2$, but also the magnitude is typically larger because there are additional important noise sources besides the tank loss. For example, the energy restorer will be noisy, and the measured spectra eventually flattens out for a large frequency offset. This floor is due to the noise associated with any active elements placed between the tank and outside world, or even the limitations in the measurement instrumentation itself. Lastly, there is almost always a $1/f^3$ region at small offsets due to the flicker noise. This modified Leeson’s model gives [41]

$$L(\Delta\omega) = 10 \log \left[ \frac{F k T}{2 P_{sig}} \frac{1}{4 Q^2} \left( \frac{\omega_o}{\Delta\omega} \right)^2 \left( 1 + \frac{\omega_c}{\Delta\omega} \right) \right]$$  \hspace{1cm} (2.18)

where the factor of $F$ accounts for the increased noise in the $1/f^2$ region, an additive factor of unity accounts for the noise floor, and a multiplicative factor $\frac{\omega_c}{\Delta\omega}$ provides a $1/f^3$ behavior at small offset frequency. The model asserts that delta $\Delta\omega_{1/f^3}$, which is the boundary between the $1/f^3$ and $1/f^2$ regions, is precisely equal to the $1/f$ corner of device noise, but measurement show no such equality, people treat $1/f^3$ as an empirical fitting parameter as well [41].

2.1.4 LC-type VCO or Ring-type VCO

LC oscillators have extraordinary noise performance with low long-term and period jitter and low phase noise, but consume large layout areas and have narrow
tuning frequencies. On the other hand, for a given power budget, 1) the delay-line ring oscillator is easier to integrate due to its compactness; a large number of delay-line oscillators take up the same chip area as a small spiral inductor in the LC tank; also, high Q inductances are difficult to implement due to the series resistance. Q’s larger than 20 are difficult to achieve in integrated circuits. 2) the delay-line oscillator can oscillate at a very high frequency, and since it is tuned in frequency by a current, it has a broader tuning range than the LC oscillator. However, delay-line oscillators suffer from the well-known degradation phase noise performance because the Q value is poor since the energy stored in the node capacitances is discharged every cycle, and the energy is restored to the resonator during the edges rather than at the voltage maxima [43]. It has been shown in [44] that to achieve the same phase noise performance, the ring-type oscillator takes 450 times the current of the LC-type oscillator. Table 2.1 summarizes the comparison of LC-type VCOs and ring-type

![Figure 2.11: Modified Leeson’s phase noise model of an oscillator](image)
Table 2.1: Performance Comparison between LC and Ring-type VCOs

<table>
<thead>
<tr>
<th></th>
<th>Pros</th>
<th>Cons</th>
</tr>
</thead>
<tbody>
<tr>
<td>LC-type VCO</td>
<td>low jitter / phase noise</td>
<td>requires high-Q inductor</td>
</tr>
<tr>
<td></td>
<td></td>
<td>large chip area (inductor)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>limited tuning range</td>
</tr>
<tr>
<td></td>
<td></td>
<td>need start-up circuitry</td>
</tr>
<tr>
<td></td>
<td></td>
<td>need accurate varactor model</td>
</tr>
<tr>
<td>Ring-type VCO</td>
<td>small chip area</td>
<td>high phase noise</td>
</tr>
<tr>
<td></td>
<td>easy to integrate and model</td>
<td>high power for low jitter</td>
</tr>
<tr>
<td></td>
<td>wide tuning range</td>
<td>sensible to disturbance</td>
</tr>
<tr>
<td></td>
<td>multi-phase signal generation</td>
<td></td>
</tr>
<tr>
<td></td>
<td>easy to start up</td>
<td></td>
</tr>
</tbody>
</table>

VCOs. According to the table, if phase noise is of the most importance, then the LC-type VCO is the best choice; however, if the requirement of phase noise can be relaxed, then the ring-type VCO is better in almost every other aspect.

2.2 SO Classifications

Based upon the ratio of the injection frequency to the oscillator output frequency, the SO is classified into three types [21]: first-harmonic, sub-harmonic, and super-harmonic SOs. In a first-harmonic SO, the injection frequency is identical to the oscillator frequency, therefore, the applications are synchronous amplifiers, clock distribution, clock recovery, frequency modulation/demodulation, etc. In a sub-harmonic SO, the injection frequency is the sub-harmonic of the oscillator frequency, yielding the applications of frequency multipliers. In a super-harmonic SO, the injection frequency is a harmonic of oscillator frequency, so the application includes frequency dividers.
Figure 2.12 shows the block diagrams of sub-harmonic and super-harmonic SOs [45]. In the sub-harmonic SO, as shown in Figure 2.12(a), the injection signal $V_i$ at frequency $\omega_i$ is firstly processed by a non-linear block and generates frequency harmonics at $k\omega_i$. Assume that $\omega_i \ll \omega_o$, for some integer $N$, $N\omega_i$ lies inside the locking range $\omega_o \pm K_{SO}$, then the oscillator locks to the frequency at $k\omega_i$. We say it is sub-harmonic injection locked and it acts as a frequency synthesizer.

For different types of SOs, although the output frequencies are different ratios of the injection frequency, the concept behind them is the same, and needs to be explored in order to understand its behavior. In the following sections, unless otherwise noted, the SO refers to the first-harmonic injection locked oscillators, and its analysis can be easily applied to sub- and super- harmonic SOs.
2.3 SO System Dynamics

As is mentioned in the previous section, in on-chip applications, oscillators are typically implemented by LC tank oscillators or delay-line ring oscillators based on the required specification. The open loop transfer functions of LC oscillators and delay-line oscillators have different natures, therefore, we need to separately study their behaviors under signal injection.

2.3.1 LC-type SO

The concept of injection locking in the SOs with tank oscillators can be illustrated with a simple one-port model as shown in Figure 2.13. The circuit consists of a parallel reactive LC tank, tank parallel conductance $G_p$ and a nonlinear negative conductance $-G_A$ from the active circuit. $V_i$ represents the signal injected into the oscillator, and $g_m$ is the transconductance of the injection device. In the conventional oscillator model, the energy lost in $G_p$ is replenished by the active circuit $-G_A$ in every cycle, thus allowing the steady oscillation. However, in the SO, because the injection feeds energy into the oscillator, the effect of $-G_A$ is reduced, so that it no longer cancels out $G_p$, which results in a conductance residue $G_p - G_A$ in the SO model. The time
dependent differential equation of the output signal shown in Figure 2.13 is found by

\[
\frac{d^2 V_o(t)}{dt^2} + \frac{G_p - G_A}{C} \frac{dV_o(t)}{dt} + \omega_o^2 V_o(t) = \frac{g_m}{C} \frac{dV_i(t)}{dt}
\]  

(2.19)

where \(\omega_o = \frac{1}{\sqrt{LC}}\) is the free running oscillator frequency. Assuming signal solutions can be written as \(V_i = \bar{V_i} e^{j(\omega_i t + \phi_i)}\) and \(V_o = \bar{V_o} e^{j(\omega_o t + \phi_o(t))}\), and define \(\phi = \phi_o(t) - \phi_i\) as the instantaneous differential phase, and \(\Delta \omega = \omega_o - \omega_i\) as the frequency offset of the injected signal from the oscillator, (2.19) can be rewritten as

\[
j \frac{d^2 \phi}{dt^2} + j \frac{G_p - G_A}{C} \left( \omega_i + \frac{d\phi}{dt} \right) + \omega_o^2 - \left( \omega_i + \frac{d\phi}{dt} \right)^2 = j \omega_i \frac{g_m \bar{V_i}}{CV_o} (\cos \phi - j \sin \phi)
\]  

(2.20)

Separating and matching the real and imaginary parts in Equation (2.20) on both left and right hand sides, we have

real part: \(\omega_o^2 - \left( \omega_i + \frac{d\phi}{dt} \right)^2 = 2\omega_i K_{SO} \sin \phi\)  

(2.21)

imag part: \(\frac{d^2 \phi}{dt^2} + \frac{G_p - G_A}{C} \left( \omega_i + \frac{d\phi}{dt} \right) = 2\omega_i K_{SO} \cos \phi\)  

(2.22)

where \(K_{SO} = \frac{g_m \bar{V_i}}{2CV_o}\) is the SO injection parameter. We can reduce Equation (2.21) to the well known Adler’s equation [16] by assuming \(\omega_i \approx \omega_o\) and the variation of phase difference with time \(\frac{d\phi}{dt} \ll \omega_i\).  

\[
\frac{d\phi}{dt} = \Delta \omega - K_{SO} \sin \phi.
\]  

(2.23)

2.3.2 Delay-line Ring-type SO

For subsequent derivations of the system dynamics for a delay-line SO, we need an expression for the phase shift introduced by a delay-line in the vicinity of oscillation. Figure 2.14 shows a linearized model [44] of a N-stage delay-line oscillator where \(-G_m\) is the inverting transconductance, and \(R\) and \(C\) are the resistance and capacitance
at the output node of each delay component, respectively. The number of the delay stage \( N \) is an odd number for a single-end delay-line. The transfer function \( H_1 (s) \) of a single stage can be represented as

\[
H_1 (s) = \frac{-G_m R}{1 + sRC}
\]  

(2.24)

Therefore, the phase shift for a single delay stage \( \phi_1 (\omega) \) can be found as

\[
\phi_1 (\omega) = \tan^{-1} (-\omega RC) = -\tan^{-1} (\omega RC) + \pi
\]  

(2.25)

The total phase shift of the delay-line \( \phi_d (\omega) \) is

\[
\phi_d (\omega) = N \phi_1 (\omega) = -N \tan^{-1} (\omega RC) + N\pi
\]  

(2.26)

where \( N = 2K + 1 \) is an odd integer and \( K \) is a positive integer. According to the Barkhausen criteria, in order for the system to oscillate, the phase shift of the total delay stages should reach \( 2K\pi \), giving \(-N \tan^{-1} (\omega RC) = -\pi\), then we can find the oscillating frequency \( \omega_o \) as

\[
\omega_o = \frac{1}{RC} \tan \frac{\pi}{N}
\]  

(2.27)
Substitution of Equation (2.27) into (2.26), we have the principle angle of the phase shift in terms of the resonant frequency $\omega_o$ and the number of stages $N$:

$$\phi_d (\omega) = -N \tan^{-1} \left( \frac{\omega}{\omega_o} \tan \frac{\pi}{N} \right)$$  \hspace{1cm} (2.28)

The quality factor $Q$ of this oscillator is defined as $Q = \frac{\omega_o}{2} \left| \frac{d\phi(\omega)}{d\omega} \right|_{\omega=\omega_o}$ [41] to measure how much the closed-loop system opposes variations in the frequency of oscillation. Therefore, we take the derivative of $\phi_d (\omega)$ with respect to $\omega$ in Equation (2.28) to find

$$Q = \frac{\omega_o}{2} \left| \frac{d\phi(\omega)}{d\omega} \right|_{\omega=\omega_o} = \frac{\omega_o}{2} \times \frac{N}{\omega_o} \sin \frac{2\pi}{N} = \frac{N}{4} \sin \frac{2\pi}{N}$$ \hspace{1cm} (2.29)

Equation (2.29) shows that $Q$ cannot exceed $\frac{\pi}{2}$ for delay-line oscillators. Therefore, delay-line oscillators are considered to be low quality factor oscillators.

When the delay-line oscillator is injected with an external signal, the linearized model for the delay-line oscillator can be modified as the delay-line SO model shown in Figure 2.15, where $V_i$ and $V_o$ are the injected signal and output signal respectively. We define $V_x$ is the signal at the input the the delay-line. Also, the instantaneous differential phase $\phi(t) = \phi_o(t) - \phi_i$, and the frequency difference between the injected signal and oscillator free running frequency $\Delta \omega = \omega_o - \omega_i$ have the same meanings.
with those in the LC tank analysis. The output frequency $\omega_{out}$ can be written as

$$\omega_{out} = \omega_i + \frac{d\phi_o(t)}{dt} = \omega_i + \frac{d\phi(t)}{dt}$$

(2.30)

and (2.28) becomes

$$\phi_d(\omega_{out}) = -N \tan^{-1} \left[ \frac{\omega_o - \Delta \omega + \frac{d\phi(t)}{dt}}{\omega_o} \tan \frac{\pi}{N} \right] \approx -\pi + \frac{N}{2} \left( \frac{\Delta \omega - \frac{d\phi(t)}{dt}}{\omega_o} \right) \sin \frac{2\pi}{N}$$

(2.31)

Expand Equation (2.31) at $\tan \frac{\pi}{N}$, we have

$$\tan \phi_d = -\tan \left[ \frac{N}{2} \left( \frac{\Delta \omega - \frac{d\phi(t)}{dt}}{\omega_o} \right) \sin \frac{2\pi}{N} \right] \approx -2Q \frac{\Delta \omega - \frac{d\phi(t)}{dt}}{\omega_o}$$

(2.32)

On the other hand, Figure 2.16 illustrates the phasor representation of the signals shown in Figure 2.15. We obtain

$$\tan (-\phi_d(t)) = \frac{\bar{V}_i \sin \phi(t)}{\bar{V}_o + \bar{V}_i \cos \phi(t)}$$

(2.33)

Equating Equations (2.33) and (2.32), we have

$$\frac{d\phi(t)}{dt} = \Delta \omega - \frac{\omega_o \bar{V}_i}{2Q \bar{V}_o} \frac{\sin \phi(t)}{1 + \frac{\bar{V}_i}{\bar{V}_o} \cos \phi(t)}$$

(2.34)
Consider that the injection signal is weak \( \left( \frac{V_i}{V_o} \ll 1 \right) \) \([13]\), then the system dynamics delay-line oscillator under low-level signal injection becomes:

\[
\frac{d\phi(t)}{dt} \approx \Delta \omega - \frac{\omega_o}{2Q} \frac{V_i}{V_o} \sin \phi(t)
\]  

(2.35)

If we define \( K_{SO} = \frac{\omega_o}{2Q} \frac{V_i}{V_o} \), Equation (2.35) becomes identical to that of the results derived in LC tank oscillators in Equation (2.23), where \( K_{SO(tank)} = \frac{g_m}{2C} \frac{V_i}{V_o} = \frac{\omega_o}{2Q} \frac{V_i}{V_o} \) once we substitute in \( Q = \omega_o RC \) for the parallel tank circuit. Therefore, Equation (2.23) can be served as the general locking equation for oscillators under low-level signal injection with

\[
K_{SO} = \frac{\omega_o}{2Q} \frac{V_i}{V_o}
\]  

(2.36)

We have discussed the dynamic phase equations for both on-chip LC-type and ring-type oscillators. For off-chip synchronous oscillator under low level injection, Equation (2.23) is also valid. We have shown in Appendix A a similar phase behavior of an astable multivibrator using off-chip op-amp ICs under signal injection.

Note that Equation (2.23) is identical to the first-order type-I PLL phase equation [46, 47] which indicates that the SO itself is basically a first-order PLL. However, it alleviates the needs for PD and feedback loop implementations, which are essential in a conventional first-order PLL.

### 2.4 SO Phase Plane Trajectory and Lock-in Range

It is instructive to look at the system dynamics by drawing the phase plane trajectory [46] of the SO described in Equation (2.23). Figure 2.17 shows \( d\phi/dt \), the frequency difference, as a function of \( \phi \), the phase difference. The equilibrium point resides at the point where the frequency error is zero and phase error is a constant.
where \( \phi_{ss} = \sin^{-1} \frac{\Delta \omega}{K_{SO}} \). By examining the existence of the equilibrium point, we can observe two regions of operation for the SO from Figure 2.17:

1) driven and locked when \( \Delta \omega - K_{SO} \leq 0 \) 
   \( (\dot{\phi} \leq 0) \)

2) driven but unlocked when \( \Delta \omega - K_{SO} > 0 \) 
   \( (\dot{\phi} > 0) \).

In the driven and locked region, a \( \phi_{ss} \) always exists such that \( \frac{d\phi}{dt} = 0 \). However, in the driven but unlocked region, the output will never be able to phase lock to the injected signal as \( \frac{d\phi}{dt} > 0 \). Therefore, the lock-in range of the SO is given by

\[
\Delta \omega_L = 2 \times K_{SO} = \frac{g_m \bar{V}_i}{C \bar{V}_o},
\]

which can also be observed as the swing of the phase plane trajectory. The SO injection parameter \( K_{SO} \) is also known as the one-sided lock-in range.

## 2.5 SO Transfer Characteristics and Output Spectrum

When the SO is driven but unlocked (\( \Delta \omega > K_{SO} \)), the spectrum of the SO’s output can be obtained following Armand’s method [14]. Noting that \( \sin \phi = \frac{2 \tan \frac{\phi}{2}}{1 + \tan^2 \frac{\phi}{2}} \),

\[
\frac{\omega}{1 + \tan^2 \frac{\phi}{2}}
\]
Equation (2.23) can be integrated as

$$\int_{\phi_0}^{\phi} \frac{d\phi}{\Delta \omega - K_{SO} \frac{2 \tan \frac{\phi}{2}}{1 + \tan^2 \frac{\phi}{2}}} = \int_{t_0}^{t} dt$$

By changing the variable $u = \tan \frac{\phi}{2}$ and carrying out the integration, we have

$$\tan \frac{\phi}{2} = \sin \theta + \cos \theta \tan \frac{\Omega t}{2}$$

with the beat frequency defined as

$$\Omega \triangleq \sqrt{\Delta \omega^2 - K_{SO}^2} = \Delta \omega \cos \theta,$$

and $\theta$ is depicted in Figure 2.18. Therefore, the output spectrum could be found:

$$V_o = \bar{V}_o \cdot e^{j \omega t} \cdot e^{j \phi}$$

$$= \bar{V}_o e^{j \omega t} \frac{1 + j \tan \frac{\phi}{2}}{1 - j \tan \frac{\phi}{2}}$$

$$= \bar{V}_o e^{j \omega t} \left[ - \frac{1}{j \tan \frac{\phi}{2}} + \frac{1 - \tan^2 \frac{\theta}{2}}{j \tan \frac{\phi}{2}} \cdot \frac{1}{1 - j \tan \frac{\theta}{2} e^{j(\Omega t + \theta)}} \right]$$

$$= j \bar{V}_o \tan \frac{\theta}{2} e^{j \omega t} + \bar{V}_o \frac{1 - \tan^2 \frac{\theta}{2}}{j \tan \frac{\phi}{2}} \sum_{n=1}^{\infty} \left( j \tan \frac{\theta}{2} \right)^n e^{jn(\Omega t + \theta) + j \omega t}$$

The output spectrum (2.41) of the SO can be interpreted in two ways: i) SO transfer characteristics where we look at the spectrum component at the injected frequency
and ii) for a specific injection $\omega_i$, the output spectrum at different spectrum frequencies.

(i) SO Transfer Characteristics

When the SO is driven but unlocked ($\Delta \omega > K_{SO}$), the spectrum component of the SO’s output at the injection frequency $\omega_i$ can be obtained from Equation (2.41) as

$$V_o(\omega_i) = j\bar{V}_o \tan \frac{\theta}{2} = \frac{j\bar{V}_o \sin \theta}{1 + \cos \theta} = \frac{j\bar{V}_o K_{SO}}{\Delta \omega + \sqrt{\Delta \omega^2 - K_{SO}^2}}$$

(2.42)

When the SO is locked, since the injected signal only introduces a phase modulation in the oscillating circuit, the output amplitude is independent of the input signal level. Figure 2.19 summarizes the SO transfer behaviors. In the unlocked region, the amplitude of the discrete Fourier component at the injection frequency is shown, and the phase is $\pm \frac{\pi}{2}$. In the locked region, the amplitude is constant and the phase displays
Table 2.2: Frequency spectrum of a driven but unlocked SO

<table>
<thead>
<tr>
<th>Freq</th>
<th>$V_o$ Amplitude</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\omega_i$</td>
<td>$V_o X$</td>
</tr>
<tr>
<td>$\omega_i + \Omega$</td>
<td>$V_o (1 - X^2)$</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>$\omega_i + n\Omega$</td>
<td>$V_o X^{n-1} (1 - X^2)$</td>
</tr>
</tbody>
</table>

an $\sin^{-1}$ function. Also, note that when the input level varies, the lock-in range will change accordingly since $\Delta \omega_L$ is proportional to $K_{SO}$. This linear relationship between the lock-in range and the injection level is fundamental to the SO operation and is referred to as the adaptive lock-in range.

(ii) SO Output Spectrum

If we let $X = \tan \frac{\theta}{2}$, we can rewrite Equation (2.41) as

$$v_o(t) = jV_o X e^{j\omega_i t} + \bar{V}_o \frac{1 - X^2}{jX} \sum_{n=1}^{\infty} (jX)^{n} e^{jn(\Omega t + \theta) + j\omega_i t}$$  \hspace{1cm} (2.43)

Based upon Equation (2.43), an entire frequency spectrum can be generated as shown in Table 2.2. $X$ ranges from 0 to 1 as $0 < \theta < 90^\circ$ in the driven but unlocked region. Starting from the second sideband $\omega_i + 2\Omega$, the energy is decreasing as compared with the energy at the previous sideband. However, the energy at the injection frequency $\omega_i$ will not exceed the first sideband $\omega_i + \Omega$ until the injection is very close to the lock-in range. In order to quantitatively find out how close the injected signal to the lock-in range will the energy at the $\omega_i + \Omega$ fall below that at the $\omega_i$, we can compare the amplitudes of the signals at the injected frequency and the first sideband. We find that if $0 < X < \frac{\sqrt{5} - 1}{2}$, which implies $\Delta \omega > \frac{\sqrt{5}}{2} K_{SO}$ ($\omega_i$ is sufficiently far from...
\( \Delta \omega > \sqrt{5} K_{SO} \) (a) \\
\( K_{SO} < \Delta \omega \leq \sqrt{5} K_{SO} \) (b)

Figure 2.20: SO output spectrum under driven but unlocked condition

\( \omega_o \), then the energy at \( \omega_i \) falls below that at the next sideband \( \omega_i + \Omega \), as shown in Figure 2.20 (a); if \( \sqrt{5} - \frac{1}{2} \leq X < 1 \), which implies \( K_{SO} < \Delta \omega \leq \frac{\sqrt{5}}{2} K_{SO} \) (\( \omega_i \) is very close to the lock-in range \( \omega_o \pm K_{SO} \)), then the energy at \( \omega_i \) exceeds that of the next sideband \( \omega_i + \Omega \), as shown in Figure 2.20 (b).

2.6 SO Phase Noise

The phase noise of the SO can be substantially reduced as compared to the oscillator without injection. Intuitively, the injection of a low-noise reference to the oscillator can correct the zero-crossing of the output waveform in each period in the time domain [11], thereby, reducing the jitter accumulation at the output.

2.6.1 LC-type SO

Once a noisy reference is applied to the LC tank oscillator, the assumption taken in the free running oscillator, that the average effective negative resistance contributed by the energy restoration element precisely cancels the positive tank resistance, will
no longer exist. When the SO is locked, \( \frac{d\phi}{dt} = \frac{d^2\phi}{dt^2} = 0 \), therefore combining Equation (2.23) with (2.22) we can obtain

\[
G_p - G_A = 2K_{SO}C\sqrt{1 - \left(\frac{\Delta\omega}{K_{SO}}\right)^2} \tag{2.44}
\]

Also, the tank impedance at an offset frequency of \( \Delta\omega_{os} \) can be found as

\[
Z_{\text{tank}}(\Delta\omega_{os}) = \frac{1}{G_p} \frac{\omega_o}{2Q\Delta\omega_{os}} \tag{2.45}
\]

Thus, the total impedance is obtained by combining Equation (2.44) and (2.45) as

\[
Z_{\text{tot}}(\Delta\omega_{os}) = Z_{\text{tank}}//1 = \frac{\omega_o}{2\omega_oK_{SO}\sqrt{1 - \left(\frac{\Delta\omega}{K_{SO}}\right)^2 + 2Q\Delta\omega_{os}}} \tag{2.46}
\]

Assume, the free-running oscillator has an inherent phase noise \( \phi_{\text{oscn}} \) associated with \( Z_{\text{tank}} \) and has a power spectral density (PSD) of \( S_{\phi_{\text{oscn}}} \); the injected signal has a phase noise \( \phi_{\text{injn}} \) associated with \( G_p - G_A \) and has a PSD of \( S_{\phi_{\text{injn}}} \). The overall output phase noise under injection can be represented as

\[
S_{\phi_{\text{out,n}}} = H_{\text{osc,n}} \cdot S_{\phi_{\text{oscn}}} + H_{\text{inj,n}} \cdot S_{\phi_{\text{injn}}} \tag{2.47}
\]

where

\[
H_{\text{osc,n}}(\Delta\omega_{os}) = \left| \frac{Z_{\text{tot}}(\Delta\omega_{os})}{Z_{\text{tank}}(\Delta\omega_{os})} \right|^2 = \frac{\Delta\omega_{os}^2}{K_{SO}^2 - \Delta\omega^2 + \Delta\omega_{os}^2} \tag{2.48}
\]

\[
H_{\text{inj,n}}(\Delta\omega_{os}) = \left( \frac{1}{G_p - G_A} \right)^2 = \frac{K_{SO}^2 - \Delta\omega^2}{K_{SO}^2 - \Delta\omega^2 + \Delta\omega_{os}^2}
\]

are the noise shaping functions for the oscillator phase noise and injected phase noise, respectively. A signal’s short-term instabilities are usually characterized in terms of the signal sideband noise spectral density. It has the unit of decibels below the carrier per hertz (dBc/Hz) and is defined in Equation 2.17. \( \mathcal{L}(\Delta\omega_{os}) \) includes the effect of
both amplitude and phase fluctuations. However, in most applications, $L(\Delta \omega_{os})$ is
-dominated by its phase portion, known as phase noise [43]. Rewrite Equation (2.47) with the phase noise notation, we have

$$L_{out}(\Delta \omega_{os}) = 10 \cdot \log \left[ H_{osc,n} \cdot 10^{\frac{L_{osc}(\Delta \omega_{os})}{10}} + H_{inj,n} \cdot 10^{\frac{L_{inj}(\Delta \omega_{os})}{10}} \right] \quad (2.49)$$

### 2.6.2 Delay-line Ring-type SO

For a delay-line SO, Equation (2.22) is not available as opposed to the LC tank SO. Therefore, the noise shaping functions in Equation (2.48) could not be obtained from the method mentioned in the previous section. A general methodology is to apply a small phase perturbation $\phi_{inj,n}$ and $\phi_{osc,n}$ on the injected signal and the oscillator, respectively. As a result of phase noise, the differential phase $\phi$ experiences a phase perturbation $\phi_n$. We can write $\omega'_i = \omega_i + \frac{d\phi_{inj,n}}{dt}$, $\omega'_o = \omega_o + \frac{d\phi_{osc,n}}{dt}$, and $\phi' = \phi + \phi_n$ where $\omega'_i$, $\omega'_o$ and $\phi'$ are the injected signal frequency, oscillator free running frequency, and differential phase, respectively, with the presence of phase noise, and $\omega_i$, $\omega_o$ and $\phi$ are the ones without phase noise. Equation (2.23) can be rewritten as

$$\frac{d\phi'}{dt} = \Delta \omega' - K_{SO} \sin \phi' \implies \frac{d(\phi + \phi_n)}{dt} = \Delta \omega + \frac{d\phi_{osc,n}}{dt} - \frac{d\phi_{inj,n}}{dt} - K_{SO} \sin (\phi + \phi_n) \quad (2.50)$$

When the SO is locked, $\phi = \phi_{ss} = \sin^{-1} \frac{\Delta \omega}{K_{SO}}$, Equation (2.50) becomes

$$\frac{d\phi_n}{dt} = \Delta \omega + \frac{d\phi_{osc,n}}{dt} - \frac{d\phi_{inj,n}}{dt} - K_{SO} \sin (\phi_{ss} + \phi_n)$$

$$\approx \Delta \omega + \frac{d\phi_{osc,n}}{dt} - \frac{d\phi_{inj,n}}{dt} - K_{SO} (\sin \phi_{ss} + \phi_n \cos \phi_{ss}) \quad [\text{small } \phi_n]$$

$$= \frac{d\phi_{osc,n}}{dt} - \frac{d\phi_{inj,n}}{dt} - K_{SO} \phi_n \cos \phi_{ss} \quad (2.51)$$
Applying the Laplace transform on Equation (2.51), we have

$$\Phi_n = \frac{(\Phi_{osc,n} - \Phi_{inj,n}) s}{s + K_{SO} \cos \phi_{ss}}$$

(2.52)

On the other hand, the perturbed output frequency can be found as

$$\omega'_{out} = \omega_i + \frac{d\phi'}{dt} + \frac{d\phi'}{dt}$$

$$= \omega_i + \frac{d\phi}{dt} + \frac{d\phi_{osc,n}}{dt} - K_{SO} \phi_n \cos \phi_{ss}$$

(2.53)

yielding the perturbed output phase to be:

$$\phi'_{out} = \int_{-\infty}^{t} \omega'_{out} dt = \omega_i t + \phi + \phi_{osc,n} - K_{SO} \cos \phi_{ss} \int_{-\infty}^{t} \phi_n dt$$

(2.54)

The output phase without noise is

$$\phi_{out} = \omega_i t + \phi_o = \omega_i t + \phi + \phi_i$$

(2.55)

The time-domain output phase perturbation is the difference between the perturbed phase in Equation (2.54) and the original phase in Equation (2.55), giving

$$\phi_{out,n} = \phi'_{out} - \phi_{out} = \phi_{osc,n} - K_{SO} \cos \phi_{ss} \int_{-\infty}^{t} \phi_n dt$$

(2.56)

Therefore,

$$\Phi_{out,n} = \Phi_{osc,n} - K_{SO} \cos \phi_{ss} \frac{\Phi_n}{s}$$

(2.57)

Combining (2.52) and (2.57), we can write

$$\Phi_{out,n} = \Phi_{osc,n} - K_{SO} \cos \phi_{ss} \frac{\Phi_{osc,n} + \Phi_{inj,n}}{s + K_{SO} \cos \phi_{ss}}$$

$$= \frac{s}{s + K_{SO} \cos \phi_{ss}} \Phi_{osc,n} + \frac{K_{SO} \cos \phi_{ss}}{s + K_{SO} \cos \phi_{ss}} \Phi_{inj,n}$$

(2.58)

Noting that when the system is locked, \(\cos^2 \phi_{ss} = 1 - \frac{\Delta \omega^2}{K_{SO}}\), then the power spectral
Figure 2.21: Phase noise shaping functions for oscillator noise and injection noise at $\omega_i = \omega_o$.

Figure 2.22: SO phase noise and noise model at $\omega_i = \omega_o$. 

(a) SO output phase noise

(b) SO phase noise model
density of the output phase noise can be written as:

\[
S_{\phi_{\text{out},n}} = \left| \frac{s}{s + K_{\text{SO}} \cos \phi_{ss}} \right|^2 S_{\phi_{\text{osc},n}} + \left| \frac{K_{\text{SO}} \cos \phi_{ss}}{s + K_{\text{SO}} \cos \phi_{ss}} \right|^2 S_{\phi_{\text{inj},n}}
\]

\[
= H_{\text{osc,n}} \cdot S_{\phi_{\text{osc},n}} + H_{\text{inj,n}} \cdot S_{\phi_{\text{inj},n}} \tag{2.59}
\]

where the noise shaping functions \( H_{\text{osc,n}} \) and \( H_{\text{inj,n}} \) have exactly the same expressions shown in Equation (2.48). Thus, Equation (2.48) becomes unified noise shaping functions for both LC tank SO and delay-line SO, and a unified phase noise expression after injection could be found in Equation (2.49). We can draw some conclusions from Equation (2.49): 1) within the lock-in range where \( \Delta \omega < K_{\text{SO}} \), the phase noise of the SO is dominated by the reference noise since the SO acts like a low-pass filter in allowing reference noise to reach the output while it acts like a high-pass filter for the oscillator noise, as shown in Figure 2.21. The reference noise is usually small since we frequently use a crystal oscillator for a frequency synthesizer, therefore the phase noise is greatly reduced because the oscillator noise is high pass filtered out. 2) as the frequency of the injected signal approaches the resonant frequency \( \omega_o \), the phase noise reduction reaches a maximum; the phase noise behavior when the injection occurs at the free running frequency (\( \Delta \omega = 0 \)) is shown in Figure 2.22(a), from where we observe the phase noise at a small offset is dominated by the injected noise, and the corresponding oscillator noise reduction is more evident than that at large offset, and the reduction vanishes at an offset frequency of infinity; 3) if the injected signal is close to the edge of the lock-in range where \( \Delta \omega = K_{\text{SO}} \), the phase noise reduction is less obvious and the reduction is finally zero when the injection is at these edges. To summarize, the 3dB corner frequency of the HPF \( \omega_{3dB} = \sqrt{K_{\text{SO}}^2 - \Delta \omega^2} \) increases with \( K_{\text{SO}} \) to suppress more VCO noise. We then can build a SO phase noise model based upon Equation (2.58), as is shown in Figure 2.22(b).
2.7 Voltage Controlled SO (VCSO) Design

To verify our analysis and to demonstrate possible on-chip applications of first-harmonic injection locking, a voltage controlled delay-line synchronous oscillator (VCSO) is designed with 130-nm standard CMOS process. The VCSO schematic design involves many considerations and tradeoffs among cost, ease of integration, and performance. Shown in Figure 2.23, the design employs a Voltage to Current Converter (V2I) and a current controlled 2-stage delay-line oscillator to achieve a wide operating frequency range. The differential delay cell is also shown in the figure. The configuration of a differential circuit is immune to supply disturbance. Active inductors realized by PMOS active loads and NMOS variable resistors are used to
compensate for the parasitic capacitance to increase the speed of the delay cell [48]. The cross coupled NMOS latch can boost the gain of each stage and can minimize the effect of supply voltage fluctuations once the latch is established. A Differential to Single (D2S) buffer is used to convert and buffer the differential output signal.

### 2.7.1 Voltage-to-Current (V2I) Converter

The SO is designed to have the voltage control capability for its further use inside the phase-locked loop, therefore, a linear V2I converter is needed. In the VCSO design, we simply use the transconductance behavior of a MOSFET’s input gate voltage and output drain current. In the square law model, when the constant term \( \frac{1}{2} \mu_C \frac{W}{L} \) is much less than the overdrive voltage \( V_{GS} - V_{th} \), the drain current is considered linearly related to the gate voltage. Note that the current in the input device is mirrored over to control the current used in the current-starved VCO, so the delay-line tail current is simply a scale of the control device drain current depending

![Figure 2.24: V2I conversion transfer functions w/ different load voltages](image)
on the width-to-length ratio of the current mirror devices. Figure 2.24 shows the linear transfer characteristic of the V2I with different drain voltages at the mirroring PMOS devices.

2.7.2 Delay Cell

The delay cell employs differential PMOS inputs to get rid of the body effect, a cross coupled NMOS latch to boost the stage gain and minimize the effect of supply voltage fluctuations once the latch is established, and active inductors realized by PMOS active loads and NMOS variable resistors to compensate for the parasitic capacitance to increase the speed [48]. As is shown in Figure 2.25, the effective impedance looking into the active inductor is

\[
Z = \frac{1 + j\omega RC_{gs}}{g_m + g_{mb} + j\omega C_{gs} (1 + Rg_{mb})}
\]  

(2.60)

The circuit is inductive when \(\omega_z < \omega_p\), yielding \(R > \frac{1}{g_m}\). The effective series resistance \(R_s\) and inductance \(L_s\) can be controlled by adjusting the triode resistance \(R\) as follows

\[
R_s = \frac{g_m + \omega^2 C_{gs}^2 R}{g_m^2 + \omega^2 C_{gs}^2}
\]

(2.61)

\[
L_s = \frac{C_{gs} g_m R - C_{gs}}{g_m^2 + \omega^2 C_{gs}^2}
\]

(2.62)
We employ a series to parallel conversion and use the active inductor reactance to partially cancel the output node capacitance, $C_L$, as shown in Figure 2.26. Thus, we find the effective time constant $\tau$ as

$$\tau = R_{\text{eff}} C_{\text{eff}} = \left( R_S + \frac{\omega^2 L_S^2}{R_S} \right) \left( C_L - \frac{L_S}{R_S^2 + \omega^2 L_S^2} \right)$$  (2.63)

### 2.7.3 Injection Ports

The VCSO is designed to receive the low level signal injection from the output of each delay stage. Simple common source differential pairs are used to convert the injection voltage to current and modulate the tail current of each delay stage, as shown in Figure 2.23. The differential pairs are designed to have the maximum injection effect and the minimum loading effect on the output node.

The VCSO design is implemented with GlobalFoundries 130nm CMOS technology. Figure 2.27 shows the final layout of VCSO.

### 2.8 VCSO Simulation and Experimental Results

This section shows the simulation and measurement results in order to validate the theory given in the previous sections.
2.8.1 IC Implementation

Figure 2.28 shows the die microphotograph of the VCSO. The core chip occupies an area of 100µm×50µm. The prototype VCSO is measured with a Cascade Probe test system which consists of a RF probe station, ground-signal-ground (GSG) coplanar RF probes, and high-speed cables. The detailed description of the on-chip test set-ups for different measurements is given in Appendix B. A 1.2V battery is employed to supply power to the VCSO chip for a low noise solution.

2.8.2 VCSO Voltage-Frequency Transfer Characteristics

Figure 2.29 plots the simulated VCSO transfer characteristics for different process corners Typical-NMOS Typical-PMOS (TT), Fast-NMOS Fast-PMOS (FF), and Slow-NMOS Slow-PMOS (SS) with no injection applied. The designed VCSO operates from 0.5GHz to 1.7GHz and achieves the linear gain $K_o$ that varies by a factor of
less than 1.3 for almost the entire range of the control voltage ($V_{Tn,ctrl} \leq V_{ctrl} \leq V_{DD}$) where $V_{Tn,ctrl}$ is the threshold voltage of the NMOS device where the control voltage is applied. The slight variation of $K_o$ will modestly impacts the loop dynamics of the PLL. Figure 2.29 also shows the measured transfer characteristic which matches well with the typical corner simulation.

2.8.3 VCSO Injection Signal Transfer Characteristics – S21

Figures 2.30 and 2.31 plots the simulated and measured injection signal transfer characteristic S21 of the designed VCSO circuit. Some characteristics are summarized as below, and they follow the analytical evaluations in Section 2.4:

- In the driven and locked region, the SO output amplitude remains constant when the input signal amplitude varies.
• The tracking bandwidth $\omega_L = 2K_{SO}$ is proportional to the input signal amplitude, as shown in Figure 2.32. This linear relationship between tracking bandwidth and injection signal level is fundamental to SO operation and is referred to as the adaptive tracking bandwidth.

• For a given injection level, the phase error $\phi$, is an arcsine function of the frequency difference $\Delta\omega$.

• A SO functions as an instantaneous bandpass filter.

In the measured S21, the center frequency is set by a control voltage which is tuned by a potentiometer. Due to the sensitivity of the potentiometer, the center frequency shifts in the measurement. Figure 2.32 compares the measured lock-in range with the simulated lock-in range for different levels of injections. The agreement can be seen from the plot.
Figure 2.30: Simulated VCSO amplitude and phase characteristics
Figure 2.31: Measured VCSO amplitude and phase characteristics
2.8.4 VCSO Output Spectrum

The SO injection locking process can be intuitively observed by looking at the output spectrum shown in Figure 2.33. In this measurement, the free running frequency is set to be 1028 MHz and the two-sided lock-in range is 64MHz with a -24 dBm signal injection. As the injection signal sweeps the frequency band, the SO output spectrum changes as shown in picture (a) through picture (f). As the injection frequency moves closer to the lock-in range, the beat frequency becomes smaller and smaller, and more sidebands can be seen on one side of the tracking band for the given frequency spectrum (picture (a)). The beat frequency in (a) calculated from Section 2.1.2 is

$$\Omega_{cal,a} = \sqrt{\Delta \omega^2 - K_{SO}^2} \approx 2\pi \cdot 21.4 \text{MHz}$$

(2.64)

which is very close to the measured results of $\Omega_{mea,a} = 2\pi \cdot 22 \text{MHz}$ in picture (a). As the injection frequency approaches the edge of the tracking range, the energy at
Figure 2.33: SO output spectrum with different injection frequency $f_i$ ($P_i = -24dBm$)
the injection begins to dominate, shown in picture (b). This is the moment just before the injection locking takes place. When the oscillator is locked in picture (c) to (d), the SO output amplitude is constant and the oscillation frequency follows the injection frequency across the tracking band. As the injection frequency leaves the lock-in range, the output spectrum is a mirror of the situation where the injection enters the lock-in range.

2.8.5 VCSO Phase Noise

Figure 2.34 compares the phase noises (PN) between the free running VCO with \( V_{\text{inj}} = 0 \) and the VCSO with \( V_{\text{inj}} = 10\text{mV}/20\text{mV}/30\text{mV} \) in both simulation and theory. The calculated VCSO phase noise is plotted by applying the noise transfer functions (2.48) on the simulated VCO phase noise curve without injection. The injection parameter \( K_{\text{SO}} \) for each injection strength can be found from Figure 2.32. The phase noise is greatly reduced in the SO system at offset frequencies below \( K_{\text{SO}} \), the one-sided lock-in range. The phase noise at an frequency offset of 1MHz improves from -87dBc/Hz to -123dBc/Hz under 30mV injection. As the offset frequency increases beyond \( K_{\text{SO}} \), the reduction is less obvious. We can also observe a lower phase noise for a higher injection level. It is predictable from Equation (2.49) that for a fixed \( \Delta \omega \) and \( \Delta \omega_{\text{os}} \), a larger \( K_{\text{SO}} \) from the larger injection level results in a larger noise reduction.

The measured VCSO phase noise is shown in Figure 2.35. Similar to the simulation results, since the VCSO noise is high passed as the result of the signal injection, the low frequency VCSO noise is reduced, and the injection level determines the strength of the noise suppression. The measured phase noise in Figure 2.35 is higher than the simulation in Figure 2.34. This phase noise deterioration is due to the reason that
control voltage noise is not considered in the SO phase noise model, and in the actual measurement, the noise from the testing equipment is involved.

2.8.6 VCSO Figure-of-Merit (FoM)

For a VCO alone without injection, the performance can be summarized with the Figure-of-Merit defined as [49,50]

\[
FoM = L (\Delta \omega) - 10 \log \left( \frac{\omega_o}{\Delta \omega} \right)^2 + 10 \log \left( \frac{P}{1mW} \right) - 10 \log \left( \frac{FTR}{VCR} \right)
\] (2.65)

showing the trade-off between power, oscillating frequency, phase noise, frequency tuning range (FTR) and control voltage range (VCR). The ratio between FTR and VCR essentially links to the VCO gain \(K_o\). The old FoM does not include \(K_o\) [51], however, \(K_o\) is a very important parameter, and has trade-off with the phase noise because for a limited power supply voltage, high VCO gain indicates the VCO is more...
Figure 2.35: VCSO measured phase noise (unfiltered): injection suppresses low offset VCO phase noise; the injection power determines the suppression strength.

Table 2.3: VCSO FoM Comparison

<table>
<thead>
<tr>
<th>Pinj</th>
<th>FoM (dBc/Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 mW</td>
<td>-146.2</td>
</tr>
<tr>
<td>-33 dBm</td>
<td>-171.2</td>
</tr>
<tr>
<td>-27 dBm</td>
<td>-176.2</td>
</tr>
<tr>
<td>-24 dBm</td>
<td>-181.2</td>
</tr>
</tbody>
</table>

sensitive to the voltage induced phase noise. Therefore, the phase noise is referred to the VCO input by dividing it with $K_o$, and the lower the input referred phase noise, the better the VCO performance [50]. For the ring-type VCSO, the phase noise is worse than the LC-type counter-part due to the low effective quality factor $Q$. The FoM of the designed ring-type VCSO has been calculated from the measurement results as shown in Table 2.3. With the help of the signal injection, the FoM of the ring-type VCSO is very competitive with the LC-type VCOs [50].
2.9 Summary

Injection locking can be useful in many on-chip applications. This chapter has focused on the study of the low-level first-harmonic injection locking phenomenon in the on-chip Synchronous Oscillators (SOs). An introduction on the commonly used on-chip oscillators has been provided at the very beginning of this chapter to help understand the behavior of the on-chip SOs. A unified phase model and a general phase noise transfer functions have been derived for both LC-type SOs and delay-line ring-type SOs. A voltage-controlled SO (VCSO) has been designed with a 2-stage delay-line ring-type oscillator implemented in 130nm CMOS process. It has a center frequency at 1GHz and occupies only 100µm×50µm. The simulation and measurement results show a good agreement with the presented analysis. The SO shows great potential in noise suppression in on-chip applications, such as resonant clock distribution, etc. More importantly in this research, the VCSO will serve as the basic building block for the proposed Reference-Injected Phase-Locked Loop (PLL-RI) in Chapter 4.
Chapter 3: Device Baseband Characterization and
Up-Conversion of Device Baseband Noise to Synchronous
Oscillator Phase Noise

Device baseband characterization can help device engineers know what they’ve made, and optimize the fabrication process and develop device models. Device characterization is also beneficial to circuit designers to help them better understand their circuits. Therefore, this chapter will first cover some important characterization techniques for MOSFET devices: the basic principle, implemented setups, and some example measurement from the devices of interest. In electronics, noise generated by electronic devices greatly affects the noise performance of the communication systems. In oscillators, device baseband noise is up-converted to the radio frequency regime in the presence of the phase noise, which is described as short-term random frequency fluctuations of a signal. Low oscillator phase noise is a necessity for the transceiver design. For FM or PM signal, the oscillator phase noise will limit the ultimate Signal to Noise Ratio (SNR); in a PSK digital transmission system, local oscillator phase noise will affect the Bit Error Rate (BER); phase noise in the receiver introduces the reciprocal mixing when there is a strong nearby interferer; and a substantial phase noise in the transmitter will corrupt the nearby receivers. So in addition to the device characterization, we review the methods to up-convert the device baseband noise to
oscillator output phase noise. Finally, the SO proposed in Section 2.7 is used as an example to show the noise up-conversion.

3.1 IV Characterization of MOSFET Devices

Generally, the characterization setup is composed of a probe system, testing equipment, software and programs that control the equipment and process the data, as well as a shielding environment. The detailed measurement setup is shown in Appendix B. We are interested in extracting the threshold voltage, carrier mobility, the effective substrate doping concentration, and interface trap density. The results are mainly based on high quality CMOS transistors with SiO$_2$ dielectric layer and polysilicon gate. The physical oxide thickness is about 30Å.

3.1.1 Threshold Voltage Extraction

The threshold voltage $V_T$ is one of the most important MOSFET parameters. Industrially, since a large number of samples are evaluated, $V_T$ is usually defined at the gate bias that drives a certain amount of drain current. For example, it is commonly measured as the gate bias which generates $I_{ds} = 100\text{nA} \cdot \frac{W}{L}$ [52]. On the other hand, in the research study, people use bench-testing more often. The most popular way to define and extract $V_T$ is the so called “linear extrapolation method” [53].

Figure 3.1 plots the transfer characteristics $I_{ds}$ vs $V_{gs}$ of the measured NMOS at different substrate biases $V_{sb}$. We first find the gate bias where the transconductance $g_m = \frac{\partial I_{ds}}{\partial V_{gs}}$ reaches the maximum, then we draw a tangent line at that particular gate bias on the current plot and find its intercept with the x axis ($V_{gs}$ axis). This intercept gives the threshold voltage of the device at the corresponding substrate bias level. With an increase of the substrate bias, the threshold voltage increases as well.
Figure 3.1: Drain current ($I_{ds}$) and transconductance $g_m$ vs. gate voltage $V_{gs}$ at different substrate biases $V_{sb}$. A Linear extrapolation at the point of tangency gives the device threshold voltage. The measurements are taken with small drain bias. (NMOS 5/1)
Figure 3.2: Flowchart for extracting the substrate doping concentration $N_A$

due to the body effect explained in Equation 3.1.

$$V_T = V_{FB} + 2\phi_F + \gamma_n \sqrt{2\phi_F + V_{sb}}$$

$$= V_{T0} + \gamma_n \left( \sqrt{V_{sb} + 2\phi_F} - \sqrt{2\phi_F} \right) \quad (3.1)$$

where $V_{FB}$ is the flatband voltage, and the threshold voltage at zero substrate bias $V_{T0}$ is defined as

$$V_{T0} = V_{FB} + 2\phi_F + \gamma_n \sqrt{2\phi_F} \quad (3.2)$$

and the body effect parameter $\gamma_n$ is

$$\gamma_n = \frac{\sqrt{2\epsilon_{ss} q N_A}}{C_{ox}} \quad (3.3)$$
where $\epsilon_s$ is the semiconductor permittivity, $q$ is the electron charge, $N_A$ is the effective substrate doping density, and $C_{ox}$ is the effective oxide capacitance. The Fermi potential $\phi_F$ is the potential difference between the Fermi level and the intrinsic energy level in the semiconductor bulk, and is given as

$$\phi_F = \frac{k_B T}{q} \ln \left( \frac{N_A}{n_i} \right) \quad (3.4)$$

where $K_B$ the Boltzmann’s constant, $T$ the absolute temperature, and $n_i$ the intrinsic carrier concentration.

An iterative method to find the substrate doping concentration $N_A$ is adopted here [53]. Figure 3.2 shows the flowchart of finding the effective $N_A$: we start with an initial guess of $N_A$, and calculate $\phi_F$ with Equation (3.4). Knowing the measured threshold voltage at each substrate biasing, we can plot $V_T$ vs. $\sqrt{V_{sb} + 2\phi_F} - \sqrt{2\phi_F}$ with the calculated $\phi_F$. From Equation (3.1), the slope of the plot is $\gamma_n$. Using

**Figure 3.3:** Converged $V_t$ vs. $\sqrt{V_{sb} + 2\phi_F} - \sqrt{2\phi_F}$ (NMOS 5/1)
Table 3.1: Extracted parameters from I-V characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>NMOS 5/1</th>
<th>PMOS 5/0.5</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{T0}$ (V)</td>
<td>0.21</td>
<td>-0.25</td>
</tr>
<tr>
<td>$N_A$ (1/cm$^3$)</td>
<td>6.2E17</td>
<td>6.5E17</td>
</tr>
<tr>
<td>$\gamma$ (\sqrt{V})</td>
<td>0.41</td>
<td>0.42</td>
</tr>
<tr>
<td>$\phi_F$ (V)</td>
<td>0.44</td>
<td>-0.45</td>
</tr>
<tr>
<td>$V_{FB}$ (V)</td>
<td>-1.05</td>
<td>1.03</td>
</tr>
</tbody>
</table>

Equation (3.3), we are able to find a new $N_A$. Update the initial guess of $N_A$ with the new one and iterate the whole process until the difference between the two values falls under some limit, and we say the process converges. Figure 3.3 plots the $V_T$ vs. $\sqrt{V_{sb} + 2\phi_F} - \sqrt{2\phi_F}$ after the $N_A$ is converged to its final value. The test results are listed in Table 3.1 for both N and P type MOSFETs.

3.1.2 Mobility Extraction

The long channel model with low drain bias gives the current expression [53]

$$I_{ds} = \frac{\beta_o (V_{gs} - V_T) V_{ds}}{1 + \theta_s (V_{gs} - V_T + 2\gamma_n \sqrt{V_{sb} + 2\phi_F})}$$  \hspace{1cm} (3.5)

where $\theta_s$ is the surface roughness parameter, and

$$\beta_o = \mu_o C_{ox} \frac{W}{L}$$  \hspace{1cm} (3.6)

with $\mu_o$ as the effective mobility excluding the surface roughness scattering. The effective mobility can be written as

$$\mu_{eff} = \frac{\mu_o}{1 + \theta_s (V_{gs} - V_T + 2\gamma_n \sqrt{V_{sb} + 2\phi_F})}$$  \hspace{1cm} (3.7)

and we notice the mobility degradation as $V_{gs}$ increases due to the high vertical electric field confines electrons to the surface of the channel [54].
From Equation (3.5), we can find the drain conductance at low $V_{ds}$:

$$g_{ds} = \frac{\partial I_{ds}}{\partial V_{ds}}|_{V_{ds}=0} \approx \frac{I_{ds}}{V_{ds}} = \frac{\beta_o (V_{gs} - V_T)}{1 + \theta_s (V_{gs} - V_T + 2\gamma_n \sqrt{V_{sb} + 2\phi_F})}$$  \hspace{1cm} (3.8)$$

Rearrange Equation (3.8):

$$\frac{V_{ds}}{I_{ds}} (V_{gs} - V_T) = \frac{1}{\beta_o} + \frac{\theta_s}{\beta_o} \left( V_{gs} - V_T + 2\gamma_n \sqrt{V_{sb} + 2\phi_F} \right)$$  \hspace{1cm} (3.9)$$

Therefore, if we plot $\frac{V_{ds}}{I_{ds}} (V_{gs} - V_T)$ vs. $\frac{1}{\beta_o} + \frac{\theta_s}{\beta_o} \left( V_{gs} - V_T + 2\gamma_n \sqrt{V_{sb} + 2\phi_F} \right)$, we can extract both $\beta_o$ and $\theta_s$ from the slope and the intercept point, then the mobility can be found from Equation (3.6). Figure 3.4 plots this curve on the measured device. The obtained values together with the other device parameters on CMOS devices with different size are listed in Table 3.2.

Notice, as the channel length decreases, the threshold voltage increases. This is because of the reverse short channel effect caused by localized heavy doping (aka.
Halo Implant) in the channel near the source and drain junction. In addition, the mobility degrades as the channel length decreases. Several reasons contribute to this phenomena: it is possible for the contact resistance to have profound contribution as the channel length is small; also when the length is small, the heavy substrate doping from the Halo implant effectively degrades the mobility. Another observation from Table 3.2 is that the mobility of electrons in NMOS is much larger than the mobility of holes in PMOS.

Also, from Table 3.2 we notice that the surface roughness parameter $\theta_s$ is not constant for different device sizes. The reason is that we need to consider the series resistance $R_s$ if we want to model is correctly [53]:

$$\theta_s = \theta_{so} + 2\mu_o C_{ox} \frac{W}{L} R_s$$

(3.10)

where $R_s$ is the series resistance in the source and drain regions and $\mu_o$ is the low-field mobility. Thus, the series resistance combined with a change in W/L can cause an increase in $\theta_s$. We can extract $R_s$ by subtracting $\theta_s$ of two NMOS devices with
different W/Ls:

\[ \theta_s \text{ (NMOS } 5/0.5) - \theta_s \text{ (NMOS } 5/1) = 1.03 - 0.90 = 2\mu_1C_{\text{ox}} \frac{5}{0.5} R_s - 2\mu_2C_{\text{ox}} \frac{5}{1} R_s \]

Substituting the extracted low-field mobility in Table 3.2 into Equation (3.11), we can calculate the series resistance \( R_s \) to be 10.8Ω.

### 3.1.3 Interface Trap Density Extraction

Interface/near-interface trap density is another important parameter to determine the overall performance of the MOSFET with thin gate dielectrics. During device operation, these trapping centers will capture carriers and shift the threshold voltage [55]. As is mentioned in Section 1.3, this trapping behavior also gives rise to the 1/f low frequency noise (LFN) and degrades the carrier mobility. In this work, we try to approximate the interface trap density through the sub-threshold slope method.

In the sub-threshold region, the drain current of a MOSFET can be written as

\[ I_d = I_o e^{\frac{\phi_{gs}}{K_BT}} \]

which describes the junction forward current at the source and the parameter \( n \) is defined as the gate voltage \( V_{gs} \) over the surface potential \( \phi_s \). The sub-threshold slope \( S \) is defined as the gate voltage range required to change the drain current by one decade:

\[ S = \ln 10 \left( \frac{\partial \ln I_{ds}}{\partial V_{gs}} \right)^{-1} = n \cdot 2.3 \cdot \frac{K_BT}{q} = n \cdot 60(\text{mV}/\text{dec}) \]

Shown in the MOSFET equivalent circuit Figure 3.5, \( n \) can be found:

\[ n = \frac{V_{gs}}{\phi_s} = 1 + \frac{C_D + C_{it}}{C_{ox}} \]
Figure 3.5: MOS capacitor equivalent circuit

where $C_{ox} = \frac{K_o \epsilon_o}{x_o}$ is the oxide capacitance, $C_D = \frac{k_s \epsilon_o}{x_D}$ is the depletion layer capacitance, and $C_{it} = qD_{it}$ is the capacitance from the interface traps with $D_{it}$ as the interface trap density. Therefore, $D_{it}$ can be found by substituting Equation (3.14) into Equation (3.13):

$$D_{it} = \frac{1}{q} C_{ox} \left[ \frac{S (\text{mV/dec})}{60} - 1 - \frac{C_D}{C_{ox}} \right]$$

(3.15)

where $k_o = 3.9$ and $k_s = 11.9$ are the relative permittivity for SiO$_2$ and Si, respectively; $x_o$ and $x_D$ are the oxide thickness and depletion layer width, respectively; $\epsilon_o = 8.85 \times 10^{-14} \text{F/cm}$ is the vacuum permittivity, and $q = 1.6 \times 10^{-19} \text{C}$ is the electron charge. The depletion region width can be approximately calculated from the doping concentration $N_A$ and the Fermi potential $\phi_F$ as [52]

$$x_D = \sqrt{\frac{2k_s \epsilon_o \cdot 2\phi_F}{qN_A}}$$

(3.16)

Shown in Figure 3.6, the sub-threshold slope can be found from the drain current plot in the sub-threshold region, as $S = 80 \text{mV/dec current}$. Therefore, $D_{it}$ of the NMOS and PMOS can be extracted, as listed in Table 3.3.
Figure 3.6: Measured sub-threshold current (NMOS 5/1)

Table 3.3: Extracted interface trapping density from the sub-threshold method

<table>
<thead>
<tr>
<th>Parameter</th>
<th>NMOS 5/1</th>
<th>PMOS 5/0.5</th>
</tr>
</thead>
<tbody>
<tr>
<td>$D_{it}$ (cm$^{-2} \cdot eV^{-1}$)</td>
<td>7.2E11</td>
<td>4.3E11</td>
</tr>
</tbody>
</table>

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3.2 Device Baseband Noise Up-conversion

As is discussed in Section 1.3, the main noise sources in the MOSFET is the thermal noise and low frequency noise (LFN). We need to consider both of them separately because the LFN fluctuates at a rate much lower than the oscillation frequency. The oscillator by itself is an integrator if we consider phase as the signal, therefore, a power transfer function of \( \frac{1}{s^2} \) will be observed for base band-noise inside the VCO to be up-converted to the phase noise. As is shown in Figure 3.7, the flicker noise is up-converted to the RF region and showing a \( 1/f^3 \) behavior, and the white noise is up converted to the RF region showing a \( 1/f^2 \) behavior.

3.2.1 White Noise Up-conversion

The relation between the phase noise and timing jitter can be found in Appendix C as:

\[
\sigma_t^2 = \frac{1}{2\pi^2 f_o^2} \int_{-\infty}^{\infty} S_\phi(f) \left( 1 - e^{j2\pi f f_o} \right) df = \frac{2}{\pi^2 f_o^2} \int_0^{\infty} S_\phi(f) \sin^2 \left( \frac{\pi f}{f_o} \right) df \quad (3.17)
\]
where the timing jitter is defined as the variance $\sigma^2_\tau$ of the timing uncertainty $\tau(t)$ around its mean value [56], and $S_\phi(f)$ is the power spectral density of the RMS value of phase fluctuations $\phi(t)$. When the offset frequency $f_{os}$ is well above $f_\Delta$ and well below $f_o$, Vendelin showed that [57]

$$S_\phi(f_{os}) = 2L(f_{os}) = \frac{2cf_o^2}{f_{os}^2}$$

(3.18)

where $L(f_{os})$ is the oscillator output phase noise, $f_\Delta = cf_o^2\pi$ is called the corner frequency of the Lorentzian process when the free-running oscillator is perturbed only by white noise sources. $c$ is an empirical constant [58]. In this case, the period jitter in Equation (C.6) can be evaluated exactly:

$$\sigma^2_\tau = \frac{2}{\pi^2 f_o^2} \int_0^\infty \frac{2cf_o^2 f_{os}^2}{f_{os}^2} \sin^2\left(\frac{f_{os}}{f_o}\right) df_{os} = \frac{2cf_o^2}{f_o^3} = \frac{2L(f_{os})f_{os}^2}{f_o^3}$$

(3.19)

Thus,

$$L(f_{os})_{\text{white}} = \frac{\sigma^2_\tau f_o^3}{\frac{1}{2} f_{os}^2}$$

(3.20)

In a N stage delay cell ring oscillator, the timing jitter is found by dividing the noise voltage by the slope $k$ of the output voltage at zero crossing, giving $\sigma^2_\tau = 2N \times \sigma^2_{td} = 2N\bar{v}_n^2/k\tau$, therefore,

$$L(f_{os})_{\text{white}} = \frac{N\bar{v}_n^2 f_o^3}{k^2 f_{os}^2}$$

(3.21)

### 3.2.2 Flicker Noise (1/f Noise) Up-conversion

For a differential oscillator, the dominant flicker noise is in the tail current which is derived from the control FET. Abidi [8] shows that the flicker noise in the differential pairs does not cause phase noise because it is low frequency, and its effect on the differential input offset voltage can be treated as constant over one oscillator period,
therefore it won’t change the oscillating frequency. However, the flicker noise in the
tail current directly modulates the delay. The delay variations in all stages will add
in phase due to the noise on the common gate voltage driving the tail FETs which is
derived from the control device and cause a large phase noise.

The process of the flicker noise in the device baseband affecting the oscillating
frequency resembles the frequency modulation (FM), which encodes the information
in a carrier signal by varying its instantaneous frequency. The frequency components
in a FM signal can be calculated using Bessel function of the first kind \( J_\alpha (\beta) \):

\[
V_{FM} (t) = V_{pk} \cos [\omega_c t + \beta \sin (\omega_m t)] = V_{pk} J_0 (\beta) \cos (\omega_c t) + \\
V_{pk} J_1 (\beta) \{ \cos [(\omega_c + \omega_m) t] - \cos [(\omega_c - \omega_m) t] \} + \\
V_{pk} J_2 (\beta) \{ \cos [(\omega_c + 2\omega_m) t] + \cos [(\omega_c - 2\omega_m) t] \} + \ldots
\]

(3.22)

where \( \omega_c(t) \) is the carrier frequency, \( \omega_m \) the frequency of the baseband signal, the
modulation index \( \beta \) is defined as \( \beta = \frac{\Delta f_{pk}}{f_m} \), and \( \Delta f_{pk} \) is the frequency deviation which
represents the maximum shift away from \( f_c \) in one direction. To apply FM theory
in the oscillator phase noise, the carrier frequency \( f_c \) compares to the oscillator free
running frequency \( f_o \), the baseband frequency \( f_m \) equates the offset frequency \( f_{os} \).
Thus, from the definition of the single sideband phase noise,

\[
\mathcal{L} (f_{os}) = \frac{[V_{pk} J_1 (\beta)]^2 / df}{[V_{pk} J_0 (\beta)]^2} = \left( \frac{\beta}{2} \right)^2 / df = \frac{\Delta f_{pk}^2 / df}{4 f_m^2}
\]

(3.23)

Assuming \( \kappa \) is the sensitivity of the oscillator frequency on the baseband 1/f noise
voltage \( v_n \) and \( S_v (f) \) is the noise voltage power spectrum density, we have \( \Delta f_{pk}^2 / df = \kappa^2 S_v (f) \), and assuming narrow band FM,

\[
\mathcal{L} (f_{os})_{\text{flicker}} \approx \frac{\kappa^2 S_v (f)}{4 f_{os}^2}
\]

(3.24)
3.3 Phase Noise in the Delay-Line SO

Consider a differential delay stage shown in Figure 3.8. To keep the analysis simple, we assume the white noise is only contributed by the effective load resistor $R_{eff}$ shown in Equation (2.63), the tail FET M2, and the differential FETs M3 and M4. We neglect the noise effect from the cross coupled device M9 and M10. Meanwhile, we assume the flicker noise in the control FET M1 contributes most of the phase noise with the reason shown in the previous section. In the following analysis, we will consider each noise source separately and find the total final phase noise from superposition of Equations (3.21) and (3.24).
3.3.1 White Noise Contribution

1. White noise coupled to effective load capacitors.

\[
\bar{v}_{n,R}^2 = \frac{k_B T}{C_{eff}} \times 2 = \frac{2k_B T}{C_{eff}} \tag{3.25}
\]

2. White noise contributed by the tail FET M2. Suppose a transition steers current from the left branch to the right. Assume a noise current \( \bar{i}_{n,\text{tail}} \) with the power spectrum density of \( S_{n,\text{tail}} = 4k_B T \gamma g_{m2} \), and the noise voltage shown on the left output is at its steady state \( \bar{v}_{n,\text{tail},SS}^2 \). Then, when the current is steered to the right, the noise voltage stored on the capacitor leaks with time. After a propagation delay \( t_d \), the rest noise voltage on the left node is

\[
\bar{v}_{n,\text{tail},L}^2 = \bar{v}_{n,\text{tail},SS}^2 \cdot \left( e^{-\frac{t_d}{2}} \right)^2 = \int_0^\infty S_{n,\text{tail}} \frac{R_{eff}}{1 + j2\pi f R_{eff} C_{eff}} \left| \tilde{W}_d (f) \right|^2 df \cdot \left( e^{-\frac{t_d}{2R_{eff} C_{eff}}} \right)^2 \tag{3.26}
\]

Once the current is switched to the right, the tail current will integrate noise on the load capacitance on the right side through a lossy integration [8]. The noise voltage on the right output can be found as [8]:

\[
\bar{v}_{n,\text{tail},R}^2 = \frac{1}{C_{eff}^2} \left| \tilde{W}_d (f) \right|^2 S_{n,\text{tail}} = \frac{1}{C_{eff}^2} A k_B T \gamma g_{m2} \frac{t_d}{2} \left( 1 - e^{-\frac{2t_d}{R_{eff} C_{eff}}} \right) \tag{3.27}
\]
where $\tilde{W}(f)$ is the Laplace transform of the lossy integration window. Therefore, the differential noise voltage is

$$v_{n,\text{tail}}^2 = v_{n,\text{tail},R}^2 + v_{n,\text{tail},L}^2$$

$$= \frac{k_B T}{C_{eff}} \gamma_2 g_m R_{eff}$$

(3.28)

3. White noise contributed by the differential FETs M3 and M4.

To simplify the analysis, let’s assume during the transition time, noise from differential pairs integrate over $t_d$ instead of some fraction of the transition time $t_T$ [8]. The power spectrum density for the noise current $i_{n,\text{diff},b}$ at balance is

$$S_{i_{n,\text{diff},b}} = 4k_B T \gamma_3 g_m$$

(3.29)

then the differential current noise spectrum density can be found as

$$S_{i_{n,\text{diff}}} = 2 \times \frac{S_{i_{n,\text{diff},b}}}{4} = \frac{S_{i_{n,\text{diff},b}}}{2}$$

(3.30)

Apply a lossy integration on Equation (3.30), we get

$$\bar{v}_{n,\text{diff}}^2 = \frac{1}{\left(C_{eff}/2\right)^2} \left| \tilde{W}(f) \right|^2 S_{i_{n,\text{diff}}}$$

$$= \frac{3}{2C_{eff}} k_B T \gamma_3 g_m R_{eff}$$

(3.31)

The total noise voltage due to white noise can be found by summarizing Equations (3.25), (3.28), and (3.31) as

$$v_{n,\text{diff}}^2 = v_{n,R}^2 + v_{n,\text{tail}}^2 + v_{n,\text{diff}}^2$$

$$= \frac{2k_B T}{C_{eff}} + \frac{k_B T}{C_{eff}} \gamma_2 g_m R_{eff} + \frac{3}{2C_{eff}} k_B T \gamma_3 g_m R_{eff}$$

(3.32)
Substituting (3.32) to (3.21) and note that the slope of the output voltage at zero crossing is $k = \frac{I_{SS}}{C_{eff}}$, we have

$$L(f_{os})_{white} = \frac{N v_n^2 f_o^3}{k^2 f_o^2} = \frac{2k_B T}{(2NR_{eff}C_{eff}I_{SS} \ln 2)^2} \left( \frac{1}{R_{eff}} + \frac{\gamma_2 g_{m2}}{\pi} + \frac{3\gamma_3 g_{m3}}{4} \right) \cdot \frac{1}{f_o^2} \quad (3.33)$$

### 3.3.2 Flicker Noise Contribution

1/f noise fluctuates at a rate much lower than the oscillating frequency. The dominant source of 1/f noise in the ring-type oscillator resides in M1, which drives the tail current and is amplified in the delay stage. Since fluctuations in each tail current are uncorrelated, the delay variations will accumulate and create significant phase noise. Therefore in our analysis, we only consider the flicker noise caused by the control FET M1. A simplified measurement based flicker noise model for MOSFET devices is given in Section 1.3 Equation (1.7) as

$$S_{n,1/f}(f) = K_f \frac{g_{m2}^2}{f A_f W L C_{ox}^2} \quad (3.34)$$

where $K_f$ and $A_f$ are fitting parameters [37]. A modified unified 1/f noise model is introduced in [10] as

$$S_{n,1/f}(f) = \eta \cdot \frac{I_D^2}{f} \quad (3.35)$$

where $\eta = \frac{k_B T}{W L} \left[ \frac{1}{N_n} + (\alpha + \beta) \mu \right]^2 \rho_t$ describes noise contribution with fluctuations in free carriers $\left[ \frac{1}{N_n} \right]$ and mobility $[(\alpha + \beta) \mu]$. $\alpha$ models Coulomb scattering, $\beta$ surface roughness, $\gamma$ 'tunneling' attenuation, while $\rho_t$ is the gate stack volume trap density.

Through simple circuit analysis, the power spectrum density of the noise current

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modulating $I_{SS}$ becomes

$$S_{I_{SS}}(f) = \eta \cdot \frac{I_{SS}^2}{f} \quad (3.36)$$

In order to find $\kappa$-the sensitivity of the oscillator frequency on the baseband $1/f$ noise current, we need to relate the oscillator frequency with the tail current. We could write

$$f_o = \frac{1}{2Nt_d} = \frac{I_{SS}}{2NC_{eff}V_{swing} \ln 2} \quad (3.37)$$

where $V_{swing} = I_{SS}R_{eff}$ is the output swing. Therefore,

$$\kappa = \frac{\partial f_o}{\partial I_{SS}} = \frac{f_o}{I_{SS}} \quad (3.38)$$

Substituting Equations (3.38) and (3.36) into Equation (3.39), we obtain the phase noise due to flicker noise:

$$L(f_{os})_{\text{flicker}} \approx \kappa^2 S_v(f) \frac{f^2}{4f_{os}^2} = \frac{\eta f_o^2}{4 f_{os}^3} \quad (3.39)$$

### 3.3.3 Numerical Results

Figure 3.9 shows the phase noise in the free running oscillator as well as in the SO system for both analytical and simulated results. Device baseband $1/f$ noise is up-converted to the high frequency regime with a slope of $1/f^3$ (-30dB/dec) while device baseband white noise is up-converted to the high frequency regime with a slope of $1/f^2$ (-20dB/dec). The analytical phase noises for both free running oscillator and SO match well with the simulated results. Also, the SO system reduces the phase noise in the low frequency offset region: 56.5 dB suppression at $\Delta f_{os} = 100$KHz and 36.3 dB suppression at $\Delta f_{os} = 1$MHz.
Figure 3.9: Predicted and simulated phase noise of the delay-line oscillator and the delay-line SO

3.4 Summary

In this chapter, we first characterize MOSFET devices with the measurement and extract some device parameters including the threshold voltage, carrier mobility, effective substrate doping concentration and interface trap density. Then the relationship between the device baseband noise and oscillators’ radio frequency phase noise has been studied. The specific phase noise expression is formulated based on the differential delay-line SO with active inductor loads and a low level signal injection.
The Phase-Locked Loop (PLL) is one of the most important building blocks in mixed-signal circuits. It generates well-timed clocks for various applications such as clock-and-data recovery, clock synchronization, clock regeneration, frequency/phase (de)modulation, frequency synthesizer, etc. The basic concept behind PLLs has been the same since its invention by Henri de Bellescize in the 1930s [59], but the design and implementation of PLLs continue to be refined for high performance systems.

The synchronization of an oscillator under the influence of an injection signal has been studied by researchers. By comparing the oscillator with a high stability reference signal source, injection locking will cause the oscillator to be phase locked to the reference source. Chapter 2 has throughly studied the injection-locked synchronous oscillator (SO). In 1976, Runge [15] firstly applied the SO with reference injection (RI), into a discrete PLL with an analog multiplier PD and LC oscillator for use in Undersea Lightwave Systems, which have been in use since 1988 in the Atlantic Ocean and 1989 in the Pacific Ocean. In the late 1980s, Uzunoglu and White [16,25] studied the low-level operation of a SO and RI into PLL with phase coherency. More recently, Razavi [11] considered the PLL under sinusoidal injection from an external.
interference, and studied the resulting frequency-pulling effect on the sidebands. Reference [33] rigorously analyzed the Local Oscillator (LO) pulling effects in frequency and discrete-time domain on PLL. However, the full potential of RI to improve the noise and settling performance of Charge-Pump PLLs has yet to be analyzed and implemented in an integrated CMOS circuit technology.

This work has applied the low-level injection-locked SO with voltage control capability (VCSO) discussed in Chapter 2 to a modified PLL to replace the conventional Voltage Controlled Oscillator (VCO), as shown in Figure 4.1. Based on Runge’s method [15], the reference signal is not only compared with the VCSO feedback signal, but also injected into the VCSO. Compared to a conventional PLL, the new system, named a Reference Injected PLL (PLL-RI), provides further noise suppression and improved locking behavior. The phase noise shaping functions of a PLL-RI
can be formulated mathematically. PLL-RI provides flexible design trade-offs by decoupling 3dB loop bandwidths for different noise sources.

This chapter starts with a brief introduction on the PLL basics, and then theoretically analyzes the PLL-RI system from the aspects of dynamic equations to study its locking condition and settling behavior, and the phase noise with noise contributions from different sources – reference/injection signal, Phase Detector (PD), and VCSO. Next, the design specifications and the design of each PLL-RI components are described. The system dynamic models and phase noise equations derived are then verified by SPICE and MATLAB simulations. In addition, measurement results on a 1GHz CMOS PLL-RI with injection-locking into a CMOS ring-type VCO, fabricated with 130nm RF CMOS technology, and occupied $100\mu\text{m} \times 200\mu\text{m}$, are provided to support the theories and simulations in this chapter. Finally, applications of PLL-RI are provided, and a special example of using PLL-RI as an integer-N frequency synthesizer is given and tested.

### 4.1 PLL Basics

A PLL is a closed-loop feedback system that causes a particular system to track with another one in phase. More precisely, a PLL is a circuit synchronizing an output signal generated by an oscillator with a reference signal in frequency as well as in phase. In the synchronized (locked) state, the phase error between the oscillator’s output signal and reference signal is zero or a constant. If a phase error builds up, a control mechanism acts on the oscillator in such a way that the phase error is again reduced to a minimum. In such a control system, the phase of the output
signal is locked to the phase of the reference signal. This is why it is referred to as a phase-locked loop [60].

4.1.1 PLL Building Blocks

A basic block diagram of a PLL is shown in Figure 4.2 and consists of four basic functional blocks: a phase detector (PD), a loop filter (LF), a voltage-controlled oscillator (VCO), and a frequency divider (FD).

**Phase Detector (PD)**

A phase detector (PD) compares the phase of the output signal with the phase of the reference signal and develops an output signal $u_d$ which is approximately proportional to the phase error $\theta_e$ within a limited range of the latter:

$$u_d(t) = K_p \theta_e(t)$$  \hspace{1cm} (4.1)

where $K_p$ in V(A)/rad represents the gain of the PD. Figure 4.3(a) is a graphical representation of Equation (4.1). In mixed signal PLLs, mainly four types of PDs are
Figure 4.3: Transfer curves of the (a) PD (b) VCO

Figure 4.4: Block diagram of the PFD with Charge Pump (CP)
used [60]. The first PD in the history of the PLL was the linear analog multiplier. When the PLL moved into digital territory, digital PDs become popular, such as the EXOR gate, the edge-triggered JK-flipflop and the most popular so-called phase-frequency detector (PFD). The main advantage of PFD is that it provides phase acquisition as well as frequency acquisition. A common linear PFD architecture uses two resettable D-Flip-Flops (DFFs) with a AND gate as shown in Figure 4.4. A PFD is usually accompanied by a Charge-Pump (CP) circuitry which is responsible for charging or discharging the loop filter according to the phase information generated by PFD. A PFD/CP can emulate the behavior of the integrator, thus implementing type-II PLLs without a real Opamp-based integrator, so both the design complexity and difficulty are reduced. Figure 4.5(a) shows the waveform of the case where the input phase \(\phi_i\) leads and has a higher frequency than the feedback phase \(\phi_{fb}\). The PFD generates an UP or a DN signal that switches the current of the CP. The DFFs are triggered by the inputs to the PFD. Initially, both outputs are low. When one of the PFD inputs rises, the corresponding output becomes HIGH until the second input goes high which in turn resets the circuit and returns the system to the initial state.

It is easily seen from the waveforms that \(u_d(i_d)\) becomes largest when the phase error is positive and approaches \(2\pi\), and smallest when the phase error is negative and approaches \(-2\pi\). Since the current flows for time duration \(t\) between the two edges, if the period is \(T\), and the charging current is \(I_p\), the average output current can be defined as

\[
\bar{i_d} = I_p \frac{t}{T} = \frac{I_p \theta_e}{2\pi}
\]  

(4.2)
therefore, the gain of the PFD/CP is

\[ K_p = \frac{I_p}{2\pi} \]  

(4.3)

If we plot the average signal \( \bar{r}_d \) versus phase error \( \theta_e \), we get a sawtooth function with a slope of \( K_p \), as shown in Figure 4.5(b). The average output signal of the PFD varies monotonically with the frequency error when the PLL is out of lock. This leads to the term phase-frequency detector. A PLL which uses the PFD will lock under any condition, irrespective of the type of loop filter used. For this reason, the PFD is the preferred PD in PLLs. The PLLs with the use of PFD/CP are usually called Charge-Pump PLLs. We should note that the characteristic shown in Figure 4.5(b) is the ideal case. The non-ideal behaviors such as cycle slip, dead-zone, blind-zone are existing, and the details will be discussed in Section 4.4.1 when we talk about the PFD/CP implementations.
Loop Filter (LF)

A loop filter (LF) is used to cancel the AC component which is superimposed on the DC component inside the output signal $u_d$ of the PD. Because of the integrator provided by the PFD/CP, the passive lead-lag loop filters shown in Figure 4.6 is almost exclusively used in PLLs working with charge pump PFDs. Figure 4.6 (a) is a first-order filter with the transfer function

$$F(s) = \frac{1 + s\tau}{sC} \quad (\Omega) \quad (4.4)$$

where $\tau = RC$, and $s$ is the Laplace operator. Seen from Equation (4.4), the phase-leading action comes from the numerator zero, whereas the denominator pole produces the phase lag. All filters used as loop filters are lead-lag filters. A much more common filter used in Charge-Pump PLLs is the second order filter with one zero and two poles, as shown in Figure 4.6 (b). If the second pole of the LP (third pole of the PLL) is far away from the origin, then we can use Equation (4.4) to approximately derive the overall transfer function of the PLL with second-order LF.
**Voltage Controlled Oscillator (VCO)**

A voltage controlled oscillator (VCO) oscillates at an angular frequency $\omega_{out}$, which is determined by the output signal $V_{ctrl}$ of the loop filter. The angular frequency $\omega_{out}$ is given by

$$\omega_o(t) = \omega_f + K_o V_{ctrl}(t) \quad (4.5)$$

where $\omega_f$ is the free running frequency of the VCO and $K_o$ is the VCO gain in rad/V·s. Figure 4.3(b) is a graphical representation of Equation (4.5). The model of the VCO should yield the VCO output phase $\phi_o$ instead of output frequency $\omega_{out}$. By definition, the phase is given by the integral over the frequency variation in Equation (4.5):

$$\phi_o(t) = \int K_o V_{ctrl}(t) \, dt = K_o \int V_{ctrl}(t) \, dt \quad (4.6)$$

In the Laplace transform, integration over time corresponds to division by $s$, so

$$\frac{\Phi_o(s)}{V_{ctrl}(s)} = \frac{K_o}{s} \quad (4.7)$$

Therefore, for phase signals, the VCO simply represents an integrator. In practical designs, there are two major architecture for the VCO: LC-type VCOs and ring-type VCOs. Details about the implementation of VCOs have been provided in Section 2.1.

**Frequency Divider**

Frequency multiplication is one of the common applications of PLLs. It requires the PLL output to be a multiple of the input frequency. In order to amplify the input frequency, the output signal needs to be divided down before it is fed back to the PD. Therefore, a frequency divider-by-$M$ has to be inserted in the feedback loop. Therefore, when the loop is locked, $\omega_{fb} = \omega_i$, yielding $\omega_{out} = M \omega_i$. Therefore, the
phase transfer function is simply:

\[
\frac{\Phi_{fb}}{\Phi_o} = \frac{1}{M} \tag{4.8}
\]

If the M is an integer number, the PLL is called an integer-M PLL, and if M is a fractional number, the PLL is called a fractional-M PLL. Therefore, the number \( M \) decides the structure of the divider, but the linear analysis is true for both types of PLLs. Details about implementing FD for integer-M PLL applications will be provided in Section 4.6.

Note that frequency multiplication also amplifies the input and PD noise. For example, the magnitude of phase noise components within the 3dB bandwidth of the PLL is multiplied by a factor of approximately \( M \).

### 4.1.2 PLL System Dynamics

Let’s look at the PLL open loop transfer function:

\[
H_{\text{open}}(s) = K_p K_o R \cdot \frac{s + \frac{1}{RC}}{s^2} \tag{4.9}
\]

The transfer function has two poles at the origin and one compensating zero (\( \omega_z = \frac{1}{RC} \)) that guarantees the closed-loop stability. The bode plot of the open-loop transfer function is drawn in Figure 4.7. If a second order LF is used, the resultant third-order PLL open-loop bode plot is also shown. If its third pole (\( \omega_{p3} = \frac{1}{RC_2} \)) is far away from the zero, then up to the unity gain point, the loop behavior of the third-order PLL is close to that of the second-order PLL using the first-order LF. For optimal stability, the third pole is usually 10 times higher than the zero, and \( C_2 \) is less than one-tenth of \( C_1 \) to meet the requirement. In the following analysis, \( C_2 \) is ignored for simplicity but comments will be made when \( C_2 \) makes an impact.
Figure 4.7: Bode diagrams for the open-loop phase transfer function $H_{\text{open}}(s)$ of a second-order PLL (solid line) and a third-order PLL (dashed line)

Figure 4.8: The mathematical model for the locked state of the PLL

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If we assume that the PLL is locked, from the previous discussions, we can develop a linear mathematical model shown in Figure 4.8 to calculate a phase transfer function $H(s)$ of a second-order PLL, which relates the phase $\phi_i$ of the input signal to the phase $\phi_o$ of the output signal:

$$H(s) = \frac{\Phi_o(s)}{\Phi_i(s)} = \frac{H_{\text{open}}(s)}{1 + \frac{H_{\text{open}}(s)}{N}} = \frac{2\omega_n \zeta s + \omega_n^2}{s^2 + 2\omega_n \zeta s + \omega_n^2}$$

(4.10)

where $\omega_n = \sqrt{\frac{K_p K_o}{MC}}$ is the natural frequency and $\zeta = \frac{RC\omega_n}{2}$ is the damping factor. By adjusting $\omega_z$ (through $R$ and $C_1$) and pump current $I_p$, $\omega_n$ and $\zeta$ can be adjusted. We can see from the Bode diagram of this closed loop transfer function drawn in Figure 4.9 (a) that the second-order PLL is actually a low-pass filter for input phase signal. The transfer function is flat between zero and approximately the natural frequency $\omega_n$. This means the second-order PLL is able to track phase and frequency modulations of the reference signal as long as the modulation frequencies remain within an angular frequency band that is roughly between zero and $\omega_n$. The exact bandwidth of a PLL is normally specified by the 3-dB corner frequency $\omega_{3dB}$, which can be found:

$$\omega_{3dB}^2 = \omega_n^2 \left[1 + 2\zeta^2 + \sqrt{1 + (1 + 2\zeta^2)^2}\right]$$

(4.11)

The damping factor $\zeta$ also plays an important role on the dynamic performance of the PLL. The PLL system is critically damped when $\zeta = 1$. If $\zeta$ is less than unity, the transient response becomes oscillatory and has large overshoot. If $\zeta$ is made considerably larger than unity, the transfer function flattens out, and the dynamic response becomes sluggish [60].

For the third-order PLL where another pole is added, Figure 4.9 (a) is not true, and the transfer function for the third-order PLL is plotted in Figure 4.9 (b): as $\zeta$ is much less than 1 (severe under-damping), slow ringing and overshoot are presented,
Figure 4.9: PLL closed-loop phase transfer function Bode diagram for (a) a second-order system (b) a third-order system
same with the second-order PLL; however, as $\zeta$ is much greater than one (severe over-
damping), fast ring and overshoot are presented. The overshooting at high damping
is due to the smoothing pole added by the second capacitor $C_2$ degrades the phase
margin [61].

We need to differentiate the order of the PLL in the above discussions with the
type of the PLL. The order of the PLL system is determined by the number of poles
in the open loop transfer function. Generally, the order of a PLL is always higher
by 1 than the order of the loop filter due to the pole contributed by the VCO. The
type of the PLL is determined by the total number of the integrators in the PLL.
The VCO is an integrator, so if the LF has another integrator, which is the case for
Charge-Pump PLL, then this PLL becomes type-II. If the LF has no integrator, the
PLL is a type-I PLL. Usually higher order filter is needed in the Type-I PLL in order
to reduce the power of the frequency spurs. Another major limitation for the type-I
PLL is it has a finite phase error once it is settled to a frequency step, making it
inappropriate for many applications where zero phase offset is as important as the
accuracy of the phase. For example, if the input frequency is a step function, which
means the input phase is a ramp function,

$$\phi_i(t) = \Delta \omega \cdot t \implies \Phi_i(s) = \frac{\Delta \omega}{s^2} \quad (4.12)$$

where $\Delta \omega$ is the magnitude of the frequency step. Knowing the type-II phase error
transfer function $fH_e(s) = 1 - H(s) = \frac{s}{s+K_pK_oF(s)/N}$, we can find the phase error as

$$\Theta_e(s)_{\text{type-I}} = \frac{\Delta \omega}{s} \frac{1}{s + K_pK_oF(s)/N} \quad (4.13)$$

According to the final value theorem of the Laplace transform:

$$\theta_e(\infty)_{\text{type-I}} = \lim_{s \to 0} s\Theta_e(s)_{\text{type-I}} = \frac{\Delta \omega}{K_pK_oF(0)/N} \quad (4.14)$$

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Figure 4.10: Transient response of a linear second-order PLL to a frequency step applied at $t = 0$ [62]

which will never be zero since $F(0)$ does not have an integrator behavior $\frac{1}{s}$ in it. Type-II PLL does not have this problem. The phase error for type-II PLL with a frequency step input is

$$
\Theta_e(s) |_{\text{type-II}} = \Phi_i(s) \cdot H_e(s) |_{\text{type-II}} = \frac{\Delta \omega}{s^2 + 2\omega_n \zeta s + \omega_n^2} \quad (4.15)
$$

and the final value theorem gives

$$
\theta_e(\infty) |_{\text{type-II}} = \lim_{s \to 0} s \Theta_e(s) = 0 \quad (4.16)
$$

Normalize the phase error to $\frac{\Delta \omega}{\omega_n}$, we get the transient response of the phase error due to the frequency step shown in Figure 4.10 with different damping factors $\zeta$ [62].

It is also interesting to see the type-II PLL’s response to an input frequency ramp function. Therefore, the input phase becomes

$$
\phi_i(t) = \frac{\Delta \omega \cdot t^2}{2} \implies \Phi_i(s) = \frac{\Delta \omega}{s^3} \quad (4.17)
$$

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Figure 4.11: Transient response of a linear second-order PLL to a frequency ramp applied at \( t = 0 \) [62]

where \( \Delta \omega \) is the rate of change of the reference frequency. Performing the same calculations as the preceding ones, we find the final phase error \( \theta_e (\infty) \) is

\[
\theta_e (\infty) = \lim_{s \to 0} s \Phi_i (s) \cdot H_e (s) = \frac{\Delta \omega}{\omega_n^2} \tag{4.18}
\]

 Normalize the phase error to \( \frac{\Delta \omega}{\omega_n^2} \), we get the transient response of the phase error due to the frequency ramp shown in Figure 4.11 with different damping factors \( \zeta \) [62].

For large phase error, the output signal of the phase detector is proportional to the sine of phase error, therefore, Equation (4.18) needs to be modified:

\[
\sin \theta_e (\infty) = \frac{\Delta \omega}{\omega_n^2} \tag{4.19}
\]

Therefore, the maximum rate of change of the reference frequency that does not cause lock-out is \( \omega_n^2 \). A more practical design limit for the maximum frequency rate is \( \omega_n^2 / 2 \) [62].

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4.1.3 Noise in PLLs

As is can be seen from the previous discussion, the signal in the PLL system is the phase, therefore, they are susceptible to phase noise or jitter. If the input signal or the building blocks of a PLL exhibit phase noise, then the output signal will suffer from phase noise. All loop components, including the PD, the LF, the VCO and the down scaler contribute noise. It’s helpful to understand how the spectrum of a given noise source is shaped as it is presented at the output. We consider the input noise $\Phi_{n,i}$, the PD noise $\Phi_{n,pd}$, the LF noise $\Phi_{n,lf}$, and the VCO noise $\Phi_{n,vco}$. Assume these noise sources are uncorrelated, and can be modeled as additive components shown in Figure 4.12.

**Input Noise**

Demonstrated in Figure 4.12, the input noise $\Phi_{n,i}(s)$ travels along the same transfer function as the input signal:

$$H_{n,i}(s) = \frac{\Phi_{n,o}(s)}{\Phi_{n,i}(s)} = \frac{2\omega_n\zeta s + \omega_n^2}{s^2 + 2\omega_n\zeta s + \omega_n^2}$$  \hspace{1cm} (4.20)
Therefore, it is shaped by the characteristic low-pass transfer function of the system when it appears at the output.

**PD Noise**

The phase noise of the PD has the same transfer function as the input noise with a scale of \( \frac{1}{K_p} \):

\[
H_{n,PD}(s) = \frac{\Phi_{n,o}(s)}{\Phi_{n,PD}(s)} = \frac{1}{K_p} \frac{2\omega_n\zeta s + \omega_n^2}{s^2 + 2\omega_n\zeta s + \omega_n^2}
\]  
(4.21)

so the similar low-pass transfer function is applied on the PD phase noise as it is present at the output.

**LF Noise**

The noise transfer function for the LF noise has a band-pass characteristic. The transfer function is represented as

\[
H_{n,LF}(s) = \frac{\Phi_{n,o}(s)}{\Phi_{n,LF}(s)} = \frac{K_o s}{s^2 + 2\omega_n\zeta s + \omega_n^2}
\]  
(4.22)

In the region around the natural frequency \( \omega_n \) of the PLL, the filter noise sufficiently contribute to the overall phase noise.

**VCO Noise**

The VCO phase noise is modeled as an additive component \( \Phi_{n,VCO} \), as shown in Figure 4.12. We can set input phase noise to zero and compute the noise transfer function for the VCO noise if they are uncorrelated:

\[
H_n(s)_{n,i} = \frac{\Phi_{n,o}(s)}{\Phi_{n,i}(s)} = \frac{s^2}{s^2 + 2\omega_n\zeta s + \omega_n^2}
\]  
(4.23)

Even though it has the same poles as the input noise transfer function, it also contains two zeros at the origin, making the characteristic a high-pass filter. Thus, increasing
the bandwidth of the PLL can lower the contribution of the VCO phase noise. However, at the same time, it will include more PD and input noise. It has been shown that the in-band noise (noise inside the loop bandwidth contributed by reference signal, PD) and the out-band noise (noise outside the loop bandwidth contributed mainly by VCO) are equally important for the noise performance, and an optimum noise performance can be achieved by setting the loop bandwidth at the position when these two noises are equal [63].

4.2 PLL-RI System Dynamics

The functional block diagram of the PLL-RI shown in Figure 4.1(a) consists of a Phase Detector (PD), a Low Pass Filter (LPF), and a voltage controlled SO (VCSO). As mentioned in Section 4.1.1, normally, in a PLL, the PD compares the phase difference between the reference and the output signals, and a control mechanism acts on the VCO in such a way that the phase error is reduced to a minimum. In PLL-RI, however, besides the loop phase tracking operation, the VCSO also functions as a tracking device. In general, either of these two mechanisms is sufficient for phase locking; however, they are combined to realize a low phase noise performance and improved locking behavior. In the practical implementation, the injection signal is usually derived from the attenuated reference signal through an attenuator (ATTN) in order to maintain the condition of small signal injection.

As a critical component of a PLL, a PD is a circuit capable of delivering an output signal that is proportional to the phase difference between its two input signals. Many circuits could be applied. Analog multiplier-type PD was used in the early analog PLLs. The Charge-Pump PLL discussed in Section 4.1, is a mixed-signal
(a) Analog PLL-RI

(b) Charge-Pump PLL-RI

Figure 4.13: PLL-RIs with analog multiplier PD and PFD/CP

type and employs a nonlinear discriminator to aid the frequency acquisition, is an improvement over the phase comparator-type early PLLs in that it also provides a frequency error output as well as a phase error, so the PLL capture range is only limited by the VCO working frequency range. It also generates a coherent output phase as the CP together with a passive integrable filter is capable to provide a pole at the origin so as to increase the order of the type of the PLL. This section will first briefly talk about the analog-type PLL-RI, then study in details on the Charge-Pump PLL-RI. The transient and steady-state behavior of the PLL-RI are described by a nonlinear differential equation, which is further studied by the phase-plane method. The nonlinear equation is linearized for the small-signal condition and the s-domain transfer function can be derived.
4.2.1 Analog PLL-RI

To operate a PLL-RI shown in Figure 4.13(a), the VCSO frequency is controlled in two ways: by an injection of the input signal and by the control voltage \( V_{ctrl} \) derived from the multiplier and the loop filter. The resultant VCSO has a new frequency given in Equation (4.5). Assume, for a simplified case where a first order loop filter \( F(s) = 1 + \frac{a}{s} \) is used and the phase detector has a gain of \( K_p \), we can rewrite Equation (4.5) as

\[
\omega_o = \omega_{fo} - K_o K_p \left[ \phi(t) + a \int_{-\infty}^{t} \sin \phi(t) \, dt \right]
\]  

(4.24)

The negative sign in front of the second term in the right hand side is due to the reason that the definition of \( \phi \) in Chapter 2 is \( \phi = \phi_o - \phi_i = -\theta_d \). We can substitute Equation (4.24) into the differential equation (2.23) of the SO system to obtain the loop dynamics of the analog PLL-RI:

\[
\frac{d^2 \phi}{dt^2} + (K_p K_o + K_{SO}) \cdot \cos \phi \cdot \frac{d\phi}{dt} + a K_p K_o \sin \phi = 0
\]

(4.25)

where \( K_{SO} = \frac{\omega_o}{2Q} \frac{\bar{V}_i}{\bar{V}_o} \) in rad/s is the injection parameter. A similar equation can be obtained for a second order PLL with \( K_{SO} = 0 \) [46]. We may eliminate one of the constants by normalizing the time variable. Letting \( t = \tau/K_p K_o \), Equation (4.25) becomes

\[
\frac{d^2 \phi}{d\tau^2} + (1 + K'_{SO}) \cdot \cos \phi \cdot \frac{d\phi}{d\tau} + a' \sin \phi = 0,
\]

(4.26)

where \( K'_{SO} = \frac{K_{SO}}{K_p K_o} \) and \( a' = \frac{a}{K_p K_o} \) are the normalized injection parameter and loop filter corner frequency to characterize the behavior of the VCSO and the remainder of the loop, respectively. Construct a graph of Equation (4.26) in which \( \phi \) is the abscissa and \( d\phi/dt \) is the ordinate in Figure 4.14 where different values of \( K'_{SO} \) and
Figure 4.14: Phase plane trajectory for PLL-RI with multiplier-PD: the lock-in range increases with $K_{SO}$ and $a'$
Figure 4.15: The lock-in range of an analog PLL-RI with multiplier PD increases with $a'$

$a'$ are considered. For the PLL-RI with a multiplier PD and a perfect integrator in the loop filter, the pull-in range is theoretically infinite [46]. However, even though the pull-in range may be infinite, the time required to achieve frequency lock may be prohibitively large if the initial frequency error is large compared with the loop gain. Note, for large values of $\frac{d\phi}{dt}$, the trajectories are practically sinusoids. As the trajectory travels from $(2n - 1)\pi$ to $(2n + 1)\pi$ (where $n$ is an integer), the decay of $\frac{d\phi}{dt}$ becomes larger as $\frac{d\phi}{dt}$ decreases. Until at $\phi = m\pi$ (where $m$ is an odd number), $\frac{d\phi}{dt}$ is within a range where the system will stop skipping cycles, and the frequency difference and phase difference will lock to zero and $2n\pi$, respectively. This range is referred to as half of the lock-in range for the PLL-RI with multiplier PD. From Figure 4.14, we can observe the lock-in range increases as $a'$ increases and their relation is plotted in Figure 4.15. Note, when $A = 0$, the single side lock-in range has the minimum value $K_{SO}$, which is identical to the VCSO single side lock-in range. Also, The PLL-RI ($K_{SO} > 0$) has a wider lock-in range than the conventional PLL
Figure 4.16: Dual loop PLL-RI (phase locked loop and injection loop) phase model for an analog PLL with multiplier PD

\( K_{SO} = 0 \) since the phase plane trajectory of the PLL-RI in one cycle opens wider than that of the PLL. Starting outside the lock-in range, the number of skipped cycles is lower for PLL-RI which implies a reduced acquisition time.

We can build a dual loop phase model for the analog PLL-RI, shown in Figure 4.16, where a conventional phase locked loop and an addition injection loop are observed.

### 4.2.2 Charge-Pump PLL-RI

For a phase frequency detector (PFD), the average output signal of the PFD varies monotonically with the frequency error when the PLL is out of lock. No such characteristic is shown in the multiplier PD. Because the output signal of the PFD depends on phase error in the locked state of the PLL and on the frequency error in the unlocked state, a PLL which uses the PFD will lock under any condition, irrespective of the type of loop filter used [60]. The current output PFD is almost always combined with a passive lead-lag loop filter as shown in Figure 4.13(b). Similar analysis to the analog PLL-RI gives:

\[
\frac{d\phi(t)}{dt} \approx \omega_{lo} + K_o V_c - \omega_i - \frac{\omega_{lo}}{2Q} \frac{V_i}{V_o} \sin \phi(t)
\] (4.27)
From the block diagram shown in Figure 4.13 (b), if we neglect the effect of the second capacitor $C_2$ since its capacitance is much smaller than $C_1$, the time domain control voltage is

$$V_{ctrl}(t) = -K_p R \phi(t) - \frac{K_p}{C_1} \int_{-\infty}^{t} \phi(t) \, dt$$  \hspace{1cm} (4.28)

where $K_p = \frac{I_p}{2\pi}$ is the gain of the PFD/CP and $I_p$ is the amplitude of the current source in the Charge-Pump. If we substitute $V_{ctrl}$ into Equation (4.27) and consider low-level injection:

$$\frac{d^2 \phi}{dt^2} + (K_p K_o R + K_{SO} \cos \phi) \frac{d\phi}{dt} + \frac{K_p K_o}{C_1} \phi = 0$$  \hspace{1cm} (4.29)

The term $K_{SO} \cos \phi$ in Equation (4.29) represents the effect of the injection on the output phase difference. We can eliminate some constants by normalizing the time variable. Letting $t = \frac{\tau}{(K_p K_o R)}$, so that $d\phi/dt = K_p K_o R (d\phi/d\tau)$, and defining $K = K_{SO}/(K_p K_o R)$ and $A = 1/(K_p K_o R \cdot RC_1)$, Equation (4.29) becomes

$$\frac{d^2 \phi}{d\tau^2} + (1 + K \cos \phi) \frac{d\phi}{d\tau} + A \cdot \phi = 0$$  \hspace{1cm} (4.30)

We may construct a phase plane trajectory of Equation (4.30) in which $\phi$ is the abscissa and $d\phi/d\tau$ is the ordinate. Shown in Figure 4.17 is the comparison of the trajectories for PLL-RI with $K > 0$ and the conventional PLL with $K = 0$. Certain observations can be made from the figures:

1. At equilibrium, the steady-state phase error $\phi_{SS}$ is zero when PLL-RI is phase-locked ($d\phi/d\tau = 0$). The same behavior can also only be observed in the analog PLL-RI with perfect integrator type of loop filter, for example, an active PI filter. If a passive RC loop filter is used or if the integrator in a second-order loop is not perfect, then the phase error will be none zero, and its value is
determined by the frequency error and the loop gain. To better understand the property of this equilibrium point, we rephrase the above system as:

\[
\begin{aligned}
\phi' &= d\phi/d\tau \\
(d\phi/d\tau)' &= -(1 + K \cos \phi) (d\phi/d\tau) - A\phi
\end{aligned}
\]  \tag{4.31}

It is easy to see that \((\phi, d\phi/d\tau) = (0, 0)\) is the only equilibrium of the above system, and the Jacobian matrix of the system (4.31) reads

\[
J \left( \phi, \frac{d\phi}{d\tau} \right) = \begin{bmatrix}
0 & 1 \\
K \frac{d\phi}{d\tau} \sin \phi - A & - (1 + K \cos \phi)
\end{bmatrix}
\]  \tag{4.32}

and corresponding eigenvalues can be found:

\[
\lambda_{1,2} = \frac{1}{2} \cdot \left[ - (1 + K \cos \phi) \pm \sqrt{(1 + K \cos \phi)^2 - 4 \left( A - K \frac{d\phi}{d\tau} \sin \phi \right)} \right]
\]  \tag{4.33}

Both eigenvalues have negative real parts, therefore, \((\phi = 0, \ d\phi/d\tau = 0)\) is the stable equilibrium and the global attractor for the system.
Figure 4.18: Numerical result of pull-in time ratios \( \log (t_{PLL}/t_{PLL-RI}) \) at different combinations of initial phase and normalized frequency difference; the PLL-RI settles faster than the PLL in 92% of the combinations.

(2) In comparison with the conventional PLL, the PLL-RI adds nonlinearity in the phase system given in Equation (4.31), therefore, the speed of the convergence of the solution to the equilibrium depends on the initial solutions of the phase difference \( \phi (0) \) and the normalized frequency difference \( d\phi/d\tau (0) \), resulting in a pull-in time difference between the PLL-RI with \( K > 0 \) and the conventional PLL with \( K = 0 \). Practically, we choose \( \phi (0) \in [-2\pi, 2\pi] \), and \( d\phi/d\tau (0) \in [0, 5\pi] \), a pull-in time comparison can then be plotted numerically by calculating at each combination of the initial conditions, the ratio of \( \log (t_{PLL}/t_{PLL-RI}) \) where \( t_{PLL} \) and \( t_{PLL-RI} \) are the pull-in time for the conventional PLL and the PLL-RI, respectively. Figure 4.18 illustrates, for a majority of cases (92%), this ratio is positive, which means the PLL-RI settles faster than the conventional PLL.
Figure 4.19: Dual loop PLL-RI phase models with the injection loop and the phase-locked loop

(3) The pull-in range of the PLL-RI is ideally infinity but practically is limited by the VCSO operating frequency, which is large in a ring-type delay-line VCSO.

We may also derive the expression for the output phase $\phi_{out}$ to have a better understanding of the injection behavior. The output phase becomes

$$\phi_{out} = \phi_{PLL} - \phi_{INJ}$$

$$= \omega_{io} t + K_o \int_{-\infty}^{t} V_{ctrl} (t) \, dt - K_{SO} \int_{-\infty}^{t} \sin \phi (t) \, dt$$

(4.34)
where $\phi_{PLL}(t) = \omega_o t + K_o \int_{-\infty}^{t} V_{ctrl}(t) \, dt$ and $\phi_{INJ}(t) = K_{SO} \int_{-\infty}^{t} \sin \phi(t) \, dt$ represent the instantaneous PLL phase and the instantaneous injection induced phase modulation, respectively. Based on Equation (4.34), the time domain phase in the PLL-RI system can be modeled as shown in Figure 4.19(a), which consists of dual loops, namely the original phase-locked loop and the injection loop. Compare it with the phase model of an analog PLL-RI shown in Figure 4.16, we can see that the only difference in the phase domain is the multiplier PD detects the sine of the phase error (for small phase error, the sine function is replaced by its argument), while the PFD detects the actual phase error. Also, for the multiplier PD, the gain $K_p$ is limited by the reference signal level as it goes close to the power supply rails, while for digital PFD, the gain is only determined by the source/sink current in the charge pump and has no limitation. We can linearize the phase model at the locked state by assuming the phase difference $\phi$ is small with $\sin \phi \approx \phi$. The linearized frequency domain phase model at locked state is shown in Figure 4.19(b), from where the PLL-RI phase-transfer function $H(s)$ becomes:

$$H(s) = \frac{s (K_p K_o R C_1 + K_{SO} C_1) + K_p K_o}{s^2 C_1 + s (K_p K_o R C_1 + K_{SO} C_1) + K_p K_o}$$  

(4.35)

Defining

natural frequency $\omega'_n = \omega_n = \sqrt{\frac{K_p K_o}{C_1}}$

damping factor $\zeta' = \frac{R C_1 \omega_n}{2} + \frac{K_{SO}}{2 \omega_n} = \zeta + \frac{K_{SO}}{2 \omega_n}$

where $\omega_n = \sqrt{\frac{K_p K_o}{C_1}}$ and $\zeta = \frac{R C_1 \omega_n}{2}$ are the natural frequency and damping factor for the conventional PLL shown in Section 4.1.2. The lock range within which a PLL locks in one single beat note between the reference frequency and output frequency.
Figure 4.20: Phase noise model for a PLL-RI

can be found [60] as \( \Delta \omega_L = 4\pi\zeta' \omega_n \), an improvement of \( K_{SO}/2 \) over the conventional PLL.

4.3 PLL-RI Noise Considerations

In this section, we will analyze the phase noise behavior of a PLL-RI under locked condition (\( \Delta \omega = 0 \)). Intuitively, the zero-crossing of the output signal in each period in the time domain is correctly by the low noise reference injection to the oscillator, thereby, reducing jitter accumulation at the output.

In a PLL-RI, the center frequency of the VCSO is changing inside the loop to match the injection reference signal, therefore, \( \Delta \omega = 0 \). Equation (2.49) then indicates the SO overall phase noise can be regarded as a feedback loop, as shown in Figure 2.22(b). Incorporating the PLL-RI phase mechanism given in Figure 4.19 re-casts a model to a dual-loop configuration as shown in Figure 4.20, from where the overall phase noise power spectral density (PSD) can be expressed as

\[
S_{out,n}(\omega_{os}) = H_{osc,n}S_{osc,n} + H_{pfd,n}S_{pfd,n} + H_{ff,n}S_{ff,n} + H_{inj,n}S_{inj,n} \quad (4.36)
\]
where

\[ H_{osc,n}(\omega_{os}) = \frac{s^2}{s^2 + (2\omega_n\zeta + K_{SO})s + \omega_n^2} \]

\[ H_{pfd,n}(\omega_{os}) = \frac{(2\omega_n\zeta s + \omega_n^2)/K_p}{s^2 + (2\omega_n\zeta + K_{SO})s + \omega_n^2} \]

\[ H_{lf,n}(\omega_{os}) = \frac{K_n}{s^2 + (2\omega_n\zeta + K_{SO})s + \omega_n^2} \]

\[ H_{mj,n}(\omega_{os}) = \frac{(2\omega_n\zeta s + \omega_n^2) + K_{SO}s}{s^2 + (2\omega_n\zeta + K_{SO})s + \omega_n^2} \]

showing that the overall phase noise is broken down into three major noise components: the inherent VCSO noise, the PFD/CP noise, the LF noise, and the reference/injection noise. Figure 4.21 displays an added power spectra from each noise source through corresponding noise shaping functions with different \( K_{SO} \). With the introduction of the \( K_{SO} \), the RI results in a noise suppression at lower frequencies as the HPF corner frequency increases, at higher frequencies as the LPF corner frequency decreases, and around the natural frequency as the BPF amplitude decreases, which means that it suppresses more VCSO noise, reference/PFDCP noise, and LF noise, respectively. The same conclusion can be drawn from a noise bandwidth perspective.

The noise bandwidth \( B_n \) is defined as the integral [62]:

\[ B_n = \frac{1}{4\pi} \int_{-\infty}^{\infty} |H(\omega)|^2 \, df \]  \hspace{1cm} (4.37)

The narrower the noise bandwidth, the greater the noise performance of the PLL [60].

**VCSO noise**

The 3dB loop bandwidth for the VCSO noise transfer function \( H_{osc,n} \) from Equation (4.36) is similar to Equation :

\[ \omega_{3dB,osc} = \omega_n \sqrt{2\zeta'^2 - 1 + \sqrt{(2\zeta'^2 - 1)^2 + 1}} \]  \hspace{1cm} (4.38)
Figure 4.21: PLL-RI output phase noise with different injection levels

where $\omega_n$ and $\zeta'$ are defined in Section 4.2.2. We can observe as $K_{SO}$ increases, $\omega_{3\text{dB,osc}}$ increases as well, which means more VCSO noise is suppressed.

Since the VCO noise is high passed, the integral in Equation (4.37) is infinity, however, the effect of far-out VCO noise is not under consideration in the PLL design since it 1) is usually low and 2) could be filtered out easily. If we change the integration limit of $\infty$ to an upper bound frequency $\omega_{up}$, the noise bandwidth for VCO noise is then calculated from Equation (4.37):

$$B_{n,\text{osc}} = \omega_{up} - \omega_n \left[ F(X) \tan^{-1} G(X) + F(-X) \tanh^{-1} G(-X) \right] \quad (4.39)$$

where

$$X \triangleq 2\zeta'^2 - 1$$
Knowing that $\zeta' = \zeta + K_{SO} K_{Z_0}$, since Equation (4.39) is a monotonically decreasing function on $\zeta'$, increasing $K_{SO}$ will decrease the noise bandwidth $B_{n, osc}$. Figure 4.22(a) plots $B_{n, osc}$ versus $\zeta$ as $K_{SO}$ increases, where we can easily see that increasing $K_{SO}$ and $\zeta$ will decrease the noise bandwidth.

**PFD/CP noise**

Usually in a conventional PLL, as shown in Section 4.1.3, noise inside the PFD/CP is low passed as it is shown at the output, therefore, reducing the loop bandwidth to suppress more PFD/CP noise will include more VCO noise in the picture. However, in a PLL-RI, the 3dB loop bandwidth for the PFD/CP noise transfer function $H_{pfd,n}$ from Equation (4.36) is

$$\omega_{3dB,pfd/cp} = \sqrt{-Y + \sqrt{\omega_n^4 + Y^2}}$$

where $Y = K_{SO} \left(1/2K_{SO} + 2\omega_n\zeta\right) - \omega_n^2 (1 + 2\zeta^2)$. As $K_{SO}$ increases, $\omega_{3dB,pfd/cp}$ decreases, which means more PFD/CP noise is suppressed. Therefore, the parameter $K_{SO}$ can decouple loop bandwidths for VCO and PFD/CP to suppress both’s noise at the same time.

The noise bandwidth due to the PFD/CP noise:

$$B_{n,pfd/cp} = \frac{\omega_n}{4K_p^2 \zeta + \frac{K_{SO}}{2\omega_n}} \left(2\zeta + \frac{1}{2\zeta}\right)$$

Thus, $B_{n,pfd/cp}$ is a monotonically decreasing function on $K_{SO}$. Figure 4.22 (b) plots $B_{n,pfd/cp}$ versus $\zeta$ as $K_{SO}$ increases. $B_{n,pfd/cp}$ has a minimum of
\[ B_{n,pfd/cp_{,\min}} = \frac{\omega_n}{2K_p^2} \sqrt{\left(\frac{K_{SO}}{\omega_n}\right)^2 + 1 - \frac{K_{SO}}{2\omega_n}} \] (4.42)

at

\[ \zeta_{,\min} = \frac{1}{2} \sqrt{\left(\frac{K_{SO}}{\omega_n}\right)^2 + 1 - \frac{K_{SO}}{2\omega_n}} \] (4.43)

**LF noise**

Noise inside the LF is band passed through the loop around the natural frequency \(\omega_n\). Shown in Figure 4.21, as \(K_{SO}\) increases, the BPF bandwidth increases slightly, however, the amplitude of the transfer function reduces dramatically. To quantify the total effect, the noise bandwidth due to the LF noise is calculated:

\[ B_{n,lf} = \frac{K_{SO}^2\pi}{4(\omega_n\zeta + \frac{K_{SO}}{2})} \] (4.44)

showing that \(B_{n,lf}\) is a monotonically decreasing function on \(K_{SO}\). Figure 4.22 (c) plots \(B_{n,lf}\) versus \(\zeta\) as \(K_{SO}\) increases. The noise bandwidth is narrowed with \(K_{SO}\) and \(\zeta\).

**Input noise**

Unlike the conventional PLL where the input noise is only low-passed, the input noise of the PLL-RI is also band-passed due to the injection loop. 3dB bandwidth is not sufficient to find its noise dependence on \(K_{SO}\). Therefore, we need to study its noise bandwidth:

\[ B_{n,inj} = \frac{\omega_n}{2} \left(\zeta' + \frac{1}{4\zeta'}\right) \] (4.45)
In order to find its dependence on $K_{SO}$, we can find $\frac{dB_{n,inj}}{dK_{SO}}$:

$$\frac{dB_{n,inj}}{dK_{SO}} = \frac{(K_{SO} + 2\omega_{n}\zeta + \omega_{n})(K_{SO} + 2\omega_{n}\zeta - \omega_{n})}{4(K_{SO} + 2\omega_{n}\zeta)^2}$$ (4.46)

Therefore, when $K_{SO} < \omega_{n}(1 - 2\zeta)$, $B_{n,inj}$ is a monotonically decreasing function on $K_{SO}$, and $K_{SO}$ can dramatically reduce the noise bandwidth. When $K_{SO} > \omega_{n}(1 - 2\zeta)$, $B_{n,inj}$ is a monotonically increasing function on $K_{SO}$. Figure 4.22 (d) plots $B_{n,inj}$ versus $\zeta$ as $K_{SO}$ increases. $B_{n,inj}$ has a minimum of $\frac{\omega_{n}}{2}$ at $\zeta = 0.5 - \frac{K_{SO}}{2\omega_{n}}$.

Since the noise bandwidth is fairly flat in the neighborhood of $\zeta = 0.5 - \frac{K_{SO}}{2\omega_{n}}$, and when $\zeta > 0.5 - \frac{K_{SO}}{2\omega_{n}}$, increasing $K_{SO}$ does not noticeably worsen the noise performance.

From the noise analysis above, $K_{SO}$ has a positive effect on the noise performance of the PLL-RI. Practically, $\zeta$ is chosen between 0.5 and 2 for low period jitter and accurate reference phase tracking [64], and $K_{SO}$ can be optimized for the minimum overall noise bandwidth by changing the injection level and the design of the oscillator. We note, the injection level can not be arbitrarily large to increase $K_{SO}$, otherwise, the criteria of the small signal injection ($\frac{\bar{V}_{i}}{V_{o}} \ll 1$) is violated and the injection will tend to quench the output amplitude.

### 4.4 PLL-RI Implementation and Numerical Results

To further illustrate the utility of the theory discussed in Sections 4.2 and 4.3, a fully integrated PLL-RI with ring-type, delay-line, VCSO has been designed. Figure 4.23 illustrates the block diagram of the proposed Charge-Pump PLL-RI. A PFD formed by True-Single-Phase-Clock (TSPC) dynamic DFFs is used for high frequency operation, and is followed by a charge pump filter to produce the VCSO control voltage. In the LPF design, all the passive components are implemented with on-chip
(a) VCO NBW decreases with increased $K_{SO}$

(b) PFD/CP NBW decreases with increased $K_{SO}$

(c) LF NBW decreases with increased $K_{SO}$

(d) Input NBW decreases with increased $K_{SO}$ when $K_{SO} < \omega_n (1 - 2\zeta)$

Figure 4.22: The normalized noise bandwidth (NBW) of a second-order PLL-RI as a function of the damping factor $\zeta$ for different $K_{SO}$
elements. The detailed VCSO design is shown in Figure 2.23, which employs a current mirror as a voltage to current converter (V2I) and a two-stage current controlled delay-line oscillator to achieve a wide operating frequency range and a minimum chip area. The output signal of the VCSO passes through a low-to-full swing amplifier and feeds back to the PFD. The design of each PLL-RI component is discussed in the following subsections.

### 4.4.1 Phase-Frequency Detector (PFD)

The PFD shown in Figure 4.4 is commonly used in the PLL for simultaneous phase and frequency acquisition. Generating high frequency clock increases the difficulty of the design of the PFDs particularly for systems in our study with high input clock frequency and minimum frequency multiplication.
Figure 4.24: PFD Implementations (a) Static PFD (b) Dynamic PFD (c) NOR gate used in (b)
Figure 4.24 (a) gives a widely used static PFD design using NAND-based latches to build the DFF. Due the large number of gates it used in the forward path, it has a large dead zone where the small phase error cannot be detected properly. Figure 4.25 explains the reason for dead-zone: if the phase difference is small, the output pulses may not be able to activate the CP completely, yielding a zero PD gain and loop gain, and the loop is basically open and the PLL noise is the same as a free running VCO noise. Delay can be added at the reset path to avoid this issue, however, the reset path already includes one 2-input NAND, one 4-input NAND and two 3-input NANDs, therefore adding more delay will limit the operating frequency, giving rise to the problem of blind zone.

The behavior of blind zone is illustrated in Figure 4.26 where the reference signal REF leads the feedback signal FB and causes an UP output. As the input phase difference approaches $2\pi$, the next REF leading edge arrives before the DFFs are reset due to the finite reset delay. The reset overrides the new REF edge and does...
not activate the UP output. This effect appears as an output having an opposite sign as compared to what is supposed to be for phase difference higher than $2\pi - \Delta$ or lower than $-2\pi + \Delta$. $\Delta$ depends on the reset path delay $t_{\text{reset}}$ and the input reference period $T_{\text{ref}}$, and is equal to $2\pi \frac{t_{\text{reset}}}{T_{\text{ref}}}$. During acquisition, the non-ideal PFD gives the wrong information periodically to prevent the frequency monotonically approaching the lock-in range. Therefore, the acquisition slows down and this error information is determined by $\Delta$. Normally, at an input frequency where $\Delta$ equals $\pi$ ($T_{\text{ref}} = 2t_{\text{reset}}$), the PFD outputs the wrong information half the time and therefore fails to acquire frequency lock unconditionally. The maximum operating frequency of the PFD can then be expressed as

$$f_{\text{max}} = \frac{1}{2t_{\text{reset}}}$$

Note that $t_{\text{reset}}$ is determined by the delay of the logic gate in the reset path and is not a function of frequency.

In the proposed PLL-RI design, we use True-Single-Phase-Clock (TSPC) dynamic DFFs and a NOR gate to implement the PFD, as shown in Figure 4.24 (b)(c). On one hand, the signal passes less gate for a high speed; on the other hand, the NOR gate can provide some delay to reduce the dead-zone. The operations of this PFD are very simple: when the input signal (REF) and the reset signal (RESET) are both low, node A is charged up to VDD though MP1 and MP2. At the rising edge of the signal, node B is connected to ground though MN2 and MN3, yielding the output signal (UP) to be HIGH due to the inversion. Then after that, node B is not affected by the input signal since charges at node A turn off MP3 and prevent node B from pulled up. Therefore, the output is always high after the rising edge of the input signal. When RESET is applied, node A is discharged to ground through MN1, and
node B is pulled up though MP3, causing output UP signal to reset. The RESET signal is asserted when the second DFF input signal (FB) experiences a rising edge. Figure 4.27 plots the simulated waveform for signals in the proposed PFD. When the PFD collects two rising edges the REF and FB, the NOR gate will assert the RESET signal and reset the output signals. The PFD is a 4-state PFD since it has a state when the outputs are both high. The width of the reset pulse is determined by the delay in the NOR gate. The effect of this delay on the maximum operating frequency is discussed in the following subsection. In the design, the NOR gate has a delay of approximately 300ps, and the PFD is running at 1GHz, so the criteria in Equation (4.47) is still met.
4.4.2 Charge-Pump (CP)

The Charge-Pump (CP) is used to sink and source current into a loop filter. When the rising edge of the reference input REF leads that of the VCO feedback input FB, the PFD output UP is high and the CP delivers charges to the capacitors in the loop filter. Thus, the loop filter output voltage increases and so does the VCO output frequency. Therefore, the CP together with the PFD transfer phase difference into current. Figure 4.28 shows the implementation of the CP used in the work. It employs the source switching to remove the issue of charge sharing and charge injection in the MOS switches, and it reduces the effect of clock feedthrough as well. When the load voltage VLOAD is equal to the biasing voltage VB, the pump-up current $I_{up}$ is equal to the pump-down current $I_{dn}$. When VLOAD deviates from VB, the difference between $I_{up}$ and $I_{dn}$ increases due to the channel length modulation. In order to reduce
the mismatch between the two currents, the VB is biased to be close to the control voltage $V_{ctrl,o}$ which sets the VCO to the desired frequency $f_o$. Figure 4.29 plots the simulated current matching characteristic when sweeping the load voltage. According to Figure 2.29, if the desired VCSO frequency is set to be 1GHz, the control voltage is at 0.7V. At the load voltage of 0.7V, $I_{dn} = 50.1\mu A$ and $I_{up} = 49.8\mu A$, giving the current mismatch to a minimum value of 0.6%. Combine the PFD with the CP, and provided that the CP current $I_p$ is selected to be 50$\mu A$, we are then able to simulate the transfer curve of the PFD/CP as shown in Figure 4.30(a). The gain is then plotted in Figure 4.30(b) by taking the derivative of the output signal with respect to the input signal in Figure 4.30(a). The simulated gain is close to the desired value of $\frac{I_p}{2\pi} = \frac{50\mu A}{2\pi}$. As can be seen from Figure 4.30(a), due to the delay of the reset path, the linear range is less than $4\pi$, and created the blind zone. Figure 4.30(a) shows
Figure 4.29: Charge-Pump current matching characteristics

Figure 4.30: PFD/CP (a) transfer characteristics (b) gain
that $\Delta \approx 0.75\pi$ satisfies the locking condition. We note that the blind zone is larger than the reset delay found in Figure 4.27. This is because, in practice, the blind zone consists of not only the reset delay $t_{\text{reset}}$, but also the precharge time of the internal nodes $t_{\text{pch}}$ [65]. When $t_{\text{reset}}$ is reduced to several hundred ps, the necessary precharge time occupies a large portion of the blind zone and cannot be ignored.

### 4.4.3 Loop Filter (LF)

The output of the CP consists of a number of terms in current. In the locked state of the PLL-RI, the first of these is a DC component that is roughly proportional to the phase error; the remaining terms are the unwanted AC components and are filtered out by the loop filter. The loop filter also converts the current signal to the voltage signal. The second-order passive lead-lag loop filter shown in Figure 4.6(b) is used to reduce the periodical ripple caused by the noncontinuous CP. The capacitance of $C_2$ is less than one tenth of the first capacitor $C_1$ to ensure stability.

### 4.4.4 Voltage Controlled Synchronous Oscillator (VCSO)

The PLL-RI uses the same VCSO design as shown in Section 2.7.

### 4.4.5 Closed Loop Simulation Results

The PLL-RI is designed to output a signal at 1GHz. Choosing the 3dB loop bandwidth $\omega_{3dB}$ to be $2\pi \times 20$MHz, damping factor $\zeta$ to be 1, and Charge-Pump current $I_p$ to be $50\mu A$, and knowing the VCSO gain from Figure 2.29 to be $2\pi \times 1.5$GHz/V, according to Equations (4.10) and (4.3), the values for the filter components can be decided to be $R = 1.2K\Omega$, $C_1 = 35\mu F$ and $C_2 = 2pF$. 

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First of all, transient simulation is run on the PLL-RI. Figure 4.31 shows the transient PLL-RI output signal compared to the reference signal. Once the system is locked, PLL-RI output tracks and phase aligned with the reference signal. The transient simulation results in Figure 4.32 compared the control voltage settling behavior of the PLL-RI with and without injection. The initial control voltage at the start-up is set to be 0.55V, from where the initial condition is calculated as \((\phi, d\phi/dt) = (0, 288\text{MHz} \times 2\pi)\). The pool in Figure 4.18 gives the ratio between the two settling time is 1.9, which is comparable to the simulated locking time ratio shown in Figure 4.32.

The PLL-RI phase noise comparison between the theory in Section 4.3 and the simulation is given in Figure 4.33 where the open loop (OL) phase noise of the VCSO, reference signal, and PFD/CP mapped to the VCSO frequency are also plotted. Unlike the previous transistor-level simulations in Section 4.4, the PLL-RI phase noise simulation has the VCSO and passive components as actual devices, but the
Figure 4.32: Transient settling behavior of the control voltage in PLL-RI and PLL: PLL-RI settles faster than the PLL

Figure 4.33: PLL-RI phase noise comparison between theory implemented by MATLAB and SPICE simulation for different levels of injection
PFD/CP is implemented with Verilog-A behavior model in order to vary its noise contribution, and the phase noise is found from the transient noise simulation. In the PLL without injection, the actual simulated noise around the offset of 10MHz peaks due to the nonlinear response of the PLL with the parasitic modeling. The PLL-RI with injection helps to suppress the noise around this region and the strength of the suppression is determined by the injection levels. The theoretical phase noise for PLL-RI with different injection levels ($K_{SO}$) matches with the corresponding simulated results. Shown in Figure 4.33, and calculated with Equations (4.38) and (4.40), the loop bandwidth for PFD/CP noise is reduced from 18MHz in a conventional PLL with $K_{SO} = 0$ to 0.95MHz in a PLL-RI with $K_{SO} = 47MHz$, and the loop bandwidth for oscillator noise is increased from 11MHz in a conventional PLL with $K_{SO} = 0$ to 60.44MHz in a PLL-RI with $K_{SO} = 47MHz$.

4.5 PLL-RI Experimental Results

Figure 4.34 shows the final layout of the PLL-RI with the topology shown in Figure 4.23. It is fabricated with GlobalFoundries standard 130nm RF CMOS process with the core size of 100$\mu$m×200$\mu$m. Measurements were performed on this 1GHz PLL-RI, shown in Figure 4.35. This prototype PLL-RI is measured with a Cascade Probe test system which consists of a RF probe station, ground-signal-ground (GSG) coplanar RF probes, and high-speed cables. The detailed test set-up is shown in Figure 4.36 and discussed in details in Appendix B. A power splitter is used to split the pulse input from the RF signal generator to feed to both the injection port with an attenuator and the reference port. The pulse power is attenuated by 3dB after the power splitter. A 1.2V battery is employed to supply power to the chip with a low
Figure 4.34: Layout of the PLL-RI
Figure 4.35: Die photo of the 1-GHz PLL-RI fabricated in 130nm RF CMOS. The core size of the 1GHz PLL-RI is 100µm × 200µm

Figure 4.36: PLL-RI measurement setup. The noise injection into the PLL-RI is determined by the Pulse Generator.
noise solution. A 50Ω variable resistor is used to provide the variable charge pump current.

The PLL-RI has a 1.2V power supply and operates from 0.5 to 1.7GHz, consuming 2.6mW power at 1GHz. The lock in range of the PLL-RI is the same as the operating range for the VCSO, whose measured transfer characteristic is shown in Figure 2.29 which matches well with the typical corner simulation.

The measured output signal and phase noise at 1GHz are shown in Figure 4.45. The PLL-RI reduces the phase noise and jitter peaking in the vicinity of the designed loop bandwidth, which is around 18MHz in this example but can be optimized for a particular application. The strength of the noise reduction is dependent on the injection constant $K_{SO}$ which is proportional to the intensity of the injection power. With a 10dB attenuation, we also have applied the transfer functions (4.36) directly on the measured phase noise of each components, and plotted a theoretical PLL-RI output phase noise which agrees with the measurement. With a 20dB attenuation, Equations (4.38) and (4.40) indicate the 3dB loop bandwidths for inherent oscillator noise and PFD/CP noise is changed from 11MHz and 18MHz respectively in a conventional PLL with $K_{SO} = 0$, to 78.6MHz and 0.7MHz respectively in a PLL-RI with $K_{SO} = 65$MHz. Same results could be observed from Figure 4.45 where loop bandwidths are decoupled for different types of noise sources: compared with a conventional PLL, for PFD/CP and input noises, the 3dB loop bandwidth is reduced by around 14dB, and for oscillator inherent phase noise, the bandwidth is increased by 8.5dB. When a 30dB attenuation is applied, phase noise at 1MHz and 10MHz offset are reduced from -118.8dBc/Hz (PLL) to -121.9dBc/Hz (PLL-RI), and -102.3dBc/Hz (PLL) to -128.3dBc/Hz (PLL-RI), respectively, with an integrated RMS jitter from
Figure 4.37: Measured PLL-RI (a) output spectrum and (b) phase noise (filtered) of PLL-RI with different attenuation levels. Prediction on the PLL-RI phase noise with 10dB ATTN is also plotted.
Table 4.1: PLL-RI Performance Summary

<table>
<thead>
<tr>
<th>Technology (nm)</th>
<th>130</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply (V)</td>
<td>1.2</td>
</tr>
<tr>
<td>VCO Topology</td>
<td>Ring-type VCSO</td>
</tr>
<tr>
<td>Frequency Range (GHz)</td>
<td>0.5-1.7</td>
</tr>
<tr>
<td>Phase Noise @ 1MHz (dBc/Hz)</td>
<td>-121.9</td>
</tr>
<tr>
<td>Phase Noise @ 10MHz (dBc/Hz)</td>
<td>-128.3</td>
</tr>
<tr>
<td>RMS Phase Jitter (ps)</td>
<td>1.55</td>
</tr>
<tr>
<td>Integrate Range (MHz)</td>
<td>0.01-30</td>
</tr>
<tr>
<td>Power (mW)</td>
<td>2.6</td>
</tr>
<tr>
<td>Area (mm²)</td>
<td>0.02</td>
</tr>
<tr>
<td>FoM* (dB)</td>
<td>-232.0</td>
</tr>
</tbody>
</table>

\[
*\text{FoM} = 10 \log \left( \frac{(\text{RMS Jitter})}{1s} \right)^2 \left( \frac{\text{Power}}{1\text{mW}} \right) \text{ dB}
\]

10KHz to 30MHz of 1.55ps. Table 4.1 summarizes the specifications and the performance of the PLL-RI.

4.6 PLL-RI Applications

The PLL-RI discussed in Sections 4.2-4.5, without a frequency divider in the feedback path, and uses the first-harmonic SO, tends to focus on applications where the output is designed to track the input signal, such as de-skewing, clock synchronization, carrier/clock recovery circuit in high speed communication systems, clock regeneration [15], frequency/phase (de)modulation, and adaptive bandpass filter for low power applications, etc. The theory formulated in Sections 4.1.2 and 4.3 can be extended to use in an integer-M frequency synthesizer where a divide-by-M is employed in the feedback loop, as discussed in Section 4.1, with the aid of a pulser-enabled sub-harmonic injection. The concept of sub-harmonic injection has been given in Section 2.2. A pulser formed by an inverter and a AND gate is usually employed as the non-linear
block shown in Figure 2.12. Shown in Appendix D, the pulse wave with amplitude $A$ and duty cycle $D$ has the $n$th harmonic of the amplitude $2AD$, assuming $nD \ll 1$. Figure 4.38 illustrates this concept. If the Nth harmonic has enough amplitude, then $K_{SO}$ is substantial to let the oscillator lock to the Nth harmonic, and enables the frequency multiplication. Consider now a complementary case where $\omega_i \gg \omega_o$ shown in Figure 2.12 (b), the oscillator will finally lock at the frequency $\frac{\omega_i}{|1+k|}$. We say the oscillator is super-harmonic injection locked and it acts as a frequency divider.

We use the concept of the sub-harmonic SO shown in Figure 2.12 (a), and apply it in a PLL-RI with a divide-by-M in the feedback path to form a sub-harmonic PLL-RI as a frequency synthesizer, shown in Figure 4.39. The dynamic locking behavior and phase noise in the sub-harmonic injected PLL-RI can be analyzed similar to the work shown in Sections 4.2 and 4.3. The PLL-RI noise transfer functions for VCO noise, PFD/CP noise, and reference/injection noise can be found:

$$H_{osc,n} (\omega_{os}) = \frac{s^2}{s^2 + (2\omega_n \zeta + K_{SO})s + \omega_n^2} \quad (4.48)$$
Figure 4.39: Simplified system block diagrams for a conventional synthesizer and a PLL-RI synthesizer

\[
H_{\text{pfd}, n}(\omega_{\text{os}}) = \left| \frac{M (2\omega_n\zeta s + \omega_n^2)/K_p}{s^2 + (2\omega_n\zeta + K_{SO}) s + \omega_n^2} \right|^2 \tag{4.49}
\]

\[
H_{\text{inj}, n}(\omega_{\text{os}}) = \left| \frac{M (2\omega_n\zeta s + \omega_n^2) + K_{SO} s}{s^2 + (2\omega_n\zeta + K_{SO}) s + \omega_n^2} \right|^2 \tag{4.50}
\]

where \(\omega_n = \sqrt{\frac{K_p K_o}{M C_1}}\), and \(\zeta = \frac{R C_1 \omega_n}{2}\) are the natural frequency and damping factor for the conventional PLL-based synthesizer.

The implementations of the building blocks PFD/CP and VCSO are the same with the ones shown in Section 4.4. The divide-by-M Frequency Divider (FD) is implemented with cascading of several fast TSPC DFFs as shown in Figure 4.40 where \(M\) is equal to 4 by cascading two DFFs. The schematic of each TSPC DFF is shown in Figure 4.41. Figure 4.42 shows the simulation result of this divide-by-4 FD. The input frequency is 1GHz, and the output frequency is 250MHz.
Figure 4.40: 2-stage cascaded frequency divider M=4

Figure 4.41: Implementation of TSPC DFF
Figure 4.42: Simulated waveform of the divide-by-4 FD

Figure 4.43: Schematic of the PLL-RI based frequency synthesizer
Figure 4.43 shows the final schematic of the PLL-RI based frequency synthesizer. It is fabricated with GlobalFoundries 130nm CMOS technology with a core size of 0.1mm x 0.2mm. Measurements were performed on this 1GHz PLL-RI synthesizer with a reference signal of 250MHz, shown in Figure 4.44. The measured 1GHz synthesizer output signal and phase noise are shown in Figure 4.45. The PLL-RI synthesizer reduces the phase noise and jitter peaking in the vicinity of the originally designed loop bandwidth, which is around 10MHz in this example but can be optimized for a particular application. The strength of the noise reduction is proportional to the intensity of the injection power. When a 30dB attenuation is applied, phase noise of the PLL-RI synthesizer at 1MHz and 10MHz offset are reduced by 9.4dB and 16.5dB, respectively, with an integrated RMS jitter from 10KHz to 30MHz of 0.84ps. Table 4.2 summarizes the performance comparison of this work with prior art. This
Figure 4.45: Measured PLL-RI output spectrum and phase noise: noise suppression observed around the loop bandwidth

research achieves comparable noise performance with LC type synthesizer, but uses a much smaller chip area and features the lowest power consumption.

It is also interesting to compare the PLL-RI based frequency synthesizer with a Multiplying Delay-Locked Loop (MDLL)-based frequency synthesizer [68]. A DLL, where a Voltage Controlled Delay-line (VCD) is used to replace the VCO, does not accumulate jitter after cycles, thus has superior jitter performance than a conventional PLL. A MDLL overcomes the regular DLL’s major limitation of the difficulty to implement clock multiplication by utilizing a frequency divider by M and a multiplexer as well as logics to remove any accumulated jitter over the past M-1 cycles. It shares the similar idea with the PLL-RI based clock multiplier to periodically clean the accumulated jitter. However, a MDLL requires a novel phase comparator design and
Table 4.2: Frequency Synthesizer Performance Comparison with Previous Work

<table>
<thead>
<tr>
<th></th>
<th>This Work</th>
<th>[66]-ISSCC</th>
<th>[67]-ISSCC</th>
<th>[46]-1st RI</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology (nm)</td>
<td>130</td>
<td>65</td>
<td>45</td>
<td>discrete</td>
</tr>
<tr>
<td>Supply (V)</td>
<td>1.2</td>
<td>0.9</td>
<td>1</td>
<td>N/A</td>
</tr>
<tr>
<td>VCO Topology</td>
<td>Ring-type</td>
<td>LC-type</td>
<td>Ring-type</td>
<td>LC-type</td>
</tr>
<tr>
<td></td>
<td>VCSO</td>
<td>ILCM</td>
<td>VCO</td>
<td>SO</td>
</tr>
<tr>
<td>Freq. (GHz)</td>
<td>0.5-1.7</td>
<td>6.8-8.3</td>
<td>2.0-3.0</td>
<td>0.05</td>
</tr>
<tr>
<td>Phase Noise @ 1MHz (dBc/Hz)</td>
<td>-120.7</td>
<td>-115.0</td>
<td>-113.8</td>
<td>N/A</td>
</tr>
<tr>
<td>Phase Noise @ 10MHz (dBc/Hz)</td>
<td>-122.7</td>
<td>-128.5</td>
<td>-116.3</td>
<td>N/A</td>
</tr>
<tr>
<td>RMS Jitter (ps)</td>
<td>0.84</td>
<td>0.25</td>
<td>0.97</td>
<td>N/A</td>
</tr>
<tr>
<td>Range (MHz)</td>
<td>0.01-30</td>
<td>0.01-30</td>
<td>0.001-200</td>
<td>N/A</td>
</tr>
<tr>
<td>Power (mW)</td>
<td>2.6</td>
<td>3.25</td>
<td>4</td>
<td>N/A</td>
</tr>
<tr>
<td>Area (mm²)</td>
<td>0.02</td>
<td>0.27</td>
<td>0.015</td>
<td>N/A</td>
</tr>
<tr>
<td>FoM* (dB)</td>
<td>-238.0</td>
<td>-247.0</td>
<td>-234.1</td>
<td>N/A</td>
</tr>
</tbody>
</table>

*FoM = 10 log \left[ \left( \frac{\text{RMS Jitter}}{1s} \right)^2 \left( \frac{\text{Power}}{1mW} \right) \right] \text{dB}

careful attention to the design of the selection and multiplexing logics to reduce the phase mismatch of the reference clock and feedback clock, whereas a PLL-RI needs a careful design to ensure the VCO tuning frequency is within the lock-in range of the harmonics of the reference signal. A PLL-RI has advantages of not only corrects the accumulation jitter in the VCO, but also suppresses phase noise in the phase detector, loop filter, frequency divider, and even the reference signal (when $K_{SO}$ is carefully designed as shown in Figure 4.22(d)), and consumes less power than the MDLL.

4.7 Summary

This chapter first discussed the basic concept behind phase locking, and in particular, a Phase-Locked Loop (PLL). The operation of each PLL component and noise
shaping behavior of different noise sources are briefly explained and these basics provide a foundation to understand the design of the Reference Injected PLL (PLL-RI). Then the PLL-RI is theoretically evaluated. The dynamic behavior including the settling time, lock in range, and the phase noise performance of the PLL-RI are studied. A PLL-RI system has been designed and fabricated with 130nm standard RF CMOS technology. The simulated and measured results indicate excellent correlation between the analysis and the fabricated PLL-RI system. Compared with the conventional PLL, the PLL-RI offers faster settling time, wider lock in range and the ability to decouple loop bandwidths for VCO noise, reference noise, LF noise, and PFD/CP noise, so that noise reduction is observed. When a 20dB attenuation is applied in the measurement, compared with a conventional PLL, the 3dB loop bandwidth for the VCO noise is increased by 8.5dB, but the 3dB loop bandwidth for the PFD/CP noise is reduced by 14dB. When a 30dB attenuation is applied, at the 10MHz offset from 1GHz carrier frequency, the phase noise is reduced by 26dB in a PLL-RI. Finally, applications of PLL-RI are provided and a special application of using PLL-RI as a frequency synthesizer is proposed and studied.
Chapter 5: Conclusions

This dissertation has theoretically evaluated the injection locking phenomenon in oscillators and Phase-Locked Loops (PLLs). The analysis shows good agreement with the simulation and experimental results obtained from the fabricated Voltage Controlled Synchronous Oscillator (VCSO) and Reference-Injected PLLs (PLL-RIs). We have also characterized the device baseband behavior, and up-convert the device baseband noise to the oscillator output as high frequency phase noise. In this chapter, conclusions of research presented in the dissertation will be discussed. In addition, recommendations will be suggested for future work of injection locking applications.

5.1 Summary of Research

Phase-Locked Loops (PLLs) are widely used to generate well-timed on-chip clocks in high-performance communication systems. Any timing jitter or phase noise in PLLs significantly degrades the performance of these systems. This is especially a case as the operating frequency increases. Oscillators are considered as the main components in all of the PLL circuitries. As an oscillator based phenomenon, the injection locking is proved to be very useful and has gained considerable attention over the years.

This research has rigorously analyzed the low-level injection locking in an oscillator to form a Synchronous Oscillator (SO) and derived unified phase and phase noise
models for on-chip LC-type SOs, and ring-type SOs. A first order ordinary differential
equation to describe the phase signal inside the SO is derived, and we arrive at
the conclusion that a SO is basically a first-order PLL. However, it alleviates the
needs for the other PLL building blocks and the feedback loop implementation. The
study of the SO phase noise indicates that the inherent oscillator noise is high pass
filtered (HPF) as it is presented at the SO output. The 3dB bandwidth of the HPF
increases with the injection constant $K_{SO}$ to suppress more oscillator noise. A voltage-
controlled SO (VCSO) has been designed with a 2-stage delay-line ring-type oscillator
and fabricated with 130nm RF CMOS process. It has a center frequency at 1GHz and
occupies 100$\mu$m×50$\mu$m chip area. The measurement of the SO shows the potential
of the SO in noise suppression for on-chip applications.

In addition, based on the analysis and measurement of the VCSO, the research
studies a PLL system under Reference Injection (RI). A second order phase differential
equation is formulated for the Charge-Pump PLL-RI, and the dynamic behavior of
the PLL-RI including the settling time, lock in range, etc., are studied. A dual loop
(phase-locked loop and injection loop) phase model is proposed, and based on this
model, phase noise shaping functions for major noise sources in a PLL were derived:
VCO inherent noise, injection (reference) clock noise, loop filter noise, and phase
detector noise. A PLL-RI system has been designed and fabricated with 130nm
RF CMOS technology. The simulated and experimental results indicate excellent
correlation between the analysis and the fabricated PLL-RI system. Compared with
the conventional PLL, the PLL-RI offers faster settling time, wider lock in range and
the ability to decouple 3dB bandwidths for VCO noise, reference noise, and PFD/CP
noise, so that an optimum noise performance can be achieved. The research has also
extended the theory to the sub-harmonic PLL-RI, and implemented a PLL-RI based integer-4 frequency synthesizer. The measurement results show noise suppression around the designed loop bandwidth due to the reason that the injection decouples loop bandwidths for different noise sources.

In the device baseband, the threshold voltage, substrate doping densities, effective mobility, and interface trap densities are extracted from the measurement. Finally, device baseband noise is studied with a focus on the low frequency noise (LFN). The LFN is conventionally thought to be caused by the traps at the oxide interface, whose time constants are widely distributed depending on the trap depth from the interface. The relationship between the device baseband noise and oscillators’ radio frequency phase noise is then proposed. Baseband thermal noise is up-converted to high frequency region through the link between the phase noise and jitter. LFN modulates the oscillator with random FM signal, so it is up-converted to phase noise from the definition of the FM signal. The up-conversion model is validated through simulation on the designed delay-line ring-type oscillator.

5.2 Recommendations for Future Research

Analysis and understanding of the injection locking phenomenon on the oscillators and PLL-RIs considering modulated injections can be beneficial for its use in frequency/phase (de)modulators, and synchronous amplifiers. The unified phase models on SO and PLL-RI presented in this research need to be modified and extended based on the modulation schemes on the injection signal. Usually the injection should be angle-modulated, such as phase-modulated (PM) or frequency-modulated (FM) signals. For the amplifier application, basically, the injection frequency $\omega_i$ is
not a constant anymore but will vary with time as $\omega_i(t) = \omega_i + \frac{d\phi_i(t)}{dt}$. Therefore the differential phase becomes $\phi(t) = \phi_o(t) - \phi_i(t)$. Once a instantaneous frequency of a low-level injection signal conforms to the synchronization condition, the oscillator will be injection-locked and synchronized, and the SO output can be regarded as an amplified version of the modulated injection signal. The transfer characteristics are shown in Fig. 2.19.

It is also worthwhile to study and measure the injection signal transfer characteristic S21 in the PLL-RI. As anticipated, in the PLL-RI, the center frequency in Figure 2.19 will change through the loop operation to the injection frequency, leaving the S21 phase to be 0 since the steady state phase error is $\phi_{ss} = \sin^{-1}\left(\frac{\Delta\omega}{K_{SO}}\right)$. Thus, a very unique transfer function can be observed as shown conceptually in Figure 5.1.
where the phase is constant throughout the tracking range. This behavior gives rise to a special application of the PLL-RI as a bandpass filter with no phase shift.

Additionally, although the effectiveness of the PLL-RI prototype has been proven from the measurements, however, there are still some improvements that can be integrated into the PLL-RI: 1) a fully integrated PLL-RI system needs to be implemented with the on-chip generation of the charge-pump current, and load biasing voltage; the injection work also needs to be done “internally” on the chip. The PLL-RI offers the possibility to design a PLL with an adaptive loop bandwidth by self-adjusting the power of the injection signal with on-chip programmable RF attenuators. 2) a voltage regulator or two will be useful to provide stable, PVT-insensitive, clean power-supply for PLL-RI. 3) the performance of the circuits needs to be validated for deep-submicron technologies less than 90nm and low voltage conditions. Understanding and overcoming scaling and low voltage limitations used in the PLL are very interesting area. The design of PLL components will require innovative design techniques to maintain the desired performance with scaling. Moreover, conceptually super-harmonic and sub-harmonic SOs can be combined together in a PLL-RI to form a fractional-N frequency synthesizer, although the detailed implementation needs more thought.

Finally, Digital PLL (DPLL) has been a very popular topic in recent years. It replaces process and noise-sensitive analog circuits with digital equivalents: PFD/CP with Time-to-Digital Converter (TDC), analog loop filter with discrete-time digital filter, VCO with digital-controlled oscillator (DCO). It also provides other benefit such as the increase of the PLL design portability and testability, flexibility in loop bandwidth and faster behavioral simulation [64]. It’s very interesting to inject signal
into the DCO of the DPLL to help with better phase tracking and remove the limit of finite frequency resolution. This sampled-system with analog injection can be modeled in the z-domain.
Appendix A: Astable Multivibrators Based Discrete SO

An astable multivibrator is an electronic device which can continuously shift between its two states with respect to the output. If the output corresponding to one particular state is high, then the output corresponding to the other state is low. This nature of the circuit is useful in producing continuous output stream of pulses. It is very easy to realize an astable multivibrator using op-amp ICs.

Figure A.1 (a) shows a circuit of a voltage controlled multivibrator [69], which consists of a Schmitt trigger comparator and an integrator. The swing of the threshold voltage $V_t$ can be found from

$$V_t = \beta V_o = \frac{R_1}{R_1 + R_2} V_o = \frac{5}{5 + 20} \times \frac{5}{2} = 0.5V \quad (A.1)$$

Therefore, the current $I_x$ charges and discharges the capacitor $C_x$ between two values (2V and 3V) of the threshold voltage around 2.5V. Signals at inverting/non-inverting inputs, and the output of the Schmitt trigger have the waveforms shown in Figure A.1(b).

A periodic signal with a frequency close to the oscillator’s frequency is then injected into the multivibrator to perturb the threshold voltage of the Schmitt trigger, as is shown in Figure A.2(a) [69]. The idea of injection here is to let the ramping voltage $V_x$ hit the perturbed threshold voltage before or after it would have if there...
Figure A.1: Voltage controlled multivibrator

Figure A.2: Injection in astable multivibrator oscillator
were no injection due to the fact that the speed of the voltage ramping is the same as before since the charging capacitance $C_x$ is kept the same. This integration speed could be found from the slope of the ramp voltage as

$$\text{slope} = \frac{2V_i}{T_o/2}$$  \hspace{1cm} (A.2)

where $T_o$ is the period of the multivibrator without injection, and its corresponding angular frequency is denoted as $\omega_o$. Assume the system is already locked to the injected frequency $\omega_i$ in its steady state, thus the output frequency $\omega = \omega_i$. Let the phase difference between the injected signal and the output signal be $\theta$, the new threshold swing can be obtained from the steady state waveforms drawn in Figure A.2(b):

$$2V_{\text{t,new}} = \text{slope} \times \frac{T_i}{2} = \frac{2V_i T_i}{T_o} = \frac{2V_i \omega_o}{\omega_i}$$  \hspace{1cm} (A.3)

On the other hand, from the geometry,

$$2V_{\text{t,new}} = 2V_i - 2V_i \sin \theta$$  \hspace{1cm} (A.4)

where $V_i$ is the amplitude of the injected signal. Therefore, equating Equation(A.3) and Equation(A.4), we have

$$\frac{\omega_i}{\omega_o} = \frac{1}{1 - \frac{V_i}{V_t} \sin \theta} \approx 1 + \frac{V_i}{V_t} \sin \theta$$  \hspace{1cm} (A.5)

The approximation in Equation (A.5) is valid if we have low level injection with $\frac{V_i}{V_t} \ll 1$. Rewrite Equation (A.5) as

$$\Delta \omega + K_I \sin \theta = 0$$  \hspace{1cm} (A.6)

where $\Delta \omega = \omega_o - \omega_i$ is the frequency difference between the free running oscillator and the injection, and $K_I = \frac{V_i}{V_t} \omega_o$ is the injection constant.
If the system is driven but unlocked, $\theta$ will vary with time and the output frequency 
$\omega = \omega_i - \frac{d\theta(t)}{dt} \neq \omega_i$. Follow the same analysis from Equations (A.3) to (A.6), we 
could get a first order differential equation that describes the system dynamics of a 
multivibrator under injection:

$$-\frac{d\theta(t)}{dt} = \Delta \omega + K_I \sin \theta(t)$$  

(A.7)

Note that Equation (A.7) is identical to Adler’s Equation for injection locked oscilla-
tors where he assumes $\phi(t) = \phi_o(t) - \phi_i = -\theta(t)$ and has

$$\frac{d\phi(t)}{dt} = \Delta \omega - K_I \sin \phi(t)$$  

(A.8)

Also note that $\Delta \omega \leq K_I$ for a steady state to exist ($\frac{d\phi}{dt} = 0$). Therefore, the pull-in 
range of the injection locked multivibrator is simply $K_I$. 

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Appendix B: Chip Description and Measurement Set-up

This appendix documents the chip layout and the testing procedures. The prototypes of the circuits developed during the work of this dissertation are fabricated with GlobalFoundries CMOS-8RF Technology through MOSIS multi-project wafer (MPW) program. CMOS-8RF is a high-speed analog radio frequency (RF) CMOS process. It is developed based on IBM CMOS-8SFG which is the advanced process technology features 130 nm lithography.

Figure B.1 shows the layout (filling removed) and the microphotograph of the final chip, which is composed of a Reference-Injected Phase-Locked Loop (PLL-RI) with no feedback divider (PLL-RI 1); a PLL-RI with divide-by-4 at the feedback path (PLL-RI 2); PLL-RI building blocks used in PLL-RI 1 and PLL-RI 2 including a Voltage Controlled Synchronous Oscillator (VCSO), a Phase Frequency Detector and a Charge Pump (PFD/CP), a divide-by-4 Frequency Divider (FD) and a buffer stage; a series of individual PMOS and NMOS devices (CMOS Device Test 1) for the baseband device modeling characterization; and several devices (CMOS Device Test 2) including active and passive components for baseband noise characterization. The chip occupies 2mm×2mm in area.

The RF characterization of the chip is measured with a Cascade Probe test system which consists of a RF probe station, ground-signal-ground (GSG) coplanar RF
Figure B.1: Final chip (a) layout and (b) microphotograph
probes, and high-speed cables. The testing environment is shown in Figure B.2. The DC characterization of the devices on chip is measured with a DC probe station in our lab shown in Fig B.3. The probe station holds the wafer and probes the devices. It is housed inside a Faraday cage which provides shielding from outside interferences. The probes are connected to the equipment through the bulkhead connectors which are fixed in the wall of the Faraday cage. In the following sections, ESD protection circuits used in the design and different test set-ups are provided for different types of measurement including RF and DC.

B.1 ESD Protection Circuits

One of the most pervasive reliability problems facing the IC industry is the ESD (electrostatic discharging) failure. It is reported up to 35% of total IC field failures
are ESD induced with an estimated annual cost to the IC industry running to several billion dollars [70]. The chip pads use the prime cell (pcell) provided by the design kit for the ESD protection [71]. The major pcells used are

- **ESD Double Diodes for DC/RF Pads**

  The two-diode clamping circuit shown in Figure B.4 will not allow voltages exceeding the positive or negative lead to get to protected device input.

- **RC-Triggered Power Clamps for VDD Pads**

  An ESD RC-Triggered Power Clamp shown in Figure B.5 is an efficient way to provide a discharge path between Vdd and ground during ESD event and is normally off at all other times. It consists of three elements: a) a RC-frequency discrimination circuit, b) inverters which have been sized to reduce the switching threshold to reduce the requirement of large R and C, and c) a big NFET clamp.
Figure B.4: ESD double diodes (a) schematic (b) layout

Figure B.5: RC-Triggered Power Clamps (a) schematic (b) layout
device. Under an ESD transient event, the RC-frequency discrimination circuit detects a short ESD pulse, and drives the gate of MOSFET into the active turn-on mode, forming a low-impedance discharge path to shunt ESD current. Because of the raised gate voltage, the MOSFET operates below the triggering and does not enter into the snapback region. Therefore, it can reduce the latchup or latchup like dangers.

B.2 VCSO Measurements Set-up

B.2.1 Output Spectrum and Phase Noise

The test set-up for measuring the VCSO input-output gain characteristic and phase noise is shown in Fig. B.6. The injection signal is provided by the signal generator (E82570D) and applied to the injection port through a BiasTee with DC voltage. The output is ac coupled to the Signal Source Analyzer (SSA E5052B). A 1.2V battery is employed to supply power and control voltage (with the help of a potentiometer) to the chip with a low noise solution.

B.2.2 Injection Signal Transfer Characteristics

The test set-up for measuring the VCSO injection signal transfer characteristic S21 is shown in Fig. B.7. The vector network analyzer (E8361A PNA) output is injected to the VCSO through a BiasTee with DC voltage. The output of the chip is AC coupled and attenuated before it is fed to the input of the network analyzer. The vector network analyzer (VNA) is first calibrated with the on-wafer calibration standard fabricated on the Impedance Standard Substrate (ISS) with all supporting circuit blocks presented. Again, a 1.2V battery is employed to supply power and control voltage to the chip with a low noise solution.
**Figure B.6:** Testing setup for VCSO output spectrum and phase noise

**Figure B.7:** Testing setup for VCSO output spectrum and phase noise
B.3 PLL-RI Measurements Set-up

The test set-up for PLL-RI is shown in Figure B.8 where a power splitter is used to split the pulse input from the RF signal generator to feed to both the injection port with an attenuator and the reference port. The pulse power is attenuated by 3dB after the power splitter. Again, a 1.2V battery is employed to supply power to the chip with a low noise solution. A 50Ω variable resistor is used to provide the variable Charge-Pump current.

Figure B.8: Testing setup for PLL-RI
Figure B.9: Device layout specifications

Figure B.10: Testing setup for the I-V measurement with HP4154A
B.4 Device IV Measurement Set-up

The detailed device layout specifications for DC characterization are shown in Figure B.9. The set-up is composed of the DC probe station, the HP4145 Semiconductor Parameter Analyzer and the computer program, as shown in Figure B.10. The transfer characteristics $I_{DS}$ vs. $V_{GS}$ are measured at low drain bias voltages by sweeping the gate voltage while monitoring the drain current with various bulk to source voltages. From the measured low drain characteristics, the device threshold voltage, doping concentration, carrier mobility, etc can be determined.

National Instrument LabVIEW system provides an environment for creating intuitive, graphically oriented programs for the automated control of the lab equipment. The Labview program functionality was implemented by previous Ph.D. student Dr. X. Zhang [55] in the group.
Appendix C: Relationship between Phase Noise and Timing Jitter [8]

The output phase $\Phi (t)$ of a practical oscillator can be written as

$$\Phi (t) = 2\pi f_o t + \phi (t)$$  \hspace{1cm} (C.1)

where $f_o$ is the nominal running frequency and $\phi (t)$ modulates phase fluctuations due to internal and external noises. The timing uncertainty $\tau (t)$, which is a random variable that characterizes the period fluctuations at any time $t$, is then calculated as

$$\tau (t) = \frac{\Phi (t + T_o) - \Phi (t) - 2\pi}{2\pi f_o} = \frac{\phi (t + T_o) - \phi (t)}{2\pi f_o}$$  \hspace{1cm} (C.2)

where $T_o = 1/f_o$ is the nominal period of the oscillator output. The timing jitter is defined as the variance $\sigma_\tau^2$ of $\tau$ around its mean value [56]:

$$\sigma_\tau^2 = \frac{1}{(2\pi f_o)^2} E \{ [\phi (t + T_o) - \phi (t)]^2 \} = \frac{1}{2\pi^2 f_o^2} [R_\phi (0) - R_\phi (T_o)]$$  \hspace{1cm} (C.3)

The autocorrelation function $R_\phi (d)$ is defined as

$$R_\phi (d) = E [\phi (t) \phi (t + d)]$$  \hspace{1cm} (C.4)

The relation between the autocorrelation function $R_\phi (d)$ and the power spectral density $S_\phi (f)$ of the RMS value of phase fluctuations $\phi (t)$ is given by Wiener-Khinchine
theorem [72]:

\[ R_\phi (d) = \int_{-\infty}^{\infty} S_\phi (f) e^{i2\pi fd} df \]  

(C.5)

Substitute (C.5) into (C.3), we can get

\[ \sigma^2 = \frac{1}{2\pi^2 f_o^2} \int_{-\infty}^{\infty} S_\phi (f) \left( 1 - e^{i2\pi \frac{f}{f_o}} \right) df = \frac{2}{\pi^2 f_o^2} \int_{0}^{\infty} S_\phi (f) \sin^2 \left( \pi \frac{f}{f_o} \right) df \]  

(C.6)
Appendix D: Fourier Components of a Pulse Waveform

This appendix reviews the Fourier components of a pulse waveform to demonstrate its usage in the sub-harmonic injection locking in the Synchronous Oscillators (SOs).

Figure D.1 shows the transient waveform $x(t)$ with period $T = \frac{2\pi}{\omega_o}$, pulse width $\Delta T = D \times T$, and pulse height $A$. For the periodic function $x(t)$, the Fourier series is a representation of the function in terms of sine and cosine functions as follows:

$$x(t) = \frac{a_o}{2} + \sum_{n=1}^{\infty} \left[ a_n \cos (n\omega_o t) + b_n \sin (n\omega_o t) \right]$$  \hspace{1cm} (D.1)

with

$$a_o = \frac{2}{T} \int_{0}^{\Delta T} x(t) \, dt = \frac{2}{T} ADT = 2AD$$

Figure D.1: Pulse waveform

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Therefore, Equation (D.1) becomes

\[
x(t) = AD + \sum_{n=1}^{\infty} \left\{ \frac{A}{\pi n} \sin (2\pi nD) \cos (n\omega_o t) + \left[ \frac{A}{\pi n} - \frac{A}{\pi n} \cos (2\pi nD) \right] \sin (n\omega_o t) \right\}
\]

(D.3)

If the pulse width is narrow, \( nD \ll 1 \), Equation (D.3) can be approximated to

\[
x(t) = AD + \sum_{n=1}^{\infty} [2AD \cos (n\omega_o t)]
\]

(D.4)

Therefore, if the pulse width is small, the Nth harmonic of the pulse train has substantial amplitude, therefore, the injection parameter \( K_{SO} \) is effective to let the oscillator lock to the Nth harmonic tone, and enables the frequency multiplication, as demonstrated in Figure D.2.
Bibliography


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