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UMI
INVESTIGATION AND DEVELOPMENT OF HIGH QUALITY GaAs-ON-Si FOR
SPACE PHOTOVOLTAICS USING A GRADED GeSi BUFFER

DISSertation

Presented in Partial Fulfillment of the Requirements for
the Degree Doctor of Philosophy in the
Graduate School of The Ohio State University

by

John Anthony Carlin, M.S.E.E.

************************

The Ohio State University
2001

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ABSTRACT

The ability to integrate the optical properties of III-V semiconductors with the current capabilities of Si microelectronics on a single substrate has been of great interest for many years. In addition, III-V/Si integration is also of great interest for space photovoltaics applications in order to combine high performance space cells with a strong, lightweight and inexpensive substrate. However, due to fundamental materials incompatibilities, namely the 4% lattice mismatch between GaAs and Si and the >63% mismatch in thermal expansion coefficient, epitaxial GaAs/Si integration has been largely unsuccessful due to uncontrolled threading dislocation (TD) nucleation resulting in thread densities greater than $10^9 \text{ cm}^{-2}$. Although many integration techniques have been able to successfully reduce TD's to $\sim 3-7 \times 10^6 \text{ cm}^{-2}$ (including thermal cycle annealing and the insertion of various III-V buffer layers), none has achieved device performance equivalent to homoepitaxial GaAs due to the residual threading dislocation density. Recently, GeSi graded buffers have provided an integration technique, which has successfully reduced threading dislocation densities (TDD's) below $1 \times 10^6 \text{ cm}^{-3}$ for a 100% Ge cap on a Si substrate. This integration approach is unique in the respect that it does not attempt to provide strain management or dislocation engineering within the III-V layers (similar to other techniques) but rather through the gradual and controlled introduction of strain during a $\text{Ge}_x\text{Si}_{1-x}$ grade from a 100% Si to a 100% Ge surface.
In this research, we investigate the application of the GeSi graded buffer for GaAs/Si integration, specifically for application to high efficiency single junction solar cells. Through atomic control of the GaAs/GeSi interface via MBE, the elimination of anti-phase boundary and TD nucleation as well as the minimization of atomic diffusion at the GaAs/GeSi interface was achieved for the GaAs/GeSi system. Combined with the low TDD enabled by the GeSi graded buffer, record GaAs/Si minority carrier lifetimes in excess of 10 ns have been achieved, more than tripling the best lifetime achieved by any other GaAs/Si integration technique to date, ~3ns. Extending this material quality to devices, $V_{oc}$'s in excess of 1040 mV were achieved for single junction GaAs solar cells, more than a 10% improvement over the previous best achieved for GaAs/Si (940mV). These results demonstrate the promise of this integration technique and will result in the realization of GaAs/Si solar cells with efficiencies exceeding 20% AM0, suggesting that the GaAs/GeSi epitaxial integration methodology is a viable and beneficial alternative for space solar applications.
DEDICATION

To my entire family. Without your love, support, tolerance, and encouragement I could not have completed this degree or any other. Special thanks to my parents. Your ideals, dreams, nourishment, and commitment have given more to my life and the lives of all your children than we could possibly repay. Please accept this accomplishment as a symbol of my appreciation for all your hard work and dedication.

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6.13 Linear and log I-V plots for 36 individual GaAs/GeSi diodes grown by MBE with area of \( 1000 \times 1000 \, \mu m^2 \). The diodes were separated into 3 groups based on the surface morphology of the diode mesa: (a) no surface defect incorporation (14 diodes), (b) surface defects but no bat defects (9 diodes), and (c) one or more bat defects on the diode mesa (10 diodes).

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6.16 Light I-V data for single junction GaAs solar cells grown by MOCVD (InGaP/GaAs) and MBE (AlGaAs/GaAs). The MOCVD grown cell area is \( 0.2 \times 0.2 \, cm^2 \) while the MBE grown cell area is \( 0.4 \times 0.4 \, cm^2 \). Some of the increased shunt and reduced \( V_{oc} \) can be attributed to the additional defects incorporated in the larger MBE device. However, MOCVD cells display minimal shunt independent of device area due to bat defect filling/passivation.

6.17 Schematic of p-n InGaP/GaAs single-junction solar cell structure used in this research grown by MOCVD. (*) denotes layers grown during GaAs/Ge nucleation procedure by MBE on Ge and GeSi substrates. Nominal doping densities for all layers are listed to the right.

6.18 Light I-V comparison of InGaP/GaAs solar cells grown by MOCVD on GaAs/Ge, and GeSi substrates. Data for the GaAs and GeSi substrates is for \( 0.2 \times 0.2 \, cm^2 \) cells (10.2% metal coverage) while data for the Ge substrate is for \( 0.4 \times 0.4 \, cm^2 \) cells (7.8% metal coverage).
6.19 External quantum efficiency measurements for MOCVD grown InGaP/GaAs solar cells on GaAs and Ge substrates. ................................................................. 188

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CHAPTER I

INTRODUCTION AND BACKGROUND

This dissertation focuses on both structural and electrical characterization of III-V compound semiconductors epitaxially integrated on group IV substrates, including Ge and Si, with an ultimate goal of achieving high quality GaAs-on-Si device performance. While the ability to combine the optical properties of III-V semiconductors with the current capabilities of Si microelectronics has been of great interest for many years for the implementation of optoelectronic integrated circuits (OEIC’s) as well as system on a chip (SoC) applications, in fact the Si technology roadmap recognizes it as one of the necessary, long-term solutions to current metal interconnect limitations.\textsuperscript{[1]} many fundamental materials incompatibilities between III-V semiconductors and Si have limited the success of large scale monolithic (epitaxial) integration. Additionally, while many integration techniques, include flip-chip bonding, etch back, pick and place, epitaxial lift-off, and lateral epitaxial overgrowth,\textsuperscript{[2,3,4,5,6]} have been developed in order to circumvent the need for direct GaAs-on-Si heteroepitaxy, each has been met with only limited success and none has provided a solution for the realization of large area III-V/Si (III-V-on-Si) devices or integration over a wafer scale. Therefore, monolithic III-V/Si
integration appears to be the only solution suitable for the application to large area. Specifically, one application which has drawn considerable interest in the past decade and which will be the concentration of this work is III-V/Si space photovoltaics.\cite{7,8} Due to the large area requirements for single devices, up to 28 cm\(^2\) cell areas,\cite{9} techniques other than heteroepitaxy do not appear to be suited for this application. Therefore, while GaAs/Si heteroepitaxy demonstrates certain fundamental materials limitations, it appears to be the only technique scalable for the large area requirements of space photovoltaics. Recently, the development of a novel integration methodology exploiting SiGe graded buffers has shown great promise in reducing the incorporation of detrimental threading dislocations for grades up to 100\% Ge. The investigation of the integration of III-V layers on this “manufactured” Ge surface will be the focus of this work.

1.1 Objective

The purpose of this research is to investigate the integration of III-V compound semiconductors on a novel SiGe graded buffer as a solution to the monolithic integration of III-V’s and Si. The development of these 100\% Ge surfaces through a SiGe “graded buffer” on a Si substrate has resulted in the realization of low threading dislocation densities (TDD’s) which have been unachieved to date through other integration techniques. However, while this grading methodology has successfully produced low TDD Ge layers, the realization of complete III-V/Si integration requires the further integration of a III-V layer (GaAs and closely lattice matched III-V alloys such as AlGaAs and InGaP will be considered in this work) on the “manufactured” Ge surface. However,
while closely lattice matched to Ge, the growth of GaAs/Ge is a non-trivial process due to chemical and polar/non-polar mismatch at the interface. Therefore, the first phase of this project was the successful control of the GaAs/Ge interface on Ge wafers, a well-studied research problem, in order to provide a base-line nucleation methodology which could be used to investigate the “ideality” of the Ge/GeSi/Si graded buffer surface for III-V nucleation. This phase of the project was completed by a previous graduate student, Dr. Robert M. Sieg, and laid the foundation for the second phase completed in this work. The objectives of this phase of the project were four fold: 1) The extension of the GaAs/Ge nucleation methodology previously developed to the growth of GaAs/Ge/GeSi/Si by molecular beam epitaxy (MBE), 2) the material characterization, both structural and electrical, of the GaAs/Ge/GeSi/Si system to determine the impact of both surface morphology and residual TDD from the GeSi grading process and to what extent the Ge/GeSi/Si buffer behaves as an “ideal” low mismatch Ge interface for GaAs nucleation, 3) characterization of the impact of the nucleation methodology, residual TDD, surface morphology, and 4) the resulting characterization of III-V material quality on device performance through the use of a simple single-junction solar cell device design.

1.2 Background

Table 1.1 provides a compilation of material properties for the elemental and compound semiconductors to be considered in this work. Additionally, while not documented in table 1.1, it is noted that the Group IV elemental semiconductors,
<table>
<thead>
<tr>
<th>Material</th>
<th>Group</th>
<th>Lattice Constant (Å)</th>
<th>Mismatch versus GaAs (%)</th>
<th>Density (gm/cm³)</th>
<th>Expansion coeff. (K⁻¹)</th>
<th>Melt. Point (°C)</th>
<th>Conductivity (W/cm-K)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>IV</td>
<td>5.43102</td>
<td>4.092</td>
<td>2.329</td>
<td>2.6x10⁻⁶</td>
<td>1412</td>
<td>1.3</td>
</tr>
<tr>
<td>Ge</td>
<td>IV</td>
<td>5.65791</td>
<td>0.082</td>
<td>5.323</td>
<td>5.5x10⁻⁶</td>
<td>937</td>
<td>0.8</td>
</tr>
<tr>
<td>GaAs</td>
<td>III-V</td>
<td>5.65325</td>
<td>-</td>
<td>5.318</td>
<td>5.5x10⁻⁶</td>
<td>1240</td>
<td>0.6</td>
</tr>
<tr>
<td>AlAs</td>
<td>III-V</td>
<td>5.660</td>
<td>0.119</td>
<td>3.760</td>
<td>5.0x10⁻⁶</td>
<td>1740</td>
<td>---</td>
</tr>
<tr>
<td>InAs</td>
<td>III-V</td>
<td>6.0583</td>
<td>7.165</td>
<td>5.667</td>
<td>4.5x10⁻⁶</td>
<td>942</td>
<td>0.4</td>
</tr>
</tbody>
</table>

Table 1.1: Compilation of materials parameters for semiconductors of interest for this discussion. (T = 300 K)

The alloy AlₓGa₁₋ₓAs is direct bandgap in the range 0 ≤ x ≤ 0.35.

including Ge and Si, have a cubic "diamond-like" lattice structure while the III-V compound semiconductors possess a cubic "zincblende" lattice structure. In addition to other materials incompatibilities, this mismatch becomes significant when considering any III-V/Group IV interface.

Unlike applications driving optical integration, such as the microprocessor, the motivation for developing GaAs/Si solar cells is not driven by the desire to integrate optical devices with Si microelectronics. III-V solar cells for space applications are currently grown on Ge wafers due to the lower cost and somewhat increased mechanical strength of Ge compared to GaAs substrates, coupled with the reasonable lattice match.
Table 1.2: Comparison of material parameters of interest for solar for Si, Ge, and GaAs. However, from solely a substrate perspective, Ge is not an optimum substrate material, especially when compared with Si, which is far cheaper, stronger, lighter and available in much larger areas than Ge. Table 1.2 shows a comparison of material parameters specifically important to space photovoltaics for Si, Ge, and GaAs wafers. In essence, the choice of Ge as the preferred substrate is a compromise, one which results from the need for matching the lattice constant of the III-V epitaxial layers so that high quality, crystalline III-V layers can be grown by epitaxial techniques, resulting in the fabrication of high efficiency cells.\textsuperscript{[9,10,11]} Silicon, unfortunately, while possessing superior substrate properties (low mass density, high thermal conductivity, inexpensive, mechanically strong), is not lattice matched to GaAs and the related III-V alloys that are optimum for solar energy conversion (figure 1.1). However, both crystalline and amorphous Si solar cells, which are commonly used for terrestrial (earth/land based) applications, possess the advantages of a Si substrate and are by definition lattice matched (crystalline case). Why then are Si cells not also used in space applications to alleviate the desire for III-V-on-Si epitaxy?
Figure 1.1: Bandgap versus lattice constant plot for many common group IV, III-V, and II-VI semiconductors. The lines between two semiconductors indicate the ternary alloy properties.

Figure 1.2: Project efficiencies for “ideal” single-junction solar cells versus bandgap under AM0 radiation, (i.e. no metal shadowing and complete collection of the above-bandgap spectrum.) \[^{[12]}\]
<table>
<thead>
<tr>
<th>Cell Technology</th>
<th>Cell Efficiency (%)</th>
<th>Module Efficiency (%)</th>
<th>Module Cost ($/Watt)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single Crystal Silicon</td>
<td>24.0</td>
<td>12-14</td>
<td>3-5</td>
</tr>
<tr>
<td>Polycrystalline Silicon</td>
<td>17.8</td>
<td>10-12</td>
<td>3-5</td>
</tr>
<tr>
<td>Amorphous Silicon</td>
<td>12.7</td>
<td>5-10</td>
<td>4-6</td>
</tr>
<tr>
<td>Single-junction GaAs</td>
<td>25.1</td>
<td>17-18</td>
<td>~2000</td>
</tr>
<tr>
<td>Double-junction GaAs</td>
<td>29.5</td>
<td>20-23</td>
<td>~3000</td>
</tr>
</tbody>
</table>

Table 1.3: Comparison of cell and module performance for various solar technologies. All efficiencies assume AM1.5 radiation. (after 14)

Figure 1.2 shows a plot of theoretical maximum efficiency versus bandgap for single-junction solar cells under Air-Mass Zero (AM0) illumination (equivalent to the photon spectrum in space). Due to a smaller bandgap relative to GaAs, Si is less efficient at converting the AM0 light spectrum, which is dominated by high energy (blue) photons. Therefore, compared to an array of GaAs cells, in order to obtain an equal amount of power, a larger area of Si cells is required. For terrestrial applications, physical area is not a limitation, and, since GaAs cells are more expensive to produce, Si cells, while less efficient, are commonly used. Currently, GaAs single-junction solar modules are more than 400 times more expensive to manufacture than single crystal Si modules (table 1.3). However, additional considerations must be addressed when designing cells for space applications. Unlike terrestrial systems, the cost of the solar array is not independent of the system cost and is no longer the dominant expense of the "solar power system". For space applications, a satellite for example, the important issues for the solar array are weight, efficiency, and radiation hardness. Since the solar
arrays must be launched into space and must also be deployed in order to collect sunlight. The most important considerations for space solar cells are not the cell cost, but the power per area (watts/m$^2$) and the specific power (watts/kg). However, in addition to the beginning of life efficiencies (BOL), due to radiation damage sustained during orbit in space, solar arrays must be designed while considering their end of life (EOL) efficiencies. The ability to successfully retain efficiencies near BOL values after radiation exposure is known as “radiation hardness”. Figure 1.3(a) shows a plot of normalized efficiency after 10 MeV proton irradiation for InP, GaAs, and Si solar cells.$^{[12]}$ While the extent of radiation exposure in space is largely determined by the satellite orbit, in addition to lower BOL efficiencies the degradation of the Si cells with radiation exposure is more severe than with InP or GaAs, requiring even larger cell arrays in order to achieve the same array power. Figure 1.3(b) shows a schematic of the area “savings” with increased cell efficiency (higher efficiency = smaller array size).$^{[15]}$ As shown in table 1.4, while the single-junction Si cell costs less, ($$/watt), than the III-V counterparts (GaAs/Ge in this case) and possesses superior substrate properties, the overall system cost is higher than for III-V solar arrays due to the increased size and weight resulting from decreased cell efficiency.$^{[15]}$ However, while GaAs/Ge cells are currently preferred over Si-based cells, the ability to combine the efficiency of the III-V cells with the superior substrate properties of Si would combine the advantages of both materials systems.

Therefore, although Si is only being exploited in this case as a “passive” substrate material and not an “active” material for optoelectronic integration, the economic and
Figure 1.3: Comparison of space solar cells. (a) Efficiency reduction for InP, GaAs, and 2 mil Si solar cells after 10 MeV proton irradiation.\textsuperscript{14} (b) Comparison of panel sizes required for various solar cell technologies in order to achieve 8 kW power.\textsuperscript{15}
Table 1.4: Cost comparison of single-junction GaAs/Ge, multiple-junction GaAs, and Si solar cells for space.\textsuperscript{[15]}

<table>
<thead>
<tr>
<th>Cell Technology</th>
<th>Multijunction GaInP/GaAs/Ge</th>
<th>Single-junction GaAs/Ge</th>
<th>Conventional Si</th>
</tr>
</thead>
<tbody>
<tr>
<td>EOL array (Watts/kg)</td>
<td>22 EOL</td>
<td>19 EOL</td>
<td>14EOL</td>
</tr>
<tr>
<td>EOL Watts needed</td>
<td>\textit{10,000}</td>
<td>\textit{10,000}</td>
<td>\textit{10,000}</td>
</tr>
<tr>
<td>Est. weight of array</td>
<td>455 kg</td>
<td>525 kg</td>
<td>714 kg</td>
</tr>
<tr>
<td>Weight savings over GaAs/Ge</td>
<td>71 kg</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Weight savings over Si</td>
<td>259 kg</td>
<td>188 kg</td>
<td>-</td>
</tr>
<tr>
<td>Launch cost savings over GaAs/Ge</td>
<td>$1,405,232</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Launch cost savings over Si</td>
<td>$5,126,128</td>
<td>$3,720,896</td>
<td>-</td>
</tr>
</tbody>
</table>

performance benefits provided by a Si substrate over GaAs or Ge are substantial enough to make GaAs/Si photovoltaics a desired technology for space applications. However, as previously mentioned, the 4% lattice constant mismatch between GaAs and Si, table 1.1, causes very high threading dislocation densities for GaAs directly grown on Si, rendering the GaAs useless as a photovoltaic material. Nevertheless, many research groups have recognized the potential benefits of achieving efficient III-V cells on Si and many methods to control and reduce the dislocation density have been investigated to deal with the mismatch problem. Most notably, these include thermally-cycled growth of the III-V intermediate layers and the insertion of various types of III-V buffer layers and superlattice structures prior to cell deposition.\textsuperscript{[16,17,18,19,20,21]} Each has been successful in reducing the density of threading dislocations from greater than $10^9$ cm$^{-2}$ for direct
Figure 1.4: Schematic representation of two approaches to GaAs/Si integration. The first involves management of the lattice mismatch entirely within III-V layers while the second utilizes group IV layer grading in order to minimize threading nucleation.

Figure 1.4 shows a schematic representation of two approaches to GaAs/Si integration. The first involves management of the lattice mismatch entirely within III-V layers while the second utilizes group IV layer grading in order to minimize threading nucleation.

As can be seen from the past two decades of activity in the field, almost all efforts to achieve GaAs based solar cells on Si have involved a form of strain management and dislocation engineering within the III-V layers themselves. It is interesting to note that the "optimal" conditions for each approach have tended to result in similar dislocation densities and carrier lifetimes for the GaAs heteroepitaxial layers. This observation implies that limitations may exist within the III-V system in mitigating this large lattice mismatch, which is only exacerbated by the large area requirements for solar cells. This has motivated an alternative approach in which the surface lattice constant of the Si substrate itself is engineered prior to III-V growth, rather than dealing with the mismatch only within the III-V regions.
the key difference between this approach and those used to date for GaAs/Si integration. In this technique, the lattice mismatch is addressed in a material system and under growth conditions that are independent from the III-V device layers. Hence, a wider range of growth conditions (temperature, growth rate, etc.) may be accessible to achieve optimal lattice relaxation than can be provided by the III-V layers. The Ge_{x}Si_{1-x} alloy system is well-suited for this application since by increasing the Ge content (x) during growth of a Ge_{x}Si_{1-x} epitaxial layer on Si, the lattice constant can be increased from that of Si to Ge, providing a close lattice match for subsequent GaAs-based device growth. However, while this integration solution mitigates the need for direct GaAs/Si heteroepitaxy and provides threading dislocation control, which is no longer required in the III-V system, the GeSi grading solution creates a Ge surface which must now be controlled during GaAs nucleation. In this work, we characterize the integration of GaAs with these “virtual” Ge substrates for application as a viable GaAs/Si integration solution. First, the following section provides a discussion of the most prominent materials integration issues associated with the mismatch between GaAs and both Group IV substrates (Si and Ge). A discussion of the GeSi grading procedure and its’ benefits is provided in section 1.5.

1.3 GaAs/Ge and GaAs/Si growth limitations

In the following sections the prominent limitations to GaAs/Si and GaAs/Ge heteroepitaxy are discussed. Since both growth systems involve III-V/Group IV epitaxy, both GaAs/Si and GaAs/Ge share issues generated from the growth of the polar/non-polar, III-V/Group IV interface. These problems include the formation of anti-phase...
domains (APD’s) as well as interface atomic intermixing which can generate auto-doping near the interface. Additionally, the GaAs/Si system possesses the additional materials issues which have limited the success of GaAs/Si monolithic integration to date. While these have been alluded to in earlier discussion, the origin and impact of the large thermal (~63%) and lattice mismatch (~4%) are discussed in more detail.

1.3.1 Impact of GaAs/Si lattice mismatch

Along with thermal mismatch, section 1.3.2, the lattice mismatch between GaAs and Si of greater than 4% is largely responsible for the inability to achieve high GaAs/Si device and material quality through monolithic integration.

Mismatch heteroepitaxy involves the growth of a layer epitaxially with a lattice constant different than that of the underlying substrate. Figure 1.5 shows a schematic representation of epitaxial growth for substrates of lattice constant both larger and smaller than the epitaxial layer. Because of this lattice mismatch, inherent in mismatched heteroepitaxy is the incorporation of either compressive or tensile strain in the epitaxial layer as shown in equation 1.1, where \( a_e \) and \( a_s \) are the lattice constant of the epitaxial layer and the substrate, respectively.\(^{[23]}\) Beyond a critical thickness, \( h_c \), this strain is no longer accommodated by lattice distortion (tetragonal distortion) as it becomes energetically favorable to relieve the strain by other methods. The exact manner in which that strain is relieved, i.e. surface roughening, dislocation nucleation, 3-D growth, etc., is
Figure 1.5: Three possible lattice combinations exist for the growth of an epitaxial layer of lattice constant, $a$, on a substrate of lattice constant, $a_0$. a) $a = a_0$, b) $a > a_0$ and c) $a < a_0$. If a lattice mismatch exists, either tensile or compressive strain can be incorporated into the film as the lattice constant of the epitaxial layer is altered. [after 23]
Figure 1.6: Schematic representation of misfit and threading dislocation segments typical for growth of lattice mismatched systems. While the misfit segment is contained at the interface, the thread segment propagates through the epilayer to the growth surface.

dependent on many factors, including growth temperature, percent mismatch, growth rate, etc. For large mismatched systems such as GaAs-on-Si (mismatch > 4%), the large lattice mismatch results in uncontrolled pathways for lattice relaxation during direct GaAs-on-Si epitaxy, such as three-dimensional growth and the introduction of a large number of immobile edge and threading dislocations.\[^{24}\] The result is a near completely relaxed film containing a threading dislocation density > $10^9$ cm\(^{-2}\). However, for many systems of lower mismatch (< 1-1.5%), the incorporation of strain is more controlled and predominately results in the formation of 60° misfit dislocations at the heterointerface and the associated threading dislocations.\[^{24,25}\]

Figure 1.6 shows a schematic of the misfit and threading dislocation incorporation. Since the orientation of the burgers vector for threading dislocations
dictates that they cannot contribute to strain relaxation, the misfit segment in the interface plane is the only portion which provides relaxation of the lattice strain. Unfortunately, for the high mismatched GaAs/Si system the uncontrolled nucleation of dislocations results in small, sessile misfit segments which require a high density of threading dislocations, while the more controlled nucleation of glissile 60° misfits for lower mismatch systems (< 1-1.5%) can produce long misfit segments requiring fewer threading segments.

For the SiGe system which is exploited in this work for GaAs/Si integration, while a total mismatch of greater than 4% is incorporated, the step grading from a Si surface to a 100% Ge layer is accomplished by the growth of a series of “low-mismatch” interfaces, resulting in the continual relaxation by misfit glide rather than the uncontrolled incorporation of misfits and threads. While the exact details of the grading procedure are discussed in section 1.5, the result has been a successful reduction in the threading dislocation density from $\sim 10^9$ cm$^{-2}$ to $\sim 1x10^6$ cm$^{-2}$. However, one artifact of the grading procedure is the generation of a periodic series of ridges and valleys on the wafer surface know as cross-hatch. The cross-hatch pattern observed on the surface of the relaxed GeSi graded buffer is oriented along the <110> directions on a (100) Si surface and is characteristic of relaxed layers for many low-mismatch systems (< 1.0-1.5% mismatch depending on the growth conditions). While the exact mechanism for the generation of the cross-hatch morphology is not agreed upon,[26,27] it is accepted that the morphology is related to the presence of the 60° misfit segments at the interface. Therefore, while the use of a SiGe graded buffer alleviates the need heteroepitaxy of a “high-mismatch”
GaAs/Si system, a threading dislocation density of ~1x10^6 cm^-2 still exists and the new "virtual" Ge nucleation surface has an additional cross-hatched surface morphology which must be considered.

1.3.2 Thermal mismatch

As previously suggested, in addition to lattice mismatch, the mismatch in thermal expansion coefficients between GaAs and Si is also a problem in monolithic integration. Thermal expansion for a semiconductor is the change in lattice constant seen for a change in temperature. For heteroepitaxy, thermal expansion coefficient (α) mismatch results in the lattice constant of one layer (i.e. GaAs) changing more than the lattice constant of another (i.e. Si) with changing temperature. For example, α(Si) = 2.6x10^-6 K^-1 and α(GaAs) = 5.7x10^-6 K^-1 at 300 K, implying that the Si lattice will expand less when heated and contract less when cooled than the GaAs lattice. (note : α(GaAs) ~ α(Ge))

Recall for the GaAs/Ge/GeSi/Si system that the nucleation of misfit and threading dislocations during epitaxy results in the relaxation of compressive strain introduced by the lattice mismatch. The result of the dislocation introduction is that the epitaxial layer (GaAs in this case) is almost completely relaxed at the growth temperature, ~700°C. However, due to the thermal expansion coefficient mismatch between GaAs and Si, the "larger" contraction of the GaAs lattice with respect to the Si lattice when cooling from the growth temperature, T_G, results in the incorporation of tensile strain in the GaAs layer. Equation 1.2 gives the magnitude of the tensile strain due to thermal expansion mismatch at a temperature T_0, where α_e and α_s are the thermal expansion coefficients of
the epilayer and the substrate respectively.^{28,29} Note that $\alpha$ is a function of temperature and therefore makes an exact calculation of the thermal strain complicated. Equation 1.3 provides a simplified estimate of the thermal strain assuming a constant thermal

$$\varepsilon_\alpha = \int_{T_a}^{T_e} (\alpha_e(T) - \alpha_s(T)) dT$$

(1.2)

$$\varepsilon_\alpha \sim \Delta \alpha \times \Delta T$$

(1.3)

expansion coefficient. However, note that in order to provide an accurate measure of the thermal stress encountered in the GaAs/Ge/GeSi/Si system one must also account for the thermal mismatch in the GeSi graded region. Considering the GaAs/Si system and using the thermal expansion coefficients at 300K, equation 1.3 estimates the thermal strain to be $\sim 2 \times 10^{-3}$, less than 10 percent of the lattice mismatch strain for the GaAs/Si system, $\sim 3.9 \times 10^{-2}$. However, while the thermal mismatch strain is significantly smaller than the lattice mismatch strain incorporated, the thermal strain can become significant at large epitaxial thicknesses where the lattice mismatch strain has been relaxed via dislocation nucleation and glide. Unlike the gradual introduction of compressive strain during the growth of the compositionally graded GeSi layers which is controllably relaxed via 60° misfit nucleation and glide, the rate of tensile strain incorporation is dependent on the cooling rate. Additionally, although some of the thermal strain can be relaxed by defect nucleation and glide, as the temperature decreases the dislocations become "frozen" (no longer mobile) and there is no longer enough thermal energy to relieve strain via defect...
nucleation or dislocation glide. The result, as seen in the GaAs/Si system for large thermal mismatch, is that the tensile strain is relieved by the incorporation of concave wafer bowing and cracking of the epilayer.\textsuperscript{30,31,32} Similar to the critical thickness for defect nucleation during growth, the extent of the epilayer cracking also depends on the thickness of the sample, which determines the magnitude of the tensile strain energy introduced during cooling. Therefore, there is a “critical thickness” below which cracking will not occur. For the GaAs/Si system (no GeSi graded buffer), reports indicate that this thickness is approximately 3-5 μm, after which epilayer cracking can result in a crack spacing of <200μm along the <110> directions.\textsuperscript{33,34} Additionally, while most reports do not indicate the presence of wafer bow, wafer bow is likely in addition to epilayer cracking. Unfortunately, for direct GaAs/Si growth 3-5 μm is not sufficient for growth of a solar cell structure while still incorporating TDD reduction layers sufficient to reduce the TDD below ~5x10^6 cm\(^{-2}\), with additional TDD reduction requiring thicker GaAs buffers. Combined with the impact of threading dislocations, this fact has limited the success of GaAs/Si monolithic integration.

However, various techniques have been attempted in order to minimize the presence of both epilayer cracking and wafer bow. Since epilayer cracks are known to initiate from points of high strain, such as wafer edges and particulates, selective area epitaxy (SAE), or growth on patterned/mesa substrates, has been successful in reducing crack formation on the mesas since nucleation sites for crack formation are minimized and cracks are unable to propagate onto the mesa from the wafer edge.\textsuperscript{33} Additionally, methods of “strain balance” have been used in an attempt to reduce both epilayer cracking
and wafer bow. In these cases, compressive strain is incorporated in order to combat the tensile strain due to the GaAs-Si thermal expansion mismatch. For example, attempts have been made to use SiO₂, which has a thermal expansion coefficient less than that of Si, \( \alpha(\text{GaAs}) > \alpha(\text{Si}) > \alpha(\text{SiO}_2) \), on either the back side of the wafer or in the mesa “valleys” in order to balance the tensile strain introduced from the GaAs layers with regions of compressive strain.\(^{[32,34]}\) While this approach has seen limited success across small areas, the tensile strain incorporated in the GaAs layers is not eliminated. Likewise, considering the GeSi graded buffer system which will be of importance to this work, while the TDD is minimized, the concerns presented by thermal mismatch are not alleviated. However, through the incorporation of compressive strain through epitaxial layers, a method of strain balance is available. In fact, this approach has been used in the fabrication of the GeSi graded buffers in order to produce 100% Ge layers which are cubic (no tensile or compressive strain) and experience no epilayer cracking at room temperature.\(^{[35]}\) However, while these Ge layers are cubic, they do not yet contain any GaAs epitaxy. Therefore, thermal mismatch problems, such as wafer bow and epilayer cracking, similar to that experienced by conventional GaAs/Si epitaxy are expected unless additional methods of strain balance are approached to combat the added tensile strain (from thermal mismatch during cooling) following GaAs epitaxy. For this reason, while this work will not specifically consider solutions to epilayer cracking and wafer bow due to thermal mismatch, it is a problem that must be constantly monitored in order to determine the impact on device properties.
1.3.3 APB formation

Since the GaAs/Ge system contains less than 0.1% lattice mismatch and no significant thermal mismatch, neither threading dislocation nucleation or epilayer cracking is a significant issue for GaAs/Ge heteroepitaxy as it is for GaAs/Si epitaxy. However, III-V nucleation on a Group IV substrate does require the elimination of anti-phase domain (APD) disorder, making it a significant issue for both GaAs/Ge and GaAs/Si epitaxy. APD’s are crystalline defects which are generated due to the lower symmetry of the III-V “zincblende” crystal structure with respect to the higher symmetry, diamond-like crystal structure of both Si and Ge. Figure 1.7 shows a pictorial representation of an APD. The APD is bound by anti-phase boundaries (APB’s) which consist of metallic As-As or Ga-Ga bonds. These bonds are expected to be electronically charged, introducing recombination centers in the bandgap and therefore degrading the GaAs electrical quality. Figure 1.8 shows a TEM image containing APB’s nucleated at a GaAs/Ge interface. As seen in figure 1.7, the APB’s are generated due to a stacking mismatch created by the single stepped (one monolayer) Group IV surface. Fortunately, replacing the single stepped surface with a “double-stepped” surface (one unit cell = 2 monolayers) eliminates the GaAs-Group IV stacking mismatch and effectively eliminates the nucleation of APB’s. In fact, Li et. al. successfully generated APB-free GaAs growth on Ge via MOCVD through a combination of large substrate offcut toward the <110> direction coupled with high substrate temperature (~650°C), relatively low growth rate (<2μm/hr), and a high As/Ga ratio (~60:1). However, additional MOCVD results reporting APB-free growth indicate system conditions which seem contradictory to those
Figure 1.7: Schematic of a single-stepped Ge surface demonstrating the formation of APB's during GaAs growth due to the "stacking" mismatch.

Figure 1.8: Cross-sectional TEM images of GaAs growth on Ge/GeSi/Si graded buffers where a) an optimal nucleation procedure successfully prevented the formation of APB's and b) a non-optimal interface nucleation procedure resulted in the incorporation of large APB's.
reported by Li et al.\textsuperscript{[37,38,39]} Unfortunately, while these reports may indicate a large growth space over which APB-free GaAs/Ge is achievable, it seems likely that the prescriptions determined for APB-free growth are more “system specific” and cannot be used universally. Regardless, the ability to control APB formation is clearly achievable and does not impede the realization of high quality GaAs/Ge material, as is evident by the current industry standard GaAs/Ge production of high efficiency space solar cells.\textsuperscript{[40]}

1.3.4 Atomic interdiffusion at III-V/Group IV interface

In addition to APB formation, a well-known problem that is shared by both GaAs/Ge and GaAs/Si integration is that of atomic interdiffusion. Since group III and group V atoms act as substitutional p-type and n-type dopants respectively in the group IV lattice and group IV atoms are amphoteric substitutional dopants in the III-V lattice (more commonly n-type), the inability to limit intermixing at the III-V/group IV heterointerface can result in the formation of inadvertent p-n junctions in either the GaAs or the group IV. Considering the growth of n-type GaAs on an n-type Ge substrate, while Ge diffusion into the GaAs layer will “further” dope the layer n-type and As diffusion in the Ge substrate will “further” dope the substrate n-type, Ga diffusion into the substrate will act as a p-type dopant and “type-convert” the diffused region IF the concentration of Ga diffused is greater than the n-type Ge doping. Figure 1.9 shows the doping profile for a GaAs layer grown on a Ge substrate by MOCVD.\textsuperscript{[41]} In this case, the inability to control the interdiffusion of Ga and As at the GaAs/Ge interface resulted in inadvertent type-conversion in the Ge substrate and the formation of a p-n junction. Note that while
the Ga diffusion (p-type doping) in limited to within 200-300 nm of the GaAs/Ge interface the Ga concentration exceeds $1 \times 10^{19}$ cm$^{-3}$. Additionally, the As diffusion (n-type doping) extends many microns into the n-type Ge substrate, also with a concentration near $1 \times 10^{19}$ cm$^{-3}$ near the interface. This is a well-studied problem in GaAs/Ge solar cells grown by MOCVD where the formation of inadvertent p-n junctions can be detrimental to device performance.$^{[42]}$ Unfortunately, while many MOCVD growth prescriptions have been reported to eliminate APB formation, no reports by MOCVD or MBE indicate the ability to simultaneously reduce cross-diffusion and therefore junction formation. This task was undertaken during the initial stages of this project by a former graduate student and the results, which will significantly contribute to the initiation of this dissertation research, are outlined below. Note that the growth issues considered are for GaAs on a Ge substrate, eliminating the added difficulties of lattice
mismatch and thermal mismatch presented by a Si surface which are addressed during integration via a GeSi graded buffer as previously mentioned.

1.4 GaAs/Ge interface nucleation solutions via MBE

Prior to the onset of the GaAs/Ge/GeSi/Si research completed in this work, a detailed investigation of the GaAs/Ge nucleation process via MBE was investigated to determine on optimum nucleation methodology to provide monolayer scale control of the GaAs/Ge interface. While the complete analysis of these findings will not be discussed here (a complete research discussion can be found in references 43 and 44), since the “cap” layer of the GeSi graded buffer terminates with a 100% Ge surface, the major conclusions of this work have a direct impact on the starting point of the growth nucleation process used for the GaAs/Ge/GeSi/Si system. In fact, the initial stages of this work will require a verification that the nucleation process determined to provide monolayer control of the GaAs/Ge interface on the Ge wafer are also applicable to the Ge/GeSi/Si “virtual Ge” surface, which possess the added complication of residual TDD as well as a surface cross-hatched morphology.

Figure 1.10 shows the complete nucleation methodology developed for GaAs/Ge MBE nucleation. The key growth processes outlined for APB-free GaAs/Ge with effective blocking of interface diffusion include: 1) Use of (001) Ge wafers offcut 6° toward the [110], 2) 1000Å deposition of epitaxial Ge at 350°C, 3) 20 minute anneal of epitaxial Ge at 640°C, 4)~50 Å GaAs growth via migration enhanced epitaxy (MEE) at 350°C, 5) ~1000 Å GaAs growth at 500°C at a growth rate of ~0.1μm/hr, and

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Figure 1.10: Schematic details of GaAs/Ge interface nucleation used in this research to eliminate APB nucleation and minimize interface cross-diffusion. Complete growth details of the nucleation procedure are listed in the table along with effect of each nucleation step.

6) conventional GaAs epitaxy at 600°C as typical for a GaAs wafer. The use of offcut Ge has been demonstrated to help in the elimination of APB formation through the promotion of a “double-stepped” (see section 1.3.3) Ge surface.\textsuperscript{[36,38]} The inclusion of the epitaxial Ge layer was determined to be a key to obtaining APB and TD free films. Without the inclusion of a Ge epitaxial layer, nucleation on the carbon contaminated surface consistently resulted in the nucleation of APB’s and TD’s at the GaAs/Ge interface. Unlike MOCVD growth processes which regularly flow hydrogen gas, providing an in-situ surface cleaning mechanism, MBE growth is limited to the thermal
desorbtion of native oxides and surface contaminants. In order to mitigate this problem
with carbon contamination, epitaxial Ge layers were implemented in order to “bury” the
carbon contamination and prevent defect nucleation at the GaAs/Ge interface. After the
Ge epitaxy, the Ge surface was raised to “high” temperature (640°C) in order to promote
a “double-stepped” Ge surface, a necessary process in order to prevent APB nucleation.
GaAs epitaxy was then initiated at 350°C via migration enhanced epitaxy (MEE). The
MEE process involves the deposition of a single atomic layer of either the Ga or As
species, and allows conformal coverage of the Ge surface with a single, complete layer of
either Ga or As instead of a “mixed” interface nucleation layer. The 350°C temperature
provides several advantages. First, the low temperature “freezes-in” the double-stepped
Ge surface, prohibiting APB formation. Second, the complete monolayer coverage
minimizes interstitial site. Combined with the low thermal energy due to the growth
temperature, diffusion of atoms across the interface is minimized. The final initiation
step is the co-evaporation of GaAs at 500°C at a low growth rate (0.1 μm/hr). After the 10
monolayer nucleation at 350°C, this final nucleation layer is also inserted to minimize
interface diffusion by lowering the thermal energy during the initial 1000 Å of growth.
The GaAs surface, after ~1050 Å of nucleation growth, is then treated as an “epitaxially-
ready” (or epi-ready) GaAs surface for additional GaAs epitaxy. While this procedure is
not necessarily unique to providing an APB-free interface while simultaneously
minimizing cross-diffusion, the series of nucleation studies completed conclude that this
process successfully enables the desired interface control, simultaneously providing
diffusion control and eliminating APB formation. Additionally, while the vast number of
Figure 1.11: Plan view and cross-sectional TEM images typical for samples containing a) threads and APB's, b) APB's, and c) only misfit dislocations typical of strain relaxed layers. Optimization of the GaAs/Ge interface nucleation process enables the elimination of both APB and thread nucleation at the GaAs/Ge interface.

reports declaring APB-free nucleation via MOCVD seem to produce contradictory nucleation prescriptions for interface control,\cite{36,37,38,39} the results presented here have been “mimicked” by other researchers for MBE growth with similar success, indicating that the nucleation control is not “system-dependent” as could be argued from the MOCVD literature.\cite{45}

Figure 1.11 shows a series of cross-section and plan-view TEM images summarizing the impact of the interface nucleation procedure on the structural properties of the GaAs/Ge layers.\cite{43} The TEM images indicate the nucleation of threading dislocations as well as APB formation with only slight variations in the GaAs/Ge nucleation procedure. These results seem to indicate only a narrow growth-space over
which structural control of the GaAs/Ge interface is achievable, with the nucleation of the initial 30-100Å of GaAs growth being the most critical. Figure 1.12 shows the successful minimization of interface diffusion for the GaAs/Ge system using the nucleation prescription described above. Note that the SIMS data indicates that the elimination of the MEE nucleation “step” increases the diffusion of both Ga and As while still resulting in Ge out-diffusion below the SIMS detection limit. However, additional, more sensitive C-V measurements indicate GaAs doping profiles modified by Ge diffusion more than 2μm from the GaAs/Ge interface. These results conclude that the MEE nucleation step is vital in controlling interface diffusion in addition to promoting an APB-free interface.
1.5 GeSi Graded Buffer

As mentioned above, the use of Ge$_{1-x}$Si$_x$ system has been implemented in order to generate a low-dislocation Ge surface on a Si platform. This technique is unique from the "conventional" approach to GaAs/Si heteroepitaxy as indicated in figure 1.4, but the concept of integrating lattice mismatch systems through the use of graded buffers is not unique, and is frequently exploited in other materials systems.$^{46,47}$ Lattice mismatched material systems are commonly integrated through the use of graded layers since the gradual introduction of strain (lattice mismatch) through graded layers eliminates the need for the "total" system mismatch to be accommodated at a single heterointerface, resulting in films with fewer threading and misfit dislocations.$^{48}$ This fact is especially relevant for high mismatch systems such as GaAs/Si where $\sim$4% lattice mismatch must be accommodated, resulting in a TDD of $>10^9$ cm$^{-2}$ for direct heteroepitaxy.$^{49}$ For graded layers, TD’s nucleated in the initial layers for strain relaxation are also capable of relieving strain in subsequent graded regions, greatly reducing the number of TD’s necessary to accommodate the lattice mismatch compared to direct heteroepitaxy. This is the motivation behind the use of a graded GeSi layer to achieve low dislocation densities in 100% Ge layers on Si substrates.

Unfortunately, while the graded layer effectively reduces TD nucleation and therefore TD interaction, which is also responsible for the inefficient relaxation provided by the TD’s which are nucleated, the deepening cross-hatch characteristic in graded layers due to dislocation glide eventually restricts glide as the dislocations become "pinned" in deep valleys and results in dislocation “pile-ups”.$^{50}$ Once glide is impeded, the existing
TD’s can no longer contribute to relaxation and additional TD’s must nucleate for continued relaxation as grading continues and additional strain is incorporated, effectively negating the benefits of the graded layer.

However, in order to mitigate this problem in the Si$_{1-x}$Ge$_x$ graded buffer system, Fitzgerald et. al. have recently developed a novel process where a chemical mechanical polishing (CMP) step incorporated into the graded layer has resulted in a “freeing” of the TD pile-ups so that the existing TD’s can continue to glide and efficiently relieve strain.$^{[35,50]}$ Through “polishing out” the valleys (surface morphology) associated with the pinning sites for TD pile-ups, the additional nucleation of TD’s has been successfully suppressed, resulting in a 100% Ge layers on Si with “true” TDD’s of $1 \times 10^6$ cm$^{-2}$ to date with further TD reduction predicted after process optimization (temperature, grading rate, placement of CMP, etc.). It should be noted that, while other GaAs/Si growth techniques have reported TDD’s as low as $-1 \times 10^6$ cm$^{-2}$,$^{[16]}$ the “counting” techniques used (TEM, etch pit density (EPD), electron beam induced current (EBIC), etc.) are unable to distinguish between a single TD and a pile-up of multiple TD’s, resulting in films where the “true” TDD can be substantially higher than reported. This fact is supported by $\tau_p$ measurements, which have not exceeded $\sim 3$ ns even though the TDD’s reported ($< 1 \times 10^6$ cm$^{-2}$) should yield lifetimes in excess of 10 ns.$^{[16,17,18,19,20,21]}$ As will be discussed in section 3.4, minority carrier lifetime is a far more reliable characterization parameter than TDD on which to predict final device performance. Figure 1.13 shows a schematic of the current SiGe grading methodology used to produce a “true” TDD’s of $1 \times 10^6$ cm$^{-3}$, the lowest TDD reported for a fully relaxed Ge layer on Si. A further discussion of the GeSi
Figure 1.13: Ge₅Si₁₋ₓ grading scheme utilizing a CMP process during the grade in order “free” pinned threading dislocations. (after 35)

graded buffer growth parameters and dislocation reduction mechanisms is beyond the scope of this dissertation. However, since the quality of the GeSi graded buffer is of paramount importance to the III-V material quality achievable in this and any other GaAs/GeSi integration, a more detailed description of the GeSi graded buffer growth has been provided by the researches supplying the SiGe graded buffers for this work and can be found in Appendix A.

1.6 Research goals and specific approach

The paramount goal of this research is to demonstrate record-quality GaAs/Si devices through the exploitation of a GeSi graded buffer. The current implementation of the GeSi graded buffer effectively controls the nucleation of threading dislocations while terminating with a 100% Ge surface. However, the ultimate goal is to achieve GaAs/Si with TDD’s similar to the Ge capping layer. Therefore, while the TDD has been
significantly reduced in the Ge "cap" layer, the ability to achieve a high quality GaAs layer is also limited by the ability to control the well-known problems of the low-mismatched GaAs/Ge interface (instead of the high-mismatch GaAs/Si interface).

The goals of this work are to exploit and build beyond the GaAs/Ge nucleation methodologies developed by R.M. Sieg, prior to this work, on Ge wafers, and determine to what extent the Ge cap of the GeSi graded buffer mimics an ideal Ge surface. The relevant issues considered include the elimination of APB formation, the reduction of interface cross-diffusion responsible for spurious p-n junction formations, and the nucleation of additional threading dislocations which would undermine the benefit of the GeSi graded buffer scheme. In addition to these structural characterizations, the electrical quality of the III-V layers will also be investigated. Electrical characterization will include the determination of minority carrier lifetimes and correlations with theoretical dependence on threading dislocation density. Finally, performance of III-V devices will be used as the ultimate characterization of the GaAs/Si material and interface quality. For this purpose, single-junction solar cells were chosen as the vehicle for characterizing the impact of the complete GaAs/Si integration methodology. Solar cells are both large area and sensitive to minority carrier properties, providing especially strict requirements for material quality. Additionally, devices will be grown on both GaAs and Ge substrates for comparison. These comparisons will allow effective separation of the material quality limitations and limitations introduced during the growth procedure and device processing steps.
1.7 Dissertation layout

The remainder of this dissertation is organized as follows. Chapter 2 is a reference chapter providing a brief description of the materials characterization techniques used in this work. Chapter 3 is a second reference chapter concentrating on device characterization. Specifically, chapter 3 deals with important design considerations and characterization issues related to photovoltaic solar cells which are used in this work as a vehicle for determining GaAs/GeSi material quality. Chapter 4 investigates the GaAs nucleation on the Ge/GeSi/Si graded buffer substrates, including APB formation, cross-diffusion, and TDD control. Additionally, characterization of the GaAs material quality via minority carrier lifetime is investigated as a function of the interface nucleation conditions and surface preparation procedure. Chapter 5 addresses the impact of the interface nucleation methodology on device performance. Specifically, chapter 5 considers the impact of the interface nucleation (Ge epitaxy in particular) on the I-V characteristics of simple p-n junction diodes. Finally, chapter 6 addresses the application of GaAs/Ge/GeSi/Si growth to the fabrication of large area, single junction GaAs/AlGaAs and GaAs/InGaP solar cells. Chapter 6 discusses modeling for optimum single-junction device design as well as the impact of residual TDD, surface morphology, surface defects, and device processing on device performance. Chapter 7 then concludes this dissertation with a brief discussion of future research directions and the impact of this work on those paths.
1.8 References


CHAPTER 2

GROWTH AND CHARACTERIZATION TECHNIQUES

2.1 Molecular beam epitaxy (MBE)

All MBE samples for this research were grown in a modified Varian GEN II solid source Molecular Beam Epitaxy (MBE) system, shown in a detailed schematic in Figure 2.1. MBE is an atomic layer film growth technique that utilizes an ultra high vacuum (UHV) environment to produce high quality layers with monolayer precision. Figure 2.2(a) shows a simplified schematic of the concept behind MBE growth. The material sources, or cells, contain high purity elements such as Ga, As, Al, In, etc., combinations of which are used in film growth. Upon heating of a cell, a molecular beam escapes from the cell orifice as the source material either evaporates or sublimes. The molecular beam, the intensity of which is dependent on the cell temperature, is then incident on a heated substrate which is in the path of the molecular beam. Due to the locations of the various cells in relation to the substrate, with some cells mounted in “upward” looking positions while others are in “downward” looking positions, the substrate is typically rotated for improved uniformity across the wafer.
Figure 2.1 Detailed schematic of Varian Gen II molecular beam epitaxy system.
Figure 2.2: (a) Schematic of evaporation during molecular beam epitaxy from source cells to the heated substrate. As shown, growth is dependent on the molecular beam's "line-of-sight" to the substrate surface.\textsuperscript{[2]}

(b) Schematic of MBE system set-up in which the main components are labeled. Note the location of the high energy electron diffraction (HEED) gun with respect to the substrate. The HEED gun is the electron source for the RHEED patterns viewed on the fluorescent screen.\textsuperscript{[2]}
As seen in figure 2.2(a), the source cells each have a shutter located directly in front of them that can be closed in order to block the evaporating beam from reaching the growth surface. Also, not as clear from the figure, the entire surrounding chamber is cooled by liquid nitrogen. This not only assists in keeping a low pressure, clean chamber, but it also assists in the gettering of the source materials. With the exception of arsenic which does not adhere completely like the other sources, all of the evaporated material will “stick” to the cold chamber walls upon contact. Therefore, a source will not participate in growth at the substrate unless the molecular beam from the cell has a direct “line-of-sight” path to the substrate. If the shutter in front of a source is closed, the source will not contribute to growth even if it is at a temperature where evaporation is occurring. It is this fact that makes MBE such a useful technique for creating structures with abrupt interfaces and allows the technique to have monolayer control over the growth thickness. While further details of the MBE growth process are not required for the results presented in this thesis, many excellent textbooks which review MBE technology in detail are available and recommended for further information.¹,³,⁴,⁵

Typically, growth of high quality MBE GaAs material is performed at a substrate temperature of around 600°C. For the growth of GaAs, an As₂ (dimeric As) to Ga beam equivalent pressure (BEP measured by an ion gauge) ratio of ≥10:1 is required. (15-20:1 for an As₄ arsenic source) This ratio, which is necessary to defeat the low As sticking coefficient, ensures sufficient As adatom adsorption for bonding to Ga atoms at the growth surface and inhibits the formation of Ga-Ga bonds which will destroy the GaAs crystalline structure and roughen the growth surface. On the MBE system used for these
experiments, a valved arsenic “cracking” zone typically heated to 900°C provides an As$_2$ arsenic source from the intrinsic As$_4$ evaporant. However, by simply decreasing the cracking zone temperature, an As$_4$ source is also readily available. In this research, As$_2$ is used exclusively as the As species. The valved arsenic source provides two benefits. (1) The arsenic beam pressure is directly controlled by the valve position. With valve settings from 0.0-240.0 (arbitrary units) available in increments of 0.1 units, (0.0 corresponding to a “shut” position or no arsenic flux and 240.0 corresponding to “full open” or a maximum arsenic flux), the pressure can be changed quickly but also set accurately depending on the gallium flux if a specific As:Ga BEP is desired. (2) The valve allows for almost immediate termination of the arsenic background pressure when the valve is closed (i.e. very fast transients of the arsenic background pressure). This is in contrast to conventional arsenic sources that are only shuttered in a similar fashion to that discussed for the other sources. Closing the shutter does not completely eliminate the arsenic background, and the arsenic pressure must be controlled by cell temperature, which has a slow thermal transient as opposed to the immediate mechanical movement of the valve position. While the As cracker valve is still shuttered, the combination of closing the valve and the As shutter simultaneously allows for termination of the As flux to a BEP on the order of $10^{-9}$ torr in seconds where it would require minutes to achieve a similar background with a non-valved, temperature controlled arsenic source.

In addition to the sources and substrate which are the necessary components of the MBE growth process, additional characterization equipment is helpful in order to improve the reproducibility and quality of the growth material as well as allow for the
addition of scientific studies not possible through monitoring ex-situ growth results. In particular, two techniques that are vital to the control of material quality, alloy composition, and thickness in MBE are infrared pyrometry and reflection high energy electron diffraction (RHEED). While RHEED has many applications for controlling the MBE growth process and will be discussed in detail in the next section, the technique of infrared pyrometry provides information related to only one growth parameter, the substrate surface temperature. Although the substrate heater temperature can easily be measured by a thermocouple near the substrate, the thermocouple is not in direct contact with the substrate mount or the substrate surface. Therefore, since it depends strongly on the substrate mounting technique, and whether indium-bonded or indium-free mechanical mounts are used, the actual surface temperature can differ from the thermocouple temperature by more than 100-200°C. Here, in order to obtain accurate substrate temperatures, the technique of infrared pyrometry is typically used. Although the details of the technique can be found elsewhere and will not be discussed in further detail here, the importance of this capability is that it is an optical measurement not requiring surface contact and enabling surface temperatures to be measured accurately regardless of mounting technique. Since the optimization of many growth mechanisms is strongly temperature dependent, the ability to control the surface temperature greatly increases material quality and reproducibility. Unfortunately, due to changing emissivity and widening of the bandgap as substrate temperatures are lowered, the detection wavelength used for the infrared pyrometer is not applicable below a GaAs surface temperature of approximately 450°C. For low growth temperatures, 350°C is used extensively in this
research, the growth temperatures quoted are thermocouple temperatures rather than from the optical pyrometer.

2.2 Reflection high energy electron diffraction (RHEED)

Reflection high energy electron diffraction (RHEED) is currently the most useful surface analytical technique for in-situ characterization in MBE. In RHEED, a collimated monoenergetic electron beam is directed toward the wafer surface at a glancing angle of typically less than one degree.\(^2\) The MBE schematic in figure 2.2(b) shows the position of the two components of the RHEED system, the electron gun and the viewing screen, with the wafer in the growth position. Typically, a phosphor screen is placed opposite the electron gun and records electrons diffracted from the wafer surface. As can be seen in Figure 2.2(b), due to the glancing angle of incidence for the electron beam, the RHEED setup does not interfere with the source cells and is used while the substrate is in the growth position. This is an important point, one which allows RHEED to be a useful in-situ technique for analyzing the substrate surface during epitaxy. Figure 2.3 shows a typical RHEED reconstruction patterns for a GaAs surface along the [110] and [1\(\bar{1}\)0] crystallographic directions. For the purposes of MBE, RHEED patterns can provide much quantitative as well as qualitative growth information. However, regardless of the technique, the most useful aspect of RHEED is, without a doubt, the ability to provide reproducible system as well as growth conditions and therefore reproducible material and device quality. Various analysis techniques take advantage of RHEED intensity variations,\(^8,9\) oscillation frequencies,\(^10\) oscillation phases\(^11\) and\(^1\)
Figure 2.3: Typical GaAs RHEED patterns along the a) [110] and b) [110] wafer directions. This particular reconstruction is known as a (2x4) or c(2x8) reconstruction.

"streak" numbers and spacing.\textsuperscript{[12,13,14]} While a great deal of information like orientation of a stepped surface, surface atom reconstruction, surface growth mechanism, etc.\textsuperscript{[22]} can be derived from the RHEED pattern data, the only applications discussed in further detail here will be the ones which were directly implemented during growth or characterization of layers for this work.

RHEED was used for two applications during MBE growth for this research. First, the RHEED intensity oscillates during two-dimensional growth with an oscillation period corresponding to the deposition of a single GaAs monolayer.\textsuperscript{[15]} The (room temperature) monolayer thickness of GaAs on an (001) surface is 2.825 angstroms, where one monolayer is defined as a single Ga plus a single As layer and corresponds to $\frac{1}{2}$ of the GaAs unit cell height. Thus, RHEED intensity oscillation frequency in hertz multiplied by 2.825 yields the growth rate in angstroms/second. The AlGaAs rate and
composition can be determined by RHEED oscillation measurements as follows. First, we recognize that the difference in lattice constants between AlAs and GaAs ($\Delta a/a \sim 0.1\%$) is negligible for this measurement which is typically accurate to $\sim 1\%$. Then, since for unity sticking coefficients the AlGaAs growth rate is given by:

$$R_{(Al,Ga_{1-x},As)} = R_{(AlAs)} + R_{(GaAs)}$$

(2.1)

it follows that

$$f_{(Al,Ga_{1-x},As)} = f_{(AlAs)} + f_{(GaAs)}$$

(2.2)

where $f$ is the RHEED oscillation frequency. It follows then that measuring the AlGaAs RHEED oscillation frequency and scaling by 2.825 gives the growth rate, and the composition can then be obtained by measuring either the corresponding AlAs or GaAs rate via equation 2.3.

$$x = \frac{R_{(AlAs)}}{R_{(Al,Ga_{1-x},As)}} = 1 - \frac{R_{(GaAs)}}{R_{(Al,Ga_{1-x},As)}}$$

(2.3)

RHEED intensity oscillations are usually attributed to island-based (but still layer-by-layer) growth where there is a maximum surface disorder obtained for $\frac{1}{2}$ monolayer (lowest intensity) and a minimum surface disorder occurring when a full monolayer is completed (highest intensity). This simple model explains the decay of oscillation amplitude with continuing growth and the lack of oscillations under growth conditions where where full two-dimensional growth occurs (since in this case the surface remains
ordered during the growth process). However, detailed studies of the RHEED oscillation process hint at additional complexities. Reference 4 provides a detailed review of RHEED intensity oscillation phenomena.

The second application for RHEED during this work was for monitoring surface periodicity and roughness. The RHEED diffraction pattern directly reflects the periodicity, figure 2.3, and roughness of the crystal surface, and can therefore be used to identify and monitor the surface reconstruction and identify the onset of three-dimensional, polycrystalline, or amorphous growth modes. For example, an oxide-coated surface is essentially amorphous and does not show periodicity-related diffraction streaks. In this dissertation, this application was more qualitative than quantitative, providing a means of verifying the surface quality and reconstruction during the GaAs/Ge interface nucleation procedure. Due to the surface sensitivity of the RHEED technique, surface reconstructions can be used to determine the onset of anti-phase domain formation within a few monolayers of the GaAs/Ge interface as detailed in reference 16.

2.3 Auger electron spectroscopy (AES)

A second characterization technique available on the MBE system at OSU is Auger electron spectroscopy (AES). Although not directly available in the MBE growth chamber, the Auger system is located in an adjacent chamber which is connected through UHV. The Auger technique detects electrons emitted from a sample due to an incident electron beam, 5keV in these studies. The Auger transition involves three particles and is schematically demonstrated in figure 2.4. The incident electron (e') ionizes a core
electron, K level in this example, leaving a hole, transition 2 in figure 2.4. The hole is then filled by a higher energy electron “falling” from another core level, L_l in this example, transition 3. For the Auger process, rather than the excess energy from the L_l-K transition being emitted as an x-ray, the energy is transferred to an electron in the same or a higher energy level, L_III in this example, providing that electron with enough energy to “escape” to the vacuum level, transition 4. The energy in excess of that needed to escape to the vacuum level is the kinetic energy of the electron and is well defined based on the core level energies involved in the Auger transition. Since core levels are involved, the Auger energy is relatively insensitive to the matrix/bonding of the atom. For this example, the Auger electron energy characteristic of the KL_lL_III transition is given by:

\[ \text{Auger electron energy} = (E_{L_l} - E_K) - E_{L_III} \]  \hspace{1cm} (2.4)
Figure 2.5: Spectrum of KLL, LMM, and MNN Auger electron energies and the elements/atomic numbers to which they correspond. Due to the well-defined core energy levels, the Auger electron energies are also well-defined.\textsuperscript{[17]}
Figure 2.5 shows the electron energies characteristic of the KLL, LMM, and MNN Auger transitions as a function of atomic number. Since the electron energies are on the order of 1000 eV, the escape depth for the Auger electrons is only on the order of 10Å, making the Auger technique extremely surface sensitive since electrons generated deeper than ~10-30Å cannot be detected external to the sample surface. However, depth AES profiling is available through destructive ion sputtering of the surface atoms. In this work, AES was exclusively used as a qualitative technique to monitor the cleanliness of the growth surface, Ge and GeSi, prior to GaAs deposition, looking for carbon and oxygen contamination in particular. A more detailed discussion of AES is provided in reference 17.

2.4 Secondary ion mass spectroscopy (SIMS)

Secondary ion mass spectroscopy (SIMS) is a powerful characterization technique for determining the chemical composition of a semiconductor film, particularly for quantitative measurements of low levels of impurities and dopants, less than 1 part per million. SIMS is a destructive process where an ion beam is used to sputter material, which is subsequently monitored by a mass spectrometer. The ion beam, typically ions with an energy of 10-20 keV, transfers energy to the surface atoms, causing them to be "ejected". The ejected atoms are predominately neutral, but ~1% are ionized and can be detected by the mass spectrometer. (Note that the ionization rate of an atom is dependent on the sputtering beam, i.e O₂⁺ and Cs⁺. Typically, multiple scans with different sputtering ions is required in order to accurately detect a wide range of atoms.) The mass
spectrometer measures the ionic spectrum through the mass/charge ratio (m/e), with each element having a characteristic mass/charge distribution. For example, the atomic mass of As is 75. Hence among the possible mass/charge values are singly ionized As\textsubscript{1} giving m/e = 75, doubly ionized As\textsubscript{1} with m/e=37.5, singly charged As\textsubscript{2} with m/e=150, singly charged As\textsubscript{3} with m/e=225, and singly charged As\textsubscript{4} with m/e=300. The intensity of the various ions is characteristic of the material as well as the ionizing beam (ion species and kinetic energy). Since SIMS necessarily requires material sputtering, it is also a depth profiling technique. While the mass spectrometer is used to monitor “counts/time”, determining the sputtering rate by measuring the depth of the sputtering pit after the measurement enables the time axis to be converted to a depth scale. Additionally, a more quantitative measure of atomic concentrations is typically obtained from the monitored “counts” through a calibration standard.

2.5 Scanning electron microscopy and electron beam induced current (EBIC)

Like Auger, scanning electron microscopy (SEM) is a characterization technique where electron emission from a sample surface is monitored while being “probed” with a focused electron beam. Figure 2.6 shows a simplified schematic of the SEM setup similar to that of the XL-30FEG used at OSU.\textsuperscript{[18]} The series of electromagnetic lenses enables the e\textsuperscript{−} beam to be focused to approximately 2-10nm in diameter. During the imaging process the focused electron beam is rastered across the surface and the image contrast is determined by the number of secondary electrons detected. For SEM, electron beam energies of 5-20 keV are typically used, resulting in a range of atomic scattering
events and a broad spectrum of electron energies, including Auger electron, secondary electrons, and backscattered electrons, as well as x-rays being generated. Figure 2.7 shows a schematic representation of "where" in the sample these characteristic signals are generated. The depth is dependent on the energy of the electrons being monitored since the electron energy will determine the "escape depth" of the electron as shown in figure 2.8.\textsuperscript{[19]} For this work, the SEM was primarily used SE mode, which detects secondary electrons. Secondary electrons are generated through multiple scattering events and interband transitions and have energies from 1-50 eV, resulting in good spatial resolution as well as detection in close proximity to the sample surface, < 1000Å, figure 2.7. Consequently, detection of secondary electrons is sensitive to surface morphology, in contrast to back scattered electrons which are more sensitive to atomic mass.

Figure 2.6: Simplified schematic of a SEM column after Reference 18.
Figure 2.7: Schematic representation of the pear-shaped volume of particle emissions (electron and X-ray) generated from an incident electron probe, similar to that used in SEM analysis. Note that the various electron emissions have energies which determine the escape depth and therefore surface sensitivity of the monitoring technique.

Figure 2.8: Electron mean free path or scattering length in an elemental solid versus electron energy. In the case of SEM and TEM, the electron path can be considered as the penetration depth or the escape depth of the electron beam at the growth surface.
The SEM "set-up" is also applicable to an imaging technique known as electron beam induced current (EBIC). When generating an EBIC image, the current flowing through a p-n junction (or schottky) is monitored. Therefore, a sample with a junction as well as electrical contacts is necessary for EBIC. The incident electron beam is used to generate electron-hole-pairs (ehp's), which are then collected across the junction to generate current, similar to the operation of a solar cell. Since the focused e' beam has a diameter of 20-100Å, the rastering of the beam across the surface results in a high resolution image which effectively measures the collection efficiency as a function of position across the sample. Additionally, since EBIC measures the collection efficiency, the presence of electrically active defects, which result in the recombination of ehp's, results in a "dark" region in the EBIC image. Figure 2.9 shows an EBIC image where

Figure 2.9: EBIC image used to determine TDD. The black spots indicate regions of high recombination characteristic electrically active defects like threading dislocations.
threading dislocations are delineated by dark spots due to the recombination near the
defect. The presence of electrically active anti-phase domains is also easily detected
through EBIC analysis. EBIC is complementary to TEM with respect to threading
dislocation density measurements, since EBIC performs well below \(10^6 \text{ cm}^{-2}\) density
levels where TEM is inapplicable.

### 2.6 Transmission electron microscopy (TEM)

Transmission electron microscopy (TEM) is an electron beam analogue to optical
microscopy for thin, transparent samples. As the electron beam is transmitted through the
sample, scattering of the high energy electrons produces the TEM image. For TEM,
electron beam energies are typically 100-200keV, as opposed to 10-20 keV used for
SEM. Unlike optical techniques where resolution is limited by the wavelength of the
incident photons, \(\lambda_{\text{photon}} \sim 300-400\text{nm}\) for blue light, the equivalent electron wavelength,
\(\lambda_{\text{electron}} (100\text{keV}) \sim 0.037\text{Å}\), enables magnification down to the atomic scale. However,
due to the penetration depth of the electrons, \(< 200\text{nm}\), the TEM samples must be thin in
order for the electrons to be transmitted and detected. Therefore, a complex sample
preparation sequence is required in order to obtain thin sample areas near the desired
interfaces for imaging. For cross-sectional TEM, the sample preparation technique is
outlined in figure 2.10. The "samples" are originally glued together with a pair of
"samples" surface-to-surface at the center of a wafer stack. Note that the other layers in
the stack are not imaged and are typically scrap pieces of similar material with
comparable ion milling rates. The wafer stack is then diced to provide cross-section slabs
Figure 2.10: Sequence of cross-section TEM sample preparation procedures. a) Two “samples” are glued surface-to-surface in a stack along with other scrap samples to provide thickness. b) Sample stack is diced into sections/slabs as thin as possible. c) The sample slab is ground/polished down to ~20μm thick. d) An ion mill is used to further thin the sample, generating a hole at the desired sample-glue-sample interface. e) Cross-sectional view of sample slab after ion milling. Near the hole the sample is thin enough for electron transmission.

for imaging of the desired interfaces. The sample must be thinned to less than 200nm for electron transmission by polishing, grinding, and finally ion milling which produces a hole at the sample-glue-sample interface. As shown in figure 2.10(e), the regions near the ion mill hole are sufficiently thin to allow electron transmission. Figure 2.11 shows a series of cross-sectional TEM images demonstrating the wealth of information which can be obtained via this technique. Since structural defects provide a scattering center for the electron beam, crystalline defects such as APB’s and threading dislocations are clearly imaged via this technique. Note that TDD’s less than $10^7 \text{ cm}^{-2}$ are not practically imaged by TEM due to the high magnification. Below a TDD of $10^7 \text{ cm}^{-2}$ multiple fields of view
would be necessary in order to image a single threading dislocation. However, TEM enables accurate TDD measurements above $10^7 \text{ cm}^{-2}$ where other methods such as EPD and EBIC become inaccurate. Additionally, TEM can also distinguish between individual layers in a multi-layer structure if the electron beam scattering contrast is sufficient, as shown in figure 2.11(c). In practice, this means that compositional but not doping differences are observable.

2.7 Capacitance-voltage dopant profiling

Capacitance-voltage (C-V) profiling provides an accurate method for determining carrier concentration in a material. By varying the depletion region formed by a p-n junction or Schottkey contact with a DC bias, capacitance variations as a function of depth
can be measured. A small-signal AC component added to the DC bias can be used to vary the edge of the depletion layer and determine \( C \) by:

\[
C = A \times \left( \frac{dQ}{dV} \right)
\]

(2.5)

where \( Q \) is the charge per unit area and \( A \) is the contact area. The derivative of the C-V curve can then be related to the carrier concentration by:[20]

\[
n(W_{dp}) = \frac{-C^3}{e \times \varepsilon \times A^2 \left( \frac{dC}{dV} \bigg|_{W_{dp}} \right)^{-1}}
\]

(2.6)

where \( W_{dp} \) is the depletion layer thickness and \( \varepsilon \) is the material dielectric constant. Since \( W_{dp} \) is a function of the reverse bias voltage, equation 2.6 provides a depth profile of the carrier concentration. Note that in order to vary the depletion layer thickness for the C-V measurement the sample must be thick enough to have an undepleted region at zero-bias. For low doping, the zero-bias depletion thickness can exceed tens of microns. However, provided a thick enough layer, C-V enables an accurate measure of carrier concentration between \( \sim 10^{13} \) and \( 10^{19} \) cm\(^{-3}\).

2.8 Etch pit density (EPD)

Similar to EBIC, EPD measurements were used in order to accurately determine threading densities in both the GaAs/Ge and GaAs/GeSi systems. Combined with EBIC, EPD is essential for determining TDD's below the practical TEM measurement limit of \( 1.0 \times 10^7 \) cm\(^{-2}\). In this technique, the GaAs or Ge surface is etched in a solution whose
etch rate is effected by the presence of a dislocation. This etch rate variation delineates the dislocations by creating an etch "pit", which can then be counted with the aid of an optical microscope. For dislocation counting on the GaAs epilayers, two solutions, one containing CrO$_3$ and HF acid and the other CrO$_3$ and HCl acid were used.$^{[21,22]}$ The two solutions enabled dislocation densities on the order of $1 \times 10^4$ cm$^{-2}$ to be recorded for the GaAs growth on Ge substrates. This value corresponds well to the initial dislocation density of the Ge substrate. Figure 2.12 shows a resultant surface image of the EPD sample. The patterns on the surface are formed by etch pits which occur at the dislocation core. Counting these pits and dividing by the area gives the dislocation density. While not shown here, EPD measurements of the GaAs/GeSi growths were also successfully completed via this technique and resulted in EPD numbers corresponding to those determined for the Ge capping layer of the GeSi graded buffer.

Figure 2.12: Surface image of resulting etch pits from the CrO$_3$/HF etchant on GeAs/Ge.
2.9 Time resolved photoluminescence (TRPL)

Photoluminescence (PL) is a non-destructive measurement in which electron-hole pairs are continuously photoinjected, typically by a laser beam whose photon energy is well above the semiconductor bandgap, and the resultant luminescence produced by radiative recombination is measured as a function of photon wavelength, typically using a monochromater. Time-resolved photoluminescence (TRPL) is a similar technique where only a single luminescence wavelength, the band-band wavelength, is continuously monitored after the photoexcitation source is abruptly terminated. The decay transient of the band-to-band luminescence is monitored as the semiconductor returns to its' equilibrium state via electron-hole recombination. Since the incorporation of states/levels in the bandgap (due to doping, material defects, etc) will result in non-radiative recombination, or radiative recombination at a wavelength other than the bandgap energy, the amount of band-to-band recombination is reduced as electrons in the conduction band are lost to other recombination paths. Therefore, band-to-band decay transient is a measure of the photo-injected electron “lifetime” in the conduction band. For a very thick film under low-level injection where the photoinjection is far from the surface or film/substrate interface, the TRPL decay will simply reflect the minority carrier lifetime of the bulk material. However, while this is a useful measure for determining minority carrier properties, such a measurement is impractical since the above-bandgap excitation is absorbed near the sample surface and not deep within the film. Because of this, the decay rate is dominated by recombination at the semiconductor/”air” interface, which typically contains a very high density of surface states. Therefore, a double-
heterojunction (DH) structure is often used. In this work, an AlGaAs/GaAs/AlGaAs DH structure was used as shown in figure 2.13. The GaAs buffer is inserted to define the proximity of the "actively" measured GaAs region (DH) to the GaAs/Ge interface and will be discussed in later sections. For this structure, the AlGaAs/GaAs interface provides a lower interface recombination rate than the GaAs/"air" interface and allows for a better determination of the bulk GaAs properties. For the DH structure, the TRPL decay lifetime is determined by both the interface recombination velocities as well as the bulk minority carrier lifetime. Assuming that the interface recombination velocities at both interfaces of the DH structure are equivalent, the TRPL lifetime can be defined by:[23]

\[
\frac{1}{\tau_{TRPL}} = \frac{1}{\tau_p} + \frac{2 \times S}{d} \tag{2.7}
\]
\[ \frac{I(t)}{I_0} = \exp \left( -\frac{t}{\tau_{TRPL}} \right) \quad (2.8) \]

where \( \tau_{TRPL} \) is the TRPL decay lifetime, \( \tau_p \) is the bulk minority carrier lifetime for n-type GaAs (a function of Schockley-Read Hall, band-band, and Auger recombination), \( S \) is the interface recombination velocity, \( d \) is the DH GaAs layer thickness, \( I(t) \) is the band-band luminescence intensity at time \( t \), and \( I_0 \) is the luminescence intensity at \( t=0 \). Figure 2.14 shows a series of TRPL decay exponentials for varying GaAs thicknesses, \( d \).

\( \tau_{TRPL} \) is determined through fitting of the decay exponentials with equation 2.8. Figure 2.15 shows a plot of the \( 1/\tau_{TRPL} \) versus \( 1/d \) for the multiple GaAs DH structure thicknesses. From equation 2.7, figure 2.15 can be used to extract the minority carrier lifetime and the interface recombination velocity from the y-intercept and slope respectively. The “linearity” of the data points is a measure of the reproducibility in both \( \tau_p \) and \( S \) from run-to-run, and is a necessary element of determining \( \tau_p \) and \( S \) via this technique. For the samples of figure 2.15, excellent uniformity across the sample set is evident in the linear data fit. However, as shown in the figure, \( \tau_{TRPL} \) contains a \( \pm 10\% \) error via this technique and can substantially impact the extracted values. In this work, a minimum of 3 TRPL data points were typically used in order to provide a more reliable curve fit and a better determination of both \( \tau_p \) and \( S \), both of which are critical parameters for designing solar cells and other minority carrier devices.
Figure 2.14: "Raw" TRPL decay data for a series of GeSi DH samples.

Figure 2.15: Plot of $1/\tau_{TRPL}$ vs. $1/d$ dependence for GaAs/GeSi TRPL lifetimes extracted from Figure 2.14. (±10% error for TRPL exponential fitting) Curve fitting provides $\tau_p$ and S values from equation 2.7.
2.10 References


7 Ircon Technical Notes TN106, “Radiation Thermometry in Molecular Beam Epitaxy”.


CHAPTER 3

GROWTH AND CHARACTERIZATION OF HIGH EFFICIENCY SOLAR CELLS

Since the device goal of this research is the growth and fabrication of high efficiency single-junction solar cells, it is relevant to provide a brief discussion on solar cell design and fabrication. Additionally, since this dissertation includes a detailed analysis of solar cell characterization measurements as a means to optimize device design as well as a vehicle for determining material quality, a review of these techniques and the information they provide is also required. Finally, a review of the current status of GaAs/Si solar devices is presented, including an analysis of the limitations which GaAs/Si integration has presented prior to this work. These results provide a realistic context for which the results of this research must be gauged in order to demonstrate the capability of the GeSi graded buffer as a viable integration methodology.

3.1 Single-junction solar cell design

Figure 3.1 shows a schematic of a single junction AlGaAs/GaAs cell design used for this research. Figure 3.2 provides a band diagram of the same cell structure. As shown, the single-junction cell is a simple p-n junction diode, with the exception of the
Figure 3.1: Schematic of a simple AlGaAs/GaAs single-junction solar cell structure.

back surface field (BSF) (Al$_{0.1}$Ga$_{0.9}$As) and the window layer (Al$_{0.85}$Ga$_{0.15}$As), which is operated under illumination for power generation. For the p-n design shown, photo-injected electrons in the p-emitter and photo-injected holes in the n-base must be collected across the p-n junction in order to generate photo-current and therefore operate as a power supply device. Therefore, ability to 1) absorb photons to generate electron-hole pairs (ehp’s) and 2) “collect” the minority carriers prior to recombination will determine the efficiency with which the solar cell converts the available photon energies. However, one fact about photon absorption must be recalled. Since a photon’s total energy is absorbed by a single electron, generating a single ehp, only those photons with an energy equal to $E_g$ will result in the maximum energy conversion efficiency, $\eta$, of 100%. As the photon energy becomes larger than $E_G$, a single ehp is generated, but energy is lost in the form of heat as the electron thermalizes back to the conduction band edge. Therefore, a photon with $E=\hbar\nu=2*E_g$ which generates only a single ehp will have a maximum efficiency of 50%, assuming all photons of that energy are absorbed and
collected across the p-n junction prior to recombination. For this reason, the maximum (ideal) efficiency of a single-junction solar cell of a given bandgap is dependent on the incident solar spectrum.

### 3.2 Solar spectrum for space application

Figure 3.3 shows the spectral content of three radiation sources, a 6000K black body, Air Mass Zero (AM0), and AM1.5. The “Air Mass” nomenclature is defined by AMn = Air Mass (n) = 1/cos θ, where θ is the angle of the sun overhead from a position...
on earth. AM0 is chosen to designate the solar spectrum as measured outside the earth's atmosphere and is not defined by this nomenclature. The power density content of the AM0 spectrum is 1.353 kW/m². AM1.5 is a common reference used for terrestrial solar cell characterization where the total power density content is 1 kW/m². From Figure 3.3, it is evident that the earth's atmosphere is responsible for absorbing a significant quantity of the "blue" and ultra-violet spectrum, as well as other discrete wavelengths. Additionally, it is noted that the solar spectrum is broadband (~200nm to greater than 2.5μm), indicating that no single material will efficiently collect the entire solar spectrum. This, in fact, is the driving force behind the development of "multiple"-junction solar cell which are the current standard for space applications. However, since this work will consider only single-junction cell designs, multiple-junction cell design and characterization will receive no further discussion in this dissertation.
Considering the single-junction cell, although no value of $E_g$ can efficiently collect the entire spectrum, the energy conversion efficiency for a given $E_g$ can be determined by integrating the power collected by a single $E_g$ across the entire solar spectrum and dividing by the total incident solar energy ($1\text{ kW/m}^2 = \text{AM1.5}, 1.353\text{kW/m}^2 = \text{AM0}$). Figure 3.4 shows such a calculation for the theoretical maximum efficiency versus bandgap for both the AM0 and AM1.5 solar spectrum.\textsuperscript{[2]} (Note that due to energy loss for photons larger than the bandgap (thermalization) and photons smaller than $E_g$ which are not absorbed, the maximum conversion efficiency is limited to less than 30%). As shown, the GaAs bandgap (1.425eV at 300K) is ideally suited for a single-junction cell design for either space (AM0) or terrestrial (AM1.5) applications. However, as discussed in chapter 1, primarily due to the cost of GaAs cells compared to their Si counterparts, Si cells are used almost exclusively in terrestrial applications. For this
work, the focus will be on single junction GaAs solar cells for space application, and optimization based on the photon distribution of the AM0 solar spectrum.

### 3.3 Design of single-junction solar cells

#### 3.3.1 Solar cell efficiency parameters

In order to understand the parameters associated with solar cell quality, which will be referenced throughout this dissertation, a brief introduction of the parameters commonly used to characterize the efficiency of solar cells is presented. Figure 3.5 shows common I-V curves for a solar cell structure in the dark and under illumination. Under illumination, the I-V curve is “pushed-down” into the 4th quadrant where both I and V have negative values as shown, indicative of a power supply device. The light I-V curve is the result of the superposition of the “ideal” diode I-V response ($I_D$) with a constant current source ($-I_L$) supplied by the photoinjected carriers, equation 3.1, where $I_0$ is the diode saturation current.
The parameters commonly used to characterize a solar cell are the short-circuit current, $I_{sc}$ (or short circuit current density, $J_{sc}$), the open-circuit voltage, $V_{oc}$, and the fill factor, $FF$. Together, these parameters define how efficiently the solar cell converts/collects the available light spectrum, $\eta$, as defined by:

$$\eta = \frac{J_{sc} \times V_{oc} \times FF}{P_{in}}$$  \hspace{1cm} (3.2)

where $P_{in}$ is the incident photon energy per area, 1.353 W/cm$^2$ for the AM0 spectrum, and $FF$ is defined by:

$$FF = \frac{I_p \times V_p}{I_{sc} \times V_{oc}} = \frac{P_{max}}{I_{sc} \times V_{oc}}$$  \hspace{1cm} (3.3)

where $P_{max}$ is the maximum power point on the light I-V curve as shown in figure 3.5. $I_{sc}$ is equal to the light generated current in the absence of series resistance effects, and is defined generally by:

$$J_{sc} = \int_{\nu_{min}}^{\infty} (J_p + J_n + J_{dp}) d\nu \hspace{1cm} \text{(amps)}$$  \hspace{1cm} (3.4)

where $J_p$, $J_n$, and $J_{dp}$ are the emitter, base, and depletion region current densities due to the diffusion of photoinjected minority carriers respectively and $\nu_{min}$ is the absorption edge of
Figure 3.6: Projected maximum short circuit current densities versus bandgap energy for AM0 and AM1.5 radiation.\[^{[3]}\]

the semiconductor. Equation 3.4 indicates that \( I_{sc} \) is the sum of the current "collected" from absorbed carriers in all the regions as a function of wavelength. Figure 3.6 shows a calculation for the maximum \( J_{sc} \) value achievable for a given bandgap for a single-junction cell design for both the AM0 and AM1.5 photon spectra. Note the increase in \( J_{sc}^{\text{max}} \) with decreasing bandgap energy since more photons will have enough energy to generate electron-hole pairs. This calculation is based on the assumption that all the absorbed photons in contribute to the photocurrent, i.e. ideal interfaces and infinite base thickness. However, due to the reduction in \( V_{oc} \) with decreasing bandgap, discussed later in this section, increasing \( J_{sc} \) without limit does not equate to increased conversion efficiency, equation 3.2. In the following section some factor limiting the "collection" of minority carriers, and therefore \( J_{sc} \), are discussed.
For an ideal cell, $V_{\infty}$ can be defined by:

$$V_{\infty} = \frac{k_B \times T}{e} \times \ln \left( \frac{I_{sc}}{I_0} + 1 \right) = \frac{1}{e} \times \left( \frac{E_g + k_B \times T \times \ln \frac{I_{sc}}{I_{so}}}{T^2} \right) \text{ (volts)} \quad (3.5)$$

where,

$$I_0 = I_{so} \times \exp \left( \frac{-E_g}{k_B \times T} \right) \text{ (amps)} \quad (3.6)$$

and

$$I_{so} = eAN_cN_v \left\{ \frac{D_nF_p}{L_nN_A} + \frac{D_pF_n}{L_pN_D} \right\} = eAN_cN_v \times \left( \frac{k_B T}{e} \right)^{\frac{1}{2}} \times \left\{ \frac{\mu_n^2}{\tau_n^2 N_A} + \frac{\mu_p^2}{\tau_p^2 N_D} \right\} \text{ (amps)} \quad (3.7)$$

where,

$$F_n = \frac{S_n \times \cosh \left( \frac{W_p}{L_n} \right) + \left( \frac{D_n}{L_n} \right) \times \sinh \left( \frac{W_p}{L_n} \right)}{S_n \times \sinh \left( \frac{W_p}{L_n} \right) + \left( \frac{D_n}{L_n} \right) \times \cosh \left( \frac{W_p}{L_n} \right)} \quad (3.8a)$$

and

$$F_p = \frac{S_p \times \cosh \left( \frac{W_n}{L_p} \right) + \left( \frac{D_p}{L_p} \right) \times \sinh \left( \frac{W_n}{L_p} \right)}{S_p \times \sinh \left( \frac{W_n}{L_p} \right) + \left( \frac{D_p}{L_p} \right) \times \cosh \left( \frac{W_n}{L_p} \right)} \quad (3.8b)$$
As expected, $V_{oc}$ is dependent on the bandgap energy. However, $V_{oc}$ is also weakly dependent on $I_{sc}$ and the saturation current, $I_0$. As shown in equations 3.6 - 3.8, through the saturation current dependence, $V_{oc}$ is also affected by doping, minority carrier diffusion length, mobility, interface recombination velocities, etc., making it more difficult to determine the limitations on $V_{oc}$ than $J_{sc}$. However, from equation 3.5 it is clear that $I_0$ (or $I_{so}$) must be minimized in order to maximize $V_{oc}$. When considering the GaAs/Si system, increased recombination in the depletion region due to threading dislocation incorporation is considered to dominate $I_0$, imposing a limit on the maximum attainable $V_{oc}$. This limitation/"ceiling" to GaAs/Si solar cell efficiency is discussed in section 3.4.

In addition to TDD, $I_q$ is also has a strong dependence on the interface recombination velocity, equation 3.8. The interface recombination velocity is the rate at which minority carriers drift to the interface and are "trapped" and recombine due to the presence of interface states in the bandgap. However, while $V_{oc}$ is affected by increased interface recombination velocity through increased $I_0$ as defined by equations 3.6-3.8, the impact on $I_{sc}$ is much clearer to explain. Since minority carriers generated close to the interface will be "drawn" into the interface for recombination due to the electric field created from the interface band-bending, those carriers are unable to diffuse to the p-n junction and be collected to contribute to the photocurrent, $I_{sc}$.

From equation 3.2, determining the maximum efficiency as previously defined in figure 3.4 can also be achieved. From this perspective, it is clear to see that as $E_g$ is
increased, $V_{oc}$ increases due to an increase in the built-in voltage ($V_{bi}$) while $J_{sc}$ decreases due to lost photon absorption. Conversely, as $E_g$ decreases, $J_{sc}$ increases due to increased photon absorption while $V_{oc}$ decreases due to a smaller $V_{bi}$. Since these terms are multiplied as shown in equation 3.2 to determine $\eta$, it follows that there is a peak in the efficiency curve where an optimal $E_g$ provides the greatest efficiency, figure 3.4. However, while these calculations provide the theoretical maximum efficiency assuming that all available photons are absorbed and collected, practical device efficiencies are limited by losses in both absorption and collection.

### 3.3.2 Absorption

First considering absorption, equation 3.9 defines the photon flux ($\Gamma$) remaining at a depth $x$ from the point of incidence on the cell surface, where $\Gamma_0(\lambda)$ is the incident photon flux at a given wavelength and $\alpha(\lambda,x)$ is the absorption coefficient for a material at the wavelength $\lambda$. For a given material, $\alpha(\lambda,x)$ increases with increasing photon energy when $h\nu>E_g$. Therefore, equation 3.9 indicates that higher energy (lower wavelength) photons will be collected close to the surface while photons with energy closer to the bandgap will be collected gradually throughout the structure.

$$\Gamma(\lambda, x) = \Gamma_0(\lambda) \cdot \exp(-\alpha(\lambda,x) \cdot x) \text{ (mW cm}^{-2}\text{)} \quad (3.9)$$

These results are schematically summarized in figure 3.7. Comparing these results with the spectral content of the AM0 spectrum, figure 3.3, two points should be noted when considering a single-junction cell design. First, since the AM0 spectrum contains a large
number of high energy photons ("blue-rich") which will be absorbed close to the cell surface, the design of a high efficiency cell should guarantee the collection of minority carriers generated by these photons. Second, since photon energies close to $E_g$ (~870nm for GaAs) have a small absorption coefficient, cell designs require a large "active" region thickness (emitter + base) in order to absorb all of the low energy "red" photons.

### 3.3.3 Solar cell design criteria

While the goal of this dissertation is not concentrated on the optimization of solar cell design, it is instructive to outline the impact of the structural design on the cell efficiency in order to understand the impact of material quality. As seen in figure 3.1, the
single-junction solar cell consists of only a few layers, limiting the design latitude that is available. The purpose of the window layer is to provide a larger bandgap material which will "passivate" the GaAs surface, reducing the interface recombination velocity, \( S_n \). \( S_n \) is the rate at which carriers recombine at the window/emitter interface for the p/n design. Unfortunately, GaAs does not currently possess an oxide, which successfully passivates surface states like SiO\(_2\) does for Si. Because of this, any GaAs/oxide interface possesses a high \( S_n \), in essence "drawing" the photo-injected minority carrier toward the interface where they are trapped and cannot be collected across the p-n junction in order to contribute to the photocurrent. The purpose of the BSF layer below the GaAs base is to "reflect" minority carriers back toward the p-n junction in order to give them a better chance of being collected. When holes are generated in the base, they can diffuse either toward or away from the p-n junction. The "step" in the valence band (p/n cell design) creates an electric field which "reflects" the carriers moving away from the junction so that they might be collected as shown in figure 3.2.

Ignoring the thicknesses of the window, contact, and BSF layers, the only parameters which can be controlled in order to optimize efficiency are the layer thicknesses and dopings of the emitter and base. In order to maximize \( V_{oc} \), it is necessary to maximize the doping in both the emitter and the base regions. However, by increasing the doping values, the layer mobility (\( \mu \)) is reduced as well as the minority carrier diffusion length (L\(_d\)), which makes it impossible to collect any carriers absorbed more than a distance L\(_d\) from the p-n junction. Unfortunately, as discussed previously, in order to absorb the maximum photon spectrum the "total" absorption thickness must be as large.
as possible, requiring the largest possible $L_D$. Therefore, design tradeoffs must be made in order to provide the optimum cell efficiency. While it is beyond the scope of this dissertation to derive the optimum cell design, fortunately software programs exist (such as PC-1D) which provide efficiency modeling for a desired cell structure when provided material parameters such as doping, diffusion length, and interface recombination velocity. Since the GaAs single-junction solar cell has seen considerable research, "standard" p/n cell designs have been developed and will be used as a starting point for this research, figure 3.1. For typical single-junction GaAs designs, in order to guarantee collection of the "blue" spectrum, the emitter thickness is maintained between 2000 and 5000 Å with a heavy doping in order to maintain a high $V_{oc}$. The base doping is then reduced in order to allow a longer diffusion length and therefore a thicker absorption region, 2.0-3.0 μm, in order to maximize $J_{sc}$. It must be noted that this design assumes low interface recombination velocities at both the window-emitter and base-BSF interfaces and GaAs diffusion lengths that are limited by doping (Shockley-Read-Hall or Band-to-Band) and not material quality. In order to truly optimize the cell design, it is necessary to know the device structure as well as the material quality which is controlling both $L_D$ and $S_n$. This issue will receive attention later with regard to the GaAs/Ge/GeSi/Si system.

3.3.4 External quantum efficiency

In addition to the light I-V characterization for solar cell quality, a second characterization technique which will be used extensively in this work is known as the
Figure 3.8: Example of external quantum efficiency measurement of a single junction AlGaAs/GaAs solar cell. Measurements were taken at NASA Glenn Research Center.

spectral response, or external quantum efficiency, EQE. The spectral response, SR, is defined by:

\[
SR(h\nu) = \frac{J_n + J_p + J_{dp}}{e \times \Gamma_0(h\nu)}
\]  

(3.10)

and is the short circuit current density, i.e. photogenerated current, generated by a monochromatic input photon density. The EQE is defined as the ratio of electron-hole-pairs collected and the number of incident photons. SR and EQE differ by only a scaling factor, and are commonly used interchangeably. Due to the definition of EQE, the maximum value at any wavelength is 1.0. In practice, EQE is a short circuit measurement where the current generated by a well defined flux of monochromatic photons is measured. When scaled to the photon flux of the AM0 spectrum, the EQE essentially provides a wavelength dependent breakdown of \( J_{sc} \), which is what makes the EQE
technique very instructive. Since, as described in section 3.3.2, different λ are collected at different depths due to the variations in absorption coefficient, EQE provides a “depth” characterization of the solar structure, providing a depth resolution for both material and interface quality. Figure 3.8 shows an example of an EQE measurement for a fully processed and anti-reflection coated solar cell of the structure shown in figure 3.1. The ~350nm and 900nm collection cutoffs are determined by the window bandgap (Al₀.₈Ga₀.₂As) and the emitter/base bandgap (GaAs) respectively. Note that any absorption in the Al₀.₈Ga₀.₂As window, short wavelength, is not collected across the GaAs p-n junction due to the low Lₙ of the Al₀.₈Ga₀.₂As layer. Although the bandgap of Al₀.₈Ga₀.₂As is only ~2.48eV (~500nm), due to the indirect bandgap there is considerable absorption in the GaAs layer out to nearly 350 nm (~3.5 eV). In addition to the absorption edges, much additional information can be implied from the shape of the EQE curve. For example, a loss in the high energy collection (blue) must be due to carrier collection loss near the front surface, since blue photons are only absorbed near the surface. The reduction could imply a poor interface recombination velocity which is generating recombination near the surface, an emitter thickness which is greater than the diffusion length of the minority carriers, or even an external problem with the anti-reflection coating which is causing reflection of the high energy spectrum. However, considering the EQE response for the “red” spectrum (near the GaAs band edge), a loss of collection is not as clearly defined since the lower energy is absorbed throughout the cell structure. The emitter, emitter/window interface, base (doping, thickness), or base/BSR interface could all contribute to a reduction in the structures ability to collect the “red”
photons. Therefore, while considerable information can be obtained from a single EQE curve, it is more instructive to be able to compare various EQE curves with similar structures. In later chapters, this approach is used extensively in comparisons between single-junction cells on GaAs, Ge, and GeSi substrates. While both fabrication and design can impact EQE response, the ability to compare EQE response enables one to “ignore” the impact of both design and fabrication in order to concentrate on deviations in material quality. In this case, the ability to characterize reductions in the GaAs/GeSi material and interface quality is of primary interest, as the impact of TDD is well-known to reduce solar cell efficiency, as discussed in the following section.

3.4 Impact of TDD on GaAs/Si solar cells

As discussed in earlier sections, the material mismatches between GaAs and Ge or Si present many growth complications leading to reductions in material quality. In particular for GaAs/Si, the incorporation of TD’s has provided a large barrier for achieving high quality GaAs/Si devices, particularly for large area solar cells, even when TDD reduction techniques are employed. While other issues such as thermal mismatch must also be considered for achieving optimum device performance and reliability, the impact of TDD on material quality, diffusion length in particular, is currently the mechanism limiting improvements in device quality for GaAs/Si growth. Therefore, it is instructive to track the previously reported impact of TDD on both material and device parameters in order to determine if the TDD can be reduced to a level useful for GaAs/Si device integration.
3.4.1 Minority carrier lifetime

Since the solar cell is a minority carrier device in which minority carriers from electron-hole pairs generated by incident photons must diffuse to/across the p-n junction in order to be “collected” or “counted”, high minority carrier diffusion lengths are required to enable maximum collection and therefore high efficiency as discussed in the previous section. However, the incorporation of threading dislocations (TD’s) increases the density of recombination generation centers and significantly reduces the minority carrier diffusion length, \( L_p \), thereby reducing the solar cell efficiency parameters, \( J_{sc} \), \( V_{oc} \), and FF, via equations 3.2-3.8, which all contain a diffusion length dependence through mobility or minority carrier lifetime.

Independently considering the contribution of TD’s, Yamaguchi et. al. developed a theoretical model to predict the effects of TDD on minority carrier properties.\(^{[4,5]} \) The minority carrier diffusion length is given by:

\[
\frac{1}{L_p^2} = \frac{1}{L_0^2} + \frac{1}{L_D^2} + \frac{1}{L_I^2}
\]  
(3.11)

where \( L_D \), \( L_I \), and \( L_0 \) are the diffusion lengths related to minority carrier recombination with a majority carrier at a dislocation, an impurity, and at other unknown defects, respectively. By solving the one dimensional continuity equation, the dislocation limited minority carrier diffusion length can be expressed as:

\[
\frac{1}{L_D^2} = \frac{n^3 \times \rho_I}{4}
\]  
(3.12)
Figure 3.9: Theoretical dependence of minority carrier lifetime on threading dislocation density. Experimental values represent the best GaAs/Si material quality achieved.^[4]

where \( \rho_T \) is the threading dislocation density. However, minority carrier lifetime, \( \tau_p \), rather than \( L_p \) has become the "standard" measure for expressing GaAs/Si material quality and will be the measure used throughout this discussion. Using equation 3.13, the minority carrier lifetime, \( \tau_p \), can be expressed as shown in equation 3.14, where \( D \) (or \( D_p \)) is the minority carrier diffusion coefficient and \( \tau_{po} \) is the minority carrier lifetime in the absence of dislocations (includes the impact of impurities as well as other defects).

\[
L = \sqrt{D \times \tau} \quad (3.13)
\]

\[
\frac{1}{\tau_p} = \frac{1}{\tau_{po}} + \frac{\pi^3 \times D_p \times \rho_T}{4} \quad (3.14)
\]

Figure 3.9 plots minority carrier lifetime as a function of TDD (\( \rho_T \) or \( N_d \)). Here, \( \tau_{po} \) is taken to be the GaAs homoepitaxial minority carrier lifetime, GaAs/GaAs, which is free.
of the TDD effects introduced during mismatched heteroepitaxy. (Note that $\tau_{\text{po}}$ is dependent on the semiconductor doping concentration. For this example, $\tau_{\text{po}} \sim 20$ ns.)

As shown in figure 3.9, theory predicts a strong dependence of $\tau_p$ on TDD. However, since the solar cell parameters ($\text{FF}$, $V_{\text{oc}}$, $J_{\text{sc}}$, and $\eta$) are also dependent on $L_p$, they can be expressed with a TDD dependence, providing a measure of device impact on material quality.\textsuperscript{[6]} Figure 3.10 shows the theoretical dependence found for $\eta$, $V_{\text{oc}}$, and $J_{\text{sc}}$ on TDD considering a reduction in the minority carrier diffusion length, as shown in equation 3.11, for a single junction cell structure. Similarly, figure 3.11 shows an empirical TDD dependence for $J_{\text{sc}}$, $V_{\text{oc}}$, and $\text{FF}$ found for single junction GaAs cells on GaAsP buffers, which were engineered with a range of TDD’s.\textsuperscript{[7]} In both cases, the strong dependence on TDD, especially for TDD $> 1 \times 10^6$ cm$^2$, indicates that high

![Figure 3.10: Theoretical dependence of various AM0 solar cell parameters ($V_{\text{oc}}$, $J_{\text{sc}}$, and efficiency) on threading dislocation density.\textsuperscript{[6]}](image)

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Figure 3.11: Empirical dependence of $V_{oc}$, $J_{sc}$, and fill factor on dislocation density. The "empty circle" data points represent samples where the TDD was "engineered" using an intermediate lattice-mismatched GaAsP layer. Data indicates a similar dependence as theoretically predicted by Yamaguchi et. al. (figure 3.10) \[^7\]

Efficiency devices comparable to homoepitaxial GaAs/GaAs (TDD < $10^3$ cm\(^{-2}\)) should be achievable, but only if TDD's can be reduced below $\sim5\times10^5$ cm\(^{-2}\). It should be noted that, in the TDD range predicted for good device quality, the separation between TD's becomes larger than the diffusion length and therefore should no longer significantly impacts the minority carrier diffusion length via recombination at the dislocation core.

Figure 3.12 helps convey this point with a plot of the dislocation limited minority carrier diffusion length, equation 3.13, and approximate dislocation spacing following:
Figure 3.12: Minority carrier diffusion length, \( L_D \), and threading dislocation density spacing versus threading dislocation density. As TDD increases, the minority carrier diffusion length is defined by the thread spacing.

\[
\text{Dislocation - Spacing} = \frac{2}{\pi \times \text{TDD}}
\]

As expected, these results are similar to those found for \( \tau_p \), where TDD’s < \( \sim 5 \times 10^5 \text{ cm}^{-2} \) should enable minority carrier material quality comparable to homoepitaxial GaAs/GaAs, figure 3.9. Therefore, the standard material parameter commonly used to characterize GaAs/Si growth, \( \tau_p \), provides a material parameter which can be extrapolated into attainable device quality.

Additionally, it should be noted that, while the TDD dependence of \( J_{sc} \) (figure 3.10 and figure 3.11) can be minimized (to an extent) through design considerations (base and emitter layer thickness)\(^[8]\) and has resulted in \( J_{sc} \) for GaAs/Si comparable to GaAs/GaAs homoepitaxy for TDD’s as high as \( \sim 1 \times 10^7 \text{ cm}^{-2} \),\(^[7,9]\) the decrease in \( V_{oc} \) for TDD > \( 1 \times 10^6 \text{ cm}^{-2} \) is not as easily accommodated through design parameters since the
increased saturation current, which reduces $V_{oc}$ as it increases (equation 3.5), comes from increased recombination in the depletion region and cannot be designed "around". This has limited typical $V_{oc}$ values for GaAs/Si below $\sim 900mV$, independent of $J_{sc}$. (Highest $V_{oc}$ reported prior to this dissertation research = $940mV$)\[^{4,9}\] In fact, as shown in figure 3.10, while current $J_{sc}$ values exceed those predicted by theoretical calculations, data collected for $V_{oc}$ is well below that predicted, implying additional factors may also be limiting $V_{oc}$ in addition to the increased depletion region recombination which is dominating the saturation current.\[^{10}\] (i.e. epi-layer cracking, heterogeneous defects, dislocation pile-ups, etc.) Therefore, while results indicating $J_{sc}$ values comparable to homoepitaxial GaAs/GaAs for GaAs/Si are promising and necessary, a true test of GaAs/Si device quality is whether the current "ceiling" for $V_{oc}$ of $\sim 900 mV$, which has existed for more than a decade, can be overcome.

### 3.4.2 Current status of GaAs/Si cell technology

While decades of research have developed methodologies aimed at reducing the TDD incorporated during GaAs-on-Si epitaxy, none has been able to successfully reduce TDD below $\sim 5-8 \times 10^{6} \text{cm}^{-2}$. This has limited minority carrier lifetime values to less than 3 ns independent of growth technique even when including post-growth hydrogen passivation techniques.\[^{11,12}\] As shown in the previous section, these values are not low enough to enable high efficiency devices. However, there have been a few isolated reports of GaAs/Si single junction solar cell efficiencies as high as 18.3\% (AM0) with $J_{sc} = 33.2mA$, $V_{oc} = 940mV$, FF = 79.1\%, and $\eta = 18.3\%$.\[^{4}\] While this efficiency is lower
than GaAs single-junction homoepitaxial solar cells ~23% AM0 due to the increased TDD, the ability to obtain such efficiencies demonstrates the promise of the GaAs/Si system. However, these promising efficiency results were reported over a decade ago and have never been duplicated (or exceeded), indicating the inability to control TDD’s and obtain reproducible material quality via such a growth technique (thermal cycle annealing (TCA) of “direct” GaAs/Si heteroepitaxy). In fact, while the growth of GaAs/Si has received much research attention over the past two decades, no growth technique has been able to achieve material quality which is considered to be applicable for high efficiency solar cells, leading many to believe that a “workable” solution for GaAs/Si epitaxy will never be achieved. In addition to the incorporation of TD’s, the thermal mismatch of the GaAs/Si system results in epilayer cracking and wafer bowing which are both detrimental to large area device processing and device performance. As can be seen from the past two decades of activity in the field, almost all efforts to achieve GaAs based solar cells on Si have involved a form of strain management and dislocation engineering within the III-V layers themselves. It is interesting to note that the “optimal” conditions for each approach have tended to result in similar dislocation densities and carrier lifetimes for the GaAs heteroepitaxial layers. This observation implies that limitations may exist within the III-V system in mitigating this large lattice mismatch, which is only exacerbated by the large area requirements for solar cells. Therefore, due to the inability of the current research directions to overcome the material limitations inherent in the GaAs/Si system, it is apparent that alternative approaches must be considered if the material quality and device performance required for such an application
is ever going to be achieved. This has motivated an approach in which the surface lattice constant of the Si substrate itself is engineered prior to III-V growth, rather than dealing with the mismatch only within the III-V regions. In this way, the lattice mismatch can be addressed in a material system and under growth conditions that are independent from the III-V device layers. Hence, a wider range of growth conditions (temperature, growth rate, etc.) may be accessible to achieve optimal lattice relaxation than can be provided by the III-V layers. The Ge\textsubscript{x}Si\textsubscript{1-x} alloy system is well-suited for this application since by increasing the Ge content (x) during growth of a Ge\textsubscript{x}Si\textsubscript{1-x} epitaxial layer on Si, the lattice constant can be increased from that of Si to Ge, providing a close lattice match for subsequent GaAs-based device growth.

In this research, the application of a GeSi graded buffer (Ge/GeSi/Si) as an alternative GaAs/Si integration solution is investigated, first considering the achievable GaAs/GeSi material quality and then concentrating on the application to single junction GaAs solar cells.

3.5 References


CHAPTER 4

GROWTH, STRUCTURAL, AND ELECTRICAL PROPERTIES OF GaAs/Ge/GeSi/Si

In order to determine the application of the GeSi graded buffer to GaAs/Si integration, the GaAs/Ge/GeSi/Si growth must be characterized similar to the GaAs/Ge characterization which was performed prior to this research by R.M. Sieg.\textsuperscript{[1,2]} As previously discussed, the first test for GaAs growth on GeSi is to follow the growth methodology developed for GaAs/Ge growth by R.M. Sieg, which successfully eliminated APB nucleation, TD nucleation, and interface interdiffusion for GaAs grown on closely lattice matched but chemically mismatched substrates. Additionally, an ancillary intent of this research is to optimize the prior GaAs/Ge interface nucleation with respect to electrical as well as structural properties. Specifically, this work will investigate the “robustness” of the GaAs/Ge interface nucleation with respect to both structural and minority carrier properties. While a single growth recipe was developed for GaAs/Ge nucleation,\textsuperscript{[1,2]} the nucleation procedure was never optimized with respect to layer thicknesses, surface preparation, or cycle times. For growth on the Ge/GeSi/Si substrate, surface preparation in particular is an important issue since the substrates cannot be treated as “epi-ready” (loaded directly into the UHV system without surface cleaning) as was adopted for the Ge
wafers. Additionally, due to the thermal expansion mismatch, the GaAs buffer thickness applied for GaAs/GeSi growth should be minimized. However, the impact of the "virtual Ge" surface cleanliness must be investigated in order to determine the impact on material quality close to the GaAs/Ge/GeSi/Si interface. All these issues will be addressed in this chapter after a complete introduction of the surface preparation and growth methodology which were introduced in section 1.4.

4.1 MBE of GaAs/Ge and GaAs/Ge/GeSi/Si

4.1.1 Sample preparation

While many variations have been investigated and will be discussed in this chapter, the "base-line" growth recipe followed in this research was described in section 1.4 and is detailed in table 4.1. While not specifically addressed in section 1.4, the ramp rates during the temperature transitions are significant, specifically the transitions without ramping which are intended to "freeze" in surface reconstructions, and are listed in the table. References 1-2 have a complete discussion of the nucleation procedure used here. For the remainder of this dissertation, the growth nucleation sequence detailed in table 4.1 will be referred to as the "optimum" growth nucleation since it was previously demonstrated to simultaneously eliminate both APB formation and atomic diffusion at the GaAs/Ge interface for work on Ge wafers. For other nucleation conditions, only deviations from the "optimum" technique will be noted. For example, a sample referred to as "without MEE" (commonly used in this work) includes all the procedures listed in Table 4.1 with the exception of the MEE nucleation step which has been omitted.
<table>
<thead>
<tr>
<th>Procedure</th>
<th>Thickness /Time</th>
<th>Temp. (°C)</th>
<th>Temp. Ramp</th>
<th>Purpose/Effect</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal anneal</td>
<td>20 min.</td>
<td>640°C</td>
<td>25°C/min</td>
<td>Oxide removal/Thermal cleaning</td>
</tr>
<tr>
<td>Ge epitaxy</td>
<td>300-1000Å</td>
<td>350°C</td>
<td>No ramp</td>
<td>&quot;Bury&quot; carbon surface contamination</td>
</tr>
<tr>
<td>Epitaxial Ge anneal</td>
<td>20 min.</td>
<td>640°C</td>
<td>25°C/min</td>
<td>Generate double-stepped Ge surface</td>
</tr>
<tr>
<td>MEE GaAs (As first)</td>
<td>10 cycles (~56 Å)</td>
<td>350°C</td>
<td>No ramp</td>
<td>Minimize APB formation as well as atomic diffusion (Well ordered surface init)</td>
</tr>
<tr>
<td>LT-GaAs</td>
<td>1000 Å</td>
<td>500°C</td>
<td>25°C/min</td>
<td>Minimize atomic diffusion</td>
</tr>
<tr>
<td>Conventional GaAs</td>
<td>-</td>
<td>600-620°C</td>
<td>25°C/min</td>
<td>Device growth</td>
</tr>
</tbody>
</table>

Table 4.1: Standard MBE procedure used throughout this work for GaAs/Ge and GaAs/GeSi growth nucleation. Temperature ramps indicate the rate of change in thermocouple temperature used for temperature adjusts to the substrate temperature. Throughout this dissertation, this nucleation methodology is referenced as the "optimum" nucleation procedure.

While the "optimum" growth technique was applied uniformly to both Ge and Ge/GeSi/Si substrates, one difference which must be noted is the variation in surface preparation prior to loading into the UHV system growth. For the Ge wafers, an initial HF:H₂O₂ cleaning procedure was adopted in order to provide a "cleaner" Ge surface for GaAs epitaxy. However, from what is believed to be preferential etching at tilt boundaries in the Ge substrate, all substrates subjected to an HF:H₂O₂ cleaning etch displayed large "pits" after GaAs epitaxy. Accordingly, cleaning of the Ge wafers was either eliminated, i.e. loaded into the UHV system as epi-ready, or limited to an oxide etch (30 seconds dionized water (DI) since the Ge oxide is water soluble) followed by a 20 minute ultra-violet ozone clean with flowing ultra-high purity air (UV-Ozone), which helps remove carbon from the Ge surface. For the GeSi substrates, a more extensive
cleaning procedure was required due to the wafer status upon delivery to OSU from Fitzgerald et. al. at MIT. In order to protect the wafer surface, the UHVCVD grown GeSi samples were first coated with SiO₂ and then photoresist prior to shipping. The purpose behind this procedure was both to protect the sample surface during shipping as well as during the wafer dicing procedure, via diamond saw, which was adopted in order to cut the 4" diameter GeSi samples into quarters so the sample size was compatible with the MBE growth system, which can accommodate a maximum 3" diameter sample. For cleaning, the photoresist was initially removed in two sequential acetone rinses followed by a (4:1) H₂SO₄:H₂O₂ (piranha) etch at −67°C to clean the back side of the Si wafer. (Note that an ice bath is required in order to keep piranha etch temperature to 67°C.) The SiO₂ was then removed in a (4:1) DI:HF solution, producing a hydrophobic Ge surface, and followed by a 20 minute UV-Ozone clean prior to loading into the UHV system. For the lifetime samples, the Ge and GeSi samples were cleaved into ~2cm x 1cm samples and multiple samples were indium bonded to a single 3" molybdenum block, a common mounting technique used in MBE for non-standard wafer sizes. One sample was placed at the center of the block for the temperature monitoring via the pyrometer as shown schematically in figure 4.1. For the solar cell growths performed on 2" wafers (Ge) or ¼-4" wafers (GeSi), an indium-free mounting technique was used, including a 2" spring plate and 3" sapphire backing plate as shown in figure 4.2. While this method is standard for a 2" wafer, the GeSi samples were “pinned” behind the 2" spring plate in order to avoid indium bonding, a concern when processing a back contact to the Si wafer. While
In-bonded samples to 3" Mo plate (5-6 samples)

Figure 4.1: In-bonding configuration used for mounting multiple Ge and GeSi samples for growth of double-heterojunction TRPL samples.

Figure 4.2: EPI spring plate mounting technique used in In-free mounting of ¼-4" GeSi samples. 2" spring plate “pins” the ¼-4" sample to minimize the chances of wafer slipping during growth.
this mounting technique is not optimum and results in lost growth area, if care is taken the GeSi can be secured in the indium-free holder and provide a “slip-free” mounting scheme.

Figure 4.3 shows a Nomarski optical microscope image for a GeSi “starting” growth surface. Note the cross-hatch surface morphology which results from the grading procedure due to the presence of misfit dislocations. Due to the thick grade, ~15 µm, the cross-hatch is severe with a periodicity of ~5000Å and an rms roughness of ~24.5nm. Additionally, due to both the current processing environment used (i.e. a non-cleanroom laboratory) as well as the “non-optimized” growth process, a large variation in material quality is evident. From the growth process (believed to be due to system cleanliness and not the grade technique itself) as well as the chemical mechanical polish step, the substrates contains a number of surface defects, as high as $5 \times 10^3$ cm$^{-2}$, as visible in Figure 4.4(a), in addition to other background defects. As the GeSi graded buffer growth
process is optimized the density of residual surface defects is expected to decline and has in fact been reduced to ~50 cm\(^{-2}\) in some instances. In addition to TDD, the crosshatch morphology and surface defects are both a concern for GaAs material quality. The impact of all these parameters are considered in the following chapters.

4.1.2 APB and TD nucleation in GaAs/GeSi

Using the GaAs/Ge nucleation procedure developed on Ge wafers and defined in table 4.1, figure 4.5 shows a cross-sectional TEM image of the GaAs layer grown on a Ge/GeSi/Si substrate. From the TEM image, the “optimum” nucleation recipe successfully suppresses APB formation at the GaAs/GeSi interface similar to that realized on the Ge wafers. This result indicates that the 100% Ge cap of the GeSi graded buffer is
indeed behaving as an ideal Ge surface for the formation of an APB-free, low-mismatch GaAs/Ge interface. In addition to the elimination of APB’s, the TEM image shows no nucleation of threading dislocations, again similar to the ideal GaAs/Ge interface nucleation on Ge wafers from which the nucleation growth methodology was developed. However, since the TEM resolution (detection limit) only verifies a TDD less than \( \sim 1 \times 10^7 \text{ cm}^{-2} \), etch pit density (EPD) measurements were performed on GaAs epilayers in a KOH solution (section 2.9) in order to verify that the TDD is limited to that present in the Ge cap layer of the GeSi graded buffer. Indeed, multiple EPD measurements indicate a TDD of \( 7 \times 10^5 - 2 \times 10^6 \text{ cm}^{-2} \) in the GaAs layer, similar to that found in the Ge cap layer.\(^{[4]}\) These results verifying the elimination of both APB formation and TD nucleation indicate that the GeSi graded buffer is behaving as an ideal, low-mismatch Ge interface for GaAs nucleation and that the nucleation methodology is not affected by either the surface crosshatch morphology nor the residual threading dislocation density.
4.1.3 GaAs/GeSi interface diffusion

One aspect of the GaAs/Ge MBE nucleation methodology developed by R.M. Sieg et. al. that is unique from other GaAs/Ge nucleation reports is the ability to simultaneously eliminate interface cross-diffusion as well as APB formation. Cross-diffusion is the diffusion of either Ga or As into the Ge substrate or Ge into the GaAs epilayer, all which act as dopant species and induces the well-known problem of autodoping at the heterointerface. Since high growth temperatures can cause diffusion of As, Ga and Ge at the GaAs/Ge interface generating high background doping over many microns or even type conversion, thin, inactive GaAs buffers used for MBE nucleation may not impede autodoping of the active GaAs layers. In previous work on GaAs growth on Ge wafers by MBE, use of the “optimum” interface nucleation procedure demonstrated successful minimization of such diffusion to negligible levels compared to previous GaAs/Ge autodoping reports. Here, these experiments are repeated for GaAs grown on Ge/GeSi/Si substrates to investigate whether residual TDD’s or the presence of crosshatch morphology characteristic of graded GeSi affects cross-diffusion at the GaAs/Ge/GeSi/Si interface.

Figures 4.6(a), 4.6 (b) and 4.6 (c) show the SIMS atomic concentration profiles obtained for Ge in GaAs, Ga in Ge, and As in Ge, for a 2.5μm thick GaAs layer (n = 3x10^15 cm^-3) grown on Ge/GeSi/Si. For comparison, SIMS profiles are also shown for GaAs grown on Ge wafers under identical growth conditions. As shown, the GaAs on Si demonstrates negligible diffusion across the interface boundary. While the Ge and Ga profiles appear to be identical for either substrate (the only difference between the
Figure 4.6: Secondary ion mass spectroscopy (SIMS) analysis for GaAs growth on both Ge and Ge/GeSi/Si substrates with identical growth nucleation procedures showing (a) Ga, (b) As and (c) Ge diffusion across the GaAs/Ge interface. Improvements seen in the SIMS detection/sensitivity limit for all cases on the Ge/GeSi/Si substrate is due to improved profiling procedures. As shown, neither the increased TDD nor the increased cross-hatch morphology appear to promote increased diffusion at the GaAs/Ge interface.
substrates is the lower detection limit for the SIMS measurements made on the 
GaAs/Ge/GeSi/Si structure. As diffusion is lower for the Ge/GeSi/Si substrate than for 
the Ge wafer. The reason for this additional improvement is not known and warrants 
additional investigation. However, the ability to block cross-diffusion by proper interface 
formation using MBE growth is clearly not adversely affected by the higher defect density 
or surface morphology of the Ge/GeSi/Si substrate as compared to the Ge wafer, 
indicating that elimination of inadvertent p-n junction formation is possible on the 
Ge/GeSi/Si substrates. Hence, we conclude that both APB and TD nucleation 
suppression as well as diffusion control can simultaneously be achieved on the GeSi 
graded buffer similar to that acquired for Ge wafers, indicating that from a structural 
standpoint (including diffusion) the Ge cap of the GeSi graded buffer is behaving as an 
ideal Ge surface, a significant achievement when considering the additional TDD, surface 
crosshatch morphology, and high density of surface defects, figure 4.4.

Additionally, for reasons that will be discussed in the following sections, a 
measure of the diffusion profiles encountered when eliminating the MEE nucleation step 
is also of interest. In the GaAs/Ge case, SIMS results by R.M. Sieg showed no Ga 
diffusion and minimal As diffusion, (~5x10¹⁸ cm⁻³ peak over 1μm), when the MEE 
nucleation step was eliminated. Additionally, while Ge diffusion was maintained 
below the SIMS detection limit of ~3x10¹⁶ cm⁻³, C-V analysis showed n-type doping 
levels near 1x10¹⁶ cm⁻³ more than 1.5 μm from the GaAs/Ge interface. For the current 
p/n growth structure these diffusion profiles should result in minimal impact on device 
performance. However, both cases demonstrate the importance of the MEE nucleation
Figure 4.7: C-V profiles for “low-doped” GaAs epilayers used to determine the extent of Ge diffusion at the GaAs/Ge interface which is below the SIMS detection limit of $\sim 3 \times 10^{16} \text{ cm}^{-3}$. Four profiles are included: 1) GaAs/Ge with MEE nucleation, 2) GaAs/Ge without MEE nucleation, 3) GaAs/GeSi with MEE nucleation, and 4) GaAs/GeSi without MEE nucleation. Note that while increased Ge diffusion is seen for the GaAs/Ge epitaxy without MEE, the GeSi substrate does not demonstrate the same trend.

procedure in providing “maximum” control over the GaAs/Ge interface. For the GaAs/GeSi system, SIMS analysis is currently underway to determine Ga, As, and Ge diffusion when the MEE nucleation step is eliminated. (Unfortunately, this data was not available at the time of this publication.) However, C-V analysis was performed in order to determine the extent of Ge diffusion into the GaAs epilayer. Figure 4.7 shows C-V data obtained for the GeSi substrate with and without the MEE nucleation step along with previous data found for the Ge wafer. The nominal GaAs doping in all cases was $3 \times 10^{15} \text{ cm}^{-3}$. The C-V analysis indicates negligible Ge diffusion in both GaAs/GeSi samples, even when eliminating the MEE nucleation step which resulted in increased diffusion for
the GaAs/Ge sample. While the reason for this improved diffusion control is unknown, without the benefit of the SIMS diffusion profiles these results suggest that the Ga and As diffusion profiles should be no worse for the GaAs/GeSi without MEE than those obtained for the GaAs/Ge sample (i.e. minimal As diffusion and no Ga diffusion), and may even be improved. While the actual SIMS results are required in order verify these assumptions, these results are consistent with the previous SIMS data indicating that the GeSi surface is indeed behaving as on "ideal" Ge interface for GaAs nucleation.

4.1.4 Thermal mismatch in GaAs/GeSi system

Although thermal mismatch is not an issue for the GaAs/Ge system due to the similar thermal expansion coefficients of GaAs and Ge (α ≈ 5.5 × 10⁻⁶ K⁻¹), the large thermal expansion coefficient mismatch between GaAs and Si, ~63%, is an important issue for GaAs/Si heteroepitaxy. Unfortunately, reports of both wafer bow and GaAs epilayer cracking due to thermal expansion mismatch are more qualitative than quantitative, making it difficult to compare the current GaAs/GeSi growths with past GaAs/Si research.¹⁹,¹⁰,¹¹ Due to the cleaving of the GeSi samples to the growth size, cracks are also routinely generated during the cleaving process and are impossible to differentiate from cracks generated solely from heating and cooling during growth. Additionally, crack generation during fabrication due to wafer bow is not uncommon since the lithography equipment is designed for a planar surface and can introduce stresses when substrates are vacuumed to planar surfaces.
The 15 µm graded buffer with multiple interfaces also makes the calculation of the thermal expansion for the entire GaAs/GeSi system a difficult problem when compared to a single GaAs layer on Si where only two different thermal expansion coefficients are involved. While K. Nakajima et. al. have developed a theoretical model for calculating the total strain due to thermal expansion for a graded system,\cite{12,13} it should be noted that Fitzgerald et. al. have successfully “balanced” the tensile strain from thermal expansion mismatch with compressive strain due to lattice mismatch, resulting in a cubic Ge surface at room temperature.\cite{14} Unfortunately, multiple GeSi graded layers grown under similar conditions have also resulted in Ge capping layers under both compressive and tensile strain, as determined via triple axis x-ray diffraction. Due to these inconsistent Ge surfaces combined with unrelated crack generation, there was no attempt in this work to correlate the GaAs growth to crack generation, for example the dependence of the GaAs epilayer thickness on the crack density/spacing. However, crack densities following device fabrication were noted along with the impact of crack incorporation on device performance and will be discussed in chapter 5. While not considered in greater detail in this dissertation, the inability to control both wafer bow and crack generation (in addition to TDD) is a major reason why GaAs/Si integration has been unsuccessful for decades and warrants future investigation for the GaAs/GeSi system. The ability to contain TD nucleation solves one of the key GaAs/Si integration issues, however, the inability to minimize the impact of thermal mismatch would still make GaAs/GeSi integration impractical at a wafer scale, making it an area for additional
research effort. However, as will be discussed in Chapter 6, this issue does not appear to hinder substantial advances in device performance due to the even larger impact of TDD.

4.1.5 Additional growth of GaAs/Ge and GaAs/Ge/GeSi/Si

Although the recipe presented in Table 4.1 has been demonstrated to simultaneously eliminate TD nucleation, APB nucleation, and atomic diffusion for GaAs growth on both Ge and GeSi substrates, numerous "non-optimum" growth procedures were also implemented during this work. In particular, both the MEE and Ge epilayer steps were consistently modified for various reasons including material quality and time constraints during growth. First, elimination of the MEE nucleation step during growth was found to be critical in achieving defect free surface morphologies. While the MEE procedure was found to be vital in eliminating APB formation and atomic diffusion, sections 4.1.2 and 4.1.3, figure 4.8 shows a large area optical image (Nomarski) of the GaAs/Ge growth surface. Although the interface is controlled on an atomic scale, the inclusion of the MEE step was found to introduce a uniform background of surface defects with a density greater than $10^8$ cm$^{-2}$. The origin of these defects is not completely understood, but our studies imply that they are likely generated due to the mechanical operation of the As valve, As shutter, and Ga shutter "spitting" contaminants toward the growth surface at the low 350°C growth temperature (possibly "uncracked" As$_4$ is the case of the As source). Since these defects were not detected for MEE initiation at 500°C, the low growth temperature likely prevents the desorption of any contaminants generated due to the mechanical shutter operation. (Note that this problem results from
Figure 4.8: Nomarski optical image showing surface defects generated during MEE nucleation and believed to be generated by the operation of the As shutter. Defect densities are as high as $5 \times 10^8$ cm$^{-2}$.

"dirty" shutters and a "dirty" As valve and may be unique to our specific MBE system.) Therefore, while the MEE nucleation itself should not result in any material defects, due to the mechanical operation of the shutters for the MBE growth technique, the inclusion of the MEE nucleation step prohibits defect-free material nucleation and was necessarily eliminated. However, section 4.1.3 indicates that the lack of MEE nucleation results in the inability to control interface diffusion. Additionally, TEM images show the inclusion of APB's for non-MEE nucleation, figure 4.9. Fortunately, while APB's are generated, they appear to annihilate within $\sim 100-200\AA$ of the GaAs/Ge interface and do not proceed into the GaAs "active" layers. Consequently, the impact of these self-annihilating, short range APB's on the GaAs electrical quality is expected to be minimal, especially compared to large APB's protruding to the GaAs surface.
Figure 4.9: Cross-sectional TEM of GaAs growth on a Ge wafer without MEE nucleation. APB's generated at the GaAs/Ge interface annihilate within ~100-200Å of the interface, prior to the AlGaAs double heterojunction barrier.

The second modification to the nucleation procedure was initially implemented to save growth time, but was later found to have significant impact on device characteristics as will be discussed in chapter 5. The purpose of the 1000 Å epitaxial Ge layer is to bury the carbon contamination of the Ge growth surface and effectively aide in reducing APB and TD nucleation. However, Auger analysis of the Ge growth surface indicated similar suppression of the carbon signal for 100 Å and 1000 Å Ge epi-layers, indicating that the 1000 Å epitaxial Ge is unnecessarily thick for burying the surface carbon contamination. Note that all samples were subjected to a UV-Ozone clean which was previously determined to aide in reducing carbon contamination of the Ge surface. TEM data shows no impact of thinning the Ge layer down to 300 Å on either TD or APB nucleation, verifying that the carbon contamination is buried for a thinner epitaxial Ge layer. (TEM analysis is currently in progress for samples containing Ge epilayers down to 50 Å but
was unavailable at the time of this publication. However, as discussed in the following chapter, device I-V data indicates no degradation as a function of buffer thickness which would indicate additional APB or TD nucleation.) For the remainder of the GaAs/Ge and GaAs/GeSi growths the epitaxial Ge was reduced to ~300 Å unless otherwise noted. In the following section the impact of both the MEE and Ge epilayer thickness variations are investigated with respect to minority carrier lifetime, an important measure of material quality, especially for solar cells. The impact of the Ge epilayer on device performance is further addressed in chapter 5.

4.2 Minority carrier lifetime in GaAs/Ge and GaAs/Ge/GeSi/Si systems

In the previous sections the ability to minimize both APB formation and atomic diffusion in the GaAs/GeSi system similar to that attained for GaAs/Ge has been demonstrated. However, along with the structural quality, a measure of the transport properties of the GaAs is also necessary in order to determine the applicability of the GaAs/GeSi integration for devices, optical devices in particular. For this work, minority carrier lifetime is used as an indication of material quality since it has become a standard measure for the GaAs/Si system, especially with regard to solar cell research. As presented in section 3.4, GaAs/Si integration has been limited by the incorporation of high threading dislocation densities, which significantly impact the minority carrier properties through recombination. However, through the use of the GeSi graded buffer GaAs layers with real threading dislocations as low as 8x10^5 cm^{-2} have been realized during MBE growth (section 4.1.2). As shown in figure 3.9, threading dislocation
densities in this range should enable minority carrier lifetimes, \( \tau \), comparable to that of homoepitaxial GaAs (\( \tau \sim 19 \) ns), a significant improvement over the best GaAs/Si minority carrier lifetime reported to date of \( \sim 3 \) ns.\cite{15,16} In this section, minority carrier lifetimes on both Ge and GeSi substrates are investigated. First, the impact of growth parameter variations on \( \tau \) were investigated for the "simpler" Ge wafer system. Finally, the impact of the GeSi graded buffer (threading dislocations, surface cross-hatch, and interface APB formation) on GaAs/Si material quality is determined.

### 4.2.1 Experimental conditions

As discussed in section 2.9, a convenient means of characterizing both the bulk minority carrier lifetime and the GaAs/AlGaAs interface recombination velocity is via time-resolved photoluminescence (TRPL) measurements of AlGaAs/GaAs/AlGaAs double heterojunction (DH) structures with varying GaAs thickness, figure 2.13. To re-iterate, the TRPL transient is given by:\cite{17}

\[
\frac{1}{\tau_{\text{TRPL}}} = \frac{1}{\tau_p} + 2S/d
\]  

(4.1)

where \( \tau_{\text{TRPL}} \) is the TRPL decay lifetime, \( \tau_p \) is the bulk minority carrier lifetime for n-type GaAs, \( S \) is the surface recombination velocity, and \( d \) is the DH GaAs layer thickness. By growing samples of several different thicknesses, \( \tau_p \) and \( S \) can be extracted using eqn (4.1), assuming sample-to-sample reproducibility for both \( \tau_p \) and \( S \).
The lifetime measurements in this study were performed in collaboration with the National Renewable Energy Laboratory (NREL), which has an elaborate TRPL system and extensive expertise in this measurement. Data were taken at room temperature (293K) using the time-correlated single-photon counting technique. In this technique, electron-hole pairs are photo-excited using a cavity-dumped dye laser synchronously pumped by a mode-locked Nd:YAG laser. The output of the dye laser was a 1 MHz train of 10 ps-wide pulses, tuned to 600 nm. The injection level of photo-excited carriers within the sample was maintained below the equilibrium carrier concentration by attenuating the average incident laser power to 50 μW and focusing to a 1 mm diameter spot. The resulting photoluminescence was collected and focused onto the slits of a scanning monochromator and detected with a micro-channel plate (MCP) detector. This system can resolve decay rates as short as 20 ps. All transients were measured by monitoring the 870 nm GaAs band-to-band transition peak.[18]

The MBE-grown Al_{0.3}Ga_{0.7}As/GaAs/Al_{0.3}Ga_{0.7}As DH structures were deposited on both Ge and on Ge/GeSi/Si wafers with GaAs thicknesses standardized at 0.5 μm, 1.0 μm, and 1.5 μm, using nucleation procedures similar to that detailed in table 4.1. Since the structures were n-type throughout, Ge outdiffusion will be negligible even without the migration enhanced epitaxy (MEE) step (see figures 4.6 and 4.7), and so the MEE step was omitted for all growth runs. The Al_{0.3}Ga_{0.7}As barrier thicknesses were 50 nm and 20 nm for the surface and buried barrier layers, respectively. The DH structures were uniformly doped at n=1.1x10^{17} cm^{-3}. Samples grown on Ge wafers typically included a 1000Å initial GaAs buffer (2000 Å when including the 1000Å buffer grown at 500°C as
discussed in table 4.1) while samples grown on Ge/GeSi/Si included GaAs buffers from 1000Å - 1µm. The initial buffer was doped at n=1×10^{18} cm^{-3}. All samples were grown at 620°C as measured by an infra-red pyrometer with As₂:group III ratio ~12:1 for the Al_{0.3}Ga_{0.7}As layers (~14:1 for the GaAs layers).

4.2.2 GaAs/Ge minority carrier lifetime

Before considering the GaAs/GeSi system where the impact of threading dislocations is unavoidable, it is instructive to first investigate the impact of the MBE nucleation on a “simpler” GaAs/Ge system without the additional threading dislocations, surface morphology, and APB formation to which the GaAs/GeSi results can be compared. For this purpose, a number of growth conditions for the GaAs/Ge system were investigated in order to determine their impact on the GaAs material quality. First, a series of 3 “epi-ready” samples were grown (d = 1.5, 1.0, and 0.5 µm) following the “optimum” growth nucleation of table 4.1 but without an MEE nucleation step. A 1.5µm sample was also grown under identical growth conditions but with a 20 minute UV-Ozone clean prior to sample loading. All samples contained a 0.1µm GaAs buffer. In addition, two DH structures (d = 1.5 and 0.5 µm) were grown with the “optimum” nucleation, a 5000Å GaAs buffer, and a 20 minute UV-Ozone clean. Figure 4.10 plots the exponential decay data for only the 1.5 µm DH structures for comparison. Figure 4.11 plots the TRPL lifetimes extracted for all the TRPL decays in order to determine both τ_p and S via equation 4.1 for the epi-ready and UV-Ozone cleaned samples respectively. Note the linear curve fit for the three epi-ready samples is in excellent
Figure 4.10: TRPL decay data for multiple 1.5 μm DH samples with various surface preparations and nucleation conditions. Table 4.2 shows extracted TRPL lifetimes from exponential curve fitting.

Figure 4.11: Plot of TRPL lifetimes (1/τ_{TRPL} versus 1/d) for samples listed in Table 4.2. (±10% error) Linear curve fits are shown when multiple samples are available. Following Equation 4.1, both minority carrier lifetime and interface recombination velocity can be determined.
Table 4.2: Compilation of minority carrier lifetime data from TRPL decay data, figure 4.10, and from figure 4.11 (via equation 4.1) for multiple GaAs/Ge double heterostructure thicknesses, \( d \). Identical growth parameters were used for all samples, only the initial surface cleaning/preparation was varied: a) epi-ready and b) UV-ozone cleaned.  

<table>
<thead>
<tr>
<th>Sample</th>
<th>Substrate Preparation</th>
<th>DH thickness (( d )) (( \mu )m)</th>
<th>GaAs buffer thickness (( \mu )m)</th>
<th>( \tau_{\text{TRPL}} ) (ns) ((T=300K))</th>
<th>S (cm/s) ((T=300K))</th>
<th>( \tau_p ) (ns) ((T=300K))</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Epi-ready</td>
<td>1.5</td>
<td>0.1</td>
<td>5.88</td>
<td>9,000</td>
<td>19.0</td>
</tr>
<tr>
<td>2</td>
<td>Epi-ready</td>
<td>1.0</td>
<td>0.1</td>
<td>4.31</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>3</td>
<td>Epi-ready</td>
<td>0.5</td>
<td>0.1</td>
<td>2.49</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>4</td>
<td>UV-Ozone</td>
<td>1.5</td>
<td>0.1</td>
<td>9.57</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>5</td>
<td>UV-Ozone</td>
<td>1.5</td>
<td>0.5</td>
<td>10.3</td>
<td>2,800</td>
<td>17.2</td>
</tr>
<tr>
<td>6</td>
<td>UV-Ozone</td>
<td>0.5</td>
<td>0.5</td>
<td>5.9</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

A number of conclusions can be drawn from these three sample sets. For the optimum growth samples with a 0.5 \( \mu \)m buffer and a UV-Ozone clean (5 and 6), \( \tau_p = 17.2 \) ns and \( S = 2.8 \times 10^3 \) cm/s, table 4.2. Within experimental error, \( \tau_p \) is comparable to values obtained for homoepitaxial GaAs in the absence of photon recycling, \(^{19,20}\) and \( S \) is consistent with AlGaAs/GaAs interfaces. These results were reproduced over various GaAs/Ge data sets and indicate excellent GaAs material quality consistent with the TEM and SIMS data reporting atomic control of the GaAs/Ge interface. Due to the 0.5mm buffer used, the “measure” GaAs layer region was 0.6 - 2.1 \( \mu \)m from the GaAs/Ge interface.
For the "epi-ready" GaAs/Ge samples without MEE nucleation (1-3), demonstrated to generate "small", annihilating APB's at the GaAs/Ge interface, $\tau_p = 19$ ns is comparable to that measured for "optimum" growth. Since these samples contained only a 1000Å GaAs buffer the "measured" GaAs material is only 0.2-1.7μm from the GaAs/Ge interface, indicating that even without MEE the GaAs/Ge nucleation successfully controlled the GaAs/Ge interface resulting in high quality GaAs growth. These results are consistent with TEM images indicating that APB's generated at the GaAs/Ge interface are annihilated prior to the "active" GaAs region, 2000Å from the interface in this case. Therefore, while elimination of the MEE nucleation step introduces some APB formation and results in minimal atomic diffusion, the minority carrier quality of the GaAs is still comparable to that of homoepitaxial GaAs. However, the interface recombination velocity, $S = 9,000$ cm/s, is three times higher than that found for the "optimum" nucleation with a 0.5 μm GaAs buffer, indicating that the 0.1 μm buffer may not be sufficient for achieving high interface quality, particularly for the rear AlGaAs/GaAs interface which is located only 2000Å from the GaAs/Ge interface which contains APB's.

Looking at sample 4, (UV-Zone, 1.5μm DH, no MEE), although $\tau_p$ and $S$ cannot be extracted from a single DH thickness, some valuable conclusions can be drawn from comparing the TRPL decay lifetime with that for the epi-ready samples since the only variation is the addition of a UV-Ozone cleaning step to reduce carbon contamination. Since the TRPL lifetime is longer for the UV-Ozone cleaned sample, it follows from equation 4.1 that either $\tau_p$ or $S$ must have been improved through the introduction of the
UV-Ozone surface clean. Since $\tau_p = 19$ ns for the non-Ozone samples is already comparable to that for homoepitaxial GaAs (as well as the optimum GaAs/Ge samples), it is reasonable to assume that the improved TRPL lifetime was a result of a reduction in $S$ rather than an increase in $\tau_p$. From equation 4.1, assuming $\tau_p = 19$ ns for TRPL = 9.57 ns and $d = 1.5\mu m$, then $S = 3.8 \times 10^3$ cm/s, considerably better than that obtained for the epi-ready Ge substrate and similar to that found for the optimum GaAs/Ge growth (within experimental error). We conclude from this data that the minimal 1000 Å GaAs buffer is sufficient to produce excellent minority carrier properties, both $\tau_p$ and $S$, even without MEE nucleation provided that proper surface cleaning is ensured. In this case, the UV-Ozone clean, which has been shown to reduce carbon contamination of the Ge surface, is necessary in reducing interface recombination velocities close to “state-of-the-art” for AlGaAs/GaAs interfaces when a minimal 1000 Å GaAs buffer is employed. In fact, additional measurements for epi-ready Ge samples showed wide variations in TRPL lifetimes indicating inconsistent sample-to-sample nucleation/interface control.

Therefore, although the elimination of the MEE nucleation process results in both APB formation as well as minimal atomic diffusion, the minority carrier properties of the GaAs appear to be unaffected even within 2000 Å (1000 Å nucleation +1000 Å GaAs buffer) of the GaAs/Ge interface. This is an important consideration since the current MBE system cannot produce defect-free surfaces when including the MEE nucleation. Additionally, the ability to minimize the GaAs buffer required for high GaAs material quality to 1000 Å is also an important conclusion. For “typical” MOCVD GaAs/Ge growth, the inability to control the GaAs/Ge interface results in the inclusion of thick, ~3-
5μm, GaAs buffers in order to allow APB annihilation prior to the "active" GaAs regions of a device. While this is not an important issue for GaAs/Ge growth, due to the thermal mismatch for the GaAs/Si system, the ability to minimize unnecessary GaAs thickness will be important in the reduction/control of crack formation and wafer bow on thick device structures, like those required for high efficiency solar cells. The impact of the GaAs buffer thickness for the GaAs/GeSi system will be considered in the following section.

In addition to the above samples where only the MEE and UV-Ozone clean were varied, additional growths were performed in order to investigate the impact of the GaAs nucleation procedure and the surface preparation/cleaning on the GaAs minority carrier properties. Table 4.3 shows a compilation of the additional GaAs/Ge DH samples.

First, GaAs co-evaporation at 350°C on unannealed epitaxial Ge, a combination demonstrated to produce large APB's, was investigated, samples 7-8. Figure 4.12 shows

<table>
<thead>
<tr>
<th>Sample</th>
<th>Substrate Preparation</th>
<th>DH thickness (d) (μm)</th>
<th>GaAs buffer thickness (μm)</th>
<th>τ&lt;sub&gt;TRPL&lt;/sub&gt; (ns) (T=300K)</th>
<th>S (cm/s) (T=300K)</th>
<th>τ&lt;sub&gt;p&lt;/sub&gt; (ns) (T=300K)</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Epi-ready</td>
<td>1.0</td>
<td>0.1</td>
<td>0.19</td>
<td>200,000</td>
<td>0.5</td>
</tr>
<tr>
<td>8</td>
<td>Epi-ready</td>
<td>0.5</td>
<td>0.1</td>
<td>0.12</td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>SiN clean</td>
<td>1.5</td>
<td>0.1</td>
<td>9.57</td>
<td>1,800</td>
<td>9.8</td>
</tr>
<tr>
<td>10</td>
<td>SiN clean</td>
<td>1.0</td>
<td>0.1</td>
<td>10.3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>SiN clean</td>
<td>0.5</td>
<td>0.1</td>
<td>5.9</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 4.3: Compilation of TRPL data for GaAs/Ge samples with a) APB incorporation (7-8) and b) an initial SiN coating prior to cleaning (9-11).
Figure 4.12: Cross-sectional TEM of GaAs growth on a Ge wafer with GaAs co-evaporation at 350°C. APB's generated at the GaAs/Ge interface penetrate through the DH structure to the growth surface.

a TEM image of the GaAs material quality typical of these growth conditions. Two DH structures were grown, d = 0.5 and 1.0 μm, resulting in TRPL lifetimes of 0.12 and 0.19 ns respectively, and τp = 0.5 ns and S = 5x10⁵ cm/s. These results indicate the detrimental impact of APB incorporation and demonstrate the importance of controlling the nucleation of the GaAs/Ge interface, relating the structural control of the GaAs/Ge interface to electronic properties of the GaAs/Ge system.[21] These results further support the above assumption that the elimination of the MEE nucleation step, resulting in APB annihilation within ~100Å of the GaAs/Ge interface, can still be used to generate high quality GaAs material.

The final TRPL sample set on Ge wafers attempts to mimic the GeSi surface preparation conditions in order to determine the possible impact on τ and S. In the previous data, table 4.2, the cleaning of the Ge surface (UV-Ozone) was found to impact the minority carrier properties, with the UV-Ozone clean of the Ge wafers improving the
interface recombination velocity but having little impact on \( \tau_p \). Since the GeSi wafers contain an additional SiO\(_2\) surface coating, it is reasonable to assume that the additional surface cleaning will also have an impact. In order to observe the possible impact of the SiO\(_2\) cleaning procedure for the GeSi surface, silicon nitride (SiN) coatings were plasma deposited on the Ge wafers prior to cleaving and cleaning. SiN instead of SiO\(_2\) coatings were used since the capabilities to plasma deposit a SiO\(_2\) coating is not available at OSU, but should equivalently simulate the additional cleaning procedures required on the GeSi substrates. The samples contained a 1000Å GaAs buffer and were grown without MEE, identical to samples 1-3. The SiN coating was etch in a (4:1) DI:HF solution prior to a 20 minute UV-Ozone cleaning similar to the procedure used for the GeSi substrates. For these three samples (9-11), \( \tau_p = 9.8 \) ns and \( S = 1.8 \times 10^3 \) cm/s. \( S \) does not appear to be effected by the additional surface cleaning procedures. In fact, combined with the data from table 4.2, these results imply that the Ge surface requires surface cleaning to optimize both \( \tau_p \) and \( S \). In particular, the UV-Ozone cleaning appears to be necessary in order to obtain low interface recombination velocities. However, \( \tau_p \) is reduced by more than 50% compared to the non-SiN coated samples cleaned via UV-Ozone, a significant fact since the GeSi substrates contain a similar coating and require a similar cleaning procedure. These results indicate that in addition to the residual TDD, the surface preparation could also play a significant role in reducing \( \tau_p \) for the GaAs/GeSi making it difficult to determine whether the TDD is indeed completely responsible for the reduction in \( \tau_p \). The following section on GeSi lifetime considers these concerns.
Figure 4.13: TRPL decay data for a series of GeSi DH samples. Table 4.4 shows extracted TRPL lifetimes from exponential curve fitting.

4.2.3 GaAs/GeSi minority carrier lifetime

In addition to the reduction in $\tau_p$ due to the incorporation of TD's as discussed in section 3.4.1, as noted in the previous section, the lifetime data for the GaAs/GeSi will likely be impacted by the cleaning/surface preparation conditions. Unfortunately, the ability to separate the impact of TD's and surface cleaning technique was limited due to sample limitations and the desire to protect the GeSi surface during shipping. Therefore, for this work a standard cleaning procedure was adopted and assumed to be independent of the lifetime parameters. As will be discussed in the following sections, the lifetime data obtained indicate that this may in fact be a valid assumption even though the previous data for Ge wafers is contradictory.
Figure 4.14: Cross-sectional TEM of GaAs/Si 0.5 μm DH structure with 1μm GaAs buffer. Nucleation without MEE results in small APB formation at the GaAs/GeSi interface.

S = 3.9x10^3 cm/s

Figure 4.15: Plot of $1/\tau_{\text{TRPL}}$ vs. $1/d$ dependence for GaAs/GeSi TRPL lifetimes extracted from Figure 4.14. (±10% error for TRPL exponential fitting) Curve fitting provides $\tau_p$ and S values from equation 4.1.
Figure 4.13 shows the TRPL decay data for a series of three samples, d = 1.5, 1.0, and 0.5 µm, grown on GeSi substrates with TDD’s of ~2x10^6 cm^-2. The samples contained a 1µm GaAs buffer and the nucleation was completed without MEE. Figure 4.14 shows a TEM image of one of the DH structures which verifies the GaAs/GeSi interface control even without the MEE nucleation, similar to that demonstrated on the Ge wafer, figure 4.9. Figure 4.15 plots the TRPL lifetimes, resulting in τ_p = 7.7 ns and S = 3.9x10^3 cm/s.  

A number of conclusions can be drawn from this first GaAs/GeSi sample set. First, the interface recombination velocity is comparable to that obtained on the Ge wafer, indicating that the surface crosshatch morphology is not limiting the surface recombination velocity. This is not unexpected since the depth of the crosshatch, ~24.5 nm rms roughness, is entirely accommodated via surface steps over the periodicity of the crosshatch, ~5000Å, and does not include any surface facets. In fact, the electron wavelength is such that the crosshatch should be transparent to the electron similar to that demonstrated for lateral electron transport in FET’s (2DEG mobility) along crosshatched surfaces.[22,23]

More important than the high S value, τ_p = 7.7ns was the highest minority carrier lifetime ever reported at the time (Dec. 1998) for GaAs/Si epitaxy, more than doubling the previous record of ~3ns even though TDD’s of 1-4x10^6 cm^-2 were reported.[16,24,25] Figure 4.16 shows the theoretical dependence of τ_p on TDD discussed in section 3.4.1 and following equation 4.1.[15] In this case, τ_o, the minority carrier lifetime independent of TD’s, is chosen to be 19ns, the lifetime determined for GaAs/Ge in the previous section. Additionally, figure 4.16 includes the best GaAs/Si data reported in the literature for
Figure 4.16: Plot of GaAs/GeSi bulk minority carrier lifetime value extract from figure 4.7 with the theoretically expected lifetime dependence on threading dislocation density.\footnote{15} Data points labeled (Δ) and (□) are GaAs/Si data from references 26 and 27 respectively.

comparison. However, only those samples whose dislocation densities have been verified by extensive EPD and/or TEM measurements have been included, keeping in mind that EPD measurements alone (as well as other techniques such as x-ray diffraction) are well-known to underestimate the actual TDD due to dislocation pile-ups\footnote{4} and that TEM statistical limits become problematic for TDD's below \( \sim 1 \times 10^7 \text{ cm}^{-2} \). Additionally, the comparison data is limited to those data which have been extracted from TRPL lifetimes to provide unambiguous comparisons.\footnote{26,27} The GaAs/GeSi lifetime, \( \tau_p = 7.7 \text{ ns} \), agrees well with the theoretical curve and clearly demonstrates minority carrier properties which are superior to those achieved by other GaAs/Si integration techniques to date, implying that the GaAs/GeSi interface nucleation methodology successfully controlled the interface
and more importantly that the GeSi graded buffer is a viable GaAs/Si integration approach for achieving high quality GaAs with low TDD. Additionally, the close agreement to theory implies that the surface cleaning technique is not limiting either \( \tau_p \) or \( S \), unlike the case demonstrated for the Ge wafers, table 4.3. The close agreement to theory also implies that the TDD calculated for the Ge buffer, \( \sim 2 \times 10^6 \text{ cm}^{-2} \), is indeed an accurate measure of the TDD in the GaAs epilayer, indicating no additional TD nucleation at the GaAs/Ge interface. Figure 4.16 further demonstrates that future improvements in the current dislocation density should result in significant improvements in lifetime beyond the current state-of-the-art value. Indeed, we did find this to be true as is discussed later in this section. Furthermore, the model indicates that the TDD need only be reduced to \( \sim 5 \times 10^5 \text{ cm}^{-2} \) in order to achieve lifetimes comparable to homoepitaxial GaAs or GaAs/Ge. The significance of this lifetime result is further pronounced by the fact that GaAs/Si TDD's as low as \( 5 \times 10^5 \text{ cm}^{-2} \) have been reported while lifetimes to date have never successfully exceeded \( \sim 3 \text{ ns} \), implying that the GeSi graded buffer approach has likely enabled the lowest TDD's achieved to date for GaAs/Si integration.

In the context of this work, these lifetime results are extremely promising for GaAs/Si solar applications. In fact, Yamaguchi and co-workers have successfully achieved single-junction GaAs/Si solar cell efficiencies of 18.3 \% AM0 with lifetimes of only 2ns, although these results are over a decade old and have never been repeated or exceeded since.\[^{28}\] Ringel et. al. have also shown theoretical calculations indicating that AlGaAs/GaAs single-junction (SJ) solar cell efficiencies of 20\% AM0 (23\% AM1.5) are achievable for a minority carrier lifetime of only 8 ns, less than 50\% of the typical

\[^{28}\]
homoepitaxial GaAs value,\textsuperscript{[29]} indicating that the current GaAs/GeSi integration methodology should also enable the fabrication of SJ-GaAs solar cells with record efficiency.

Before considering GaAs/GeSi device results, it should be noted that, unlike the Ge samples, a 1\textmu m GaAs buffer was exploited for the GaAs/GeSi growth in order to move the active region of the DH structure further from the GaAs/GeSi interface. Therefore, although the lifetime data is encouraging and exceeds previous results, the GaAs buffer is 10x thicker than that used during the GaAs/Ge epitaxy and \sim33\% of the 3\textmu m GaAs “critical thickness” beyond which GaAs epilayer cracking is reported to result during GaAs/Si epitaxy due to thermal mismatch.\textsuperscript{[9,10,11]} In order to minimize the thermal mismatch concerns as introduced in section 1.3.2, it is important to be able to minimize this GaAs buffer. Therefore, additional samples were grown in order to determine the impact of the GaAs buffer thickness on both $\tau_p$ and $S$.

First, figure 4.17 shows the $1/\tau_{TRPL}$ versus $1/d$ dependence for multiple Ge and Ge/GeSi/Si substrates, each for a range of DH thicknesses. The data for the Ge substrates are replotted from figure 4.11. All the GaAs/Ge/GeSi/Si DH structures plotted contain a minimal 1000Å GaAs buffer, not a 1.0\textmu m buffer as in figure 4.15. The observed linear relationships imply that both $\tau_p$ and $S$ are consistent from run-to-run for both the Ge and Ge/GeSi/Si substrates. Since $S$ is proportional to the line slope, equation 4.1, the parallel lines indicate that the interface recombination velocities achieved on Ge/GeSi/Si are, within experimental error, identical to those for the Ge substrate. In addition to demonstrating excellent reproducibility of $\tau_p$ and $S$ over many runs, these results indicate
that there is no degradation in $S$ from the Ge to the Ge/GeSi/Si substrate even for the minimal 0.1 μm GaAs buffer. Note that, since $\tau_p$ can be extracted via equation 4.1 for a single TRPL decay curve using a single DH thickness ($d$) if the interface recombination velocity is known, the reproducibility demonstrated for $S$ over multiple runs on Ge and Ge/GeSi/Si for various GaAs buffer thicknesses provides the opportunity to extract $\tau_p$ from a single DH with a high degree of confidence.

To investigate the dependence of $\tau_p$ on GaAs buffer thickness, table 4.4 shows a compilation of lifetime data for 29 different DH growths on both Ge and Ge/GeSi/Si substrates for different GaAs buffer thicknesses from 1000 Å to 1.0 μm. For the GaAs/GeSi cases where multiple DH thicknesses were not available in order to extract $\tau_p$
Table 4.4: Compilation of lifetime data for 29 DH samples with similar growth conditions \((n=1.1 \times 10^{17} \text{ cm}^{-3})\). GaAs buffer thickness indicates the proximity of the GaAs DH to the GaAs/Ge interface. In all cases, APD formation was suppressed. \(^{[1]}\)

Indicates substrates without UV-Ozone treatment.

Indicates samples where multiple data points were not available. For these cases, \(\tau_p\) was calculated assuming \(S = 2 \times 10^3 \text{ cm/s}\).

and \(S\) via equation 4.1, \(S\) was assumed to be \(2 \times 10^3 \text{ cm/s}\), the average \(S\) value of samples J-X, and \(\tau_p\) was calculated from equation 1. As previously stated, the reproducibility demonstrated for \(S\) in figure 4.17 allows \(\tau_p\) to be calculated with a high degree of confidence for only a single DH thickness.

As shown in table 4.4, the bulk lifetime values obtained for all GaAs DH growths on the GeSi substrates ranged from \(~6\) ns to 10 ns. The reduced lifetime compared to that obtained for GaAs growth on Ge is a direct consequence of the increased TDD from
\(~1 \times 10^4\) cm\(^{-3}\) for Ge wafers to \(5 \times 10^5 - 2 \times 10^6\) cm\(^{-2}\) for the various GeSi substrates as measured by EPD on the GaAs/Ge/GeSi/Si. Note that the 6 ns to 10 ns lifetimes match the range theoretically expected for TDD values of \(5 \times 10^5 - 2 \times 10^6\) cm\(^{-2}\) as calculated using M. Yamaguchi's model for bulk minority carrier lifetimes limited by recombination at threading dislocations for an n-type doping density of \(1.1 \times 10^{17}\) cm\(^{-3}\).[15] The (new) record 10.5 ns GaAs/Si lifetime demonstrates continued improvement over the 7.7 ns lifetime previously achieved due to continued TDD reduction in the GeSi graded buffer and is only a 50% reduction from homoepitaxial GaAs results, indicating that GaAs/Si lifetimes comparable to homoepitaxial could be attained with minimal additional TDD reduction through graded buffer optimization. A significant result considering GaAs/Si lifetimes have seen no improvement in the last decade of research. Figure 4.18 shows the additional GeSi lifetime data plotted with the theoretical dependence of \(\tau_p\) on TDD in addition to the 7.7 ns lifetime achieved for a 1µm GaAs buffer. Even with a 1000 Å buffer, the lifetime values are consistent with the theoretical dependence and are reproducible over a series of growth runs on various GeSi substrates. Note that multiple GeSi substrates were used in this work, accounting for the slight variations in TDD as the graded buffers were continually optimized for lower TDD. Moreover, table 4.4 shows that the \(\tau_p\) and S values are not dependent on the GaAs buffer thickness, indicating that the GaAs buffer can safely be reduced to an almost negligible thickness of 1000 Å with no measurable degradation of either \(\tau_p\) or S. Most importantly, the demonstration of a greater than 10ns minority carrier lifetime implies that the GeSi system has successfully overcome what many considered a fundamental limit to TDD reduction for GaAs/Si.
Figure 4.18: Plot of bulk minority carrier lifetime values measured for GaAs/GeSi samples listed in Table 4.4 with the theoretically expected lifetime dependence on threading dislocation density. [after 15]

integration by controlling the mismatch relaxation in the Group IV graded buffer. The GaAs/Si material system now approaches the quality of homoepitaxial GaAs, from a minority carrier perspective, and can be treated similar to the GaAs/GaAs system for device design (solar). The ability to successfully translate the GaAs/GeSi structural and state-of-the-art minority carrier properties into high efficiency solar cells will be discussed in Chapter 6.

4.3 Conclusions

The GaAs/Ge interface nucleation procedure previously demonstrated to simultaneously eliminate TD nucleation, EPB nucleation, and atomic diffusion at the GaAs/Ge interface has been found to provide similar control for the GaAs/Ge/GeSi/Si interface with no detrimental impact from either residual threading dislocations or the
crosshatched surface morphology. In addition to the structural control of the interface, minority carrier lifetime measurements revealed excellent minority carrier properties, \( \tau_p \) and \( S \), even in close proximity to the GaAs/GeSi interface. The highest minority carrier lifetime achieved for the GaAs/GeSi system was 10.5ns, table 4.4. As previously stated, this value is a record for GaAs/Si material quality and is a direct result of dislocation density control through the exploitation of the GeSi graded buffer. The excellent agreement with the theoretical dependence of \( \tau_p \) on TDD verifies that the GaAs/GeSi interface was also successfully controlled during GaAs nucleation similar to that determined previously for Ge wafers. These results are extremely encouraging for a number of device applications and should enable state-of-the-art GaAs material quality for this new GaAs/Si integration methodology. In the following chapters GaAs/GeSi devices will be considered, with particular interest in achieving record efficiencies for GaAs/Si solar cells.

4.4 References

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8 Charles Evans and Associates, private communication.


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CHAPTER 5

ELECTRICAL CHARACTERISTICS OF GaAs/Ge and GaAs/Ge/GeSi/Si

p/n-JUNCTION DEVICES

The previous chapter demonstrated the ability to control the GaAs/Ge interface for GaAs/Ge/GeSi/Si epitaxy via MBE similar to that previously demonstrated on Ge wafers. This nucleation methodology combined with the unique capability of the GeSi graded buffer integration technique to minimize threading dislocations and reduce dislocation pile-ups has enabled record GaAs/Si material quality as indicated by minority carrier TRPL measurements. However, although record material quality has been achieved through interface control during nucleation via the “optimum” nucleation procedure outlined in table 4.1, the success of the integration technique must ultimately be defined by the ability to produce device qualities comparable to that achieved for homoepitaxial GaAs. In this chapter, the impact of the GaAs/Ge interface nucleation on GaAs/Ge and GaAs/GeSi devices is investigated. Specifically, I-V characteristics of simple p/n junction diodes are compared for GaAs, Ge, and GeSi substrates. In the first section I-V characteristics related to the formation of the GaAs/Ge interface as well as device fabrication procedures are discussed. Specifically, the impact of these factors on a series
resistance effect, $R_s$, in the I-V response is investigated. Possible sources of $R_s$ are considered with special attention given to the Ge epilayer thickness. Simple device modeling suggests that the Ge epilayer can be modified in order to reduce the impact on the diode I-V characteristics. A detailed investigation into the impact of the Ge epilayer thickness on device performance is presented. Finally, the achievable GaAs/Ge and GaAs/GeSi device performance (small area diodes) is compared to that found for homoepitaxial GaAs and the outlook for larger area devices is discussed, i.e. solar cells.

It should be noted from the onset that while the bulk of this chapter primarily considers device “problems/limitations” associated with the current GaAs/Ge nucleation technique, it is important to maintain a proper perspective for this discussion. The series resistance effect investigated does pose a limitation to the integration of GaAs/Ge devices as well as GaAs/GeSi devices due to the GaAs/Ge interface nucleation process used and warrants analysis in addition to that provided in this research. However, the limitations discussed in this chapter are only a primary concern for future work which will include multi-junction cell designs which are actively exploiting the GaAs/Ge interface region for carrier collection. These devices are not directly considered in this dissertation. For the single junction cell design which is of primary interest for this research, the ability to minimize the impact of the GaAs/Ge interface nucleation on device performance as discussed in section 5.4.2 does enable the successful fabrication of high efficiency GaAs/GeSi and GaAs/Ge solar cells as detailed in chapter 6. From this perspective, the series resistance associated with the GaAs/Ge interface nucleation should be thought of as an “efficiency loss mechanism” (a secondary effect) related to the unique MBE nucleation
procedure required in order to control both APB's and TD's at the GaAs/Ge interface. While methods to reduce this effect may warrant further consideration, the series resistance effect does not impede the ability to fabricate high efficiency GaAs/GeSi solar cells in order to characterize the impact of the GeSi graded buffer integration technique on GaAs/Si device performance, the long term goal of this research.

5.1 I-V characteristics of p/n GaAs/Ge solar cells

5.1.1 Light I-V response and the "kink" effect

Figure 5.1 shows the light I-V response of for GaAs/GaAs and GaAs/Ge single-junction solar cell structures grown via MBE (structure from figure 3.1). The GaAs/Ge sample was grown using the interface nucleation procedure outline in table 4.1 without MEE nucleation. The thickness of the unintentionally doped (uid) epitaxial Ge layer was 300Å. Although the GaAs/Ge material quality has been demonstrated to be APB-free with a minority carrier lifetime comparable to that of homoepitaxial GaAs, \( \tau_p = 19 \text{ns} \), figure 5.1 demonstrates that the GaAs/Ge device quality is dramatically different than that obtained for homoepitaxial samples. Figure 5.2 shows the "dark" I-V characteristics for the same sample set.

Considering the log I-V plot, instead of an exponential increase in current the GaAs/Ge sample is demonstrating a "rolling" increase in current which is a characteristic effect of series resistance. The "rolling" increase results from a more linear (ohmic, \( V = IR \)) rather than exponential (\( I = \exp(qV/nkT) \)) increase in current. (A similar effect is
Figure 5.1: Light I-V comparison between GaAs/GaAs and GaAs/Ge single junction solar cells. I-V data is for 0.2x0.2 cm² cells prior to cap etch and ARC.

Figure 5.2: (a) Linear and (b) log I-V data for 1mm² GaAs p-n junction diodes fabricated on GaAs and Ge substrates. Device structure is identical to that for the single-junction solar cells seen in figure 5.1.
Figure 5.3: Light I-V response of an 8 cm$^2$ GaAs/Ge solar cell illuminated by two different solar simulators. The effect of a "weak" p-n junction formed in the Ge substrate is not evident in the "one-light" simulator due to an infrared content which is higher than for the AM0 spectrum.$^{[1]}$

typically seen during high level injection for diodes when series resistance losses ($I^2R$) become significant.) While both $J_{sc}$ and $V_{oc}$ appear unaffected by the series resistance, figure 5.1, the "knee" in the GaAs/Ge light I-V significantly reduced the Fill Factor (FF) which in turn reduces the conversion efficiency, $\eta$, of the cell. This effect at first appears to be similar to the well-known "kink" effect reported in the light I-V response of p/n GaAs/Ge cell grown by MOCVD, figure 5.3.$^{[1]}$ In the MOCVD reports, the formation of a weak Ge p/n junction by Ga and As diffusion at the GaAs/Ge interface was found to be responsible for the light I-V characteristics.$^{[2]}$ The higher $V_{oc}$ value (higher than SJ-GaAs where $V_{oc}=1030$ mV) indicates the presence of a Ge p/n junction (second junction) which is "actively" contributing to photon collection, i.e. a multiple junction cell. The presence of the Ge junction was verified by spectral response. The "kink" effect in the light I-V
was determined to result from the poor current matching between the top (GaAs) and bottom (Ge) cells. Additionally, the Ge junction was determined to be driven into reverse bias during cascade operation, with the superposition of the reverse characteristic of the GaAs/Ge interface and the forward bias characteristics of the p-n junction leading to the kinked I-V response.\textsuperscript{[1,3,4]}

While this “kink” effect appears to resemble that seen in figure 5.1, the fact that \textit{V}_{oc} shows no increase indicates that an “active” Ge junction is not present. In fact, this result was verified by spectral response measurements which indicate no current collection below the GaAs bandgap, and therefore no “active” Ge p/n junction formation. While GaAs/Ge growth via MOCVD is well-known to result in both Ga and As diffusion over many microns, the lack of formation of a Ge p/n junction is consistent with the SIMS data discussed in chapter 4 indicating no Ga diffusion and minimal As diffusion at the GaAs/Ge interface, figure 4.6 (using the “optimum” nucleation methodology for growth via MBE). Although not discussed here, GaAs/GeSi p/n junction devices demonstrate a similar I-V response, leading to the conclusion that, while different than the characteristics seen for MOCVD growth, the GaAs/Ge interface region is also likely responsible for the series resistance effect of the I-V response seen here, figure 5.1.
Figure 5.4: Schematic showing two different mesa etch depths used for isolation during this research. (a) Sample I contains a “complete” mesa etch which isolates the GaAs/Ge interface as well as the GaAs p-n junction. (b) The mesa etch for sample II is stopped approximately halfway through the n-GaAs base region and isolates only the GaAs p-n junction. Sample II will be referred to as a “limited” or “incomplete” mesa etch.

5.1.2 Etch depth dependence of I-V response

In order to verify the impact of the GaAs/Ge interface on the I-V response, two identical solar cell structures were fabricated. In both cases, processing was identical with the exception of the final mesa etch to isolate the individual devices. As shown in figure 5.4, for sample I the mesa depth was into the Ge substrate while for sample II the mesa was limited to just past the GaAs p/n junction. Figure 5.5 shows the linear and log I-V comparison between these two samples and a homoepitaxial GaAs “ideal” cell. While some series resistance ($R_S$) is still present in sample II, the magnitude is greatly reduced from that seen for sample I where the GaAs/Ge interface region is isolated by the mesa etch. Since sample II does not isolate the device current through this region, these
Figure 5.5: (a) Linear and (b) log I-V data for a GaAs/Ge single junction solar cell structure grown by MBE after 1) “complete” (sample I) and 2) “limited” (sample II) mesa etch. Note the decrease in series resistance for sample II. The “ideal” homoepitaxial GaAs sample is included for comparison. (Note that in all cases the “inflection” voltage on the log I-V curve is not 0V. This shift in the I-V to positive voltage is an artifact of the measurement under room light and does not impact the curve at higher voltage where the series resistance is of interest.)

results are consistent with a large $R_s$ associated with the GaAs/Ge interface region.

Consider the simple parallel resistor model shown in figure 5.6, where a large GaAs/Ge interface resistance is given by $R_3$. Without isolating the GaAs/Ge interface via the mesa etch, figure 5.6(a), multiple current paths (i.e. $R_1$, $R_2$, etc. = dislocations, defects, sidewalls, etc.) are available across the GaAs/Ge interface “mesa” which is defined by the wafer size rather than the GaAs p-n junction mesa. (Note that the large area “wafer size” mesa also reduces the current density across the GaAs/Ge interface region.)
Figure 5.6: Schematic representation of a parallel resistor model used to explain the increase in series resistance for a “complete” mesa etch. $R_3$ represents the GaAs/Ge interface resistance while $R_1$, $R_2$, $R_4$, and $R_5$ represent additional available current paths (i.e. dislocation, defects, sidewalls, etc.) For (a), since the resistances are in parallel, $R_{\parallel}$ will be less than the smallest resistance value. For (b), $R_{\parallel} = R_3$.

Since $R_{\parallel}$ is defined by:

$$\frac{1}{R_{\parallel}} = \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} + \frac{1}{R_4} + \frac{1}{R_5}; \quad (5.1)$$

$R_{\parallel}$ will be less than that of the lowest resistance path. Conversely, in the case of sample I, figure 5.6(b), $R_{\parallel}$ is equal to the resistance of the GaAs/Ge interface region, $R_3$, since the mesa etch effectively eliminates any other conduction paths. Therefore, one solution to the series resistance effect on GaAs/Ge devices, which will be discussed later in the chapter, is to simply avoid the isolation of the GaAs/Ge interface region with the
processing mesa etch. While this is a practical solution in order to investigate the impact of other factors on device performance, i.e. TDD for GaAs/GeSi, as shown in figure 5.5, there is still a measurable series resistance which will impact device performance. Specifically for solar cells, increased Rs will reduce the FF directly impacting device efficiency. Therefore, a continued investigation into the source of the series resistance is warranted.

5.2 Source of Rs in GaAs/Ge devices

Due to the implications of high series resistance on GaAs/Ge device performance, an investigation into the source of the series resistance was completed. Specifically, the impact of each step in the GaAs/Ge nucleation procedure was considered. While providing excellent GaAs material quality (both structural and minority carrier), the nucleation procedure may not be "optimum" with respect to carrier transport across the GaAs/Ge interface. After a systematic study as to the impact of each of the GaAs/Ge nucleation steps (i.e. MEE, epitaxial Ge, etc.), it was found that variations in the epitaxial Ge layer thicknesses were the only factors which greatly impacted the diode I-V characteristics. Specifically, the Rs value was greatly reduced when reducing the thickness of the uid-Ge layer from 1000Å to 300Å. Upon further investigation, C-V profiling of a uid-Ge epilayer on a Ge substrate revealed that the uid-Ge, which was thought to be lightly doped since SIMS profiles indicated no significant Ga or As diffusion (likely n-type due to the As background in the MBE system), was actually heavily p-type, p ~ 1x10^{19} cm^{-3}. Since the Ge/Ge epitaxy could not be affected by
Ga diffusion, a p-type dopant during diffusion for GaAs/Ge epitaxy, SIMS analysis was completed in order to determine the source of the p-type dopant, producing quite unexpected results. As shown in figure 5.7(a), Al and In, both p-type dopants on the Group IV lattice, were present in concentrations of $4 \times 10^{18}$ cm$^{-3}$ and $2 \times 10^{17}$ cm$^{-3}$ respectively, accounting for the p-type nature of the Ge epilayer. However, as shown in figure 5.7(b), the Ge epilayer also exhibits high concentrations of As, O, and Ni, $\sim 3 \times 10^{18}$ cm$^{-3}$, $\sim 3 \times 10^{18}$ cm$^{-3}$, and $\sim 1 \times 10^{18}$ cm$^{-3}$ respectively. In both cases, these results indicate large impurity incorporation in the Ge epilayer which are quite unexpected. Specifically, while both Al and In are group III sources available in MBE growth, both the substrate orientation during growth as well as the Al and In cell temperatures would suggest that neither element should be evaporating/incorporating on the Ge surface during growth. While there are a number of explanations which could account for the high impurity concentrations, including contamination of the Ge source material (either from the stock Ge or due to In and Al “dripping” in the MBE system), the explanation that seems to account for the wide variety of impurities incorporated involves the temperature of the Ge source cell during deposition. The Ge source cell temperature during evaporation is 1460°C, higher than that of any other MBE source. Due to the high temperature, the Ge evaporation results in significant heating of the MBE chamber walls near the Ge cell since the Ge cell is the only cell not isolated by a liquid nitrogen “cryo-shroud”. Since both the Al and In sources are located “near” the Ge, in addition to evaporating As off the chamber walls the chamber heating could result in the re-evaporation of both In and Al leading to the contamination indicated in the SIMS data. Additionally, due to the high
Figure 5.7: SIMS analysis of ~1.1 \( \mu \)m of epitaxial Ge on a Ge substrate. In addition to As incorporation, the Ge epilayer demonstrates high concentrations of In, Al, O, and N. These impurities account for the heavy p-type doping of the uid-Ge layer.
cell temperature the background pressure in the chamber is typically \(5\text{--}7 \times 10^{-9}\) torr during Ge epitaxy (rest pressure \(2\text{--}4 \times 10^{-10}\) torr with other cells heated). The background pressure is largely \(N_2\) generated by the poly-boron nitride (PBN) crucible of the Ge cell at the high growth temperature. While nitrogen is typically considered difficult to incorporate during epitaxy (i.e. InGaAsN epitaxy),\(^5\) the SIMS data indicates a large Nitrogen contamination due to this background pressure. Unfortunately, while the incorporation of Al, In, As, N, and O can be “accounted for” by the above explanation, there is no clear method to eliminate or minimize their incorporation during epitaxy. While it may be possible to better isolate the Ge cell by orienting it in one of the “conventional” source ports which includes liquid nitrogen shrouding, the current system configuration and limited number of ports does not provide this option at OSU. While an alternative solution would be to eliminate the epitaxial Ge layer, previous characterization has demonstrated the Ge epilayer to be a vital step in burying carbon surface contamination and enabling an APB-free GaAs/Ge interface.\(^6,7\) (Recall that controlled mesa etching also provides a method to minimize the impact of the resistive interface.) Therefore, since the incorporation of the p-type Ge epilayer is unavoidable for the current MBE set-up, modeling of the p-type Ge incorporation was investigated in order to determine the theoretical impact on device performance and compare with the current I-V results.
5.3 PC-ID modeling of a p-type Ge epilayer

In order to investigate the impact of the p-type Ge epilayer on device performance, PC-ID (software simulation program) was used to perform device modeling of the diode structure shown in figure 5.8. Along with I-V data, bandgap diagrams were also found as a function of the p-type Ge epilayer doping and thickness. Figure 5.9 shows I-V simulation data for 1000Å, 300Å, and 0Å p-Ge epilayers. Based on the C-V and SIMS data, the p-type doping level was modeled at $1 \times 10^{19}$ cm$^{-3}$. While not identical to the I-V data found for the GaAs/Ge MBE grown samples, the simulation does indicate a “limiting” of the current which is “improved” when the Ge epilayer thickness is reduced from 1000Å to 300Å. In fact, as shown in figure 5.10, as the Ge epilayer thickness is reduced down to 50Å the I-V response is identical to that found without a p-type Ge layer (i.e. “ideal”). As shown in figure 5.11, the reason for this improved I-V performance is that the conduction band “spike” created by the p-type Ge layer is reduced as the Ge layer...
Figure 5.9: Simulated I-V response using PC-ID of the diode structure shown in figure 5.8 for p-Ge epilayer thicknesses of 1000 Å, 300 Å, and 0 Å. 0 Å simulates an “ideal GaAs/Ge interface.

Figure 5.10: Simulated I-V response using PC-ID of the diode structure shown in figure 5.8 for p-Ge epilayer thicknesses of 300 Å, 150 Å, 100 Å, 50 Å and 0 Å. Thinning the p-Ge epilayer to 50 Å results in an I-V response identical to that for the “ideal” GaAs/Ge interface case.
Figure 5.11: Simulated bandgap structure for GaAs/Ge diode structure of figure 5.8 as a function of p-Ge thickness. Note that as the p-Ge layer is thinned the conduction band “spike” inhibiting majority carrier electron transport is reduced. All simulation taken for zero-bias under steady state conditions.

is thinned to the order of the depletion region width. Therefore, device simulation suggests that thinning the p-type Ge layer should result in I-V performance which is comparable to that without a p-type Ge epilayer (i.e. no series resistance effect). For the current research, this would enable the continued use of the Ge epi-layer, which is required in order to suppress interface APB and TD nucleation, without the negative impact the series resistance generated by the GaAs/Ge interface region presents for device performance. However, while the 1000Å and 300Å Ge layers were shown to bury the
carbon interface contamination and minimize GaAs/Ge defect nucleation, it must also be
determined whether a minimal 50Å Ge epilayer will produce similar results. The
following section discusses device results obtained from a series of samples grown to
determine the impact of thinning the Ge epilayer on device performance.

5.4 Impact of Ge epilayer thickness on I-V characteristics

In order to investigate the impact of the uid-Ge epilayer thickness (p~1x10^{19} \text{ cm}^{-3})
during GaAs/Ge nucleation on diode I-V characteristics, a series of samples were grown
with the structure shown in figure 5.8 without MEE nucleation and Ge epilayer
thicknesses of 1000Å, 300Å, 150Å, 100Å, and 50Å. For these three samples, two cases
were considered. 1) Samples mesa etched into the Ge substrate isolating the GaAs/Ge
interface region (figure 5.4(a)) and 2) samples mesa etched only through the GaAs p/n
junction, (figure 5.4(b)).

5.4.1 Case 1: “complete” mesa isolation

Figure 5.12 shows the I-V response found for the samples subjected to a
“complete” mesa isolation etch (case 1), figure 5.4(a). While reducing the Ge thickness
does result in increased current flow similar to that predicted by the simulation results,
the minimal 50Å uid-Ge buffer does not result in device performance comparable to that
of homoepitaxial GaAs (or simulation results with a 0 Å p-Ge epilayer). (Note that the
current levels found are similar to those predicted by simulation, figure 5.9) The
deviation from the simulation results suggests that either the uid-Ge epilayer is doped
more heavily than the C-V data suggests at 1x10^{19} \text{ cm}^{-3}, or, more likely, that there are
Figure 5.12: Linear I-V plot of GaAs/Ge diode structures for varying Ge epilayer thicknesses when fabricated with a “complete” mesa etch. While not identical to simulation, note that the current scale is identical to that obtained during simulation, indicating that the p-Ge epilayer is indeed responsible for the series resistance effect. However, unlike the simulated data, the 50 Å Ge epilayer is not sufficient to eliminate $R_s$.

Additional factors at the GaAs/Ge interface which are impacting the current transport characteristics (i.e. interface states, buried carbon surface contamination, etc.). It is interesting to note that while the initial GaAs/Ge solar cell development was concentrated on p/n devices similar to the ones in this research, GaAs/Ge solar cell manufacturers have uniformly converted to an n/p cell design. The history of research documenting “problems” with p/n device performance combined with this fact suggests that the “non-trivial” control of the GaAs/Ge interface is possibly more easily accommodated in an n/p design. Based on these results and considering the current industry commitment to n/p cell design, future GaAs/GeSi research should also consider the development of p-type GeSi substrates to demonstrate compatibility with the current industry standards.
While much additional investigation into the characteristics of the GaAs/Ge interface is possible, this research chose to concentrate on GaAs/GeSi device integration, specifically solar cells. Therefore, as discussed in previous sections, since limiting the mesa isolation etch to only the GaAs p/n junction interface (figure 5.4(b)) results in a much improved device performance while still demonstrating some series resistance, this method was chosen for fabricating solar devices in order to concentrate on the impact of GaAs/Si integration issues (i.e. thermal expansion mismatch and TDD) on device performance rather than the GaAs/Ge interface. (Note that this refers to the "series resistance" issues (i.e. transport) and not APB formation or atomic diffusion which have already been addressed and are controlled for the current MBE nucleation procedure.)

5.4.2 Case 2: limited mesa isolation

In order to determine the impact of the uid-Ge epilayer thickness, $t_{Ge}$, on the device performance for an "incomplete/limited" mesa etch, diodes with "limited" mesas were fabricated on the same structures measured in the previous section for a "complete" isolation etch. As shown in figure 5.13, in addition to the "limited" mesa etch improving the I-V characteristics dramatically over the samples with a "complete" mesa etch, thinning the p-Ge epilayer further reduces the series resistance impacting the I-V performance. As shown in figure 5.14, a value for $R_s$ can be extracted from the high current region of the I-V curve where the current increase is no longer exponential with voltage (i.e. no longer linear on the log I-V plot).[^8]
Figure 5.13: (a) Linear and (b) log I-V plots for samples identical to figure 5.12 but fabricated with only a "limited" mesa etch into the n-GaAs base region. Note the significant decrease in $R_s$ as the uid-Ge epilayer is reduced from 1000 Å to 50 Å.
Figure 5.14: Plot of the characteristic I-V shape for an ideal p-n junction diode showing the various regions of n=1 and n=2 operation. At high currents, series resistance losses emerge as a "roll-off" in the linear increase of the log I-V plot (exponential on linear scale). Any "roll-off", even at lower current can be attributes to a "series resistance - like" effect.

\[ \frac{dV}{d(\ln I)} = I \times R_s + n \left( \frac{k_B T}{q} \right) \]  \hspace{1cm} (5.2)

where \( n \) is the diode ideality factor. Using this technique, figure 5.15 plots \( R_s \) as a function of \( t_{Ge} \). While \( R_s \) is not eliminated when \( t_{Ge} \) is thinned to 50 Å, \( R_s \) is reduced as \( t_{Ge} \) is thinned from 1000 Å (\(~5300 \, \Omega\)) to 150 Å (\(~80 \, \Omega\)), with no additional reduction in \( R_s \) as \( t_{Ge} \) is reduced to 50 Å. \( R_s \) was found to be \(~5\, \Omega\) for homoepitaxial GaAs samples. Note that \( t_{Ge} = 0 \, \text{Å} \) is not used since previous GaAs/Ge nucleation results indicate the need for a Ge buffer in order to suppress APB and threading dislocation nucleation.
Figure 5.15: Plot of series resistance versus epitaxial Ge thickness, $t_{\text{Ge}}$, for diode structure of figure 5.8. 500\(\mu\)m (■), 750\(\mu\)m (●) and 1000 \(\mu\)m (▲) diodes were measured. Note $R_S$ decreases with decreasing Ge thickness but does not reach the homoepitaxial GaAs value at 50\(\AA\). Note that $t_{\text{Ge}} = 0$ \(\AA\) is not used since GaAs/Ge nucleation results indicate the need for a Ge buffer in order to suppress APB and threading dislocation nucleation. ($R_S$ found via equation 5.2.)

From these results, we conclude that $t_{\text{Ge}} < 150$ \(\AA\) produces the lowest $R_S$ and should enable the best GaAs/Ge device performance in spite of the uid-Ge (p-type) buffer.

Therefore, while the GaAs/Ge interface issues are not completely solved and warrant further investigation (particularly when considering multi-junction cell designs), the current reduction in series resistance is sufficient to enable the development of high
efficiency GaAs/Ge and GaAs/GeSi solar cells. Recall that since the complete GaAs/Ge (and GaAs/GeSi) integration technique discussed during this research is unique, similar to any other device development process, factors limiting the device performance must be identified and addressed. Fortunately, $R_s$ in this case is a secondary effect which does not prohibit the characterization of GaAs/GeSi devices and the impact of the graded GeSi buffer integration technique (i.e. TDD, cross-hatch, and thermal expansion mismatch) on their performance, the long term goal of this research. Therefore, GaAs/Ge and GaAs/GeSi integration for solar cell devices was continued (while limiting the mesa etch to the GaAs p/n junction region) knowing that the minimal $R_s$ from the GaAs/Ge interface may result in some reduction in device efficiency parameters, specifically Fill Factor. While not available at the time of this publication, TEM analysis is currently underway to investigate any impact of reducing the uid-Ge epilayer thickness (down to 50 Å) on APB and TD nucleation at the GaAs/Ge interface. (Note that I-V results indicate no additional leakage current, implying similar control of the GaAs/Ge interface independent of the uid-Ge buffer thickness down to 50 Å.)

5.5 GaAs/GeSi I-V characteristics

Recall that while much of the above discussion considered GaAs/Ge growth, the issues associated with the GaAs/Ge interface apply to both GaAs/GeSi as well as GaAs/Ge epitaxy. For the remainder of this dissertation, in order to minimize the impact of the GaAs/Ge interface series resistance on the GaAs/GeSi device quality and
Figure 5.16: Comparison of GaAs p-n junction diode characteristics on GaAs, Ge, and GeSi substrates.

characterize the impact of TDD's as well as thermal expansion mismatch, all device fabrication was completed while minimizing the mesa etch only into the base of the solar cell structure, figure 5.4(b).

Figure 5.16 shows I-V curves obtained for GaAs p/n junction diodes (structure from figure 3.1), grown on GaAs, Ge, and Ge/GeSi/Si substrates with mesa etches limited to the GaAs p/n junction. Included for comparison is an identical GaAs/Ge device structure with a “complete” mesa isolation etch of the GaAs/Ge interface. As shown on the linear I-V plot, 1 mm diameter diodes grown on each substrate demonstrated nearly identical I-V characteristics (for a limited mesa etch), with turn-on voltages of ~1 V for all cases, and identical reverse leakage currents out to at least ~2 volts, with a value of less than 15 nA at ~2 V in each case. Reverse saturation current densities ($J_0$) were ~2.0
x10^{-12}, ~5.0 x10^{-11}, and ~1.0 x10^{-10} A/cm^2 for the GaAs, Ge, and Ge/GeSi/Si substrate respectively, with ideality factors (n) of ~1.5, ~1.5 and ~2.0 respectively. The similar current characteristics indicate that the residual TDD of ~8x10^5 cm^{-2} - 1x10^6 cm^{-2} in the cell structures on Ge/GeSi/Si are not introducing significant shunt or recombination currents in these diodes that would otherwise significantly lower the diode turn on voltage and increase the reverse leakage current and suggests that shunt currents in a completed, GaAs cell on Ge/GeSi/Si should not be significantly impacted by threading dislocations at our current threading dislocation density. In the following chapter, based on the excellent material and I-V characteristics of the GaAs/GeSi devices, we consider the extension of the GaAs/GeSi device performance to large area GaAs/Ge/GeSi/Si solar cells. Note that GaAs/Ge devices are also investigated to monitor the impact of the GaAs/Ge interface on device performance.

5.6 References


While the previous sections of this dissertation have verified the material quality which can be achieved through the use of the GeSi graded buffer for GaAs/Si integration, the final goal of this research is to determine if the improved material quality can be translated into improved device quality, specifically higher efficiency GaAs/Si solar cells. Since only a small area is sampled during the material quality characterization, TRPL, TEM, SIMS, the large area solar cell is an excellent characterization tool for device quality since it can be impacted by both epilayer cracking due to thermal expansion mismatch and the GeSi heterogeneous surface defects as well as the residual TDD. Hence, the solar cell is, in a sense, the most stringent device test for lattice mismatched electronic materials. In this chapter, both the growth and characterization of single junction solar cells are discussed along with some limitations to applying the GeSi graded buffer to large area solar cell integration.
6.1 Structure and design of single-junction GaAs/GeSi solar cells

Figure 6.1 shows a schematic of the AlGaAs/GaAs single junction solar cell structure grown by MBE for this research. The structure was chosen based on the GeSi lifetime data indicating $L_p = 1.93 - 2.5 \mu m$ ($\tau_p = 6 - 10 \text{ ns}$) for $n = 1.1 \times 10^{17} \text{ cm}^{-3}$. As shown in figure 6.2, in order for the BSF layer to effectively "reflect" holes in the n-type base toward the p-n junction for collection, the diffusion length of the holes must be large enough for the holes to return to the junction prior to recombining. Of course, this assumes that the interface recombination velocity of the base/BSF interface, $S_p$, is low and does not result in significant recombination at the interface. For solar cell design, a general rule of thumb is for the base width, $W_b$, to be no greater than the diffusion length of minority carriers in the base, again assuming low $S_p$. Note that the choice of $W_b$ is a tradeoff between the ability to collect holes after absorption and prior to recombination.
(requires thinner base) and the ability to absorb photons (requires thicker base). Due to variations in \( L_p \) consistent with TDD variations, \( L_p = 2.0 \, \text{μm} \) was used as a conservative estimate for cell design. Accordingly \( W_B \) was chosen to be 2.0 \( \text{μm} \) for all samples.

Unlike the base, the emitter thickness, \( W_E \), is typically not determined by \( L_n \), but rather by the recombination velocity of the window/emitter interface as discussed in section 3.3.3. While a thicker emitter would provide much needed thickness in order to absorb carriers, the absorption of high energy photons close to the \( \text{Al}_{0.8}\text{Ga}_{0.2}\text{As/GaAs} \) interface combined with the interface recombination velocity and low minority carrier lifetime in the emitter due to high doping requires a thin emitter in order to guarantee collection of the photoinjected electrons. For typical designs, \( W_E = 4000-5000 \, \text{Å} \) for p-type emitters and \( \sim 1000\,\text{Å} \) for n-type emitters (due to differences in \( L_n \) and \( L_p \)).

Additionally, due to reports of significant epilayer cracking for the GaAs/Si system for
epilayer thicknesses greater than ~3μm, it is desirable to limit the total GaAs epilayer thickness on the GeSi substrate below this threshold. Therefore, for the samples grown in this work the emitter and base thicknesses were chosen to be 4000 Å and 2.0 μm respectively, resulting in a total device thickness of ~3.25 μm. This design is consistent with PC-1D modeling indicating near optimum carrier collection based on τp(Lp) and S data obtained for GaAs/GeSi TRPL samples.

6.2 MBE growth of GaAs/GeSi solar cells

Table 6.1 provides a detailed growth sequence for the MBE growth of the solar structure of figure 6.1. These steps are in addition to the interface nucleation procedures required for the Ge and GeSi substrates as discussed in chapter 4, table 4.1. The “growth

<table>
<thead>
<tr>
<th>Thickness (Å)</th>
<th>Growth Time (sec)</th>
<th>Sub Temp. (°C)</th>
<th>Doping</th>
<th>III/V Ratio</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>5000</td>
<td>1770</td>
<td>615</td>
<td>n~8x10^17</td>
<td>14:1</td>
<td>n+ GaAs buffer</td>
</tr>
<tr>
<td>1500</td>
<td>480</td>
<td>615</td>
<td>n~8x10^17</td>
<td>12:1</td>
<td>Al0.1Ga0.9As back surface field (BSF)</td>
</tr>
<tr>
<td>Stop A</td>
<td>300</td>
<td>615</td>
<td>-</td>
<td>-</td>
<td>Lower Si doping for base</td>
</tr>
<tr>
<td>20000</td>
<td>7030</td>
<td>615</td>
<td>n~4x10^17</td>
<td>14:1</td>
<td>n- GaAs base</td>
</tr>
<tr>
<td>Stop B</td>
<td>300</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>Lower substrate for p-type emitter, Increase As flux</td>
</tr>
<tr>
<td>4000</td>
<td>1416</td>
<td>575</td>
<td>n~2x10^18</td>
<td>20:1</td>
<td>p-GaAs emitter</td>
</tr>
<tr>
<td>Stop C</td>
<td>1770</td>
<td>575</td>
<td>-</td>
<td>-</td>
<td>Lower Ga cell temp for high Al content window</td>
</tr>
<tr>
<td>500</td>
<td>255</td>
<td>575</td>
<td>p~3x10^18</td>
<td>20:1</td>
<td>p-Al0.85Ga0.15As window</td>
</tr>
<tr>
<td>Stop D</td>
<td>1770</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>Raise Ga, Be temperature for GaAs contact layer</td>
</tr>
<tr>
<td>1500</td>
<td>530</td>
<td>550</td>
<td>p~2x10^19</td>
<td>~28:1</td>
<td>p+-GaAs contact layer</td>
</tr>
</tbody>
</table>

Table 6.1: MBE growth sequence used in this research for the growth of solar cell structures showing growth stops for furnace and substrate temperature changes. Note both growth times and layer dopings were modified for design variations.
stops" are a result of the need to change the Ga and Al furnace temperatures in order to change the AlGaAs alloy composition or to change the substrate temperature in order to minimize Be diffusion during p-type doping. Note that the long, 30 minute, growth stops (C and D) are due to the "settling time" of the Ga and Al furnaces over large temperature swings. These growth stops are undesirable, especially at the emitter/window interface whose interface recombination velocity has a large impact on solar cell performance, but the single Ga furnace on the MBE system makes these growth stops unavoidable.

For all solar cell growths, Ge wafers were cleaned with a 30 sec DI rinse followed by a 20 minute UV-ozone clean. Unlike the TRPL samples, the GeSi substrates were delivered "uncoated" after the UHVCVD growth, eliminating the SiO₂ and photoresist cleaning steps. The ¼-4" GeSi substrates were cleaned with 5 cycles of [10 second H₂O₂, 1 minute DI, 10 second HF, 1 minute DI] etching prior to a 20 minute UV-ozone clean. All GaAs growths were performed on 2" GaAs substrates which were loaded epi-ready (i.e. no cleaning).

Appendix B provides a detailed sequence of the solar cell fabrication procedures followed, including contact metals, lithography procedures, and etch solutions. Solar cell lithography masks included 1 x1 cm², 0.6 x 0.6 cm², 0.4 x 0.4 cm², and 0.2 x 0.2 cm² cells, all with similar metal grid designs but having 5%, 6%, 7.5%, or 10.2% metal coverage area respectively. Figure 6.3 shows completed solar cell with Au fingers and mesa. Cell characterization, light I-V (to determine efficiency) and spectral response/EQE, were completed at NASA Glenn Research Center, considered the national standard for space solar cell characterization.
MOCVD growth was also performed during this research on GaAs, Ge, and GeSi substrates. Since not available at OSU, the MOCVD growths were completed by collaborators at both NASA Glenn Research Center and Sandia National Laboratories, both with significant MOCVD experience. However, neither of these collaborators possessed experience with the complex GaAs/Ge growth process, which requires controlled nucleation in order to eliminate APB’s as discussed in section 1.3.3. (In fact, direct MOCVD growth of GaAs onto bare Ge surfaces resulted in rampant APB formation and poor device performance.) Therefore, since this research has demonstrated the ability to control APB formation via MBE nucleation, GaAs/Ge and GaAs/GeSi buffers (1000Å GaAs buffer) were supplied as a nucleation surface for subsequent MOCVD growth. The impact of this “extra” growth step will be considered in the following sections.
6.3 External quantum efficiency of GaAs/GeSi

While the single junction solar cell design chosen for this research should enable high efficiency GaAs/Si cells, the cell designs were not optimized prior to the growth of GaAs/Si solar cells. Therefore, MBE growth was also performed on Ge and GaAs substrates in order to separate the impact of cell design, growth technique, and material limitations on the solar cell efficiency parameters. (i.e. GaAs/GaAs cell efficiencies will provide an efficiency baseline while comparisons between GaAs/GaAs and GaAs/Ge cell parameters will enable an investigation into the impact of the GaAs/Ge interface nucleation independent of the high residual TDD and surface crosshatch morphology also impacting the GaAs/GeSi cells.)

Figure 6.4 shows EQE data obtained for the single junction cell structure of figure 6.1 grown on GaAs, Ge, and GeSi substrates. The EQE data was taken after completed cell fabrication for all samples. As shown, the EQE data for the cell structure of figure 6.1 appears to be independent of substrate choice, indicating that neither the GaAs/Ge nucleation procedure nor the SiGe graded buffer (TDD or crosshatch morphology) are limiting the photoinjected carrier collection for this GaAs/GeSi cell design. Specifically, the short wavelength (blue response) EQE data for the GeSi substrate indicates that the interface recombination velocity, S, is not higher for GaAs/GeSi than for homoepitaxial GaAs. Additionally, the identical high wavelength ("red") response indicates that the diffusion length in the GaAs/GeSi base is not limiting the collection of photoinjected carriers for a base thickness of 2.0 μm (which was considered in the cell design) since both the GaAs/Ge and GaAs/GaAs cells have a larger Lp than the GaAs/GeSi system.
This conclusion is again consistent with TRPL data and indicates that the minority carrier lifetime reported in section 4.2, for GaAs/GeSi, is accurate and is maintained throughout device fabrication. In order to determine the maximum base thickness for the GaAs/GeSi system, a series of thicker bases could be fabricated in order to determine when $L_p$ begins to limit carrier collection. This experiment was not completed in this research due to substrate supply limitations and the uncertainty of the impact of epilayer thickness on epilayer cracking. However, the identical collection of photoinjected carriers for the GaAs/GeSi, GaAs/Ge, and the homoepitaxial GaAs samples for $W_B = 2.0 \mu m$ is extremely encouraging since the best previously reported AM0 GaAs/Si efficiency of 18.3% was grown using a (thin) 1.3\mu m GaAs base due to the high TDD and low $L_p$.\(^1\)
6.4 Light I-V of GaAs/GeSi solar cells grown by MBE

The excellent agreement between the GaAs/Si and homoepitaxial GaAs EQE data verifies that the GaAs material quality was maintained through device processing and ensures that $J_{sc}$ will be independent of substrate choice. However, $J_{sc}$ is much easier to “match” to homoepitaxial GaAs since the solar cell design can be (and was) used to compensate for shorter diffusion lengths. On the other hand, $V_{oc}$ is not as easily “engineered” and has been a key factor limiting GaAs/Si solar cell efficiency. Maximum GaAs/Si $V_{oc}$ values have typically been limited to $\sim 900$ mV (a single, isolated maximum to date of 940 mV has been reported) due to recombination in the depletion region from increased TDD, while $V_{oc}$ values for homoepitaxial GaAs exceed 1030 mV (device design dependent). $V_{oc}$ is defined in equation 6.1. For high TDD, $J_0$ is assumed to be dominated
by recombination current in the depletion region as defined by equation 6.2, where \( W_{dp} \) is the depletion region thickness assuming a heavily doped p-layer.

\[
V_{oc} = \frac{k_B \cdot T}{e} \times \ln\left(\frac{I_{sc}}{I_0} + 1\right) = \frac{1}{e} \times \left(\frac{E_g + k_B \cdot T \times \ln \frac{I_{sc}}{I_{SO}}}{I_0} \right) \text{ (volts)} \quad (6.1)
\]

\[
J_0 = J_{0,dp} = \frac{e \times n_i \times W_{dp} \times D_p}{2 \times L_p^2} \text{ (A/cm}^2\text{)} \quad (6.2)
\]

Figure 6.5 plots the theoretical dependence of \( V_{oc}, J_{sc}, FF, \) and \( \eta \) on TDD based on the assumption that 1.) the depletion region recombination at TD's dominates \( J_0 \) and 2.) the TDD limits the diffusion length as discussed in chapter 4.\textsuperscript{[21]} The experimental data for GaAs/Si included on the plot, after Yamaguchi,\textsuperscript{[1,3]} indicate that while \( J_{sc} \) values in good agreement with theory have been achieved \( V_{oc} \) values are consistently lower than predicted by this simple model, demonstrating the difficulty in achieving high \( V_{oc} \) for GaAs/Si solar cells. Therefore, while \( J_{sc} \) values comparable to GaAs/GaAs are routinely obtained, GaAs/Si cell efficiencies are limited by the inability to achieve high \( V_{oc} \) values comparable to homoepitaxial GaAs, making \( V_{oc} \) a better indicator of GaAs/Si material quality than \( J_{sc} \).

Figure 6.6 shows light I-V curves obtained for GaAs/Ge and homoepitaxial GaAs solar cells having identical structures prior to ARC and illuminated with an uncalibrated ELH lamp. The excellent agreement between the GaAs/GaAs and GaAs/Ge curves indicates excellent control of the GaAs/Ge interface is obtained and that minimal impact of the GaAs/Ge interface nucleation on the solar properties is expected when considering
Figure 6.6: Light I-V of MBE grown AlGaAs/GaAs single junction solar cells (0.4 x 0.4 cm$^2$) on both GaAs and Ge substrates. Data taken prior to contact layer etch and ARC. The difference recorded in $J_{sc}$ current is due to the measurements being taken on an “uncalibrated” ELH bulb and not a standard AM0 simulator.

the GaAs/GeSi system. However, note that for this specially grown pair of baseline cells, $V_{oc}$~988mV, $J_{sc}$~29.9 mA/cm$^2$, FF~82% and η~17.25% (after complete device processing with anti-reflection coating) which are all below state-of-the-art values for single junction AlGaAs/GaAs solar cell design. In fact, these values are below those obtained for other homoepitaxial AlGaAs/GaAs solar cells grown via MBE at OSU with a similar cell design. The reason for this reduction may be the presence of growth stops during MBE or the particular fabrication sequence used. However, the important thing to keep in mind here is the comparison of otherwise identical GaAs cells grown on two different substrates. The identical response between the GaAs/GaAs and GaAs/Ge cells indicates a minimal impact of the GaAs/Ge interface nucleation or TDD ($\sim 10^4$ cm$^{-2}$) and should translate to the GaAs/GeSi system.
Figure 6.7: Light I-V of MBE grown AIGaAs/GaAs solar cells (0.4 x 0.4 cm²) on both Ge and GeSi substrates. Measurements were taken after cap etch but prior to AR coating on standard AM0 simulator.

Figure 6.7 shows both a dark and light I-V comparison between a GaAs/Ge solar cell and the “best” MBE grown GaAs/GeSi device to date prior to AR coating, area = 0.16 cm². A number of conclusions can be drawn from the GaAs/GeSi I-V data. First, there is a large shunt current present in the GaAs/GeSi device that is not seen for GaAs/Ge. Note that this was the best GaAs/GeSi solar cell measured and other devices contained significantly larger shunt currents with no uniformity over multiple sample growths and devices. Although these samples have not been AR coated, $V_{oc} = 949$ mV is comparable with (slightly higher than) the best GaAs/Si devices reported in the literature, an encouraging result since the current $V_{oc}$ value is clearly limited by the shunt current. Unfortunately, the shunt significantly reduces the FF to a value of 65.7%, and therefore limits the maximum efficiency of the GaAs/GeSi cells.
Figure 6.8: Light I-V curve reported for GaAs/Si single junction GaAs solar cell by Yamaguchi et. al. The 18.3% AM0 GaAs/Si efficiency is the highest reported for GaAs/Si prior to this work.

While $J_0$ (or $I_s$) increases for increasing TDD due to increased recombination in the depletion region, the magnitude of the shunt seen in these devices is much larger than expected and clearly inconsistent with the impact of threading dislocations. As shown in figure 6.8, these shunt effects are not seen by Yamaguchi et. al. for GaAs/Si devices containing a higher TDD, implying that the interface nucleation, the GeSi surface morphology, GeSi surface defects, GaAs epilayer cracking, or other factors must be influencing the device performance. Since the MBE grown GaAs/Ge devices do not demonstrate this large shunt current, figure 6.6, the origin of the shunt cannot be attributed to the GaAs/Ge nucleation procedure. I-V results comparable to homoepitaxial GaAs were also obtained for smaller area GaAs/GeSi diodes. The GeSi diodes contained epilayer cracks as well as the characteristic crosshatched surface morphology, suggesting that the concentration of surface defects characteristic of the current GeSi buffer (due to
processing environment), figure 4.4, is limiting the GaAs/GeSi large area device performance. In fact, a detailed EBIC analysis of the GaAs/GeSi solar cells indicates that one type of GeSi surface defect in particular appears to be responsible for the current GaAs/GeSi device performance. This defect is discussed in the following section.

6.5 Impact of GeSi surface defect on I-V characteristics

While there is a large density of surface defects on the GeSi graded buffers that could all contribute to the shunt current seen in the large area solar cells, figure 4.4, figure 6.9 shows a Nomarski optical microscope image of a characteristic surface defect believed to be most detrimental to the I-V characteristics. These defects, referred to here as “bat” defects due to their characteristic shape, are consistently oriented along the [110] direction with the “ears” in the direction of the 6° wafer offcut. While the exact origin of these defects is unknown (identification of the surfaces is ongoing), it is believed that

Figure 6.9: Nomarski optical microscope image of a pair of “bat” defects characteristic of the current GeSi graded buffers. The defects are ~20 x 20 μm² with a density of 20-500 cm⁻² depending on the GeSi substrate.
these defects either result from either poor surface preparation or a contaminant during UHVCVD growth. The non-cleanroom growth environment currently used in our collaborators laboratory is also a very likely source of particulate contamination. While the bat defect density have been measured as low as ~20 cm⁻², the density is uncontrolled from wafer-to-wafer with densities as high as ~1000 cm⁻², and higher densities near the wafer edge. The variation indicates a wafer dependence rather than a growth technique dependence, supporting wafer handling and process environment as a primary concern. It should be noted that while the CMP process after the initial GeSi grade is a "dirty" process requiring significant handling of the wafers prior to regrowth, defects similar to the final form of the bat defect exist prior to the CMP process and regrowth indicating that the CMP process is not responsible for the bat defect nucleation. Figure 6.10 shows an SEM and EBIC image of a bat defect in a solar cell device. The dark lines inside the bat in the EBIC image indicate regions of high recombination, implying that the defect is indeed electrically active and could account for the shunt current seen in the solar cell I-V data. Figure 6.11 shows a 3-D rendering of a bat defect generated from an AFM scan. The defect is approximately 20 x 20 μm². AFM line scans as well as cross-sectional SEM indicate a defect depth of greater than 2μm.

In order to better define the impact of the bat defect on the I-V characteristics of GaAs/GeSi devices, a series of diodes were fabricated and inspected via optical microscopy for the incorporation of a bat defect on the diode mesa. The diodes were then separated into three categories:
Figure 6.10: SEM (a) and EBIC (b) images of a bat defect on a GaAs/GeSi solar cell grown by MBE. The “black” highlight in the EBIC image indicates a region of high recombination in the center of the bat defect.
Figure 6.11: 3-D rendering of an AFM scan of a bat defect from a GaAs/GeSi solar cell grown by MBE. The defect size is ~20 x 20 μm² with a depth of ~1.88μm.

1) containing a bat defect on the diode mesa, 2) containing residual surface defects from the GeSi grade but NOT containing a bat defect, and 3) mesas free of any surface defects. Figures 6.12 and 6.13 show a series of I-V data taken and divided into these three categories for both 750x750 μm² (36 diodes) and 1000x1000 μm² (33 diodes), respectively. Both the linear and log I-V plots are included, with the current magnitude plotted in the log I-V case. From these plots, the magnitude of current in reverse-bias can easily be used to determine the impact of the surface defects and their contribution to the severe shunt current found for the large area devices. For diodes without bat defects, saturation currents (and reverse bias currents) comparable to homoepitaxial GaAs are obtained, similar to that reported in chapter 5. However, the diodes containing any surface defects demonstrated a considerable increase in leakage current (reverse bias), as
Figure 6.12: Linear and log I-V plots for 36 individual GaAs/GeSi diodes grown by MBE with area of 750 x 750 μm². The diodes were separated into 3 groups based on the surface morphology of the diode mesa: (a) no surface defect incorporation (22 diodes), (b) surface defects but no bat defects (8 diodes), and (c) one or more bat defects on the diode mesa (6 diodes).
Figure 6.13: Linear and log I-V plots for 36 individual GaAs/GeSi diodes grown by MBE with area of 1000 x 1000 μm². The diodes were separated into 3 groups based on the surface morphology of the diode mesa: (a) no surface defect incorporation (14 diodes), (b) surface defects but no bat defects (9 diodes), and (c) one or more bat defects on the diode mesa (10 diodes).
much as 5 orders of magnitude at −2V, indicating that the incorporation of heterogeneous defects in the GeSi graded buffers is responsible for the shunt observed for the large area devices. From the I-V data, regardless of the surface defect type, i.e. bat or non-bat, the leakage currents are large and non-uniform, similar to the I-V results obtained for the large area cells. Additionally, the leakage current for the samples containing bat defects is consistently higher than those samples without a bat defect, even if other surface defects are incorporated on the device mesa. While this data is not conclusive proof that the bat defects are primarily responsible for the shunt current seen on the large area devices, the fact that each solar cell with an area of only 0.16 cm$^2$ will contain a minimum of 10–15 bat defects makes these defects the likely source of the efficiency limiting shunt current characteristic of the large area devices grown via MBE. Unfortunately, since these defects are characteristic of the GeSi graded buffer for the current growth environment, MBE is an ineffective growth technique for characterizing the impact of TDD or thermal expansion mismatch on large area devices since the present device limitations are neither III-V growth, TDD, or thermal expansion mismatch related. That is, unless the bat defects can be electrically isolated from the rest of the cell mesa.

In order to conclusively relate the shunt current to the bat defect, the bat defects were isolated from a number of cell mesas via etching. On average, ~10 bat defects were “removed” from each device. A Nd:YAG laser was used to selectively open windows on a fully fabricated, photoresist coated GaAs/GeSi substrate. The bat defects were then isolated from the cell with a mesa etch around the defect itself. Unfortunately, although EBIC images verified that the bat defects were indeed isolated from the cell area, the
shunt current, while reduced, was not eliminated as expected with the isolation of the active bat defects, implying that either additional shunt paths were introduced during etching (likely) or that additional surface defects are also significantly contributing to the shunt current. Therefore, since, unlike other GaAs/Si growth techniques, the leakage current is not controlled by the TDD, device results can not be compared to theoretical data as desired, an unfortunate conclusion since all measures up to this point indicate GaAs material quality superior to that achieved by any other GaAs/Si integration techniques used to date.

Fortunately, collaborations with outside laboratories enabled the continuation of this research without waiting for the GeSi buffer optimization to eliminated bat defect nucleation.

6.6 Growth solution for large area GaAs/GeSi devices

Due to the depth and facets of the “pit” located at the center of the bat defect, the MBE growth technique, which is well-known to be directional and provide minimal coating of step sidewalls, does not appear to be well suited to provide a uniform coating of the diode structure across the defect morphology. Recall that the solar cell structure is ~3µm while the depth of the defect is ~2µm. In optical microscope images of a bat defect both before and after MBE growth, the defect morphology appears unaltered by the 3µm GaAs growth, implying a non-uniform GaAs coverage since a uniform growth rate along all surfaces would be expected to “smooth” the faceted defect morphology. Therefore,
Figure 6.14: Nomarski optical image comparing the bat defect morphology after (a) MBE growth and (b),(c) after MOCVD growth. The image following MBE grown is identical to that obtained prior to any epitaxial growth. Two different MOCVD reactors were used for GaAs/GeSi growth, (b) a “home-built” horizontal flow reactor and (c) a vertical flow production reactor.

the inability of the MBE growth technique to uniformly coat the GeSi surface could explain the shunt path provided at these defects.

Since MOCVD growth is well known to provide a more uniform deposition due to the growth mechanism differences from MBE, samples were grown via this technique in order to investigate the impact of a more uniform deposition on the electrical activity of the bat defects. Figure 6.14 provides a comparison of Nomarski images of the bat defect morphology before and after the MOCVD growth. As expected, the bat defect appears to be “filled” or “smoothed” by the MOCVD growth, implying a more uniform GaAs deposition. The electrical activity of the MOCVD coated bat is shown in figure 6.15. The EBIC analysis indicates that while recombination near the center of the bat defect has been minimized, recombination near the edges of the bat defect remain
Figure 6.15: SEM (a) and EBIC (b) images of a bat defect on a GaAs/GeSi solar cell grown by MOCVD in a horizontal reactor. The “black” highlight in the EBIC image indicates a region of high recombination in the bat defect. The region of recombination is substantially reduced compared to that shown in figure 6.10 for MBE growth.
Figure 6.16: Light I-V data for single junction GaAs solar cells grown by MOCVD (InGaP/GaAs) and MBE (AlGaAs/GaAs). The MOCVD grown cell area is 0.2x0.2 cm$^2$ while the MBE grown cell area is 0.4 x0.4 cm$^2$. Some of the increased shunt and reduced $V_{oc}$ can be attributed to the additional defects incorporated in the larger MBE device. However, MOCVD cells display minimal shunt independent of device area due to bat defect filling/passivation.

unaffected, suggesting that the MOCVD growth provides some, but not complete "passivation" of the bat defect. However, figure 6.16 shows light I-V curves for MBE and MOCVD grown GaAs/GeSi solar cells with an area of 0.16 cm$^2$. For the MBE grown sample $J_{sc} = 28.3$mA/cm$^2$, $V_{oc} = 851$ mV, FF = 62.5% and $\eta = 11.2\%$ while for the MOCVD grown sample $J_{sc} = 28.3$mA/cm$^2$, $V_{oc} = 1023$ mV, FF = 80.5% and $\eta = 17.1\%$.

The significant reduction in the shunt current for the MOCVD grown samples is uniform across the GeSi wafer and is attributed to the “coating” of the bat defects. In addition to a greater FF, the MOCVD sample also demonstrates a substantial increase in $V_{oc}$, as will be discussed later in the section. From these results, we conclude that while the MBE
growth technique is ineffective for the characterization of large area devices unless the incorporation of bat defects in the GeSi graded buffer can be eliminated, MOCVD growth provides a viable alternative for the realization of high efficiency GaAs/GeSi solar cells (and the continuation of this research) if material quality comparable to that demonstrated via MBE growth can be realized. Unfortunately, similar to the MBE research completed at OSU, controlling the GaAs/Ge interface during MOCVD growth is non-trivial as is evident by the considerable research attention it has received.[4,5,6,7] In order to avoid this complication, the initial stages of this work were exploited in order to produce “virtual GaAs” substrates on GeSi graded buffers via MBE (controlling both TDD and APB nucleation) for subsequent MOCVD growth. However, the addition of MOCVD growth and sample transfer to either Sandia National Labs (Albuquerque, NM) or NASA Glenn (Cleveland, OH) after the initial UHVCVD and MBE growths adds a level of complexity as well as the additional opportunity for particulates to contaminate the growth surface. For all MOCVD growth, the MBE grown GaAs buffer was only 1000Å since prior results have indicated this thickness to be sufficient to annihilate any APB’s nucleated at the GaAs/GeSi interface.

6.7 Characterization of MOCVD grown GaAs/GeSi solar cells

6.7.1 MOCVD growth parameters

Figure 6.17 shows a schematic of the solar cell structure grown via MOCVD. While the layer thicknesses are similar to the MBE grown cell, both the base doping and window/BSF material were modified. In₀.₄₈Ga₀.₅₂P instead of AlGaAs was used for the
window and BSF layers. While providing a slightly smaller window bandgap, due to a common oxygen contamination problem when growing AlGaAs via MOCVD, InGaP is commonly used in place of the AlGaAs layers in both the window and BSF layers. Also, the base doping was lowered to \( n \sim 2 \times 10^{16} \text{cm}^{-3} \) from \( n \sim 3 \times 10^{17} \text{cm}^{-3} \) based on previous results at Sandia growing single junction GaAs solar cells in this MOCVD reactor with \( V_{oc} \) value exceeding 1030mV. PC-1D modeling indicates that a lower \( V_{oc} \) should be expected based on this doping change and will be commented on in the following section.

The cell structure of figure 6.17 was grown on GaAs, Ge, and GeSi substrates and solar cell areas of 0.2 x 0.2 cm\(^2\) and 0.4 x 0.4 cm\(^2\) were fabricated. The small area cells were fabricated in order to provide a large number of GaAs/GeSi solar cells for comparison and "statistics" while also attempting to minimize the possible impact of epi-layer cracking due to thermal expansion mismatch on these initial MOCVD growth runs.

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**Figure 6.17**: Schematic of p-n InGaP/GaAs single-junction solar cell structure used in this research grown by MOCVD. (*) denotes layers grown during GaAs/Ge nucleation procedure by MBE on Ge and GeSi substrates. Nominal doping densities for all layers are listed to the right.
Figure 6.18: Light I-V comparison of InGaP/GaAs solar cells grown by MOCVD on GaAs/Ge, and GeSi substrates. Data for the GaAs and GeSi substrates is for 0.2 x 0.2 cm$^2$ cells (10.2% metal coverage) while data for the Ge substrate is for 0.4 x 0.4 cm$^2$ cells (7.8% metal coverage).

Additionally, fewer bat defects are incorporated for a smaller device area, possibly resulting in a cell without a single bat defect which could then be compared to determine the impact of the bat defect on cell performance.

6.7.2 Light I-V response of MOCVD grown GaAs/GeSi

Figure 6.18 shows light I-V data obtained for InGaP/GaAs single junction cells grown on all three substrates, GaAs, Ge, and GeSi. Several important conclusions are immediately evident from these curves. First, the homoepitaxial GaAs cell parameters, $V_{oc} = 1036$, $J_{sc} = 30.0$, FF= 86.7, and $\eta = 18.9\%$ are improved over those obtained for MBE growth, most notably $V_{oc}$ which was increased from ~985 mV to ~1035 mV. While the base doping was decreased for the MOCVD growth runs, the higher $V_{oc}$ achieved can be attributed to the lack of growth stops using MOCVD compared to MBE. Note that
while $J_{sc}$ is similar between the MBE and MOCVD grown samples, the FF has also been improved for MOCVD growth resulting in an increase in absolute efficiency, $\eta$, of $>1.5\%$.

Second, the efficiency parameters obtained for the GaAs/Ge cells, with the exception of $V_{oc}$, are considerably lower than those obtained for the GaAs/GaAs samples. Note that while $V_{oc}$ of 1060 mV was achieved for the GaAs/Ge cell of figure 6.18 the average $V_{oc}$ value was similar to the GaAs/GaAs samples. While some degradation is expected due to the increased residual TDD for GaAs/Ge ($\sim 10^{14}$ cm$^{-2}$), the 4% absolute reduction in FF is primarily attributed to the increased series resistance resulting from the MBE GaAs/Ge interface (the epitaxial uid p-Ge buffer and the buried carbon as discussed in chapter 5). This reduction is also expected to translate to the GaAs/GeSi due to the GaAs/Ge interface nucleation. Considering the reduction in $J_{sc}$, figure 6.19 shows a comparison between the EQE response of the GaAs/Ge and homoepitaxial GaAs samples. As shown, the reduction in current collection is due to a decrease in the “red” response of the GaAs/Ge cell. While this reduction could be attributed to a low minority carrier lifetime in the n-base of the GaAs/Ge cell growth, based on the TRPL measurements demonstrating minority carrier lifetimes comparable to homoepitaxial GaAs for GaAs/Ge MBE, this reduction is most likely attributed to the additional handling required when transferring substrates to Sandia National Labs (for cell growth) from OSU after initial GaAs/Ge buffer is deposited. This result would be consistent with an increased interface recombination velocity at the base/BSF interface, which could be
attributed to a somewhat thin 1000Å MOCVD GaAs buffer grown prior to the “active” solar cell structure after transfer from the MBE UHV growth chamber.

Finally, and most importantly, the GaAs/GeSi light I-V response does not contain the “large” shunt current typical of the previous MBE GaAs/GeSi growth results, section 6.4. This result is attributed to the “passivation” (filling) of the bat defects (as well as additional surface defects), demonstrating the success of the MOCVD growth approach in “circumventing” the limitations presented by bat defect incorporation to MBE grown devices. The MOCVD growth technique resulted in minimal shunt current for more than 80 devices across a 7 cm² GeSi sample, excellent uniformity compared to the device-to-device variations/non-uniformity encountered in the GaAs/GeSi MBE growth, figures 6.12 and 6.13. Moreover, since shunt current due to surface defect incorporation is no
Figure 6.20: Histogram of $V_{oc}$ data recorded for InGaP/GaAs single junction solar cells grown via MOCVD on (a) GaAs, (b) Ge, and (c) GeSi substrates. $V_{oc}$ values for GeSi were measured over 2 samples for 0.2 x 0.2 cm$^2$ area cells.
longer limiting GaAs/GeSi device performance, it is now possible to investigate the impact of TDD on solar cell performance and compare with theoretical results, an investigation not possible for MBE GaAs/GeSi device growth while shunt currents limited \( V_{oc} \), FF, and \( \eta \). Figure 6.20(c) shows a histogram of the \( V_{oc} \) values obtained for MOCVD growth of 80 GaAs/GeSi single junction solar cells. (Note that all the \( V_{oc} \) values are “world records” for single junction GaAs AM0 cells on Si via any prior approach to mismatch heteroepitaxial integration. The average \( V_{oc} \) value, \( \sim 1010 \) mV, represents a >7% increase over the highest GaAs/Si \( V_{oc} \) reported previously, \( \sim 940 \) mV (<900 mV typical), with the highest \( V_{oc} \) value of 1048 mV representing a 12% increase in \( V_{oc} \), or \( \sim 1\)-2% (absolute) increase in \( \eta \) from:

\[
\eta = \frac{J_{sc} \times V_{oc} \times FF}{P_{in}} \tag{6.3}
\]

Note that, in agreement with GaAs/Ge and GaAs/GeSi SIMS diffusion data, section 4.1.3, EQE data for the GaAs/GeSi and GaAs/Ge cells do not indicate an active Ge p-n junction below the GaAs solar cell which could be contributing to the higher \( V_{oc} \) value.

As previously stated, it is more difficult to achieve GaAs/Si \( V_{oc} \) values comparable to homoeptaxial GaAs than \( J_{sc} \) values due to the residual threading dislocation density (and additional recombination paths increasing the saturation current), as evident by the lower \( V_{oc} \) values previously obtained for GaAs/Si (<900 mV for GaAs/Si and >1030 mV typical for GaAs/GaAs). These results confirm that the GaAs/Si device integration via a GeSi graded buffer, which has demonstrated superior TDD and minority carrier lifetime versus previous GaAs/Si integration techniques, is in fact only limited by the residual threading
Figure 6.21: Theoretical plot of $V_{oc}$ versus TDD based on equation 6.1 assuming $J_0$ is dominated by recombination in the depletion region due to TDD, equation 6.2. Data points for other GaAs/Si reports are included along with the results from this work for comparison.\(^{[1,2,10]}\)

dislocation density which has been successfully reduced below $1 \times 10^6$ cm\(^{-2}\) and maintained throughout GaAs integration. Figure 6.20 demonstrates that the $V_{oc}$ values obtained for the GaAs/GeSi MOCVD growth are comparable to those obtained on both the GaAs and Ge substrates, with the lower average $V_{oc}$ consistent with the theoretical reduction in $V_{oc}$ for a TDD of $\sim 1 \times 10^6$ cm\(^{-2}\). Note that the lowest $V_{oc}$ recorded for these GaAs/GeSi solar cells, $\sim 965$ mV, is still higher than the greatest GaAs/Si $V_{oc}$ reported for any other epitaxial integration technique.

Figure 6.21 shows the theoretical dependence of $V_{oc}$ based on equation 6.1, assuming $J_0$ is dominated by recombination in the depletion region as defined by equation 6.2 and $L_p$ is TDD limited per equation 3.14. (For the doping levels chosen, $W_{dp} \sim 0.14$ $\mu$m, $D_p = 6.5$ cm\(^2\)/s, and $n_i = 1.8 \times 10^6$ cm\(^{-3}\) $J_{sc} \approx 32-33$ mA/cm\(^2\) for a SJ GaAs solar cell.)

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Included for comparison are $V_{oc}$ values from other reported GaAs/Si integration techniques.$^{[2,8,9,10,11]}$ Note that these values are consistently lower than predicted by theory implying recombination due to threading dislocation incorporation not accounted for in the depletion region approximation, equation 6.2.$^{[12]}$ However, while $V_{oc}$ values from other GaAs/Si integration methods have been limited to $\sim 900$ mV (typical), $V_{oc}$ values for MOCVD grown GaAs/GeSi agree well with theory, again confirming the "true" GaAs/Si threading dislocation density of $<1 \times 10^6$ cm$^{-2}$ via the GeSi graded buffer and demonstrating that the crosshatch surface morphology does not limit device performance. These results imply that the GaAs/GeSi material quality demonstrated in chapter 4, a direct result of the ability of the GeSi graded buffer to reduce residual threading dislocation densities below $\sim 1 \times 10^6$ cm$^{-2}$ and inhibit APB penetration, is indeed translating into device quality for the GaAs/GeSi single junction cells and should successfully enable record efficiency GaAs/Si single junction solar cells.

However, as shown in figure 6.18, while $V_{oc}$ values are comparable to theory, the GaAs/GeSi efficiency has been limited to $\eta=17\%$ and does not exceed the bests GaAs/Si cells achieved to date of $\sim 18.3\%$ as predicted based on the material quality achieved. From equation 6.3, only reductions in FF and $J_{sc}$ can be responsible for this inconsistency. For the GaAs/GeSi samples, $FF_{GeSi} = 78-80\%$. As indicated for GaAs/Ge ($FF_{Ge}=82\%$), values are lower than homoepitaxial GaAs ($FF_{GaAs}=85-87\%$) due to the increased series resistance introduced by the GaAs/Ge interface nucleation, chapter 5. The additional difference between $FF_{GaAs/GeSi}$ and $FF_{GaAs/Ge}$ can be attributed to the increased TDD, consistent with theory, figure 6.5. While it appears that higher $FF_{GeSi}$ values are
attainable for improved GaAs/Ge interface control, values are comparable to other reports for GaAs/Si and do not account for the efficiency reduction.\cite{11} Therefore, it is concluded that only $J_{sc}$ is currently limiting the GaAs/GeSi maximum efficiency, an interesting point since it has been determined that $V_{oc}$ values are harder to optimize than $J_{sc}$ values for the GaAs/Si system. These results imply that the GaAs/GeSi material quality is not the limiting factor in determining $J_{sc}$ for the current growth approach. Therefore, an investigation into $J_{sc}$ is now warranted.

6.7.3 EQE comparison of GaAs/GeSi for determining $J_{sc}$ limitation

$J_{sc} = 28.3 \text{mA/cm}^2$ for the GaAs/GeSi MOCVD devices ($J_{sc}^{\text{GeSi}}$) fabricated during this research while $J_{sc} = 33.2 \text{mA/cm}^2$ was reported for the $\eta=18.3\%$ GaAs/Si solar cell by Yamaguchi et. al.\cite{11} Due to the small area cells grown during this research, the cells contain $\sim 10.2\%$ metal coverage instead of the $\sim 4-5\%$ metal coverage typical of a larger area cell design. Since there is no absorption under the metal layer, the $5\%$ increase in metal coverage area translates directly into a $5\%$ reduction in $J_{sc}$. Approximating $J_{sc}^{\text{GeSi}}$ for a $5\%$ metal coverage solar cell grid design results in $J_{sc}^{\text{GeSi}} = 30.0 \text{mA/cm}^2$, a value still lower than that reported for GaAs/Si. However, $J_{sc}^{\text{GaAs}} = 31.5 \text{mA/cm}^2$ (adjusted for $5\%$ metal coverage) is also significantly lower than the $33.2 \text{mA/cm}^2$ reported for GaAs/Si, indicating a limitation to $J_{sc}$ which is not material quality related but dependent on the fabrication process (i.e. ARC) and/or cell design. In order to provide insight into the factors limiting $J_{sc}$, a series of EQE spectra are investigated.
Figure 6.22: External quantum efficiency measurements for single junction solar cells grown by MOCVD (InGaP/GaAs) and MBE (AlGaAs/GaAs).

Figure 6.22 plots two single-junction homoepitaxial GaAs samples, one grown via MOCVD and one grown via MBE. For the MBE grown AlGaAs/GaAs sample, \( J_{sc} = 31.0 \) mA/cm\(^2\) (adjusted to 5\% metal coverage). The lost "blue" response for the MOCVD sample is significant in terms of \( J_{sc} \) since the AM0 spectrum contains a high flux in this region, figure 3.3, and can be directly correlated to the loss in \( J_{sc} \). Due to the excellent red response of the MOCVD grown cell, near 1.0, the reason for the loss in the "blue" response can not be related to the emitter (i.e. low \( L_n \) due to heavy doping or high interface recombination velocity) since a problem with collection in the emitter would effect both the red and blue responses since both are absorbed in the emitter region. Also, although the window layers are different, \( \text{Al}_{0.85}\text{Ga}_{0.15}\text{As} \) and \( \text{In}_{0.48}\text{Ga}_{0.52}\text{P} \), the minimal difference in bandgap does not account for the severe blue loss for the \( \text{In}_{0.48}\text{Ga}_{0.52}\text{P} \) window. Therefore, we conclude that the reduction is due to factors external to the cell.
design and material quality. In this case, we find that the anti-reflection coating (ARC) is lowering the “blue” response of the \( \text{In}_{0.48}\text{Ga}_{0.52}\text{P/GaAs} \) cell design. Since the ARC is designed/matched to the refractive index of an \( \text{Al}_{0.8}\text{Ga}_{0.2}\text{As} \) window, the use of the same ARC for the \( \text{In}_{0.48}\text{Ga}_{0.52}\text{P} \) window design, although originally thought to be similar to \( \text{AlGaAs} \), results in a higher reflectance due to “poor” index matching. This assumption is supported by visual inspection of the cells after ARC where the \( \text{AlGaAs/GaAs} \) cells appear “black” while the \( \text{InGaP/GaAs} \) cells appear “bluish”, implying the reflection of high energy photons which are not collected as seen in the EQE response of figure 6.22. Further reflection measurements performed on the AR coated \( \text{InGaP/GaAs} \) cell structure would verify these conclusions. Currently, the design of an ARC better suited for the \( \text{InGaP/GaAs} \) structure is being investigated.

Figure 6.23 shows EQE data obtained for MOCVD growth on \( \text{GaAs}, \text{Ge}, \) and \( \text{GeSi} \) substrates. Similar to the \( \text{GaAs/Ge} \) sample, the \( \text{GaAs/GeSi} \) shows a reduction in the “red” response compared to homoepitaxial \( \text{GaAs} \) due to the MBE/MOCVD growth procedure as previously discussed while the blue response across all three substrates is nearly identical. Similar to the light I-V data, EQE indicates that the \( \text{GeSi} \) substrate is behaving as an “ideal” \( \text{Ge} \) interface and that \( L_p \) is not limiting the photon collection in the n-base region. \( J_{sc}^{\text{GeSi}} \) is only \( \sim 1.5 \text{ mA/cm}^2 \) lower than \( J_{sc}^{\text{GaAs}} \) due to the reduced red response and should increase identically to the homoepitaxial \( \text{GaAs} \) with a correction in the ARC currently limiting the collection of high energy photons. Considering these facts, \( J_{sc} \) values near homoepitaxial \( \text{GaAs} \) quality should be achievable for the \( \text{GaAs/GeSi} \) material quality demonstrated during this dissertation. Conservatively, \( J_{sc} \) values of 32
mA/cm² should be easily obtained for large area cells (~5% metal coverage) once a suitable InGaP/GaAs ARC is designed. From equation 6.3, assuming similar FF and \( V_{oc} \) values are also maintained and not improved upon, (FF = 80% and \( V_{oc} = 1020 \) mV), \( \eta = 19.3\% \) should be realized via GaAs/GeSi integration. Assuming \( J_{sc} = 33.2 \) mA/cm² as reported by Yamaguchi et. al. is achieved, \( \eta > 20\% \) is possible. Additionally, while initial MOCVD cell results have been limited to small area designs, 0.04 cm², due to concerns over bat defect incorporation as well as thermal expansion mismatch, the minimal shunt current indicates that the bat defect does not impact device performance for MOCVD growth. Moreover, figure 6.24 shows an MOCVD grown GaAs/GeSi cell which contains multiple (4) cracks due to thermal expansion mismatch with a spacing of ~500 μm. The crack incorporation was similar across the GeSi sample and showed no signs of reducing \( V_{oc}, \text{FF}, J_{sc}, \) or \( \eta \). While one can not conclusively determine from this
result that the thermal expansion mismatch will not have a larger impact on larger area devices, these results are promising for the realization of large area, > 1cm², GaAs/Si solar cells through the application of a GeSi graded buffer with record efficiencies. However, while not considered in this dissertation, a detailed investigation of thermal expansion mismatch for the GaAs/GeSi system warrants investigation and should be considered as a future extension of this work in conjunction with the investigation of large area cells as well as multi-junction cell designs.

6.8 Additional EQE results and comments

In addition to the reduced blue response of the MOCVD InGaP/GaAs solar cell discussed in the previous section, figure 6.22, the MBE AlGaAs/GaAs design demonstrates a substantial reduction in red response compared to the InGaP design. The strong blue response indicates that this reduction can be attributed to the base/BSF and not the window/emitter region. Figure 6.25 provides more insight into the reduced red
Figure 6.25: External quantum efficiency measurements for single junction AlGaAs/GaAs solar cells grown by MBE on GaAs substrates. One cell contained a 2.0 \( \mu \)m base layer with a 10% AlGaAs BSF layer while the other contained a thinner, 1.5 \( \mu \)m, base with a super-lattice BSF containing 30% AlGaAs barriers.

collection, comparing the EQE for GaAs/GaAs cells with varying base thickness, 1.5\( \mu \)m and 2.0 \( \mu \)m. The EQE response for the two homoepitaxial GaAs cells grown by MBE shows identical collection for both structures. Since the diffusion length in the n-GaAs base is on the order of 3.5 \( \mu \)m (GaAs/GaAs growth), the additional base thickness, which enables more absorption, should enable greater collection. In fact, multiple MOCVD InGaP/GaAs cells with various base thicknesses demonstrated increase \( J_{sc} \) as the base thickness was increased to 3.0 \( \mu \)m. Assuming \( L_p \) for the MBE grown cells is comparable to that attained via MOCVD, figure 6.25 indicates that the MBE BSF layer (10% AlGaAs) is not aiding in the collection of the red spectrum. In fact, upon further consideration, due to the heavy doping in the Al\(_{0.1}\)Ga\(_{0.9}\)As, it is evident that the
Al$_{0.1}$Ga$_{0.9}$As BSF layer does not provide the valence band offset necessary for the back surface electric field and was in fact a poor choice during the initial cell design. A higher Al content would provide a more effective BSF layer and should be utilized during future MBE growths. In order to maintain a low interface recombination velocity (and low lattice mismatch) in addition to increasing the valence band offset, Al$_{0.3}$Ga$_{0.7}$As is recommended.

### 6.9 References


7.1 Conclusions

The course of this research has successfully demonstrated the GeSi graded buffer to be a viable integration technique for achieving high GaAs/Si material quality, as well as high efficiency solar cells. Successful GaAs/GeSi interface control by MBE, i.e. elimination of APB formation, TD nucleation, and interface cross diffusion, similar to that previously obtained on Ge wafers has been achieved, concluding that the Ge cap of the GeSi graded buffer is behaving as an “ideal” Ge interface even with the incorporation of surface crosshatch morphology and residual TD’s characteristic of the GeSi graded buffer. Unlike previous integration approaches which have exclusively relied on dislocation engineering and strain management within the III-V layers themselves, i.e. strained-layer superlattice, thermal cycle annealing, and selective area epitaxy, the graded GeSi buffer technique has successfully reduced TDD’s below $1-2 \times 10^6 \text{ cm}^{-2}$ while minimizing dislocation pile-ups by accommodating the lattice mismatch within group IV buffers prior to III-V nucleation. The TDD reduction and subsequent control of the Ge
interface during MBE growth has resulted in the highest GaAs material quality to date on a Si-based substrate. The >10 ns minority carrier lifetime, which approaches that of homoepitaxial GaAs and exceeds the best GaAs/Si minority carrier lifetime reported prior to this research by more than 300%, agrees well with the theoretical dependence of $\tau_p$ on TDD previously presented by Yamaguchi et al.\textsuperscript{[1,2]} and indicates that additional reductions in TDD as the graded GeSi buffer is optimized will result in lifetimes comparable to homoepitaxial GaAs. This result is significant when considering that neither GaAs/Si TDD's nor minority carrier lifetimes have seen significant improvement for more than a decade, implying a limitation to the previous integration approaches which has finally been mitigated by the group IV grading methodology.

In addition, this research has demonstrated the successful extension of the GaAs/Si material quality to GaAs/GeSi device quality. Again consistent with theory for a reduction in TDD, GaAs/GeSi solar cells have demonstrated $V_{oc}$ values of 1046 mV, comparable to homoepitaxial GaAs and exceeding the previous best $V_{oc}$ achieved on GaAs/Si of 940 mV by more than 11%. From a device perspective the significance of this result is clear since the increase in $V_{oc}$ translates directly into increased efficiency from:

$$\eta = \frac{J_{sc} \times V_{oc} \times FF}{P_{in}}$$ (7.1)

For this work, while material quality and $V_{oc}$ have been demonstrated to exceed previous "records" for GaAs/Si, due to both current device design and processing limitations
independent of the GaAs/GeSi material quality (i.e. ARC) (primarily limiting the maximum achieved $J_{sc}$) absolute efficiencies of 19.2% (or higher) have yet to be achieved. In spite of this, all measures of material quality consistently indicate that the GaAs/GeSi integration technique will enable high efficiency GaAs/Si solar cells which have previously been unrealized due to TDD limitations. In fact, accounting for both current metal coverage and ARC mismatches which have limited the device efficiency in this research (and should be noted can be easily corrected and is currently under development), GaAs/Si efficiencies in excess of 20% are imminent, making GaAs/Si integration, which has been of great interest for many years, a viable option for application to space solar photovoltaics (PV). Additionally, while space PV is the only application considered in this research, the material and device results represent a much larger impact for GaAs/Si integration. Since the photovoltaic cell provides the strictest test of material quality, the successful display of large area minority carrier devices demonstrates the applicability of the GeSi graded buffer to GaAs/Si integration for other devices applications. In particular, both optical and electronic devices as well as the integration of these devices with Si electronics for system-on-a-chip applications, which have been previously unrealized due to TDD limitations, can now be successfully realized through integration with a GeSi graded buffer. In fact, the future directions of this research project should include the application of the GeSi graded buffer system to various optical devices as well as continued PV applications. The following section details considerations for future work on the GaAs/GeSi integration project at OSU.
7.2 Future directions

1.) Since current results indicate that MBE cannot be effectively applied for GaAs/GeSi integration for large area devices on the GeSi buffers until the surface contamination issues of our collaborators are eliminated, it is necessary to investigate and characterize the direct growth of GaAs/GeSi via MOCVD in order to eliminate the need for GaAs/GeSi initiation via MBE to address GaAs/Ge interface control. Since current MBE results imply that the GeSi buffer behaves as an ideal Ge surface for subsequent III-V initiation, MOCVD techniques proven to eliminate APB formation on Ge substrates should be readily applicable for the GeSi substrate. Unfortunately, since reports of APB-free GaAs/Ge are contradictory and appear to vary substantially from system-to-system,\textsuperscript{[3,4,5,6]} GaAs/Ge growth techniques should be optimized for Ge wafers prior to application to GaAs/GeSi growth. Although the desire to switch exclusively to MOCVD growth is driven in this case by current defect limitations, from an industry standpoint MOCVD is more desirable due to higher growth rates and throughput, making it necessary to demonstrate that the GaAs/GeSi integration is compatible with this growth technique.

2.) Although not considered in this work, the impact of the GaAs:Si thermal expansion mismatch warrants immediate investigation. In order to minimize epi-layer cracking, layer thicknesses were limited to less than 3.5μm in this research based on previous GaAs/Si reports of a “crack threshold”. However, both MBE and MOCVD growth still resulted in crack spacings near 500 μm. In order to minimize strain in the
GaAs layer, strain balance techniques similar to that used to generate a “strain-free” Ge capping layer on the GeSi graded buffer may also be applicable. By engineering the GeSi buffer to be under tensile strain at room temperature (instead of “strain-free”), the additional compressive strain generated during GaAs growth could possibly be exploited to produce a “strain-free” GaAs epi-layer and eliminate epi-layer cracking (as well as wafer bow) due to the tensile strain encountered upon cooling due to the thermal expansion mismatch. At the very least, a determination of a “crack-threshold” for GeSi graded buffer system should be researched.

3.) While single-junction GaAs/GeSi cells have been successfully demonstrated and are convenient for device and material characterization, industrial applications require multiple junction cells for increased efficiency, typically double or triple junction. The design, growth, fabrication, and characterization of high efficiency multi-junction GaAs/GeSi cells would demonstrate that the GaAs/Si integration technique could successfully compete with the current GaAs/Ge cell design in space PV applications from an efficiency perspective while providing the added benefits of a Si-based substrate. Also, although the additional junctions will only increases the total layer thickness by less than 5000Å, due to the thermal expansion mismatch the impact of the additional layer thickness must be considered as stated in 2.

4.) Considering multi-junction cell design, the GeSi graded buffer provides a unique opportunity for the integration of an epitaxial low-bandgap solar cell for either a
triple-junction or dual-junction optimal cell design. While a diffused Ge p-n junction is exploited in some cases to provide a third (bottom) cell, the inability to control the As diffusion creating the p-n Ge junction produces inconsistent device performance and has led some manufacturers to maintain a dual-junction design. The ability to epitaxially produce a cell in the GeSi graded layer provides not only improved reliability, but it also enables the growth of a cell with variable bandgap by not grading to 100% Ge (i.e. Ge₁₋₀.₉₄ Si₀.₀₆), providing a unique opportunity to "ideally" match bandgap pairs for an optimum multi-junction cell design. (Note that these designs will not necessarily include GaAs cells.) While the nucleation of III-V epi-layers on a GeₓSi₁₋ₓ “substrate” would require optimization similar to that performed for the III-V/Ge interface nucleation, the GeSi graded buffer provides the opportunity for a variable lattice constant and low threading dislocation density simultaneously on a Si-based substrate, making it advantageous for the same reasons as GaAs/Si integration.

5.) As discussed in chapter 5, the current MBE nucleation method results in a series resistance in the diode I-V characteristics which is attributed to the GaAs/Ge interface. While the complete source of this resistance is currently unknown, (as discussed in chapter 5 the effect is partially attributed to the p-type Ge epiaxy as well as other factors) the ability to successfully integrate an epitaxial Ge p-n junction for a multi-junction cell design requires the elimination of this effect. Since research reports for MOCVD initiation on Ge wafers indicate that this particular effect is specific to the current MBE initiation technique, elimination of the MBE nucleation in favor of a more
desirable single-MOCVD initiation/growth procedure would mitigate the series resistance problem if proper control of the GaAs/Ge interface could be obtained. However, in order to retain MBE as a viable integration option, which is desirable since MBE provides in-situ surface/interface characterization capability unavailable with MOCVD growth, a more detailed investigation into the source of resistance for the GaAs/Ge interface nucleation is warranted.

First, since the uid-Ge epilayer has been determined to be heavily p-type, a method for achieving n-type Ge should be investigated since the Ge epilayer cannot be eliminated due to its importance in controlling the interface nucleation “structurally”. However, since the current system set-up results in extensive impurity incorporation due to the thermal heating of the chamber walls near the Ge source and would likely not be improved with new Ge source material or a new effusion cell, achieving an n-type Ge epilayer may not be possible with the current system configuration. Second, since one possible source of the series resistance is contamination of the growth surface, particularly carbon, the addition of a hydrogen cleaning source on the MBE to provide in-situ cleaning of the Ge surface could be investigated. One simple solution, if the p-type Ge epi-layer is in fact the main resistance source, would be to initiate on p-type rather than n-type substrates, favoring a n-p rather than a p-n cell design. Currently, p-type GeSi substrates are being processed to investigate this possibility.

Finally, since the Ge epilayer is heavily p-type, it should be possible to create a Ge “bottom cell” for a multi-junction cell design. While the current growth structure does not result in an active Ge p/n junction, the device structure is similar to that achieved
during MOCVD growth, which provides an active Ge junction through diffusion. Note that in order to provide current generation from both the top and bottom cells the multi-junction cell design requires a tunnel junction between the top and bottom cells. For the MOCVD case, this tunnel junction is formed due to high diffusion of both Ge and Ga providing n+ and p+ layers in the GaAs and Ge respectively. In this work, the minimization of Ge diffusion into the GaAs layer is likely responsible for “not providing” the necessary tunneling effect. However, through heavy doping of the n-GaAs buffer layer or growth of a p+/n+ GaAs tunnel junction near the GaAs/Ge interface the epitaxial p-Ge may be exploitable to provide an epitaxial Ge bottom cell. Note that this is unique for the GaAs/GeSi system since GaAs/Si epitaxy does not have a Ge layer to enable such a multi-junction design.

6.) In addition to device applications, many opportunities exist within the III-V growth to further reduce threading dislocations below the current \( \sim 1 \times 10^6 \text{ cm}^{-2} \) range which has been achieved through the GeSi graded buffer. Methods which have been exploited to minimize TDD for “direct” GaAs/Si epitaxy, such as thermal cycle annealing\(^7\) and strained layer superlattice buffers\(^8\) should still be applicable to the GaAs/GeSi system in order to further reduce TDD. Although TDD’s \(< 2 \times 10^6 \text{ cm}^{-2} \) have not been successfully demonstrated by any combination of these techniques to date, data indicates that the ability to apply increased numbers of thermal cycles (and hence increased buffer thickness) will continue to reduce GaAs/Si thread density. Unfortunately, due to the added concern with thermal expansion mismatch, buffer layers
of infinite thickness cannot be used for continued TDD reduction. For the GeSi substrate, layer thicknesses comparable to those used for current GaAs/Si epitaxy (including TDD reducing buffers) can be implemented, treating the GeSi buffer similar to the Si substrate, and should result in a lower thread density since the residual GeSi TDD is already \( \sim 1 \times 10^6 \) cm\(^{-2}\). Additionally, dislocations over a limited growth range may be reduced through the technique of selective area epitaxy (SAE). SAE involves growth over limited areas, of order a few tens of \( \mu \text{m}^2 \) to perhaps as large as 1-2 mm\(^2\). The growth areas can be defined by simple wet chemical etching of mesas in the Ge/Si\(_x\)Ge\(_{1-x}\) buffer, or by deposition of a dielectric masking grid. The SAE approach can help reduce the threading density via two mechanisms: 1) the reduced growth area will minimize dislocation-dislocation interactions and dislocation multiplication and 2) SAE greatly increases the probability that existing dislocation threads will glide to the edges of the growth area, by reducing the total distance across which a thread must glide in order to reach the edge of the growth area. While reduced TDD will have minimal impact on applications to PV as primarily considered in this research, through further reductions in TDD, small area applications such as laser diodes can be considered, where these devices are impractical due to short device lifetimes (caused by dark line defects) at current thread densities. The demonstration of a reliable III-V laser on Si would make the III-V/GeSi/Si system a possible solution for system-on-a-chip applications, one of the major driving forces behind integration technology.
7.3 References


HISTORY AND BACKGROUND OF GeSi GRADED BUFFER DEVELOPMENT

The following background and discussion of the GeSi graded buffer technique for threading dislocation control was graciously provided by M.T. Currie and E.A. Fitzgerald from Massachusetts Institute of Technology (MIT). MIT has been a longtime collaborator with OSU and is the “supplier” of the GeSi graded buffers used in this research and is currently the only group pursuing GeSi as an integration technique for GaAs/Si. This discussion includes a brief history of the development of the GeSi graded buffer which has occurred at Bell Labs and MIT over the past decade.

A.1 GeSi graded buffer development at MIT

The most successful and proven technique for the production of highly mismatched semiconductor epilayers with low threading dislocation densities is the relaxed graded buffer. First employed in the SiGe materials system by Fitzgerald, et al. in 1991, the relaxed graded buffer operates on a straightforward premise: maintain a low strain state to prevent rampant dislocation nucleation while maintaining a high growth temperature to maximize dislocation glide. Thus, the highly mismatched target...
layer is approached gradually via the deposition of many layers of low lattice mismatch. Each layer in the buffer relaxes to its intermediate lattice constant, and a low strain state is maintained throughout, minimizing dislocation nucleation. Additionally, threading dislocations from previous layers are "reused" at each subsequent interface as they glide to create misfit dislocations. A high growth temperature is utilized to maximize the glide length of each threading dislocation at each interface, eliminating the need for additional dislocations for strain relief. In the ideal case, the threading dislocations created during the very first layer of the graded buffer can be reused to relax every layer up to the desired final composition. This results in a steady-state threading dislocation density independent of the final Ge concentration of the SiGe graded buffer.

In practice, maintaining a steady-state threading dislocation density becomes difficult when grading to highly mismatched layers with high Ge contents, as will be discussed later in this section. The relaxed graded buffer technique has been successfully used to control threading dislocation densities in the SiGe/Si, InGaAs/GaAs, and the InGaP/GaP materials systems.\textsuperscript{[2,3,4]} Often, a successfully produced graded buffer acts as a template for heteroepitaxial growth not possible with the more conventional Si, GaAs, or InP substrates. This application of a relaxed graded buffer provides the motivation for its alternate moniker—the virtual substrate. Virtual substrates have been used to integrate dissimilar materials and create novel electronic and optoelectronic devices previously impossible to fabricate.

In the absence of excess dislocation nucleation, a steady-state threading dislocation density can be predicted for our SiGe virtual substrates. Thus, regardless of
the final Ge content, approximately constant threading dislocation densities in SiGe virtual substrates should be observed. In reality, very different behavior is observed in SiGe graded buffers grown to various Ge contents. There is a clear increase in threading dislocation density as the final Ge content of the buffer increases, counter to theoretical models. Clearly, some mechanism is activated when grading to high Ge contents that causes the nucleation of excess threading dislocations. During the relaxation of SiGe graded buffers, misfit dislocations form an orthogonal pattern along the in-plane \(<110>\) directions. The strain fields of these misfit dislocations affect the local growth rate of the film, resulting in the characteristic “crosshatched” surface morphology of SiGe virtual substrates. The rms surface roughness of SiGe virtual substrates also tends to increase with the final Ge content. This trend mirrors the observed increase in threading dislocation density. In fact, it has been shown that the two phenomena are linked—the increase in one results in the increase of the other. The mechanism for these trends is the threading dislocation pileup.

The recognition and control of threading dislocation pileups has formed the basis for much of the MIT SiGe virtual substrate materials quality improvement effort. The earliest efforts at grading to 100% Ge, dating back to research by E.A. Fitzgerald et. al. at AT&T Bell Lab, involved growths performed at temperatures of 800°C and pressures of 50 mT.\[1\] The samples were graded at 10% Ge/μm, and this resulted in threading dislocation densities of 1-5 x 10^7 cm^-2. The dislocation nucleation rate is controlled by the strain rate applied in the graded buffer, and this strain rate corresponds directly to the grading rate. In recognition of this fact, the first 100% Ge graded buffer effort at MIT
involved a decrease in grading rate by a factor of two. Although this 5% Ge/μm grading rate results in the deposition of twice as much material, the hope was that the threading dislocation density would decrease. The growth was performed at 750°C and 25 mT, and graded at 5% Ge/μm. Unfortunately, the threading dislocation density did not decrease, and the increased thickness of SiGe material presented a whole host of new problems. Cracks formed in the thick buffer due to thermal mismatch strain between Si and Ge. The sample also suffered from a very large particulate density due to gas phase nucleation of GeH₄ during the deposition of high Ge content layers at the high temperature and high pressure. Thus, the realization was made that grading rates of at least 10% Ge/μm were necessary to prevent cracking, and that lower temperatures and pressures needed to be utilized during the final stages of growth to prevent gas phase nucleation.

In parallel to these efforts of 100% Ge virtual substrate materials improvement, a greater understanding of the threading dislocation pileup phenomenon had been achieved. The formation of these pileups had been attributed to a cooperative interaction between the strain fields of underlying misfit dislocations and the surface roughness of the growing buffer. Much work had already been done demonstrating that growth of these buffers on offcut substrates resulted in lower threading dislocation densities, pileup densities, and surface roughness. However, as can be seen from the above efforts, growth on the offcut substrates was not enough to produce 100% Ge on Si with threading dislocation densities below 10⁷ cm⁻². In an effort to decrease the surface roughness of the graded buffer during growth, the concept of the intermediate planarization step was
formulated. The graded buffer growth would be halted at 50% Ge, the wafers would be planarized via chemical mechanical polishing (CMP), and the growth would resume on the newly flattened wafers. The effects would be two-fold: the decreased surface roughness would inhibit the formation of new threading dislocation pileups, and the planarization process would free dislocations already trapped in pileups.

The combination of the intermediate planarization step with the 10% Ge/μm grading rate and the decreased growth temperatures and pressures at high Ge contents resulted in the first really successful growth to 100% Ge. The initial grade to 50% Ge was performed at 750°C and 25 mT, and capped by 3 μm of 50% SiGe. After the CMP process, the grade was resumed at the same temperature and pressure until the 76% Ge point. At this point, the growth temperature was reduced to 550°C, and the pressure was reduced to 3 mT.

The growth continued to 92% Ge, whereupon a large jump in Ge concentration to 100% Ge was made. This strategically-placed jump was designed to incorporate compressive mismatch strain into the graded buffer at the growth temperature. This compressive strain balanced out the tensile strain due to thermal mismatch that resulted during cooling to room temperature, resulting in a crack-free Ge surface. The decreased temperature and pressure of the final part of the growth also resulted in a much lower particle density on the wafer surface. The final threading dislocation density of this sample was approximately $2 \times 10^6$ cm$^{-2}$, even lower than it had been at the 50% Ge point where the wafers were planarized. Thus, threading dislocations that had been already trapped in pileups at the 50% Ge point were freed by the CMP process. This excess dislocation
density, made glissile by planarization, experienced dislocation annihilation events that led to a decrease in overall threading dislocation density by the 100% Ge point.\cite{5}

Subsequent materials quality improvement efforts for the 100% Ge graded buffers have concentrated on reductions in particle density and threading dislocation density. Most of the changes have been made in the handling of the wafers and in the growth schedule of the reactor. The CMP process continues to be performed at the 50% SiGe point. The growth temperature of the growth to 50% SiGe has been increased recently to 900\textdegree{}C, and the threading dislocation density at the 50% point has decreased appreciably. However, the particle density on the wafers, while vastly decreased from the levels of the earliest growths, continues to be very high for solar cell applications. Growth temperatures of both 750\textdegree{}C and 650\textdegree{}C have been utilized during the 50-76% portion of the growth.

While the lower growth temperature should inhibit any gas phase nucleation during that part of the growth, it also slows dislocation glide. Thus, temperatures as high as possible continue to be utilized for the growths to keep the dislocation density low. At this point, the main sources of particles on the wafers are SiGe particles from the wall of the UHVCVD reactor raining down during growth and particles from the air that the wafers are exposed to between CMP and regrowth. In order to minimize the particulate problem in the reactor, these growths to 50% SiGe and regrowths to 100% Ge are performed very soon after a reactor tube change. Thus, very little SiGe thickness has accumulated on the reactor wall, and less particulate contamination will occur during growth. Secondly, a laminar air hood has been installed above the load lock of the UHVCVD. This mini-cleanroom atmosphere minimizes the amount of particulate contamination during the
loading of the wafers for regrowth to 100% Ge. All of these growth sequence alterations and precautions have resulted in lower particulate densities on the wafers, but only incremental improvements in the threading dislocation density. Thus, the material quality of these buffers has basically reached its realistic limits for growths in this research lab, non-cleanroom UHVCVD reactor. Fortunately, threading dislocation densities of $10^6$ cm$^{-2}$ or slightly lower have proven to be low enough to demonstrate the promise of this technology as a materials integration platform. As this technology moves towards a production environment, more materials quality improvements can be anticipated.

A.2 References

APPENDIX B
SOLAR CELL FABRICATION

Required fabrication equipment:

Thermal evaporator
e-beam evaporator
Au and Zn boats (p-type)
Au and AuGe boats (n-type GaAs)
Scale (for measuring evaporation metals, etc)
Spinner (4000 rpm, 30 sec)
3 Photomasks (Front contact metal, mesa etch, AR coating {optional})
Mask aligner (20 sec, 20 mW/cm²)
Resist bake oven (96-97 °C)
Furnace (400-410 °C, capable of handling 2” wafers or 1/4 x 4” wafers as needed)
Thermal evaporator for evaporation of anti-reflection coating (currently use at NASA)

Chemicals required:

<table>
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<tr>
<th>Shorthand</th>
<th>Chemical Name</th>
<th>Manufacturer</th>
<th>Purpose</th>
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<tr>
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<td>Phosphoric acid</td>
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<td>HI-V etch</td>
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<tr>
<td>H₂O₂</td>
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<tr>
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<td>GaAs selective etch.</td>
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<tr>
<td>ZnS</td>
<td>Zinc sulfide</td>
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<td>Anti-reflection coating</td>
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</tbody>
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**Mixed chemicals, etch procedures, and contacts:**

1. **Phosphoric etch = P-etch**
   
   \[3 : 4 : 1 \quad \text{H}_3\text{PO}_4 : \text{H}_2\text{O}_2 : \text{DI}\]
   
   GaAs etch rate ~ 700 angstroms / second = 4.2 microns / min – {at 300K}
   
   Does NOT etch germanium or gold

2. **Ammonium hydroxide GaAs etch**
   
   \[2 : 1 : 50 \quad \text{NH}_4\text{OH} : \text{H}_2\text{O}_2 : \text{DI}\]
   
   GaAs etch rate ~3000-4000 Å/min. – {at 300K}
   
   Etch appears more uniform than P-etch.  
   
   DOES etch Ge slowly.

3. **Ge etch – Acetic acid etch**
   
   \[1 : 2 : 3 \quad \text{HF} : \text{H}_2\text{O}_2 : \text{Acetic acid}\]
   
   Ge etch rate ~ 6 μm/min. – {at 300K}

4(a). **Back-side etch (GaAs)**
   
   P-etch (or \(\text{NH}_4\text{OH}\)) – (~30 sec)
   
   DI rinse
   
   Pure undiluted HCl - (~30 sec)
   
   Removes GaAs oxides, but does NOT etch GaAs

4(b). **Back-side etch (Ge)**
   
   Acetic acid etch - (30 sec)
   
   DI rinse
   
   DI rinse should remove Ge oxide.

4(c). **Back-side etch (GeSi)**
   
   \(\text{NH}_4\text{OH}\) GaAs etch IF residue from MOCVD growth
   
   DI rinse
   
   Acetic acid Ge etch for GeSi from UHVCVD - (30 sec)
   
   DI rinse
   
   HF : DI (1:1) Si oxide etch (~30 sec)

5. **Front-side GaAs oxide etch**
   
   \[1 : 1 \quad \text{HCl} : \text{DI}\]
   
   Removes GaAs oxides, but does NOT etch GaAs
   
   Etch rate for phosphides reduced by orders of magnitude by diluting with DI

6. **InGaP window and BSR etch**
   
   Undiluted HCl – (~30-60 sec for 500 Å for InGaP window) – {at 300K}
   
   Etch rate for phosphides reduced by orders of magnitude by diluting with DI
7. GaAs contact etch — Selective over AlGaAs
   4 : 4 : 1  Citric : DI : H₂O₂
   Etch rate ~3000 Å/min. Total etch time ~ 30 sec. — {at 300K}
   Etches GaAs with a selectivity of ~ 200 over Al₀.₈₅Ga₀.₁₅As
   Selectivity varies for Al composition and mix percentages. See Reference M.Tong

8. Reverse imaging PR (for metal lift-off)
   AZ1529 photoresist + 1 % (weight) imidazole
   Mix and let sit overnight -- makes negative PR with correct edge dovetailing


10(a). n-contact -- Au/Ge/Au for n-GaAs — THERMAL (No longer used)
   90 wt% Au : 10 wt% Ge
   ~ 3.5 grams Au : ~0.4 grams Ge yields ~1.5 microns metal
   Two boats, one with pure Au, one with AuGe (prevents Ge reaction with boat)
   Evaporate <1000 A Au (~2 min at 30 amperes), all of AuGe, rest of Au
   Post-deposition anneal: 410-420°C, 9.5 sccm N₂, ~5 minutes (remove PR first)

10(b). n-contact -- Ni/Ge/Au for n-GaAs or n-Ge — e-beam
   50 Å Ni
   328Å Ge
   672Å Au

10(c). n-contact -- Au/Ni/Au for n-Ge (e-beam evaporator)
   200Å Au
   50Å Ni
   1000Å Au  (goto thermal evaporator to generate thicker Au)

10(d). n-contact -- Al for n-Si (e-beam evaporator)
   ~3000Å  Al

10(e). n-contact -- Au/Sb for n-GaAs and n-Ge — THERMAL
   0.5% Sb (powder) by weight
   Sb is placed in same boat with Au pellets.
   NOTE: Cannot use this contact for GeSi substrates. Although applicable
   for Ge, contact causes “pitting” of the GeSi upon anneal making further
   lithography steps difficult. (Especially spinning since vacuum will not
   hold.)

11. p-contact -- Cr/Au for p-GaAs (e-beam evaporator)
   100 Å Cr  (Cr acts as both sticking and diffusion barrier layer)
   1000Å Au  (thermal evaporator for thicker Au - ~13 pellets for 2.5 µm)
NOTE: Contact may NOT need to be annealed. Contact resistance tests were inconclusive compared to device results. If true, back contact must be annealed prior to deposition.

Image reversal using AZ-1529 photoresist

The AZ-1529 photoresist is a ~2.9mm thick positive resist which can be "modified" to behave as a negative resist for the purpose of metal liftoff. By mixing the AZ-1529 with 1% Imidazole (by weight), the following exposure and baking sequence will provide the necessary "undercut" resist profile for metal liftoff.

1.) Spin resist at 4000 rpm for 30 sec using 10000 rpm/sec ramp rate.
2.) Soft-bake resist for 15 min at ~95-97°C
3.) Expose resist using "negative image mask" (i.e. — areas exposed will remain resist covered) for approximately 20 seconds at a UV intensity of 20 mW/cm²
4.) Soft-bake resist again for 40 minutes
5.) "Flood" or "blanket" expose resist for additional 20 seconds at a UV intensity of 20 mW/cm²
6.) Develop in 4:1 DI:AZ-351 developer solution till all windows are cleared. (Should require 20-30 seconds) Provide additional ~5 second develop after clearing to guarantee cleared finger areas with proper profile. However, DO NOT continue to over-develop. The continued develop will deteriorate the under-cut liftoff profile.

Notes/Hints for successful exposure:
1.) The soft-bake ovens at OSU do not respond quickly to temperature fluctuations and do not stabilize quickly either. In order to prevent large temperature swings, DO NOT hold open the oven door while loading multiple samples. Keep door closed as much as possible to prevent heat loss. Should the temperature drop significantly below 95°C, the duration of the bake (15 or 40 minutes) should only be counted when the oven is at the required temperature of 95°C.

2.) The Cobalt mask aligner is currently the only aligner at OSU used for solar processing since it can accept 4" masks. The required exposure dose, 20mW/cm² for 20 seconds, is currently approximately accurate for a new, uncoated bulb which is properly aligned. However, these power readings do not agree with those measured using the Thermopile detector which has been noted in the log book. Consequently, it is frequently necessary to run calibration samples in order to determine the optimum exposure time. For the develop stage it is also instructive in determining whether the resist is "over" or "under" exposed. "Under" exposed resist will require longer to develop and at the same time will "thin" the entire resist layer. Consequently, the final window will no longer have a 2.9µm step, but something less (possibly much less!).
3.) AZ-1529
   a.) The AZ-1529 photoresist has an expiration date of less than 1 year after purchase. Since the resist is only available in 1 gallon quantities (~$800), it is impractical to dispose of the resist after the expiration. Fortunately, if the resist is refrigerated it will last well past expiration. How long past expiration the resist is useful cannot be determined. If there are exposure problems which cannot be accounted for by any other explanations, new resist may be the solution.
   b.) In order to refrigerate the "stock" AZ-1529, portions should be transferred to "amber" bottles for daily use. The daily AZ-1529 (no imidazole) stock should only sit for ~3 months before being dumped and replenished from the main stock. NOTE: When taking the AZ-1529 from the refrigerator, allow the bottle to warm-up to avoid water condensation when opening. For the gallon bottle, this could take a few hours. (Letting it sit out overnight may be more viable.)
   c.) The "negative" AZ-1529 /Imidazole mixture should only be used for ~1 month prior to mixing a new solution. Also, after mixing the imidazole the solution needs to sit overnight prior to use in order for the imidazole to properly dissolve.

4.) The current solar mask sets (3 variations (cell size) of 3-level process), as well as the patterning masks, were manufactured at Advanced Reproductions Corporation. The mask containing 1cm$^2$ cells WAS NOT designed at OSU but provided by N. Fatemi while he was processing for Essential Research Corporation. The mask containing 0.4x0.4 cm$^2$ and 0.6x0.6 cm$^2$ cells the mask containing the 0.2x0.2 cm$^2$ cells were both designed at OSU. Through Advanced Reproductions, it is possible to have a "master" set of masks made in order to make additional copies of the mask cheaper if they are ordered in the future. A "master" of the 0.4x0.4 cm$^2$ mask was made, meaning that copies of a given plate will only cost ~$50 instead of ~$300. However, since the original 1cm$^2$ mask design was not done at OSU, we are unable to have additional copies of these masks made since the rights belong to Essential Research.

**Detailed fabrication sequence:**

**Back Contact**

Until recently, back contact metalization has been performed in the thermal evaporator (NRC), or a combination of the NRC and e-beam evaporator (CHA) in order to unable a thicker metal for the solar cell. However, due to the large area of the back contact, it has been determined that a thinner back contact is also acceptable. Below is the process used for all three substrates (GaAs, Ge, and GeSi) for the back contact deposition in the CHA.

1. Spin PR on front. (Protect front side) AZ1529/4000 rpm/30 sec
2. Soft bake at 90-100 °C for 15-20 min.
4. Clean back-side: Etch and oxide removal (substrate dependent)
5. Load into evaporator, and deposit appropriate back contact for substrate.
6. Remove front-side resist -- straight acetone for 1-2 minutes will do it
7. Post metallization anneal IF only annealing back contact, 
400°C (8 sccm N₂ for 4” tube furnace, 5 sccm N₂ for small 2” furnace) 
5 min for GaAs and Ge – Au contact (30 sec push / 4 min anneal / 30 sec pull) 
15 min for SiGe – Al contact (30 sec push / 15 min anneal / 30 sec pull)

Front Contact – reverse-imaging photostep

1. Spin on AZ1529 + 1 wt% imidazole (mixed previous night)
2. Soft bake at 96-97 °C for 15 minutes
3. UV exposure with photomask -- 20 sec, 20 mW/cm²
   Emulsion should contact wafer
   Clean mask after each use with acetone (chromium or iron oxide emulsions)
4. Soft bake at 96-97 °C for 40 minutes
5. Mix developer during bake -- 4 : 1 DI : concentrated AZ351 developer
   Does not keep overnight -- mix the day of use
6. Flood UV exposure (no mask) -- 20 sec, 20 mW/cm²
7. Develop -- use 2 beakers of developer
   First beaker - watch for pattern to emerge, should take < 30 seconds
   DI rinse (do not overdevelop here, since flood exposure makes PR weaker)
   Second beaker - ~5 seconds to make sure open areas are clear of PR
   DI rinse > 1 minute, flowing DI

Front contact – metallization and liftoff

Cr-Au “unannealed” is the contact of choice based on recent cell results. Prior 
feeling was that the e-beam process would damage the emitter and result in poor device 
performance. Using “slow” deposition rates (< 3.0 Å/sec) and thin layers (< 1000 Å), 
results do not support this conclusion. In addition, the Cr-Au contact provides better 
“sticking” than the thermally evaporated Au-Zn contact. However, this does not 
conclude that the e-beam evaporated Au-Zn contact would not provide a better contact 
resistance. However, due to the concerns about Zn diffusion even without a contact 
anneal, the Cr-Au contact, also unannealed, appears to be a good solution. (Although 
unproven, Dr. Andy Allerman at Sandia National Labs believes that the annealing of the 
Cr-Au contact could lead to spiking into the emitter and higher contact resistance.)

1. Front metallization -- 2-3 microns thick
   Pre-clean: 5:1 DI:HCl, ~30 sec, DI rinse, N₂ dry (removes GaAs oxide)
2. Metal deposition in e-beam evaporator followed by “thicker” (~2.5µm) Au 
   deposition in thermal evaporator. (~13 pellets = 2.5µm)
3. Liftoff metal in pure acetone
   Metal is in tension, which helps liftoff
   Metal should begin peeling off in a few seconds
Helpful to “spray” fingers off on a towel with acetone bottle in order to keep solution and beaker walls “clean” of Au fingers. Also, aggressive spray may be required to dislodge final fingers. Ultrasonic cleaner may be necessary to free final Au residue as well.

NO DI rinse during this step

3. Dektak thickness check is appropriate at this point - need minimum 2 microns

Mesa etching -- isolates individual solar cells

1. Spin on AZ1529 photoresist (positive resist, no imidazole)
2. Soft bake for 35 minutes, 90-100 °C
3. UV expose through mesa etching mask -- 20 seconds, 20 mW/cm²
4. Mix developer during bake -- 4 : 1 DI : concentrated AZ351 developer
   Does not keep overnight -- mix the day of use
5. First beaker - watch for pattern to emerge, should take < 30 seconds
   DI rinse (some overdeveloping here will be ok)
   Second beaker - ~5 seconds to make sure open areas are clear of PR
   DI rinse > 1 minute, flowing DI
6. Etch using NH₄OH etch ONLY ~1μm into base region
   Straight HCl required to etch window layer IF InGaP window used.
   Dektak resist thickness prior to etch and also post-etch to verify mesa depth. Do NOT want to “over-etch” down to Ge interface due to current problems with series resistance with interface initiation.
    DI rinse
7. Remove PR in straight acetone

Anti-reflection coating:

1. Spin AZ-1529 resist (no imidazole) and expose with ARC mask. Develop as with other resist examples.
2. Remove p⁺⁺ GaAs contact cap
   Citric selective etch for AlGaAs window
   NH₄OH for InGaP window (HCl only will etch InGaP)
   Metal grid is the etch mask. MUST completely remove cap to avoid excess absorption. However, due to “undercut” do not want to over-etch to long.
3. AR coating: 75 Å MgF₂ (sticking layer for ZnS)
   480 Å ZnS
   990 Å MgF₂
4. Acetone dip for liftoff of ARC in contact pads.

NOTES:

1. Current data indicates that this ARC is matched ONLY to an AlGaAs window and NOT to the current 500 Å InGaP window. Phil Jenkins at NASA Glenn
Research Center provided the calculations for this ARC “recipe” based on Al$_{0.85}$Ga$_{0.15}$As. Additional calculations should be performed for an ideal InGaP ARC, but was not available at the time of this printing.

2. Additionally, it is also possible to use the ARC mask in order to “etch-back” the ARC post-deposition. In this case, the AZ-1529 + imidazole solution must be used. Also, the ARC, while removed readily in HF, is difficult to remove ~24 hours after deposition. Etch-back should be completed the same day as deposition if possible.

3. The ARC evaporator crystal monitor must be calibrated periodically in order to verify the correct tooling factors for deposition. Thick layers of MgF$_2$ are typically used. These calibrations have recently been provided by Mark Smith at NASA Glenn Research Center who is frequently running the Arc evaporator.

4. Past problems with ARC’s “lifting off” in an acetone dip were attributed to an excess of oil in the belljar which was then incorporated into the film. In order to ensure a clean evaporation, it is helpful to wipe down the bell jar with acetone either before or after every run.

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Metal liftoff process:


Selective citric acid etch:

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