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ABSTRACT

In the past decade, CMOS technology has played a major role in the rapid advancement and the increased integration of VLSI systems. CMOS devices feature high input impedance, extremely low offset switches, high packing density, low switching power consumption, and most importantly, they are easily scaled. With the reduction of the device minimum feature size, in order to prevent the transistor from breakdown because of the higher electrical field across the gate oxide and to ensure its reliability, the power supply voltage is necessary to be reduced.

With the reduction of the device minimum feature size, more and more transistors can be fabricated into a single chip. Nevertheless, the large amount of circuits integrated in a chip result in huge power consumption. Decrease of the supply voltage can not only ensure the device reliability, but also reduce power consumption in a significant amount. Furthermore, portable/mobile electronic equipments have become the trends of the present and future market demands. Low power supplies are the requirements of the portable/mobile electronic products.

In this dissertation, we focus on the low-voltage, low-power CMOS circuit design. Each circuit either features a rail-to-rail common-mode input voltage and/or consumes very low power. These circuits target applications in mobile telecommunications (rail-to-rail strong-inversion circuits) and in (portable) medical applications
(low-power weak-inversion circuits). Three CMOS low-voltage rail-to-rail V-I converters are introduced. In each of the rail-to-rail V-I converters, an N-type V-I converter cell is connected in parallel with its P-type counterpart to achieve common-mode rail-to-rail operation. Based on the same approach for the rail-to-rail V-I converter, a rail-to-rail multiplier and a rail-to-rail input stage of a Differential Difference Amplifier (DDA) are also designed accordingly. The rail-to-rail V-I converter and multiplier can be used as a basic building block to construct rail-to-rail analog computational circuits, and DDA-based analog circuits can provide a competitive design choice to Op-Amp-based circuits.

Through the use of the rail-to-rail V-I converter, a low-voltage 5th-order elliptic low-pass GM-C filter is designed. Because of the rail-to-rail OTAs inside, the resultant filter also has a rail-to-rail common-mode input voltage. This low-pass filter is designed for the application in baseband mobile/wireless communication. A V-I converter and a multiplier structures, which can work in either the weak-inversion or the strong-inversion saturation region, are described. By tuning the resistance value inside, the same circuit can work in both of these two regions. The weak-inversion V-I converter is applied into the design of a micropower weak-inversion GM-C filter. Because it is working in the weak-inversion region and its output current is in the nA level, only small capacitance is needed. Thus, a single-chip solution for a very low frequency filter is feasible. The cutoff frequencies of two weak-inversion low-pass filters cover the entire range of speech, so they are suitable for speech signal processing and medical hearing applications, such as integrated speech systems for hearing aids.
A low-voltage weak-inversion Variable Gain Amplifier (VGA) is described. The VGA circuit is basically comprised by an exponential converter, a four-quadrant analog multiplier, and an Operational Current Amplifier. Its applications are on the speech, audio signal processing and (portable) medical systems. Results are presented for all of these circuits.
TO MY FAMILY
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Studies in Mathematics
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CHAPTER 1

INTRODUCTION

1.1 Background

In recent years, low-voltage VLSI circuits have received lots of attentions [1, 2, 3, 4]. The power supply voltage has decreased to 3V and will continue to decrease. The demands for low voltage systems are mainly driven from three factors: technology-driven, design-driven, and market-driven. They are: reduction of the minimum feature size to scale down the chip area, fabricating millions of transistors on a single chip to save cost, and the increase in market demands for mobile/portable electronic products, respectively. These demands seem to be independent of each other, however, the advances in VLSI technology, circuit design, and product market are actually interrelated to one another.

In the past decade, CMOS technology has played a major role in the rapid advancement and the increased integration of VLSI systems. CMOS devices feature high input impedance, extremely low offset switches, high packing density, low switching power consumption, and most importantly, they are easily scaled. The minimum feature size of a MOS transistor has been decreasing [5, 6]. Current VLSI technology is scaled down to around 0.18\(\mu\)m. Scaling down the transistor sizes can then integrate more circuit components in a single chip, so the circuit area and thus its cost will be
reduced. Besides this economic consideration, smaller geometry usually lowers the parasitic capacitances, which lead to higher operating speed and lower consumption power [7]. When a MOS transistor size is decreased, not only its channel length and width are reduced, but also the thickness of the gate oxide. As a MOS transistor has a thinner gate oxide, in order to prevent the transistor from breakdown because of the higher electrical field across the gate oxide and to ensure its reliability, the power supply voltage is necessary to be reduced [8, 9, 10].

With the reduction of the device minimum feature size, more and more transistors, even millions of transistors, can be fabricated into a single chip. Nevertheless, the large amount of circuits integrated in a chip result in huge power consumption. Usually, most of the chip area is occupied by the digital circuits and the average power consumption for digital circuits is proportional to the square of the power supply voltage [7]. Thus, decrease of the supply voltage can not only ensure the device reliability, but also reduce power consumption in a significant amount.

Furthermore, portable/mobile electronic equipments have become the trends of the present and future market demands. Low power supplies are the requirements of the portable/mobile electronic products. Therefore, all of these factors contribute to the necessity of low-voltage circuit solutions.

Since the digital circuits are more and more popular, the computer-aided design tools for digital circuits are very mature, and digital circuits certainly occupy most of the fabricated chip area, the electrical characteristics of MOS transistors are optimized mainly for digital circuits. Switching to use lower power supply voltage, digital circuits do not suffer the degradation of their performances too much. However, a fundamental issue here is the fact that propagation delay in conventional CMOS logic increases
rapidly when the supply voltage is reduced to a level close to $V_T$. New logic design techniques, e.g. Pass Transistor Logic (PTL) [7], are being developed with the goal of reducing parasitic capacitances. This will reduce both power consumption and delay.

On the other hand, for analog circuits, the circuit performances, such as gain, dynamic range, speed, bandwidth, linearity, etc., are strongly affected by the low voltage supply. Therefore, new design techniques for low-voltage analog circuits are required to be developed. Moreover, we are living in an analog world, so it is inevitable to use analog signal processing. Modern analog and mixed-signal VLSI applications in areas such as telecommunications, smart sensors, battery-operated consumer electronics and artificial neural computation require CMOS analog design solutions. Thus, analog signal and information processing in low-voltage applications is really a field in which devotion of efforts is eager.

In digital circuit design, a lower supply voltage almost guarantees the lower power consumption. But, this is not always the case for analog circuit design. To achieve the same goal of circuit performance by either using a low or a higher supply voltages might lead to approximately the same level of power consumption because different circuit design techniques are utilized for using different supply voltages. Thus, low-voltage analog circuit design with the emphasis of low power consumption has become a major challenge for analog circuit designers.

1.2 Significance

The Voltage-to-Current Converter (V-I Converter), which is very often used as a basic analog building block, is one of the most essential analog cells. Based on the V-I converter, a multiplier, a GM-C (OTA-C) filter, or some other circuits can be built.
With the reduction of power supply voltage, a V-I Converter, designed to operate from higher supply voltages, will lose a significant amount of operating range and need to be reconsidered and redesigned. Achievement of a rail-to-rail operating range is a key issue for the circuit and also the other low-voltage circuits. On the other hand, low-voltage circuit design with the emphasis of low power consumption has become a major challenge for circuit designers. Low power consumption is another important consideration for circuit design. In this dissertation, there are two group of V-I converters to be presented. The first group of V-I converters operate in the strong saturation region and have rail-to-rail common-mode input voltages. The operating range is doubled compared to that of the original V-I converter design. The other group of V-I converter works in the weak-inversion region and has the micro-power consumption. It is used to built some other low-power circuits.

Based on the rail-to-rail V-I converter, all the developed circuits can thus have the property of the rail-to-rail common-mode operating voltage, which becomes even more significant when the power supply voltage keeps decreasing. A multiplier, which is also a highly useful analog cell, is built from the V-I converter, so it has the rail-to-rail input voltage. These two circuits can be used as basic building blocks to construct simple current-mode analog computational circuits. Numerous analog computational circuits can be constructed using these circuits as well.

A CMOS Differential Difference Amplifier (DDA) is a basic CMOS analog building block yielding simple analog VLSI circuits with low component count. The DDA, which is implemented by the combination of two V-I converters and an output stage, is basically an extension to the concept of an Op-Amp. Linear V-I converters with wide input ranges are required to construct a wide range DDA. The input stage of this
DDA has two rail-to-rail V-I converters, so the DDA also has a rail-to-rail common-mode input voltage range. DDA-based circuits can be realized with low component count and without component matching external to the DDA, which, however, is a requirement in almost all Op-Amp-based circuits. Therefore, DDA-based analog circuits provide a competitive design choice to Op-Amp-based circuits.

As there is a great demand for lighter hand-held mobile phones and longer battery life-time, low voltage low power IC circuit design solutions must be developed. Actually, the goal of the portable RF transceiver design is to reduce the power consumption by 30% every year [11]. As the level of integration in RF transceivers increases, CMOS will emerge as the technology with the greatest potential for cost effectiveness. This will be particularly true when mobile, wireless communication is integrated in future multimedia systems [12, 13, 14]. Most of the key building blocks for a complete RF front-end for personal communication systems applications have recently been demonstrated in CMOS, including complete RF ICs [15]. Because baseband digital circuitry is currently implemented in standard sub-micron CMOS, there is a tendency to use the same digital CMOS processes for baseband data converters and analog filters. Traditionally in CMOS, the baseband filters are realized with Switched-Capacitor (SC) techniques. However, turning MOS switches on and off and maintaining proper OpAmp operation are difficult to achieve in SC circuits with reduced supply voltage. Solutions involving on-chip voltage multiplication to boost the clock signal are not possible in scaled-down technologies where devices can not sustain the multiplied voltage. Switched OpAmps have the potential to solve these problems [16]. However, in larger bandwidth systems like CDMA with filter signal bands over several hundreds of kilohertz, continuous-time GM-C filter realizations
tend to be less power consuming. Furthermore, GM-C filters do not require extra processing steps compared to RC filters and their frequency tuning is easily achieved using DC bias currents.

The rail-to-rail V-I converter is used to be an Operational Transconductance Amplifier (OTA) in the design of a low-voltage 5th-order elliptic low-pass GM-C filter with rail-to-rail common-mode input voltage intended for use as a baseband channel selection filter in mobile RF transceivers as shown in Fig. 1.1. Therefore, no matter what the DC output voltage of the pre-stage is, this filter can be plugged into the circuit easily. This facilitates the design of the whole circuit significantly because the whole supply voltage range can all be utilized.

Figure 1.1: Mobile radio transceiver architecture.
Similarly, the second group of V-I converter, working in the weak-inversion region, is used to build the same functions of circuits as mentioned above, but with very low current and thus low power consumption. A weak-inversion multiplier is built. If the resistance value, given by the active resistor circuits inside the V-I converter and multiplier, is tuned down to certain value, the V-I converter and multiplier is able to work in the strong-inversion saturation region. Therefore, the V-I converter and the multiplier structures can be actually used to work in either the weak-inversion or the strong-inversion saturation region, depending on the resistance values and the DC bias current levels.

Considerable attentions are paid to the resultant GM-C filters. The cutoff frequency of the GM-C filter is proportional to $I/C$, i.e., $g_m/C$, where $I$ and $g_m$ are the output current and the transconductance of the OTA, respectively, and $C$ is the capacitance. If the OTA is operating in the strong saturation region, its output current is usually in the $\mu A$ level. If one wants to have a low cutoff-frequency filter, a single-chip solution for this filter is almost impossible because a large capacitance is then required. With the presented circuit, because it is working in the weak-inversion region and its output current is in the $nA$ level, only small capacitance is needed. Thus, a single-chip solution for a (very) low frequency filter is feasible. Two low-voltage, micropower 5th-order elliptic low-pass GM-C filters based on the same architecture are designed. Their cutoff frequencies cover the entire range of speech frequencies, so these filters can be applied for speech signal processing. The techniques provide a practical means for implementing very large time constants on-chip allowing single-chip solutions at very low frequencies. Fig. 1.2 shows a configuration of an integrated
speech training system for hearing impaired [17]. One can see that all of the low-pass filters have the cutoff frequencies in the range of speech frequency or even lower. These low-pass filters can be implemented by the presented weak-inversion GM-C filters. Low voltage and low power consumption are the requirements for its portable usage.

Figure 1.2: An integrated speech training system for hearing impaired [17].

Automatic Gain Control (AGC) circuits are usually used to optimize the dynamic range of an entire system. A Variable Gain Amplifier (VGA) is a critical part in the automatic gain control circuits. A low-voltage weak-inversion VGA was designed in this research. Because of its operation in the weak-inversion region, the power
dissipation is very low. Its applications are on the speech, audio signal processing and (portable) medical systems, such as hearing aids. The exponential output to linear input characteristic is required to minimize the variation in the output signal. Similarly, its application in the hearing aid can modify the input signal to be the same accepted output level, which makes hearing easier for hard-hearing people.

1.3 Organization

In this dissertation, all the circuit design is based on the low power supply voltage of 3 V. Some circuits are designed to work in the weak-inversion region, whose operating current is in the level of nA, so very low power is consumed. This dissertation consists of the design of the V-I converter or, say, the Operational Transconductance Amplifier. Some of the V-I converters feature the rail-to-rail common-mode input voltage and some of them emphasize on low power consumption. Based on the OTAs, their application circuits in multiplier, Differential Difference Amplifier, and filter (GM-C filter) design are then developed. These circuits target applications in mobile telecommunications (rail-to-rail strong-inversion circuits) and in (portable) medical applications (low-power weak-inversion circuits).

In Chapter 2, three CMOS rail-to-rail V-I Converters or OTAs are presented. Two prototypes of N-type (because the input terminals are connected to the gates of NMOS input transistors) V-I converters are introduced. Because the common-mode input range of a single N-type V-I converter is limited, in order to have a rail-to-rail common-mode input range, a complementary P-type V-I converter is connected in parallel with the N-type V-I converter to form a complete rail-to-rail V-I converter. Two different approaches are utilized to achieve the rail-to-rail constant-\( g_m \) V-I converter.
In the first approach, a constant transconductance is achieved through the use of two maximum-current selecting circuits and an output subtraction stage. In the second method, a constant transconductance value is obtained by manipulating the DC bias currents of N- and P-type V-I converter cells. These circuits can operate from rail to rail with a power supply of 3V, or less depending on the VLSI technology and the DC bias current level.

In Chapter 3, a rail-to-rail multiplier and DDA are introduced. The N-type multiplier is realized by a parallel connection of the two N-type V-I converters. The same topology, as approach I in Chapter 2, is used to reach the rail-to-rail operation for the multiplier. The input stage of this DDA has two rail-to-rail V-I converters, so the DDA also has a rail-to-rail common-mode input voltage range. Because of the linear V-I converters, the differential input range of the DDA is thus widened. Low-voltage DDA-based circuits, such as an adder/subtractor and an integrator, are also given in this chapter. They constitute basic blocks of modern low-voltage analog signal and information processing systems.

In Chapter 4, a CMOS design of low-voltage 5th-order elliptic low-pass GM-C filter with rail-to-rail common-mode input voltage is discussed. The low-voltage rail-to-rail V-I converter, introduced in Chapter 2, is used to be an Operational Transconductance Amplifier in this filter design. Seven identical OTAs and seven capacitors are utilized to build up the low-pass filter. This low-pass filter is designed for the application in baseband mobile/wireless communication.

In Chapter 5, a micro-power V-I converter and multiplier are addressed. The V-I converter and multiplier operate in the weak-inversion region, so very low power consumption is obtained. If the resistance value, provided by the active resistor
circuits inside the V-I converter and multiplier, is tuned down by, at least, the factor of 300, one can find out that the V-I converter and multiplier can then work in the strong-inversion saturation region. Two different sets of device sizes were fabricated to approve this observation.

In Chapter 6, CMOS implementations of two low-voltage, micropower 5th-order elliptic low-pass GM-C filters are presented. The OTA in these GM-C filter design is based on the weak-inversion V-I converter, introduced in Chapter 5. Its transconductance can be changed by DC currents or DC voltage. The tunable cutoff frequencies of the two filters are from 32 Hz to 1 KHz and from 1 KHz to 5 KHz, respectively. These filters provide a practical means for implementing very large time constants on-chip allowing single-chip solutions at very low frequencies. They can be applied in speech processing systems, medical applications, and other very low frequency applications.

In Chapter 7, a low-voltage weak-inversion VGA is described. The VGA circuit is basically comprised by an exponential converter, a four-quadrant analog multiplier, and an Operational Current Amplifier (OCA). The first stage of the VGA is an exponential output to linear input circuit, which converts a linear input voltage to an exponential output voltage. The second stage is a weak-inversion multiplier, which receive two exponential gain control signals from the previous stage and take two input signals. At last, the OCA converters the output current of the multiplier to the final output voltage of the VGA. This VGA circuit provides a good output gain control accuracy. Its applications emphasize on the audio signal processing and portable medical systems.

Finally, Chapter 8 concludes the circuit design given in this dissertation and provides some possible future research directions.
CHAPTER 2

LOW-VOLTAGE RAIL-TO-RAIL V-I CONVERTERS

In this chapter, three CMOS low-voltage rail-to-rail voltage-to-current converters (V-I converter), which could be used as basic building blocks to construct low-voltage current-mode analog VLSI circuits, are presented. In each of the circuits, an N-type V-I converter cell is connected in parallel with its P-type counterpart to achieve common-mode rail-to-rail operation. A linear differential relationship of the N-type V-I converter, or its P-type complement, is obtained using a new class-AB linearization technique. In the first two rail-to-rail V-I converter circuits, a constant transconductance is achieved through the use of two maximum-current selecting circuits and an output subtraction stage. In the third circuit, a constant transconductance value is obtained by manipulating the DC bias currents of N- and P-type V-I converter cells. These circuits can operate from rail to rail with a power supply of 3V, or less depending on the VLSI technology and the DC bias current level.

2.1 N-Type V-I Converter Cells

In this section, we introduce two low-voltage V-I converter cells, which can also perform the square-root function. One of them requires fully-differential inputs, but the other one doesn’t.
2.1.1 V-I Converter Requiring Fully-Differential Inputs

![V-I Converter Diagram]

Figure 2.1: An N-type V-I converter cell requiring fully-differential inputs.

An N-type low-voltage CMOS V-I converter is shown in Fig. 2.1 [18] [19], where $V_{in+} = V_C + V_{in}/2$ and $V_{in-} = V_C - V_{in}/2$. Assume MOS transistors $M_1$, $M_2$, and $M_3$ are matched, $K_1 = K_2 = K_3 = K_N$ and $V_{T1} = V_{T2} = V_{T3} = V_T$, the simple square-law drain current expression, $I_d = K_N(V_{gs} - V_{TN})^2/2$ for an NMOS transistor is used ($K_N = (\mu_{eff}C_oxW/L)_N$, where $\mu_{eff}$ is the effective electron mobility, $C_ox$ is the gate-oxide capacitance per unit area, $W$ is the channel width and $L$ is the channel length).

Refer to this circuit with $v_{in}$ as an input, and assume that $I_C$ is a fixed reference current. Due to the current mirror $M_4$ and $M_5$, the drain current of $M_3$ is equal to the constant current, $I_C$. As the input $v_{in}$ changes, the source terminals of transistors
$M_1$, $M_2$, and $M_3$ follow accordingly. The current through $M_3$ is constant. Any change in the voltage at the source terminals is amplified by the common-gate transistor $M_3$, and the result is fed back by $M_6$, $M_8$, and the common-source amplifier $M_7$ to stabilize the current through $M_7$. Hence, the drain voltage of $M_7$ is kept constant. Therefore, in the saturation region, $V_{gs3} - V_T$ of $M_3$ will be a constant, say $V_{dc}$. Because $M_1$, $M_2$, and $M_3$ are tied at their sources, we have

$$\frac{v_{in}}{2} = V_{gs1} - V_{gs3} = V_{gs3} - V_{gs2} \quad \text{(2.1)}$$

$$\frac{v_{in}}{2} = (V_{gs1} - V_T) - (V_{gs3} - V_T) \quad \text{(2.2)}$$

$$= (V_{gs3} - V_T) - (V_{gs2} - V_T) \quad \text{(2.3)}$$

Therefore,

$$V_{gs1} - V_T = (V_{gs3} - V_T) + \frac{v_{in}}{2} = V_{dc} + \frac{v_{in}}{2} \quad \text{(2.4)}$$

$$V_{gs2} - V_T = (V_{gs3} - V_T) - \frac{v_{in}}{2} = V_{dc} - \frac{v_{in}}{2} \quad \text{(2.5)}$$

Note that this results in the sum of $V_{gs1} + V_{gs2}$ being a constant. This property is referred to as “class-AB” linearization technique [20].

The output current of the V-I converter is then obtained as the difference of the two currents, $I_1$ and $I_2$. That is

$$I_1 = \frac{K_N}{2} (V_{dc} + \frac{v_{in}}{2})^2 \quad \text{(2.6)}$$

$$I_2 = \frac{K_N}{2} (V_{dc} - \frac{v_{in}}{2})^2 \quad \text{(2.7)}$$

$$I_1 - I_2 = K_N V_{dc} v_{in} = K_N \sqrt{2I_C/K_N v_{in}}$$

$$= \sqrt{2K_N I_C v_{in}} = g_{mN} v_{in} \quad \text{(2.9)}$$
where \( g_{mN} \) is a constant. Thus, a linear V-I converter is obtained. A detector circuit, as shown in Fig. 2.2, is usually used to obtain the common-mode input voltage [21], which is \( V_C \) in this case.

![Figure 2.2: A common-mode voltage detector.](image)

### 2.1.2 V-I Converter Requiring No Fully-Differential Inputs

Another low-voltage N-type V-I converter, in which the cancelation of the second order nonlinearity does not depend on balanced inputs, is shown in Fig. 2.3 [18] [19]. Assume MOS matched transistors \( M_1, M_2, M_3, \) and \( M_4 \) having \( K_1 = K_2 = K_3 = K_4 = K \) and \( V_{T1} = V_{T2} = V_{T3} = V_{T4} = V_T \).

Refer to this circuit with \( V_1 \) and \( V_2 \) as inputs, and assume that \( I_C \) is a fixed reference current. Due to the current mirrors \( M_5, M_6, \) and \( M_7 \), the drain currents of \( M_1 \) and \( M_4 \) are equal to the constant current, \( I_C \). Two output currents, \( I_1 \) and \( I_2 \), are the drain currents of transistors \( M_2 \) and \( M_3 \), respectively. The circuit is composed
Figure 2.3: An N-type V-I converter, which does not require fully-balanced inputs.

of two identical NMOS subcircuits. Transistors $M_1$, $M_2$, $M_8$, $M_{11}$ and $M_{12}$ make up one subcircuit and transistors $M_3$, $M_4$, $M_9$, $M_{13}$ and $M_{14}$ make up the other one. There are two feedback loops, $M_1$, $M_8$, $M_{12}$, $M_{11}$ and $M_4$, $M_9$, $M_{13}$, and $M_{14}$, whose loop gain and bandwidth, respectively, determine the accuracy and speed of the transconductor. $M_1$ and $M_4$ with their associated feedback circuits behave like ideal level shifters, where the gate-to-source voltages of transistors $M_1$ and $M_4$ are the shift amounts [22]. From the cross-coupled pairs of ($M_2$, $M_4$) and ($M_1$, $M_3$), the DC transfer function of this circuit is derived as follows:

$$V_1 - V_{gs2} + V_{gs4} = V_2$$ (2.10)

$$V_1 - V_{gs1} + V_{gs3} = V_2$$ (2.11)

$$\sqrt{\frac{2I_1}{K}} - \sqrt{\frac{2I_C}{K}} = V_1 - V_2$$ (2.12)
\[
\sqrt{\frac{2I_C}{K} - \sqrt{\frac{2I_2}{K}}} = V_1 - V_2
\] (2.13)

\[
I_1 = \frac{K}{2} (V_1 - V_2)^2 + I_C + \sqrt{2I_CK(V_1 - V_2)}
\] (2.14)

\[
I_2 = \frac{K}{2} (V_1 - V_2)^2 + I_C - \sqrt{2I_CK(V_1 - V_2)}
\] (2.15)

\[
I_1 - I_2 = \sqrt{8I_CK(V_1 - V_2)}
\] (2.16)

\[
= g_{mN}(V_1 - V_2)
\] (2.17)

where \(g_{mN}\) is a constant. Thus, a linear V-I converter is also obtained. Because the common-mode input range of a single N-type V-I converter is limited, and in order to have a rail-to-rail common-mode input range, a complementary P-type V-I converter is connected in parallel with the N-type V-I converter to form a differentially linear V-I converter with rail-to-rail common-mode input range [23][24].

### 2.2 Low-Voltage Rail-To-Rail V-I Converters

For a rail-to-rail V-I converter, the total transconductance has to always be constant from rail to rail, i.e., independent of the common-mode input voltage. A constant-\(g_m\) will keep harmonic distortion at very low levels [25]. For the proposed single N-type cell and its counterpart, a P-type converter cell, themselves, the V-I relations are given by

\[
I_{n1} - I_{n2} = \sqrt{2K_NI_Cv_{in}} = g_{mN}v_{in}
\] (2.18)

\[
I_{p2} - I_{p1} = \sqrt{2K_PI_Cv_{in}} = g_{mP}v_{in}
\] (2.19)

where \((I_{n1}, I_{n2})\) and \((I_{p1}, I_{p2})\) are the output currents in the N-type and P-type cells respectively, and \(g_{mN}, g_{mP}\) are the transconductances of the N-type and P-type cells.
respectively. The V-I relations are only linear when the input transistors are operating in the saturation regions. Their operating range is thus limited. In this section, we will present two approaches to achieve a constant-$g_m$ rail-to-rail V-I converter.

In the first approach, a constant transconductance is achieved by manipulating the total instantaneous output currents through the use of two maximum-current selecting circuits and an output subtraction stage. In the second method, a constant transconductance value is obtained by manipulating the DC bias currents of the N- and P-type V-I converter cells.

The applications of the new circuits are many, e.g. Operational Transconductance Amplifiers (OTA) in a GM-C filter with rail-to-rail common-mode input voltage (Chapter 4) [26]. They are also suitable for the development of a family of computational circuits (Chapter 3), which can be seen as rail-to-rail low-voltage counterparts of the computational circuits in [18] [27]. Another important application which takes advantage of the rail-to-rail common-mode operation is the use of these circuits in the implementation of large transconductance-based analog VLSI circuits, such as the cellular neural network implementation proposed in [28]. In this case, no DC level shifting will be required between outputs and inputs of different transconductors in the network.

### 2.2.1 Approach I

In this approach, the constant transconductance is achieved through the use of two maximum-current selecting circuits and an output subtraction stage. A maximum-current selecting circuit is shown in Fig. 2.4 [29]. The output current, $I_{out}$, will
always take the maximum value of $I_1$ and $I_2$. Its operational principles are explained as follows.

**Figure 2.4**: A maximum-current selecting circuit.

I. $I_1 > I_2$

Because of the current mirrors of $M_{p1}$, $M_{p2}$ and $M_{n4}$, $M_{n5}$, $M_{n6}$, the drain current of $M_{p2}$ is $I_1$ and the drain currents of $M_{n5}$, $M_{n6}$ are $I_2$. Thus, the current flowing through $M_{n8}$ is $(I_1 - I_2)$, and so is the current in $M_{n7}$. Therefore, the output current is given by

$$I_{out} = I_2 + (I_1 - I_2) = I_1 = MAX(I_1, I_2)$$  \hspace{1cm} (2.20)

II. $I_1 \leq I_2$

Again, because of the current mirrors of $M_{p1}$, $M_{p2}$ and $M_{n4}$, $M_{n5}$, $M_{n6}$, the drain
current of $M_{p2}$ is $I_1$ and the drain currents of $M_{n5}, M_{n6}$ should be $I_2$. However, in a series connection of a current source and a current sink, the minimum current always dominates [30]. Thus, because of $I_1 \leq I_2$, the drain current of $M_{n5}$ becomes $I_1$, but the drain current of $M_{n6}$ is still $I_2$. There is no current flow in $M_{n8}$ at this situation. $M_{n7}$ and $M_{n8}$ are turned off. Therefore, the output current will be

$$I_{out} = I_{M_{n6}} = I_2 = \text{MAX}(I_1, I_2) \quad (2.21)$$

From I and II, we can see that

$$I_{out} = \text{MAX}(I_1, I_2) \quad (2.22)$$

### Rail-To-Rail V-I Converter Requiring Fully-Differential Inputs

The complete circuit of the first rail-to-rail V-I converter, using the V-I converter requiring fully-differential inputs, is shown in Fig. 2.5 [31]. As we can see, this converter consists of a parallel connection of an N-type and a P-type converter cells, and also two maximum-current selecting circuits. The N-type converter cell is connected in parallel with the P-type complementary cell in order to cover all the operating common-mode input range from rail to rail. Both cells are linearized to extend the differential input signal swing. Through adjustments of transistor sizes, $K_N$ is set to be equal to $K_P$, that is, the maximum $g_m$ values, $g_{mN}$ and $g_{mP}$, which are also constant, are equal. Fig. 2.6 (a) shows the simulation result of the four currents $I_{n1}, I_{n2}, I_{p1},$ and $I_{p2}$ (indicated in Fig. 2.5) as we change the common-mode voltage from rail to rail. After taking maximum values of $(I_{n1}, I_{n2})$ and $(I_{p1}, I_{p2})$, the result is shown
in Fig. 2.6 (b). Thus, by using two maximum-current selecting circuits and a subtraction circuit, which subtracts current $\text{MAX}(I_{n2}, I_{p1})$ from current $\text{MAX}(I_{n1}, I_{p2})$ in the output stage, the output current is given by

$$I_{\text{out}} = \text{MAX}(I_{n1}, I_{p2}) - \text{MAX}(I_{n2}, I_{p1})$$ (2.23)

$$= \sqrt{2K_N I_C} v_{in} = \sqrt{2K_P I_C} v_{in}$$ (2.24)

$$= g_{mT1} v_{in}$$ (2.25)

where $g_{mT1} = g_{mN} = g_{mP}$. Therefore, a rail-to-rail linear V-I converter is obtained. Notice, from Fig. 2.6 (a), that whenever $I_{n1} > I_{p2}$ that $I_{n2} > I_{p1}$ also and that whenever $I_{p1} > I_{n2}$ that $I_{p2} > I_{n1}$ also. So, at any given time, the output currents from one particular converter, the N- or the P-type, will be inputs to the subtraction circuit. That is, the total transconductance $g_{mT1}$ will just be the maximum value of $g_{mN}$ and $g_{mP}$, as illustrated in Fig. 2.7. This also ensures that the nonlinearity cancelation as explained in Section 2.1.1 will always be maintained. The idea of a parallel connection of an N-type and a P-type cell circuits and the use of maximum-current selecting circuits can be widely extended to other computational circuits to reach the rail-to-rail operation for low-voltage VLSI applications. A similar principle has recently been used in the design of low-voltage/low-power opamps [32].

**Rail-To-Rail V-I Converter Requiring No Fully-Differential Inputs**

Similarly, another rail-to-rail V-I converter, using the V-I converter cell requiring no fully-balanced inputs, is shown in Fig. 2.8 [26]. As one can see, this converter also consists of a parallel connection of an N-type and a P-type converter cells and two maximum-current selecting circuits. For a single N-type and P-type converter cells
Figure 2.5: The complete circuit of a rail-to-rail V-I converter by Approach I, which requires fully-balanced inputs. The arrows show the direction of the ac currents when $V_{in+} > V_{in-}$. 
Figure 2.6: Simulation of (a) currents $I_{n1}$, $I_{n2}$, $I_{p1}$, and $I_{p2}$, (b) $MAX(I_{n1}, I_{p2})$ and $MAX(I_{n2}, I_{p1})$ for a rail-to-rail common mode input voltage sweep.
Figure 2.7: Simulation of transconductance $g_{mN}$, $g_{mP}$, and $g_{mT1}$ for a rail-to-rail common mode input voltage sweep.

themselves, the V-I relations

$$I_{n1} - I_{n2} = \sqrt{8K_N I_C(V_1 - V_2)} = g_{mN}(V_1 - V_2) \quad (2.26)$$

$$I_{p2} - I_{p1} = \sqrt{8K_P I_C(V_1 - V_2)} = g_{mP}(V_1 - V_2) \quad (2.27)$$

are also only linear when their input transistors are in the saturation regions. However, for the output current of Fig. 2.8,

$$I_{out} = MAX(I_{n1}, I_{p2}) - MAX(I_{n2}, I_{p1}) \quad (2.28)$$

$$= \sqrt{8K_N I_C(V_1 - V_2)} \quad (2.29)$$

$$= \sqrt{8K_P I_C(V_1 - V_2)} \quad (2.30)$$

$$= g_{mT12}(V_1 - V_2) \quad (2.31)$$
Figure 2.8: The complete circuit of a rail-to-rail V-I converter by Approach I, which does not require fully-balanced inputs. The arrows show the direction of the ac current when $V_1 > V_2$. 
it is linear from rail to rail. Another rail-to-rail linear V-I converter is obtained. The only difference from the last rail-to-rail V-I converter is a different core V-I converter cell used here, which does not require fully-balanced inputs.

2.2.2 Approach II

For a rail-to-rail V-I converter, if the total transconductance is the sum of the transconductances of the N-type and P-type cells, requiring fully-balanced inputs, we need [25] [23]

\[ g_{mN} + g_{mP} = \text{constant} \]  

This means that we need \( \sqrt{I_{CN}} + \sqrt{I_{CP}} = \text{constant} \) if we set \( K_N \) and \( K_P \) equal, where \( I_{CN} \) and \( I_{CP} \) are the bias currents \( (I_C) \) in the N-type and P-type V-I converter cells, respectively. From Eq.( 2.6) and ( 2.7), we can see that

\[ \sqrt{I_1} + \sqrt{I_2} = 2\sqrt{\frac{K_N}{2} V_{dc}} \]  

From the discussion in Section 2.1.1, \( V_{dc} \) is constant and therefore \( \sqrt{I_1} + \sqrt{I_2} \) is also a constant. This means that the total transconductance will be constant if the bias currents \( I_{CN} \) and \( I_{CP} \) are provided by currents \( I_1 \) and \( I_2 \) of Eq.( 2.6) and ( 2.7). Therefore, in addition to the complementary circuit of the N-type and P-type V-I converter cells, another pair of complementary N-type and P-type bias circuits are needed to provide proper DC bias currents such that a constant-\( g_m \) is achieved.

The N-type bias circuit is shown in Fig. 2.9. The circuit is a modified version of the N-type V-I converter cell. \( M_{16} \) and \( M_{12} \) play the same roles of \( M_1 \) and \( M_3 \) of Fig. 2.1, respectively. Note that the output current, \( I_{out} \), which is the bias current \( I_{CN} \) of the N-type V-I converter cell, is limited to \( 4I_C \), as the drain current of \( M_{16} \) will not exceed \( 4I_C \). The reason why we limit the maximum current to \( 4I_C \) will become
clear in the following discussion. The operation of the current limiter is also based on the fact that in a series connection of a current source \((M_{15})\) and a current sink \((M_{16})\), the minimum current always dominates [30]. The output current of this bias circuit will flow into the drain terminal of transistor \(M_3\) of the N-type V-I converter in Fig. 2.1.

The complete circuit of the parallelly connected N-type and P-type V-I converters with the N-type and its complementary P-type bias circuits is shown in Fig. 2.10 [23] [33]. The DC transfer equation of this complete V-I converter is derived next.

For the bias currents \(I_{CN}\) and \(I_{CP}\) provided from the N-type and P-type bias circuits, assume \(K_N = K_P = K\), similar to Eq. (2.6), (2.7), and (2.33), we have

\[
\sqrt{I_{CN}} + \sqrt{I_{CP}} = 2\sqrt{\frac{K}{2}} V_{dcB} \tag{2.34}
\]
Figure 2.10: The complete circuit of the rail-to-rail V-I converter by Approach II.
where $V_{dcB} = \sqrt{2IC/K}$ ($V_{dcB} = V_{dc}$ due to the same bias currents $I_C$ for Fig. 2.1 and 2.9). Therefore,

$$\sqrt{I_{CN}} + \sqrt{I_{CP}} = 2\sqrt{\frac{K}{2}} \sqrt{\frac{2IC}{K}} = 2\sqrt{IC} \quad (2.35)$$

From Eq. (2.35), we can see why the current limiter is necessary. When one of the N-type or P-type bias circuits is turned off, the current limiter will limit the other bias current to $4IC$ which is consistent with Eq. (2.35), e.g. when $I_{CN} = 0$, $I_{CP} = 4IC$, and $\sqrt{I_{CN}} + \sqrt{I_{CP}} = 2\sqrt{IC}$.

For the N-type V-I converter cell,

$$I_{n1} = \frac{K}{2}(V_{dc1} + \frac{v_{in}}{2})^2 \quad (2.36)$$
$$I_{n2} = \frac{K}{2}(V_{dc1} - \frac{v_{in}}{2})^2 \quad (2.37)$$

where $V_{dc1} = \sqrt{2I_{CN}/K}$. Thus,

$$I_{n1} - I_{n2} = KV_{dc1}v_{in} \quad (2.38)$$

Similarly, for the P-type V-I converter cell,

$$I_{p2} - I_{p1} = KV_{dc2}v_{in} \quad (2.39)$$

where $V_{dc2} = \sqrt{2I_{CP}/K}$. Finally,

$$I_{out} = (I_{n1} - I_{n2}) + (I_{p2} - I_{p1}) \quad (2.40)$$
$$= K(V_{dc1} + V_{dc2})v_{in} \quad (2.41)$$
$$= K\sqrt{\frac{2}{K}}(\sqrt{I_{CN}} + \sqrt{I_{CP}})v_{in} \quad (2.42)$$
$$= K\sqrt{\frac{2}{K}}2\sqrt{IC}v_{in} \quad (2.43)$$
$$= 2\sqrt{2KIC}v_{in} = g_{mT2}v_{in} \quad (2.44)$$
Notice that this resultant transconductance is different from that in Approach I, and that the total transconductance $g_{mT2}$ here is two times larger than the transconductance $g_{mT1}$. This is because in Approach I, a constant transconductance is achieved by selecting the maximum value, instead of taking the sum of the two transconductances.

2.3 Experimental Results

In this section, we discuss performance results of the three circuits.

2.3.1 Approach I

Two rail-to-rail V-I converters, using different V-I converter core cells, by Approach I were fabricated. Their measurement results are addressed in this subsection.

V-I Converter Requiring Fully-Differential Inputs

The rail-to-rail V-I converter, which requires fully-balanced in Fig. 2.5, using Approach I was fabricated in a $2\mu m$ N-Well Double-Poly CMOS Process by MOSIS having $V_{Tn} = 0.8013V$ and $V_{Tp} = -0.9793V$. The chip microphotograph of this V-I converter is shown in Fig. 2.11. The transistor sizes used in this circuit are illustrated in Table 2.1. The power supply used for this circuit is a single 3V supply voltage. This circuit also works well with a power supply of $3V \pm 0.3V$. It can also operate at levels below 2.7 V depending on the DC bias current levels used and, of course, the values of $V_{Tn}$ and $V_{Tp}$.

For this rail-to-rail V-I converter, its measured DC transfer curves are illustrated in Fig. 2.12 and 2.13. In Fig. 2.12, the five straight lines were obtained when $I_C = 20\mu A, 40\mu A, 60\mu A, 90\mu A, and 140\mu A$, respectively. We can see that the input signal
Figure 2.11: The chip microphotograph of the rail-to-rail V-I converter by Approach I, which requires fully-differential inputs. The figure shows clockwise starting from the top left hand corner, N-type cell, output subtraction stage, two maximum current-selecting circuits, and P-type cell.

swing is $2V_{pp}$ when the bias current, $I_c$, is varied from $20\mu A$ to $140\mu A$. Also, the transconductance is changed from about $200\mu S$ to $400\mu S$, as shown in the figure. In Fig. 2.13, when we decrease the input signal swing from $2V_{pp}$ to $1V_{pp}$ to keep the same linearity as in Fig. 2.12, a larger transconductance range, from $100\mu S$ to $400\mu S$, is obtained while the bias current, $I_c$, is tuned from $3\mu A$ to $150\mu A$. The large transconductance tuning range is achieved through the tradeoff of the smaller input signal swing. Fig. 2.14 shows the measured output current for a rail-to-rail common mode input voltage sweep when we set $v_{in} = 0.1V$. The maximum output current variation is about 15%. From this figure, we can see that the rail-to-rail operation of this V-I converter is achieved. As for the linearity of the V-I converter, there is about 1.61% and 2.46% total harmonic distortion (THD) for $1V_{pp}$ and $2V_{pp}$ 10KHz input signals, respectively.
Table 2.1: The transistor sizes of the rail-to-rail V-I converter, requiring fully-differential inputs, by Approach I.

### V-I Converter Requiring No Fully-Differential Inputs

The second rail-to-rail V-I converter, which does not require fully-balanced inputs in Fig. 2.8, using Approach I was fabricated in the 1.2\( \mu \text{m} \) CMOS process of AMS, having \( V_{\text{rn}} = 0.736\text{V} \) and \( V_{\text{rp}} = -0.751\text{V} \), in Austria. The chip microphotograph of the V-I converter is shown in Fig. 2.15. It occupies 0.0989\( \text{mm}^2 \) area. The power supply used for this circuit is also a single 3V supply voltage.

For this rail-to-rail V-I converter, all the transistor sizes are illustrated in Table 2.2. The measured DC transfer curves of the V-I converter are shown in Fig. 2.16 and 2.17. In Fig. 2.16, the V-I curves were obtained when \( I_C = 3\mu\text{A}, 5\mu\text{A}, \) and \( 7\mu\text{A} \), respectively. We can see that the input signal swing is \( 2V_{pp} \) for changing the bias current, \( I_C \), from 3\( \mu\text{A} \) to 7\( \mu\text{A} \). Also, the transconductance is changed from about 30\( \mu \text{S} \) to 40\( \mu \text{S} \), as shown in the figure. In Fig. 2.17, when we decrease the input signal swing from \( 2V_{pp} \) to \( 1V_{pp} \) to keep the same linearity as in Fig. 2.16, a larger transconductance range, from 15\( \mu \text{S} \) to 40\( \mu \text{S} \), is obtained while the bias current, \( I_C \),
is tuned from $0.5\mu A$ to $7\mu A$. The larger tuning transconductance range is achieved through the tradeoff of the smaller input signal swing. Fig. 2.18 shows the measured output current for a rail-to-rail common mode input voltage sweep when $V_1 - V_2 = 0.2V$ and $I_C = 5\mu A$. The maximum output current variation is about 12%. From this figure, we can see the rail-to-rail operation of this V-I converter is achieved. As for the linearity of this V-I converter, there is about 0.45% and 1.23% total harmonic distortion (THD) for $1V_{PP}$ and $2V_{PP}$ 1KHz input signals, respectively. The DC power consumption is about $0.37mW$ when $I_C = 5\mu A$, $V_2 = 1.5V$, and $V_1 - V_2 = 0.2V$. Its measured -3 dB frequency is about 5 MHz.
Figure 2.13: The measured DC transfer curves of the Approach-I V-I converter, which requires fully-differential inputs, with $I_C = 3\mu A$, $20\mu A$, $50\mu A$, and $150\mu A$, respectively.

2.3.2 Approach II

The rail-to-rail V-I converter, which requires fully-balanced inputs in Fig. 2.10, using Approach II was fabricated in the $1.2\mu m$ CMOS process of AMS, having $V_{Tn} = 0.736\,V$ and $V_{Tp} = -0.751\,V$, in Austria. The chip microphotograph of the V-I converter is shown in Fig. 2.19. It occupies $0.129\,mm^2$ area. The transistor sizes used are shown in Table 2.3. The power supply used for this circuit is a single $3\,V$ supply voltage and the circuit can also work well with a power supply of $2.7\,V$ or lower depending on the values of $V_T$ used and on the levels of the DC bias currents. Generally, note that the minimum supply voltage that can be used in both Approach
Figure 2.14: The measured output current of the Approach-I V-I converter, which requires fully-differential inputs, for a rail-to-rail common mode input voltage sweep with $v_{in} = 0.1V$.

$I$ and II is approximately equal to $2V_{GS} + 2V_{DS,sat}$. Below this level the input transistors may go from strong to weak inversion and the DC bias current sink (source) of the N-type (P-type) cell may go from the saturation to the triode region.

For the rail-to-rail V-I converter, its V-I curves are shown in Fig. 2.20 and 2.21. In Fig. 2.20, the transfer curves were obtained when $I_C = 2\mu A$, $4\mu A$, and $6\mu A$, respectively. We can see that the input signal swing is $2V_{PP}$ and that the transconductance is changed from about $20\mu S$ to $35\mu S$ by changing the bias current, $I_C$, from $2\mu A$ to $6\mu A$. In Fig. 2.21, when we decrease the input signal swing from $2V_{PP}$ to $1V_{PP}$ to keep the same linearity, a larger transconductance range, from $10\mu S$ to $35\mu S$, is obtained while the bias current, $I_C$, is tuned from $0.5\mu A$ to $6\mu A$. Fig. 2.22 shows the output current for a rail-to-rail common mode input voltage sweep using $v_{in} = 0.4V$
Figure 2.15: The chip microphotograph of the rail-to-rail V-I converter by Approach I, which requires no fully-differential inputs.

<table>
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<th>W/L ((\mu m/\mu m))</th>
<th>Comment</th>
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</tr>
<tr>
<td>M5, M6, M7</td>
<td>60/3</td>
<td>cell</td>
</tr>
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</tr>
<tr>
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<td>9.6/6</td>
<td>P-type V-I Converter</td>
</tr>
<tr>
<td>Mp5, Mp6, Mp7</td>
<td>20.4/3</td>
<td>cell</td>
</tr>
<tr>
<td>Mp8, Mp9, Mp11, Mp12, Mp13 Mp14</td>
<td>110.4/1.8</td>
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</tr>
<tr>
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<td>60/1.8</td>
<td>Maximum-current</td>
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<td>selecting circuit</td>
</tr>
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<td>30/1.8</td>
<td>output stage</td>
</tr>
<tr>
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<td>10.2/1.8</td>
<td></td>
</tr>
</tbody>
</table>

Table 2.2: The transistor sizes of the rail-to-rail V-I converter, which does not require fully-balanced inputs, by Approach I.

when \(I_C = 2\mu A\). The two bumps at common-mode input voltages close to 1V and 2V are because the N-type input transistors are not entirely cut off, but work in the weak-inversion region, when the P-type transistors are entering the strong saturation region, and vice versa. The maximum output current variation for common mode voltage from 0 to 2.8V is about 13%. From this figure, we can see that the rail-to-rail operation of this V-I converter is nearly achieved. For the linearity of the V-I
Figure 2.16: The measured DC transfer curves of the Approach-I V-I converter, which does not require fully-balanced inputs, with $I_C = 3\mu A$, $5\mu A$, and $7\mu A$, respectively.

At $I_C = 2\mu A$, $V_{CM} = 1.5V$, and $v_{in} = 0.4V$, the DC power consumption for the Approach-II circuit is about 0.31 mW. When we decrease the transistor sizes of the first Approach-I circuit (also requiring fully-balanced inputs) to have the same output transconductance as Approach II at $I_C = 2\mu A$, its power consumption is only about 0.12 mW. In Approach II, a constant $g_m$ is achieved through additional circuitry to the DC part of the circuit. This may not be very suited for low-power applications. On the other hand, in Approach I, a constant $g_m$ is achieved by manipulating the output, rather than DC, currents of the N- and P-type cells. This leads to saving in power consumption.
Figure 2.17: The measured DC transfer curves of the Approach-I V-I converter, which does not require fully-balanced inputs, with $I_c = 0.5\mu A$, $1.5\mu A$, $3\mu A$, $5\mu A$, and $7\mu A$, respectively.

2.4 Improvement of the $K_N \neq K_P$ Condition

For the two rail-to-rail V-I converters developed by Approach I, their rail-to-rail operation accuracies strongly rely on the assumption of $K_N = K_P$. For the V-I converter requiring fully-balanced inputs,

$$I_{out} = \sqrt{2K_N I_C V_{in}} = g_{mN11} V_{in}$$

(2.45)

$$= \sqrt{2K_P I_C V_{in}} = g_{mP11} V_{in}$$

(2.46)

$$= g_{mT11} V_{in}$$

(2.47)

For the rail-to-rail V-I converter requiring no fully-balanced inputs,

$$I_{out} = \sqrt{8K_N I_C (V_1 - V_2)} = g_{mN12} (V_1 - V_2)$$

(2.48)

$$= \sqrt{8K_P I_C (V_1 - V_2)} = g_{mP12} (V_1 - V_2)$$

(2.49)
Figure 2.18: The measured output current of the Approach-I V-I converter, which does not require fully-balanced inputs, for a rail-to-rail common mode input voltage sweep with $V_1 - V_2 = 0.2V$.

\[ I_{\text{out}} = g_{mT12}(V_1 - V_2) \]  \hspace{1cm} (2.50)

$K_N$ is set to be equal to $K_P$ so that $g_{mN1*} = g_{mP1*} = g_{mT1*}$ in each case because the same bias current $I_C$ is used. Thus, the output current can be kept constant from rail to rail.

For $K_N$ and $K_P$,

\[ K_N = \frac{1}{2} \mu_n C_{OX} \left( \frac{W}{L} \right)_n \]  \hspace{1cm} (2.51)

\[ K_P = \frac{1}{2} \mu_p C_{OX} \left( \frac{W}{L} \right)_p \]  \hspace{1cm} (2.52)

If a pre-defined fabrication process is accessible, one can have enough information about the electron mobility to the hole mobility ratio so that $(W/L)_n$ and $(W/L)_p$ can be correctly chosen to satisfy the assumption of $K_N = K_P$. However, if we do not
have prior knowledge to the process or the process used is usually changed from one to another run, having a compensation circuit to achieve $K_N I_{CN} = K_P I_{CP}$ will be helpful to achieve a constant output current from rail to rail for the two V-I converters by Approach I, where $I_{CN}$ and $I_{CP}$ are the bias currents for N-type and P-type V-I converter cells, respectively.

Fig. 2.23 [34] [25] shows the compensation circuit, which satisfies $K_N I_{CN} = K_P I_{CP}$, and an NMOS and a PMOS current mirrors, which provide bias currents $I_{CN}$ and $I_{CP}$ for the N-type and P-type V-I converter cells. As one can see, from transistors MB1, MB2, MB3, and MB4 [34] [25],

$$V_{GS1} + V_{SG4} = V_{SG3} + V_{GS2} \tag{2.53}$$

$$(\sqrt{\frac{I_{CP}}{K_N}} + V_{TN}) + (\sqrt{\frac{I_{CN}}{K_P}} - V_{TP}) = (\sqrt{\frac{I_{CN}}{K_P}} - V_{TP}) + (\sqrt{\frac{I_{CP}}{K_N}} + V_{TN}) \tag{2.54}$$

$$\sqrt{\frac{I_{CP}}{4K_N}} + \sqrt{\frac{I_{CN}}{K_P}} = \sqrt{\frac{I_{CN}}{4K_P}} + \sqrt{\frac{I_{CP}}{K_N}} \tag{2.55}$$

$$\sqrt{\frac{I_{CN}}{K_P}} = \sqrt{\frac{I_{CP}}{K_N}} \tag{2.56}$$

Therefore,

$$K_N I_{CN} = K_P I_{CP} \tag{2.57}$$
In this section, the first rail-to-rail V-I converter, requiring fully-balanced inputs, is taken as an example to see the difference made between this converter with and without the $K_{NiCN} = K_{PiCP}$ compensation circuit.

A SPICE parameter model from MOSIS, which shows $\mu_n/\mu_p$ ratio is about 2.8, is used. There are two comparisons which are made. The first comparison is made by assuming we have the prior knowledge to the fabrication process which will be used, so $(W/L)_n$ and $(W/L)_p$ can be correctly chosen to make $K_N = K_P$. The $(W/L)_p$ to $(W/L)_n$ ratio is set to be 2.8. Fig. 2.24 illustrates the simulated output currents of the V-I converters with and without the compensation circuit for a rail-to-rail common mode input voltage sweep, at $V_1 - V_2 = 0.2V$, when $(W/L)_p$ to $(W/L)_n$ ratio is set to be 2.8. The rail-to-rail output current variation for the V-I converters with and without the $K_{NiCN} = K_{PiCP}$ circuit are about 4.0% and 9.2%, respectively. The

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Table 2.3: The transistor sizes of the rail-to-rail V-I converter by Approach II.
second comparison is made by assuming that we have no any information about the process which will be used and that the \( \frac{W}{L}_p \) to \( \frac{W}{L}_n \) ratio is chosen to be 2. Fig. 2.25 shows the simulated output currents of the V-I converters with and without the \( K_N I_{CN} = K_P I_{CP} \) circuit for a rail-to-rail common mode input voltage sweep, at \( V_1 - V_2 = 0.2V \), when \( \frac{W}{L}_p \) to \( \frac{W}{L}_n \) ratio is set to be 2. The rail-to-rail output current variation for the V-I converters with and without the \( K_N I_{CN} = K_P I_{CP} \) circuit are about 12.5% and 28.6%, respectively. We can see in both situations the one with the \( K_N I_{CN} = K_P I_{CP} \) circuit has less output current variation. The compensation circuit does help the rail-to-rail V-I converter have more constant output current.
Figure 2.21: The measured DC transfer curves of the Approach-II V-I converter with $I_C = 0.5\mu A, 1\mu A, 2\mu A, 4\mu A$, and $6\mu A$, respectively.

Figure 2.22: The measured output current of the Approach-II V-I converter for a rail-to-rail common mode input voltage sweep with $v_{in} = 0.4V$. 
Figure 2.23: A compensation circuit which satisfies $K_N I_{CN} = K_P I_{CP}$.

Figure 2.24: The simulated output currents of the V-I converter with and without the $K_N I_{CN} = K_P I_{CP}$ circuit at $V_1 - V_2 = 0.2V$ when $(W/L)_p$ to $(W/L)_n$ ratio is set to be 2.8.
Figure 2.25: The simulated output currents of the V-I converter with and without the $K_N I_{CN} = K_P I_{CP}$ circuit at $V_1 - V_2 = 0.2V$ when $(W/L)_p$ to $(W/L)_n$ ratio is set to be 2.
CHAPTER 3

LOW-VOLTAGE RAIL-TO-RAIL MULTIPLIER AND DIFFERENTIAL DIFFERENCE AMPLIFIER

This chapter discusses a low-voltage rail-to-rail multiplier and a rail-to-rail Differential Difference Amplifier (DDA). The basic cells inside these circuits are the prototype V-I converters, introduced in Chapter 2. For the N-type multiplier, it is realized by a parallel connection of the two N-type V-I converters with fully-balanced inputs. Two maximum-current selecting circuits are utilized to achieve the rail-to-rail multiplier, the same strategy as the Approach I described in Chapter 2. For the DDA, its input stage comprises two rail-to-rail V-I converters, so it can have a rail-to-rail common-mode input voltage. The experimental results are presented after the description of the circuit designs.

3.1 Low-Voltage Rail-to-Rail Multiplier

In this section, an N-type multiplier is introduced first. As the Approach I discussed in Chapter 2, through a parallel connection of an N-type and a P-type multiplier cells and the use of maximum-current selecting circuits, a rail-to-rail multiplier is then obtained.
3.1.1 N-Type Multiplier

An N-type multiplier cell is shown in Fig. 3.1 [18] [27]. This analog four-quadrant multiplier is realized by a parallel connection of two N-type V-I converters, shown in Fig. 2.1 in Chapter 2. For this multiplier cell, its DC transfer equation is derived as follows [18] [27]. From transistors M1 and M3,

\[ V_{1P} - V_{2P} = V_{gs1} - V_{gs3} = \sqrt{\frac{2I_1}{K_1}} - \sqrt{\frac{2I_3}{K_3}} \tag{3.1} \]

\[ \sqrt{I_1} = \sqrt{\frac{K_1}{2}}(V_{1P} - V_{2P}) + \sqrt{\frac{K_1 I_C}{K_3}} \tag{3.2} \]

\[ I_1 = \frac{K_1}{2}(V_{1P} - V_{2P})^2 + \frac{K_1 I_C}{K_3} + \sqrt{\frac{2I_C}{K_3}}K_1(V_{1P} - V_{2P}) \tag{3.3} \]

Similarly,

\[ I_2 = \frac{K_2}{2}(V_{1M} - V_{2P})^2 + \frac{K_2 I_C}{K_3} + \sqrt{\frac{2I_C}{K_3}}K_2(V_{1M} - V_{2P}) \tag{3.4} \]
\[ I_7 = \frac{K_7}{2}(V_{1M} - V_{2M})^2 + \frac{K_7 I_C}{K_8} + \frac{2I_C}{K_8}K_7(V_{1M} - V_{2M}) \]  
\[ I_9 = \frac{K_9}{2}(V_{1P} - V_{2M})^2 + \frac{K_9 I_C}{K_8} + \frac{2I_C}{K_8}K_9(V_{1P} - V_{2M}) \]  

\( I_i \) (i=1,2,...) is the current through the ith transistor. Assuming \( V_{1P} = V_C + V_1/2 \), \( V_{1M} = V_C - V_1/2 \), \( V_{2P} = V_C + V_2/2 \), \( V_{2M} = V_C - V_2/2 \), \( K_1 = K_2 = K_3 = K_7 = K_8 = K_9 = K \) and by appropriately combining these currents we obtain the desired output current.

\[ I_{out} = I_Y - I_X = I_2 + I_9 - I_1 - I_7 = KV_1V_2 \]  

Note that for the multiplier, the parallel architecture allows response time equal to that of an N-type V-I converter cell.

### 3.1.2 Design of the Rail-to-Rail Multiplier

![Block Diagram of Rail-to-Rail Analog Multiplier](image)

Figure 3.2: The block diagram of a rail-to-rail analog multiplier.

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For a rail-to-rail analog multiplier, it is implemented in a similar way as the rail-to-rail V-I converter using Approach I in Chapter 2, that is, a parallel connection of an N-type and a P-type multiplier cells and the inclusion of two maximum-current selecting circuits, as illustrated in the block diagram of Fig. 3.2. For the single N-type and P-type cells themselves, the following multiplication function can be obtained

\[ I_{nx} - I_{ny} = K_N V_1 V_2 \]  \hspace{1cm} (3.8)
\[ I_{px} - I_{ny} = K_P V_1 V_2 \]  \hspace{1cm} (3.9)

The relations are also satisfied only when their input transistors are in the saturation regions. By using the two maximum-current selecting circuits and the subtraction circuit in the output stage, the output current is given by

\[ I_{out} = MAX(I_{nx}, I_{px}) - MAX(I_{ny}, I_{py}) \]  \hspace{1cm} (3.10)
\[ = K V_1 V_2 \]  \hspace{1cm} (3.11)

Therefore, a low-voltage rail-to-rail analog multiplier is obtained.

### 3.1.3 Experimental Results

The multiplier circuit was fabricated in a 2\( \mu \)m N-Well Double-Poly CMOS Process by MOSIS. Its microphotographs is shown in Fig. 3.3. The transistor sizes used are shown in Table 3.1. A single 3V supply voltage was used to measure the circuit. This circuit can also work well with a power supply of 3V ± 0.3V.

Fig. 3.4 and 3.5 show the measured DC transfer curves of the multiplier when \( I_C = 130\mu A \). In Fig. 3.4, the horizontal axis represents the differential input voltage \( V_1 \) and the vertical axis is the output current. The curves were obtained by sweeping \( V_1 \) from -0.5V to 0.5V, while varying \( V_2 \) from -0.8V to 0.8V with a step of 0.2V.
Figure 3.3: The microphotographs of the rail-to-rail multiplier.

For Fig. 3.5, the horizontal axis represents the differential input voltage $V_2$ and the vertical axis is also the output current. These curves were obtained by sweeping $V_2$ from -0.8V to 0.8V, while varying $V_1$ from -0.5V to 0.5V with a step of 0.1V. We can see that the input signal swings of the multiplier are $1V_{pp}$ for $V_1$ and $1.6V_{pp}$ for $V_2$. Fig. 3.6 shows the measured output current for a rail-to-rail common mode input voltage sweep when $V_1 = V_2 = 0.1V$ and $I_C = 130\mu A$. The maximum output current variation is about 18%. From this figure, we can see the rail-to-rail operation of the multiplier is achieved. Also, when $I_C = 130\mu A$, the distortion of this multiplier for $V_1$ and $V_2$ with a $1V_{pp}$ 10KHz input signal is about 1.74% and 0.23%, respectively. The linearity of the input signal at $V_2$ is better than that at $V_1$. 

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Table 3.1: The transistor sizes of the rail-to-rail multiplier.

### 3.2 Low-Voltage Rail-to-Rail Differential Difference Amplifier

This section introduces a low-voltage rail-to-rail wide range CMOS Differential Difference Amplifier. The input stage of this DDA comprises two rail-to-rail V-I converters with large signal handling capability. The DDA is designed to have a rail-to-rail constant input transconductance and a rail-to-rail output swing. Low-voltage DDA-based circuits, such as an adder/subtractor and an integrator, are given here. They constitute basic blocks of modern low-voltage analog signal and information processing systems.

#### 3.2.1 Introduction

The DDA is a basic CMOS analog building block yielding simple analog VLSI circuits with low component count [35, 36, 37, 38]. The symbol of the DDA is shown
in Fig. 3.7. A DDA is basically an extension to the concept of an Op-Amp. The main difference between these two circuits is that the DDA has two pairs of differential inputs \((V_{pp} - V_{pn})\) and \((V_{np} - V_{nn})\) while an Op-Amp only has one pair of input ports. The output of a DDA can be expressed as

\[
V_o = A_o [(V_{pp} - V_{pn}) - (V_{np} - V_{nn})]
\]  

(3.12)

where \(A_o\) is the open-loop gain of the DDA. When \(A_o\) is very large and a negative feedback is introduced, one can obtain

\[
V_{pp} - V_{pn} = V_{np} - V_{nn}
\]

(3.13)
Figure 3.5: The measured output current of the multiplier for sweeping $V_2$ from -0.8V to 0.8V, while varying $V_1$ from -0.5V to 0.5V with the step of 0.1V.

We can see that although $V_{pp}$ and $V_{pm}$ ($V_{np}$ and $V_{nn}$) do not have the property of virtual ground, the difference between the two differential input voltages is virtually zero.

As the supply voltage decreases, the common mode input voltage of conventional DDAs, defined as the input voltage range over which the input stage properly responds to differential difference input signals as a linear amplifier, becomes very small. This is mainly caused by the unchanged turn-on voltage of the input transistors. To keep the signal-to-noise ratio as large as possible, the common mode input voltage should be kept as wide as possible. Therefore, NMOS input pairs and PMOS input pairs are in parallel connected to reach the rail-to-rail operation.
Figure 3.6: The measured output current of the multiplier with $V_1 = V_2 = 0.1V$ and $I_C = 130\mu A$ for a rail-to-rail common mode input voltage sweep.

However, if there are no any $g_m$-control circuits in the DDA to control the input transconductance, the $g_m$ value in the mid-supply voltage will be about two times larger than those in the two extreme rails, as shown in Fig. 3.8. Also in this figure, a DDA with $g_m$-control circuits shows a constant-$g_m$ from rail to rail. Because the unity-gain frequency is proportional to the input transconductance, if we do not have a constant rail-to-rail input transconductance, the unity-gain frequency will be changed with the common-mode input voltage, as illustrated in Fig. 3.9. One can see that the unity-gain frequency of the DDA without $g_m$-control circuits is varied with the common-mode voltage. The frequency response is not optimized. When this is the case, for the worst-case design, we need to design the second pole of the DDA based on the maximum possible unity-gain frequency in order to have enough phase margin.

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to ensure its stability. Note that the second-pole frequency is proportional to the transconductance in the output stage. If a maximum possible second-pole position is designed, the output stage is necessary to flow the maximum current. Under this situation, when this DDA is operated at certain common-mode voltages with a lower unity-gain frequency, it will result in a un-efficient usage of current and also power in the output stage. Therefore, a rail-to-rail constant transconductance is required in order to maintain a good amplifier performance.

Figure 3.7: The symbol of the DDA.

Figure 3.8: The input transconductances of DDAs with and without $g_m$-control circuits.

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As mentioned, since the DDA does not have the virtual short property between the two inputs in the same differential pair, it needs a wide linear input range and the voltage between them could then be quite large. Thus, we use two V-I converters to construct the input stage of the DDA to have a wide range DDA. For a DDA, built by two V-I converters, with NMOS input pairs only, usually the range of its common-mode input voltage is, say, from 1.5V to 3V by a 3V power supply. The input signals of the DDA can be changed within the linear-transconductance range of the input-stage V-I converter at the common-mode voltage range of 1.5V to 3V. However, if one has a rail-to-rail DDA, the four input signals of the DDA can be applied within the linear-transconductance range of the input-stage V-I converter at the common-mode voltage range of 0 to 3V. This is then really a so-called “wide range” DDA. Therefore, for a DDA circuit, owning the property of a rail-to-rail common-mode voltage can then make the thorough use of the DDA functions.

Figure 3.9: The unity-gain frequencies of DDAs with and without $g_m$-control circuits.
Further, for DDA-based applications, for example, in Fig. 3.18, the DDA-based adder/subtractor, \( V_o = V_1 + V_2 - V_3 \). \( V_{np} \) is connected to the output. Only if \( V_2 \) (or say, \( V_{nn} \)) and \( V_{np} \) have a rail-to-rail common-mode voltage (The common-mode voltage values of \( V_1 \) and \( V_3 \) are canceled out.), the output voltage \( V_o \) (\( V_{np} \)) can then follow any input signal change from rail to rail at \( V_2 \) (\( V_{nn} \)). Similarly, if \( V_{pn} \) is connected to the output, \( V_{pp} \) and \( V_{pn} \) need to have the rail-to-rail property to make the output voltage, \( V_{pn} \), produce the same change at \( V_{pp} \) from rail to rail. This kind of configurations, \( V_{pp} \) and/or \( V_{nn} \) are the inputs and a negative feedback is connected to \( V_{pn} \) or \( V_{np} \), which are very similar to the non-inverting connection in the Op-Amp case, are almost inevitable in the DDA-based applications. Therefore, to achieve a rail-to-rail common mode input voltage is very critical for a low-voltage DDA, as that for a low-voltage Op-Amp.

### 3.2.2 Design of the DDA

![Figure 3.10: The block diagram of the DDA.](image)

A DDA can be implemented as shown in Fig. 3.10 [36, 38]. In this block diagram, two V-I converters convert two pairs of differential voltages into currents, which are
subtracted, converted back to voltage, and then amplified. In order to have a wide range DDA, linear V-I converters with wide input ranges are required. A rail-to-rail V-I converter is necessary to ensure a rail-to-rail DDA. The low-voltage rail-to-rail V-I converter [26], which does not require balanced inputs, illustrated in Fig. 2.8 in Chapter 2, is used for this DDA design.

Based on the V-I converter, a rail-to-rail input stage of the DDA is built. Even though two rail-to-rail V-I converters are needed, instead of four, only two maximum current-selecting circuits are used for this input stage because at any given time, the output currents from one particular converter, the N- or the P-type, will be inputs to the output stage. The rail-to-rail input stage of the DDA is shown in Fig. 3.11.

![Figure 3.11: The rail-to-rail input stage of the DDA.](image-url)
To do the current subtraction, voltage conversion, and amplification, an output stage is required for the DDA. An output stage with gain and class AB control circuits is shown in Fig. 3.12 [39]. This output stage is compact, power-efficient, and has a rail-to-rail output swing. One can find more detailed discussion in [39]. Connecting $I_{out1}$, $I_{out2}$ of the input stage to $I_{in1}$, $I_{in2}$ in the output stage, respectively, we can then obtain the entire DDA structure.

![Figure 3.12: The output stage with gain and class AB control circuits.](image)

3.2.3 Experimental Results

This DDA circuit was fabricated in the 1.2μm CMOS process of AMS in Austria. The chip microphotograph of the DDA is shown in Fig. 3.13. It occupies 0.287 mm$^2$ area. The two rail-to-rail V-I converters in its input stage are exactly the same. The
transistor sizes of the V-I converter are shown in Table 3.2. The transistor sizes of the DDA output stage are shown in Table 3.3. Measurements and simulations have been performed using a 3 V supply. The circuit is biased by the bias current $I_C = 5\mu A$.

![Figure 3.13: The chip microphotograph of the rail-to-rail DDA.](image)

Fig. 3.14 shows the simulated class AB operation of the DDA output stage with $1K\Omega$ load. We can see that almost from rail to rail, neither Mo1 nor Mo2 output transistor is turned off, so this will increase the operating speed. The measured output current of the DDA in the unity-gain configuration with $1K\Omega$ load is shown in Fig. 3.15. One can see that the output current curve in Fig. 3.15 can be obtained from the subtraction of the two curves in Fig. 3.14, so the measurement result is very close to the simulation.

The simulated input transconductance of the DDA is shown in Fig. 3.16. The transconductance is fairly constant and the variation is only about 7% for common-mode voltages between 0.1 V to 3 V. A rail-to-rail constant-$g_m$ input stage of the DDA is thus achieved. Because of the constant input transconductance, the unity-gain frequency of the DDA will also be constant from rail to rail. The unity-gain
Table 3.2: The transistor sizes of the V-I converter in the DDA input stage.

<table>
<thead>
<tr>
<th>Transistor</th>
<th>W/L (μm/μm)</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1, M2, M3, M4</td>
<td>4/6</td>
<td>N-type V-I Converter</td>
</tr>
<tr>
<td>M5, M6, M7</td>
<td>60/3</td>
<td>cell</td>
</tr>
<tr>
<td>M8, M9, M11, M12, M13 M14</td>
<td>330/1.8</td>
<td></td>
</tr>
<tr>
<td>Mp1, Mp2, Mp3, Mp4</td>
<td>9.6/6</td>
<td>P-type V-I Converter</td>
</tr>
<tr>
<td>Mp5, Mp6, Mp7</td>
<td>20.4/3</td>
<td>cell</td>
</tr>
<tr>
<td>Mp8, Mp9, Mp11, Mp12, Mp13 Mp14</td>
<td>110.4/1.8</td>
<td></td>
</tr>
<tr>
<td>Mp11, Mp12</td>
<td>60/6</td>
<td>Maximum-current</td>
</tr>
<tr>
<td>Mn 14, Mn15, Mn16, Mn17, Mn18</td>
<td>20.4/3</td>
<td>selecting circuit</td>
</tr>
<tr>
<td>MO1, MO2</td>
<td>20.4/3</td>
<td>output stage</td>
</tr>
</tbody>
</table>

Table 3.3: The transistor sizes of the DDA output stage.

<table>
<thead>
<tr>
<th>Transistor</th>
<th>W/L (μm/μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M5, M6, M7</td>
<td>30/2</td>
</tr>
<tr>
<td>M8, M9, M11, M12, M13 M14</td>
<td>60/2</td>
</tr>
<tr>
<td>M15, M16, M17, M18</td>
<td>20/2</td>
</tr>
<tr>
<td>MO1</td>
<td>480/2</td>
</tr>
<tr>
<td>M02</td>
<td>120/2</td>
</tr>
</tbody>
</table>

frequencies of the DDA with $C_L = 30pF$ at various common-mode voltages are shown in Fig. 3.17. They are changed from about 800 KHz to 1.1 MHz. Some of the DDA parameters are summarized in Table 3.4. The simulated power consumption at 1.5 V common-mode voltage is about 0.92 mW.

A DDA-based adder/subtractor circuit is shown in Fig. 3.18. Using Eq. (3.13), we have
Note that there are no additional component required and the high input impedances are still maintained. Several functions can be realized by this circuit. For instance, when $V_1$ and $V_2$ are connected together as inputs and $V_3$ is grounded, this circuit becomes a doubler. Similarly, a voltage follower, an inverter, a divider, a level shifter, and a voltage subtracter can be implemented by this circuit. Fig. 3.19 shows the simulated I/O curves for the DDA-based follower, inverter, doubler, and divider. In the follower case, when $V_1$ is connected as the input and $V_2$ and $V_3$ are grounded, the output voltage range of this DDA can be measured as its common-mode range. The common-mode range of the DDA is from 0.01 V to 3 V, almost rail-to-rail. Fig. 3.20 shows the offset voltages of two DDA input pairs.
The Total Harmonic Distortion (THD) was measured in the voltage follower configuration with 1KΩ load. Fig. 3.21 and 3.22 show the THD results measured by 1 KHz input signals. In Fig. 3.21, the THD numbers were obtained when a 0.8V_{pp} sinusoidal signal is applied to the DDA and the input common-mode voltage is changed. Fig. 3.22 shows the results when the common-mode voltage is 1.5 V and the amplitude of the input signal is increased. We can see that the linearity of the DDA is very good and that the THD is less than

Fig. 3.23 illustrates a DDA-based differential integrator [38] [40]. In this configuration, only a single capacitor and a single resistor are needed, so there are no component matching problems as in the case of the Op-amp-based integrator. By using Eq.( 3.13), the output voltage is given by

\[ V_o = \frac{V_1 - V_2}{sRC} \]  

(3.15)
Figure 3.16: The constant rail-to-rail input transconductance of the DDA.

With $R = 100M\Omega$ and $C = 2.2nF$, the frequency responses of the integrator at various common-mode voltages are shown in Fig. 3.24. The frequency responses are very close. The integrator is operated from rail to rail.

Fig. 3.25 illustrates a DDA-based resonator filter using the integrator of Fig. 3.23 as a building block [38] [40]. This DDA-based circuit consists of two DDAs to implement the filters, a lossy integrator and a lossless integrator. However, for an Op-Amp-based resonator filter, which has the same functions as Fig. 3.25, it needs a lossy integrator, a lossless integrator, and an inverter, as shown in Fig. 3.26. One can see that the Op-Amp-based circuit is even more complicated, needs more components, and component matching is required as well. Assume that DDAs in Fig. 3.25 are ideal, the transfer functions of the bandpass and lowpass filters are given by

$$\frac{V_{BP}}{V_{in}} = \frac{s^2}{s^2 + \frac{1}{R_3C_1}s + \frac{1}{R_1R_2C_1C_2}}$$

(3.16)
Figure 3.17: The unity-gain frequencies of the DDA with $C_L = 30pF$ at various common-mode voltages.

\[ V_{\text{cm}}(V) \]

\[ \frac{V_{\text{LP}}}{V_{\text{in}}} = \frac{1}{s^2 + \frac{1}{R_1 R_3 C_1 C_2} + \frac{1}{R_2 C_1 C_2}} \]  \hspace{1cm} (3.17)

\[ w_n = 1/\sqrt{R_1 R_2 C_1 C_2} \] and \[ Q = R_3 \sqrt{C_1 / R_1 R_2 C_2}. \] With $R_1 = R_2 = R_3 = 100K\Omega$ and $C_1 = C_2 = 2.2nF$, the measured frequency responses for the bandpass and lowpass filters at various common-mode voltages are shown in Fig. 3.27 and 3.28, respectively. These filters work well from rail to rail.

Figure 3.18: The DDA-based adder/subtractor.
Parameter | Experimental Results
--- | ---
DC Gain | 72dB@V\text{cm} = 0.5V
| 70dB@V\text{cm} = 1.5V
| 69dB@V\text{cm} = 2.5V
Unity-Gain Frequency | 0.8MHz@V\text{cm} = 0.5V
| 1.1MHz@V\text{cm} = 1.5V
| 0.85MHz@V\text{cm} = 2.5V
Slew Rate | 2.6V/\mu s@V\text{cm} = 0.5V
| 3.2V/\mu s@V\text{cm} = 1.5V
| 2.8V/\mu s@V\text{cm} = 2.5V
Settling Time | 2.7\mu s@V\text{cm} = 0.5V
| 2.3\mu s@V\text{cm} = 0.5V
| 2.7\mu s@V\text{cm} = 0.5V
Common-Mode Range | 0.01V - 3V
Output Swing | 0.02V - 3.02V

Table 3.4: Summary of the DDA parameters.

In addition to the integrator and filters, DDA can also be applied to make a multiplier/modulator, A/D and D/A converters [40]. With the ability of rail-to-rail operation, the application circuits can have the entire rail input operating voltage, too.

DDA-based circuits can be realized with low component count and without component matching external to the DDA, which, however, is a requirement in almost all Op-Amp-based circuits. Therefore, DDA-based analog circuits provide a competitive design choice to Op-Amp-based circuits.
Figure 3.19: The simulated I/O curves for the DDA-based voltage follower, inverter, doubler, and divider.

Figure 3.20: The offset voltages of the DDA inputs.
Figure 3.21: Measured THD of the DDA as a function of the input common-mode voltage.

Figure 3.22: Measured THD of the DDA as a function of the input AC small signal.
Figure 3.23: The DDA-based integrator.

Figure 3.24: The frequency responses of the DDA-based integrator at various common-mode voltages.

Figure 3.25: DDA-based resonator filter.
Figure 3.26: Op-Amp-based resonator filter.

Figure 3.27: The frequency responses of the DDA-based bandpass filter at various common-mode voltages.
Figure 3.28: The frequency responses of the DDA-based lowpass filter at various common-mode voltages.
CHAPTER 4

LOW-VOLTAGE GM-C FILTER WITH RAIL-TO-RAIL COMMON-MODE VOLTAGE

This chapter presents a CMOS design of a low-voltage 5th-order elliptic low-pass GM-C filter with rail-to-rail common-mode input voltage [41]. The Operational Transconductance Amplifier (OTA) inside this filter is a low-voltage rail-to-rail V-I converter, introduced in Chapter 2. Because all the OTAs inside this filter have rail-to-rail common-mode input voltages, thus we can obtain the resultant filter also with a rail-to-rail common-mode voltage. The 5th-order elliptic low-pass GM-C filter operates at a supply voltage of 3V and has a cutoff frequency of 320 KHz. This filter was designed for application in the baseband mobile/wireless communication.

4.1 Low-Voltage Rail-To-Rail V-I Converter

A low-voltage rail-to-rail V-I converter, shown in Fig. 2.8 in Chapter 2, is used to be an OTA in the design of the 5th-order elliptic low-pass GM-C filter. In this V-I converter, the cancelation of the second order harmonic does not depend on balanced inputs, so fully-balanced inputs are not required. The rail-to-rail operation of the V-I converter is achieved by Approach I in Chapter 2, that is, the inclusion of a parallel
connection of an N-type and a P-type converter cells and two maximum-current selecting circuits.

Figure 4.1: The measured DC transfer curves of the Approach-I V-I converter, which does not require fully-balanced inputs, at $V_a = 0.5\,\text{V}$ with $I_C = 3\mu\text{A}$, $5\mu\text{A}$, and $7\mu\text{A}$, respectively.

In Chapter 2, Fig. 2.16 and 2.17 show the DC transfer curves of the V-I converter when $V_2 = 1.5\,\text{V}$. Fig. 4.1 and 4.2 also show its V-I transfer curves, but with $V_2 = 0.5\,\text{V}$ and $2.5\,\text{V}$, respectively. From the comparison of Fig. 2.16, 4.1, and 4.2, one can see that no matter which bias current is used, the output current at $V_2 = 0.5\,\text{V}$ and $2.5\,\text{V}$ is always larger than that at $V_2 = 1.5\,\text{V}$. This is due to the body effect of transistors, which results from the nonzero source to bulk voltage ($V_{SB}$) which widens the depletion region between the source and bulk and thus increases the absolute value
of the threshold voltage. The threshold voltage, depending on $V_{SB}$, is given by

$$V_{Tn} = V_{Tno} + \gamma(\sqrt{2|\phi_F| + V_{SB}} - \sqrt{2|\phi_F|}) \quad \text{for NMOS} \quad (4.1)$$

$$V_{Tp} = V_{Tpo} - \gamma(\sqrt{2|\phi_F| + V_{BS}} - \sqrt{2|\phi_F|}) \quad \text{for PMOS} \quad (4.2)$$

where $2|\phi_F|$ is the potential required for strong inversion and $\gamma$ is the body effect parameter. We can see that for this V-I converter, as the input common-mode voltage approaches both rails from the mid-rail of the power supply voltage, the absolute value of the input NMOS/PMOS threshold voltage will be decreasing because $V_{SB}/V_{BS}$ is decreased. The smaller the absolute value of the threshold voltage is, the larger the current flows. Therefore, the output current of this V-I converter at $V_{cm} = 0.5\,V$ and $2.5\,V$ is larger than that at $V_{cm} = 1.5\,V$. Because of this reason, later in this chapter,
in the Simulation and Experimental Results of the 5th-Order Elliptic Low-Pass GM-C Filter, we will find that the cutoff frequency of the filter is a little shifted when the common-mode voltage is changed.

### 4.2 5th-Order Elliptic Low-Pass GM-C Filter

The 5th-order elliptic low-pass filter design is initialized by a standard 5th-order elliptic low-pass LC-ladder prototype. From the LC-ladder prototype, through the use of element replacement or signal-flow graph method [42], the 5th order elliptic low-pass GM-C filter, which consists of 7 OTAs and 7 capacitors, including two floating capacitors, is obtained. The final GM-C filter implementation is shown in Fig. 4.3 [43]. Because this OTA has a rail-to-rail common-mode input voltage, the resultant filter also has a rail-to-rail common-mode input voltage, which is quite significant when the supply voltage keeps decreasing. It is also important to note that at the system level, this rail-to-rail property will allow the use of the filter at different locations in the system having different DC common-mode input levels, thus conveniently avoiding the need for DC level shifting.

The cutoff frequency of the GM-C filter is proportional to $I/C$, i.e., $g_m/C$, where $I$ and $g_m$ are the output current and the transconductance of the OTA, respectively, and $C$ is the capacitance. The goal of this filter is to have a cutoff frequency of 500 KHz. In order to have a reasonable value of capacitance, that is, to have a single-chip solution for this filter, a transconductance of $35\mu S$ ($I_C = 5\mu A$) is designed for these OTAs. Thus, according to this transconductance value, all the required capacitor values, implemented in layout, are given by
Figure 4.3: A 5th-order elliptic low-pass GM-C filter.

\[
\begin{align*}
C_1 &= 14.0705\text{pF} & C_2 &= 0.5711\text{pF} \quad (4.3) \\
C_3 &= 17.5708\text{pF} & C_4 &= 1.9700\text{pF} \quad (4.4) \\
C_5 &= 8.9463\text{pF} & C_{L2} &= 24.0855\text{pF} \quad (4.5) \\
C_{L4} &= 15.2089\text{pF} \\ 
\end{align*}
\]

We can see that the maximum capacitance is only about 24pF. Note that if a MOS OTA operating in the weak inversion is used, a \( g_m \)-C filter operating at very low frequencies, <100Hz, for medical applications can be implemented on a single chip (Chapter 6) [44]. In this case \( g_m \propto I \). \( I \) is in the nA range and capacitor values used will be < 50pF allowing a single chip design at very low frequencies.
4.3 Experimental Results

The filter was fabricated in the 1.2\textmu m CMOS process of AMS in Austria. The chip microphotograph of this filter is shown in Fig. 4.4. It occupies 1.62mm\textsuperscript{2} area. All of the measurements and simulations were done with a single DC supply of 3V. The transistor sizes inside each OTA are exactly the same as those of the rail-to-rail V-I converter requiring no fully-balanced inputs, shown in Table 2.2.

![Chip Microphotograph of the Rail-to-Rail GM-C Low-Pass Filter](image)

Figure 4.4: The chip microphotograph of the rail-to-rail GM-C low-pass filter.

The HSPICE simulation results of the filter is shown in Fig. 4.5 and 4.6. We can see that the cutoff frequency of the low-pass filter is 500 KHz and that the transfer function of this filter is almost the same from 0V to 3V.

Fig. 4.7 and 4.8 illustrate the measurement results of this filter for different common-mode voltages, using \( I_C = 5\mu A \). As designed, the cutoff frequency should be 500 KHz. From the measurement, the cutoff frequency at the common-mode voltage of 0.5V, 1.0V, 1.5V, 2.0V, and 2.5V are around 340 KHz, 320 KHz, 310 KHz, 340 KHz, and 340 KHz, respectively. This deviation in the cutoff frequency is expected in light of the fact that no automatic tuning scheme was used to compensate

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Figure 4.5: The simulation results of the low-pass filter with the common mode voltage at 0V, 0.5V, 1V, and 1.5V, respectively.

for random process variations. The measured -3 dB frequency of the OTA is about 5 MHz, but its simulated -3 dB frequency is 9 MHz. This reduced bandwidth results in an increase of unwanted phase lag around two-integrator loops in the filter. This, in turn, results in Q-enhancement effects which cause an increase in the passband ripples. Well-known compensation techniques can be used to mitigate such effects and restore the frequency response close to the ideal. One such technique [45] is to use resistors, which can be built with MOSFETs operating in triode region, in series with the filter's capacitors to produce compensating phase lead. Fortunately, it has been shown [46] that compensation of only the middle two-integrator loops in the filter structure would significantly reduce Q-enhancement effects. In the filter structure, this can be done using a single compensating resistor in series with $C_3$. 78
This was verified by simulation and applied in the design of weak-inversion GM-C filters in Chapter 6. In this case a MOSFET in triode region is used with its gate voltage adjusted, through automatic tuning, to provide the proper amount of phase lead. The nonlinearities contributed by the MOSFET are practically negligible since its $V_{ds}$ is very small. The process variation behind the smaller cutoff frequencies can be confirmed with the results in Chapter 6, where all the filter cutoff frequencies are measured to be smaller as well.

As discussed in Section 4.1, the output current of the V-I converter, utilized as the OTA inside this filter, is increased when the input common-mode voltage approaches both rails from the mid-rail of the supply voltage. When the output current, or say the output transconductance, is increased, the cutoff frequency of the filter is increased.
accordingly. This explains the small shift of the measured cutoff frequencies when the common-mode voltage is changed. Using 5μA bias current, this filter consumes 2.48mW DC power consumption when the common mode input voltage is 1.5V.

![Graph showing measured results of the low-pass filter](image)

**Figure 4.7:** The measured results of the low-pass filter with the common mode voltage at 0.5V, 1V, and 1.5V, respectively.

The total in-band output noise was measured to be 180μV, 160μV, 190μV, 180μV, and 180μVrms for \( V_{CM} = 0.5V, 1V, 1.5V, 2V, \) and 2.5V, respectively. The noise spectrum at \( V_{CM} = 2V \) is shown in Fig. 4.9. This, combined with 1% THD for 1.4\( V_{pp} \), 0.9\( V_{pp} \), 0.6\( V_{pp} \), 1.4\( V_{pp} \), 1.2\( V_{pp} \) input at one-third of the respective measured cutoff frequencies (with 0.5 dc gain), results in 63 dB, 60 dB, 55 dB, 63 dB, and 61 dB dynamic range for \( V_{CM} = 0.5V, 1V, 1.5V, 2V, \) and 2.5V, respectively. The PSRR results at \( V_{CM} = 2V \) are shown in Fig. 4.10 and 4.11. These PSRR - \( V_{DD} \)
and PSRR - $V_{SS}$ are somewhat similar because both NMOS and PMOS devices are used for OTA signal inputs.

The transfer function of this filter can be manually tuned by changing the $I_C$ bias current of the OTA transconductance. Fig. 4.12 and 4.13 show the measured results of the low-pass filter with $I_C = 3\mu A$ and $7\mu A$, respectively. As expected, the cutoff frequency of the filter becomes smaller/larger when the bias current is decreased/increased. For $I_C = 3\mu A$, the cutoff frequency at the common-mode voltage of 0.5V, 1.5V, and 2.5V are 310 KHz, 280 KHz, and 300 KHz, respectively. For $I_C = 7\mu A$, the cutoff frequency at the common-mode voltage of 0.5V, 1.5V, and 2.5V are about 400 KHz, 340 KHz, and 405 KHz, respectively.
Notice that from all the measured filter frequency responses, the stopband attenuation, about 35 to 40dB, is low compared with the 60dB attenuation in the simulation results. The reason behind this is due to the long analog-ground metal wire in the physical layout. It results in distributed parasitic resistance between the capacitors and the analog ground, as illustrated in Fig. 4.14. The resistors $R_1 - R_{agnd}$ do not affect the low-frequency performance too much because of the dominance of capacitors, but at higher frequencies, circuit performance will be strongly degraded by these parasitic resistors because the capacitors will have low impedance levels. Thus, the passband of the filter is not altered by the resistance and the stopband becomes quite different. Simulations were performed to support this argument. For simplicity, assume that $R_1 = R_2 = R_3 = R_4 = 0$. Fig. 4.15 and 4.16 show the simulated frequency responses of the low-pass filter with $R_{agnd} = 100\Omega$ and $300\Omega$, respectively, at different
common-mode voltages. We can see that when $R_{agnd} = 100\Omega$, the stopband attenuation becomes 40dB and when $R_{agnd}$ is only 300Ω, the stopband attenuation even becomes less than 35dB. The change of the stopband attenuation can be seen more clearly from Fig. 4.17, which compares the simulation results of the low-pass filter with $R_{agnd} = 0$, 100Ω, and 300Ω at the common-mode voltage of 1.5V. The resistive analog-ground wire really contributes to the small attenuation of the filter stopband.

A basic way to solve this problem is, of course, to have a careful layout to produce a very short analog-ground metal wire. An advanced solution is to layout a wider analog-ground rectangular area, instead of a thin line, so that the resultant resistance becomes smaller and also to insert a simple buffer, as shown in Fig. 4.18, such that the impedance at the analog-ground point will be very low. The analog ground voltage
Figure 4.11: The PSRR - $V_{SS}$ of the GM-C low-pass filter.

can then be inputed from the positive terminal of the buffer off chip or by using a voltage divider to provide the analog ground directly on chip [47].
Figure 4.12: The measured results of the low-pass filter with $I_C = 3\mu A$ and the common mode voltage at $0.5V$, $1.5V$, and $2.5V$, respectively.

Figure 4.13: The measured results of the low-pass filter with $I_C = 7\mu A$ and the common mode voltage at $0.5V$, $1.5V$, and $2.5V$, respectively.
Figure 4.14: A possible layout extraction of part of the 5th-order elliptic low-pass GM-C filter.

Figure 4.15: The simulation results of the low-pass filter with $R_{agnd} = 100\Omega$ at different common-mode voltages.
Figure 4.16: The simulation results of the low-pass filter with $R_{agnd} = 300\Omega$ at different common-mode voltages.

Figure 4.17: The simulation results of the low-pass filter with $R_{agnd} = 0$, 100\,$\Omega$, and 300\,$\Omega$ at the common-mode voltage of 1.5\,V.
Figure 4.18: A solution to the resistive analog ground in the layout and design of the 5th-order elliptic low-pass GM-C filter.
CHAPTER 5

LOW-VOLTAGE UNIVERSAL V-I CONVERTER AND MULTIPLIER STRUCTURES

In this chapter, a V-I converter and a multiplier structures [48], which can work in either the weak-inversion or the strong-inversion saturation region, are described. When the V-I converter and multiplier operate in the weak-inversion region, micro-power dissipation is expected. As one will see later, if the resistance value, given by the active resistor circuits inside the V-I converter and multiplier, is tuned down to certain value, the V-I converter and multiplier is able to work in the strong-inversion saturation region. CMOS implementations of two different sets of the V-I converter and multiplier were fabricated to prove these circuit structures’ universality in operation regions.

5.1 Weak-Inversion Operation

Low-voltage circuit design with emphasis on low power consumption presents a major challenge for circuit designers. With the drive to low power operation, circuits which work in the weak-inversion region have become more popular [49] [50]. However, in addition to the low-power consumption, a large input signal swing is also necessary for a V-I converter and a multiplier. Here, the weak-inversion operation of
a V-I converter and a multiplier is discussed. Because of their low power consumption and large signal ranges, they are suitable to be used in the large transconductor- or multiplier-based analog VLSI circuits, such as the cellular neural network implementation proposed in [28] and [51]. The V-I converter and multiplier can also be used as a basic building block to construct low-voltage, micropower analog VLSI signal processing systems.

5.1.1 V-I Converter

For a MOS transistor working in the weak-inversion region with $v_{DS}$ larger than a few times $U_T$, its current equation is given by

$$I_D = \frac{W}{L} I_{D0} \exp\left(\frac{v_{GS}}{nU_T}\right)$$

(5.1)

where $W$ and $L$ are the width and length of the transistor, respectively, $I_{D0}$ is reverse voltage saturation current, $n$ is the subthreshold slope factor, and $U_T = KT/q$ is the thermal voltage. The exponential relationship between the drain current and the gate-source voltage is similar to that between the emitter current and the base-emitter voltage of a bipolar transistor. For a small signal, a differential pair can produce a linear voltage-to-current relation. However, in order to have a large linear range, the technique used to linearize bipolar transistors’ voltage-to-current relations by B. Gilbert [52] [53] can also be utilized here due to the similar current equations. The input voltage for output transistors should be logarithmically determined first and then through the exponential relationship of Eq. (5.1), the output current is linearized.

Fig. 5.1 [48] shows the circuit diagram of the weak-inversion V-I converter. As shown in this figure, the diode-connected transistors $M_5$ and $M_6$ are driven by the
current sinks $I_1$ and $I_2$. Assume that transistors $M_1 - M_6$ have the same sizes and that the difference between the two input voltages of transistors $M_3$ and $M_4$ is $V_d$. $V_d$ can be obtained by

$$V_d = nU_T \ln \left( \frac{I_1}{I_2} \right)$$  \hspace{1cm} (5.2)

For currents $I_3$ and $I_4$,

$$\frac{I_3}{I_4} = \exp \left( \frac{V_d}{nU_T} \right)$$  \hspace{1cm} (5.3)

Substituting Eq.( 5.2) into Eq.( 5.3), we can obtain

$$\frac{I_3}{I_4} = \frac{I_1}{I_2}$$  \hspace{1cm} (5.4)
Notice that transistors $M_3, M_4, M_5,$ and $M_6$ actually form a translinear loop, which also leads us to Eq.( 5.4). From Eq.( 5.4), we can further obtain

$$\frac{I_3 - I_4}{I_3 + I_4} = \frac{I_1 - I_2}{I_1 + I_2} \quad (5.5)$$

$$I_o = I_3 - I_4 \quad (5.6)$$

$$= \frac{I_3 + I_4}{I_1 + I_2} (I_1 - I_2) \quad (5.7)$$

$$= \frac{I_{C2} I_1 - I_2}{I_{C1}} \quad (5.8)$$

To make sure a linear voltage-to-current conversion is achieved, that is, to achieve the linear relation between $(I_1 - I_2)$ and $(V_1 - V_2)$, it is necessary that a resistor $R_{eq}$ is connected between the source terminals of transistors $M_1$ and $M_2$. The resistor is required to be much larger than $U_T/I_{C1}$ so that

$$\frac{I_1 - I_2}{2} R_{eq} = V_1 - V_2 \quad (5.9)$$

$$I_{C1} = \frac{I_1 + I_2}{2} \quad (5.10)$$

Thus,

$$I_o = \frac{I_{C2} V_1 - V_2}{R_{eq}} \quad (5.11)$$

From Eq.( 5.11), we can see that the output current can be tuned by the resistor or the two DC bias currents $I_{C1}$ and $I_{C2}$.

Because of the nA level of the weak-inversion operating current $I_{C1}$, in order to have the resistor much larger than $U_T/I_{C1}$, we need a very large equivalent resistor here. The resistor $R_{eq}$ in Fig. 5.1 is actively built by 6 transistors, as shown in Fig. 5.2 [54] [55]. In Fig. 5.2, all transistors are operating in the strong-inversion region with transistors $M_{23}$ and $M_{24}$ operating in the triode region. The equivalent resistance
between $V_{R1}$ and $V_{R2}$ is given approximately by [55]

$$R_{eq} = \frac{2}{K(V_b - V_T)}$$  \hspace{1cm} (5.12)

![Equivalent Resistor Circuit](image)

Figure 5.2: The equivalent resistor circuit.

Transistors $M_{23}$ and $M_{24}$ are sized rather long to have large equivalent resistance, as we can see from Eq. (5.12). The longer the transistors are, the smaller the $K$ is, and the larger the equivalent resistor, $R_{eq}$ will be. Also, to ensure low power consumption for transistors $M_{21}$, $M_{22}$, $M_{25}$, and $M_{26}$ in the strong-inversion region, these four transistors are chosen to be a little long to adjust the flowing current to the nA level.

Finally, combining Eq. (5.11) and (5.12), it is very clear that a linear voltage to current relation is obtained. The output current can be tuned by the two DC bias currents $I_{C1}$ and $I_{C2}$ and also the bias voltage, $V_b$, for the active resistor.

Note that the transistor $M_9$ and the bias voltage $V_{B1}$ in the output stage are used to cancel the $\lambda$ effect (channel-length modulation effect) from the current mirror $M_7$ and $M_8$ because of their different $V_{DS}$ drops, so that the output offset current can be
minimized. Due to the fact that the current level in the weak-inversion region is so small, minimizing the output offset current is very crucial.

5.1.2 Multiplier

Based on the V-I converter structure, one more differential pair is parallely added into the second stage, and then a multiplier can be obtained [48] [56] [53], as shown in Fig. 5.3.

![Figure 5.3: The universal multiplier structure.](image)

Basically, it applies the same principles as the V-I converter: to linearize the exponential drain current with respect to the gate-source voltage, the voltage is logarithmically predetermined [52]. In addition, to obtain the multiplying function here,
two cross-couple differential pairs are necessary to be driven by the logarithmic voltage signal. In fact, the structure of the cross-couple differential pairs is the same idea as the parallel connection of two N-type V-I converters to achieve the N-type multiplier structure, described in Chapter 3. The expression of the differential output current of the weak-inversion multiplier is derived as follows [53].

As referring to Fig. 5.3,

\[ \frac{I_1}{I_2} = \exp\left(\frac{V_d}{nU_T}\right) \]  
\[ I_1 - I_2 = (I_1 + I_2) \tanh\left(\frac{V_d}{2nU_T}\right) \]  

For currents \( I_1, I_2, I_5, I_6, I_7, \) and \( I_8, \) similar current ratio relation, like Eq. (5.13), can be obtained, as derived from Eq.( 5.2) to Eq.( 5.4) in the V-I converter case,

\[ \frac{I_1}{I_2} = \frac{I_6}{I_8} = \frac{I_5}{I_7} \]  

From Eq ( 5.14) and ( 5.15),

\[ I_6 - I_8 = I_3 \tanh\left(\frac{V_d}{2nU_T}\right) \]  
\[ I_5 - I_7 = I_4 \tanh\left(\frac{V_d}{2nU_T}\right) \]  

The differential output current \( I_o \) is given by

\[ I_o = I_{L1} - I_{L2} \]
\[ = (I_6 + I_7) - (I_5 + I_8) \]
\[ = (I_6 - I_8) - (I_5 - I_7) \]
\[ = I_3 \tanh\left(\frac{V_d}{2nU_T}\right) - I_4 \tanh\left(\frac{V_d}{2nU_T}\right) \]
\[ = (I_3 - I_4) \tanh\left(\frac{V_d}{2nU_T}\right) \]
\[ = (I_3 - I_4) \frac{I_1 - I_2}{I_1 + I_2} \]
Similarly, as the V-I converter case, two equivalent resistor circuits $R_{eqx}$ and $R_{eqy}$ are used to converter the linear relation between $(I_1 - I_2)$ and $(V_{x1} - V_{x2})$ and also between $(I_3 - I_4)$ and $(V_{y1} - V_{y2})$ with the limitations of $R_{eqx} \gg U_T/I_{C1}$ and $R_{eqy} \gg U_T/I_{C2}$. The same circuit, as shown in Fig. 5.2, is utilized to actively build the resistor circuit, with its resistance value given by Eq.( 5.12). Because of

$$\frac{I_1 - I_2}{2} R_{eqx} = V_{x1} - V_{x2} \quad (5.24)$$

$$\frac{I_3 - I_4}{2} R_{eqy} = V_{y1} - V_{y2} \quad (5.25)$$

we can obtain

$$I_o = \frac{2}{I_{C1}R_{eqx}R_{eqy}}(V_{x1} - V_{x2})(V_{y1} - V_{y2}) \quad (5.26)$$

Here is the weak-inversion multiplier circuit. The two resistor circuits $R_{eqx}$ and $R_{eqy}$ actually have the same transistor sizes as $R_{eq}$ in the weak-inversion V-I converter. For simplicity, $I_{C2}$ is set to be the same as $I_{C1}$ in fabrication and thus once $R_{eqx} \gg U_T/I_{C1}$ is satisfied, $R_{eqy} \gg U_T/I_{C2}$ is satisfied, too.

### 5.1.3 Experimental Results

In this section, we discuss the experimental results.

#### V-I Converter

The weak-inversion V-I converter was fabricated in the 1.2$m\mu$m CMOS process of AMS, having $V_{Tn} = 0.736V$ and $V_{Tp} = -0.751V$, in Austria. The chip microphotograph of the V-I converter is shown in Fig. 5.4. It occupies 0.176mm$^2$ area. The power supply used is a single 3V supply voltage. The transistor sizes of the V-I converter are illustrated in Table 5.1.
Figure 5.4: The chip microphotograph of the weak-inversion V-I converter.

<table>
<thead>
<tr>
<th>Transistor</th>
<th>W/L (μm/μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1, M2, M3, M4, M5, M6</td>
<td>15/3</td>
</tr>
<tr>
<td>M7, M8, M9</td>
<td>90/12</td>
</tr>
</tbody>
</table>

Table 5.1: The transistor sizes of the universal V-I converter.

From Section 5.1, one knows that the output current of the V-I converter can be changed by the two DC bias currents $I_{C1}$ and $I_{C2}$. In the measurement, different V-I transfer curves were obtained by changing these two currents. Fig. 5.5 and 5.6 show the measured results. These results were obtained when $V_2$ was set to be 1.2V. Simulation also shows when $I_{C1} = I_{C2} = 40nA$ and $V_2 = 1.2V$, the DC power dissipation is about $0.55μW$. 

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Figure 5.5: The measurement results of the weak-inversion V-I converter by changing both currents $I_{C1}$ and $I_{C2}$.

Multiplier

The weak-inversion multiplier was fabricated in the 1.2$\mu$m CMOS process of AMS, having $V_{TN} = 0.736V$ and $V_{TP} = -0.751V$, in Austria. The chip microphotograph of the multiplier is shown in Fig. 5.7. It occupies 0.356$mm^2$ area. The power supply is a single 3V supply voltage. The transistor sizes of the multiplier are illustrated in Table 5.2.

From Eq. (5.26) in Section 5.1,

$$I_o = \frac{2}{I_{C1} R_{eqz} R_{eqy}} (V_{x1} - V_{x2})(V_{y1} - V_{y2})$$

(5.27)
Figure 5.6: The measurement results of the weak-inversion V-I converter by changing both currents $I_{C1}$ and $I_{C2}$.

$R_{eqx}$ and $R_{eqy}$ were already fixed in the fabrication process. In the measurement, $I_{C1}$ was also fixed to be 20 nA. Then, we can change $(V_{x1} - V_{x2})$ and $(V_{y1} - V_{y2})$ to see the multiplying function of this circuit.

Fig. 5.8 and 5.9 show the measured DC transfer curves of the multiplier. In Fig. 5.8, the horizontal axis represents the differential input voltage $(V_{x1} - V_{x2})$ and the vertical axis is the output current. The curves were obtained by sweeping $(V_{x1} - V_{x2})$ from -0.4V to 0.4V, while varying $(V_{y1} - V_{y2})$ from -0.6V to 0.6V with a step of 0.2V. For Fig. 5.9, the horizontal axis represents the differential input voltage $(V_{y1} - V_{y2})$. These curves were obtained by sweeping $(V_{y1} - V_{y2})$ from -0.7V to 0.7V, while varying $(V_{x1} - V_{x2})$ from -0.4V to 0.4V with a step of 0.1V. We can see that the input
Figure 5.7: The chip microphotograph of the weak-inversion multiplier.

<table>
<thead>
<tr>
<th>Transistor</th>
<th>W/L (μm/μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1, M2, M5, M6</td>
<td></td>
</tr>
<tr>
<td>M7, M8, M11, M12</td>
<td>15/3</td>
</tr>
<tr>
<td>M3, M4</td>
<td>30/3</td>
</tr>
<tr>
<td>M9, M10, M15</td>
<td>180/12</td>
</tr>
</tbody>
</table>

Table 5.2: The transistor sizes of the universal multiplier.

signal swings of the multiplier are $0.8V_{PP}$ and $1.4V_{PP}$ for $(V_{z1} - V_{z2})$ and $(V_{y1} - V_{y2})$, respectively.

5.2 Strong-Inversion Saturation Operation

In this section, we describe the same V-I converter and multiplier structures as stated in the last section, but operating in the strong-inversion saturation region.

5.2.1 V-I Converter

Certainly, in this subsection, all the transistors in Fig. 5.1 are assumed to operate in the strong-inversion region. Starting from $V_{z1}$ and $V_{z2}$ in Fig. 5.1,

$$V_{z1} - V_{z2} = (V_{DD} - V_{gs5}) - (V_{DD} - V_{gs6}) = V_{gs6} - V_{gs5} \quad (5.28)$$

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Figure 5.8: The measured output current of the weak-inversion multiplier for sweeping \((V_{x1} - V_{x2})\) from -0.4V to 0.4V, while varying \((V_{y1} - V_{y2})\) from -0.6V to 0.6V with the step of 0.2V.

The same assumption is made as in the last section, transistors \(M_1 - M_6\) have the same sizes. Because the same current \(I_1\) flows through transistors \(M_1\) and \(M_5\), and the same current \(I_2\) also flows through transistors \(M_2\) and \(M_6\), respectively,

\[
(V_{g5} - V_T)^2 = (V_{g1} - V_T)^2 = (V_1 - V_{g1} - V_T)^2 \tag{5.29}
\]
\[
(V_{g6} - V_T)^2 = (V_{g2} - V_T)^2 = (V_2 - V_{g2} - V_T)^2 \tag{5.30}
\]
\[
V_{g5} = V_{g1} = V_1 - V_{s1} \tag{5.31}
\]
\[
V_{g6} = V_{g2} = V_2 - V_{s2} \tag{5.32}
\]
Figure 5.9: The measured output current of the weak-inversion multiplier for sweeping \((V_{y1} - V_{y2})\) from -0.7V to 0.7V, while varying \((V_{x1} - V_{x2})\) from -0.4V to 0.4V with the step of 0.1V.

From Eq. (5.28), (5.31), and (5.32), assume \(I_1 > I_2\) and that the current flowing through \(R_{eq}\) is \(\Delta I\),

\[
V_{z1} - V_{z2} = (V_2 - V_{s2}) - (V_1 - V_{s1})
\]

\[
= (V_2 - V_1) - (V_{s2} - V_{s1})
\]

\[
= (V_2 - V_1) + R_{eq}\Delta I
\]

And

\[
V_1 - V_2 = (V_{x2} - V_{x1}) + R_{eq}\Delta I
\]

For currents \(I_1\) and \(I_2\), obviously, one can see

\[
I_1 = I_{C1} + \Delta I = \frac{K}{2}(V_{gs1} - V_T)^2
\]
\[ I_2 = I_{C1} - \Delta I = \frac{K}{2} (V_{gs2} - V_T)^2 \]  

Thus,

\[ V_{gs1} = \sqrt{\frac{2(I_{C1} + \Delta I)}{K}} + V_T \]  
\[ V_{gs2} = \sqrt{\frac{2(I_{C1} - \Delta I)}{K}} + V_T \]

Again, from Eq. (5.28), (5.31), and (5.32),

\[ V_{z2} - V_{z1} = V_{gs1} - V_{gs2} \]
\[ = \sqrt{\frac{2}{K}(\sqrt{I_{C1} + \Delta I} - \sqrt{I_{C1} - \Delta I})} \]
\[ = \sqrt{\frac{2I_{C1}}{K} \left( \sqrt{1 + \frac{\Delta I}{I_{C1}}} - \sqrt{1 - \frac{\Delta I}{I_{C1}}} \right)} \]

For \( \Delta I/I_{C1} \ll 1, \Delta I \ll I_{C1}, \)

\[ V_{z2} - V_{z1} = \sqrt{\frac{2I_{C1}}{K} \left[ \left( \frac{1 + \frac{1}{2} \frac{\Delta I}{I_{C1}}} \right) - \left( \frac{1 - \frac{1}{2} \frac{\Delta I}{I_{C1}}} \right) \right]} = \sqrt{\frac{2}{KI_{C1}}} \Delta I \]

Substitute Eq. (5.44) into Eq. (5.36), we obtain

\[ V_1 - V_2 = \sqrt{\frac{2}{KI_{C1}}} \Delta I + R_{eq} \Delta I \]  

Therefore,

\[ \Delta I = \frac{1}{\sqrt{\frac{2}{KI_{C1}} + R_{eq}}} (V_1 - V_2) \]
\[ V_{z2} - V_{z1} = \frac{\sqrt{\frac{2}{KI_{C1}}} (V_1 - V_2)}{\sqrt{\frac{2}{KI_{C1}} + R_{eq}}} \]

Here, \( R_{eq} \) is not the same as the tens of MΩ resistor in the weak-inversion V-I converter. If \( R_{eq} \) is too large, for example, tens of MΩ, \( \Delta I \) will be almost zero. There is no difference between \( V_{z1} \) and \( V_{z2} \) and then there is no current flowing in the output.
either. Therefore, $R_{eq}$ is re-sized from that in the weak-inversion V-I converter. Its value is made to be comparable to $\sqrt{\frac{2}{K I_{C1}}}$ so that the difference of $(V_{z2} - V_{z1})$ is large enough to produce output current.

The output current $I_o$ is obtained by

$$I_o = I_3 - I_4$$

$$= \frac{K}{2} (\Delta V_z) \sqrt{\frac{4I_{C2}}{K} - \Delta V_z^2}$$

where $\Delta V_z = V_{z2} - V_{z1}$. For a small $\Delta V_z$ compared to $\sqrt{4I_{C2}/K}$,

$$I_o \approx \frac{K}{2} (\Delta V_z) \sqrt{\frac{4I_{C2}}{K}}$$

$$= \frac{\sqrt{4I_{C2}}}{\sqrt{K I_{C1}} + R_{eq}} (V_1 - V_2)$$

The transconductance of this V-I converter can also be changed by bias currents $I_{C1}$ and $I_{C2}$, but it is not proportional to $I_{C2}/I_{C1}$ ratio, as in the weak-inversion case.

### 5.2.2 Multiplier

Similarly, in this subsection, all the transistors in Fig. 5.3 are all assumed to operate in the strong-inversion region. Follow the same derivation as that in the strong-inversion V-I converter, one can see in this multiplier case, Eq.( 5.47) becomes

$$V_{z2} - V_{z1} = \frac{\sqrt{\frac{2}{K I_{C1}}}}{\sqrt{\frac{2}{K I_{C1}} + R_{eq}}}(V_{z1} - V_{z2})$$

The output current of this multiplier is given by

$$I_o = I_{L1} - I_{L2}$$

$$= (I_6 + I_7) - (I_5 + I_8)$$

$$= (I_6 - I_8) - (I_5 - I_7)$$

$$= \frac{K}{2} (\Delta V_z) \sqrt{\frac{4I_3}{K} - \Delta V_z^2} - \frac{K}{2} (\Delta V_z) \sqrt{\frac{4I_4}{K} - \Delta V_z^2}$$
where $\Delta V_z = V_{z2} - V_{z1}$. For a small $\Delta V_z$ compared to $\sqrt{4I_3/K}$ and $\sqrt{4I_4/K}$,

$$I_o \approx \frac{K}{2} (\Delta V_z)(\sqrt{\frac{4I_3}{K}} - \sqrt{\frac{4I_4}{K}}) \quad (5.57)$$

$$= \frac{K}{2} (\Delta V_z) \sqrt{2} [(V_{y1} - V_{s3} - V_T) - (V_{y2} - V_{s4} - V_T)] \quad (5.58)$$

$$= \frac{K}{\sqrt{2}} (\Delta V_z) [(V_{y1} - V_{y2}) - (V_{s3} - V_{s4})] \quad (5.59)$$

From the observation of Eq. (5.34) and (5.47), similarly, we know

$$(V_{y1} - V_{y2}) - (V_{s3} - V_{s4}) = \frac{\sqrt{2}}{\sqrt{\frac{K}{I_{C1}}} + R_{eqy}} (V_{y1} - V_{y2}) \quad (5.60)$$

Finally,

$$I_o = \frac{K}{\sqrt{2}} \frac{\sqrt{\frac{2}{K}}}{\sqrt{\frac{2}{K}} + R_{eqy}} \frac{\sqrt{\frac{2}{K}}}{\sqrt{\frac{2}{K}} + R_{eqy}} (V_{x1} - V_{x2})(V_{y1} - V_{y2}) \quad (5.61)$$

This is a multiplier operating in the strong-inversion region.

### 5.2.3 Experimental Results

In this section, we discuss the experimental results of the strong-inversion V-I converter and multiplier.

**V-I Converter**

The V-I converter, working in the strong-inversion saturation region, was fabricated in the 1.2$\mu$m CMOS process of AMS, having $V_{Tn} = 0.736V$ and $V_{Tp} = -0.751V$, in Austria. The chip microphotograph of the V-I converter is shown in Fig. 5.10. It occupies $0.0745mm^2$ area. The utilized power supply is a single 3V supply voltage. The transistor sizes of the V-I converter are exactly the same as those of the weak-inversion V-I converter, as shown in Table 5.1. The only difference between these two circuits is the different-sized equivalent resistor circuit.
From Eq. (5.51) in Section 5.2, we can see that the output current of the V-I converter can be changed by the two DC bias currents $I_{C1}$ and $I_{C2}$. In the physical layout, currents $I_{C1}$ and $I_{C2}$ were set to be the same, so for its measurement, different V-I transfer curves were obtained by changing current $I_{C1}$ only. Fig. 5.11 and 5.12 show the measured results. In Fig. 5.11, a larger transconductance range was obtained by larger $I_{C1}$ bias currents. In Fig. 5.12, smaller $I_{C1}$ currents were used to bias the circuit, so a smaller transconductance range and a smaller input signal swing were expected. The tunable transconductance range is from $1.5\mu S$ to $4\mu S$ or so. Its THD is about 0.71% and 1.05% for 1 KHz $0.8V_{pp}$ and $1.2V_{pp}$ signals, respectively, with $I_{C1} = 30\mu A$.

**Multiplier**

The strong-inversion multiplier was fabricated in the 1.2$\mu m$ CMOS process of AMS, having $V_{Tn} = 0.736V$ and $V_{Tp} = -0.751V$, in Austria. The chip microphotograph of the multiplier is shown in Fig. 5.13. It occupies 0.120$mm^2$ area. The power supply is a single 3.3V supply voltage. The transistor sizes of the multiplier are exactly the same as those of the weak-inversion multiplier, as shown in Table 5.2. The only difference between these two multipliers is the different-sized resistor circuits.
Figure 5.11: The measurement results of the strong-inversion V-I converter with $I_{C1} = 10\mu A$, 15$\mu A$, 20$\mu A$, and 30$\mu A$.

From Eq.(5.61) in Section 5.2, similar to the weak-inversion case, $R_{eqx}$ and $R_{eqy}$ were already fixed in the fabrication process. In the measurement, $I_{C1}$ was also fixed to be 30$\mu A$. We can see its multiplying function by changing $(V_{x1} - V_{x2})$ and $(V_{y1} - V_{y2})$ values.

Fig. 5.14 and 5.15 show the measured DC transfer curves of the multiplier. In Fig. 5.14, the horizontal axis represents the differential input voltage $(V_{x1} - V_{x2})$ and the vertical axis is the output current. The curves were obtained by sweeping $(V_{x1} - V_{x2})$ from -0.3V to 0.3V, while varying $(V_{y1} - V_{y2})$ from -0.4V to 0.4V with a step of 0.1V. For Fig. 5.15, the horizontal axis represents the differential input voltage $(V_{y1} - V_{y2})$. These curves were obtained by sweeping $(V_{y1} - V_{y2})$ from -0.4V to 0.4V, while varying $(V_{x1} - V_{x2})$ from -0.3V to 0.3V with a step of 0.1V. We can see that
the input signal swings of the multiplier are $0.6V_{PP}$ and $0.8V_{PP}$ for $(V_{z1} - V_{z2})$ and $(V_{y1} - V_{y2})$, respectively. One can see that in both figures, the transfer curves are not quite linear. This is because the final multiplying equation, Eq. (5.61), is obtained through lots of approximation during the equation derivation. Certain distortion was already predicted from the theoretical deduction. The THD is about $0.90\%$ and $1.27\%$ for 1 KHz $0.2V_{pp}$ and $0.3V_{pp}$ $(V_{z1} - V_{z2})$ signals when $V_{y2} - V_{y1} = 0.2V$, and $0.98\%$ and $1.62\%$ for 1 KHz $0.2V_{pp}$ and $0.3V_{pp}$ $(V_{y1} - V_{y2})$ signals when $V_{z2} - V_{z1} = 0.2V$. Therefore, if people only need small input voltage ranges for multiplying, this simple circuit is still a good candidate.
Figure 5.12: The measurement results of the strong-inversion V-I converter with $I_{C1} = 4\mu A, 6\mu A, 8\mu A, \text{ and } 10\mu A$.

Figure 5.13: The chip microphotograph of the strong-inversion multiplier.
Figure 5.14: The measured output current of the strong-inversion multiplier for sweeping \((V_{x1} - V_{x2})\) from -0.3V to 0.3V, while varying \((V_{y1} - V_{y2})\) from -0.4V to 0.4V with the step of 0.1V.
Figure 5.15: The measured output current of the strong-inversion multiplier for sweep­ing \((V_{y1} - V_{y2})\) from -0.4V to 0.4V, while varying \((V_{x1} - V_{x2})\) from -0.3V to 0.3V with the step of 0.1V.
Low cutoff frequency filters are very important in the speech signal processing and medical hearing applications. However, there are some problems encountered in these low frequency filter design. The main issue is the large time constant involved and the values of the resistors and capacitors are limited by the silicon area [57]. There are several techniques presented for low frequency filter design. They are capacitance multiplication, current division by using current mirrors, current cancellation, and triode biased transistor [58]. Capacitance multiplication is obtained by using the miller effect [59]. The price for the technique is an additional amplifier. For the method of current division by using current mirrors, current can be largely reduced by using current mirrors with large division factors [59] [60], but a large silicon area is required. Current cancellation uses partial positive feedback in a differential pair OTA connection to reduce the output transconductance [61], so the input signal range will be very small. Some recent works about low frequency filters were reported. The OTA circuit in [58] is based on a triode biased transistor and current division techniques, so a large silicon area can be expected. A 175 Hz sixth-order Butterworth bandpass filter was introduced in [57]. The four transistor integrator was utilized in the work,
so the sensitivity in the transistor mismatch and output thermal noise were increased. Also, the filter occupied a silicon area of 27mm$^2$.

For CMOS transistors, the weak-inversion operation provides not only a low power consumption choice, but also a circuit alternative for audio signal processing [50]. This chapter presents CMOS implementation of two low-voltage, micropower 5th-order elliptic low-pass GM-C filters based on the same architecture [44]. Their cutoff frequency ranges cover 32 Hz to 1 KHz and 1 KHz to 5 KHz, respectively. The techniques used are the nA current level in the MOS weak-inversion region and triode biased transistors. These two filters occupy the silicon areas of 2.73mm$^2$ and 2.59mm$^2$, respectively. Their input signal swings are large in these OTAs, as addressed later. There are no additional requirements for amplifiers or matched transistors inside the filter. The filters can be applied for speech signal processing or used in integrated speech systems, for example, the integrated speech training system [17]. The Operational Transconductance Amplifier (OTA) in these GM-C filter design is implemented by the low-voltage V-I converter working in the weak-inversion region, as described in Chapter 5. The transconductance can be tuned by DC currents or DC voltage. These filters provide a practical means for implementing very large time constants on-chip allowing single-chip solutions at very low frequencies.

6.1 Operational Transconductance Amplifier

6.1.1 Design of the OTA

As mentioned, the OTA here is based on the design of the weak-inversion V-I converter, Fig. 5.1, in Chapter 5. A cascode output stage, which functions as a current multiplier and also increases the output impedance to enhance its driving
capability, is added for the final OTA design. Two different sets of device sizes for the output stage are used to yield two different designs of the OTA. Their current multiplying constants are 1 and 10, respectively. Fig. 6.1 shows the circuit diagram of the weak-inversion OTA.

\[ V_{DD} \]

\[ M_{03} \quad M_{07} \]

\[ MS \quad M_{04} \]

\[ M_{05} \quad M_{06} \]

\[ V_B2 \]

\[ V_{1} \quad \text{I1} \]

\[ V_{d} \quad \text{I2} \]

\[ M_{08} \quad M_{02} \]

\[ M_{01} \quad M_{03} \]

\[ V_B1 \quad V_B3 \quad V_{SS} \]

\[ M_{07} \quad M_{08} \]

\[ M_{02} \quad M_{06} \]

\[ V_{B} \]

\[ \text{Req} \]

\[ \text{Ic1} \quad \text{Ic2} \]

\[ \text{V}_{VSS} \]

Figure 6.1: The weak-inversion OTA.

The current multiplier in the output stage increases the output current by 1 or 10 times. Therefore, the output current of the V-I converter is given by

\[ I_{out} = A I_o \]  \hspace{1cm} (6.1)

\[ = A \frac{I_{C2} V_2 - V_1}{I_{C1} \text{Req}} \]  \hspace{1cm} (6.2)

Where A is 1 or 10. From Eq. (6.2), we can see that the output current can be tuned by the resistor (the bias voltage \( V_B \)) or the two DC bias currents \( I_{C1} \) and \( I_{C2} \).
6.1.2 Experimental Results

These two OTAs were fabricated in the 1.2µm CMOS process of AMS in Austria. All the measurements were done with a single DC supply of 3V. The chip microphotograph of the OTA with A=1 is shown in Fig. 6.2. It occupies 0.200mm² area. Its transistor sizes are illustrated in Table 6.1.

![Figure 6.2: The chip microphotograph of the OTA with A=1.](image)

<table>
<thead>
<tr>
<th>Transistor</th>
<th>W/L (µm/µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1, M2, M3, M4, M5, M6</td>
<td>15/3</td>
</tr>
<tr>
<td>M7, M8, M9</td>
<td>30/6</td>
</tr>
<tr>
<td>M01, M07</td>
<td>120/24</td>
</tr>
<tr>
<td>M02, M08</td>
<td>40/24</td>
</tr>
<tr>
<td>M03, M04</td>
<td>60/12</td>
</tr>
<tr>
<td>M05, M06</td>
<td>20/12</td>
</tr>
</tbody>
</table>

Table 6.1: The transistor sizes of the OTA with A=1.
Fig. 6.3 and 6.4 illustrates the experimental result of the weak-inversion OTA with $A = 1$. These curves were measured when $V_2$ was set to be 1.35V. In these figures, different transconductance values of the OTA are obtained by changing both currents $I_{C1}$ and $I_{C2}$. The transconductance value is changed from about 1.5nS to 130nS according to different $I_{C2}/I_{C1}$ ratios.

![Graph showing transconductance values](image)

Figure 6.3: Measurement results of the OTA with $A = 1$ by changing both currents $I_{C1}$ and $I_{C2}$.

The chip microphotograph of the OTA with $A=10$ is shown in Fig. 6.5. It occupies 0.163mm$^2$ area. Its transistor sizes are illustrated in Table 6.2. Fig. 6.6 and 6.7 illustrate the measurement results of the weak-inversion V-I converter with $A = 10$. These curves were measured when $V_2$ was set to be 1.2V. Different transconductance
Figure 6.4: Measurement results of the OTA with $A = 1$ by changing both currents $I_{C1}$ and $I_{C2}$.

values of the OTA are obtained by changing both currents $I_{C1}$ and $I_{C2}$. The transconductance is changed from $65\text{nS}$ to $1100\text{nS}$ according to the changes of $I_{C1}$ and $I_{C2}$. For a 1KHz $0.8V_{PP}$ input signal, the total harmonic distortion of this circuit is about 0.88%.

6.2 5th-Order Elliptic Low-Pass GM-C Filters

6.2.1 Design of the GM-C Filters

The 5th-order elliptic low-pass GM-C filter structure utilized here is the same as that shown in Fig. 4.3 in Chapter 4 [43]. It consists of 7 OTAs and 7 capacitors, including two floating capacitors. The OTAs introduced in the last section are used in the two 5th-order elliptic low-pass filter design.
Figure 6.5: The chip microphotograph of the OTA with $A=10$.

<table>
<thead>
<tr>
<th>Transistor</th>
<th>$W/L$ (μm/μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1, M2, M3, M4, M5, M6</td>
<td>15/3</td>
</tr>
<tr>
<td>M7, M8, M9</td>
<td>30/6</td>
</tr>
<tr>
<td>MO1, MO7</td>
<td>16.2/3</td>
</tr>
<tr>
<td>MO2, MO8</td>
<td>5.4/3</td>
</tr>
<tr>
<td>MO3, MO4</td>
<td>162/3</td>
</tr>
<tr>
<td>MO5, MO6</td>
<td>54/3</td>
</tr>
</tbody>
</table>

Table 6.2: The transistor sizes of the OTA with $A=10$.

The cutoff frequency of the GM-C filter is proportional to $I/C$, i.e., $g_m/C$, where $I$ and $g_m$ are the output current and the transconductance of the OTA, respectively, and $C$ is the capacitance. If the OTA is operating in the strong saturation region, its output current is usually in the $\mu A$ level. If one wants to have a low cutoff-frequency filter, a single-chip solution for this filter is almost impossible because a large capacitance is then required. With the presented circuit, because it is working in the weak-inversion region and its output current is in the $nA$ level, only small capacitance is needed. Thus, a single-chip solution for a (very) low frequency filter is feasible. In the filter design, for simplicity, all the required capacitors for these two
Figure 6.6: Measurement results of the OTA with $A = 10$ by changing both currents $I_{C1}$ and $I_{C2}$.

filters are designed to be the same. The cutoff frequency ranges were designed to cover the entire speech frequency. After denormalization, the capacitance values are given by

\begin{align*}
C_1 & = 21.2139pF \quad C_2 = 0.6892pF \quad (6.3) \\
C_3 & = 35.6046pF \quad C_4 = 2.1024pF \quad (6.4) \\
C_5 & = 17.3644pF \quad C_{L2} = 16.6147pF \quad (6.5) \\
C_{L4} & = 23.7935pF \quad (6.6)
\end{align*}
These values, shown above, were actually extracted from the layout parameters. We can see that the maximum capacitance is only about $35pF$, so a single-chip solution is achievable.

From Eq. (6.2), the output current of the OTA can be changed by $I_{C1}$ and $I_{C2}$. $f_{cutoff} \propto I/C$, so the cutoff frequencies of the two filters are also tunable by these two bias currents.

6.2.2 Experimental Results

Using the results of Fig. 6.3, 6.4, 6.6, and 6.7, two tunable low-pass filters were designed. These two filters were fabricated in the $1.2\mu m$ CMOS process of AMS in Austria. All the measurement results were done with a single DC supply of $3V$. 
The chip microphotograph of the first filter with the OTAs of $A = 1$ is shown in Fig. 6.8. It occupies $2.73 \text{mm}^2$ area. The experimental results are shown in Fig. 6.9 and 6.10. In these two figures, the cutoff frequency of the low-pass filter is changed from about 32 Hz to 1 KHz. Actually, from the simulation, the lowest reachable cutoff frequency was around 3 Hz. When we decrease the $I_{C2}/I_{C1}$ ratio, the output transconductance of the weak-inversion OTA is decreased and, thus, the cutoff frequency of the filter is decreased, too, as described in the last subsection. The output impedance of the filter is $1/g_m$, which is increased with the reduction of the OTA output transconductance. When $I_{C2}/I_{C1}$ is decreased to be $20\text{nA}/80\text{nA}$, the filter output impedance becomes about $200 M\Omega$ (from Fig. 6.3). However, at this time, the input impedance of the measurement setup seems not to be large enough, compared with the $200 M\Omega$, so the measured filter output gain is affected and becomes distorted. Therefore, from the experimental results, the lowest obtained cutoff frequency was only 32 Hz.

Figure 6.8: The chip microphotograph of the first filter with the OTAs of $A=1$.  

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When $I_{C1} = 80nA$ and $I_{C2} = 40nA$, the simulated DC power consumption of the filter is only about $18\mu W$. It is indeed a micropower low-pass filter. The transistor sizes of each OTA inside this filter are exactly the same as those shown in Table 6.1.

When $I_{C1} = 10nA$ and $I_{C2} = 100nA$, the total in-band output noise was measured to be $250\mu V_{rms}$. Its noise spectrum is shown in Fig. 6.11. This, combined with 1% THD for $0.5V_{pp}$ input at 330 Hz (The output signal is $0.25V_{pp}$.), results in 51 dB dynamic range. The power supply rejection performances are shown in Fig. 6.12 and 6.13. These PSRRs are all more than 30 dB.

The circuit diagram of the second weak-inversion elliptic low-pass filter with the OTAs of $A = 10$ is shown in Fig. 6.14. In this filter, an NMOS transistor $M_r$ is added in series with capacitor $C_3$. This transistor, operating in the triode region with the
Figure 6.10: The measurement results of the first weak-inversion GM-C low-pass filter by changing both currents $I_{C1}$ and $I_{C2}$.

gate voltage biased by $V_{gr}$, acts as a resistor to perform phase compensation for the filter. This kind of phase correction technique has been used to compensate the phase lag, resulted from the op-amp's limited unity-gain bandwidth, in the integrator and filter designs before [45] [46]. A. M. Soliman and M. Ismail have shown that one only needs a single resistor added in series with one of the capacitors to achieve perfect phase compensation [45] [46]. Recently, this technique was also used in an integrator design to perform excess phase cancelation, where the excess phase was resulted from the parasitic capacitance of the integrator [62].

The insertion of the resistor-functioned transistor creates a zero at $-g_{ds}/C_3$, where $g_{ds}$ is the drain-source conductance of the transistor Mr. Because of the left-half plane zero, it increases the phase for the filter. Therefore, this phase increment compensates
the phase lag due to the parasitic capacitance of the OTA. Because of $g_{ds} \propto (V_{gs} - V_{T})$, when the filter has a higher cutoff frequency, a larger $V_{or}$ is required to compensate the phase lag at higher frequencies.

The chip microphotograph of this filter is shown in Fig. 6.15. It occupies $2.59 \text{mm}^2$ area. The experimental results of the second weak-inversion filter with the OTAs of $A = 10$ are shown in Fig. 6.16 and 6.17. In these two figures, the cutoff frequency of the low-pass filter is changed from about 1 KHz to 5 KHz. Fig. 6.18 illustrates the measurement results of the filter with and without phase compensation when $I_{C1} = I_{C2} = 40nA$. We can see that the phase lag is cancelled by this compensation technique. One can choose to connect or skip the compensation transistor by outside-chip connection.
Figure 6.12: The PSRR - $V_{DD}$ of the first weak-inversion GM-C low-pass filter when $I_{C1} = 10nA$ and $I_{C2} = 100nA$.

When $I_{C1} = I_{C2} = 40nA$, the simulated DC power consumption is about $25\mu W$, a micropower low-pass filter. The transistor sizes of each OTA inside this filter are exactly the same as those shown in Table 6.2.

When $I_{C1} = I_{C2} = 40nA$, the total in-band output noise was measured to be $360\mu V_{rms}$. Its noise spectrum is shown in Fig. 6.19. This, combined with 1% THD for $0.8V_{pp}$ input at 666 Hz (The output signal is $0.4V_{pp}$), results in 52 dB dynamic range. The power supply rejection performances are shown in Fig. 6.20 and 6.21. These PSRRs are more than 30 dB.

The cutoff frequencies of the two low-pass filters are changed from 32 Hz to 5 KHz, which covers the entire range of speech, so they are suitable for speech signal processing [17]. The techniques presented here provide a practical means for implementing
Figure 6.13: The PSRR - $V_{SS}$ of the first weak-inversion GM-C low-pass filter when $I_{C1} = 10nA$ and $I_{C2} = 100nA$.

very large time constants on-chip allowing single-chip solutions at very low frequencies. Results also demonstrate that these techniques are suitable for low-voltage, micropower applications at very low frequency.
Figure 6.14: The circuit diagram of a weak-inversion 5th-order elliptic low-pass GM-C filter with the OTAs of $A = 10$.

Figure 6.15: The chip microphotograph of the second filter with the OTAs of $A=10$. 

Figure 6.16: The measurement results of the second weak-inversion GM-C low-pass filter by changing both currents $I_{C1}$ and $I_{C2}$.

Figure 6.17: The measurement results of the second weak-inversion GM-C low-pass filter by changing both currents $I_{C1}$ and $I_{C2}$.
Figure 6.18: The measurement results of the second weak-inversion GM-C low-pass filter with and without phase compensation when $I_{C1} = I_{C2} = 40nA$.

Figure 6.19: The noise spectrum of the second weak-inversion GM-C low-pass filter when $I_{C1} = I_{C2} = 40nA$. 
Figure 6.20: The PSRR - $V_{DD}$ of the second weak-inversion GM-C low-pass filter when $I_{C1} = I_{C2} = 40\, \text{nA}$.

Figure 6.21: The PSRR - $V_{SS}$ of the second weak-inversion GM-C low-pass filter when $I_{C1} = I_{C2} = 40\, \text{nA}$. 

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CHAPTER 7

LOW-VOLTAGE WEAK-INVERSION VARIABLE GAIN AMPLIFIER

In audio/video mixed-signal circuits, to optimize the dynamic range of the entire system, Automatic Gain Control (AGC) circuits are usually used [63]. A Variable Gain Amplifier (VGA) plays an important role in the automatic gain control circuits [64]. A VGA needs to precede the analog-to-digital converter in order to maximize the dynamic range of the system [63]. In addition to the applications in communication systems and audio/video mixed-signal IC's, VGAs can also be utilized in the disk drive read channels to stabilize the voltage to the detector and filter sections of the read channel [65].

In this chapter, the design and operation of a low-voltage weak-inversion VGA is described. Because of its operation in the weak-inversion region, the power dissipation is very low. Its applications are emphasized on the audio signal processing and medical systems, such as hearing aids [47]. The exponential output to linear input characteristic is required to minimize the variation in the output signal [66, 67, 68, 69, 65]. Similarly, its application in the hearing aid can amplify the input signal to be the same accepted output level, which makes hearing easier for hard-hearing people [47].
In the following sections, design of the VGA will be presented first and then its results will be addressed.

7.1 Design of VGA

A VGA circuit is usually comprised by a four-quadrant analog multiplier and a detector [70]. This VGA design is also based on this principle. The block diagram of the VGA is shown in Fig. 7.1. The first stage of the VGA is an exponential output to linear input circuit, which converts a linear input voltage to an exponential output voltage. The second block of Fig. 7.1 is a weak-inversion multiplier, which receive two exponential gain control signals from the previous stage and also take two input signals. At last, an Operational Current Amplifier (OCA) will converter the output current of the multiplier to the final output voltage of the VGA.

![Block Diagram of the VGA](image)

Figure 7.1: The block diagram of the VGA.
7.1.1 Exponential Converter

The methodology to produce the exponential output signal here is to use the approximation of the exponential function as [65] [71]:

\[ \exp(2x) \approx \frac{1 + x}{1 - x} \]  
(7.1)

and

\[ \exp(4x) \approx \left( \frac{1 + x}{1 - x} \right)^2 \]  
(7.2)

There is a good match for \(-0.7 < x < 0.7\) in Eq. (7.1). However, the maximum gain range of 30 dB can only be obtained for \(-0.698 < x < 0.698\) in Eq. (7.2) [65]. Therefore, in this design, efforts are devoted to approach the function of Eq. (7.2).

First of all, let us look back Fig. 5.1 in Chapter 5. By combining Eq. (5.2) and (5.3),

\[ V_d = nU_T \ln \left( \frac{I_1}{I_2} \right) \]  
(7.3)

\[ \frac{I_3}{I_4} = \exp \left( \frac{V_d}{nU_T} \right) \]  
(7.4)

Eq. (5.4) was derived as

\[ \frac{I_3}{I_4} = \frac{I_1}{I_2} \]  
(7.5)

Assume the current flows through resistor \(R_{eq}\) is \(\Delta I\).

\[ I_1 = I_{C1} + \Delta I \]  
(7.6)

\[ I_2 = I_{C1} - \Delta I \]  
(7.7)

\[ \frac{I_1}{I_2} = \frac{I_{C1} + \Delta I}{I_{C1} - \Delta I} \]  
(7.8)

Thus,

\[ \frac{I_1}{I_2} = \frac{1 + \frac{\Delta I}{I_{C1}}}{1 - \frac{\Delta I}{I_{C1}}} \]  
(7.9)
Assume $\Delta I/I_{C1} = y$. Eq. (7.9) becomes

$$\frac{I_3}{I_4} = \frac{I_1}{I_2} = \frac{1 + y}{1 - y}$$

(7.10)

which is the same form as Eq. (7.1). In order to maximize the output gain range, however, Eq. (7.2) is preferred.

As one can see, in Fig. 5.1, $V_{z2} - V_{z1} = V_d$. To have the form of Eq. (7.2), we need to have $V_{z2} - V_{z1} = 2V_d$. This can be achieved by cascode connecting another diode-connected transistor with M5 and M6, respectively, as shown in Fig. 7.2, which is the exponential converter, the first stage of the VGA design here. Hence, current $I_1$ flows through transistors M5 and M15 and current $I_2$ flows through transistors M6 and M16. Eq. (7.3) is still consistent with Fig. 7.2, but Eq. (7.4) becomes

$$\frac{I_3}{I_4} = \exp\left(\frac{2V_d}{nU_T}\right)$$

(7.11)

Therefore, Eq. (7.10) turns out to be

$$\frac{I_3}{I_4} = \left(\frac{I_1}{I_2}\right)^2 = \left(\frac{1 + y}{1 - y}\right)^2$$

(7.12)

Then, the other part of the exponential converter will transform the $I_3/I_4$ ratio to produce two output voltages.

In Fig. 7.2, from the two current mirrors of (M7, M9) and (M8, M10), currents flowing through transistor M9 and M10 are $\alpha I_3$ and $I_4$, respectively, where $\alpha = K_{p9}/K_{p7}$. Assume currents flowing through transistors M11 and M18 are $I_{11}$ and $I_{18}$. $I_{11}$ and $I_{18}$ can be written as

$$I_{11} = \frac{K_{n11}}{2}(V_G - V_{Th})^2$$

(7.13)

$$I_{18} = \frac{K_{p18}}{2}(V_{DD} - V_G - |V_{Th}|)^2$$

(7.14)
Because $I_4 + I_{18} = I_{11}$ and $K_{n11} = K_{p18} = K$, $V_G$, i.e., the gate voltage of M12, can be obtained as [71]

$$V_G = \frac{V_{DD} - |V_{T_p}| + V_{T_n}}{2} + \frac{I_4}{K(V_{DD} - |V_{T_p}| - V_{T_n})} \quad (7.15)$$

The voltage $V_G$ is proportional to current $I_4$, that is, the two back-to-back connected transistors offer a constant linear resistance at the input terminal [71]. Because transistor M12 operates in the triode region, it acts as a voltage-controlled resistor. For a small drain-source voltage, this M12 resistance can be approximated as

$$R_{DS12} = \frac{1}{K_{n12}(V_G - V_{T_n})} \quad (7.16)$$

Figure 7.2: The exponential converter for the first stage of VGA.
Current $\alpha I_3$ flows through M12, so the drain-source voltage of M12 can be expressed as

$$V_D = V_{DS12} = \alpha I_3 R_{DS12} \propto \frac{I_3}{I_4}$$

Therefore, $V_D$ will exhibit the approximated exponential function when the control voltage $(V_{x1} - V_{x2})$ changes. This technique using two back-to-back connected transistors has been formerly exploited and used by A. Motamed [71].

In order to apply this exponential signal to the inputs of the multiplier, a level shifter is used to produce two output signals $V_{x01}$ and $V_{x02}$, where $V_{x01} - V_{x02} = V_D$.

One might wonder that in the weak-inversion region, the CMOS transistors have the intrinsic logarithmic characteristics already and why the presented circuit does not thoroughly utilize it. Actually, in Fig. 7.2, if the first part of this circuit, that is, transistors M1, M2, M5, M6, M15, M16, two current sinks $I_{C1}$, and $R_{eq}$, is taken out, we can directly use $2V_d$ as the input control voltage because $I_3/I_4 = \exp(2V_d/nU_T)$. An exponential function is directly generated from the $I_3/I_4$ ratio. This can lead to a larger output gain range, but the input control voltage range for $2V_d$ is quite small, about $2U_T$, because the structure is a differential pair. The circuit presented here gives another alternative for exponential converter. This circuit provides a much better output gain control accuracy, even with less gain range. The tradeoff is between the input control voltage range and the output gain range. The choice of the VGAs depends on its applications.

7.1.2 Multiplier

The weak-inversion multiplier utilized inside the VGA here is exactly the same as Fig. 5.3 in Chapter 5, except the transistor sizes inside the equivalent resistor circuit
are changed to have smaller resistance. The multiplier has four input signals, \( V_{x01}, V_{x02}, V_{y1}, \) and \( V_{y2} \). Its multiplying function is expressed as

\[
I_o = \frac{2}{I_{C1} R_{eqx} R_{eqy}} (V_{x01} - V_{x02}) (V_{y1} - V_{y2})
\] (7.18)

\( V_{x01} \) and \( V_{x02} \) are the exponential gain control inputs from the previous exponential converter. The input signal is differentially applied to \( V_{y1} \) and \( V_{y2} \). Its output current will be input to the Operational Current Amplifier to produce an exponential output voltage.

### 7.1.3 Operational Current Amplifier

![Operational Current Amplifier Diagram](image)

Figure 7.3: The OCA for the last stage of VGA.
The Operational Current Amplifier (OCA) circuit is shown in Fig. 7.3 [72]. This circuit takes current as input and amplify it to a output voltage. Because the input is current, NMOS transistor \( M_{O1} \) and PMOS transistor \( M_{O3} \) are used to be the input transistors to result in low input impedance, \( 1/2g_{m1} \) \( (g_{m1} = g_{m3}) \). The input transistors \( M_{O1} \) and \( M_{O3} \) are biased by \( M_{O2} \) and \( M_{O4} \). Current mirrors \( (M_{O5}, M_{O6}) \) and \( (M_{O7}, M_{O8}) \) by a factor of 5 amplify the input current \( I_o \) to reach the output. The transresistance of the OCA at low frequencies is obtained by [72]

\[
A_R = \frac{V_o}{I_o} = 5r_{o68} \tag{7.19}
\]

where \( r_{o68} = r_{o6}/r_{o8} \).

The value of \( r_{o68} \), namely, the transistor sizes of \( M_{O6} \) and \( M_{O8} \), needs to be choose carefully in order not to reach the output saturation voltage and also to maintain the gain range from current \( I_o \).

### 7.2 Results

The VGA was fabricated in the 1.2\( \mu m \) CMOS process of AMS in Austria. The chip microphotograph of the VGA is shown in Fig. 7.4. It occupies 0.533\( mm^2 \) area. The transistor sizes of the exponential converter and OCA are illustrated in Table 7.1 and 7.2, respectively. The transistor sizes of the multiplier was shown in Table 5.2.

Measurements were done using the power supply of 3V. However, no reasonable results were obtained. Only almost constant saturation voltage was measured while the gain control voltage was changed from 0 to 0.8V. It might be due to the mismatch of transistors inside the VGA, which results in offset and saturates the output. Therefore, in this section, only simulation results are presented. Simulations have been performed using AMS HSPICE models with 3 V supply voltage.

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Figure 7.4: The chip microphotograph of the VGA.

<table>
<thead>
<tr>
<th>Transistor</th>
<th>W/L (μm/μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1, M2</td>
<td>15/45</td>
</tr>
<tr>
<td>M5, M6, M15, M16</td>
<td>50/1.2</td>
</tr>
<tr>
<td>M3, M4</td>
<td>15/35</td>
</tr>
<tr>
<td>M7, M8, M10</td>
<td>45/9</td>
</tr>
<tr>
<td>M11</td>
<td>4/120</td>
</tr>
<tr>
<td>M12</td>
<td>4/80</td>
</tr>
<tr>
<td>M18</td>
<td>12/120</td>
</tr>
<tr>
<td>M9, MPO3</td>
<td>60/1.2</td>
</tr>
<tr>
<td>MPO2</td>
<td>90/1.2</td>
</tr>
</tbody>
</table>

Table 7.1: The transistor sizes of the exponential converter.

Fig. 7.5, 7.6, and 7.7 show the output voltage \((V_{x_1} - V_{x_2})\) of the exponential converter, the output current \(I_o\) of the multiplier, and the final output voltage of the VGA versus the input control voltage \((V_{x_1} - V_{x_2})\) from 0 to 0.8V, respectively, at \(V_{y_1} - V_{y_2} = 0.1V\) and \(I_{C1} = 50nA\). \(V_{x_2}\) and \(V_{y_2}\) are set to be 1.2V and 1.35V, respectively. We can see from these three figures, the output gain range of the VGA is around 20 dB. Fig. 7.8 illustrates the VGA frequency responses at \(V_{x_1} - V_{x_2} = 0\)
Table 7.2: The transistor sizes of the OCA.

<table>
<thead>
<tr>
<th>Transistor</th>
<th>W/L (μm/μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MO1, MO7</td>
<td>8/2.4</td>
</tr>
<tr>
<td>MO3, MO5</td>
<td>24/2.4</td>
</tr>
<tr>
<td>MO2</td>
<td>4/11</td>
</tr>
<tr>
<td>MO4</td>
<td>12/11</td>
</tr>
<tr>
<td>MO6</td>
<td>119.8/2.4</td>
</tr>
<tr>
<td>MO8</td>
<td>37.4/2.4</td>
</tr>
</tbody>
</table>

and $V_{x1} - V_{x2} = 0.8V$. It shows that the output gain range is 18 dB and that the -3dB frequency is more than 30 KHz. The THDs of the VGA at different input control voltages are tested by using 0.1$V_{pp}$ and 0.2$V_{pp}$ 1 KHz input signals, as shown in Fig. 7.9. At $V_{x1} - V_{x2} = 0$, the VGA outputs for 0.1$V_{pp}$ and 0.2$V_{pp}$ 1 KHz input signals are given in Fig. 7.10. One can see that with 0.2$V_{pp}$ input, the output voltage swing is from 0.2 V to 2.8V, i.e., 2.6$V_{pp}$, but the THD is 3.25%. With 0.1$V_{pp}$ input, the output voltage swing is from 0.8 V to 2.2V, i.e., 1.4$V_{pp}$, and the THD is 1.66%.

As for the input voltage swing of the VGA, it is the same as the $V_y$ input pair of the multiplier. It was measured as 1.2$V_{pp}$ from the multiplier experimental results in Section 5.1.3.

Some of the VGA parameters are summarized in Table 7.3. Its output gain range is about 18 dB. The -3 dB frequency is more than 30 KHz, which makes the circuit useful in the speech and audio signal processing. The 0.8 V control voltage range over the 18 dB output gain provides a good output gain control accuracy. Power dissipation at minimum and maximum gain is about 8.63μW and 10.19μW, respectively.
Figure 7.5: The output voltage ($V_{xo1} - V_{x02}$) of the exponential converter as function of the input control voltage ($V_{x1} - V_{x2}$) at $V_{y1} - V_{y2} = 0.1V$ and $I_{C1} = 50nA$.

The micropower consumption allows this circuit to be applied into portable medical systems.
Figure 7.6: The output current $I_o$ of the multiplier as function of the input control voltage ($V_{x1} - V_{x2}$) at $V_{y1} - V_{y2} = 0.1V$ and $I_{C1} = 50nA$.

Figure 7.7: The final output voltage of the VGA as function of the input control voltage ($V_{x1} - V_{x2}$) at $V_{y1} - V_{y2} = 0.1V$ and $I_{C1} = 50nA$. 
Figure 7.8: The VGA frequency responses at $V_{x1} - V_{x2} = 0$ and $V_{x1} - V_{x2} = 0.8V$.

Figure 7.9: The THDs of the VGA at different input control voltages for $0.1V_{pp}$ and $0.2V_{pp}$ 1 KHz input signals.
Figure 7.10: The outputs of the VGA for $0.1V_{pp}$ and $0.2V_{pp}$ 1 KHz input signals at $V_{x1} - V_{x2} = 0$.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>$3V$</td>
</tr>
<tr>
<td>Minimum Gain</td>
<td>$-2.64 dB$</td>
</tr>
<tr>
<td>Maximum Gain</td>
<td>$15.32 dB$</td>
</tr>
<tr>
<td>-3 dB Frequency at -2.64 dB</td>
<td>$33.9 kHz$</td>
</tr>
<tr>
<td>-3 dB Frequency at 15.64 dB</td>
<td>$32.4 kHz$</td>
</tr>
<tr>
<td>Input Voltage Swing</td>
<td>$1.2 V_{pp}$</td>
</tr>
<tr>
<td>Output Voltage Swing</td>
<td>$2.6 V_{pp}$</td>
</tr>
<tr>
<td>THD at 15.32 dB</td>
<td>$3.25%$</td>
</tr>
<tr>
<td>Output Voltage Swing</td>
<td>$1.4 V_{pp}$</td>
</tr>
<tr>
<td>THD at 15.32 dB</td>
<td>$1.66%$</td>
</tr>
<tr>
<td>Power Dissipation at -2.64 dB</td>
<td>$8.63 \mu W$</td>
</tr>
<tr>
<td>Power Dissipation at 15.32 dB</td>
<td>$10.19 \mu W$</td>
</tr>
</tbody>
</table>

Table 7.3: Summary of the VGA parameters.
CHAPTER 8

CONCLUSIONS AND FUTURE RESEARCH

8.1 Conclusions

In this dissertation, all the circuits were designed to work at the low supply voltage of 3 V. Some of the circuits are even designed to work in the weak-inversion region, so low power consumption can be obtained. With the reduction of power supply voltage, circuits, designed to operate from higher supply voltages, will lose a significant amount of operating range. On the other hand, with the drive to low power operation, circuits which are able to work in the weak-inversion region have become more popular. In order to have circuits operate at low voltage and/or with low power consumption, lots of basic circuit cells and building blocks are necessary to be reconsidered and redesigned. Achievement of a rail-to-rail operating range is an important specification for low-voltage circuits to maintain acceptable levels of signal-to-noise ratio. Also, to design low-voltage circuits, which can work in the weak-inversion region, can provide a circuit alternative for audio signal processing, in addition to the advantage of the low power consumption. The circuits in this research target applications in mobile telecommunications (rail-to-rail strong-inversion circuits) and in portable medical applications (low-power weak-inversion circuits).
Three CMOS low-voltage rail-to-rail V-I converters were introduced. They are based on two V-I converter cells. One of them requires fully-differential inputs, but the other one does not. In each of the rail-to-rail V-I converters, an N-type V-I converter cell is connected in parallel with its P-type counterpart to achieve common-mode rail-to-rail operation. Using the same parallel connection, there were two approaches proposed to design the rail-to-rail V-I converters. In the first two rail-to-rail V-I converter circuits, a constant transconductance is achieved through the use of two maximum-current selecting circuits and an output subtraction stage, as the Approach I. In the third circuit, a constant transconductance value is obtained by manipulating the DC bias currents of N- and P-type V-I converter cells, as the Approach II. The applications of the new circuits are many, e.g. Operational Transconductance Amplifiers in a GM-C filter with rail-to-rail common-mode input voltage [26]. They are also suitable for the development of a family of computational circuits, which can be seen as rail-to-rail low-voltage counterparts of the computational circuits in [18] [27]. Another important application which takes advantage of the rail-to-rail common-mode operation is the use of these circuits in the implementation of large transconductance-based analog VLSI circuits, such as the cellular neural network implementation proposed in [28]. In this case, no DC level shifting will be required between outputs and inputs of different transconductors in the network.

As mentioned, the rail-to-rail V-I converters are suitable for the development of a family of rail-to-rail computational circuits. An example is a low-voltage rail-to-rail multiplier. An N-type multiplier is realized by a parallel connection of the two N-type V-I converters. As the Approach I for a rail-to-rail V-I converter, through a
parallel connection of an N-type and a P-type multiplier cells and the use of maximum-current selecting circuits, a rail-to-rail multiplier is then obtained. The rail-to-rail V-I converter and multiplier can be used as a basic building block to construct rail-to-rail analog computational circuits, which can perform functions such as square-rooting, squaring, multiplication, sum of squares, difference of squares etc. Also, the idea of a parallel connection of an N-type and a P-type circuit cells and the use of a maximum-current selecting circuits can be widely extended to other computational circuits to reach rail-to-rail operation for low-voltage VLSI applications, that is, the other rail-to-rail computational circuits can be achieved in the same way, by replacing the N- and P-type multiplier cells in Fig. 3.2 with their own N- and P-type circuit cells.

A low-voltage rail-to-rail wide range Differential Difference Amplifier was presented. The input stage of the DDA comprises two rail-to-rail V-I converters, so it can have a rail-to-rail common-mode input voltage. Because of the linear V-I converters, the differential input range of the DDA is widened. Low-voltage DDA-based circuits, such as an adder/subtractor, an integrator, bandpass and lowpass filters, are also given. These circuits can be realized with low component count and without component matching external to the DDA, which, however, is a requirement in almost all Op-Amp-based circuits. DDA-based analog circuits not only constitute basic blocks of modern low-voltage analog signal and information processing systems, but also provide a competitive design choice to Op-Amp-based circuits.

Another application of the rail-to-rail V-I converter is to use it as an Operational Transconductance Amplifier in the GM-C filter design. A CMOS implementation of a low-voltage 5th-order elliptic low-pass GM-C filter with rail-to-rail common-mode
input voltage for baseband mobile communication is presented. Because of the rail-to-rail OTAs inside, the resultant filter also has a rail-to-rail common-mode input voltage, which has become more and more significant when the supply voltage keeps decreasing. The rail-to-rail property of the filter allows its use conveniently at the system level in different locations without input DC level shifting. This facilitates the design of the whole circuit significantly because the whole supply voltage range can all be utilized. The minimum power supply needed is in the order of $2V_{GS} + 2V_{DS\text{sat}}$ which can be around 2.5 V or less depending on bias current levels. This filter was designed for application in the baseband mobile/wireless communication.

In Chapter 5, a V-I converter and a multiplier structures, which can work in either the weak-inversion or the strong-inversion saturation region, are described. When the V-I converter and multiplier operate in the weak-inversion region, micro-power dissipation is expected. In addition to the low-power consumption, a large input signal swing is also necessary for a V-I converter and a multiplier. Because of their low power consumption and large signal ranges, they are suitable to be used in the large transconductor- or multiplier-based analog VLSI circuits, such as the cellular neural network implementation proposed in [28] and [51]. The V-I converter and multiplier can also be used as a basic building block to construct low-voltage, micropower analog VLSI signal processing systems. If the resistance value, given by the active resistor circuits inside the V-I converter and multiplier, is tuned down to certain value, the V-I converter and multiplier is able to work in the strong-inversion saturation region. The universal operations of the V-I converter and the multiplier structures were approved by the measurement results.
The weak-inversion V-I converter was also applied to be an OTA in the design of a micropower weak-inversion GM-C filter, as the rail-to-rail V-I converter used in the design of the rail-to-rail GM-C filter. The cutoff frequency of the GM-C filter is proportional to $I/C$, where $I$ is the output current of the OTA and $C$ is the capacitance. For strong inversion operation, if one wants to have a low cutoff-frequency filter, a single-chip solution for this filter is almost impossible because a large capacitance is then required. With the presented circuit, because it is working in the weak-inversion region and its output current is in the nA level, only small capacitance is needed. Thus, a single-chip solution for a (very) low frequency filter is feasible. The cutoff frequencies of the two weak-inversion low-pass filters are changed from 32 Hz to 1 KHz and from 1 KHz to 5 KHz, which cover the entire range of speech, so they are suitable for speech signal processing and medical hearing applications. The techniques presented here provide a practical means for implementing very large time constants on-chip allowing single-chip solutions at very low frequencies. Experimental results also demonstrate that these techniques are suitable for low-voltage, micropower applications at very low frequency.

A low-voltage weak-inversion VGA was designed. The VGA circuit is basically comprised by an exponential converter, a four-quadrant analog multiplier, and an Operational Current Amplifier (OCA). The first stage of the VGA is an exponential output to linear input circuit, which converts a linear input voltage to an exponential output voltage. The second stage is a weak-inversion multiplier, which receive two exponential gain control signals from the previous stage and take two input signals. At last, the OCA converters the output current of the multiplier to the final output
voltage of the VGA. Due to the mismatch of transistors inside the VGA, which results in offset and saturates the output, only simulation results are presented. Its output gain range is about 18 dB. The -3 dB frequency is more than 30 KHz, which makes the circuit useful in the speech and audio signal processing. The 0.8 V control voltage range over the 18 dB output gain provides a good output gain control accuracy. Power dissipation at minimum and maximum gain is about 8.63 $\mu W$ and 10.19 $\mu W$, respectively. The micropower consumption allows this circuit to be applied into portable medical systems.

8.2 Future Research

Designing circuits, where the circuits operate at low supply voltage with the advantage of rail-to-rail common-mode voltage and/or low power dissipation, is the purpose of this research. To achieve the rail-to-rail operation, a parallel connection of input NMOS and PMOS pairs is the only solution currently. For the rail-to-rail circuits, their performance variation through the entire rail strongly relies on the assumption of $K_N = K_P$. During the circuit design, because of the pre-known parameter model from the fabrication process, designers can adjust NMOS and PMOS transistor sizes to compensate the difference between the electron and hole mobilities to reach $K_N = K_P$. If a well-defined fabrication process is available, $K_N = K_P$ can be easily maintained through this adjustment. However, if the pre-known parameter model is changed from time to time, a circuit, which can assure $K_N = K_P$, will be very helpful in the design of rail-to-rail circuits. In Section 2.4, a circuit which achieves $K_N I_N = K_P I_P$ was presented. It was shown that the circuit could decrease
the output current variation through the whole common-mode voltage range. Therefore, the performance variation through the entire rail will be improved, if this kind of compensation circuit can be utilized in the rail-to-rail circuits.

In Chapter 2, three rail-to-rail V-I converters were introduced. On the other hand, a weak-inversion V-I converter was presented in Chapter 5. The latter one consumes very low power, on the order of $\mu W$, but its operating voltage range is not wide enough, compared with the former one. Therefore, it will be glad if a rail-to-rail weak-inversion V-I converter can be accomplished.

In this dissertation, the rail-to-rail low-pass GM-C filter in Chapter 4 and the weak-inversion low-pass GM-C filters in Chapter 6 do not have the automatic tuning scheme inside. To make sure the accurate frequency response of the filter, a precise ratio of the OTA transconductance to the capacitance value needs to be maintained. Due to the possible process variation in the chip fabrication, the circuit performance will be advancedly guaranteed if the automatic tuning is included into the filter. In the automatic tuning scheme, a MASTER-SLAVE control system is usually utilized. The performance of the automatic tuning strategy highly depends on the matching and tracking between these MASTER and SLAVE circuits. For the GM-C filter, an additional OTA is constructed inside the chip to serve as the MASTER. It tracks all the process deviation continuously by a feedback route until a correct signal is obtained, so this signal can be then applied to the OTA itself and also the main filter (SLAVE). Even there is any bias change during the circuit operation, MASTER can monitor it and inform SLAVE about the change. If a Switched-Capacitor tuning scheme is used, the output transconductance of the MASTER OTA can be designed to be proportional to the value of the capacitor inside the tuning scheme. Therefore,
any change for the capacitor values in the filter will be compensated, too, because
now in this filter, the transconductance-capacitance ratio becomes the capacitance-
capacitance ratio already. The filter performance can be better controlled with an
automatic tuning circuit inside.

In Chapter 5, the universal structures of a V-I converter and a multiplier were
addressed. For them to work in weak- and strong-inversion regions, resistor circuits
with the same scheme, but different-sized transistors, were applied. It will be very
useful if a resistor circuit with a large resistance tuning range is designed. Thus,
the same V-I converter or multiplier can work in either the weak- or strong-inversion
region by only changing the resistor bias conditions. Furthermore, through the use
of this V-I converter to be an OTA in the filter design, a programmable filter with a
very large tuning cutoff frequency range can be easily achieved as well.
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