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LOW-VOLTAGE ANALOG VLSI CIRCUITS AND SIGNAL PROCESSING

DISSERTATION

Presented in Partial Fulfillment of the Requirements for
the Degree Doctor of Philosophy in the Graduate
School of The Ohio State University

By

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* * * * *

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ABSTRACT

Constant reduction of the minimum feature size in the past three decades has enabled circuit designers to achieve higher device density and higher functionality per chip. The limitations on the maximum allowed power dissipation of now increasingly crowded and faster chips and market demand for light weight and long life portable equipment have brought the low-voltage/low-power analog and digital circuit design to the research forefront.

The input voltage handling of analog circuits should be maximized in order to fully utilize the available supply voltage range and enhance the signal to noise ratio. This is especially important in the era of mixed-mode integrated circuits, where analog circuits should be insensitive to switching noise of digital circuits.

This research mainly focuses on ways to enhance the input voltage range of basic analog circuit building blocks. To this end a new approach based on using a current-mode maximum selecting circuit is developed. The new idea is applied to the input stage of an Operational Amplifier (Op Amp). Two input stages are designed based on two different variations of this method. The new input stages can achieve rail-to-rail operation with nearly constant transconductance. In order to verify the method, two Op Amps are designed and fabricated using a MOSIS 2-μm nwell process. The measurement and simulation results are presented. The approach is not limited to Op Amp input stages, but can be applied to the other analog circuits as well. To show
another application of this method, a low-voltage four-quadrant analog multiplier with enhanced input voltage range is designed. The new multiplier possesses an input voltage range nearly twice that achievable by a simple four-quadrant multiplier.

A new low-voltage composite transistor is then introduced and used in conjunction with the analog multiplier to design a low-voltage variable gain amplifier. Since logarithmic gain behavior is required in most applications, a new exponential voltage generator is designed and used to control the gain of the amplifier.
In memory of my parents.
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CHAPTER 1

Introduction

1.1 Background

Constant reduction of the minimum feature size in the past three decades has enabled circuit designers to achieve higher device density and higher functionality per chip. As Gordon Moor predicted in the late 1960's in what is known as Moor's law [1, 2], the number of transistors on the chip will double every year. Indeed, the number of devices on a chip has grown exponentially in past two decades, as manifested in the availability of low-cost computation power and communication capacity, which has shaped our lives unparalleled to any other technological advancement. It is safe to believe that this trend will last for at least two more decades despite the concern raised that approaching fundamental limits of the semiconducting materials will slow down and eventually stop further reduction of the minimum feature size.

In addition to the acknowledged market demand for light weight and long life portable equipment, the supply voltage should be reduced in order to keep the maximum electric field intensity in semiconducting devices below its critical value and thereby achieve and maintain acceptable level of reliability. Moreover, the limitations on the maximum allowed power dissipation of now increasingly crowded and faster
chips is yet another driving force behind the current trend toward power supply voltage reduction.

Although lower supply voltage directly translates to lower power consumption in digital circuits, similar conclusion cannot necessarily be drawn for analog circuits. Therefore low-power analog design raises its own challenges that should be met under the constraints of low-voltage design. Furthermore, in the era of mixed-mode integrated circuits, the design of the analog circuits should be carried at in the presence of noisy digital circuits with a technology optimized not for analog but for digital circuits [3, 4, 5]. This is one reason why rail-to-rail analog integrated circuit design with its clear advantage in achieving higher signal-to-noise ratio (SNR) and wide dynamic range has gained so much attention in recent years [6, 7, 8].

The threshold voltages of MOS transistors determine the number of MOS transistors that can be stacked between two supply rails. Using nominal threshold voltages of 0.7V to 0.8V and a drain-source saturation voltage of 0.2V, only two transistors and two current sources can be stacked in circuits with a 3V supply voltage. Consequently, most analog circuit topologies in our arsenal that worked well at higher supply voltages demonstrate little or no applicability in meeting the challenges of low-voltage and low-power analog circuit design at hand. Industry is hesitating to adopt a lower threshold voltage mainly due to concerns about increased leakage current with its adverse effect on the reliability of dynamic memories and increased static power consumption of digital circuits [9, 10, 11]. Alternatively, the use of new technologies such as the multi-threshold process, where the threshold voltages of digital and analog circuits can be set independently, is justifiable only if the cost is inconsequential.
Speed is another challenge faced equally by both digital and analog designers. As transistor size decreases, so does the capacitance associated with the transistor, leading to faster transistor operation. However, devices in analog circuits are seldom of minimum size. Therefore, except some marginal improvements due to lower parasitic capacitances, a process with lower minimum feature size does not offer much to analog circuit designers. On the other hand, digital circuits where most transistors are of minimum size could operate much faster only if the signal does not need to be transmitted over now longer and more intricate interconnections. As the minimum feature size decreases and chip area increases, longer and more closely spaced interconnections show higher resistance, capacitance and mutual inductance, which severely limits the intra-chip communication speed [12, 13]. Ironically, the problems faced by digital designers are becoming more analog in nature.

1.2 Significance of the research

The relentless strive for larger input and output voltage swings of low-voltage and low-power analog circuits is the main theme of this research. Operational Amplifiers (Op Amps) are among the most widely used building blocks in analog integrated circuit design. Op Amps can be used either in inverting or non-inverting configurations. In the inverting configuration, rail-to-rail operation of the input stage is usually not required because the input common mode voltage $V_{CM}$ is fixed and does not depend on the input signal. Alternatively, the input common mode voltage of an Op Amp in the non-inverting configuration may vary from rail-to-rail. Consequently, for proper operation, the input stage should possess rail-to-rail characteristics, i.e., should be capable of handling input voltages from rail to rail. It is shown [14] that
by employing one n-type differential pair in parallel with one p-type differential pair an input stage with rail-to-rail operation can be designed. However, such an input stage shows strong transconductance \( g_m \) variation and prohibits optimal frequency compensation of the Op Amp. Several methods have been proposed to reduce the \( g_m \) variation of the rail-to-rail input stage [15, 16, 17, 18, 19, 14, 20, 21, 22]. Almost all these methods are based on handling and controlling the bias currents of the input differential pairs. In addition to their complex bias circuitry, these architectures rely on a rather simplified model of the MOS transistor, limiting the design to specific technologies and operating regions.

A novel idea based on processing of the signal current is presented in this thesis and applied to the operational amplifier input stage [23, 24]. The new input stage can achieve rail-to-rail operation while avoiding the main drawbacks of the conventional designs. The proposed method is universal in that it can be applied independent of the device type (bipolar or MOS). In the case of MOS transistors, this approach can be implemented independent of the operating region, i.e. strong or weak inversion. Two variations of this idea are examined. One is based on processing of the AC signal only while the other is based on processing of the total instantaneous current where the AC signal current is superimposed on a constant DC current. The potential of signal current handling is not limited to the operational amplifier input stage but can be applied to other basic analog building blocks as well. Application of this idea can lead to design of a low-voltage four-quadrant analog multipliers with an extended input voltage range.

Analog multipliers are widely used in communication circuits as modulators and demodulators. The concept of the input voltage range and rail-to-rail operation of
analog multipliers is scrutinized and the differences between rail-to-rail operation of an Op Amp input stage and a multiplier is highlighted. Accordingly, the same idea of handling signal currents used in the design of a constant-$g_m$ input stage is applied to the design of a four-quadrant analog multiplier in order to extend its input voltage range. This design achieves larger input voltage ranges by cooperative operation of two basically independent analog multipliers.

The CMOS composite transistor proved to be a versatile transconductor element. The current through the device can be controlled by two high impedance terminals, simplifying the design of many analog circuit building blocks. The composite transistor can be viewed as a single transistor with an effective threshold voltage of $V_{Tn} + |V_{Tp}|$, where $V_{Tn}$ and $V_{Tp}$ are the threshold of n- and p-type transistors, respectively. Due to its higher threshold voltage, the composite transistor is not suitable for low-voltage applications. To alleviate this problem, a new low-voltage composite transistor is devised and used in the design of a Variable Gain Amplifier (VGA) possessing exponential gain control with applications in audio and video analog signal processing. The designed VGA can achieve larger input voltage ranges than other designs based on transconductance control of a differential stage.

1.3 Organization

This dissertation is organized as follows;

In Chapter 2, the complementary differential stage is discussed and is shown to cause large variations of the inputs stage transconductance. Several problems caused by the transconductance variation are investigated. A new architecture based on handling the AC signal and using a current-mode maximum selecting circuit is
proposed in this chapter. Simulation and experimental results of an Op Amp design based on this idea is also presented.

In Chapter 3, the idea introduced in Chapter 2 is further developed. A new minimum selecting circuit is presented and its operation is explained. A novel design for the design of a rail-to-rail constant-$g_m$ input stage based on the handling of the total instantaneous currents is introduced. This input stage is used in the design of a low-voltage Op Amp. The chapter concludes with the simulation and experimental results of the Op Amp.

In Chapter 4, the input voltage range and the rail-to-rail operation of four-quadrant analog multipliers are investigated. A four-quadrant analog multiplier with the extended input voltage range is designed. This design is based on the handling of the signal currents and uses the current-mode maximum selecting circuits. Simulation results of the multiplier are presented.

In Chapter 5, two VGA designs based on analog multiplier with exponential gain control are discussed. A new low-voltage composite transistor which can improve input voltage range is introduced. This composite transistor is used in the design of a new VGA with enhanced input voltage range. Simulation and experimental results of both VGAs are also presented. Finally, Chapter 6 provides a summary and concluding remarks of the research conducted as well as recommendations for future research in this area.
CHAPTER 2

CONSTANT TRANSCONDUCTANCE INPUT STAGES

2.1 Introduction

Analog VLSI circuits comprise only a small portion of a digitally dominated mixed-signal IC design environment. Therefore, we are experiencing a trend in supply voltage reduction that has been mainly slowed down by minimum acceptable noise margin of digital circuits and not by the design constraints of analog integrated circuits. While in most cases, conventional digital circuit design methods remain unaltered at lower supply voltages, new analog design techniques must be developed to account for the reduction in the supply voltage.

Digital processing of signals has gained wide popularity in audio and video applications. However, since real world audio and video signals are analog, the use of analog circuits is inevitable for interfacing purposes in mixed signal chips. The conventional design methods of analog integrated circuits are challenged by the strict voltage and power requirements of battery operated applications such as portable computers, portable instrumentation and cellular communication systems, where low supply voltage and power consumption are of prime importance. Low supply voltage not only reduces the number, and thereby the weight, of the needed batteries, but also is vital to ensure reliability of sub-micron implementation of integrated circuits.
This chapter presents a novel approach to the design of low-voltage CMOS Op Amps. This approach is based on the use of a current-mode maximum selecting circuit (Max-circuit) which takes the output currents of two complementary differential input pairs and delivers a near constant current at its output. The proposed implementation of the Op Amp achieves a nearly constant transconductance ($g_m$), independent of the common-mode input voltage. Moreover, the designed Op Amp is capable of operating in both weak and strong inversion and is suitable as a building block in analog cell libraries.

This chapter is organized as follows. Section 2.2 explains how rail-to-rail operation can be achieved in the input stage and addresses some problems encountered with input stages having a variable transconductance. This section also briefly discusses conventional approaches to design of low-voltage, rail-to-rail input stages with constant-$g_m$ behavior. Section 2.3 introduces a new approach to the design of rail-to-rail constant-$g_m$ input stages. In section 2.4, the Max-circuit is described. Section 2.5 further discusses the Max-circuit in the context of low-voltage Op Amp and demonstrates how a constant $g_m$ can be achieved without resorting to the often complicated bias current control schemes. Finally, simulation and experimental results of the proposed Op Amp are presented in section 2.6 which concludes the chapter.

2.2 Rail-to-rail input stage

In low-voltage applications, it is of crucial importance to take advantage of the whole available supply voltage range. In other words, the input stage of a general purpose Op Amp should be capable of handling common-mode voltages ($V_{CM}$) in the range of $V_{SS}$ to $V_{DD}$ and the output stage should be able to handle voltage swings
very close to $V_{DD} - V_{SS}$ without introducing unacceptable distortion. To extend the common-mode input voltage range and thereby achieve rail-to-rail operation, a parallel combination of n- and p-type differential pairs is used [14]. This method is shown in Figure 2.1(a). Respectively, the n- and p-type differential pairs show constant transconductances of 

$$g_{mn} = \sqrt{k_n \left( \frac{W}{L} \right)_n I_{BN}}$$ (2.1)

when

$$V_{CM} \geq V_{SS} + V_{ds,satn} + V_{Tn} + \sqrt{\frac{I_{BN}}{k_n} \left( \frac{L}{W} \right)_n}$$ (2.2)

and

$$g_{mp} = \sqrt{k_p \left( \frac{W}{L} \right)_p I_{BP}}$$ (2.3)

when

$$V_{CM} \leq V_{DD} - V_{ds,satp} + V_{Tp} - \sqrt{\frac{I_{BP}}{k_p} \left( \frac{L}{W} \right)_p}$$ (2.4)

where $V_{ds,satn}$ and $V_{ds,satp}$ are the saturation voltages of the n- and p-type differential stage current sources, respectively.

In conventional designs, the $g_{mn}$'s of both differential pairs will be added in the gain stage which usually has a folded cascode architecture. In this case the total transconductance of the input stage $g_{mt}$ is equal to $g_{mn} + g_{mp}$ as shown in Figure 2.1(b). For low common-mode input voltages, the p-type pair operates and $g_{mt}$, the total transconductance of the complementary input stage, is equal to $g_{mp}$. As the common-mode voltage increases, the n-type pair starts to operate and therefore contributes to $g_{mt}$. In this voltage range, the input stage shows higher transconductance.
Finally, for higher common-mode voltages, only the n-type pair operates and $g_{mn}$ is equal to $g_{mn}$. Figure 2.1(b) shows that the midrange $g_{mt}$ of the input stage is twice as large compared to that for low and high common-mode input voltage ranges.

The use of complementary input pairs results in certain drawbacks which could limit the overall performance. Each pair exhibits a different DC behavior. In addition to causing a variable slew rate, the CMRR degrades when the common-mode input is such that one of the pairs turns off. A much more serious drawback, though, is the variation of the input stage transconductance, $g_{mt}$, with the common-mode input voltage. When both input pairs operate the overall transconductance $g_{mt}$ varies by a factor of two from the level at which only one pair operates. Such variation causes signal distortion and introduces variations in the unity gain bandwidth [25, 21, 15]. Each of these problems will be discussed further in the following subsections.
2.2.1 Op Amp compensation

To avoid instability and guarantee enough phase margin, the Op Amp should be compensated using one of the available compensation methods. Since the unity gain frequency of an Op Amp is proportional to the $g_{mt}$ of its input stage [16], variations in the transconductance of the input stage prohibit the optimum frequency compensation of the Op Amp.

A single pole-compensation method, which is based on pole-splitting, is the most widely used compensation scheme. A simplified small signal model of the compensated Op Amp is shown in Figure 2.2. In this circuit $C_c$ is the compensation capacitor

![Compensated two poles model of the Op Amp.](image)

and the $g_{mt}$ and $g_{mo}$ are the transconductances of the input and output stage respectively. Moreover, $g_a$, $C_a$ and $g_b$, $C_b$ are the output conductance and capacitance of the input stage and the output stage, respectively. The transfer function of the Op Amp can be written as

$$A(s) = \frac{A_0 \left(1 - \frac{s}{2\pi f_{ct}}\right)}{(1 + \frac{s}{2\pi f_{cp1}})(1 + \frac{s}{2\pi f_{cp2}})}$$  \hspace{1cm}(2.5)
Where $A_o$ is the DC gain of the Op Amp. Assuming $g_{mo} \gg g_a$ and $g_b$, the following equations can be written [26]

$$A_0 = \frac{g_{mt}g_{mo}}{g_a g_b}$$  \hspace{1cm} (2.6)$$

$$f_{c1} \approx \frac{g_{mt}}{2\pi A_0 C_c}$$  \hspace{1cm} (2.7)$$

and

$$f_{c2} \approx \frac{1}{2\pi} \frac{g_{mo} C_c}{C_a C_b + C_c (C_a + C_b)}$$  \hspace{1cm} (2.8)$$

which reduces to

$$f_{c2} \approx \frac{g_{mo}}{2\pi C_b}$$  \hspace{1cm} (2.9)$$

assuming $C_a < C_c \ll C_b$. The zero of the transfer function is located at

$$f_z \approx \frac{-g_{mo}}{2\pi C_c}$$  \hspace{1cm} (2.10)$$

The unity gain frequency of the Op Amp is equal to

$$f_u \approx \frac{g_{mt}}{2\pi C_c}$$  \hspace{1cm} (2.11)$$

For a phase margin of $60^\circ$, $f_{c2}$ should be 2.2 times higher than the unity gain frequency, assuming the zero is at least ten times larger than unity gain frequency [26]. This condition can be written as

$$\frac{g_{mo}}{2\pi C_b} \approx 2.2 \frac{g_{mt}}{2\pi C_c}$$  \hspace{1cm} (2.12)$$

or

$$C_c \approx 2.2 \frac{g_{mt} C_b}{g_{mo}}$$  \hspace{1cm} (2.13)$$
Therefore, the value of compensation capacitor is directly proportional to the transconductance of the input stage. To maintain sufficient phase margin for the whole common mode input voltage range, the Op Amp should be compensated for the worst case, where the input stage has the maximum transconductance of \( g_{mt} = g_{mn} + g_{mp} \). However, this compensation capacitor reduces the unity gain frequency at low and high common mode voltages (where \( g_{mt} \) is only equal to \( g_{mp} \) and \( g_{mn} \), respectively) and limits the useful bandwidth of the Op Amp. The lower unity gain frequency also increases the phase margin of the Op Amp. It can be shown that a 50% reduction of the unity gain frequency increases the phase margin to almost 75°. This larger phase margin leads to an over-damped time response behavior in the Op Amp. Moreover, the larger compensation capacitor deteriorates the slew rate.

### 2.2.2 Slew rate

Figure 2.3(a) shows the nonlinear model of a unity gain Op Amp used in the evaluation of the slew rate. The slew rate depends on the value of the compensation capacitor, which acts as an integrator capacitor, and the available charging current supplied by the input stage. Figure 2.3(b) shows the available charging current as a function of the output voltage when a step input is applied. Assuming \( V_o = 0 \) at \( t = 0 \), the input step voltage turns on both the p- and the n-stage (region I). Therefore, the charging current is equal to the sum of the bias currents, namely \( I_{BN} + I_{BP} \). As the output voltage increases above \( v_{ip} \), the output current of the p-stage decreases. This gives rise to the exponential behavior of the slew rate in region II. The charging current in region III, where only the n-stage is operating, is equal to \( I_{BN} \). In this region the output voltage increases linearly but the slew rate is one
Figure 2.3: Operational Amplifier Model for the evaluation of Slew Rate. $I_N$ and $I_P$ are the n- and p-type differential pairs tail currents, respectively.
Table 2.1: Slew rate equations for the Op Amp with variable \( g_m \) input stage.

<table>
<thead>
<tr>
<th>Time</th>
<th>Condition</th>
<th>Output Voltage equation</th>
</tr>
</thead>
<tbody>
<tr>
<td>( 0..t_1 )</td>
<td>( V_o &lt; V_{1p} )</td>
<td>( V_o = \frac{(I_{BN} - I_{BP}) t}{C_c} ) (for ( t_1 &lt; t &lt; t_2 ))</td>
</tr>
<tr>
<td>( t_1..t_2 )</td>
<td>( V_{1p} &lt; V_o \leq V_{2p} )</td>
<td>( V_o(t) = V_{2p} + (V_{2p} - V_{1p}) \left( \frac{I_{BN}}{I_{BP}} + (1 + \frac{I_{BN}}{I_{BP}}) e^{\frac{t}{C_c(V_{2p} - V_{1p})}} \right) )</td>
</tr>
<tr>
<td>( t_2..t_3 )</td>
<td>( V_{2p} &lt; V_o \leq V_{in} )</td>
<td>( V_o = V_{2p} + \frac{I_{BN}(t - t_2)}{C_c} ) (for ( t_2 &lt; t &lt; t_3 ))</td>
</tr>
<tr>
<td>( t_3..t_4 )</td>
<td>( V_{in} &lt; V_o &lt; V_{DD} )</td>
<td>( V_o(t) = V_{DD} - (V_{DD} - V_{in}) e^{\frac{t}{C_c(V_{DD} - V_{in})}} )</td>
</tr>
</tbody>
</table>

As the output voltage increases the n-stage starts to turn off and decreases the charging current which again, leads to an exponential behavior of the slew rate (region IV). Table 2.1 summarizes the slew rate equations. Figure 2.4 illustrates the nonlinear behavior of the slew rate. The dependency of the slew rate on the common mode input voltage leads to a non-constant large signal settling time of the amplifier [27].

2.2.3 Common mode rejection ratio

The Common Mode Rejection Ratio (CMRR) of an Op Amp can be simply defined as the ratio of the differential gain to common mode gain:

\[
CMRR = \frac{\partial V_o}{\partial V_{in}} = \frac{A_d}{A_c} \tag{2.14}
\]

where \( A_d \) and \( A_c \) are the differential and common mode gains, respectively. Practical limitations such as device mismatches, design asymmetry and the finite output
resistance of the input differential pair current sources increase the common mode gain and limit the maximum achievable CMRR. Moreover, the variation of $g_m$ with $V_{CM}$ can be coupled into the output stage and further degrades the CMRR of the Op Amp. This occurs because an input stage with non-constant transconductance can introduce a new way for $V_{CM}$ to affect the output signal. The adverse effect of $g_m$ variation on the CMRR can be best explained using the simplified block diagram of an Op Amp shown in Figure 2.5. This figure shows two separate blocks representing the differential and the common mode gain. All the aforementioned non-idealities which cause a non-zero common mode gain is absorbed in the block with the transconductance of $g_{mc}$ and the differential gain is represented by another block with the transconductance of $g_{md}$. The output voltage $v_o$ can be written as

$$v_o = g_{md}r_o v_id + g_{mc}r_o V_{CM}$$  

(2.15)
Figure 2.5: Simple block diagram of an Op Amp used to evaluate the effect of $g_m$ variation on CMRR. Two blocks with the transconductances of $g_{md}$ and $g_{mc}$ represent the differential and common mode gain of the Op Amp.

where $r_o$ is the transresistance of the gain stage. Using Eq. 2.14 and 2.15 the CMRR of an Op Amp with an ideally flat $g_m$ can be written as

$$CMRR = \frac{\partial v_o}{\partial v_{id}} = \frac{g_{md}}{g_{mc}}$$

(2.16)

Now let us examine the CMRR of an input stage with a non-constant transconductance $g_{md}$. In this case $g_{md}$ is function of $V_{CM}$ and CMRR is equal to

$$CMRR = \frac{\partial v_o}{\partial v_{id}} = \frac{g_{md}}{v_{id} \frac{\partial g_{md}}{\partial V_{CM}} + g_{mc}}$$

(2.17)

Depending on the sign of the term $v_{id} \frac{\partial g_{md}}{\partial V_{CM}}$, an input stage with $g_{md}$ variation can demonstrate higher common mode gain and lower CMRR. Moreover, CMRR is function of the input differential voltage. As Eq. 2.17 suggests, the CMRR can be improved by decreasing the transconductance variation of the input stage. However, as is explained in next section, achieving a constant $g_m$ using conventional methods may even further degrade CMRR due to the fact that introducing additional transistors

17
in the bias current paths tends to lower the impedances present at the sources of the input differential pairs and thereby increase the common mode gain.

2.2.4 Conventional methods

In conventional design, as mentioned earlier, the \( g_m \) and \( g_p \) of the input differential pairs will be added in the gain stage which gives rise to a total transconductance of \( g_{mt} = g_{mn} + g_{mp} \). In strong inversion the transconductance of an MOS input stage is proportional to the square root of the bias currents. Using Eq. 2.1 and Eq. 2.3, \( g_{mt} \) can be expressed as

\[
g_{mt} = \sqrt{k_n \left( \frac{W}{L} \right)_n I_{BN}} + \sqrt{k_p \left( \frac{W}{L} \right)_p I_{BP}}
\]

(2.18)

Alternatively, the transconductance of a bipolar transistor, or an MOS input stage operating in weak inversion, is directly proportional to the bias current itself. In this case \( g_{mt} \) can be written as

\[
g_{mt} = k(I_{BN} + I_{BP})
\]

(2.19)

where \( k \) is a constant factor.

Several methods have been proposed in the literature to achieve constant \( g_m \) and overcome the problems caused by its variation. These methods are based on one fundamental concept, i.e., controlling DC tail currents of the differential input stages as shown in Figure 2.6. These methods can be categorized into two main schemes: in the first scheme, which is suited for MOS designs in strong inversion, constant transconductance is achieved by keeping the sum of the square roots of the tail current constant \[15, 16, 17, 18, 19\]. the second scheme which targets bipolar \[14, 20\] and MOS input stages operating in weak inversion \[21, 19, 16\], involves keeping the sum
Figure 2.6: In conventional methods constant-$g_m$ is achieved by controlling the tail currents of the input differential pairs.

of the tail currents flowing into the n- and p-type input pairs constant. However, weak-to-moderate and moderate-to-strong transitions of the transistors accompanied with different dependency of $g_m$ on the bias current [16] in these regions introduce degradation in circuit performance.

The first design for a rail-to-rail constant-$g_m$ input stage to be considered here is based on Eq. 2.19 and involves keeping the sum of the tail currents flowing through both the n- and p-type input pairs constant. Figure 2.7 shows a possible implementation. The current switch, N3, together with the one-to-one current mirror, P3-P4, redirects part of the bias current $I_B$ to the p-type differential pair in such a way the sum of the tail currents of n- and p-type differential pair is always constant and equal to $I_B$. This design can be used both for bipolar input stages [14, 20] and MOS input stages operating in weak inversion [21, 28, 16].

The second scheme, which is based on Eq. 2.18, is suited for MOS designs in strong inversion. In this design constant $g_m$ is achieved by keeping the sum of the
square roots of the tail currents constant \([29, 16, 17, 18, 19, 22]\). An example of this method is shown in Figure 2.8, where \(V_{B2}\) is a few hundred millivolts less than \(V_{DD}\) and \(V_{B1}\) is a few hundred millivolts more than \(V_{SS}\). At low common mode voltages, the current switch, \(P3\) is off while the current switch, \(N3\) is on. Hence, the current \(I_{B1}\) flows through \(N3\) to the current mirror \(P4-P5\) where it is multiplied by a factor of 3. The output current of the current mirror is summed with \(I_{B2}\). Since \(I_{B1} = I_{B2} = I_B\), the total tail current of the p-type input pair becomes \(4I_B\). At mid-rail \(V_{CM}\), both the current switches, \(N3\) and \(P3\), are off and the tail currents of n- and p-type input pairs are equal to \(I_B\). At high common mode voltages, the current switch \(N3\) is off while the current switch \(P3\) is on. In this case the current \(I_{B2}\) flows through \(P3\) to the current mirror \(N4-N5\), where it is multiplied by a factor of 3 and added to \(I_{B1}\).
Figure 2.8: A complementary input stage with one-to-three current mirror.

and increases the total tail current of the n-type input pair to $4I_B$. Therefore, at any common mode input voltage, assuming $k_n(W/L)_n = k_p(W/L)_p = K$, Eq. 2.18 can be rewritten as

$$g_m = \sqrt{K} (\sqrt{I_{BN}} + \sqrt{I_{BP}}) = 2\sqrt{K} \sqrt{I_B}$$  \hspace{1cm} (2.20)

which guarantees a constant $g_m$. Unfortunately, the $g_m$ variation can not be readily decreased below 16% due to the operating region transition of the input stages and the turn-over voltages of the current switches.

A different implementation of a constant-$g_m$ input stage using a square-root circuit is shown in Figure 2.9. Assuming all transistors are in saturation region, the operation of the circuit can be described as follows: the current mirror N5-N6 forces the sum of $I_{N7}$, $I_{N10}$, and $I_{P7}$ to be equal to the sum of $I_{N8}$, $I_{N9}$, and $I_{P8}$. Since $I_{N7}$ and $I_{N9}$
Figure 2.9: A complementary input stage with square-root bias control circuit.

are equal to \( I_{\text{REF}} \), we can write

\[
I_{N10} + I_{P7} = I_{N8} + I_{P8}
\]  

(2.21)

At low common mode voltages where \( V_{B2} \) is lower than \( V_{B1} \), the current \( I_{P8} \) is larger than \( I_{P7} \). Consequently, \( I_{N10} \) should increase in order to satisfy Eq. 2.21, resulting in a matching increase of \( I_{BP} \). A translinear equation can be written for the gate-source voltages of N7-N10, i.e.

\[
V_{GS,N7} + V_{GS,N9} = V_{GS,N8} + V_{GS,N10}
\]  

(2.22)

Eq. 2.22 can be rewritten as

\[
\sqrt{I_{N7}} + \sqrt{I_{N9}} = \sqrt{I_{N8}} + \sqrt{I_{N10}}.
\]  

(2.23)
Substituting $I_{REF}, I_{BP}, I_{REF}$, and $I_{BN}$ for $I_{N9}, I_{N10}, I_{N7}$, and $I_{N8}$ into Eq. 2.23, we have

$$\sqrt{I_{BN}} + \sqrt{I_{BP}} = 2\sqrt{I_{REF}}.$$  \hspace{1cm} (2.24)

Thus, using $I_{BP}$ and $I_{BN}$ as the bias currents for the differential pairs leads to a constant $g_m$ behavior of the input stage.

None of the methods discussed above can be applied universally at the same time to both bipolar and MOS input stages operating in weak and/or strong inversion regions since the way of of implementing a constant $g_m$ is different in each case. Consequently, special and elaborate non traditional bias circuitry is needed in each case which could, in some designs, consume large static power.

Unfortunately, bias current control circuits tend to decrease the impedances of the input differential pair current source and deteriorate the CMRR. Moreover, in order to decrease $g_m$ variation, the differential input stages are usually biased in such a way to avoid an overlap of constant regions of $g_{mn}$ and $g_{mp}$ at mid-rail voltages. Such a biasing condition forces the current sources to operate close to their linear region where they show lower output impedances.

The next section introduces a novel and universal concept which is independent of the input transistor type (MOS, Bipolar, or BICMOS) and their operating regions (weak or strong inversion for MOS and active for bipolar) to obtain rail-to-rail constant $g_m$, using simple, traditional bias circuitry. The new concept is based on the processing of signal currents, rather than manipulating DC tail currents. This concept considerably simplifies the design of low-voltage Op Amps and makes it more systematic. It could also significantly reduce static power consumption.
2.3 New constant-$g_m$ input stage

The approach adopted here is unique in that we attempt to track regions of constant $g_{mn}$ and $g_{mp}$ of the input differential pairs. In other words, instead of controlling the bias current we can use a current-mode maximum selecting circuit (Max-circuit) to obtain a constant $g_m$, i.e. the output signal of the input pair with a higher $g_m$ will always be regenerated at the output of the Max-circuit. For proper operation of the circuit, the regions of constant $g_m$ of the input differential pairs must overlap. Combining Eq. 2.1 through 2.4 gives the necessary condition for such an overlap as

$$V_{DD} - V_{SS} \geq V_{TN} - V_{TP} + V_{ds,satn} + V_{ds,satp} + \frac{I_{BN}}{g_{mn}} + \frac{I_{BP}}{g_{mp}}$$

(2.25)

Moreover, $g_{mn}$ and $g_{mp}$ should be equal to ensure constant transconductance over the whole common-mode input voltage range. To illustrate the idea a simple complementary input stage is considered as shown in Figure 2.10. If the body effect is ignored, the input common mode voltage range of this input stage is limited to

$$V_{CM,min} = V_{SS} + \sqrt{\frac{I_{BP}}{k_n} \left( \frac{L}{W} \right)_{N3,N4}} + V_{TN} - | V_{TP} |$$

(2.26)

and

$$V_{CM,max} = V_{DD} - \sqrt{\frac{I_{BN}}{k_p} \left( \frac{L}{W} \right)_{P3,P4}} + V_{TN} - | V_{TP} |$$

(2.27)

Therefore, almost rail-to-rail operation can be achieved. However, to improve the common mode input voltage range and thereby achieve the full rail-to-rail input voltage range, a folded cascode configuration for the input stage may be used. Figure 2.11(a) shows the variation in normalized input stage transconductance, defined as
as a function of bias current $I_B$ and common-mode input voltage. If the input complementary differential pairs have an overlapping constant $g_m$ region, a constant $g_m$ can be obtained simply by picking the maximum $g_m$ at any given $V_{CM}$ (see Figure 2.11(c)).

To this end, we need a circuit which compares the amplitudes of the signals at the outputs of the n- and the p-type differential pairs and redirects the largest one to the output. The Max-circuit discussed in the next section can be used for this purpose. For input voltages close to the negative supply voltage, the p-channel differential pair has a larger $g_m$ and the Max-circuit will select the output current of this stage. As $V_{CM}$ increases, $g_{mn}$ increases while $g_{mp}$ stays nearly constant. At some voltage level,
Figure 2.11: Normalized (a) $g_{mn}$ and $g_{mp}$, (b) $g_{mn}+g_{mp}$ and (c) $\max(g_{mn}, g_{mp})$ of the input stage as a function of the common-mode input voltage and the bias current.
both the n- and the p-type differential pairs have the same $g_m$ and hence the signal currents at the inputs of the Max-circuit would be equal. However, this situation does not introduce any complications, because the Max-circuit operates in a continuous manner and does not rely on switching certain transistors on or off to activate or deactivate a certain pair, as encountered in some of the existing conventional techniques, to achieve a constant $g_m$. For $V_{CM}$ close to the positive supply the output of the n-type differential pair dominates larger than the output of the p-type differential pair. As a result, the signal at the output of the Max-circuit would be equal to the output signal of the n-type differential pair. This idea is illustrated in the simplified block diagram of an Op Amp shown in Figure 2.12. This concept will be further explained in section 2.5. Using this scheme we can avoid complications of controlling the bias currents of the differential pairs.

Figure 2.12: A simplified block diagram of an Op Amp with rail-to-rail input stage. A constant $g_m$ is achieved by selecting the maximum signal current at any input common mode voltage.
The implementation of this concept is possible in two ways: processing either AC currents only (AC method) which will be discussed in this chapter or AC currents superimposed on bias currents, i.e., the total instantaneous output currents (TIC method) of the input pairs which is the subject of the next chapter.

The maximum current selecting circuit, a basic analog cell, used in the design of constant-\(g_m\) input stage, is described in the next section.

### 2.4 The Current-mode Max-circuit

![Block diagrams of the Max-circuit for different directions of the input currents and the output current.](image)

Figure 2.13: Block diagrams of the Max-circuit for different directions of the input currents and the output current.

Figure 2.13 shows the block diagrams of the current mode Max-circuit [30]. Figure 2.14(a) shows the circuit diagram of the current-mode Max-circuit of Figure 2.13(a) using an NMOS realization. The PMOS realization (dual of the NMOS realization).
is also possible and is shown in Figure 2.14(b). The bipolar realizations of the Max-circuit is shown in Figure 2.14(c) and 2.14(d) where the transistor Q6 is added to reduce the error caused by the base currents of Q3 and Q4.

Here only the n-type MOS realization will be explained. Transistors N3, N4 and N5 form a simple current mirror. Therefore, the currents through N3 and N5 are equal to the current of N4, namely $I_{in2}$. The voltage current relationship of N3 and N2 can be written as

$$I_{N3} = \frac{k_n}{2} \left( \frac{W}{L} \right) N3(V_{gs3} - V_{Tn})^2(1 + \lambda V_{ds3})$$

(2.30)

$$I_{N2} = \frac{k_n}{2} \left( \frac{W}{L} \right) N2(V_{gs2} - V_{Tn})^2(1 + \lambda V_{gs2})$$

(2.31)

where $\lambda$ is the channel length modulation factor which models the non-zero slope of the $I_d$ versus $V_d$ characteristic curve in saturation region.

The three possible scenarios for the input currents are,

a) $I_{in1} < I_{in2}$

b) $I_{in1} = I_{in2}$

c) $I_{in1} > I_{in2}$

The operation of the circuit for case (a) can be explained as follows. When $I_{in2}$ is larger than $I_{in1}$, N3 has enough gate-source voltage to sink the current $I_{in1}$. At this point transistor N3 is no longer in the saturation mode and the current mirror function of the N3-N4 pair ceases, causing the current through N3 to stop following $I_{in2}$. According to Eq. 2.31, $V_{ds3} = V_{gs2}$ is small and the current through N2 is negligible. Hence, the current mirror pair N1-N2 does not contribute to the output current. Therefore, the output current would be equal to $I_{in2}$ which in our case is equal to 29
Figure 2.14: Max-circuit of type (a) NMOS, (b) PMOS, (c) nnp and (d) pnp.
the maximum of $I_{in1}$ and $I_{in2}$. In case (b) where $I_{in1} = I_{in2}$, the current mirror pair N1-N2 is still not conducting and the output current would be equal to $I_{in2}$, which is again equal to the maximum of $I_{in1}$ and $I_{in2}$. Now let us consider the case (c) where $I_{in1} > I_{in2}$. Because N3 does not have enough gate-source voltage to sink $I_{in1}$, as Eq. 2.30 suggests, $V_{ds3}$ increases and creates a conducting path for the current difference which is equal to $I_{in1}-I_{in2}$. The copy of this current will flow through N1 and adds to the current through N5. The output current can be simply written as $I_{out} = I_{in2} + (I_{in1}-I_{in2}) = I_{in1}$. Hence, the output current is equal to $I_{in1}$ which is again equal to the maximum of $I_{in1}$ and $I_{in2}$. As can be seen the output current is always equal to the maximum of the input currents.

For ideal reproduction of the maximum current at the output. N3, N4 and N5 should be the same size. Transistors N1 and N2 should also match in order to get the exact copy of the current difference. To optimize the sizes of the transistors, several issues should be addressed. For example, consider the case where all five transistors are operating, i.e. where N3 is flooded with the current $I_{in1} > I_{in2}$. A rapid increase of $V_{ds3}$ is desirable because it turns on N2 and creates a conducting path for the current difference, $I_{in1}-I_{in2}$. To enhance the sensitivity of the circuit the output impedance of N3 and therefore its channel length should be increased. Since N3 through N5 are matched, the channel length of N4 and N5 should be increased as well. The matched pair N1-N2 should be wide enough to handle the current difference without substantial gate-source voltage.

Figure 2.15(a) shows the output current while the input currents are swept from 0 to 40μA. The error is shown in Figure 2.15(b). The maximum error is equal to 3.7%
and is mainly due to the channel length modulation effect of the transistors operating at different drain-source voltages.

![Diagram]

**Figure 2.15:** (a) Output current of the Max-circuit as a function of the input currents. (b) % Error of the Max-circuit as a function of the input currents.

All the n-type and p-type Max-circuits, shown in Figure 2.14, are unidirectional. The n-type realization operates only when the currents are flowing into the circuit while the p-type realization operates when the currents are flowing out of the circuit.

### 2.5 The new constant $g_m$ CMOS operational amplifier

To demonstrate the application of the Max-circuit an Op Amp with a constant-$g_m$ input is designed. The main idea here is that only $g_{m,\text{max}}$ is selected and used
throughout the entire input common-mode input voltage range, resulting in a rail-to-rail constant-$g_m$ input stage. For this purpose, as mentioned earlier, two different approaches are developed. The first one which processes the differential small-signal output currents (AC signal currents) is discussed in this section.

2.5.1 Principles of operation

The total instantaneous output current of the n- and p-type differential pair shown in Figure 2.1(a) can be written as

\[ I_{n1} = \frac{I_N}{2} + g_{mn} \frac{v_{id}}{2} \]  
(2.32)

\[ I_{n2} = \frac{I_N}{2} - g_{mn} \frac{v_{id}}{2} \]  
(2.33)

and

\[ I_{p1} = \frac{I_P}{2} - g_{mp} \frac{v_{id}}{2} \]  
(2.34)

\[ I_{p2} = \frac{I_P}{2} + g_{mp} \frac{v_{id}}{2} \]  
(2.35)

respectively. In the above equations, $v_{id}$ is the small signal differential input voltage and $I_N$ and $I_P$ are the tail currents of n- and p-type differential pairs respectively. Eq. 2.32 through 2.35 are general and valid regardless of the implementation in hand (MOS, Bipolar, BICMOS, etc.) and can be used to express output currents in different regions of operation, e.g., MOS weak and strong inversion regions.

As explained in section 2.2.4, the conventional methods of achieving a constant $g_m$ are based on manipulating the DC tail currents $I_N$ and $I_P$, which appear in the equation of $g_m$ in different ways depending on the VLSI technology used and on the
regions of operation. The proposed technique, on the other hand, is universal in that it is based on Eq. 2.32-2.35 without any assumption on the current dependency of the input stage transconductance. MOS circuits are used here for illustration purposes mainly because they can show both exponential (weak inversion) and square-low behavior.

As the common-mode input voltage \( V_{CM} \) is swept from rail-to-rail, the complementary input pairs go through the following three operating regions (see Figure 2.1(b)).

Assuming \( I_{BN} = I_{BP} = I_B \):

Region I:

When \( V_{CM} \) is close to the negative rail, the p-type input stage is fully operating in such a way that the tail current \( I_P \) is equal to its maximum \( I_B \) while the tail current of the n-type input stage \( I_N \) is smaller than \( I_B \). In this region we have

\[
I_N < I_P = I_B, \quad g_{mn} < g_{mp} = g_{m,\text{max}} \quad (2.36)
\]

Region II:

When \( V_{CM} \) is at mid-rail, the tail currents of both n- and p-type input pairs reach their maximum values \( I_B \). Then, we have

\[
I_N = I_P = I_B, \quad g_{mn} = g_{mp} = g_{m,\text{max}} \quad (2.37)
\]

Region III:

When \( V_{CM} \) is close to the positive rail, the n-type input pair is fully operating so that the tail current is equal to its maximum value \( I_B \) while the tail current of the p-type is smaller than \( I_B \). In this region we have

\[
I_N = I_B > I_P, \quad g_{mn} = g_{m,\text{max}} > g_{mp} \quad (2.38)
\]

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Here it is assumed that the maximum $g_{mp}$ (at the maximum $I_p$) of the p-type and the maximum $g_{mn}$ (at the maximum $I_N$) of the n-type input pairs are equal to $g_{m,\text{max}}$.

In the AC method two signal currents $i_{\text{diff}} = I_{n1} - I_{n2}$ and $I_{\text{diff}} = I_{p1} - I_{p2}$ are obtained. A constant $g_m$ is then achieved by selecting the maximum of $i_{\text{diff}}$ and $i_{\text{diff}}^2$. Based on Eq. 2.32-2.35 and 2.36-2.38, the resulting current can be written as

$$i_o = \text{MAX}(i_{\text{diff}}, i_{\text{diff}}^2) = g_{m,\text{max}} v_id$$

(2.39)

Therefore $g_m$ is constant and equal to $g_{m,\text{max}}$ regardless of the input common-mode voltage. To verify this let us discuss the operation in each of the three regions of Figure 2.1(b).

According to Eq. 2.32-2.35 and the previously mentioned conditions Eq. 2.36-2.38, $i_{\text{diff}}$ and $i_{\text{diff}}^2$ can be written as

$$i_{\text{diff}} = \text{the difference between } I_{n1} \text{ and } I_{n2}$$

$$= g_{mn} v_id \text{ in Region I}$$

$$= g_{m,\text{max}} v_id \text{ in Region II}$$

$$= g_{m,\text{max}} v_id \text{ in Region III}$$

$$i_{\text{diff}}^2 = \text{the difference between } I_{p1} \text{ and } I_{p2}$$

$$= g_{m,\text{max}} v_id \text{ in Region I}$$

$$= g_{m,\text{max}} v_id \text{ in Region II}$$

$$= g_{mp} v_id \text{ in Region III}$$

Hence the maximum value of $i_{\text{diff}}$ and $i_{\text{diff}}^2$ can be expressed as

$$i_o = \text{MAX}(i_{\text{diff}}, i_{\text{diff}}^2)_{\text{Region I,II,III}} = g_{m,\text{max}} v_id$$

(2.40)
Eq. 2.40 guarantees that $g_m$ is constant and equal to $g_{m, max}$ in the entire common-mode input voltage range. It is worth mentioning that input stage architectures based on handling small signal currents only may consume much less power when compared to the other methods.

### 2.5.2 Circuit implementation

Figure 2.16: A simplified circuit diagram of a low-voltage Op Amp using the Max-circuit.

Figure 2.16 illustrates a simplified block diagram of this Op Amp which uses a simple complementary input stage. A bi-directional operation can be achieved by using two n-type, two p-type or a combination of one n-type and one p-type Max-circuits. In order to generate the two $180^\circ$ out of phase current signals required for bi-directional operation, an additional n- and p-type input differential pair are used. The circuit diagram of the input stage is shown in Figure 2.17. Max-circuit1 (N9-N13) responds when $v_{in^+} > v_{in^-}$ and Max-circuit2 (N14-N18) responds when $v_{in^+} < v_{in^-}$. Due to the differential behavior of the input stage, all input currents to the
Figure 2.17: A constant-\(g_{in}\) input stage using two n-type Max-circuits. The arrows show the directions of the AC currents when \(v_{in}^+ > v_{in}^-\).

Max-circuit are zero when \(v_{in}^+ = v_{in}^-\). A Bipolar implementation of this input stage is also possible and is shown in Figure 2.18. In this case the npn input devices were slightly emitter-degenerated with small resistors at the emitter to make \(g_{mn}\) close to \(g_{mp}\). Simple emitter followers were also used for level shifting at the inputs to extend the common mode range closer to the rail.

Figure 2.19 shows the circuit diagram of the complete Op Amp using two n-type Max-circuits. This is not the only conceivable realization. For instance, instead of using two n-type Max-circuits, a combination of an n-type and a p-type realization may be used. However, an n-type realization is preferred due to higher electron mobility and smaller area of n-type transistors, which give rise to the superior performance at high frequencies.
Figure 2.18: The Bipolar implementation of the constant-$g_m$ Op Amp using two n-type Max-circuits.

Figure 2.19: A constant-$g_m$ Op Amp using two n-type Max-circuits including both constant-$g_m$ input stage and class-AB output stage.
2.5.3 The output stage

Almost all commercially available Op Amp’s use a class-AB output stage. Class-AB output stages can source and sink load currents which are larger than the DC quiescent current flowing through the output transistors without completely turning off one transistor or the other. The power-efficient class-AB output stages are preferable in low-power analog circuit design. Moreover, the common-source configuration of the output transistors P19-N27 guarantees maximum output voltage swing. Figure 2.20 shows the desired characteristic of the output transistor currents as a function of the load current. The exact relationship between the drain currents is not required as long as one of the transistors conduct a minimum current while the other conduct heavily [31].

![Figure 2.20: The desired drain currents of the class-AB output transistors as a function of the load current.](image)

The class-AB action is performed by keeping the voltage between the output transistors constant. The floating class-AB control circuit is formed by P16-N24, the
stacked connected transistors P17-P18 and N26-27 and current sources $I_{B1}$ and $I_{B2}$.

In order to make the quiescent current of the output transistors insensitive to supply voltage variation, the floating current sources P15-N23 is added. This current source has the same structure as the class-AB control circuit and can compensate its supply voltage dependency. The value of the current source is set by two translinear loops including P11, P15, P17, P18 and N18, N23, N25, N26.

### 2.6 Simulation and experimental results

The Op Amp shown in Figure 2.19 is implemented using a 2$\mu$m double poly double metal nwell CMOS process with $V_{Tn}=0.80$V and $V_{Tp}=0.98$V. Figure 2.21 shows the micro-photograph of the OP Amp. Transistor sizes are given in Table 2.2. The cascode current sources are used for current sources $I_{BN}$ and $I_{BP}$ in Figure 2.19 to reduce the $g_m$ variation in weak inversion usually caused by large slopes of $g_{mn}$ and $g_{mp}$ curves near both ends of input common mode voltage. Moreover, cascode current
sources can increase the CMRR. One disadvantage of cascode current source is its rather high saturation voltage, shrinking the overlap region of $g_{mn}$ and $g_{mp}$ curves. This overlap region could even diminish at relatively high bias currents. This problem can be solved by increasing the input transistors sizes at the expense of speed and die area.

The simulation results of $g_{mn}$, $g_{mp}$ and $g_{mt}$ are demonstrated in Figure 2.22(a) and (b), for strong and weak inversion, respectively. This figure shows a simulated $g_{mt}$ variation of less than 3.8%.

The measured $g_{mn}$, $g_{mp}$ and $g_{mt}$ of the implemented input stage with a bias current $1\mu A$ is shown in Figure 2.23(a) with a maximum error of 17%. The measured $g_{mn}$, $g_{mp}$ and $g_{mt}$ in weak inversion is depicted in Figure 2.23(b) where an error of 9% is observed.

The percentage variation in $g_{mt}$ is defined as

<table>
<thead>
<tr>
<th>Transistor</th>
<th>Size</th>
<th>Transistor</th>
<th>Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>N1-N8</td>
<td>40/2</td>
<td>P1-P8</td>
<td>108/2</td>
</tr>
<tr>
<td>N9-N18</td>
<td>15/2</td>
<td>P9-P10</td>
<td>30/2</td>
</tr>
<tr>
<td>N19-N22</td>
<td>30/4</td>
<td>P11-P14</td>
<td>84/4</td>
</tr>
<tr>
<td>N23</td>
<td>10/4</td>
<td>P15</td>
<td>28/4</td>
</tr>
<tr>
<td>N24</td>
<td>8/4</td>
<td>P16</td>
<td>20/4</td>
</tr>
<tr>
<td>N25-N26</td>
<td>5/4</td>
<td>P17-P18</td>
<td>14/4</td>
</tr>
<tr>
<td>N27</td>
<td>40/2</td>
<td>P19</td>
<td>103/2</td>
</tr>
</tbody>
</table>

Table 2.2: Transistor sizes of the CMOS Op Amp designed using AC method.
Figure 2.22: Simulated $g_{mn}$, $g_{mp}$ and $g_{mt}$ of the Op Amp when input is swept from 0 to 3V. (a) with $I_{BN} = I_{BP} = 1\mu A$ and an error of 9.4%. (b) with $I_{BN} = I_{BP} = 20\mu A$ and an error of 10.3%.
Figure 2.23: Measured $g_{mn}$, $g_{mp}$ and $g_{nt}$ of the Op Amp when input is swept from 0 to 3V. (a) with $I_{BN} = I_{BP} = 1\mu A$ and an error of 17%. (b) with $I_{BN} = I_{BP} = 20nA$ and an error of 9%.
\[ g_{mt,\text{variation}} = \frac{MAX(g_{mt}) - MIN(g_{mt})}{g_{mt,\text{avg}}} \] \hspace{1cm} (2.41)

and \( g_{mt,\text{avg}} \) is defined as

\[ g_{mt,\text{avg}} = \frac{1}{V_{CM,\text{MAX}} - V_{CM,\text{MIN}}} \int_{V_{CM,\text{MIN}}}^{V_{CM,\text{MAX}}} g_{ml}(V_{CM})dV_{CM} \] \hspace{1cm} (2.42)

\[ \approx \frac{1}{n} \sum_{i=1}^{n} g_{mt,i} \]

where \( n \) is the total number of data points.

The simulation results of the bipolar input stage transconductances are shown in Figure 2.24, which shows \( g_{mt} \) variation of almost 7%.

![Figure 2.24: Simulated transconductance of the bipolar input stage with \( I_{BN} = I_{BP} = 15 \, \mu A \).](image)

The simulated output transistors' (N19 and P19) currents as function of the load current are depicted in Figure 2.25. This figure clearly shows the Class-AB operation.
of the output stage. Figure 2.26 depicts the simulated input-output voltage behavior of the unity gain buffer configuration when the input is swept from 0 to 3V. The experimental characteristic is shown in Figure 2.27. The measured input offset voltage is shown in Figure 2.28 with a maximum of 7mV.

![Simulated output transistor currents as function of load current $I_{load}$](image)

**Figure 2.25:** Simulated output transistor currents as function of load current $I_{load}$.

With the unity gain buffer implementation of Figure 2.19 operating in the strong inversion region with $I_{BN} = I_{BP} = 1 \mu A$, Figure 2.29 shows the simulated transient behavior when a rectangular pulse is applied to the input with a slew rate of 0.17 V/µSec. Figure 2.30 shows the measured transient response under the same circumstances. The measured slew-rate is equal to 0.04V/µSec which is smaller than the simulated slew-rate.
Figure 2.26: Simulated input-output behavior of the Op Amp in unity gain configuration when input is swept from 0 to 3V.

Figure 2.27: Measured input-output behavior of the Op Amp in unity gain configuration when input is swept from 0 to 3V.
Figure 2.28: DC offset voltage of the Op Amp in the unity gain configuration when input is swept from 0 to 3V.

Figure 2.29: Simulated transient behavior of the Op Amp with a bias current of $I_{BN} = I_{BP} = 1\mu A$ when a rectangular pulse is applied to the input. This figure shows an slew-rate of 0.17 V/\mu Sec
Figure 2.30: Measured transient behavior of the Op Amp with a bias current of $I_{BN} = I_{BP} = 1\mu A$ when a rectangular pulse is applied to the input.

The Open loop frequency frequency response of the proposed circuit in strong ($I_{BN} = I_{BP} = 1\mu A$) and weak ($I_{BN} = I_{BP} = 20nA$) inversion regions with different values of the common mode voltages ($V_{CM} = 0.5, 1.5$ and $2.5V$) are shown in Figure 2.31 and 2.32, respectively. In strong inversion the simulated unity gain frequency and phase margin are $77kHz$ and nearly $40^\circ$ respectively, while in weak inversion the simulation shows a unity gain frequency and phase margin of $2kHz$ and $68^\circ$, respectively. The measured DC gain, unity gain frequency and phase margin of the Op Amp are presented in Table 2.3.

Figure 2.33 shows the frequency spectrum of the Op Amp in unity gain configuration at $1KHz$ for five different common mode voltages. The DC gain, unity gain frequency and phase margin for different values of $V_{CM}$ and bias current of $1\mu A$ and $20nA$ are summarized in Table 2.4 and 2.6, respectively. Table 2.5 presents the simulated CMRR of the Op Amp for different values of common mode voltage.
### Table 2.3: Measured DC gain, unity gain frequency and phase margin of the Op Amp.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Measured</th>
<th>Simulated</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Open loop gain</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>@ $V_{CM}=0.5\text{V}$</td>
<td>70</td>
<td>75</td>
</tr>
<tr>
<td>@ $V_{CM}=1.5\text{V}$</td>
<td>72</td>
<td>72</td>
</tr>
<tr>
<td>@ $V_{CM}=2.5\text{V}$</td>
<td>70</td>
<td>70</td>
</tr>
<tr>
<td><strong>Unity gain frequency</strong></td>
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<td></td>
</tr>
<tr>
<td>@ $V_{CM}=0.5\text{V}$</td>
<td>72</td>
<td>80</td>
</tr>
<tr>
<td>@ $V_{CM}=1.5\text{V}$</td>
<td>72</td>
<td>70</td>
</tr>
<tr>
<td>@ $V_{CM}=2.5\text{V}$</td>
<td>80</td>
<td>60</td>
</tr>
<tr>
<td><strong>Unity gain phase margin</strong></td>
<td></td>
<td></td>
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<tr>
<td>@ $V_{CM}=0.5\text{V}$</td>
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<tr>
<td>@ $V_{CM}=2.5\text{V}$</td>
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<td>50</td>
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Figure 2.31: Simulated open loop frequency response of the Op Amp with $I_{BN} = I_{BP} = 1\mu\text{A}$. 

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Figure 2.32: Simulated open loop frequency response of the Op Amp with $I_{BN} = I_{BP} = 20\text{nA}$. 
Figure 2.33: Measured frequency spectrum of the Op Amp in unity gain configuration with a bias current of $I_{BN} = I_{BP} = 1\mu A$ and a 1KHz sine wave is applied to the input.
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<thead>
<tr>
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<th>$f_U(KHz)$</th>
<th>$\phi^o$</th>
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Table 2.4: Simulated frequency response of the Op Amp with $I_{BN} = I_{BP} = 1\mu A$, $R_L=10K$ and $C_L=10pf$. 

52
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Table 2.5: Simulated CMRR of the Op Amp with $I_{BN} = I_{BP} = 1\mu A$, $R_L=10K$ and $C_L=10\mu F$. 

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Table 2.6: Simulated frequency response of the Op Amp with \( I_{BN} = I_{BP} = 20nA, R_L=10K \) and \( C_L=10pf \).
CHAPTER 3

CONSTANT-$g_m$ INPUT STAGE; TIC METHOD

3.1 Introduction

In this chapter a new approach to designing a constant-$g_m$ input stage will be presented. This method is based on the idea presented in Chapter 2; i.e., at any input common mode voltage the maximum signal should be selected and directed to the gain stage. The approach adopted here is unique in that we attempt to track regions of constant $g_{mn}$ and $g_{mp}$ of the input differential pairs while selecting the maximum signal current at any $V_{CM}$. This method radically simplifies the design procedure while maintaining small variation in $g_{mt}$. Hence it is particularly useful in the context of creating analog VLSI cell libraries for low voltage applications.

This method, referred to as, the TIC (Total Instantaneous Current) method, is different from the AC method presented in Chapter 2 in that rather than instead of monitoring the signal current (AC signal) itself we monitor the total instantaneous current (AC+DC) of the input differential pairs. The proposed input stage is also universal and maintains nearly constant $g_{mt}$ regardless of the operating region of the input transistors. Although in general the TIC method can be extended to a constant-$g_m$ bipolar input stage, the implementation presented in this chapter is limited to CMOS technology.
3.2 Principles of operation

As explained in Chapter 2, rail-to-rail operation of the input stage can be achieved by utilizing one n-type and one p-type input differential pair in parallel, forming a complementary differential input stage [14]. The resulting complementary input differential pair along with its three different regions of operation are shown in Figure 3.1(a) and Figure 3.1(b), respectively. In the TIC method, the total instantaneous currents of the input stage, namely $I_{n1}$, $I_{n2}$, $I_{p1}$, and $I_{p2}$ will be monitored and processed.

![Diagram](a) ![Diagram](b)

Figure 3.1: (a) Complementary rail-to-rail input stage. (b) $g_{mn}$ and $g_{mp}$ of a complementary MOS input stage as a function of $V_{CM}$. 
The total instantaneous drain currents, when $v_{in^+} > v_{in^-}$, are

\[ I_{n1} = \frac{I_N}{2} + \frac{g_{mn} v_{id}}{2} \]  
\[ I_{n2} = \frac{I_N}{2} - \frac{v_{id}}{2} \]  
\[ I_{p1} = \frac{I_P}{2} - \frac{g_{mp} v_{id}}{2} \]  
\[ I_{p2} = \frac{I_P}{2} + \frac{g_{mp} v_{id}}{2} \]

where $v_{id} = v_{in^+} - v_{in^-}$, is the small signal differential input voltage and $I_N$ and $I_P$ are the tail currents of n- and p-type differential pairs, respectively. These equations are general and valid regardless of the input stage transistors’ operating regions, i.e. strong or weak inversion.

As $V_{CM}$ changes from rail to rail, the complementary differential pair goes into three different regions of operation shown as region I, II and III in Figure 3.1(b).

In region I, since $V_{CM}$ is close to $V_{SS}$, only the p-type differential pair is operating so that

\[ I_N < I_P = I_B, \quad g_{m,max} = g_{mp} > g_{mn} \]  

In region II, since $V_{SS} + V_T n < V_{CM} < V_{DD} - | V_{Tp} |$, both the n- and p-type differential pairs are operating so that

\[ I_P = I_N = I_B, \quad g_{m,max} = g_{mp} = g_{mn} \]

Finally in region III, since $V_{CM} > V_{DD} - | V_{Tp} |$, only the n-type differential pair is operating and the following holds

\[ I_N = I_B > I_P, \quad g_{m,max} = g_{mn} > g_{mp} \]
These equations are written assuming the n- and p-type transistors are scaled such that the maximum of $g_{mn}$ and $g_{mp}$ are equal.

The proposed input stage is shown in Figure 3.2. It consists of the complementary differential pairs N1-N2 and P1-P2 and two floating current mirrors depicted inside dashed borders. Each mirror uses a pair of composite CMOS transistors. The composite transistor can be viewed as a single NMOS or PMOS transistor with an effective threshold voltage and transconductance parameter of [32, 16]

$$V_{Teq} = V_{Tn} + |V_{Tp}| \quad (3.8)$$

and

$$\frac{1}{\sqrt{K_{eq}}} = \frac{1}{\sqrt{K_n}} + \frac{1}{\sqrt{K_p}} \quad (3.9)$$

respectively. Where $K_n$ and $K_p$ are defined as $k_n(\frac{W}{L})_n$ and $k_p(\frac{W}{L})_p$, respectively.

The current through the controlling branch of the floating current mirrors, N7-P7 and N10-P10, has a value which is the minimum of the available source and sink currents. This is because in a series connection of a CMOS current source and a current sink, the smallest current dominates[5].

With 1:1 mirrors, $I_{m1} = I_1 = I_4$, $I_{m2} = I_2 = I_3$ and we can write

$$I_{m1} = I_1 = I_4 = MIN(I_B - I_{n1}, I_B - I_{p2}) \quad (3.10)$$

$$I_{m2} = I_2 = I_3 = MIN(I_B - I_{n2}, I_B - I_{p1}) \quad (3.11)$$

Eq. 3.10 and Eq. 3.11 can be rewritten as

$$I_{m1} = I_1 = I_4 = I_B - MAX(I_{n1}, I_{p2}) \quad (3.12)$$

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Figure 3.2: Circuit diagram of the low-voltage, rail-to-rail input stage.
\( I_{m2} = I_2 = I_3 = I_B - \text{MAX}(I_{n2}, I_{p1}) \quad (3.13) \)

The currents \( I_1 \) through \( I_4 \) are added according to

\[ I_o = I_2 - I_1 + I_3 - I_4 \quad (3.14) \]

which yields an output current, \( I_o \), given by

\[ I_o = 2\text{MAX}(I_{n1}, I_{p2}) - 2\text{MAX}(I_{n2}, I_{p1}) \quad (3.15) \]

At low \( V_{CM} \) where \( I_{p1} > I_{n2} \) and \( I_{p2} > I_{n1} \), Eq. 3.15 reduces to

\[ I_o = 2(I_{p2} - I_{p1}) = 2v_{id}g_{mp} = 2v_{id}g_{m,max} \quad (3.16) \]

while at \( V_{CM} \) close to the positive supply voltage, \( I_{n1} > I_{p2} \) and \( I_{n2} > I_{p1} \) which results in

\[ I_o = 2(I_{n1} - I_{n2}) = 2v_{id}g_{mn} = 2v_{id}g_{m,max} \quad (3.17) \]

For \( V_{CM} \) at mid-rail where \( I_{n1} = I_{p2} \) and \( I_{n2} = I_{p1} \) the output current is

\[ I_o = 2v_{id}g_{mn} = 2v_{id}g_{mp} = 2v_{id}g_{m,max} \quad (3.18) \]

Thus at any given \( V_{CM} \), the resulting input stage transconductance is constant and equal to the maximum transconductance.

In order to show how this maximum signal selection takes place, part of the input stage is redrawn in Figure 3.3. This figure also shows the signal wave forms for the operation in region III where \( V_{CM} \) is close to \( V_{DD} \). At \( V_{CM} \) close to \( V_{DD} \) the n-type differential pair shows a larger tail current and transconductance than the p-type differential pair. Therefore, we have \( I_N > I_P \) and \( g_{mn} > g_{mp} \) and the current \( I_1 = I_B - I_{n1} \) has lower DC current than \( I_2 = I_B - I_{p2} \). As mentioned above, the minimum
current in this branch dominates and the current flowing through the floating current mirror N7 and P7 would be equal to $I_1$ which has a lower DC current but carries the maximum signal current. This current will be copied to $I_m$ by N8 and P8 at the output of the floating current mirror. It is important to note that in this case the lower current source goes into the linear region and ceases to operate as a current source.

Figure 3.4(a) shows the current $I_m$ (see Figure 3.3) as a function of $I_{n1}$ and $I_{p2}$ when these currents are swept from 0 to 4μA. Figure 3.4(b) depicts the mathematical function $\min(I_{n1}, I_{p2})$. Evidently, the circuit shown in the broken line border in Figure 3.3 can be viewed as a circuit realization of the mathematical $\min()$ function.
as can be proved by the relatively small error between Figure 3.4(a) and Figure 3.4(b) as shown in Figure 3.4(c).

![Figure 3.4: (a) $I_m$ as a function of $I_{n1}$ and $I_{p2}$ as they are swept from 0 to 4 $\mu$A (b) $I_m$ as evaluated by the mathematical function $min(I_{n1}, I_{p2})$ (c) the difference between the circuit output shown in (a) and ideal output shown in (b).](image)

An Op Amp is designed using the described constant-$g_m$ input stage. The circuit diagram of this Op Amp is shown in Figure 3.5. This Op Amp uses the same output stage explained in Chapter 2.
Figure 3.5: The complete circuit diagram of the Op Amp with a constant-$g_m$ input stage based on the TIC method.

### 3.3 Simulation and experimental results

The Op Amp shown in Figure 3.5 is implemented using a 2$\mu$m double poly, double metal, nwell CMOS process with $V_{Tn}=0.80\text{V}$ and $V_{Tp}=0.98\text{V}$. Figure 3.6 shows the micro-photograph of the Op Amp. Transistor sizes are given in Table 3.1.

The simulation results of $g_{mn}$, $g_{mp}$ and $g_{mt}$ of the input stage shown in Figure 3.2 are demonstrated in Figure 3.7. This figure shows simulated $g_{mt}$ variations of less than 4.8% and 13.4% at 2$\mu$A and 3$\mu$A, respectively. In weak inversion the errors are 24.9% and 24.5% at 20nA and 30nA, respectively.

The experimental measurement of $g_{mn}$, $g_{mp}$ and $g_{mt}$ of the implemented input stage is shown in Figure 3.8 with an error of 6% and 14% at 2$\mu$A and 3$\mu$A, respectively. This input stage shows an error of 20% and 24% in weak inversion when the bias currents are 20nA and 30nA, respectively. Part of the error for both simulation and experiment can be contributed to the $g_m$ variations of the n- and p-pair input differential stages in their operating regions as is evident by non-zero slope of $g_{mn}$.
Figure 3.6: The micro-photograph of the implemented Op Amp using 2μm double poly, double metal nwell CMOS process.

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Table 3.1: Transistor sizes of the CMOS Op Amp designed using the TIC method.
Figure 3.7: Simulated $g_m$ of the input stage (a) at 2μA, 3μA with an error of 4.8%, 13.4% and (b) at 20nA and 30nA with an error of 24.9% and 24.5%, respectively.

and $g_{mp}$ curves. If these variations are excluded the error due to maximum selecting current circuit is at most 12% and 22% in strong and weak inversion, respectively. This figure also shows that the input $V_{CM}$ can exceed either rail by almost 0.3V.

With the unity gain buffer implementation of the Op Amp shown in Figure 3.5 operating in strong inversion with $I_B = 3μA$, Figure 3.9 shows the simulated transient behavior when a rectangular pulse is applied to the input with slew-rate of 0.617V/μsec. Figure 3.10 shows the measured transient response under the same circumstances. The measured slew-rate is equal to 0.6V/μsec which is in close agreement with the simulated value.
Figure 3.8: Measurement results of $g_m$ (a) in strong inversion, $I_B=2\mu A$ and $3\mu A$ with an error of 6%, 14% and (b) in weak inversion, $I_B=20nA$ and $30nA$ with an error of 20% and 24%, respectively.
Figure 3.9: Simulated transient behavior of the Op Amp with a bias current of $I_B = 3\mu A$ when a rectangular pulse is applied to the input. This figure shows an slew-rate of $0.617 \text{ V/\mu sec}$.

Figure 3.10: Measured transient behavior of the Op Amp with a bias current of $I_B = 3\mu A$ when a rectangular pulse is applied to the input.
Figure 3.11 depicts the simulated input-output voltage behavior of the unity gain buffer configuration when the input is swept from 0 to 3V. The experimental characteristics (shown in Figure 3.12) are once again in accord with the simulated result. The maximum and minimum output voltages are 0.08V and 2.91V, respectively. The measured input offset voltage is shown in Figure 3.13 with a maximum of 6mV.

![Graph showing input-output behavior](image)

Figure 3.11: Simulated input-output behavior of the Op Amp in unity gain configuration when input is swept from 0 to 3V.

The open loop frequency response of the proposed circuit in strong ($I_B = 3\mu A$) and weak ($I_B = 20nA$) inversion regions with different values of the common mode voltages ($V_{CM} = 0.5, 1.5$ and $2.5V$) are shown in Figures 3.14 and 3.15, respectively. In strong inversion the measured unity gain frequency and phase margin is nearly 617KHz and 61°, respectively. Simulated values for gain, unity gain frequency and
Figure 3.12: Measured input-output behavior of the Op Amp in unity gain configuration when input is swept from 0 to 3V.

Figure 3.13: DC offset voltage of the Op Amp in the unity gain configuration when input is swept from 0 to 3V.
phase margin for different values of $V_{CM}$ for $I_B = 3\mu A$ and $10nA$ are given in Table 3.2 and 3.3, respectively.

Figure 3.14: Simulated open loop frequency response of the Op Amp with $I_B=3\mu A$ and different values of $V_{CM}$.

Figure 3.16 shows the measured frequency spectrum of the Op Amp in unity gain configuration at 1KHz with $I_B=3\mu A$ for three different common mode voltages.

The simulated output transistors' (N19 and P19) currents as functions of the load current are depicted in Figure 3.17. This figure clearly shows the Class-AB operation of the output stage. The simulated Common Mode Rejection Ratio (CMRR) of the Op Amp as a function of $V_{CM}$ for strong and weak inversion are given in Table 3.4 and 3.5, respectively. Figure 3.18 graphs the simulated CMRR of the Op Amp at 1Hz.
Figure 3.15: Simulated open loop frequency response of the Op Amp with $I_B=20\text{nA}$, $R_L=10\text{K}$ and different values of $V_{CM}$.

Figure 3.16: Measured frequency spectrum of the Op Amp in unity gain configuration with a bias current of $I_B=3\mu\text{A}$ and a 1KHz sine wave is applied to the input.
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Table 3.2: Simulated frequency response of the Op Amp with $I_B = 3\mu A$, $R_L = 2K$ and $C_L = 10$pf.
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Table 3.3: Simulated frequency response of the Op Amp with $I_B = 20\text{nA}$, $R_L = 10\text{K}$ and $C_L = 10\text{pf}$.
Figure 3.17: Simulated output transistor currents as function of load current $I_{load}$.

Figure 3.18: The CMRR of the Op Amp at 1Hz with $I_B = 3\mu A$, $R_L=2K$ and $C_L=10\text{pf}$. 

74
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Table 3.4: Simulated CMRR of the Op Amp with $I_B = 3\mu A$, $R_L = 2K$ and $C_L = 10$pF.
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Table 3.5: Simulated CMRR of the Op Amp with $I_B = 20\,nA$, $R_L = 10K$ and $C_L = 10\,pf$.  

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The simulation results of the Power Supply Rejection Ratio (PSRR) for both positive and negative (0V in our case) supplies are illustrated in Figures 3.19 and 3.20, respectively. A minimum PSRR of 90dB is observed for $V_{CM}=2.5V$. Table 3.6 summarizes the measured parameters of the Op Amp.

Figure 3.19: Simulated power supply rejection ratio of the Op Amp for different values of $V_{CM}$ with $I_B=3\mu A$, $R_L=10K$: (a) Positive supply, (b) Negative supply
Figure 3.20: Power supply rejection ratio of the Op Amp for different values of $V_{CM}$ with $I_B = 20\text{nA}$ and $R_L=10\text{K}$: (a) Positive supply, (b) Negative supply.
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<th>RL=10K, CL=10pf, IB=3μA</th>
<th>Supply Voltage</th>
<th>Quiescent current</th>
<th>Output voltage swing</th>
<th>Offset voltage</th>
<th>Open loop gain</th>
<th>Unity gain frequency</th>
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Table 3.6: Measured parameters of the Op Amp.
CHAPTER 4

Low-voltage Analog Multiplier

4.1 Introduction

Analog multipliers have found many applications in communications and analog signal processing circuits. There are two basic types of analog multipliers; the one-quadrant analog multiplier which is restricted to input signals of only one polarity, and four-quadrant analog multipliers which can operate on input signals with either polarity. This chapter mainly concentrates on the design of four-quadrant analog multipliers due to their versatility and widespread application.

The conventional analog multiplier schemes based on variable transconductance principles which lend themselves well to bipolar technology can not be easily extended to MOS technology. This is mainly due to hard-to-cancel inter-coupled terms in the output current equations. Another class of the four-quadrant analog multipliers can be realized using square law operation of MOS transistors in the saturation region. The input voltage range of these multipliers is rather restricted, an important disadvantage in low-voltage applications. The input voltage range can be extended using active attenuators [33] at the expense of lower signal to noise ratio and increased nonlinearity. This chapter presents a new method to enhance the input voltage range using current-mode maximum selecting circuit (Max-circuit) introduced in Chapter
2 [34]. The multiplier discussed in this chapter shows high input resistance for all inputs and avoids the use of voltage attenuators, thereby considerably enhancing the signal to noise ratio.

This chapter is organized as follows: Section 4.2 introduces some definitions used in this chapter. Section 4.3 explains the structure and operating region of the simple composite transistors. Section 4.4 discusses the square-law based multiplier using a simple composite transistor. Section 4.5 introduces the new multiplier architecture with an extended differential input voltage range.

4.2 Definitions

The input-output transfer relationship of a four-quadrant-analog multiplier can be expressed as

\[ V_o = KV_{12}V_{34} \quad (4.1) \]

where \( V_{12} \) and \( V_{34} \) are two differential inputs and \( V_o \) is the output voltage. The multiplier scale factor, namely \( K \), is usually set in such a way to allow full-scale output when full-scale inputs are applied [35]. Consequently, for a \( V_{DD}-V_{SS} \) supply voltage range, \( K \) will be equal to

\[ K = \frac{1}{V_{DD} - V_{SS}} \quad (4.2) \]

The input voltage range of an analog multiplier is usually restricted to a fraction of the power supply voltage. Hence, it is convenient to express the input voltages in terms of a differential voltage superimposed on a common-mode voltage, i.e.,

\[ V_1 = V_{CM1} + \frac{v_{d1}}{2} \quad V_2 = V_{CM1} - \frac{v_{d1}}{2} \quad (4.3) \]

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and

\[ V_3 = V_{CM2} + \frac{v_{d2}}{2} \quad V_4 = V_{CM} - \frac{v_{d2}}{2} \]  \hspace{1cm} (4.4)\]

where \( V_{CM1} \) and \( V_{CM2} \) are the input common-mode voltages. Input differential voltages are denoted by \( v_{d1} \) and \( v_{d2} \) and are defined as

\[ v_{d1} = V_1 - V_2 \]  \hspace{1cm} (4.5)\]

and

\[ v_{d2} = V_3 - V_4 \]  \hspace{1cm} (4.6)\]

### 4.3 CMOS composite transistor

The current through an MOS transistor in the saturation region shows the square law dependency on the gate-source voltage. The drain current of an n- or p-type MOS transistor can be written as

\[ I_d = \frac{K_n}{2} (V_{gs} - V_{Tn})^2 \]  \hspace{1cm} (n-type) \hspace{1cm} (4.7)\]

\[ I_d = \frac{K_p}{2} (V_{gs} - |V_{Tp}|)^2 \]  \hspace{1cm} (p-type) \hspace{1cm} (4.8)\]

respectively. In the above equations \( K_n, V_{Tn} \) and \( K_p, V_{Tp} \) are the transconductance parameter and the threshold voltage of NMOS and PMOS transistors, respectively.

Eq. 4.7 and 4.8 show that a single MOS transistor is able to generate the square-law current-voltage characteristic required in many signal processing applications such as analog multipliers and voltage-to-current converters. However, in most cases, the low input impedance at the source of the transistor restricts the applicability of the single transistor solution and calls for more elaborate designs. Moreover, in
many applications, the generated currents of NMOS and PMOS transistors should be combined in one way or another to implement the desired signal processing task. For proper operation, these signal processing circuits rely on the assumption that the NMOS and PMOS transconductance parameters namely $K_n$ and $K_p$ are equal, a far reaching goal due to inevitable process variations. The aforementioned problems can be alleviated by combining one MOS and one PMOS transistor to form a composite transistor [32] as illustrated in Figure 4.1.

![Composite transistor formed by combining one NMOS and one PMOS transistor.](image)

Figure 4.1: Composite transistor formed by combining one NMOS and one PMOS transistor.

The resulting composite transistor offers two high impedance terminals which can be used interchangeably as gate and source terminals. It can be shown that the current through this composite pair is equal to [16]

$$I_d = \frac{K_{eq}}{2}(V_{gs} - V_{Teq})^2$$

(4.9)

where $K_{eq}$ and $V_{Teq}$ are the equivalent transconductance parameter and the threshold voltage of the composite transistor, respectively. The equivalent transconductance
parameter, $K_{eq}$, is related to $K_n$ and $K_p$ by

$$\frac{1}{\sqrt{K_{eq}}} = \frac{1}{\sqrt{K_n}} + \frac{1}{\sqrt{K_p}}$$  (4.10)

and $V_{T_{eq}}$ is given by

$$V_{T_{eq}} = V_{Tn} + |V_{Tp}|$$  (4.11)

---

Figure 4.2: Normalized drain current $\frac{I_d}{K_{eq}}$ of a composite transistor as a function of gate and source voltages.

Eq. 4.11 shows that the simple composite transistor has a larger threshold voltage as compared to a single MOS transistor. This high threshold voltage limits the operating voltage range of the transistor to a small fraction of the total supply voltage range which constitutes the main drawback of this device in low-voltage applications. Figure 4.2 shows the normalized drain current $\frac{I_d}{K_{eq}}$ of the composite transistor as a function of both gate and source voltages. The input voltage range of the composite transistor is limited to the gate and source voltages which satisfies the condition $V_g - V_s \geq V_{T_{eq}}$. 

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Depending on the relative value of the gate and source voltages, a composite transistor can be used either as an NMOS or PMOS transistor. Moreover, it has the advantage that its transconductance parameter exhibits similar functional dependency on both $K_n$ and $K_p$. This property assures that the composite transistor, whether used as n- or p-type composite transistor exhibits the same transconductance parameter, a highly desirable feature in low voltage analog circuit design.

### 4.4 Square-law based analog multiplier

Figure 4.3 shows the block diagram of a square-law based four quadrant analog multiplier [36]. Although each building block in Figure 4.3 can be implemented using a single MOS transistor, we are more interested in the composite transistor implementation which leads to a more linear and simpler design.

The currents $I_{13}$, $I_{14}$, $I_{23}$ and $I_{24}$ are given by the following equations, assuming that the transconductance parameter and the threshold voltage of each block is equal
to $K_{eq}$ and $V_{Teq}$, respectively.

$$I_{13} = \frac{K_{eq}}{2} (V_1 - V_3 - V_{Teq})^2 \quad (4.12)$$

$$I_{14} = \frac{K_{eq}}{2} (V_1 - V_4 - V_{Teq})^2 \quad (4.13)$$

$$I_{23} = \frac{K_{eq}}{2} (V_2 - V_3 - V_{Teq})^2 \quad (4.14)$$

$$I_{24} = \frac{K_{eq}}{2} (V_2 - V_4 - V_{Teq})^2 \quad (4.15)$$

The output current, $I_{out}$, can be evaluated as

$$I_{out} = I_{14} + I_{23} - I_{24} - I_{13} = K_{eq} (V_1 - V_2) (V_3 - V_4) \quad (4.16)$$

Figure 4.4 shows a possible implementation of the multiplier using simple composite transistors. For proper operation $V_1$ and $V_2$ should be larger than $V_3$ and $V_4$ by at least $V_{Teq}$.

The region of operation for this multiplier is shown in Figure 4.5. This Figure shows that the multiplier is operating only when all four input voltages, namely $V_1$, $V_2$, $V_3$ and $V_4$, fall in the triangular pedestal.

The rectangular, double cross hatched region of Figure 4.6 shows the input voltage range for symmetrical operation, i.e. when the input voltages have the same differential input magnitudes. In this case maximum peak-to-peak differential input voltages are limited to

$$v_{12,max} = v_{34,max} = \frac{V_{DD} - V_{SS} - V_{Teq}}{2} \quad (4.17)$$

A voltage level shifter can be used in conjunction with the input voltages to move this triangular region of operation in the $(V_1,V_2)$, $(V_3,V_4)$ plane. This idea is
Figure 4.4: CMOS implementation of the square-law based multiplier using simple composite transistors.

Figure 4.5: Region of operation of the CMOS multiplier shown in Figure 4.4. For proper operation $V_1$ through $V_4$ should be confined in the pedestal area.
Figure 4.6: Input voltage range of the basic four-quadrant analog multiplier cell.

Figure 4.7: Basic four-quadrant analog multiplier cell (CELL 1) where $V_1$ and $V_2$ are shifted up and $V_3$ and $V_4$ are shifted down.
illustrated in Figure 4.7. Assuming $K_{p,P5}=K_{p,P6}=K_{p,s}$ and $K_{p,N3}=K_{p,N6}=K_{n,s}$, the shifted voltages $V_{1s}$ through $V_{4s}$ can be written as

\begin{align}
V_{1s} &= V_1 + |V_{Tp}| + \sqrt{\frac{2IB_1}{K_{p,s}}} \\
V_{2s} &= V_2 + |V_{Tp}| + \sqrt{\frac{2IB_1}{K_{p,s}}} \\
V_{3s} &= V_3 - V_Tn - \sqrt{\frac{2IB_1}{K_{n,s}}} \\
V_{4s} &= V_4 - V_Tn - \sqrt{\frac{2IB_1}{K_{n,s}}}
\end{align}

The new region of operation is shown in Figure 4.8. In this figure $V_X$ and $V_Y$ are equal to

![Figure 4.8: Input voltage range of the four-quadrant analog multiplier cell shown in Figure 4.7.](image)

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\[ V_X = V_{T_p} + V_{DS_{sat}} + \sqrt{\frac{2IB_1}{K_{p,s}}} \]  \hspace{1cm} (4.22)

\[ V_Y = V_{T_n} + V_{DS_{sat}} + \sqrt{\frac{2IB_1}{K_{n,s}}} \]  \hspace{1cm} (4.23)

where \( V_{DS_{sat}} \) is the drain-source saturation voltage of the current sources. The region of operation extends beyond the diagonal line by

\[ V_e = \sqrt{\frac{2IB_1}{K_{p,s}}} + \sqrt{\frac{2IB_1}{K_{n,s}}} \]  \hspace{1cm} (4.24)

The incorporation of level shifters allow the common mode input voltages to approach the middle of the supply voltage range. However, the maximum allowable input differential voltages stay the same as the area of the triangle remains unaltered.

Figure 4.9: Basic four-quadrant analog multiplier cell (CELL 2) where \( V_1 \) and \( V_2 \) are shifted down and \( V_3 \) and \( V_4 \) are shifted up.

A second multiplier cell (CELL 2) can be implemented by interchanging \( V_1 \) with \( V_3 \) and \( V_2 \) with \( V_4 \). The resulting circuit diagram and its corresponding region of
Figure 4.10: Input voltage range of the four-quadrant analog multiplier cell shown in Figure 4.9.

operation are shown in Figure 4.9 and 4.10, respectively. The shifted voltages $V'_{1s}$ through $V'_{4s}$ in Figure 4.9 can be written as

$$V'_{1s} = V_1 - V_{Tn} - \sqrt{\frac{2IB_1}{K_{n,s}}}$$  \hspace{1cm} (4.25)

$$V'_{2s} = V_2 - V_{Tn} - \sqrt{\frac{2IB_1}{K_{n,s}}}$$  \hspace{1cm} (4.26)

$$V'_{3s} = V_3 + |V_{Tp}| + \sqrt{\frac{2IB_1}{K_{p,s}}}$$  \hspace{1cm} (4.27)

$$V'_{4s} = V_4 + |V_{Tp}| + \sqrt{\frac{2IB_1}{K_{p,s}}}$$  \hspace{1cm} (4.28)

As can be seen in Figures 4.8 and 4.10, the two implementations of the basic multiplier cell covers different input voltage ranges with a small overlap. Hence, it is possible to cover a larger area in $(V_1, V_2)$, $(V_3, V_4)$ plane by employing the two multipliers in a cooperative way. The basic idea here is to combine the outputs of the
two aforementioned basic cells, i.e., CELL 1 and CELL 2, in such a way as to extend the input voltage range beyond that achievable by using a single multiplier cell. This idea is illustrated in Figure 4.11.

![Figure 4.11: A larger signal swing can be achieved by combining the outputs of the two multiplier cells with different operating input voltage range using current-mode Max-circuits.](image)

This method uses current-mode maximum selecting circuits (Max-circuits), described in Chapter 2, in order to unite the operating regions of the individual cells to form a larger operating voltage range. As suggested in Figure 4.11 the input differential voltages can be increased nearly two times.
4.5 Four-quadrant multiplier with extended input voltage range

Figure 4.12 shows the partial circuit diagram of the proposed multiplier. This circuit is composed of two four quadrant square-law based multipliers and four current-mode Max-circuits.

![Circuit Diagram](image)

Figure 4.12: Circuit diagram of the low-voltage four-quadrant analog multiplier with extended input voltage range.

Using Eq. 4.9 and Eqs. 4.18-4.21 the output currents of CELL 1 can be written as follows:

\[ I_{13} = \frac{K_{eq}}{2} (V_1 - V_3 + \alpha + \beta)^2 \]  
\[ I_{14} = \frac{K_{eq}}{2} (V_1 - V_4 + \alpha + \beta)^2 \]  
\[ I_{23} = \frac{K_{eq}}{2} (V_2 - V_3 + \alpha + \beta)^2 \]  
\[ I_{24} = \frac{K_{eq}}{2} (V_2 - V_4 + \alpha + \beta)^2 \]
where \( \alpha \) and \( \beta \) are defined as \( \sqrt{\frac{2T}{K_{n,s}}} \) and \( \sqrt{\frac{2T}{K_{p,s}}} \), respectively. The above equations hold only if the input voltages, i.e., \( V_1 \) through \( V_4 \), fall in the triangular area shown in Figure 4.8. Alternatively, if the input voltages fall in the triangular operating region of Figure 4.10, CELL 1 cease to operate and CELL 2 takes over. In this case, the currents \( I_{31}, I_{41}, I_{32} \) and \( I_{42} \) are given by

\[
I_{31} = \frac{K_{eq}}{2} (V_3 - V_1 + \alpha + \beta)^2
\]  
(4.33)

\[
I_{41} = \frac{K_{eq}}{2} (V_4 - V_1 + \alpha + \beta)^2
\]  
(4.34)

\[
I_{32} = \frac{K_{eq}}{2} (V_3 - V_2 + \alpha + \beta)^2
\]  
(4.35)

\[
I_{42} = \frac{K_{eq}}{2} (V_4 - V_2 + \alpha + \beta)^2
\]  
(4.36)
+ \beta in the Eqs. 4.37-4.40, direct evaluation of $I_{out}$ does not yield to the correct result. Therefore, the term $\alpha + \beta$ should be eliminated before the summation can be performed. The circuit shown in Figure 4.13 shows a possible solution to this problem. This circuit accepts currents $I_{m13}$ through $I_{m14}$ and cancels the $\alpha+\beta$ term by converting each current to a voltage where $\alpha+\beta$ term can be conveniently eliminated by subtracting an appropriate voltage. Subsequently, the resulting voltages are converted back to current before $I_{out}$ is evaluated.

![Figure 4.13: Schematic of the current correction circuit for the multiplier of Figure 4.12.](image)

The principles of operation of the sub-circuit consisting of transistors N13-N15 and the associated current source IB2 will be explained here. Assuming $IB2 \gg I_{o13}$, we can write the following equations for $V_a$, $V_b$ and $V_c$:

$$V_a = \sqrt{\frac{K_{eq}}{K_{n13}}} (|V_1 - V_3| + \alpha + \beta) + V_{Tn} \quad (4.41)$$

$$V_b = \sqrt{\frac{2IB3}{K_{n25}}} + V_{Tn} \quad (4.42)$$
\[ V_c = V_b - V_{Th} - \sqrt{\frac{2IB^2}{K_{n15}}} \quad (4.43) \]

Using Eqs. 4.41-4.43, the current \( I_{o13} \) can be written as

\[ I_{o13} = \frac{K_{n14}}{2} \left[ \sqrt{\frac{K_{eq}}{K_{n13}}} | V_1 - V_3 | + \sqrt{\frac{K_{eq}}{K_{n13}}} (\alpha + \beta) - \sqrt{\frac{2IB^3}{K_{n25}}} + \sqrt{\frac{2IB^2}{K_{n15}}} \right]^2 \quad (4.44) \]

The constant term in the above equation can be set to zero, i.e.

\[ \sqrt{\frac{K_{eq}}{K_{n13}}} \left( \sqrt{\frac{2IB_1}{K_{n,s}}} + \sqrt{\frac{2IB_1}{K_{p,s}}} \right) - \sqrt{\frac{2IB^3}{K_{n25}}} + \sqrt{\frac{2IB^2}{K_{n15}}} = 0 \quad (4.45) \]

where \( \alpha \) and \( \beta \) are substituted with \( \sqrt{\frac{2IB_1}{K_{n,s}}} \) and \( \sqrt{\frac{2IB_1}{K_{p,s}}} \), respectively. In this case the current \( I_{o13} \) simplifies to

\[ I_{o13} = \frac{K_{n14}}{2} \left( \sqrt{\frac{K_{eq}}{K_{n13}}} | V_1 - V_3 | \right)^2 \quad (4.46) \]

The currents \( I_{o23}, I_{o24} \) and \( I_{o14} \) can be expressed in the same way as

\[ I_{o23} = \frac{K_{n17}}{2} \left( \sqrt{\frac{K_{eq}}{K_{n16}}} | V_2 - V_3 | \right)^2 \quad (4.47) \]

\[ I_{o24} = \frac{K_{n20}}{2} \left( \sqrt{\frac{K_{eq}}{K_{n19}}} | V_2 - V_4 | \right)^2 \quad (4.48) \]

\[ I_{o14} = \frac{K_{n23}}{2} \left( \sqrt{\frac{K_{eq}}{K_{n22}}} | V_1 - V_4 | \right)^2 \quad (4.49) \]

Assuming \( K_{n13} = K_{n16} = K_{n19} = K_{n22} = K_{na} \) and \( K_{n14} = K_{n17} = K_{n20} = K_{n23} = K_{nb} \), the current \( I_{out} \) defined as \( I_{m14} + I_{m23} - I_{m24} - I_{m13} \) can be evaluated as

\[ I_{o14} = \frac{K_{nb}K_{eq}}{K_{na}} (V_1 - V_2)(V_3 - V_4) \quad (4.50) \]

Figure 4.14 shows the 3D view of region of operation of each cell along with the region of operation of the whole circuit. As can be seen, this method nearly doubles
Figure 4.14: Simulated DC Transfer Characteristics of CELL 1, CELL 2 and the Final Circuit Comprised of Cell 1 and Cell 2 shown at the bottom.

Figure 4.15 shows the simulated transfer characteristics of the proposed multiplier. Figure 4.16 shows the output when two sinusoidal signals with frequencies of 1KHz and 100Hz are applied to the inputs. Figure 4.17 shows the small signal frequency response of the multiplier.
Figure 4.15: Simulated DC transfer characteristics of the combined multiplier.

Figure 4.16: Simulated DC transfer characteristics of the combined multiplier.
Figure 4.17: Simulated DC transfer characteristics of the combined multiplier.
CHAPTER 5

Low-voltage CMOS variable gain amplifiers

5.1 Introduction

This chapter describes the design and operation of a low-voltage CMOS Variable Gain Amplifiers (VGA) with numerous applications in communication systems and audio/video analog signal processing circuits. The voltage gain, or the transconductance of the VGA can be varied by a control voltage or current. In most designs the variable transconductance is achieved by controlling the bias current of a differential pair. However, this approach is not well suited for applications where wide gain variation is required, mainly due to square root dependency of the differential pair transconductance on the bias current. For instance, in order to achieve a 30dB gain variation, the differential pair bias current should be varied in the range of 1 to 1000. Some designs attempt to avoid large bias current variation by using two or more differential pairs in cascade; resulting in smaller gain variation range per stage. A more serious drawback of the differential pair lies on its rather limited input voltage range. Unfortunately, cascading differential pairs have adverse effect as the subsequent differential pairs experience an increasing signal amplitude. It can be shown that the maximum input differential voltage that can be applied to an NMOS or PMOS differential pair without severe distortion is limited to a few tenths of a volt
and is given by [26]

\[ v_{id,\text{max}} = \sqrt{\frac{2I_B}{K_{n,p}}} \]  

(5.1)

where \( I_B \) is the differential pair bias current. Alternatively, an analog multiplier can be used as a VGA with significantly larger input voltage range. In general, the output current of a four quadrant analog multiplier can be expressed as

\[ I_o = \alpha(V_1 - V_2)(V_3 - V_4) \]  

(5.2)

where \( \alpha \) is the transconductance constant of the multiplier. If required, a resistor or a transresistor element can be used at the output to convert the output current signal into a voltage signal.

A VGA with an exponential gain control characteristic is desired in applications where wide range gain control is required; that is, the gain should increase monotonically on a decibel scale with linear increments in gain control signal. To fulfill this need, a new pseudo-exponential voltage generator is designed to map the input gain control signal into a corresponding exponential voltage.

Figure 5.1 shows how an analog multiplier can be used as a variable gain amplifier. The input signal is differentially applied to one pair of input terminals, labeled \( V_1 \) and \( V_2 \), and the gain control signal is applied to the second pair of terminals labeled \( V_3 \) and \( V_4 \). The output current of the multiplier which is proportional to the product of the two input differential voltages, i.e. \( v_{12} = V_1 - V_2 \) and \( v_{34} = V_3 - V_4 \) can subsequently be converted into a voltage using a simple resistive load or a gain stage with proper transresistance.

A VGA is designed using the square-law based analog multiplier. This VGA, referred to as VGA1 in this chapter, has an input and output voltage range of 1Vpp.
and a gain range of 0.26dB to 28.4 dB. The input voltage range is primarily limited by a rather high equivalent threshold voltage of the composite transistor used in the analog multiplier circuit. To further extend the input voltage range, a new low-voltage composite transistor is introduced and used in the design of the second VGA, referred to as VGA2 in this chapter. The modified design, i.e., VGA2, can achieve an input voltage range of $2V_{pp}$. Moreover, the second design requires smaller transistors and its power consumption is a tenth of VGA1.

This chapter is organized as follows; the new pseudo-exponential voltage generator is introduced in section 5.2. Section 5.3 presents the complete design and simulation results of the VGA1. The new low-voltage composite transistor is introduced in section 5.4. The complete design, simulation and experimental results of the of the VGA2 designed using low-voltage composite transistors is presented in section 5.5. Finally, section 5.6 presents a brief noise analysis of VGA1 and VGA2.
5.2 Exponential current-to-voltage converter

In this section the design of a new current-to-voltage converter with exponential characteristics is explained. This converter as shown in the block diagram of Figure 5.1 is responsible for generating an exponential voltage to control the gain of the VGA. Here, the input control signal is assumed to be a current. However, as we will see shortly, due to the constant input resistance of the converter a voltage gain control signal can be used as well.

There is no intrinsic logarithmic device in CMOS technology. One possibility is to generate the required exponential characteristic using parasitic bipolar devices [37, 38]. Alternatively, a new pseudo-exponential voltage generator is introduced in this section. This very compact and power efficient sub-circuit offers a superb exponential characteristic.

Let us examine the circuit shown in Figure 5.2 which is a back-to-back connection of two current mirrors. The gain control signal $I_C$ is a bidirectional current with positive direction chosen to be outward.

Assuming the current mirrors have a one-to-one ratio, i.e. $K_{n1} = K_{n2} = K_n$ and $K_{p1} = K_{p2} = K_p$, currents $I_1$ and $I_2$ can be written as

$$ I_1 = \frac{K_{p1}}{2} (V_{DD} - V_c - |V_{TP}|)^2 $$

(5.3)

and

$$ I_2 = \frac{K_{n1}}{2} (V_c - V_{TN})^2 $$

(5.4)

using the fact that $I_2 = I_1 - I_C$ and further assuming $K_n = K_p = K$ we obtain

$$ V_c = \frac{V_{DD} - |V_{TP}| + V_{TN}}{2} - \frac{I_C}{K (V_{DD} - |V_{TP}| - V_{TN})} $$

(5.5)
substituting Eq. 5.5 into Eq. 5.4 and Eq. 5.3 yields

\[ I_1 = \frac{K}{2} \left( \frac{V_{DD} - |V_{tp}| - V_{tn}}{2} + \frac{I_C}{K (V_{DD} - |V_{tp}| - V_{tn})} \right)^2 \quad (5.6) \]

and

\[ I_2 = \frac{K}{2} \left( \frac{V_{DD} - |V_{tp}| - V_{tn}}{2} - \frac{I_C}{K (V_{DD} - |V_{tp}| - V_{tn})} \right)^2 \quad (5.7) \]

The ratio of the two currents \( I_1 \) and \( I_2 \) can be written as

\[ \frac{I_1}{I_2} = \frac{\left(1 + \frac{I_C}{2K\gamma^2}\right)^2}{\left(1 - \frac{I_C}{2K\gamma^2}\right)^2} \quad (5.8) \]

where \( \gamma \) is defined as

\[ \gamma = \frac{V_{DD} - |V_{tp}| - V_{tn}}{2} \quad (5.9) \]

By further defining \( y = \frac{I_C}{2K\gamma^2} \), Eq. 5.8 assumes the form

\[ f(y) = \frac{I_1}{I_2} = \left(\frac{1 + y}{1 - y}\right)^2 \quad (5.10) \]
The function $f(y)$ is a close approximation of the exponential function $\text{Exp}(4y)$. Figure 5.3 compares these two functions on a semi-logarithmic coordinates and defines the range where the approximation holds within less than 2% and 5% error. Figure 5.4(a) shows the simulated currents $I_1$ and $I_2$ of this circuit as a function of the control current $I_C$. As stated previously, the current $I_C$ can assume both positive and negative values. Figure 5.4(b) depicts the ratio $\frac{I_1}{I_2}$ as $I_C$ is varied from -30µA to 30µA. The accuracy of the approximation can be perceived better by plotting the graph on a semi-logarithmic axis as shown Figure 5.4(c).

The two back-to-back connected current mirrors of Figure 5.2 have another interesting characteristic as revealed by Eq. 5.5, i.e. it offers a constant linear resistance at the input terminal. The resistance can be simply found by examining the Eq. 5.5.
Figure 5.4: (a) Simulated currents $I_1$ and $I_2$ of the circuit of Figure 5.2 (b) The ratio $\frac{I_1}{I_2}$ (c) The ratio $\frac{I_1}{I_2}$ expressed in dB.

and can be expressed as

$$R_{in} = \frac{1}{K(V_{DD} - |V_{T_p}| - V_{T_n})} \quad (5.11)$$

The negative sign in Eq. 5.5 appears simply because the positive direction of the $I_c$ is chosen to be outward as shown in Figure 5.2. Constant input resistance implies that the circuit is responsive to a gain control voltage $V_C$ as well as a gain control current. This property is useful if the gain control signal is in voltage form. Figure 5.5 shows the simulated input voltage-current characteristics of this circuit where the slope of the line represents the input conductance. This figure also shows that $V_C$ should vary
from almost 1.2V to 1.9V in order to obtain the same effect as sweeping $I_C$ from -30μA to 30μA. The measured voltage-current characteristics are shown in Figure 5.6.

![Graph](image)

Figure 5.5: Simulated input voltage-current characteristic of two diode connected MOS transistors.

Figure 5.7 shows the complete circuit diagram of the pseudo-exponential voltage generator. The current mirror P3-P4 is used to direct the current $I_2$ to the drain of P5 and N4. Here, the constant resistance of the two diode connected MOS transistors is used again to convert the current $I_2$ to a corresponding voltage. The gate voltage of N3, namely $V_G$ (Eq. 5.5), can be expressed as

$$V_G = \frac{V_{DD} - |V_{TP}| + V_{TN}}{2} + \frac{I_2}{K(V_{DD} - |V_{TP}| - V_{TN})} \quad (5.12)$$

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Figure 5.6: Measured input voltage-current characteristic of two diode connected MOS transistors.

Figure 5.7: The complete circuit diagram of the pseudo-exponential voltage generator.
Transistor N3 operates in triode region and acts as a voltage controlled resistor. For small drain-source voltages, the resistance exhibited by N3 can be approximated by

\[
R_{DS} = \frac{1}{K_{n3} (V_G - V_{Th})}
\]  

(5.13)

The current \(I_1\) flows through N3 and generates a drain-source voltage of \(V_{DS} = R_{DS}I_1\), which is proportional to \(\frac{I_1}{I_2}\). Figure 5.8 shows the simulated drain-source voltage of N3 in both linear and logarithmic scale versus \(I_C\).

The following section describes the integration of the exponential voltage generator discussed in this section with the simple square-law based analog multiplier discussed in Chapter 4.
5.3 The programmable gain amplifier: VGA1

This section presents the first design of a variable gain amplifier referred to as VGA1. This design is based on the analog multiplier described in Chapter 4 in conjunction with the pseudo-exponential voltage generator discussed in Section 5.2.

Figure 5.9: The complete circuit diagram of the VGA1 including the exponential voltage generator (N7-N10, P14-P18) and the output stage (P8-P13, N5, N6).

Figure 5.9 shows the complete circuit diagram of the VGA1 including the gain stage. The transistor sizes, current source and resistor values are given in Table 5.1 and Table 5.2, respectively.

The exponential voltage generator consists of transistors N7-N10 and P14-P18 and its output is connected to the gate of transistors P1-P2. The input signal is differentially applied to the gates of N1-N4. In order to reduce the required supply voltage, a folded architecture is used. The common-gate transistors P10-P11 decreases the voltage swing at the drain of N1-N4 and P6, P7 which otherwise could force these transistors out of the saturation region. Resistors $R_1$ and $R_2$ are used to convert the current signals to a voltage signal at the gates of differential stage P12-P13.
<table>
<thead>
<tr>
<th>Transistor</th>
<th>Size</th>
<th>Transistor</th>
<th>Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>N1-N4</td>
<td>500/2</td>
<td>P1-P4</td>
<td>1500/2</td>
</tr>
<tr>
<td>N5, N6</td>
<td>200/2</td>
<td>P5-P7</td>
<td>6000/4</td>
</tr>
<tr>
<td>N7, N8</td>
<td>12/8</td>
<td>P8, P9</td>
<td>900/4</td>
</tr>
<tr>
<td>N9</td>
<td>12/4</td>
<td>P10, P11</td>
<td>2500/2</td>
</tr>
<tr>
<td>N10</td>
<td>5/4</td>
<td>P12, P13</td>
<td>240/2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>P14, P15</td>
<td>36/8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>P16, P17</td>
<td>160/4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>P18</td>
<td>15/4</td>
</tr>
</tbody>
</table>

Table 5.1: Transistor sizes of the VGA1.

<table>
<thead>
<tr>
<th>$I_{B1}$</th>
<th>$3mA$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{B2}$</td>
<td>$600\mu A$</td>
</tr>
<tr>
<td>$R_{1,2}$</td>
<td>$2K\Omega$</td>
</tr>
<tr>
<td>$R_L$</td>
<td>$48K\Omega$</td>
</tr>
</tbody>
</table>

Table 5.2: Current source and resistor values of the VGA1.
The differential pair is biased by a constant current source. The differential voltage present at the gates of P12 and P13 is relatively small. Therefore, the differential pair does not cause any noticeable distortion. In addition to introducing the required gain, the differential pair effectively generates a current at the output of the current mirror N5,N6 which is proportional to the multiplication of the input signal and the generated exponential gain control voltage. Finally, the output current of the VGA1 is converted to voltage using the load resistance $R_L$.

A precise load resistance is required in order to adjust the absolute gain of the VGA1 as pertinent to the application at hand. Here the value of the $R_L$ is set in such a way as to obtain a gain range of nearly 1dB to 28dB with a maximum input and output voltage swing of $1V_{PP}$. Figure 5.10 shows the gain of VGA1 as $I_C$ is swept from -30$\mu$A to 30$\mu$A and the differential input voltage is kept constant at 40mV. This figure shows a minimum and a maximum gain of 0.26 and 28.4, respectively.

In most applications, the VGA is embedded in an automatic gain control loop where the output voltage is monitored and kept at its maximum value [39]. Hence, a plot showing the gain of the VGA when the output is kept at a maximum value is a preferred way to assess the linearity of the gain characteristic. To this end, Figure 5.11 depicts the gain of VGA1 as a function of $I_C$ when the output is kept constant at $1V_{PP}$ by adjusting the input voltage. The similarity between the plots in Figures 5.11 and 5.14 indicates a relatively small distortion of VGA1.

Figure 5.12 depicts the Total Harmonic Distortion (THD) versus $I_C$ of VGA1 at 1KHz at the maximum output value. The maximum distortion of 2.4% occurs at the maximum input voltage which reinstates the limited input voltage range of the composite transistor, especially in low-voltage applications.
Figure 5.10: The VGA1 gain as a function of control current $I_C$ when input is kept constant at 40$mV_{pp}$.

Figure 5.11: The VGA1 gain as a function of control current $I_C$ when the output is kept constant at 1$V_{pp}$. 
Figure 5.12: Total harmonic distortion (THD) of the VGA1 as function of the gain control current at 1KHz and $V_{out} = 1V_{pp}$.

It is desirable that the output DC voltage shows minimal sensitivity to the gain control signal. Otherwise, a single ended architecture may not be suitable for most applications. Figure 5.13 depicts the simulated output voltage when the input is shorted and $I_C$ is varied from -30\,$\mu$A to 30\,$\mu$A. This figure shows only a small sensitivity of the DC output voltage to gain variations.

Figure 5.14 shows the VGA1 output signal when a 40m$V_{pp}$ sinusoidal signal at 1KHz is applied at the input and the gain is set to its maximum value.

The frequency response of the VGA1 for three different values of $I_C$ is illustrated in Figure 5.15 which shows a minimum -1dB frequency of 10MHz. The simulation results of the VGA1 is summarized in Table 5.3.
Figure 5.13: The variation of the VGA1 output DC voltage when $V_{\text{in}}=0$ and $I_C$ is changed from $-30\mu A$ to $30\mu A$.

Figure 5.14: The VGA1 output when $40\text{mV}_{\text{pp}}$ sinusoidal signal is applied at the input and gain is set to its maximum.
Figure 5.15: The VGA1 small signal frequency response for $I_C=30\mu A$, $0\mu A$ and $-30\mu A$.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>value</th>
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<tbody>
<tr>
<td>Supply voltage</td>
<td>3V</td>
</tr>
<tr>
<td>Minimum gain</td>
<td>0.26dB</td>
</tr>
<tr>
<td>Maximum gain</td>
<td>28.4dB</td>
</tr>
<tr>
<td>Linearity</td>
<td>Excellent</td>
</tr>
<tr>
<td>-1dB frequency at 28.4dB</td>
<td>10MHz</td>
</tr>
<tr>
<td>-1dB frequency at 0.26dB</td>
<td>14MHz</td>
</tr>
<tr>
<td>Input voltage swing</td>
<td>$1V_{PP}$</td>
</tr>
<tr>
<td>Output voltage swing</td>
<td>$1V_{PP}$</td>
</tr>
<tr>
<td>Input referred noise @ 0.26dB</td>
<td>$650 \frac{mV}{\sqrt{Hz}}$</td>
</tr>
<tr>
<td>Input referred noise @ 1.4dB</td>
<td>$560 \frac{mV}{\sqrt{Hz}}$</td>
</tr>
<tr>
<td>Input referred noise @ 28.4dB</td>
<td>$25 \frac{mV}{\sqrt{Hz}}$</td>
</tr>
<tr>
<td>Supply current at 28.4dB</td>
<td>8.5mA</td>
</tr>
<tr>
<td>Supply current at 0.26dB</td>
<td>9.7mA</td>
</tr>
</tbody>
</table>

Table 5.3: Simulated results of the VGA1.
5.4 Low-voltage CMOS composite transistor

The high threshold voltage of the simple CMOS composite transistor can limit its application in low-voltage analog circuit design. This section introduces a new low-voltage composite transistor with improved input voltage range. While capable of operating at lower supply voltages, the new device shares the most important feature of the simple composite transistor, i.e. offering two high impedance terminals to control the current through the device.

A folded structure is used here again to decrease the required voltage of the composite transistor. This concept is depicted in Figure 5.16. A simple level shifter is added between the sources of the two transistors. The voltage gain of the level shifter is ideally assumed to be 1. If the level shifter shifts the voltage by \( \Delta V \),

![Figure 5.16: Modified composite transistor. A simple level shifter is added between the sources of PMOS and NMOS transistors.](image)

then the new composite device operates when \( V_g - V_s \geq V_{Teq} - \Delta V \) and thereby extends the operating region of the composite transistor by the same amount. The NMOS and PMOS transistors in the original composite transistors share the same current. To reconstruct the same condition, a current mirror is added to redirect the
drain current of the NMOS transistor to the source of the PMOS transistor. This arrangement is shown in Figure 5.17 and guarantees equal currents flowing through the NMOS and PMOS transistors, imitating the original composite transistor. The circuit implementation of the modified composite transistor, suitable for low-voltage applications, is shown in Figure 5.18. A simple common source stage with a current source as a load is used to shift the voltage at the source of P1 by almost $V_{Tn}$ and feed it to the source of N1. A more rigorous analysis of the circuit is given below.

### 5.4.1 Analysis of the low-voltage composite transistor

The currents $I_1$ through $I_3$ shown in Figure 5.18 can be written as

$$I_1 = \frac{K_{n1}}{2} (V_g - V_x - V_{Tn})^2 \quad (5.14)$$

$$I_2 = \frac{K_{n2}}{2} (V_g - V_x - V_{Tn})^2 \quad (5.15)$$
Figure 5.18: Modified composite transistor with lower equivalent threshold voltage.

\[ I_3 = \frac{K_{pl}}{2} (V_y - V_x - |V_{T_P}|)^2 \]  

Eq. 5.14 through 5.16 can be rewritten in the form of

\[ V_g - V_x = \sqrt{\frac{2I_1}{K_{n1}}} + V_{T_n} \]  
\[ V_y - V_x = \sqrt{\frac{2I_2}{K_{n2}}} + V_{T_n} \]  
\[ V_y - V_s = \sqrt{\frac{2I_1}{K_{pl}}} + |V_{T_P}| \]

Using the fact that \( V_{gs} = V_{gx} + V_{xy} + V_{ys} \) and \( I_B = I_1 + I_2 \) we can write

\[ V_{gs} - |V_{T_P}| = \sqrt{\frac{2I_1}{K_{eq}}} - \sqrt{\frac{2(I_B - I_1)}{K_{n2}}} \]

where \( K_{eq} \) has the same definition as given in Eq. 3.9. In the case where \( I_B \gg I_1 \) the above equation can be simplified and written in the conventional form of

\[ I_1 = \frac{K_{eq}}{2} (V_{gs} - V_{Teq})^2 \]
with the equivalent threshold voltage $V_{Teq}$ defined as $|V_{Tp}| - \sqrt{\frac{2I}{Kn^2}}$.

The conditions for operation in saturation region are $V_g \geq V_{Th} + V_{DS, sat, I_B}$ and $V_s \leq V_{DD} - |V_{Tp}| - V_{DS, sat, P3}$. Where $V_{DS, sat}$ denote the drain-source saturation voltage of the current sources. Figure 5.19 shows the simulated drain current of the new low-voltage composite transistor as a function of gate and source voltages. While Figure 5.20 shows the measured results.

![Figure 5.19: Simulated drain current of the low-voltage composite transistor as a function of the gate-source voltage.](image)

Figure 5.19: Simulated drain current of the low-voltage composite transistor as a function of the gate-source voltage.

Figure 5.21 shows the frequency characteristic of the drain current for four different values of gate-to-source voltage. The measured drain current of the low-voltage composite transistor along with simulated drain current and numerical evaluations of Eq. 5.20 and Eq. 5.21 are shown in Figure 5.22. This figure further justifies the assumption made in driving Eq. 5.21.
Figure 5.20: Measured drain current of the low-voltage composite transistor as a function of the gate-source voltage.

Figure 5.21: \( I_d \) [dB\( \mu \)A] of the low-voltage composite transistor as a function of frequency.
The new low-voltage composite transistor introduced in the previous section can be used instead of the simple composite transistor to extend the common mode input voltage range. Figure 5.23 shows such an implementation where each composite transistor is replaced with the low-voltage composite transistor of Figure 5.22.

Figure 5.25 shows the input voltage range of this multiplier with remarkable improvement over the conventional implementation using simple composite transistors.

For a symmetric operation, i.e. $v_{12,max} = v_{34,max}$, the common mode voltage of $V_1$, $V_2$ and $V_3$, $V_4$ should be set to 2.5V and 0.5V, respectively, as shown in Figure 5.26. This correspond to a maximum differential input of $1V_{PP}$ for both $v_{12}$ and $v_{34}$. Figure 5.27 depicts the DC transfer characteristics for this symmetric operation.
Figure 5.23: CMOS implementation of the square-law based multiplier using low-voltage composite transistor.

Figure 5.24: Micro-photograph of the implemented circuit of Figure 5.23 including the pseudo-exponential voltage generator of Figure 5.7.

Figure 5.25: Region of operation of the CMOS multiplier shown in Figure 5.23.
Figure 5.26: \( V_{12,\text{com}} \) and \( V_{34,\text{com}} \) for symmetric operation where \( v_{12,\text{max}} = v_{34,\text{max}} \).

Figure 5.27: DC transfer characteristics of multiplier using new low-voltage composite transistors.
Although symmetric operation might be required for analog multipliers, it is usually possible to relax this requirement in the design of variable gain amplifiers. Rewriting equation Eq. 4.16 yields

\[ I_o = K_{eq} v_{12} v_{34} \]  

(5.22)

where \( v_{12} \) and \( v_{34} \) are differential input voltages. The gain control voltage \( v_{34} \) is usually varied in such a way as to maintain the maximum output current as the input voltage \( v_{12} \) changes. Therefore, we can write

\[ I_{o,\text{max}} = K_{eq} v_{12,\text{max}} v_{34,\text{min}} \]  

(5.23)

and

\[ I_{o,\text{max}} = K_{eq} v_{12,\text{min}} v_{34,\text{max}} \]  

(5.24)

combining Eq. 5.23 and Eq. 5.23 yields

\[ v_{12} = \frac{v_{12,\text{min}} v_{34,\text{max}}}{v_{34}} \]  

(5.25)

This shows that as the input voltage decreases, \( v_{34} \) increases. This situation can also be interpreted in reverse; a large control voltage requires a small input voltage. This observation leads to the tapered region of operation shown in Figure 5.28. Comparison of Figure 5.26 with Figure 5.28 reveals that this characteristic of the VGA allows more efficient utilization of the operating region and can enhance the maximum input differential voltage range. This characteristic of the VGA is further depicted in the DC transfer characteristic of Figure 5.29, where an input differential voltage as high as \( 2V_{pp} \) is attainable. In this figure, the region of operation is limited to the shaded area. Therefore, the nonlinearities at the extreme ends of the transfer characteristic curves are avoided.
Figure 5.28: Region of operation of a VGA2 with exponential gain control

Figure 5.29: DC transfer characteristics of the VGA2. Shaded area shows the region of operation for 0 to 30dB gain variation.
Figure 5.30 shows the overall transconductance of the VGA2 as a function of gain control current $I_C$. The transconductance of the VGA can vary as much as 30dB as $I_C$ varies between -30μA and 30μA. The measured transconductance of the VGA2 is shown in Figure 5.31.

![Figure 5.30: The VGA2 transconductance as a function of control current.](image)

The output stage of the VGA2 raises certain challenges which are different than those encountered in the design of the Op Amp's output stage. Generally speaking, any gain above the minimum required exhibited by an Op Amp output stage can be considered acceptable. This is because the overall gain is usually set by the feedback loop. The situation for the VGA output stage is totally different. The VGA output stage should possess high and precise transresistance without compromising the frequency response. A very high impedance node at the output stage can severely limit the frequency response of the VGA. Moreover, high levels of impedance cause a DC
Figure 5.31: Measured VGA2 transconductance as a function of control current.

voltage at the output that shows a strong dependency on the gain control current and the input common mode voltage. At the same time, the output stage should handle large voltage swings with low signal distortion.

Figure 5.32 shows the proposed output stage. Current mirror N9-N10 generates the current $I_o = I_2 + I_3 - I_1 - I_4$. The first stage of the amplification includes the cascode stage N11-N12 and the current source $I_{BO}$. The feedback resistor $R_f$ sets the gain of this stage. The second gain stage includes transistors P19-P21 and N13-N15. The common gate transistors N13 and P19 are used to improve the frequency response and also extend the output voltage swing. The load resistor $R_L$ is required to set the gain of the second stage.

The transistor sizes, current source and resistor values of VGA2 are given in Table 5.4 and Table 5.5.
Figure 5.32: The VGA2 output stage.

<table>
<thead>
<tr>
<th>Transistor</th>
<th>Size</th>
<th>Transistor</th>
<th>Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>N1, N4, N5, N8</td>
<td>5/2</td>
<td>P1-P3</td>
<td>120/4</td>
</tr>
<tr>
<td>N2, N3, N6, N7</td>
<td>100/2</td>
<td>P4, P5</td>
<td>15/2</td>
</tr>
<tr>
<td>N7-N8</td>
<td>12/8</td>
<td>P6-P11</td>
<td>120/4</td>
</tr>
<tr>
<td>N9, N10</td>
<td>20/2</td>
<td>P12, P13</td>
<td>15/2</td>
</tr>
<tr>
<td>N11</td>
<td>10/2</td>
<td>P14-P16</td>
<td>120/4</td>
</tr>
<tr>
<td>N12</td>
<td>20/2</td>
<td>P17, P18</td>
<td>60/2</td>
</tr>
<tr>
<td>N13</td>
<td>40/2</td>
<td>P19</td>
<td>108/2</td>
</tr>
<tr>
<td>N14</td>
<td>6/2</td>
<td>P20</td>
<td>24/2</td>
</tr>
<tr>
<td>N15</td>
<td>18/2</td>
<td>P21</td>
<td>72/2</td>
</tr>
</tbody>
</table>

Table 5.4: Transistor sizes of the VGA2.
<table>
<thead>
<tr>
<th>$I_B$</th>
<th>120(\mu)A</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{BO}$</td>
<td>29(\mu)A</td>
</tr>
<tr>
<td>$R_f$</td>
<td>500K(\Omega)</td>
</tr>
<tr>
<td>$R_L$</td>
<td>40K(\Omega)</td>
</tr>
</tbody>
</table>

Table 5.5: Current source and resistor values of the VGA2.

Figure 5.33 depicts the output voltage of the VGA2 at maximum gain (29dB) in response to a 1KHz signal with a total harmonic distortion (THD) of 0.9%. The overall VGA2 gain as a function of the control current is shown in Figure 5.34 where the input is kept constant at 80mV and control current $I_C$ is swept from -30\(\mu\)A to 30\(\mu\)A.

In order to investigate the large signal behavior, the gain of VGA2 is simulated while keeping the output voltage swing at its maximum (2V\text{pp}) and for different values of $I_C$. The result is shown in Figure 5.35. The similarity between large and small signal gains (Figure 5.34 and 5.35) illustrates the excellent linearity and minimal large signal distortion of the circuit.

Figure 5.36 shows the THD of the VGA2 at 1KHz and the maximum output voltage swing of 2V\text{pp} as the gain control current is swept from -30\(\mu\)A to 30\(\mu\)A.

Figure 5.37 shows the variation of the DC output voltage when the input terminals are shorted and the $I_C$ is swept from -30\(\mu\)A to 30\(\mu\)A. Figure 5.38 shows the small
Figure 5.33: The VGA2 output when a 80mV_{PP} sinusoidal signal at 1kHz is applied at the input and gain is set to 29dB.

Figure 5.34: The VGA2 gain as a function of control current $I_C$ when the input is kept constant at 80mV_{PP}.
Figure 5.35: The VGA2 gain as a function of control current $I_C$ when the output is kept constant at $2V_{PP}$.

Figure 5.36: The THD of the VGA2 as function of the gain control current at 1KHz and $V_{out} = 2V_{PP}$. 

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Figure 5.37: The variation of the VGA2 output DC voltage when $V_{in}=0$ and $I_C$ is changed from $-30\mu A$ to $30\mu A$.

signal frequency response of the VGA2 for three different values of $I_C$. Table 5.6 summarizes the simulated parameters of the VGA2.
<table>
<thead>
<tr>
<th>Parameter</th>
<th>value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>3V</td>
</tr>
<tr>
<td>Minimum gain</td>
<td>-0.4dB</td>
</tr>
<tr>
<td>Maximum gain</td>
<td>29.6dB</td>
</tr>
<tr>
<td>Linearity</td>
<td>Excellent</td>
</tr>
<tr>
<td>-1dB frequency at 29.6dB</td>
<td>6MHz</td>
</tr>
<tr>
<td>-1dB frequency at -0.4dB</td>
<td>6.3MHz</td>
</tr>
<tr>
<td>Input Voltage swing</td>
<td>1.9V</td>
</tr>
<tr>
<td>Output Voltage swing</td>
<td>2V</td>
</tr>
<tr>
<td>Input referred noise @ 0.26dB</td>
<td>$4.9 \frac{\mu V}{\sqrt{Hz}}$</td>
</tr>
<tr>
<td>Input referred noise @ 1.4dB</td>
<td>$4.35 \frac{\mu V}{\sqrt{Hz}}$</td>
</tr>
<tr>
<td>Input referred noise @ 29.6dB</td>
<td>$308 \frac{\mu V}{\sqrt{Hz}}$</td>
</tr>
<tr>
<td>Supply current at -0.4dB</td>
<td>960μA</td>
</tr>
<tr>
<td>Supply current at 29.6dB</td>
<td>880μA</td>
</tr>
</tbody>
</table>

Table 5.6: Simulated parameters of the VGA2.
5.6 Noise analysis

This section briefly discusses the thermal noise characteristics of both simple and low-voltage composite transistors. In general, the thermal noise in the drain-source channel of an MOS transistor can be written as [40, 41]

\[
\overline{v_n^2} = \frac{8K T g_m \Delta f}{3}
\]

(5.26)

where \( K \) is the Boltzmann constant and \( T \) is the absolute temperature. The input thermal noise voltage can be simply written as

\[
\overline{v_n^2} = \left( \frac{\overline{v_n^2}}{g_m^2} \right) = \frac{8K T \Delta f}{3g_m}
\]

(5.27)

For a simple composite transistor, the equivalent transconductance \( g_{meq} \) can be expressed in terms of NMOS and PMOS transistor transconductances as

\[
\frac{1}{g_{meq}} = \frac{1}{g_{mn}} + \frac{1}{g_{mp}}
\]

(5.28)
Hence, the input voltage noise of a simple composite transistor can be written as

\[ \overline{v^2}_{n,\text{comp}} = \frac{8KT\Delta f}{3g_{mn}} + \frac{8KT\Delta f}{3g_{mp}} = \overline{v^2}_{n,NMOS} + \overline{v^2}_{n,PMOS} \]  

(5.29)

Here $\overline{v^2}_{n,NMOS}$ and $\overline{v^2}_{n,PMOS}$ are the input noise voltages of NMOS and PMOS transistors, respectively.

The small signal currents $i_1$ through $i_4$ of a square-law based multiplier using simple composite transistor shown in Figure 5.9 are given as

\[ i_1 = g_{meq1}v_1 \]  

(5.30)

\[ i_2 = g_{meq2}v_2 \]  

(5.31)

\[ i_3 = g_{meq3}v_1 \]  

(5.32)

\[ i_4 = g_{meq3}v_2 \]  

(5.33)

where $g_{meq1}$ through $g_{meq4}$ are the equivalent transconductances of the composite transistors N1-P1 through N4-P4, respectively. Using the fact that $g_{meq1} = g_{meq2}$ and $g_{meq3} = g_{meq4}$, the small signal output current can be expressed as

\[ i_o = i_2 + i_3 - i_1 - i_4 = (g_{meq3} - g_{meq1}) (v_1 - v_2) \]  

(5.34)

The total output noise current can be written as

\[ i_{n,o} = i_{n,1}^2 + i_{n,2}^2 + i_{n,3}^2 + i_{n,4}^2 = \frac{16KT(g_{meq1} + g_{meq3})\Delta f}{3} \]  

(5.35)

Eq. 5.34 and Eq. 5.35 reveal one disadvantage of multiplier-based variable gain amplifiers, that is the output signal is proportional to difference between the transistor
transconductances while the noise is proportional to the sum of the noise contributed by each composite transistor.

The equivalent transconductance of the low-voltage composite transistor shown in Figure 5.18 can be obtained as

\[
g_{\text{eq}} = \frac{\partial I_d}{\partial V_{gs}} = \frac{1}{g_{m,N1}} + \frac{1}{g_{m,P1}}
\]

(5.36)

which is the same as the transconductance of a simple composite transistor. Neglecting the noise contribution of the p-type current mirror, the input noise voltage can be expressed as

\[
\overline{v^2}_{n} = \overline{v^2}_{n,N1} + \overline{v^2}_{n,N2} + \overline{v^2}_{n,P1} = \frac{8KT\Delta f}{3} \left( \frac{1}{g_{\text{eq}}} + \frac{1}{g_{m,N2}} \right)
\]

(5.37)

and the noise current is given by

\[
\overline{i^2}_{n} = \frac{8KTg_{\text{eq}}\Delta f}{3} \left( 1 + \frac{g_{\text{eq}}}{g_{m,N2}} \right)
\]

(5.38)

The term \( \frac{g_{\text{eq}}}{g_{m,N2}} \) in the above equation represent the noise contributed by the level shifter N2. Including the noise contribution the p-type current mirror, the noise current assumes the form

\[
\overline{i^2}_{n} = \frac{8KTg_{\text{eq}}\Delta f}{3} \left( 1 + \frac{g_{\text{eq}}}{g_{m,N2}} \right) + \frac{16KTg_{m,\text{mirror}}\Delta f}{3}
\]

(5.39)

where \( g_{m,\text{mirror}} = g_{m,P2} = g_{m,P4} \) is the transconductance of the p-type transistors of the current mirror. The level shifter transconductance, \( g_{m,N2} \), can be increased so that the term \( \frac{g_{\text{eq}}}{g_{m,N2}} \) becomes negligible. In this case Eq. 5.39 yields

\[
\overline{i^2}_{n} = \frac{8KTg_{\text{eq}}\Delta f}{3} \left( 1 + \frac{2g_{m,\text{mirror}}}{g_{\text{eq}}} \right)
\]

(5.40)

The output noise current of the VGA2 shown in Figure 5.23 can be written as

\[
\overline{i^2}_{n} = \frac{16KT\Delta f}{3} \left( g_{\text{eq}1} \left( 1 + \frac{2g_{m,\text{mirror}1}}{g_{\text{eq}1}} \right) + g_{\text{eq}2} \left( 1 + \frac{2g_{m,\text{mirror}2}}{g_{\text{eq}2}} \right) \right)
\]

(5.41)
where

\[
\frac{1}{g_{meq1}} = \frac{1}{g_{m,N1}} + \frac{1}{g_{m,P4}} = \frac{1}{g_{m,N4}} + \frac{1}{g_{m,P5}}
\]  

(5.42)

\[
\frac{1}{g_{meq3}} = \frac{1}{g_{m,N5}} + \frac{1}{g_{m,P12}} = \frac{1}{g_{m,N8}} + \frac{1}{g_{m,P13}}
\]  

(5.43)

and

\[
g_{m,mirror1} = g_{m,P1} = g_{m,P3} = g_{m,P6} = g_{m,P8}
\]  

(5.44)

\[
g_{m,mirror2} = g_{m,P9} = g_{m,P11} = g_{m,P14} = g_{m,P16}
\]  

(5.45)

and the small signal output current is given by

\[
i_o = (g_{meq3} - g_{meq1})(v_1 - v_2)
\]  

(5.46)

Comparing Eq. 5.26 with Eq. 5.40 shows that the low-voltage composite transistor has higher noise current than a simple composite transistor. This is the price paid for a larger input voltage range achievable only by the low-voltage composite transistor.
CHAPTER 6

Conclusion

In Chapter 1, the driving forces behind the trend toward lower supply voltages were identified. The clear advantages of the rail-to-rail operation of analog integrated circuits in achieving higher SNR and better utilization of limited supply voltage range were pointed out.

In Chapter 2, the operation of complementary input stage which is the only known way to obtain rail-to-rail operation at the input is explained. It was shown that the complementary input stage causes large input stage transconductance variation. The problems associated with the large transconductance variation such as non-optimal frequency compensation, low common mode rejection ratio and signal distortion were examined in detail. This chapter also reviewed the representative conventional method to design constant-$g_m$ input stages. All these schemes were based on the handling bias currents. In contrast, a new method based on processing the signal currents were introduced. The new architecture which uses the current-mode maximum selecting circuit can achieve nearly constant transconductance independent of the technology and operating region of the input stage transistors. This chapter examined one possible implementation of this idea which is based on the handling the AC signal only.
In Chapter 3, the idea first introduced in Chapter 2 was extended to processing the total instantaneous currents. The second method which is based on the minimum current selecting circuit led to a more compact and symmetrical design.

In Chapter 4, the input voltage range and the meaning of rail-to-rail operation of analog multipliers are investigated. Then the Max-circuit introduced in Chapter 2 is used in the design of four-quadrant analog multiplier with extended input voltage range.

In Chapter 5, the analog multiplier of Chapter 4 is used in the design of a low voltage Variable Gain Amplifier (VGA). A new pseudo-exponential voltage generator is introduced in this chapter and used in conjunction with the VGA to obtain a logarithmic gain control. A new low-voltage composite transistor is introduced next and used in the design of a new VGA with enhanced input voltage range.

6.1 Future work

Addition and subtraction of signals as well as amplification which is a specific case of signal multiplication were in use in analog circuit design for many years. It is hard to conceive any analog circuit which does not use any of the aforementioned operations in one way or another. The purpose of this research was to introduce two new operations, i.e. \( \min() \) and \( \max() \). We are hoping that these new operations could help the analog designer to cope with the challenges of the low voltage era and may eventually lead to a new paradigm in analog circuit design.

This research mainly dealt with the application of this idea as it pertains to an Op Amp’s input stage, and analog multipliers. However, the author strongly believes that this idea can be successfully extended to other analog building blocks such as
voltage-to-current converters as investigated elsewhere [42], Op Amp's output stages, comparators and etc.. The application of this idea to Op Amps' output stages could lead to simpler and more efficient Class-AB designs.

The analog multiplier discussed in Chapter 4 could take advantage of the low-voltage composite transistor introduced in Chapter 5, leading to an even larger input voltage range.

Finally, the min- and max-circuits, if used in signal paths, could deteriorate the noise and frequency performance of a circuit. A theoretical study should be conducted to assess its impact and practical ways should be devised to eliminate or at least lessen such undesirable effects.
APPENDIX A

DISTORTION MEASUREMENT

This appendix explains how to measure the distortion using HP-3585B spectrum analyzer. A BASIC program that can be used to control HP-3585B and download the measured data from the HP-3585B to a PC is listed. This appendix also contains a MATLAB program which can extract the harmonics peak values and calculate the Total Harmonic Distortion (THD).

A.1 Measurement setup

Figure A.1 shows the setup to measure the THD of an Op Amp in unity gain configuration using HP-3585B spectrum analyzer and HP-8165A programmable signal source.

Figure A.1: Test setup for distortion measurement of an Op Amp in unity gain configuration.
Figure A.2 shows the spectrum of the HP8165A operating at 1KHz and 400 \( mV_{pp} \) for three different common mode voltages of 0.5 [V], 1.5 [V] and 2.5 [V].

Figure A.2: Frequency spectrum of the HP-8165A programmable signal source operating at 1KHz for different common mode voltages.

Due to relatively high distortion of the signal source use of a passive low-pass filter to reduce the distortion at the source is required. Figure A.3 shows the circuit diagram of a passive sixth order low pass filter with a -3dB frequency of 500 Hz. This filter can effectively attenuate high order harmonics and hence improve signal source distortion. The spectrum of the signal at the output of the low-pass filter is shown in Figure A.4.

The measurement can be done either in linear or logarithmic scale. Up to 1001 points can be spaced evenly across the desired frequency range set on the HP-3585.
Figure A.3: Circuit diagram of a passive low-pass filter with -3dB frequency of 500Hz.

Figure A.4: Frequency spectrum of the signal at the output of low-pass filter.
spectrum analyzer. The number of points can be specified by the user and can be any number between 2 and 1001. However, on a logarithmic scale, a fixed set of 64 points will be taken, which cannot be changed without modifying the program.

'This Basic Program for taking data from HP3585B
'This program reads the frequencies and amplitudes
'and save in a file. Total Harmonic Distortion can
'also be obtained.

'==============================================
'QuickBASIC 4.0/4.5 - Declarations

'NOTE: include this file only if you are using QuickBASIC Version
'4.0 or higher, or Microsoft BASIC 6.0.
'==============================================
'$INCLUDE: 'qbdecl.bas'

'==============================================
'Main Program
'==============================================

DECLARE SUB DataRead (DV%, WRT$, f, amp)

'The device name is given as 'HP3585B' (assigned in 'ibconf').
'Here 'IBFIND' command opens the device and returns unit
'descriptor DV% If DV% is less than zero, call RFIND with
'an error message.

CLS
PRINT " "  "==================================================================" "
PRINT " "  | A QuickBASIC program to read data and calculate |"
PRINT " "  | THD from HP3585B using NI-488. |"          
PRINT " "  "=================================================================="          
PRINT DNames$ = "HP3585B"
CALL IBFIND(DNames$, DV%)
IF DV% < 0 THEN GOSUB RFIND:

\----------
'Tranfer data or not?

INPUT "Data Transfer? (Y/N) ", Ans$
IF UCASE$(Ans$) = "Y" THEN

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' ===========================
' Read Data from HP3585B
' ===========================

' ---
' Input a file name to store the desired data.
' If no name is given, the data will be display on the screen.

INPUT "Enter Filename or RETURN to show on the screen. ", FILENAME$
' IF FILENAME$ = "" THEN FILENAME$ = "CONS:
IF FILENAME$ <> "" THEN OPEN FILENAME$ FOR OUTPUT AS #1

' ---
' Input peak number for peak search if desired

INPUT "Search Peaks for accuracy? (Y/N) ", Ans$
IF UCASES(Ans$) = "Y" THEN
  INPUT "How many peaks? ", pn%
  PRINT "Searching peaks..."
  DIM peak(0 TO pn%, 1 TO 2)
  WRT$ = "SP,D2,T5"
  CALL DataRead(DV%, WRT$, peak(1, 1), peak(1, 2))
  FOR I% = 2 TO pn%
    WRT$ = "NP,D2,T5"
    CALL DataRead(DV%, WRT$, peak(I%, 1), peak(I%, 2))
  NEXT I%

' ---
' Sort the peaks by frequencies

FOR I% = pn% - 1 TO 1 STEP -1
  FOR J% = 1 TO I%
    IF peak(J%, 1) < peak(J% + 1, 1) THEN
      SWAP peak(J%, 1), peak(J% + 1, 1)
      SWAP peak(J%, 2), peak(J% + 1, 2)
    END IF
  NEXT J%
NEXT I%
END IF

' ---
' Input the output format

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PRINT "Data output format: (1) Log Mode (2) Linear Mode"
INPUT "Enter the selection: ", choice%
IF choice% = 1 THEN
   FOR I% = 0 TO 3
      J1% = 10 ^ I%
      Sp% = 2 ^ (-I%) * J1%
      J2% = 10 * J1% - Sp%
      FOR K% = J1% TO J2% STEP Sp%
         IF K% <= 1001 THEN
            WRT$ = "MK" + STR$(K% + 1) + "D2,T5"
            CALL DataRead(DV%, WRT$, f, amp)
            PRINT f%
         END IF
      NEXT K%
   NEXT I%
ELSE
   INPUT "How many points? (2-1001) ", J%
   J% = 1000 / (J% - 1)
   FOR I% = 1 TO 1001 STEP J%
      WRT$ = "MK" + STR$(I%) + "D2,T4"
         WRT$ = "IR"
      CALL DataRead(DV%, WRT$, f, amp)
      'PRINT f, WRT$
   NEXT I%
END IF
' Add peak frequency and amplitude
WHILE (pn% > 0) AND (peak(pn%, 1) < f)
    IF FILENAME$ = "" THEN
        PRINT peak(pn%, 1), peak(pn%, 2)
    ELSE
        PRINT #1, peak(pn%, 1), peak(pn%, 2)
    END IF
    pn% = pn% - 1
WEND
'
IF FILENAME$ = "" THEN
    PRINT f, amp
ELSE
    PRINT #1, f, amp
END IF
NEXT I%
CLOSE #1
PRINT
PRINT "Done!!"
PRINT
END IF
'
' Calculate THD or not?

INPUT "THD Calculation? (Y/N) ", Ans$
IF UCASE$(Ans$) = "Y" THEN

' Calculate Total Harmonic Distortion

PRINT
PRINT "Please wait ..."
PRINT
'
' Read the start and stop frequency

WRT$ = "MK1,D2,T5"
CALL DataRead(DV%, WRT$, f, amp)
StartF = f
WRT$ = "MK1001,D2,T5"
CALL DataRead(DV%, WRT$, f, amp)
StopF = f

' Ask users to put the marker on the fundamental frequency

WRT$ = "SP"
CALL IBWRT(DV%, WRT$)
PRINT "Put the marker on the peak of the fundamental frequency."

' Return to local and allow manual control
CALL IBLOC(DV%)

' Wait till ready
INPUT "Press any key when ready. ", READY$
PRINT
INPUT "Enter Filename or RETURN to show on the screen. ", FILENAMES
IF FILENAMES = "" THEN FILENAMES = "CONS:"
OPEN FILENAMES FOR OUTPUT AS #2

WRT$ = "MC,MS,RL,DV,D2,T5"
CALL DataRead(DV%, WRT$, f, amp)
f1 = f
amp1 = amp
PRINT
PRINT #2, "Fundamental frequency: "; f1; " Hz"
PRINT #2, "Fundamental Component: "; amp1; " dBV"

' Calculate highest component Maxharm
' If Maxharm is larger than 10, set to be 10

Maxharm = INT(StopF / f1)
IF Maxharm > 10 THEN Maxharm = 10

' Get the harmonic components

THD = 0
FOR I% = 2 TO Maxharm
    WRT$ = "CF,UP,D2,T5"
    CALL DataRead(DV%, WRT$, f, amp)
    PRINT #2, "Harmonic "; I%; "; amp = amp1; "dB"
    THD = THD + (10 ^ (amp / 20)) * 2
NEXT I%
THD = SQR(THD) / (10 ^ (amp1 / 20)) * 100
PRINT #2,
PRINT #2, "Total Harmonic Distortion= "; THD; " %"

, ------------
' Return to the original setup
WRT$ = "FA" + STR$(StartF) + "HZ,FB" + STR$(StopF) + "HZ"
CALL IBWRT(DV%, WRT$)
END IF
CLOSE #2

, ------------
' Return to local
CALL IBLOC(DV%)
END

, ===============
' Error Messages
, ===============
RFIND:
    PRINT "IBFIND ERROR!": STOP
RGPIB:
    PRINT "GPIB ERROR!": STOP

,' ===============
' Subroutine DataRead
,' ===============
SUB DataRead (DV%, WRT$, f, amp) STATIC
    CALL IBWRT(DV%, WRT$)
    IF IBSTA% < 0 THEN PRINT "GPIB ERROR!": STOP
    RD$ = SPACE$(30)
    CALL IBRD(DV%, RD$)
    f = VAL(LEFT$(RD$, 12))
    amp = VAL(MID$(RD$, 14, 8)) * 10 ^ (VAL(MID$(RD$, 23, 2)))
END SUB
The MATLAB program listed below can read the data file generated by data
transfer program. This program first finds the magnitude of harmonic components
for the frequency range of 0Hz to 10KHz. For an input signal of 1Khz the main or
first harmonics is at 1Khz and we have total of nine higher order harmonics. The
magnitude of harmonics with a frequency higher than 10KHz are very small and the
error caused by limiting the evaluation of THD to first ten harmonics is negligible.

THD is calculated using

\[ \text{THD}\% = \frac{\sqrt{\sum_{i=2}^{10} v_i^2}}{v_1} \times 100 \]  

where \( v_1 \) is the rms value of the main harmonic at 1KHz and \( v_2 \) through \( v_{10} \) are the
rms value of higher harmonics.

% MATLAB program to plot the spectrum and calculate
% the Total Harmonic Distortion.

load filename.dat
N=1001;  %number of data points
f=temp(:,1);
vo=temp(:,2);
%------------------------------------------
% Find the value (max1) and the frequency (fmax1)
% of the main harmonic.
%------------------------------------------
f1=300;
f2=1500;
for I=1:N,
    if f(I) < f2
        I2=I;
    end
end
for I=N:-1:1,
    if f(I) > f1
        I1=I;
    end
end
max1=-200;
max2=-200;
fmax1=0;
fmax2=0;

for I=I1:I2,
    if vo(I) > max1
        max1= vo(I);
        fmax1=f(I);
    end
end

% Find the value (max2) and the frequency (fmax2)
% of the 2nd harmonic.

f1=1800;
f2=2400;
for I=1:N,
    if f(I) < f2
        I2=I;
    end
end
for I=N:-1:1,
    if f(I) > f1
        I1=I;
    end
end

max2=-200;
fmax2=0;
for I=I1:I2,
    if vo(I) > max2
        max2= vo(I);
        fmax2=f(I);
    end
end

% Find the value (max3) and the frequency (fmax3)
% of the 3rd harmonic.

f1=2600;
f2=3200;
for I=1:N,
    if f(I) < f2
        I2=I;
    end
end
for I=N:-1:1,
    if f(I) > f1
        I1=I;
    end
end
max3=-200;
fmax3=0;
for I=I1:I2,
    if vo(I) > max3
        max3= vo(I);
        fmax3=f(I);
    end
end
%-------------------------------------------
% Find the value (max4) and the frequency (fmax4)
% of the 4th harmonic.
%-------------------------------------------
f1=3800;
f2=4200;
for I=1:N,
    if f(I) < f2
        I2=I;
    end
end
for I=N:-1:1,
    if f(I) > f1
        I1=I;
    end
end
max4=-200;
fmax4=0;
for I=I1:I2,
    if vo(I) > max4
        max4= vo(I);
        fmax4=f(I);
    end
end
%-------------------------------------------
% Find the value (max5) and the frequency (fmax5)
% of the 5th harmonic.
%-------------------------------------------
f1=4800;
f2=5200;
for $I=1:N,$
    if $f(I) < f2$
        $I2=I$;
    end
end
for $I=N:-1:1$,
    if $f(I) > f1$
        $I1=I$;
    end
end
$max5=-200$;
$fmax5=0$;
for $I=I1:I2$,
    if $vo(I) > max5$
        $max5= vo(I)$;
        $fmax5=f(I)$;
    end
end

%-------------------------------------------
% Find the value (max6) and the frequency (fmax6)
% of the 6th harmonic.
%-------------------------------------------
$f1=5800$;
$f2=6200$;
for $I=1:N$,
    if $f(I) < f2$
        $I2=I$;
    end
end
for $I=N:-1:1$,
    if $f(I) > f1$
        $I1=I$;
    end
end
$max6=-200$;
$fmax6=0$;
for $I=I1:I2$,
    if $vo(I) > max6$
        $max6= vo(I)$;
        $fmax6=f(I)$;
    end
end

%-------------------------------------------
% Find the value (max7) and the frequency (fmax7) % of the 7th harmonic.
%-------------------------------------------
fl=6800;
f2=7200;
for I=1:N,
    if f(I) < f2
        I2=I;
    end
end
for I=N:-1:1,
    if f(I) > f1
        I1=I;
    end
end
max7=-200;
fmax7=0;
for I=I1:I2,
    if vo(I) > max7
        max7= vo(I);
        fmax7=f(I);
    end
end
%-------------------------------------------
% Find the value (max8) and the frequency (fmax8) % of the 8th harmonic.
%-------------------------------------------
fl=7800;
f2=8200;
for I=1:N,
    if f(I) < f2
        I2=I;
    end
end
for I=N:-1:1,
    if f(I) > f1
        I1=I;
    end
end
max8=-200;
fmax8=0;
for I=I1:I2,
    if vo(I) > max8
\begin{verbatim}
max8= vo(I);
fmax8=f(I);
end
end
%---------------------------------------------------------------
% Find the value (max9) and the frequency (fmax9) 
% of the 9th harmonic. 
%---------------------------------------------------------------
f1=8800;
f2=9200;
for I=1:N,
  if f(I) < f2
    I2=I;
  end
end
for I=N:-1:1,
  if f(I) > f1
    I1=I;
  end
end
max9=-200;
fmax9=0;
for I=I1:I2,
  if vo(I) > max9
    max9= vo(I);
    fmax9=f(I);
  end
end
%---------------------------------------------------------------
% Find the value (max10) and the frequency (fmax10) 
% of the 10th harmonic. 
%---------------------------------------------------------------
f1=9800;
f2=10000;
for I=1:N,
  if f(I) < f2
    I2=I;
  end
end
for I=N:-1:1,
  if f(I) > f1
    I1=I;
  end
end
\end{verbatim}
end
max10=-200;
fmax10=0;
for I=I1:I2,
    if vo(I) > max10
        max10 = vo(I);
        fmax10 = f(I);
    end
end

% Convert dBV to voltage
max1v = 10^((max1/20);
max2v = 10^((max2/20);
max3v = 10^((max3/20);
max4v = 10^((max4/20);
max5v = 10^((max5/20);
max6v = 10^((max6/20);
max7v = 10^((max7/20);
max8v = 10^((max8/20);
max9v = 10^((max9/20);
max10v = 10^((max10/20);

% Calculate the Total Harmonic Distortion
Sigma_harmonics = ((max2v)^2 + (max3v)^2) + ((max4v)^2) + ((max5v)^2) + ((max6v)^2) + ((max7v)^2) + ((max8v)^2) + ((max9v)^2) + ((max10v)^2))^(0.5);
THD=Sigma_harmonics/max1v*100;

% Plot the frequency spectrum
plot(f,vo);
xlabel('Frequency [Hz]');
ylabel('Vout dBV');
APPENDIX B

CIRCUIT NETLISTS

This appendix contains the AFLAC netlists of the circuit presented in this dissertation.

$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
$$ Op Amp with constant gm input stage (AC method) $$
$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
Model MosfetLevelTwo
Model "CMOSN" FLAG=N LEVEL=2 PHI=0.700000 TOX=4.1300E-08
  + XJ=0.200000U TPG=1 VTO=0.8013
  + DELTA=3.385E+00 LD=1.469E-07 KP=4.4782E-05
  + UD=535.6 UEXP=1.3190E-01 UCRIT=9.3480E+04
  + RSH=6.488 GAMMA=0.5714 NSUB=6.877E+15
  + NFS=1.98E+11 NEFF=1.0000E+00 VMAX=5.653E+04
  + LAMBDA=3.184E-02 CGDD=3.842E-10 CGSO=3.8424E-10
  + CGBO=4.49E-10 CJ=1.25E-04 MJ=0.575
  + CSW=4.49E-10 MJ=0.292 PB=0.400000
** Weff = Wdrawn - Delta_W
**KP=1.675E-05
Model "CMOSP" FLAG=P LEVEL=2 PHI=0.700000 TOX=4.1300E-08
  + XJ=0.200000U TPG=-1 VTO=-0.9793
  + DELTA=5.845+00 LD=1.5170E-07 KP=1.5844E-05
  + UD=189.5 UEXP=2.4160E-01 UCRIT=1.0120E+05
  + RSH=1.0430E-01 GAMMA=0.6367 NSUB=8.5380E+15
  + NFS=3.27E+11 NEFF=1.0000E+00 VMAX=9.9990E+05
  + LAMBDA=4.1326E-10 CGDO=3.9026E-10 CGSO=3.9026E-10
  + CGBO=1.326E-10 CJ=3.27E-04 MJ=0.593
  + CSW=2.82E-10 MJ=0.341 PB=0.900000
$ Circuit definition:
MOSFET mn1 4 1 3 0 MODEL=MosfetLevelTwo
  + MODEL="cmosn" w=40um l=2um
MOSFET mn2 5 1 3 0 MODEL=MosfetLevelTwo
  + MODEL="cmosn" w=40um l=2um
MOSFET mn3 6 2 3 0 MODEL=MosfetLevelTwo
  + MODEL="cmosn" w=40um l=2um
MOSFET mn4 7 2 3 0 MODEL=MosfetLevelTwo
  + MODEL="cmosn" w=40um l=2um
MOSFET mp1 8 1 9 100 MODEL=MosfetLevelTwo $ HSPICE: U0=250
  + MODEL="cmosp" w=108um l=2um
MOSFET mp2 8 1 10 100 MODEL=MosfetLevelTwo $ HSPICE: U0=250
  + MODEL="cmosp" w=108um l=2um
MOSFET mp3 8 2 11 100 MODEL=MosfetLevelTwo $ HSPICE: U0=250
  + MODEL="cmosp" w=108um l=2um
MOSFET mp4 8 2 12 100 MODEL=MosfetLevelTwo $ HSPICE: U0=250
  + MODEL="cmosp" w=108um l=2um
MOSFET mp5 100 6 5 100 MODEL=MosfetLevelTwo $ HSPICE: U0=250
  + MODEL="cmosp" w=108um l=2um
MOSFET mp6 100 6 6 100 MODEL=MosfetLevelTwo $ HSPICE: U0=250
  + MODEL="cmosp" w=108um l=2um
MOSFET mp7 100 4 4 100 MODEL=MosfetLevelTwo $ HSPICE: U0=250
  + MODEL="cmosp" w=108um l=2um
MOSFET mp8 100 4 7 100 MODEL=MosfetLevelTwo $ HSPICE: U0=250
  + MODEL="cmosp" w=108um l=2um
MOSFET mn5 10 10 0 0 MODEL=MosfetLevelTwo
  + MODEL="cmosn" w=40um l=2um
MOSFET mn6 11 10 0 0 MODEL=MosfetLevelTwo
  + MODEL="cmosn" w=40um l=2um
MOSFET mn7 9 12 0 0 MODEL=MosfetLevelTwo
  + MODEL="cmosn" w=40um l=2um
MOSFET mn8 12 12 0 0 MODEL=MosfetLevelTwo
  + MODEL="cmosn" w=40um l=2um
MOSFET mp9 5 13 14 100 MODEL=MosfetLevelTwo
  + MODEL="cmosp" w=30um l=2um
MOSFET mp10 7 13 15 100 MODEL=MosfetLevelTwo
  + MODEL="cmosp" w=30um l=2um
$Max circuits
MOSFET mn9 16 14 0 0 MODEL=MosfetLevelTwo
  + MODEL="cmosn" w=15um l=2um
MOSFET mn10 14 14 0 0 MODEL=MosfetLevelTwo
  + MODEL="cmosn" w=15um l=2um
MOSFET mn11 14 9 0 0 MODEL=MosfetLevelTwo
  + MODEL="cmosn" w=15um l=2um
MOSFET mn12 9 9 0 0 MODEL=MosfetLevelTwo
+ MODEL="cmosn" w=15um l=2um
MOSFET mn13 16 9 0 0 MODEL=MosfetLevelTwo
+ MODEL="cmosn" w=15um l=2um
MOSFET mn14 17 15 0 0 MODEL=MosfetLevelTwo
+ MODEL="cmosn" w=15um l=2um
MOSFET mn15 15 15 0 0 MODEL=MosfetLevelTwo
+ MODEL="cmosn" w=15um l=2um
MOSFET mn16 15 11 0 0 MODEL=MosfetLevelTwo
+ MODEL="cmosn" w=15um l=2um
MOSFET mn17 11 11 0 0 MODEL=MosfetLevelTwo
+ MODEL="cmosn" w=15um l=2um
MOSFET mn18 17 11 0 0 MODEL=MosfetLevelTwo
+ MODEL="cmosn" w=15um l=2um
$ Output stage
MOSFET mp11 100 19 16 100 MODEL=MosfetLevelTwo $ HSPICE: U0=250
+ MODEL="cmosp" w=84um l=4um
MOSFET mp12 100 19 17 100 MODEL=MosfetLevelTwo $ HSPICE: U0=250
+ MODEL="cmosp" w=84um l=4um
MOSFET mp13 16 20 19 100 MODEL=MosfetLevelTwo $ HSPICE: U0=250
+ MODEL="cmosp" w=84um l=4um
MOSFET mp14 17 20 21 100 MODEL=MosfetLevelTwo $ HSPICE: U0=250
+ MODEL="cmosp" w=84um l=4um
MOSFET mp15 19 22 23 100 MODEL=MosfetLevelTwo $ HSPICE: U0=250
+ MODEL="cmosp" w=28um l=4um
MOSFET mp16 21 22 25 100 MODEL=MosfetLevelTwo $ HSPICE: U0=250
+ MODEL="cmosp" w=20um l=4um
MOSFET mp17 100 27 27 100 MODEL=MosfetLevelTwo $ HSPICE: U0=250
+ MODEL="cmosp" w=14um l=4um
MOSFET mp18 27 22 22 100 MODEL=MosfetLevelTwo $ HSPICE: U0=250
+ MODEL="cmosp" w=14um l=4um
MOSFET mn19 18 23 0 0 MODEL=MosfetLevelTwo
+ MODEL="cmosn" w=30um l=4um
MOSFET mn20 32 23 0 0 MODEL=MosfetLevelTwo
+ MODEL="cmosn" w=30um l=4um
MOSFET mn21 23 26 18 0 MODEL=MosfetLevelTwo
+ MODEL="cmosn" w=30um l=4um
MOSFET mn22 25 26 32 0 MODEL=MosfetLevelTwo
+ MODEL="cmosn" w=30um l=4um
MOSFET mn23 19 24 23 0 MODEL=MosfetLevelTwo
+ MODEL="cmosn" w=10um l=4um
MOSFET mn24 21 24 25 0 MODEL=MosfetLevelTwo
+ MODEL="cmosn" w=8um l=4um
MOSFET mn25 28 28 0 0 MODEL=MosfetLevelTwo
+ MODEL="cmosn" w=5um l=4um
MOSFET mn26 24 24 28 0 MODEL=MosfetLevelTwo
+ MODEL="cmosn" w=5um l=4um
Curr ib2 100 24 DC={ib2=2u}
Volt vb2 26 0 DC={vb2=1.7} I=I_vb2
Curr ib1 22 0 DC={ib1=1u}
Volt vb3 20 0 DC={vb3=1.3} I=I_vb3
Volt vb1 13 0 DC={vb1=1.45} I=I_vb1

MOSFET mn27 29 25 0 0 MODEL=MosfetLevelTwo
+ MODEL="cmosn" w=40um l=2um
MOSFET mp19 100 21 29 100 MODEL=MosfetLevelTwo
+ MODEL="cmosp" w=103um l=2um

$ n- and p-type current source
MOSFET mn28 3 33 34 0 MODEL=MosfetLevelTwo
+ MODEL="cmosn" w=60um l=2um
MOSFET mn29 33 35 0 MODEL=MosfetLevelTwo
+ MODEL="cmosn" w=60um l=2um
MOSFET mn30 34 35 0 0 MODEL=MosfetLevelTwo
+ MODEL="cmosn" w=60um l=2um
MOSFET mn31 35 35 0 0 MODEL=MosfetLevelTwo
+ MODEL="cmosn" w=60um l=2um
Curr ibn 100 33 DC={ibn=20n}

MOSFET mp20 100 36 37 100 MODEL=MosfetLevelTwo $ HSPICE: U0=250
+ MODEL="cmosp" w=120um l=2um
MOSFET mp21 100 36 100 MODEL=MosfetLevelTwo $ HSPICE: U0=250
+ MODEL="cmosp" w=120um l=2um
MOSFET mp22 37 38 100 MODEL=MosfetLevelTwo $ HSPICE: U0=250
+ MODEL="cmosp" w=120um l=2um
MOSFET mp23 36 38 38 100 MODEL=MosfetLevelTwo $ HSPICE: U0=250
+ MODEL="cmosp" w=120um l=2um
Curr ibp 38 0 DC={ibp=20n}

$ Compensation capacitors
Cap c1 21 29 9.9pf
Cap c2 25 29 9.9pf

$ Supply voltage
Volt vdd 100 0 DC={vdd=3} I=I_vdd
VCVS E1 1 99 1 98 0 [1] LINEAR
VCVS E2 2 99 1 98 0 [-1] LINEAR

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$ load resistance and capacitance
Res rload 29 39 10K
Cap cload 29 39 10pf
Volt vload 39 0 DC={vload=1.5} I=I_vload
$$$$$$$$ AC $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
Volt vcom 99 0 DC {com_val} I=I_vcm
Volt vin 98 0 AC=1 I=I_vd1

Sweep " Ac Analysis"
+ LOOP 31 APLACVAR com_val RANGE 31 LIN 0.3 0
+ LOOP 100 FREQ LOG 1 0.1MEG
+ LOGX
+ Y "AV" "db" 0 100

Show
+ Y MagdB(Vac(29)/(Vac(1)-Vac(2))) LINE (com_val)
+ Y Pha(Vac(29)) LINE (com_val)

print Format "%e" Real com_val
+ S " " Format "%e" Real (10^(loopindex*5/99))
+ S " " Format "%e" Real MagdB(Vac(29)/(Vac(1)-Vac(2)))+180
+ S " " Format "%e" Real Pha(Vac(29)) if
$$+ S " " Format "%e" Real Idc(I_vload) if
$$+ S " " Format "%e" Real Vdc(111)
$$+ S " " Format "%e" Real vdc(102) if
$$+ S " " Format "%e" Real Idc(I_vdd)
$$+ S " " Format "%e" Real Vdc(111)-vdc(102) if

ENDSweep

$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
$$ Op Amp with constant gm input stage (TIC method) $$
$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
Model MosfetLevelTwo
Model "CMOSN" FLAG=N LEVEL=2 PHI=0.700000 TOX=4.1300E-08
+ XJ=0.200000U TPG=1 VTO=0.8013
+ DELTA=3.385E+00 LD=1.469E-07 KP=4.4782E-05
+ U0=535.6 UEXP=1.3190E-01 UCRIT=9.3480E+04
+ RSH=6.488 GAMMA=0.5714 NSUB=6.877E+15
+ NFS=1.98E+11 NEFF=1.0000E+00 VMAX=5.653E+04

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+ LAMBDA=3.184E-02 CGD0=3.842E-10 CGS0=3.8424E-10
+ CGBO=3.4581E-10 CJ=1.25E-04 MJ=0.575
+ CJSW=4.49E-10 MJSW=0.292 PB=0.400000
** Weff = Wdrawn - Delta_W
** KP=1.675E-05
Model "CMOSP" FLAG=P LEVEL=2 PHI=0.700000 TDX=4.1300E-08
+ XJ=0.2000000U TPG=-1 VTO=-0.9793
+ DELTA=5.845+00 LD=1.5170E-07 KP=1.5844E-05
+ U0=189.5 UEXP=2.4160E-01 UCRT=1.0120E+05
+ RS=3.104E-01 GAMMA=0.6367 NSUB=8.5380E+15
+ NFS=3.27E+11 NEFF=1.0000E+00 VMAX=9.9999E+05
+ LAMBDA=4.1830E-02 CGD0=3.9026E-10 CGS0=3.9026E-10
+ CGBO=4.1326E-10 CJ=3.27E-04 MJ=0.593
+ CJSW=2.82E-10 MJSW=0.341 PB=0.900000

$ Circuit definition:
MOSFET mn1 3 1 4 0 MODEL=MosfetLevelTwo
+ MODEL="cmosn" w=40um l=4um
MOSFET mn2 5 2 4 0 MODEL=MosfetLevelTwo
+ MODEL="cmosn" w=40um l=4um

* p-channel differential input stage
MOSFET mp1 6 1 7 100 MODEL=MosfetLevelTwo $ HSPICE: U0=250
+ MODEL="cmosp" w=112um l=4um
MOSFET mp2 6 2 8 100 MODEL=MosfetLevelTwo $ HSPICE: U0=250
+ MODEL="cmosp" w=112um l=4um

* n-type current source
MOSFET mn3 9 9 0 0 MODEL=MosfetLevelTwo
+ MODEL="cmosn" w=30um l=8um
MOSFET mn4 4 9 0 0 MODEL=MosfetLevelTwo
+ MODEL="cmosn" w=30um l=8um
MOSFET mn5 8 9 0 0 MODEL=MosfetLevelTwo
+ MODEL="cmosn" w=30um l=8um
MOSFET mn6 7 9 0 0 MODEL=MosfetLevelTwo
+ MODEL="cmosn" w=30um l=8um
Curr ibn 100 9 DC={ibn=3u}

*p-type current source
MOSFET mp3 100 10 10 100 MODEL=MosfetLevelTwo $ HSPICE: U0=250
+ MODEL="cmosp" w=80um l=4um

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**Max circuit**

MOSFET mn7 3 3 11 0 MODEL=MosfetLevelTwo
+ MODEL="cmosn" w=20um l=4um
MOSFET mn8 12 3 13 0 MODEL=MosfetLevelTwo
+ MODEL="cmosn" w=20um l=4um
MOSFET mn9 16 5 17 0 MODEL=MosfetLevelTwo
+ MODEL="cmosn" w=20um l=4um
MOSFET mn10 5 5 15 0 MODEL=MosfetLevelTwo
+ MODEL="cmosn" w=20um l=4um
MOSFET mp7 11 8 8 100 MODEL=MosfetLevelTwo $ HSPICE: U0=250
+ MODEL="cmosp" w=84um l=4um
MOSFET mp8 13 8 14 100 MODEL=MosfetLevelTwo $ HSPICE: U0=250
+ MODEL="cmosp" w=84um l=4um
MOSFET mp9 17 7 18 100 MODEL=MosfetLevelTwo $ HSPICE: U0=250
+ MODEL="cmosp" w=84um l=4um
MOSFET mp10 15 7 7 100 MODEL=MosfetLevelTwo $ HSPICE: U0=250
+ MODEL="cmosp" w=84um l=4um

**Output stage**

MOSFET mp11 100 19 12 100 MODEL=MosfetLevelTwo $ HSPICE: U0=250
+ MODEL="cmosp" w=84um l=4um
MOSFET mp12 100 19 16 100 MODEL=MosfetLevelTwo $ HSPICE: U0=250
+ MODEL="cmosp" w=84um l=4um
MOSFET mp13 12 20 19 100 MODEL=MosfetLevelTwo $ HSPICE: U0=250
+ MODEL="cmosp" w=84um l=4um
MOSFET mp14 16 20 21 100 MODEL=MosfetLevelTwo $ HSPICE: U0=250
+ MODEL="cmosp" w=84um l=4um
MOSFET mp15 19 22 23 100 MODEL=MosfetLevelTwo $ HSPICE: U0=250
+ MODEL="cmosp" w=28um l=4um
MOSFET mp16 21 22 25 100 MODEL=MosfetLevelTwo $ HSPICE: U0=250
+ MODEL="cmosp" w=20um l=4um
MOSFET mp17 100 27 27 100 MODEL=MosfetLevelTwo $ HSPICE: U0=250
+ MODEL="cmosp" w=14um l=4um
MOSFET mp18 27 22 22 100 MODEL=MosfetLevelTwo $ HSPICE: U0=250
+ MODEL="cmosp" w=14um l=4um
Curr ib1 22 0 DC={ib1=4u} 
Volt vb2 20 0 DC={vb2=1.2} I=I_vb2 
MOSFET mn11 18 23 0 0 MODEL=MosfetLevelTwo 
  + MODEL="cmosn" w=30um l=4um 
MOSFET mn12 14 23 0 0 MODEL=MosfetLevelTwo 
  + MODEL="cmosn" w=30um l=4um 
MOSFET mn13 23 26 18 0 MODEL=MosfetLevelTwo 
  + MODEL="cmosn" w=29um l=4um 
MOSFET mn14 25 26 14 0 MODEL=MosfetLevelTwo 
  + MODEL="cmosn" w=29um l=4um 
MOSFET mn15 19 24 23 0 MODEL=MosfetLevelTwo 
  + MODEL="cmosn" w=10um l=4um 
MOSFET mn16 21 24 25 0 MODEL=MosfetLevelTwo 
  + MODEL="cmosn" w=10um l=4um 
MOSFET mn17 28 28 0 0 MODEL=MosfetLevelTwo 
  + MODEL="cmosn" w=5um l=4um 
MOSFET mn18 24 24 28 0 MODEL=MosfetLevelTwo 
  + MODEL="cmosn" w=5um l=4um 
Curr ib2 100 24 DC={ib2=4u} 
Voltp vbl 26 0 DC={vb1=1.7} I=I_vbl 

MOSFET mn19 29 25 0 0 MODEL=MosfetLevelTwo 
  + MODEL="cmosn" w=40um l=2um 
MOSFET mp19 100 21 29 100 MODEL=MosfetLevelTwo $ HSPICE: UO=250 
  + MODEL="cmosp" w=110um l=2um 

* Compensation capacitors 
Cap c1 21 29 2.69pf 
Cap c2 25 29 2.69pf 

* Supply voltage 
Volt vdd 100 0 DC={vdd=3} I=I_vdd 

VCVS E1 1 99 1 98 0 [1] LINEAR 
VCVS E2 2 99 1 98 0 [-1] LINEAR 

* Load resistance and capacitance 
Res rlace 29 30 1OK 
Cap clace 29 30 10pf 
Voipt vload 30 0 DC={vload=1.5} I=I_vload
$\text{Sweep "Ac Analysis"}
+ \text{LOOP 3 APLICVAR com_val RANGE 3 LIN 0.5 2.5}
+ \text{LOOP 100 FREQ LOG 1 1OMEG}
+ \text{LOGX}
+ \text{Y "AV" "db" 0 100}

\text{Show}
+ \text{Y MagdB(Vac(29)/(Vac(1)-Vac(2))) LINE (com_val)}
+ \text{Y Pha(Vac(29)) LINE (com_val)}
\text{ENDSweep}

$\text{VGA1}$

$\text{.MODEL definitions:}$
\text{Model MosfetLevelTwo}
\text{Model "CMOSN" FLAG=N LEVEL=2 PHI=0.600000 T0X=4.1000E-08}
+ XJ=0.200000 TPG=1 VTO=0.8177
+ DELTA=6.6420E+00 LD=2.4780E-07 KP=4.7401E-05
+ UO=562.8 UEXP=1.5270E-01 UCRIT=7.7040E+04
+ RSH=2.4000E+01 GAMMA=0.4374 NSUB=4.0880E+15
+ NFS=1.9800E+11 NEFF=1.0000E+00 VMAX=5.8030E+04
+ LAMBDA=3.1840E-02 CGDO=3.1306E-10 CGSO=3.1306E-10
+ CGBO=4.3449E-10 CJ=9.5711E-05 MJ=0.7817
+ CJSW=5.0429E-10 MJSW=0.346510 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -5.4940E-07
\text{Model "CMOSp" FLAG=P LEVEL=2 PHI=0.600000 T0X=4.1000E-08}
+ XJ=0.200000 TPG=-1 VTO=-0.8356
+ DELTA=5.7540E+00 LD=3.0910E-07 KP=1.7106E-05
+ UO=203.1 UEXP=2.1320E-01 UCRIT=8.0280E+04
+ RSH=6.6770E+01 GAMMA=0.6180 NSUB=8.1610E+15
+ NFS=3.2700E+11 NEFF=1.5000E+00 VMAX=9.9990E+04
+ LAMBDA=4.5120E-02 CGDO=3.9050E-10 CGSO=3.9050E-10
+ CGBO=4.1280E-10 CJ=3.2437E-04 MJ=0.5637
+ CJSW=3.3912E-10 MJSW=0.275876 PB=0.800000

$ Circuit definition:
MOSFET mn1 6 1 5 5 MODEL=MosfetLevelTwo
+ MODEL="cmosn" w=500um l=2um
MOSFET mm2 7 2 8 8 MODEL=MosfetLevelTwo
+ MODEL="cmosn" w=500um l=2um
MOSFET mp1 5 3 0 5 MODEL=MosfetLevelTwo $ HSPICE: UO=250
+ MODEL="cmosp" w=1500um l=2um
MOSFET mp2 8 3 0 8 MODEL=MosfetLevelTwo $ HSPICE: UO=250
+ MODEL="cmosp" w=1500um l=2um
MOSFET mn3 6 1 12 12 MODEL=MosfetLevelTwo
+ MODEL="cmosn" w=500um l=2um
MOSFET mn4 6 2 14 14 MODEL=MosfetLevelTwo
+ MODEL="cmosn" w=500um l=2um
MOSFET mp3 12 4 0 12 MODEL=MosfetLevelTwo $ HSPICE: UO=250
+ MODEL="cmosp" w=1500um l=2um
MOSFET mp4 14 4 0 14 MODEL=MosfetLevelTwo $ HSPICE: UO=250
+ MODEL="cmosp" w=1500um l=2um
Volt vshort 4 0 DC={vshort=0} I=I_vshort
MOSFET mp5 100 15 15 100 MODEL=MosfetLevelTwo $ HSPICE: UO=250
+ MODEL="cmosp" w=6000um l=4um
MOSFET mp6 100 15 6 100 MODEL=MosfetLevelTwo $ HSPICE: UO=250
+ MODEL="cmosp" w=6000um l=4um
MOSFET mp7 100 15 10 100 MODEL=MosfetLevelTwo $ HSPICE: UO=250
+ MODEL="cmosp" w=6000um l=4um
Curr ibinl 15 0 DC={ibinl=3m}
MOSFET mp8 6 25 26 6 MODEL=MosfetLevelTwo $ HSPICE: UO=250
+ MODEL="cmosp" w=2500um l=2um
MOSFET mp9 7 25 27 7 MODEL=MosfetLevelTwo $ HSPICE: UO=250
+ MODEL="cmosp" w=2500um l=2um
Volt vgate1 25 0 DC={vgate1=1.5} I=I_vgate1
Res r1 26 0 2000
Res r2 27 0 2000
MOSFET mp10 100 20 16 100 MODEL=MosfetLevelTwo $ HSPICE: UO=250
+ MODEL="cmosp" w=900um l=4um
MOSFET mp11 100 20 20 100 MODEL=MosfetLevelTwo $ HSPICE: UO=250
+ MODEL="cmosp" w=900um l=4um
Curr ibiasl 20 19 DC={ibiasl=600u}
MOSFET mp12 16 26 17 100 MODEL=MosfetLevelTwo $ HSPICE: UO=250
+ MODEL="cmosp" w=240um l=2um
MOSFET mp13 16 27 18 100 MODEL=MosfetLevelTwo $ HSPICE: UO=250
+ MODEL="cmosp" w=240um l=2um

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MOSFET mn5 17 17 0 0 MODEL=Mosfet LevelTwo
+ MODEL="cmosn" w=200µm l=2µm
MOSFET mn6 18 17 0 0 MODEL=Mosfet LevelTwo
+ MODEL="cmosn" w=200µm l=2µm
Res r11 100 18 240k
Res r12 18 0 60k

******************************************************************************
* current controlled resistor
MOSFET mn402 301 401 0 0 MODEL=Mosfet LevelTwo
+ MODEL="cmosn" w=12µm l=4µm
MOSFET mp400 100 302 302 100 MODEL=Mosfet LevelTwo $ HSPICE: U0=250
+ MODEL="cmosp" w=160µm l=4µm
MOSFET mp401 100 302 401 100 MODEL=Mosfet LevelTwo $ HSPICE: U0=250
+ MODEL="cmosp" w=5µm l=4µm
MOSFET mn601 401 401 0 0 MODEL=Mosfet LevelTwo
+ MODEL="cmosn" w=15µm l=4µm

* control circuit
MOSFET mn300 302 300 0 0 MODEL=Mosfet LevelTwo
+ MODEL="cmosn" w=12µm l=8µm
MOSFET mn301 300 300 0 0 MODEL=Mosfet LevelTwo
+ MODEL="cmosn" w=12µm l=8µm
MOSFET mp300 100 300 301 100 MODEL=Mosfet LevelTwo $ HSPICE: U0=250
+ MODEL="cmosp" w=36µm l=8µm
MOSFET mp301 100 300 300 100 MODEL=Mosfet LevelTwo $ HSPICE: U0=250
+ MODEL="cmosp" w=36µm l=8µm

Curr itest 305 0 DC={itest=0.0}
Curr itest 305 0 DC={itest=31e-6}
Volt vts9 305 300 DC={vts9=1.5} I=I_vts9
Volt vshort1 3 301 DC={vshort1=0} I=I_vshort1
VCVS E1 1 1200 1 1201 0 [0.5] LINEAR
VCVS E2 2 1200 1 1201 0 [-0.5] LINEAR
Volt vin 1201 0 DC={vin=0.01} I=I_vin
Volt vcom 1200 0 DC={vcom=2.4} I=I_vcom
Volt vdd 100 0 DC={vdd=3v} I=I_vdd

* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -4.1580E-07

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.MODEL definitions:
$ HSPICE defaults:
Model MosfetLevelTwo
Model "CMOSn" FLAG=N LEVEL=2 PHI=0.600000 TOX=4.10000E-08
+ XJ=0.200000U TPG=1 VT0=0.8177
+ DELTA=6.6420E+00 LD=2.4780E-07 KP=4.7401E-05
+ U0=562.8 UEXP=1.5270E-01 UCRIT=7.7040E+04
+ RSH=2.4000E+01 GAMMA=0.4374 NSUB=4.0880E+15
+ NFS=1.9800E+11 NEFF=1.0000E+00 VMAX=5.8030E+04
+ LAMBDA=3.1840E-02 CGDO=3.1306E-10 CGSO=3.1306E-10
+ CGBO=4.3449E-10 CJ=9.5711E-05 MJ=0.7817
+ CJSW=5.0429E-10 MJSW=0.346510 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -5.4940E-07
Model "CMOSp" FLAG=P LEVEL=2 PHI=0.600000 TOX=4.10000E-08
+ XJ=0.200000U TPG=-1 VT0=-0.8356
+ DELTA=5.7540E+00 LD=3.0910E-07 KP=1.7106E-05
+ U0=203.1 UEXP=2.1320E-01 UCRIT=8.0280E+04
+ RSH=5.6770E+01 GAMMA=0.6180 NSUB=8.1610E+15
+ NFS=3.270E+11 NEFF=1.5000E+00 VMAX=9.9990E+05
+ LAMBDA=4.5120E-02 CGDO=3.9050E-10 CGSO=3.9050E-10
+ CGBO=4.1280E-10 CJ=3.2437E-04 MJ=0.5637
+ CJSW=3.3912E-10 MJSW=0.275876 PB=0.800000

$ Circuit definition:
* first stage
MOSFET mn1 6 1 5 0 MODEL=MosfetLevelTwo
+ MODEL=":cmosn" w=5um l=2um
MOSFET mn2 100 7 5 0 MODEL=MosfetLevelTwo
+ MODEL=":cmosn" w=100um l=2um
MOSFET mn3 8 8 0 0 MODEL=MosfetLevelTwo
+ MODEL=":cmosn" w=120um l=2um
MOSFET mn4 5 8 0 0 MODEL=MosfetLevelTwo
+ MODEL=":cmosn" w=120um l=4um
MOSFET mn5 12 8 0 0 MODEL=MosfetLevelTwo
+ MODEL=":cmosn" w=120um l=4um
Curr ii 100 8 DC={il=120u}
MOSFET mp1 100 6 6 100 MODEL=MosfetLevelTwo $ HSPICE: U0=250
+ MODEL=":cmosp" w=60um l=2um
MOSFET mp2 100 6 7 100 MODEL=MosfetLevelTwo $ HSPICE: U0=250
+ MODEL="cmosp" w=60um l=2um
MOSFET mp3 7 3 0 100 MODEL=MosfetLevelTwo $ HSPICE: UO=250
+ MODEL="cmosp" w=15um l=2um
MOSFET mp4 100 6 9 100 MODEL=MosfetLevelTwo $ HSPICE: UO=250
+ MODEL="cmosp" w=60um l=2um
SHORT vcon13 9 7 31 I_L_vcon13
MOSFET mn6 11 2 12 0 MODEL=MosfetLevelTwo
+ MODEL="cmosn" w=5um l=2um
MOSFET mn7 100 13 12 0 MODEL=MosfetLevelTwo
+ MODEL="cmosn" w=100um l=2um
MOSFET mp5 100 11 13 100 MODEL=MosfetLevelTwo $ HSPICE: UO=250
+ MODEL="cmosp" w=60um l=2um
MOSFET mp6 100 11 11 100 MODEL=MosfetLevelTwo $ HSPICE: UO=250
+ MODEL="cmosp" w=60um l=2um
MOSFET mp7 13 3 0 100 MODEL=MosfetLevelTwo $ HSPICE: UO=250
+ MODEL="cmosp" w=15um l=2um
MOSFET mp8 100 11 10 100 MODEL=MosfetLevelTwo $ HSPICE: UO=250
+ MODEL="cmosp" w=60um l=2um
*second stage
MOSFET mn8 26 1 25 0 MODEL=MosfetLevelTwo
+ MODEL="cmosn" w=5um l=2um
MOSFET mn9 100 27 25 0 MODEL=MosfetLevelTwo
+ MODEL="cmosn" w=100um l=2um
MOSFET mn10 25 8 0 0 MODEL=MosfetLevelTwo
+ MODEL="cmosn" w=120um l=4um
MOSFET mn11 212 8 0 0 MODEL=MosfetLevelTwo
+ MODEL="cmosn" w=120um l=4um
MOSFET mp9 100 26 26 100 MODEL=MosfetLevelTwo $ HSPICE: UO=250
+ MODEL="cmosp" w=60um l=2um
MOSFET mp10 100 26 27 100 MODEL=MosfetLevelTwo $ HSPICE: UO=250
+ MODEL="cmosp" w=60um l=2um
MOSFET mp11 27 4 0 100 MODEL=MosfetLevelTwo $ HSPICE: UO=250
+ MODEL="cmosp" w=15um l=2um
MOSFET mp12 100 26 10 100 MODEL=MosfetLevelTwo $ HSPICE: UO=250
+ MODEL="cmosp" w=60um l=2um
MOSFET mn12 211 2 212 0 MODEL=MosfetLevelTwo
+ MODEL="cmosn" w=5um l=2um
MOSFET mn13 100 213 212 0 MODEL=MosfetLevelTwo
+ MODEL="cmosn" w=100um l=2um
MOSFET mp13 100 211 213 100 MODEL=MosfetLevelTwo $ HSPICE: UO=250
+ MODEL="cmosp" w=60um l=2um
MOSFET mp14 100 211 211 100 MODEL=MosfetLevelTwo $ HSPICE: UO=250
+ MODEL="cmosp" w=60um l=2um

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MOSFET mpl5 213 4 0 100 MODEL=MosfetLevelTwo $ HSPICE: U0=250
+ MODEL="cmosp" w=15um l=2um
MOSFET mpl6 100 211 9 100 MODEL=MosfetLevelTwo $ HSPICE: U0=250
+ MODEL="cmosp" w=60um l=2um
SHORT vc2 4 0 I I_vc2

*****************************************************************************
* output stage
*****************************************************************************
MOSFET mp17 9 730 712 100 MODEL=MosfetLevelTwo $ HSPICE: U0=250
+ MODEL="cmosp" w=60um l=2um
MOSFET mp18 10 730 713 100 MODEL=MosfetLevelTwo $ HSPICE: U0=250
+ MODEL="cmosp" w=60um l=2um
Volt vbias1 730 0 DC={vbias1=1.0} I=I_vbias1
MOSFET mn14 712 712 0 0 MODEL=MosfetLevelTwo
+ MODEL="cmosn" w=20um l=2um
MOSFET mn15 713 712 0 0 MODEL=MosfetLevelTwo
+ MODEL="cmosn" w=20um l=2um
MOSFET mp76 100 840 707 100 MODEL=MosfetLevelTwo $ HSPICE: U0=250
+ MODEL="cmosp" w=40um l=4um
MOSFET mp77 100 840 840 100 MODEL=MosfetLevelTwo $ HSPICE: U0=250
+ MODEL="cmosp" w=40um l=4um
Curr ibout 840 0 DC={ibout=29u}
MOSFET mn81 707 835 830 0 MODEL=MosfetLevelTwo
+ MODEL="cmosn" w=20um l=2um
MOSFET mn89 830 713 0 0 MODEL=MosfetLevelTwo
+ MODEL="cmosn" w=10um l=2um
Volt vbnbias 835 0 DC={vbnbias=1.6} I=I_vbnbias
MOSFET mp70 100 700 700 100 MODEL=MosfetLevelTwo $ HSPICE: U0=250
+ MODEL="cmosp" w=24um l=2um
MOSFET mn70 702 702 0 0 MODEL=MosfetLevelTwo
+ MODEL="cmosn" w=6um l=2um
MOSFET mp71 100 700 703 100 MODEL=MosfetLevelTwo $ HSPICE: U0=250
+ MODEL="cmosp" w=72um l=2um
MOSFET mn71 703 702 0 0 MODEL=MosfetLevelTwo
+ MODEL="cmosn" w=18um l=2um
MOSFET mp72 707 708 702 100 MODEL=MosfetLevelTwo $ HSPICE: U0=250
+ MODEL="cmosp" w=108um l=2um
MOSFET mn72 700 706 707 0 MODEL=MosfetLevelTwo
+ MODEL="cmosn" w=40um l=2um
Volt vgp 708 0 DC={vgp=0.4} I=I_vgp
Volt vgn 706 0 DC={vgn=2.5} I=I_vgn
Res rf1 838 713 500k
SHORT vfeed 707 838 I I_vfeed
Res ro 705 729 40k
Volt vll 729 0 DC={vll=1.5} I=I_vll
*current controled resistor
MOSFET mn402 402 401 0 0 MODEL=MosfetLevelTwo
+ MODEL="cmosn" w=12um l=4um
MOSFET mp400 100 403 403 100 MODEL=MosfetLevelTwo $ HSPICE: UO=250
+ MODEL="cmosp" w=160um l=4um
MOSFET mp401 100 403 401 100 MODEL=MosfetLevelTwo $ HSPICE: UO=250
+ MODEL="cmosp" w=160um l=4um
MOSFET mn601 401 401 0 0 MODEL=MosfetLevelTwo
+ MODEL="cmosn" w=5um l=4um
MOSFET mp601 100 401 403 100 MODEL=MosfetLevelTwo $ HSPICE: UO=250
+ MODEL="cmosp" w=15um l=4um
*control circuit
MOSFET mn300 403 300 0 0 MODEL=MosfetLevelTwo
+ MODEL="cmosn" w=12um l=8um
MOSFET mn301 300 300 0 0 MODEL=MosfetLevelTwo
+ MODEL="cmosn" w=12um l=8um
MOSFET mp300 100 300 402 100 MODEL=MosfetLevelTwo $ HSPICE: UO=250
+ MODEL="cmosp" w=36um l=4um
MOSFET mp301 100 300 300 100 MODEL=MosfetLevelTwo $ HSPICE: UO=250
+ MODEL="cmosp" w=36um l=8um
Curr itest 300 0 DC={itest=0.0}
SHORT vcl 3 402 I I_vcl
VCVS E1 1 99 1 98 0 [0.5] LINEAR
VCVS E2 2 99 1 98 0 [-0.5] LINEAR
Volt vcom 99 0 DC={vcom=2.05} I=I_vcom
Volt vin 98 99 DC={vin=0.01} I=I_vin
Volt vdd 100 0 DC={vdd=3v} I=I_vdd
$ Analysis commands:
$ .dc itest -30e-6 31e-6 0.5e-6
Sweep "DC Analysis" DC
+ LOOP (1+(31e-6-(-30e-6))/(0.5e-6)) APLACVAR itest LIN -30e-6 31e-6
+ NW=1
EndSweep
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