INFORMATION TO USERS

While the most advanced technology has been used to photograph and reproduce this manuscript, the quality of the reproduction is heavily dependent upon the quality of the material submitted. For example:

- Manuscript pages may have indistinct print. In such cases, the best available copy has been filmed.

- Manuscripts may not always be complete. In such cases, a note will indicate that it is not possible to obtain missing pages.

- Copyrighted material may have been removed from the manuscript. In such cases, a note will indicate the deletion.

Oversize materials (e.g., maps, drawings, and charts) are photographed by sectioning the original, beginning at the upper left-hand corner and continuing from left to right in equal sections with small overlaps. Each oversize page is also filmed as one exposure and is available, for an additional charge, as a standard 35mm slide or as a 17"x23" black and white photographic print.

Most photographs reproduce acceptably on positive microfilm or microfiche but lack the clarity on xerographic copies made from the microfilm. For an additional charge, 35mm slides of 6"x9" black and white photographic prints are available for any photographs or illustrations that cannot be reproduced satisfactorily by xerography.
Lee, Yung-Huei

DUAL-CARRIER CHARGE TRANSPORT AND DAMAGE FORMATION OF LPCVD NITRIDE FOR NONVOLATILE MEMORY DEVICES

The Ohio State University

University Microfilms International 300 N. Zeeb Road, Ann Arbor, MI 48106

Copyright 1986 by Lee, Yung-Huei All Rights Reserved
PLEASE NOTE:

In all cases this material has been filmed in the best possible way from the available copy. Problems encountered with this document have been identified here with a check mark ✓.

1. Glossy photographs or pages ______
2. Colored illustrations, paper or print ______
3. Photographs with dark background ✓
4. Illustrations are poor copy ______
5. Pages with black marks, not original copy ______
6. Print shows through as there is text on both sides of page ______
7. Indistinct, broken or small print on several pages ______
8. Print exceeds margin requirements ______
9. Tightly bound copy with print lost in spine ______
10. Computer printout pages with indistinct print ______
11. Page(s) _______ lacking when material received, and not available from school or author.
12. Page(s) _______ seem to be missing in numbering only as text follows.
13. Two pages numbered ______. Text follows.
14. Curling and wrinkled pages ______
15. Dissertation contains pages with print at a slant, filmed as received ______
16. Other ____________________________
    ____________________________
    ____________________________

University
Microfilms
International
DUAL-CARRIER CHARGE TRANSPORT AND DAMAGE FORMATION
OF LPCVD NITRIDE FOR NONVOLATILE MEMORY DEVICES

DISSERTATION

Presented in Partial Fulfillment of the Requirements for
the Degree Doctor of Philosophy in the Graduate School
of The Ohio State University

by

Yung-Huei Lee, B.S., M.Sc.

* * * * *

The Ohio State University
1986

Reading Committee:

Dr. J.G. Gottling
Dr. M.O. Thurston
Dr. G.J. Valco
Dr. S.B. Bibyk

Approved by

[Signature]
Advisor
Department of Electrical Engineering
Copyright by
Yung-Huei Lee
1986
To my mother
and my fiancee
ACKNOWLEDGMENTS

The author wishes to express his sincere appreciation and gratitude to his advisor, Dr. J.G. Gottling, for his advice, encouragement, and support in the completion of this research. The author is also grateful to Dr. M.O. Thurston for his guidance and continuing encouragement. He is indebted to Dr. S.B. Biblyk for his constructive criticism, support, and generosity throughout this project. The author is also grateful to Dr. G.J. Valco for his assistance. For providing samples, services, and many helpful suggestions, the author would like to extend his appreciation to Dr. K.M. Chang of Motorola Corporation, Mr. S.O. Chen of Intel Corporation, and to Mr. R. Turi of NCR Corporation. The author also express deep appreciation to his seniors Dr. Gian Gerosa, Dr. Jose Maiz, Dr. Babak Sabi, and his friends at The Ohio State University for their stimulating conversations and support.

For sponsoring and supporting this research, the author would like to thank Dr. J. Hollander of The Ohio State University Office of Research and Graduate Studies, Dr. G.R. St. Pierre of the Department of Metallurgical Engineering, and Dr. D. Silversmith of the National Science Foundation (contract No. ECS-8504535).
VITA

Yung-Huei Lee

January 30, 1956  Born: Taipei, Taiwan, The Republic of China

1979  B.S. Electrophysics, National Chiao-Tung University
      Hsinchu, Taiwan

1979-1981  Lieutenant, Chinese Air Force
           Taiwan, The Republic of China

1982  M.Sc. Electrical Engineering, The Ohio State
      University, Columbus, Ohio

1982-1986  Research Associate, Department of Electrical
           Engineering, The Ohio State University

1984  Device Engineer, Technology Development, Intel Corp.,
      Aloha, Oregon

1983-1985  Teaching Associate, Department of Electrical
           Engineering, The Ohio State University

FIELD OF STUDY

Studies in Semiconductor Devices:  Dr. M.O. Thurston
Studies in Electronics:  Dr. J.G. Gottling
Studies in Electromagnetics:  Dr. R.G. Kouyoumjian
Studies in Quantum Mechanics:  Dr. K. Tanaka
Studies in Mathematics:  Dr. S. Drobot
# TABLE OF CONTENTS

<table>
<thead>
<tr>
<th>DEDICATION</th>
<th>ii</th>
</tr>
</thead>
<tbody>
<tr>
<td>ACKNOWLEDGMENTS</td>
<td>iii</td>
</tr>
<tr>
<td>VITA</td>
<td>iv</td>
</tr>
<tr>
<td>LIST OF TABLES</td>
<td>viii</td>
</tr>
<tr>
<td>LIST OF FIGURES</td>
<td>ix</td>
</tr>
</tbody>
</table>

## CHAPTER

1. **INTRODUCTION**

2. **DEVICE FABRICATION**

   2.1 Al-gate and Au-gate capacitors

   2.2 SONOS and SNOS Structures

      2.2.1 LOCOS Process

      2.2.2 ONO and NO gate

      2.2.3 Passivation, Contact, and Metalization

   2.3 Dual-Channel Transistors

3. **EXPERIMENT METHODOLOGY**

   3.1 Experimental Apparatus

   3.2 I-V Measurement

   3.3 C-V Measurement

   3.4 Constant Voltage Stress I-t Measurement

   3.5 Constant Current Stress V-t Measurement
<table>
<thead>
<tr>
<th>CHAPTER</th>
<th>PAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>4. STEADY-STATE CHARGE TRANSPORT</td>
<td>45</td>
</tr>
<tr>
<td>4.1 Principal Formulations</td>
<td>48</td>
</tr>
<tr>
<td>4.2 Single Trap level, Single Current</td>
<td>54</td>
</tr>
<tr>
<td>4.2.1 Hole Flow</td>
<td>54</td>
</tr>
<tr>
<td>4.2.2 Electron Flow</td>
<td>58</td>
</tr>
<tr>
<td>4.3 Two Trap Levels, Two Currents</td>
<td>62</td>
</tr>
<tr>
<td>4.3.1 No Detrapping</td>
<td>62</td>
</tr>
<tr>
<td>4.3.2 Trapping and Detrapping Without Recombination</td>
<td>73</td>
</tr>
<tr>
<td>5. RESULTS AND ANALYSIS</td>
<td>84</td>
</tr>
<tr>
<td>5.1 Current Distribution and Energy Band Diagram</td>
<td>84</td>
</tr>
<tr>
<td>5.1.1 Gold-Gate Capacitors</td>
<td>85</td>
</tr>
<tr>
<td>5.1.2 Aluminum-Gate Capacitors</td>
<td>93</td>
</tr>
<tr>
<td>5.1.3 Poly-Gate Capacitors</td>
<td>95</td>
</tr>
<tr>
<td>5.2 Constant Voltage Stress</td>
<td>105</td>
</tr>
<tr>
<td>5.2.1 Gold-Gate Capacitors</td>
<td>108</td>
</tr>
<tr>
<td>5.2.2 N+ Poly-Gate Capacitors</td>
<td>110</td>
</tr>
<tr>
<td>5.3 Role of Thick Oxide in Nonvolatile Memory Devices</td>
<td>112</td>
</tr>
<tr>
<td>5.4 In Search of The Clue</td>
<td>115</td>
</tr>
<tr>
<td>5.4.1 Flat-Band Voltage Change under Constant Voltage Stress</td>
<td>120</td>
</tr>
<tr>
<td>5.4.2 Effective Charge Change under Constant Voltage Stress</td>
<td>128</td>
</tr>
<tr>
<td>5.5 Analysis of Constant Current Stress Result</td>
<td>130</td>
</tr>
<tr>
<td>CHAPTER</td>
<td>PAGE</td>
</tr>
<tr>
<td>---------</td>
<td>------</td>
</tr>
<tr>
<td>5</td>
<td>RESULTS AND ANALYSIS (cont’d)</td>
</tr>
<tr>
<td>5.6</td>
<td>Numerical Simulation</td>
</tr>
<tr>
<td>5.7</td>
<td>A Double Turnaround Curve</td>
</tr>
<tr>
<td>6</td>
<td>DISCUSSION</td>
</tr>
<tr>
<td>6.1</td>
<td>Electron and Hole Flow</td>
</tr>
<tr>
<td>6.2</td>
<td>Metal-Gate MNOS Devices</td>
</tr>
<tr>
<td>6.2.1</td>
<td>MNOS Devices Under Positive Bias</td>
</tr>
<tr>
<td>6.2.2</td>
<td>MNOS Devices Under Negative Bias</td>
</tr>
<tr>
<td>6.3</td>
<td>N+ Poly-Gate MNOS Devices</td>
</tr>
<tr>
<td>6.3.1</td>
<td>Injection Under Positive Bias</td>
</tr>
<tr>
<td>6.3.2</td>
<td>Injection Under Negative Bias</td>
</tr>
<tr>
<td>6.4</td>
<td>I-V Asymmetry</td>
</tr>
<tr>
<td>6.5</td>
<td>Two Components of Tunneling Current in SNS Structures</td>
</tr>
<tr>
<td>6.6</td>
<td>Nitride Breakdown</td>
</tr>
<tr>
<td>6.6.1</td>
<td>Breakdown Mechanism</td>
</tr>
<tr>
<td>6.6.2</td>
<td>Two-Step MNOS Dual-Dielectric Breakdown</td>
</tr>
<tr>
<td>7</td>
<td>CONCLUSIONS AND FUTURE STUDIES</td>
</tr>
</tbody>
</table>

APPENDICES

A. General Case of Dual-Carrier Flow | 185 |
B. Relation Between $\Delta V_g$ and $\Delta V_p$ During Charge Injection | 189 |

LIST OF REFERENCES | 196 |
# LIST OF TABLES

<table>
<thead>
<tr>
<th>TABLE</th>
<th>PAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Dual-dielectric thickness</td>
<td>10</td>
</tr>
<tr>
<td>2. Split information of N-channel devices</td>
<td>18</td>
</tr>
<tr>
<td>3. Dielectric gate thickness of CMOS devices</td>
<td>25</td>
</tr>
<tr>
<td>4. Definitions of variables and coefficients in the charge transport kinetics equations</td>
<td>52</td>
</tr>
<tr>
<td>5. $E_{RM}$ and $x_{RM}$ for no recombination case</td>
<td>83</td>
</tr>
<tr>
<td>6. Summary of the charge trapping with both positive and negative bias</td>
<td>121</td>
</tr>
<tr>
<td>7. Results of the flat-band voltage shift after 600 seconds current stressing for Au-gate devices</td>
<td>135</td>
</tr>
<tr>
<td>8. I-V measurement data for SNS devices with 280 Å nitride dielectric</td>
<td>164</td>
</tr>
</tbody>
</table>
# LIST OF FIGURES

<table>
<thead>
<tr>
<th>FIGURE</th>
<th>PAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Cross section of a MNOS capacitor</td>
<td>12</td>
</tr>
<tr>
<td>2. Define isolation region</td>
<td>14</td>
</tr>
<tr>
<td>3. Blanket field implant</td>
<td>14</td>
</tr>
<tr>
<td>4. Field oxide growth</td>
<td>15</td>
</tr>
<tr>
<td>5. Threshold voltage adjustment implant</td>
<td>15</td>
</tr>
<tr>
<td>6. ONO deposition</td>
<td>17</td>
</tr>
<tr>
<td>7. Isolation for S/D diffusion</td>
<td>17</td>
</tr>
<tr>
<td>8. S/D implant</td>
<td>19</td>
</tr>
<tr>
<td>9. Passivation and contact holes</td>
<td>19</td>
</tr>
<tr>
<td>10. Metalization</td>
<td>21</td>
</tr>
<tr>
<td>11. Top view of the n-channel transistor</td>
<td>22</td>
</tr>
<tr>
<td>12. Top view of the capacitor</td>
<td>22</td>
</tr>
<tr>
<td>13. Cross section of the twin-tub dual-channel device</td>
<td>25</td>
</tr>
<tr>
<td>14. Complete experimental arrangement</td>
<td>27</td>
</tr>
<tr>
<td>15. Energy band diagram of MONOS and SONOS structures with poly-Si, Au, and Al electrodes</td>
<td>31</td>
</tr>
<tr>
<td>16. Transistor I-V measurement setup</td>
<td>34</td>
</tr>
<tr>
<td>17. Capacitor I-V measurement setup</td>
<td>34</td>
</tr>
<tr>
<td>18. Transistor gate current $I_g$ measurement setup</td>
<td>35</td>
</tr>
<tr>
<td>19. Transistor electron current $I_e$ measurement setup</td>
<td>35</td>
</tr>
<tr>
<td>20. Transistor hole current $I_p$ measurement setup</td>
<td>36</td>
</tr>
<tr>
<td>FIGURE</td>
<td>Title</td>
</tr>
<tr>
<td>--------</td>
<td>----------------------------------------------------------------------</td>
</tr>
<tr>
<td>21.</td>
<td>Schematic diagram of high-frequency C-V circuit</td>
</tr>
<tr>
<td>22.</td>
<td>Quasi-Static C-V measurement setup</td>
</tr>
<tr>
<td>23.</td>
<td>Gate current ( I_g ) measurement setup under constant voltage stress</td>
</tr>
<tr>
<td>24.</td>
<td>Electron current ( I_n ) measurement setup under constant voltage stress</td>
</tr>
<tr>
<td>25.</td>
<td>Hole current ( I_p ) measurement setup under constant voltage stress</td>
</tr>
<tr>
<td>26.</td>
<td>Constant voltage stress for capacitor</td>
</tr>
<tr>
<td>27.</td>
<td>Schematic circuit diagram for constant current stress</td>
</tr>
<tr>
<td>28.</td>
<td>Typical I-V curves for SNOS and SONOS capacitors</td>
</tr>
<tr>
<td>29.</td>
<td>Electric field distribution due to trapping of hole charge</td>
</tr>
<tr>
<td>30.</td>
<td>Trap distribution for holes – single carrier case</td>
</tr>
<tr>
<td>31.</td>
<td>Normalized hole and electron current distributions under two different ( R_{pp} ). ( R_{pp} = \frac{J}{J_{pp}}, ) ( J ) is the total current density and ( J_{pp} ) is the hole injection current density at ( \text{SiO}_2/\text{Si}_3\text{N}_4 ) interface. ( \lambda ) is the effective trapping length</td>
</tr>
<tr>
<td>32.</td>
<td>Typical electric field distribution plots for nitride layer with negligible detrapping. ( AE = E-E_0 ), where ( E_0 ) is the contact electric field at ( \text{SiO}_2/\text{Si}_3\text{N}_4 ) interface</td>
</tr>
<tr>
<td>33.</td>
<td>Typical I-V curves for ( I_n ) and ( I_p ) with two different dielectric thickness</td>
</tr>
<tr>
<td>34.</td>
<td>Typical electric field distribution for the negligible recombination case</td>
</tr>
<tr>
<td>35.</td>
<td>Typical trapped charge distributions for the negligible recombination case</td>
</tr>
</tbody>
</table>
LIST OF FIGURES (cont'd)

FIGURE | PAGE
-------|------
36. HF-CV curves for gold-gate capacitors with nitride/oxide thickness as 20/104 Å, obtained after a -100 nA gate current stress under different stress time | 87
37. Constant current stress V-t curves for gold-gate capacitor with nitride/oxide thickness of 20/295 Å | 88
38. Constant current stress V-t curves for gold-gate capacitor with nitride/oxide thickness of 20/387 Å | 88
39. Constant current stress V-t curves for gold-gate capacitor with nitride/oxide thickness of 30/99 Å | 89
40. Constant current stress V-t curves for gold-gate capacitor with nitride/oxide thickness of 20/206 Å | 89
41. HF C-V shift of gold-gate capacitors, obtained after a 20 nA constant current stress with different stress time | 92
42. HF C-V shift of aluminum-gate capacitors, obtained after a 20 nA positive constant current stress with different stress time | 94
43. HF C-V shift of N+ poly-gate capacitors, obtained after a 0.2 nA negative constant current stress with different stress time | 96
44. HF C-V shift of N+ poly-gate capacitors, obtained after a 60 nA negative constant current stress with different stress time | 96
45. Constant current stress V-t curves for N+ poly-gate capacitors | 97
46. C-V shift of N+ poly-gate capacitors with nitride dielectric under -100 μA constant current stress with different stress time | 99
47. C-V shift of N+ poly-gate capacitors with pure nitride dielectric under -40 nA constant current stress with different stress time | 99
48. Typical V-t curves of p-type N+ poly-gate SNS capacitor under negative current stress | 101
<table>
<thead>
<tr>
<th>FIGURE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>49.</td>
<td>C-V shift of N+ poly-gate capacitors with pure nitride dielectric under 100 nA gate bias</td>
</tr>
<tr>
<td>50.</td>
<td>Typical V-t curves of n-type N+ poly-gate SNS capacitor under positive current stress</td>
</tr>
<tr>
<td>51.</td>
<td>Typical turn-around curve of a poly-gate capacitor with constant voltage stress</td>
</tr>
<tr>
<td>52.</td>
<td>Schematic diagram of the electric field distribution with the two-carrier charge trapping</td>
</tr>
<tr>
<td>53.</td>
<td>Schematic diagram of the electric field distribution with hole trapping dominant</td>
</tr>
<tr>
<td>54.</td>
<td>Schematic diagram of the electric field distribution with electron trapping dominant</td>
</tr>
<tr>
<td>55.</td>
<td>I-t curves of the gold-gate capacitors with dielectric thickness of 20/206 Å under negative voltage stress</td>
</tr>
<tr>
<td>56.</td>
<td>C-V plots of gold-gate capacitors with dielectric thickness of 20/206 Å under negative 15 V stress</td>
</tr>
<tr>
<td>57.</td>
<td>C-V plots of gold-gate capacitors with dielectric thickness of 20/206 Å under negative 6 V stress</td>
</tr>
<tr>
<td>58.</td>
<td>C-V plots of N+ poly-gate capacitors with dielectric thickness of 34/303/0 Å under 25 V stress</td>
</tr>
<tr>
<td>59.</td>
<td>C-V plots of N+ poly-gate capacitors with dielectric thickness of 34/303/0 Å under -10 V stress</td>
</tr>
<tr>
<td>60.</td>
<td>Typical I-t curves of N+ poly-gate capacitors with dielectric thickness of 34/303/0 Å under negative voltage stress</td>
</tr>
<tr>
<td>61.</td>
<td>C-V plots of N+ poly-gate capacitors with n-type substrate and 0/280/130 Å dielectric thickness under 30 V stress</td>
</tr>
<tr>
<td>62.</td>
<td>I-t curves of the n-type substrate N+ poly-gate capacitors with dielectric thickness of 0/280/130 Å under 30 V stress</td>
</tr>
<tr>
<td>FIGURE</td>
<td>DESCRIPTION</td>
</tr>
<tr>
<td>--------</td>
<td>-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>63.</td>
<td>I-t curves of the p-type substrate N+ poly-gate capacitors with dielectric thickness of 150/250/0 Å under -32 V stress</td>
</tr>
<tr>
<td>64.</td>
<td>I-t curves of the p-type substrate N+ poly-gate capacitors with dielectric thickness of 150/250/0 Å under 32 V stress</td>
</tr>
<tr>
<td>65.</td>
<td>C-V plots of n-type substrate N+ poly-gate capacitors with dielectric thickness of 0/280/0 Å, taken after stress for 5000 seconds under different positive current stress</td>
</tr>
<tr>
<td>66.</td>
<td>C-V plots of n-type substrate N+ poly-gate capacitors with dielectric thickness of 0/280/0 Å, taken after stress for 5000 seconds under different negative current stress</td>
</tr>
<tr>
<td>67.</td>
<td>C-V plots of p-type substrate N+ poly-gate capacitors with dielectric thickness of 34/303/0 Å, taken after stress for 5000 seconds under different negative current stress</td>
</tr>
<tr>
<td>68.</td>
<td>C-V plots of p-type substrate N+ poly-gate capacitors with dielectric thickness of 34/303/0 Å, taken after stress for 5000 seconds under different negative voltage stress</td>
</tr>
<tr>
<td>69.</td>
<td>Poole-Frenkel plots of I-V curves for p-channel SNS capacitors under both biasing polarities</td>
</tr>
<tr>
<td>70.</td>
<td>Poole-Frenkel plots of I-V curves for n-channel SNS capacitors under both biasing polarities</td>
</tr>
<tr>
<td>71.</td>
<td>Modified P-F plot for a n-channel SNS capacitor under negative bias</td>
</tr>
<tr>
<td>72.</td>
<td>Typical I-t curves of the SNS capacitors under negative bias</td>
</tr>
<tr>
<td>73.</td>
<td>$V_{PB}$-t curves transformed from the I-t curves shown in Fig. 72</td>
</tr>
<tr>
<td>74.</td>
<td>Effective charge calculated from the I-t data shown in Fig. 72</td>
</tr>
</tbody>
</table>
### LIST OF FIGURES (cont'd)

**FIGURE** | **PAGE**
---|---
75. Typical C-V shifts of gold-gate MNOS capacitors with dielectric thickness O/N of 20/100 Å, obtained after constant current stress for 600 seconds | 131
76. Typical C-V shifts of gold-gate MNOS capacitors with O/N of 20/200 Å, obtained after constant current stress for 600 seconds | 131
77. Typical C-V shifts of gold-gate MNOS capacitors with O/N of 20/300 Å, obtained after constant current stress for 600 seconds | 132
78. Typical C-V shifts of gold-gate MNOS capacitors with O/N of 20/400 Å, obtained after constant current stress for 600 seconds | 132
79. V-t curves for gold-gate MNOS capacitors with O/N of 20/100 Å | 133
80. V-t curves for gold-gate MNOS capacitors with O/N of 20/200 Å | 133
81. V-t curves for gold-gate MNOS capacitors with O/N of 20/300 Å | 134
82. V-t curves for gold-gate MNOS capacitors with O/N of 20/400 Å | 134
83. Flat-band voltage shifts recorded after different current stressing | 136
84. Flat-band voltage shifts versus nitride thickness | 137
85. Analytical solutions of the flat-band voltage shift versus different nitride thickness | 140
86. Analytical solutions of the flat-band voltage shift versus different nitride thickness with higher $r_p$ | 142
87. Analytical solutions of the flat-band voltage shift for gold-gate MNOS capacitors | 143
88. Typical I-t curves of gold-gate MNOS capacitors under negative voltage stress | 145
LIST OF FIGURES (cont'd)

<table>
<thead>
<tr>
<th>FIGURE</th>
<th>DESCRIPTION</th>
<th>PAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>89.</td>
<td>Typical turnaround curve</td>
<td>146</td>
</tr>
<tr>
<td>90.</td>
<td>Typical two-turnaround curve</td>
<td>147</td>
</tr>
<tr>
<td>91.</td>
<td>Energy band diagram and possible electron injection path</td>
<td>150</td>
</tr>
<tr>
<td>92.</td>
<td>Typical I-V plot of N+ poly-gate SONOS FET with variable reverse bias at substrate</td>
<td>153</td>
</tr>
<tr>
<td>93.</td>
<td>Typical I-V plot of N+ poly-gate SNOS FET with variable reverse bias at substrate</td>
<td>153</td>
</tr>
<tr>
<td>94.</td>
<td>Energy band diagram of MNOS devices under positive bias</td>
<td>154</td>
</tr>
<tr>
<td>95.</td>
<td>Energy band diagram of MNOS devices under negative bias</td>
<td>156</td>
</tr>
<tr>
<td>96.</td>
<td>Energy band diagram of N+ poly-gate devices under positive bias</td>
<td>158</td>
</tr>
<tr>
<td>97.</td>
<td>Energy band diagram of N+ poly-gate devices under negative bias</td>
<td>160</td>
</tr>
<tr>
<td>98.</td>
<td>I-V curves of n-channel poly-gate SNS transistors under both positive and negative gate bias</td>
<td>162</td>
</tr>
<tr>
<td>99.</td>
<td>I-V curves of p-channel poly-gate SNS transistors under both positive and negative gate bias</td>
<td>163</td>
</tr>
<tr>
<td>100.</td>
<td>Typical transistor I-t curves of $I_g$, $I_n$, and $I_p$ recorded during negative 18 V stress</td>
<td>167</td>
</tr>
<tr>
<td>101.</td>
<td>Typical transistor I-t curves of $I_g$, $I_n$, and $I_p$ recorded during negative 22.5 V stress</td>
<td>168</td>
</tr>
<tr>
<td>102.</td>
<td>Typical transistor I-t curves of $I_g$, $I_n$, and $I_p$ recorded during positive 18 V stress</td>
<td>169</td>
</tr>
<tr>
<td>103.</td>
<td>Current distribution of p-channel test transistor circuit</td>
<td>170</td>
</tr>
<tr>
<td>104.</td>
<td>SEM micrograph of the cross section of a gold-gate MNOS capacitor</td>
<td>173</td>
</tr>
<tr>
<td>FIGURE</td>
<td>Description</td>
<td>PAGE</td>
</tr>
<tr>
<td>--------</td>
<td>-------------</td>
<td>------</td>
</tr>
<tr>
<td>105.</td>
<td>Bubble formation at the surface of a gold-gate MNOS device</td>
<td>173</td>
</tr>
<tr>
<td>106.</td>
<td>TEM micrograph of the cross section of a gold-gate MNOS capacitor</td>
<td>174</td>
</tr>
<tr>
<td>107.</td>
<td>I-t curves showing typical two-step breakdown of a gold-gate MNOS capacitor</td>
<td>178</td>
</tr>
<tr>
<td>108.</td>
<td>V-t curves showing typical two-step breakdown of a gold-gate MNOS capacitor</td>
<td>178</td>
</tr>
<tr>
<td>109.</td>
<td>I-t curves showing typical two-step breakdown of both gold- and aluminum-gate MNOS capacitors</td>
<td>179</td>
</tr>
</tbody>
</table>
Chapter 1

Introduction

To provide high performance and high circuit density, selection of the dielectric material has always been an important issue for modern VLSI circuit design. Silicon nitride was selected because of its ability to provide a good impurity diffusion barrier [1]-[3], high dielectric constant [4], [5], low defect density [6], high oxidation selectivity over silicon in the local-oxidation isolation (LOCOS) process [7], high dielectric strength [6], high storage capacitance [8], and good isolation properties [9].

Applications [10] of thin nitride films include anti-reflection coatings for solar cell, gettering of microdefects, alkali-metal ion barriers, microelectronics circuit encapsulation and, most importantly, storing charge in memory devices. Employment of semiconductor memories for data storage in computers was initiated in 1969, soon after the invention of the floating-gate nonvolatile semiconductor memory [11] and the MIOS memory [12]. Compared to magnetic memories, semiconductor memories have the merits of fast speed, large density, low cost, small power consumption, and easy interface with semiconductor logic circuitry. When compared with magnetic memories, these features lead to preference of semiconductor over magnetic memories [13]. Transition from magnetic memories to semiconductor memories became more pronounced
after the improvement of chemical vapor deposition (CVD) techniques. In recent years, the low-pressure CVD (LPCVD) nitride has been extensively used in many areas, such as the dielectric layer in the MONOS storage cell of dynamic random-access-memories (DRAM's) [14], the dielectric layer in the MNOS dual-dielectric non-volatile memory devices [15], and the inter-poly-silicon coupling and insulating layer in floating-gate non-volatile memories of EPROM's and EEPROM's [16].

Early in the exploration of silicon nitride films in MIS systems, it was found that they exhibited a charge storage property and a substantial effort has been devoted to measuring and explaining this phenomena. Since the stored quantity consists of charge in the dielectric of memory devices, the switching characteristics deal with the amount of charge stored; hence, study of the switching time of memory devices in terms of the charge transport mechanisms at the gate dielectric of the memory device becomes an important issue in understanding the charge storage operation. Various models have been put forth to explain the charge transport mechanism. The early investigators in this area included Ross et al. [17], Pao and O'Connell [18], Sewell et al. [19], Wallmark and Scott [20], Lenzlinger and Frohmann-Bentchkovsky [21], and Kendall [22].

Although attempts have been made in the past to characterize nitride transport properties and the understanding of nitride dielectrics has made considerable progress recently, knowledge about the nature and behavior of the carrier transport and charge trapping of nitride has not yet reached the level obtained for silicon dioxide.
Among properties of the nitride layer, the carrier type and the charge trapping mechanism are two of the most important issues in understanding the read-write-erase and fatigue characteristics of MNOS devices. Since the charge storage effects in MNOS devices are caused by charge capture in traps distributed over the oxide/nitride interface as well as within the nitride bulk [23], [24], with the continuing reduction of layer thickness applied in electronic device structures, charge trapping by the nitride has an increasing influence on the ultimate performance of integrated circuits. From thermally stimulated current (TSC) measurements on silicon nitride, Kendall [22] found that a complex energetic and spatial trap distribution exists in these films. The trapping and detrapping processes that occur during the charge transport through the nitride might involve all of the impurity trap levels, which complicates the charge transport kinetics inside the nitride films. Meanwhile, existence of different carrier types causes different switching speed, retentivity, and endurance. To understand charge transport in nitride films, it is therefore essential to have a wide knowledge of the carrier type and the trap properties as well as of the charge transport mechanism.

Before 1975, electrons were considered to be the majority carrier concentration inside the nitride layer. The first person to address the issue of the carrier transport mechanism and carrier type in nitride is Sze [25]. From I-V experiments, Sze discovered that the transport mechanism in nitride films was bulk controlled instead of being controlled by the electrodes. Sze concluded that the conduction current inside nitride films is mainly due to field-enhanced thermal excitation
of trapped electrons from the impurity trap level to the conduction band and can be divided into three terms: a component due to the Poole-Frenkel mechanism, a component due to field ionization of trapped electrons, and a contribution caused by thermal hopping of excited electrons. Sze also found that the current transport depends little on the substrate material, the film thickness, or the polarity of the electrode. Frohman-Bentchkowsky and Lenzlinger [21], assuming electron flow, predicted the charge accumulation at the dielectric interface of the MNOS structure; and they concluded that the accumulated interface charges depend on temperature, oxide thickness, dielectric current-field characteristics, and charging time. From measurements of charge injection and propagation of charge in the nitride films of an MNOS structure caused by a pulsed electric field, Yun [26] concluded that the spatial distribution of the trapped electrons are not limited near the oxide/nitride interface as the trapped electrons actually extend in depth into the nitride film. A two-band Si$_3$N$_4$ conduction model proposed by Ginovker [27] was the first attempt to determine the hole and electron components of stationary current in the dual-dielectric MNOS structure. He found that the basic current component at the Si-SiO$_2$ interface in thin oxide MNOS structures is associated with carriers flowing from the semiconductor to the dielectric, while in thick oxide MNOS structures the basic component of the Si-SiO$_2$ interface current is due to injection from the dielectric into the silicon.

In the charge centroid measurement by Yun [28], he assumed that the injection from the gate electrode is negligible, so that the hole and electron charge centroid can be determined from the negative and
positive bias respectively. Based on the experimental data, he claimed that holes are more mobile than electrons in chemically vapor deposited Si$_3$N$_4$, and that the hole traps are likely to be shallower than the electron traps, resulting in enlarged hole conduction in the silicon nitride. Large hole conduction is also found for both polarities in Weinberg and Pollak's [29] current transport measurement, in which the carrier injection was from low-energy corona ions and a shallow junction diode detector. The two-carrier model of three trap levels given by Svensson [30] is the first attempt to theoretically take into account the role of hole conduction in silicon nitride films. In the current conduction at the dielectric layer of MNOS devices Schroder, White [31], and Suzuki [32]–[33] concluded that hole flow dominates under both gate polarities, in contrast to the conclusion made by Watanabe and Wakayama [34] that electron flow dominates under positive gate voltage and hole flow dominates under negative bias.

While the dominance of hole conduction under negative voltage stress in MNS is generally accepted [31], [32], [34], [35], there are still some discrepancies between the charge carriers in the nitride of MNS structures under positive gate polarity and charge carriers in the nitride of MNOS structures under positive and negative gate polarities as well. In the study of charge flow in poly-silicon/top-oxide/nitride/bottom-oxide/silicon (SONOS) structures, Liou and Chen [36] claimed that the dominant charge carriers flowing across the top and bottom oxide are different: conduction through the bottom oxide is dominated by electron flow while conduction through the top oxide and nitride is dominated by hole flow for positive gate voltage. Yau [37] argued that
since most of the literature used Ginovker's [27] measurement method to determine carrier type and the hole and electron currents measured are located in the silicon substrate - not in the nitride, the species conducted in the nitride do not necessarily correlate to the holes or electrons transported through the silicon. By using the same method but with three different structures, Yau concluded that electrons dominate the conduction process in nitrides of HNS and MNOS for both gate polarities.

In the study of charge trapping phenomena of nitride films, most people use a single-carrier model in analyzing trapping properties. However, as different carrier types have been used, the capture cross section, trap level, mean free path, effective mass, and mobility of electrons and holes are totally different. Several researchers have tried to determine the carrier type and the charge centroid from the flat-band voltage shift, but they did not investigate further the distribution of the stored charges. It is well known that a good memory device should be able to operate at fast speed, low writing-erasing voltage, and long retentivity of stored data, but all of these traits rely upon the high quality and good performance of the dielectric layer. To optimize the nitride properties, such as the trapping efficiency, switching time, and leakage current, or to change the nitride dielectric fabrication processes, a clear understanding of the carrier type as well as of the trap distributions is extremely critical.

In modern VLSI circuit design, applied voltages are scaled down less than device dimensions; hence, the devices are usually operated under high field stress which can substantially degrade the performance
of the device. When the gate dielectric of memory devices are electrically stressed, charge trapping occurs in the silicon/dioxide, oxide/nitride or silicon/nitride interfaces and dielectric bulk. This trapped charge will cause a significant change of the electric field inside the nitride bulk. Such phenomena were anticipated to be directly related to the breakdown event [38]. Although there is still no well-developed breakdown model for the nitride layer, commonly cited breakdown mechanisms for SiO₂ like a critical charge model [39] and an impact ionization model [40] can be used to explain the nitride breakdown as well. It is believed that under lower applied fields the charge trapping will increase the localized electric field and, once the field is higher than a certain critical value, current multiplication will eventually lead to breakdown. Under high applied fields the charge carrier concentration inside the nitride increases due to carrier multiplication by impact ionization. If the applied field is higher than some field value, each carrier produces on the average more than one additional carrier and the current then increases without limit. In either case the conduction current and trapped charge play an important role in the dielectric breakdown.

The purpose of this research is to investigate the carrier type, trap distribution, as well as the kinetics of the charge transport in thin Si₃N₄ films and the nitride breakdown mechanism. Our primary interest is the study of these phenomena in the presence of DC voltage and DC current stress.

This dissertation presents many experimental results including I-t, V-t, and C-V curves with constant current stress and constant
voltage stress. New breakdown phenomena and characteristics of Si$_3$N$_4$ films have been discovered from these electrical tests. A steady-state two-carrier charge transport model in the nitride layer has been developed. This model gives a detailed description of the trapped electron and hole spatial distribution as well as the peak electric field distribution responsible for excess current and damage formation. The trap distribution and the kinetics of charge transport inside the nitride will be discussed, based on the experimental and calculated results in the model.

This dissertation is organized as follows. Chapter II summarizes the fabrication processes of all the devices utilized in our study. Chapter III introduces the experimental setup and the measurement methods that were developed. Chapter IV presents kinetics of the proposed two-carrier charge transport model, which includes the charge trap distribution as well as the electric field distribution. The numerical solution of the equations comprising the model will also be described. Chapter V covers the experimental results and the analytical solutions that were obtained. Chapter VI gives a thorough investigation of two-carrier charge transport in MNOS devices and is followed by a two-step breakdown model, which is related with the oxide and nitride dielectric breakdown mechanisms. The conclusions presented in Chapter VII highlight important aspects of the work and possible areas for future study are proposed.
Chapter 2

Device Fabrication

In this study of charge transport kinetics in LPCVD nitride layers, our interest concentrates on thin dielectrics. However, in addition to the effect produced by dielectric thickness variation, different gate materials or different kinds of channel type at the silicon surface also will change the carrier injection conditions. Therefore, several kinds of devices have been utilized in our study to investigate all of the injection possibilities. The devices employed have single dielectric (N), dual dielectric (NO), and triple dielectric (ONO) gate structures. Different gate materials such as aluminum, gold, and N+ polysilicon are utilized. The transistors utilized are both p- and n-channel poly-gate FETs.

2.1 Al-gate and Au-gate Capacitors

Devices were fabricated on 4 inch p-type silicon wafers with <100> orientation and have resistivities varying from 14 Ohm-cm to 21 Ohm-cm. Wafers were initially cleaned with standard chemical cleaning procedures. Next, the wafers were oxidized in nitrogen-diluted dry oxygen to grow a tunnel oxide layer of 20 or 30 Å thickness. Then, silicon nitride films of various thickness (Table 1) were deposited at 750 °C by a conventional low-pressure chemical-vapor-deposition (LPCVD) method. In this process the ratio of ammonia (NH₃) to dichlorosilane
<table>
<thead>
<tr>
<th>Wafer #</th>
<th>Oxide (Å)</th>
<th>Nitride (Å)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>103</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>181</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>295</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>399</td>
</tr>
<tr>
<td>5</td>
<td>20</td>
<td>104</td>
</tr>
<tr>
<td>6</td>
<td>20</td>
<td>206</td>
</tr>
<tr>
<td>7</td>
<td>20</td>
<td>295</td>
</tr>
<tr>
<td>8</td>
<td>20</td>
<td>387</td>
</tr>
<tr>
<td>9</td>
<td>30</td>
<td>99</td>
</tr>
<tr>
<td>10</td>
<td>30</td>
<td>199</td>
</tr>
<tr>
<td>11</td>
<td>30</td>
<td>292</td>
</tr>
<tr>
<td>12</td>
<td>30</td>
<td>394</td>
</tr>
</tbody>
</table>
The chemical equation for this reaction is

\[ 4 \text{NH}_3 + 3 \text{SiH}_2\text{Cl}_2 \rightarrow \text{Si}_3\text{N}_4 + 6 \text{HCl} + 6 \text{H}_2 \]

The back nitride was then removed by using a 49% hydrofluoric acid (HF) for the back ohmic contact formation. Both aluminum and gold were used for the gate metal evaporation. To avoid metal spiking in the insulator, no annealing was performed. After photolithography and metal etching processes for defining the capacitor pattern, the back of the substrate was also covered with aluminum by vacuum evaporation to reduce parasitic resistance and capacitance. The final capacitor patterns have circular shapes and diameters of 395 to 400 μm. The gate metal thickness ranges from 3000 Å to 3500 Å (Fig. 1). All dimensions were measured using a Sloan Dektak IIa surface profilometer.

2.2 SONOS and SNOS Capacitor and Transistor

2.2.1 LOCOS Process

The n-channel transistors and MIS capacitors with N+ poly/top-oxide/nitride/pad-oxid/silicon-substrate/back-contact were fabricated on p-type <100> oriented silicon wafers. The substrates have thicknesses ranging from 24.01 to 25.19 mils and resistivities ranging from 7 to 12.5 Ohm-cm.

The conventional LOCOS process was adopted in fabricating these MIS structures. The starting wafers were five-inch in diameter. A 30 Å layer of starting oxide was grown first, followed by another 30 Å of thermal nitride. Then, 250 Å of the nitride was deposited by the LPCVD technique. The isolation pattern was then defined by photolithography
(a) Metal gate (3000 Å)
(b) LPCVD nitride (100-400 Å)
(c) Thin pad oxide (20-30 Å)
(d) Silicon substrate (500 μm)
(e) Aluminum back contact (4000 Å)

Figure 1. Cross section of a MNOS capacitor
and etching processes (Fig. 2).

The thin nitride layer was etched by a special nitride etchant, a blanket boron field implant with a dose concentration of \(8 \times 10^{12} \text{ cm}^{-2}\) at 30 keV was implanted to compensate the surface concentration change due to surface migration during the field-oxide growth (Fig. 3). In the oxidation cycle, since nitride itself is highly impervious to oxygen, the silicon underneath the nitride is not affected by the oxidation. However, at the edges of the nitride layer, lateral diffusion of oxygen produces a tapered oxide which resembled a bird's beak \[41\]. This effect is not desirable because the bird's beak takes up lateral space. To reduce the bird's beak, first a 1000 Å oxide was grown in dry oxygen with 3% HCl atmosphere, followed by 6500 Å field oxide grown in steam to form a total of 7500 Å field oxide (Fig. 4).

The final step of the LOCOS process was a threshold voltage \(V_T\) adjust implant. Nitride was first etched, followed by growth of a 400 Å oxide layer at 920 °C. This extra step protects the silicon surface. Since films deposited directly on bulk silicon tend to cause damage sites, sacrificial oxidation was used to remove those defects on the surface and also was used as a protection layer. The blanket threshold voltage \(V_T\) adjust implant, using Arsenic with a dose concentration of \(5 \times 10^{12} \text{ cm}^{-2}\), was then implanted at the defined region (Fig. 5).

### 2.2.2 ONO and NO gate

After the LOCOS process, the wafers were separated into several splits in order to grow different dielectric thickness. The bottom pad oxide was first thermally grown in a dry oxygen ambient at 775 °C. A
Figure 2. Define isolation region

Figure 3. Blanket field implant
Figure 4. Field oxide growth

Figure 5. Threshold voltage adjustment implant
LPCVD nitride film with NH_{3} to SiH_{2}Cl_{2} gas ratio of 20 to 1 was then deposited to the desired thickness. The top oxide growth then followed to complete the ONO structure. The wafers were oxidized in steam at 900 °C for 60 minutes by pyrogenic oxidation to obtain a 30 Å top oxide and were then annealed in a hydrogen atmosphere at 400 °C for 15 minutes. N+ polycrystalline silicon was deposited onto the top oxide to be used as the poly gate (Fig. 6). The capacitors fabricated here have an area of 107.1 mil^2 (256.5 μm * 269.2 μm). The final thickness of the various dielectrics are listed in Table 2. The isolation pattern for the source and drain areas was then defined by photolithography and etching processes (Fig. 7).

Before the source and drain (S/D) implant, a 600 Å sacrificial poly oxide was grown on doped polysilicon. The reason for this extra process is to protect the silicon surface so that films deposited on bulk silicon will not cause damage sites. Arsenic with dose concentration of 1x10^{16} cm^{-2} was then implanted at 80 keV to form the drain and source of the n-channel transistor (Fig. 8). The N+ poly-gate transistor has a channel width to length ratio of 50 μm to 50 μm.

2.2.3 Passivation, Contact, and Metallization

Following the arsenic implant was a phosphorus-silica-glass (PSG) passivation processes which forms a 8000 Å passivation layer on top of the MIS structures, as shown in Fig. 9. The contact patterns were then defined with a partially wet etch followed by a dry etch process. With this two-step etching process, the window opened can be limited to within an acceptable range. To ensure a good ohmic contact at the
Figure 6. ONO deposition

Figure 7. Isolation for S/D diffusion
Table 2  Split information of N-channel devices

<table>
<thead>
<tr>
<th>WAFER #</th>
<th>PAD OXIDE(Å)</th>
<th>NITRIDE(Å)</th>
<th>TOP OXIDE(Å)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-6</td>
<td>34</td>
<td>108</td>
<td>0</td>
</tr>
<tr>
<td>7-12</td>
<td>34</td>
<td>108</td>
<td>30</td>
</tr>
<tr>
<td>13-18</td>
<td>34</td>
<td>303</td>
<td>0</td>
</tr>
<tr>
<td>19-24</td>
<td>34</td>
<td>303</td>
<td>30</td>
</tr>
<tr>
<td>25-30</td>
<td>66</td>
<td>402</td>
<td>0</td>
</tr>
<tr>
<td>31-36</td>
<td>66</td>
<td>402</td>
<td>30</td>
</tr>
<tr>
<td>37-42</td>
<td>66</td>
<td>416</td>
<td>0</td>
</tr>
<tr>
<td>43-48</td>
<td>66</td>
<td>416</td>
<td>30</td>
</tr>
</tbody>
</table>
Figure 8. S/D implant

Figure 9. Passivation and contact holes
substrate, the back surfaces of the wafers were implanted with boron at a dose concentration of $2 \times 10^{15}$ cm$^{-2}$ at 35 keV.

The front surface was then deposited with aluminum to a thickness of nearly 7700 Å. After completion of the metalization of the surface contact, the back of the substrate was coated with another layer of aluminum to ensure a good ohmic contact to the substrate. The annealing process then was done at 450 °C in a forming gas atmosphere (5% hydrogen and 95% nitrogen) for 30 minutes. The cross section of the final transistor pattern is shown in Fig. 10. The final top view of the transistor is shown in Fig. 11, and the final pattern of the capacitor is shown in Fig. 12.

2.3 Dual-Channel Transistors

In the standard CMOS process n-channel devices are placed inside a diffused p-well region embedded within a n-type substrate. However, in order to lower the substrate bias effect of the threshold voltage and parasitic capacitance of drain/source in both n- and p-channel transistors, a n-well CMOS technology seems to be more promising [42]. The devices fabricated for our study use the twin-tub-well CMOS technology. The n- and p-channel devices were fabricated at the same time inside the p- and n-well respectively. With this twin-tub CMOS technology secondary effects that commonly cause the failure of the CMOS devices, such as the latch-up problem, can be significantly improved [43].

The initial substrate was 4 inch p-type silicon wafer with <100> orientation and having a resistivity of 30 to 50 Ohm-cm. A p-type
Figure 10. Metalization
Figure 11. Top view of the n-channel transistor

Figure 12. Top view of the poly-gate capacitor
epitaxial layer of about 4 μm thickness was grown on top of this heavily-doped p-type substrate to reduce the effective substrate resistance [44].

The n-well region was first defined by growing a starting oxide and nitride layer followed by the photolithography process. Phosphorus ions were then implanted onto the silicon substrate at 70 keV. A 5000 Å layer of blocking oxide was then grown on the n-well area. Boron ions were implanted into the field region outside of the n-well at 50 keV with a dose concentration of 8x10^{12} cm^{-2}. A drive-in of both wells was performed at 1150 °C in a nitrogen atmosphere.

After thermal growth of silicon dioxide all over the substrate, a 30 Å of thermal nitride was grown followed by a 250 Å LPCVD nitride deposition, and a nitride layer was then selectively etched to define the diffusion pattern. In fact, all thin films and dielectrics were etched during the fabrication processes in parallel-plate plasma reactors to reduce lateral undercuts.

The following steps are the same as the LOCOS process described in Section 2.2. First, a bottom pad oxide was thermally grown, then the nitride layer was grown by LPCVD at 800 °C with an ammonia to dicholosilane gas ratio of 10:1, and finally the top oxide was thermally grown at 900 °C in dry oxygen atmosphere. The dual-dielectric gate p- and n-channel transistors were fabricated using standard CMOS processes. Arsenic ions were implanted at 50 keV with a dose concentration of 4x10^{15} cm^{-2} to form the source and drain of the n-channel devices. The BF_{2} ions were implanted at 50 keV with a dose concentration of 4x10^{15} cm^{-2} to form the source and drain of the p-channel devices. The
back of the substrate had been implanted with a boron dose. A gold evaporation was also done in order to form a good ohmic contact to the substrate. After completing the fabrication processes, the surface concentration of the n well is about $1 \times 10^{17}$ cm$^{-2}$. The diffusion junction breakdown voltages are all larger than 15 volts. The leakage current is approximately 1 pA. The channel length and width is 50 μm by 50 μm. A summary of the devices is shown in Table 3, and the final pattern is shown in Fig. 13.

All capacitor and transistor structures described above are fabricated in the industry [45].
Table 3. Dielectric gate thickness of CMOS devices

<table>
<thead>
<tr>
<th>WAFER #</th>
<th>CHANNEL TYPE</th>
<th>PAD OXIDE (Å)</th>
<th>NITRIDE (Å)</th>
<th>TOP OXIDE (Å)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>N</td>
<td>100</td>
<td>250</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>P</td>
<td>100</td>
<td>250</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>N</td>
<td>0</td>
<td>280</td>
<td>130</td>
</tr>
<tr>
<td></td>
<td>P</td>
<td>0</td>
<td>300</td>
<td>130</td>
</tr>
<tr>
<td>3</td>
<td>N</td>
<td>0</td>
<td>280</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>P</td>
<td>0</td>
<td>280</td>
<td>0</td>
</tr>
</tbody>
</table>

Figure 13. Cross section of the twin-tub dual-channel device
Chapter 3

Experimental Methodology

An experimental system was constructed to study different physical properties of the dielectrics, such as high frequency C-V curves, quasi-static C-V characteristics, current-voltage I-V relationships, leakage currents, and transient responses. A description of this system and its characteristics were previously covered by Chang [46]. Therefore, in this chapter we will emphasize only the characteristics of newly added equipment and give a brief descriptions of the system performance.

3.1 Experimental Apparatus

Figure 14 shows the complete experimental arrangement. This data acquisition system has been found satisfactory for most of the experiments. The apparatus can be divided into three sections: probe station, testing instruments and minicomputer. The wafer probe is placed inside a well-shielded aluminum box to minimize light or other kinds of electromagnetic noise. Two triax-to-coax adapters are mounted on one side of the box. Through this adaptor, the probe can be connected to the low-leakage triaxial cable used by the HP 4140B pico-ammeter and the Keithley 617 electrometer. Very small currents can be measured without difficulty through the triax-coax cable circuit with careful electrical shielding. Next to the triax-to-coax adapters are a row of six BNC connectors to provide connections between the probe and the circuit...
Figure 14. Complete experimental arrangement
outside the shielded aluminum box. The wafer probe, made by Wentworth Labs, is equipped with a Nikon optical microscope, a Nikon lightsource, and a vacuum chuck with x-y control. The probe as well as the vacuum chuck are electrically isolated from the probe base. However, due to the potential difference between the vacuum chuck and the probe base during measurement, the poor isolation material between them create a small leakage current on the order of 10 fA. Inside the aluminum box the probe station is equipped with a nitrogen flow nozzle, use of which prevents the leakage paths created by the accumulation of moisture at the wafer surface. During measurement the box is grounded through the cable connection between the wall of the box and the measuring instruments.

The testing instruments utilized for this dielectric charge transport study include: a Keithley 225 current source, a Keithley 195 system digital multimeter, a Keithley 192 programmable DMM, a Keithley 642 Electrometer, a Keithley 617 programmable electrometer/source, a HP 4140B pA meter/DC voltage source, a HP 4275A multifrequency LCR meter, and a HP 4145 semiconductor parameter analyzer. The Keithley 225 can supply DC current from 100 pA to 99 mA with both polarities. A voltage compliance control allows the output voltage to be ranged from 10 to 100 volts. Modification was done to allow output voltage measurement of the current source with the Keithley 192 digital multimeter. Since the smallest current source is 0.2 nA, any constant current stress less than 0.2 nA can not be furnished with this current source. The Keithley 192 is a six and one-half digit fast autoranging DMM with 100 nV DC sensitivity and its input resistance is greater than 1 G-ohm. The Keithley
195 is a highly sensitive electrometer, which can detect currents and voltages as small as 100 pA and 100 nV. The Keithley 642 is a direct-reading MOSFET-based electrometer for sensitive measurement of current, voltage, and charge. The currents measured vary between 10 aA and 200 mA with a voltage burden typically less than 1 mV. The Keithley 617 is a sensitive, versatile instrument. The full autoranging capability of this meter provides a wide range of current measurement from 100 aA to 20 mA [47]. The HP 4140B consists of an extremely stable pA meter and two programmable DC voltage sources, one of which operates as a ramp and staircase generator and as a DC source. The HP 4275A is equipped with multi-spot frequencies so that complex impedances of semiconductor or dielectric materials can be measured. These can then be transferred into the equivalent R, L, and C circuit elements. The HP 4145, the semiconductor parameter analyzer, is a fully automatic, high performance, self programmable test instrument. It consists of four programmable stimulus/measurement units. Each can be independently programmed to function either as a voltage-source/current-monitor or a current-source/voltage-monitor. Indeed, they are capable of high resolution sourcing and sensing of a wide range of currents and voltages from 1 pA to 100 mA and 1 mV to 100 V.

Data acquisition is controlled by the Digital PDP-11/03-L minicomputer. The test instruments are connected to the minicomputer through the IEEE-488 GPIB buses. A HP 7225 graphics plotter and an Apple Imagewriter printer are connected to the series port of the PDP-11 through the RS-232C bus. A Tektronix 611 storage display unit and a Digital Decwriter II are also connected to the PDP-11 for data checking,
plotting, and printing.

Many experimental techniques [35] of examining the trapping phenomena inside the dielectric have been investigated by various researchers [22], [26]-[29], [48]-[54]. These techniques include:

1) Flat-band C-V measurement to find the magnitude and polarity of trapped charge in the insulator.

2) Carrier-type measurement to determine the contribution of electron current to the total insulator conduction current at the silicon interface.

3) Dark current measurement to indicate the relative importance of interface and bulk conduction mechanism.

4) Internal photoemission to measure the interface barriers and to find the energy band diagram (Fig. 15).

5) Charge-centroid measurement to indicate charge movement in the nitride bulk during the initial buildup of trapped space charge.

Our major experiments involve the study of the charge transport kinetics in the MNOS nonvolatile memory devices due to the carrier flow through the thin nitride layer. The MOS devices have an oxide thickness of about 700 Å, so that carriers can not easily pass through the oxide layer. For the thin pad oxide MNOS devices, however, the trapped charge at the silicon/oxide, oxide/nitride interfaces, and pad oxide bulk can easily tunnel to the nitride layer. Hence, in this experiment we do not intend to characterize the surface-state parameters, although there are several methods [55]-[62] of finding the interface charge $D_{it}$ for the MOS structure. These methods can be applied to thick oxide MNOS
Figure 15. Energy band diagram of MONOS and SONOS structure with poly-Si, Au, and Al electrodes
devices, but do not apply to thin oxide MNOS devices. In conclusion, the methods used in our experiments involving charge trapping and carrier flow are:

1. Step voltage-current I-V measurement.
2. High frequency (HF) and quasi-static (QS) C-V measurements.
3. Constant voltage stress I-t measurement.
4. Constant current stress V-t measurement.

I-V measurement is only suitable in the case of the low-trap samples in which current can immediately reach a quasi-static state. C-V measurement is convenient for measuring the trapped charge and memory window closing. However, if we are only concerned about the carrier transport, the best method would be the constant voltage stress (I-t) and constant current stress (V-t) measurements. Since our primary interest is in the carrier type and trapping mechanism, we will explain the I-t and V-t experimental techniques in detail, while a description of the I-V and C-V methods can be found in references [27] and [35].

3.2 I-V measurement

In the study of two-carrier charge transport of N, NO, and ONO structures, a source of minority carriers is usually required for minority carrier injection. In our study of charge transport kinetics in the nitride layer, both p- and n-channel MIS transistors with poly-gate/oxide/nitride/oxide/silicon or poly-gate/nitride/oxide/silicon as well as poly-gate/nitride/silicon structures were used as tools for separating electron and hole tunneling currents in ultra-thin ONO, NO, and N films.
The technique of separating the electron and hole currents was first proposed by Ginovker [27]. A negative or positive bias was applied to the gate of the devices, as shown in Fig. 16. Three electrometers were used to detect the gate, drain, and substrate currents. For a n-channel device with positive bias, hole current $I_p$ results from holes diffusing from dielectric to substrate, while electrons injected from the N+ drain region and holes lost by recombination in the dielectric are observed as $I_n$. The detailed description of the carrier flow will be discussed in Chapter 6. Also shown in Fig. 17 is the capacitor I-V measurement setup.

Because the Keithley 195 does not have a wide current range $I_p$, $I_n$, and $I_g$ of the transistors can not be recorded accurately at the same time. Instead, three separate measurement were conducted for $I_p$, $I_n$, and $I_g$ respectively as shown in Figs. 18 through 20. Although these currents were not measured at the same time, the validity of the I-V curves is justified by comparison with measurement results using the HP 4145. Also supporting this assertion is that on each wafer there were 390 dies and the devices fabricated on each die were close to each other. Since the currents were measured on devices having the same wafer, the performance of these devices should be similar to each other.

3.3 C-V measurement

C-V data are generated for each device in order to obtain some understanding of charge storage, trapping, and transport. There are two kinds of C-V measurement methods: high-frequency C-V and quasi-static C-V. The schematic diagram of the high frequency C-V circuit is shown
Figure 16. Transistor I-V measurement setup

Figure 17. Capacitor I-V measurement setup
Figure 18. Transistor gate current measurement setup

Figure 19. Electron current measurement setup
Figure 20. Hole current measurement setup
in Fig. 21. The vector voltmeter, vector ammeter, and the voltage source are built inside the HP 4275A multi-frequency LCR meter. The vector ammeter is used to detect vector current in the device under test (DUT) and the vector voltmeter is used to detect vector voltage across the DUT. The DC bias, start voltage, step voltage, step size, and step delay time of the voltage sweep are controlled by the PDP-11 minicomputer. The quasi-static C-V measurement, in which a voltage ramp generator is used to supply a time varying gate bias, uses the relationship between the differential capacitance and the displacement current in the capacitor to measure the capacitance value. With this measurement method, a frequency of a fraction of a Hz is easily attainable. The circuit diagram of the quasi-static C-V measurement is shown in Fig. 22, in which the pico ammeter and ramp voltage source are parts of the HP 4140B pA-meter/DC voltage source.

3.4 Constant Voltage Stress I-t Measurement

Continuous stress is known to produce a variety of changes in electrical characteristics such as an increase in the interface charge density of the MOS device, a shift and closing of the memory window as mentioned in the description of the C-V measurement, and eventually, device breakdown and failure.

Constant voltage stress is done for $I_g$, $I_n$, and $I_p$ respectively. Unlike the I-V measurement as shown in Fig. 16, the voltage source $VA$ has been changed to a constant voltage source. Also, a Keithley 617 is employed as an electrometer. The circuit used for gate, drain, and substrate current measurements under constant voltage stress are shown
Figure 21. Schematic diagram of high-frequency C-V circuit

Figure 22. Quasi-static C-V measurement setup
in Figs. 23 through 25. The I-t measurement setup for capacitors is shown in Fig. 26.

In the substrate current measurement, a leakage current problem has to be taken into account. Usually the dielectric can effectively block the conduction current unless an external bias is applied to the dielectric, which causes tunneling current to pass through the dielectric. However, an additional unavoidably large leakage current could be created during device probing. When the light shines on the wafer during the probing process, the light could generate some electron-hole pairs. This photo generation current then passes through the substrate and reaches the substrate contact and the electrometer [63]. The current recorded by the electrometer is on the order of 1 μA. Once the light is turned off, there is still a current on the order of 10 to 100 pA. A current of more than 0.1 pA can not be offset by the HP 4140B pico ammeter. Hence, in order to detect currents coming only from the gate bias, the leakage current should first be removed. Most of the leakage current can be removed by:

(1) Use of proper circuit connection to reduce the cable wire length.

(2) Connection of cable wire directly from the probe to the testing instrument without a BNC connector in between.

(3) Inspection of the electric/light shielded box carefully to be sure that the room light is turned off so that no light will penetrate the box.

(4) Isolation of the wafer chuck from the probe station.
Figure 23. Gate current $I_G$ measurement setup under constant voltage stress

Figure 24. Electron current $I_N$ measurement setup under constant voltage stress
Figure 25. Hole current $I_p$ measurement setup under constant voltage stress

Figure 26. Constant voltage stress for capacitor
(5) Waiting 20 to 30 minutes until all light generating electron-hole pairs have either been diffused or recombined before stressing.

Even with these precautions, there is still a small leakage current due to charge stored inside the triaxial cable, which was generated either in the previous test or in the probing process. Fortunately, the leakage current caused by this stored charge is very small, usually less than 0.1 pA, and can be neglected or offset.

3.5 Constant Current Stress V-t measurement

Constant current injection is one method of introducing charge into the dielectric. Unlike constant voltage stress, during constant current stress an electric field at the silicon/oxide interface is fixed and the voltage across the dielectrics layer reveals the trapping charge. The schematic circuit diagram is shown in Fig. 27. A Keithley 225 constant current source is used to provide constant current. The reading is monitored through a Keithley 195 system electrometer for large current values or through a Keithley 642 programmable electrometer for small current values. Voltage across the device is detected by a Keithley 192 programmable DMM.

There is a problem encountered in using this circuit setup. Since the Keithley 225 is not a programmable source, short rise time of the current waveform prevents turning on the power supply and recording the correct data with specified current value at the same time. In order to accurately record data during the experiment, the current level should reach the expected value when the computer starts to count the
Figure 27. Schematic circuit diagram for constant current stress
stressing time and record the data. To solve this problem, the power supply of the Keithley 225 is controlled through a "BNC short" at the output connection in the Keithley 225 front panel. Before current injection, output current is sunk by this "BNC short", which is connected to both a "BNC tee" and the probe. Current injection will start once the "BNC short" is removed. In the meantime, voltage readings versus time (V-t) are recorded by the PDP-11 through the IEEE 488 GPIB bus. As mentioned earlier, this current stress method is limited as the injection current can not be less than 0.2 nA.
Chapter 4

Steady-State Charge Transport

In Chapter 1, we mentioned that electron and hole flow both play important roles in current conduction inside the nitride dielectric. Although many researchers have contributed to the nitride study, a clear picture about the charge transport mechanism inside the nitride is still unknown. The purpose of this chapter is to present a closed form theoretical solution to the field distribution, trap distribution, and electron and hole current distributions along the nitride layer of memory devices. Certain simplifying procedures are used in the development of the theory, which will be explained in detail. Charge transport through the nitride layer can be either transient or steady state. The transient response of carrier transport in the MNOS dielectric is a complicated process, hence, detailed analysis is extremely difficult [64] if not impossible. In this chapter, we focus on the steady-state case in which both electron and hole flow participate in the carrier transport.

The dependence of the MNOS device performance on the thin oxide gate dielectric has been studied extensively [65]-[69]. The thickness of the pad oxide between the nitride and the silicon strongly affects the MNOS characteristics. If the thickness is larger than 43 Å [70], the hole flow will be effectively blocked by the oxide, but the electron
current can still tunnel through the oxide layer and reach the nitride layer. Because the number of carriers tunneling through the tunnel oxide bears an exponential relationship to the thickness, the normally ultra-thin 20 Å pad oxide used to reduce the interface traps should not be further reduced in thickness [71] to avoid large leakage current. This leakage current might penetrate the oxide interface and reach the gate electrode, causing a reliability problem. The oxide/silicon interface is actually not abrupt. In fact, it has been reported [72] that Auger measurement of MNOS devices indicates a continuous region of loose chemical composition of about 50 Å width between the silicon substrate and the nitride layer. The thin oxide actually exists as an oxynitride and never reaches stoichiometry. Therefore, many properties of the thin oxide, such as the dielectric constant or band-bending diagram are still unknown.

The ultra-thin oxide used in memory devices plays an important role in the memory function. If another oxide is placed on top of the oxide/nitride dual-dielectric layer, a detailed analysis of the reliability study would be very difficult. This type of ONO structure is used in EPROM and EEPROM devices. The top oxide layer acts as a potential barrier for carriers injected into the nitride. For values of thickness larger than 30 Å, the carrier flow can be significantly reduced. A comparison of the I-/E curves for SNOS capacitors and SONOS capacitors with 30 Å thick top oxide are shown in Fig. 28.

Interface charges provide important information to study the charge transport kinetics at individual layers of the ONO and NO systems. However, since it is impossible to locate the amount of interface
Figure 28. Typical I-V curves for SNOS and SONOS capacitors
charge stored in the silicon/pad oxide, pad oxide/nitride and nitride/ top oxide individually [73], an attempt to study the whole ONO and NO systems would be almost impossible. Nevertheless, an investigation of the charge transport mechanism of the nitride layer based on the nitride properties will help understand memory operations. Therefore, a detailed analysis such as electric field distribution, trap charge distribution, and transport current distribution for both electrons and holes inside the nitride layer will be the main theme of this chapter.

4.1 Principal Formulation

MNOS device characteristics and charge storage effects have been associated with charge capture in traps. The traps referred to are electron or hole energy levels relating impurities or defects in the nitride layer of the MNOS structures. Kapoor and Bibyk [74] reported that five well-defined levels of trap types exist in the nitride. Svensson's two-carrier conduction mechanism model [30] simplifies this picture, assuming that there are only three trap levels - one deep hole-trap level, one shallower hole-trap level and a deep electron-trap level. In our study, we believe that the shallower hole trap would be empty in steady state due to the large effective localized electric field resulting from either trapped charge or the applied field across the dielectrics. The shallow trap level effectively does not exist, since a large electric field will easily cause the detrapping of charges stored at the shallow trap level. To simplify our study, only single-trap level and two-trap level cases will be discussed in the following discussion.
The principal equations used for describing the charge transport mechanism are [46]:

[1] Continuity Equation

\[
\frac{dp}{dt} = - \frac{1}{q} \frac{dJ_p}{dx} - \frac{\sigma_p J_p (N_{pt} - p_t)}{q} + \langle e_p \rangle p_t - \frac{\sigma_p J_p (n_t + n)}{q} \tag{4.1}
\]

\[
\frac{dn}{dt} = \frac{1}{q} \frac{dJ_n}{dx} - \frac{\sigma_n J_n (N_{nt} - n_t)}{q} + \langle e_n \rangle n_t - \frac{\sigma_n J_n (p_t + p)}{q} \tag{4.2}
\]

In each equation above, the first term accounts for free-carrier flow. The second term is due to charge trapping. The third term is the charge detrapping term, and the last term is the charge loss due to recombination. In Eq. (4.1) the hole capture coefficient \( \sigma_p \) in the second term is assumed to have the same value as the recombination coefficient \( \sigma_p \) in the fourth term for the hole trap level. The same assumption is also made in Eq. (4.2), where the electron capture coefficient \( \sigma_n \) in second term is assumed to have the same value as the recombination coefficient \( \sigma_n \) in fourth term of the electron trap level. Unlike the situation in bulk silicon, the electron-hole charge pair generation is negligible in the dielectric bulk. Therefore, the generation term as well as the diffusion term are neglected in the dielectric layer charge transport equations.

[2] Trapping kinetics

\[
\frac{dp_t}{dt} = \frac{\sigma_p J_p (N_{pt} - p_t)}{q} - \langle e_p \rangle p_t - \frac{\sigma_n J_n p_t}{q} \tag{4.3}
\]
\[
\frac{dn_t}{dt} = \frac{\sigma_n J_n (N_{nt} - n_t)}{q} - \frac{\langle e_n \rangle n_t - \sigma_p J_p n_t}{q} \tag{4.4}
\]

In Eqs. (4.3) and (4.4), the trapping kinetics is assumed to be Shockley-Read-Hall (SRH) type [75], the detrapping of the filled trap is of Poole-Frenkel type [76].

[3] Poole-Frenkel Internal Emission

\[
\langle e_p \rangle = \nu_p \exp\left[-\frac{q}{kT} (\phi_{nt} - \beta/E)\right], \quad \nu_p = N_v V_{th} \sigma_p \tag{4.5}
\]

\[
\langle e_n \rangle = \nu_n \exp\left[-\frac{q}{kT} (\phi_{nt} - \beta/E)\right], \quad \nu_n = N_c V_{th} \sigma_n \tag{4.6}
\]

Equations (4.5) and (4.6) are the Poole-Frenkel emission coefficient [76] of holes and electrons respectively. \(\langle e_p \rangle\) represents the increase of the conduction holes due to field-enhanced thermal excitation of trapped holes into the valence band and \(\langle e_n \rangle\) represents the increase of the conduction electrons due to field-enhanced thermal excitation of trapped electrons into the conduction band.


\[
J_p = q\nu_p \tag{4.7}
\]

\[
J_n = q\nu_n \tag{4.8}
\]

\[
J = J_p + J_n \tag{4.9}
\]
In the conduction current inside the dielectric layer, electron and hole diffusion currents are neglected compared to drift currents caused by the high electric field across the dielectric.

[5] Poisson's Equation

\[
\frac{dE}{dx} = \frac{q}{\epsilon} (p_t + p - n_t - n) \tag{4.10}
\]

The electric field distribution can be related to the trapped charges and the free carriers by Poisson's equation, as indicated in Eq. (4.10). However, the free carrier terms can be neglected, which is reasonable under the high-field stress condition. During high-field stress, drift velocity of the free carriers reach their saturation value, which is on the order of \(1 \times 10^7\) cm/sec. With such a high velocity and small current it is reasonable to neglect the free carriers compared to the high trapped charge densities.

All quantities used in the charge transport kinetics and their units are described in Table 4.

As mentioned earlier, the analysis will concentrate only on the steady-state or the quasi steady-state case. Under such circumstances, the equations depicted above for the time-dependent case are still valid. The only change will be that the time variation terms are set to zero. Furthermore, since direct recombination is negligible, the free carrier concentrations \(n\) and \(p\) in the recombination terms of Eqs. (4.1)
Table 4 Definitions of variables and coefficients in the charge transport kinetics equations

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$p$</td>
<td>free hole density ($#/cm^3$)</td>
</tr>
<tr>
<td>$n$</td>
<td>free electron density ($#/cm^3$)</td>
</tr>
<tr>
<td>$p_t$</td>
<td>trapped hole density ($#/cm^3$)</td>
</tr>
<tr>
<td>$n_t$</td>
<td>trapped electron density ($#/cm^3$)</td>
</tr>
<tr>
<td>$N_{pt}$</td>
<td>total hole trap density ($#/cm^3$)</td>
</tr>
<tr>
<td>$N_{nt}$</td>
<td>total electron density ($#/cm^3$)</td>
</tr>
<tr>
<td>$J_p$</td>
<td>hole current density ($A/cm^2$)</td>
</tr>
<tr>
<td>$J_n$</td>
<td>electron current density ($A/cm^2$)</td>
</tr>
<tr>
<td>$J$</td>
<td>total current ($A/cm^2$)</td>
</tr>
<tr>
<td>$&lt;e_p&gt;$</td>
<td>hole emission rate from hole trap (1/sec)</td>
</tr>
<tr>
<td>$&lt;e_n&gt;$</td>
<td>electron emission rate from electron trap (1/sec)</td>
</tr>
<tr>
<td>$\varepsilon$</td>
<td>dielectric permittivity (F/cm)</td>
</tr>
<tr>
<td>$\varepsilon_n$</td>
<td>permittivity of nitride (F/cm)</td>
</tr>
<tr>
<td>$E$</td>
<td>electric field (V/cm)</td>
</tr>
<tr>
<td>$T$</td>
<td>temperature ($^\circ$K)</td>
</tr>
<tr>
<td>$\sigma_p$</td>
<td>hole trap capture cross-section ($cm^2$)</td>
</tr>
<tr>
<td>$\sigma_n$</td>
<td>electron trap capture cross-section ($cm^2$)</td>
</tr>
<tr>
<td>$q\phi_{pt}$</td>
<td>hole trap depth from the top of valence band (eV)</td>
</tr>
<tr>
<td>$q\phi_{nt}$</td>
<td>electron trap depth from the bottom of the conduction band (eV)</td>
</tr>
<tr>
<td>$\nu_p$</td>
<td>attempt-to-escape frequency of trapped holes from hole traps (1/sec)</td>
</tr>
<tr>
<td>$\nu_n$</td>
<td>attempt-to-escape frequency of trapped electrons from electron traps (1/sec)</td>
</tr>
</tbody>
</table>
Table 4 (cont'd)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>k</td>
<td>Boltzmann's constant (J/°K)</td>
</tr>
<tr>
<td>(N_v)</td>
<td>effective density of states at the edge of the valence band (cm(^{-3}))</td>
</tr>
<tr>
<td>(N_c)</td>
<td>effective density of states at the edge of the conduction band (cm(^{-3}))</td>
</tr>
<tr>
<td>(\beta)</td>
<td>Poole-Frenkel coefficient (V x cm(^{-1}))</td>
</tr>
<tr>
<td>(E_{NM})</td>
<td>peak electric field inside the nitride bulk (V/cm)</td>
</tr>
<tr>
<td>(E_{AVE})</td>
<td>average electric field across the dielectric (V/cm)</td>
</tr>
<tr>
<td>(X_{ENM})</td>
<td>location of the peak electric field inside the nitride (cm)</td>
</tr>
<tr>
<td>(Q_P)</td>
<td>total charge of trapped holes (Coul)</td>
</tr>
<tr>
<td>(Q_n)</td>
<td>total charge of trapped electrons (Coul)</td>
</tr>
<tr>
<td>(\rho_P)</td>
<td>charge densities of trapped holes (Coul/cm(^3))</td>
</tr>
<tr>
<td>(\rho_n)</td>
<td>charge densities of trapped electrons (Coul/cm(^3))</td>
</tr>
<tr>
<td>(\bar{X}_p)</td>
<td>charge centroid of trapped holes (cm)</td>
</tr>
<tr>
<td>(\bar{X}_n)</td>
<td>charge centroid of trapped electrons (cm)</td>
</tr>
</tbody>
</table>
and (4.2) can be neglected. Equations (4.1) to (4.4) become

\[ \frac{1}{q} \frac{dJ_p}{dx} + \frac{\sigma_p J_p (N_{pt} - pt)}{q} + \frac{\sigma_p J_p n_t}{q} = <e_p> p_t \]  
(4.11)

\[ \frac{1}{q} \frac{dJ_n}{dx} + \frac{\sigma_n J_n (N_{nt} - n_t)}{q} + \frac{\sigma_n J_n p_t}{q} = <e_n> n_t \]  
(4.12)

\[ \frac{\sigma_p J_p (N_{pt} - p_t)}{q} = <e_p> p_t + \frac{\sigma_n J_n p_t}{q} \]  
(4.13)

\[ \frac{\sigma_n J_n (N_{nt} - n_t)}{q} = <e_n> n_t + \frac{\sigma_p J_p n_t}{q} \]  
(4.14)

4.2 Single Trap Level, Single Current

4.2.1 Hole Flow

For a p-type substrate with a gold gate, a negative bias applied to the gate will induce accumulation of holes on the silicon surface. Those holes will be injected into the dielectric through the tunneling mechanism and will also cause electron injection from the gate electrode if the buildup field due to trapped holes is large enough to effectively decrease the electron injection barrier near the cathode. If the Fermi level of the metal gate is lower than that of the gold, electron current is unlikely to exist for small negative gate bias. In this section, a purely hole flow case will be discussed.
Since holes are assumed to be the dominant carrier, electron traps will be unoccupied, owing to the absence of electron current. Hence,

\[ n \ll p, \quad n_t \ll p_t \]

\[ J_n \ll J_p \]

and

\[ J_p = J \]

Eqs. (4.13) and (4.14) can be used to solve for \( J_n \) and \( J_p \). In general

\[
J_p = \frac{q p_t}{\sigma_p} \left[ \frac{\langle e_p \rangle (N_{nt} - n_t) + \langle e_n \rangle n_t}{(N_{pt} - p_t)(N_{nt} - n_t) - p_t n_t} \right]
\]

(4.15)

and

\[
J_n = \frac{q n_t}{\sigma_n} \left[ \frac{\langle e_n \rangle (N_{pt} - p_t) + \langle e_p \rangle p_t}{(N_{pt} - p_t)(N_{nt} - n_t) - p_t n_t} \right]
\]

(4.16)

If we assumed that the trap depths for electrons and holes are 2 eV and 1.1 eV [74] respectively, Eqs. (4.5) and (4.6) indicates that \( \langle e_n \rangle \) is less than \( \langle e_p \rangle \) by fifteen orders of magnitude. Hence, it is reasonable to neglect the electron detrapping term from Eqs. (4.15) and (4.16).

With the assumptions mentioned above, \( J_n \) and \( J_p \) can be simplified to

\[
J_p = \frac{q}{\sigma_p} \frac{p_t}{N_{pt} - p_t} \langle e_p \rangle
\]

(4.17)

and

\[
J_n = \frac{q n_t}{\sigma_n} \frac{\langle e_n \rangle p_t}{(N_{pt} - p_t)(N_{nt} - n_t)}
\]

(4.18)
Substituting Eq. (4.5) into $J_p$ yields

$$J_p = J_{pc} \frac{p_t}{N_{pt} - p_t} \exp\left[- \frac{q}{kT} (\phi_{pt} - \beta/E)\right]$$  \hspace{1cm} (4.19)$$

where

$$J_{pc} = \frac{q \nu_p}{\sigma_p} = qN_vV$$

the constant $J_{pc}$ is a material-dependent value, which also is a field-dependent value. However, in the case of high-field stress, $V = V_{th}$, and $J_{pc}$ can be regarded as a constant [64]. The saturation velocity $V_{th}$ is about $1 \times 10^7$ cm/sec.

The trapped hole density as a function of the distance can be derived from Eq. (4.19)

$$p_t(x) = \frac{N_{pt}}{1 + \frac{J_{pc}}{J_p} \exp\left[- \frac{q}{kT} (\phi_{pt} - \beta/E)\right]}$$  \hspace{1cm} (4.20)$$

The field distribution can be determined from Poisson's equation and Eq. (4.20)

$$\frac{dE}{dx} = \frac{qp_t}{\epsilon_n} = \frac{q}{\epsilon_n} \frac{N_{pt}}{1 + \frac{J_{pc}}{J_p} \exp\left[- \frac{q}{kT} (\phi_{pt} - \beta/E)\right]}$$  \hspace{1cm} (4.21)$$
Separating the variables in Eq. (4.21) and integrating the electric field from $E_o$ to $E$ yields

$$
\int_{E_o}^{E} \left[ 1 + J_{pc} \left( \frac{qN_{pt}}{kT} \right) \exp \left( \frac{q\beta}{kT} \right) \right] \frac{1}{J_{p}} \exp \left( -\frac{q\beta}{kT} \right) dE' = \int_{0}^{x} \frac{qN_{pt}}{\varepsilon_n} \frac{dx'}{E}.
$$

(4.22)

where $E_o$ is the contact field at the oxide/nitride interface and $x$ is measured from the interface.

The hole trap density $N_{pt}$ can be time dependent due to bond breaking under high field stress and therefore also is a position-dependent value. However, for simplicity, we assume that in the steady-state case the hole trap density $N_{pt}$ is almost a constant value under high-field stress. As a result, $N_{pt}$ can be assumed to be a position-independent value and $N_{pt}(x) = N_{pt}$. Also, because hole flow produces the major current component, $J_p(x) = J = J = \text{constant}$. With these assumptions, Eq. (4.22) simplifies to

$$
\int_{E_o}^{E} \frac{J_{pc}}{J_{p}} \exp \left( -\frac{q\phi_{pt}}{kT} \right) \exp \left( \frac{q\beta}{kT} \right) dE' = \frac{qN_{pt}}{\varepsilon_n} \int_{0}^{x} \frac{dx'}{E}.
$$

(4.23)

Integration of Eq. (4.23) by parts gives

$$
\left[ \frac{E'}{2} + \frac{J_{pc}}{J} \exp \left( -\frac{q\phi_{pt}}{kT} \right) \left( \frac{\sqrt{E'}}{q\beta} - \frac{1}{q\beta} \right) \exp \left( \frac{q\beta}{kT} \right) \right] \bigg|_{E_o}^{E} = \left[ \frac{qN_{pt} \chi'}{\varepsilon_n} \right] \bigg|_{0}^{x}.
$$

(4.24)
The relationship between electric field and the position \( x \) can be expressed as

\[
E + \frac{2J_{pc} \frac{kT}{J} \sqrt{E - \frac{kT}{q\beta}}} {q\beta} \exp \left( -\frac{q}{kT} (\phi_{pt} - \beta/E) \right) + C = \frac{qN_{pt}}{\varepsilon_N} x \tag{4.25}
\]

where

\[
C = \frac{2J_{pc} \frac{kT}{J} \left( \frac{kT}{q\beta} - \sqrt{E_o} \right) \exp \left( -\frac{q}{kT} (\phi_{pt} - \beta/E_o) \right) - E_o}{q\beta} \tag{4.26}
\]

The plot of the electric field distribution is depicted in Fig. 29. Once the field is solved, the trapped hole distribution can be obtained using Eq. (4.20) and is plotted in Fig. 30.

### 4.2.2 Electron Flow

If a capacitor with an aluminum gate is fabricated with an n-type silicon substrate, then a positive current or voltage stress will inject electrons from the silicon interface into the nitride. Although trapped electrons will reduce the energy barrier for hole injection near the gate electrode [46], the hole injection from the gate is usually negligible compared to the electron injection from the n-type silicon substrate, therefore, the current transport inside the nitride layer is mainly due to electrons.

For this case, absence of hole current leaves the hole traps unoccupied. Following the same procedure as in Section 4.1.1, we assume

\[
n \gg p, \quad n_t \gg p_t
\]

\[
J_n \gg J_p
\]
Figure 29. Electric field distribution due to trapping of hole charges.
Figure 30. Trap distribution for holes - one carrier case
and

\[ J_n = J \]

Using the same derivation as for holes, the electron current density is

\[ J_n = J_{nc} \frac{n_t}{N_{nt}-n_t} \exp\left[-\frac{q}{kT} (\phi_{nt}-\beta/E)\right] \quad (4.27) \]

where

\[ J_{nc} = \frac{q \nu_n}{\sigma_n} = q \overline{N}v_{th} \]

and the electron trap distribution is

\[ n_t(x) = \frac{N_{nt}}{1 + \frac{J_{nc}}{J} \exp\left[-\frac{q}{kT} (\phi_{nt}-\beta/E)\right]} \quad (4.28) \]

By assuming \( N_{nt}(x) = N_{nt} \) at high-field stress, the electric field in terms of position is

\[ E + \frac{2J_{nc}}{J} \frac{kT}{q\beta} \left[ \sqrt{E} - \frac{kT}{q\beta} \right] \exp\left[-\frac{q}{kT} (\phi_{nt}-\beta/E)\right] + C = -\frac{qN_{nt}}{\varepsilon_n} x \quad (4.29) \]

where

\[ C = 2\frac{J_{nc}}{J} \frac{kT}{q\beta} \left[ \frac{kT}{q\beta} - \sqrt{E_0} \right] \exp\left[-\frac{q}{kT} (\phi_{nt}-\beta/E_0)\right] - E_0 \quad (4.30) \]

It is clear that the electric field and trap distribution for electrons bears resemblance to those of holes. The differences reside in the values of the various parameters.
4.3 Two Trap Levels, Two Currents

Two-carrier flow in the nitride is a complex system even in steady state. To simplify the analysis, we separate the transport mechanism into three categories. Two simplified cases, the negligible detrapping case and the negligible recombination case, will be discussed here. The general case with charge trapping, detrapping, and recombination of both electrons and holes will be discussed in the Appendix A.

4.3.1 No Detrapping Case

Detrapping of the trapped charge occurs if the stored charge has a large density or if the trap level is very shallow. If the dielectric has a poor trapping efficiency or if the stored charge is not large enough that the trapped charge wave front does not have the capability of inducing high electric field, then detrapping of the trapped charge is unlikely to happen. Although nitride has been found to have large trapping density, whether these traps in the nitride can be filled or not depends on the amount of charge tunneling into the nitride layer. Since the silicon/nitride interface usually traps a lot of charge, whether the charges will propagate deeply into the nitride or not depends on the external field applied. If the field is very low, after the oxide blocks some of the tunneling charge not many trapping charges can tunnel into the nitride; hence, detrapping phenomenon will not happen.

Under such a condition, the detrapping coefficient $\langle e_n \rangle$ and $\langle e_p \rangle$ are approximately zero, therefore, Eqs. (4.11) to (4.14) can be simplified to
\[
\frac{dJ_p}{dx} + \sigma_p J_p (N_{pt} - p_t) + \sigma_p J_p n_t = 0
\]

(4.31)

\[
- \frac{dJ_n}{dx} + \sigma_n J_n (N_{nt} - n_t) + \sigma_n J_n p_t = 0
\]

(4.32)

\[
\sigma_p J_p (N_{pt} - p_t) = \sigma_n J_n p_t
\]

(4.33)

\[
\sigma_n J_n (N_{nt} - n_t) = \sigma_p J_p n_t
\]

(4.34)

Rearranging Eq. (4.34) yields

\[
\frac{N_{nt} - n_t}{n_t} = \frac{\sigma_p J_p}{\sigma_n J_n} = \frac{\sigma_p J_p}{\sigma_n (J - J_p)}
\]

and

\[
\frac{1}{n_t J_p} = \frac{1}{N_{nt}} - \frac{\sigma_p}{\sigma_n (J - J_p)}
\]

(4.35)

Similarly, Eq. (4.33) yields

\[
\frac{1}{p_t J_n} = \frac{1}{N_{pt}} - \frac{\sigma_n}{\sigma_p (J_n - J)}
\]

(4.36)

Combining Eqs. (4.33) and (4.31) gives

\[
\frac{dJ_p}{dx} = - \sigma_n J_n p_t - \sigma_p J_p n_t
\]

(4.37)
Substituting Eqs. (4.35) and (4.36) yields

\[
\frac{dJ_p}{dx} = - \frac{(N_{pt} + N_{nt}) \left[ \sigma_p \sigma_n r_p (1 - r_p) \right] J}{\sigma_p r_p + \sigma_n (1 - r_p)} \tag{4.38}
\]

where

\[ r_p = \frac{J_p}{J} \]

Separating \( r_p \) and \( x \) gives

\[
\left[ \frac{1}{\sigma_p r_p} + \frac{1}{\sigma_n (1 - r_p)} \right] dr_p = - (N_{pt} + N_{nt}) dx \tag{4.39}
\]

Integrating both sides yields

\[
\frac{1}{\sigma_p} \frac{r_p}{(1 - r_p)} = \frac{1}{\sigma_p} \frac{r_{po}}{(1 - r_{po})} \exp \left[ - (N_{pt} + N_{nt}) x \right] \tag{4.40}
\]

where \( r_{po} \) is the hole injection current ratio at the oxide/nitride interface.

Consider Eq. (4.40), the electron trap level is deep and the hole trap level is shallow. While holes are easily captured, there is also greater chance to be detrapped. Compared with hole traps, electron traps have less possibility of capturing electrons; however, once an electron has been trapped it can stay longer. Also, the drift velocities may be different for electrons and holes. For the above reasons, it is difficult to compare the capture cross-sectional area of
electrons and holes because the capture cross-sectional area is a function of both the capture coefficient and the velocity. Also

\[ \sigma_p = \frac{\langle C_p \rangle}{V_{p\text{th}}} \]
\[ \sigma_n = \frac{\langle C_n \rangle}{V_{n\text{th}}} \]

where \( \langle C_p \rangle \) and \( \langle C_n \rangle \) are capture coefficients and \( V_{p\text{th}} \) and \( V_{n\text{th}} \) are drift saturation velocities of holes and electrons. Nevertheless, for simplicity, we assume that the capture cross-sectional areas are equal

\[ \sigma_p = \sigma_n = \sigma \]

Equation (4.40) then becomes

\[ \frac{r_p}{1-r_p} = \frac{r_{p\text{to}}}{1-r_{p\text{to}}} \exp\left[-\sigma(N_{p\text{t}}+N_{n\text{t}})x\right] \quad (4.41) \]

The effective trapping length \( \lambda \) can be defined as

\[ \lambda = \left[ \sigma(N_{p\text{t}}+N_{n\text{t}}) \right]^{-1} \]

Substituting \( \lambda \) into Eq. (4.41), \( r_p \) can be solved in terms of \( x \) as

\[ r_p = \left[ 1 + \frac{1-r_{p\text{to}}}{r_{p\text{to}}} \exp\left(\frac{x}{\lambda}\right) \right]^{-1} \quad (4.42) \]

and the hole current density is

\[ J_p(x) = J \frac{1-r_{p\text{to}}}{1 + \frac{1-r_{p\text{to}}}{r_{p\text{to}}} e^{x/\lambda}} \quad (4.43) \]
The electron current distribution can be obtained by combining the current Eqs. (4.9) and (4.43), which gives

\[ J_n(x) = \frac{J}{1 + \frac{r_p}{1-r_p} e^{-x/\lambda}} \]  

(4.44)

The current density equations shown above indicate that as \( x \) increases the hole current starts to decrease due to hole trapping and recombination, whereas the electron current increases and reaches its maximum value at the nitride/gate interface. A plot of the normalized \( J_p(x) \) and \( J_n(x) \) is depicted in Fig. 31.

The equations derived above concentrate on the charge injection near the oxide/nitride interface; the nitride thickness was not explicitly involved in the theoretical derivation. Since different nitride thickness might result in different phenomena, especially for the ultra-thin nitride layer, the following discussion focuses on finding the relationship between the injection current level at both cathode and anode electrodes and the nitride thickness.

Instead of using the oxide/nitride interface hole injection current, an alternate approach to the transport mechanism is to use the electron current injection ratio at the nitride/metal-gate interface. Following the same procedure as for \( J_p \) in Eq. (4.38), Eqs. (4.32) and (4.33) can be manipulated to obtain

\[ \frac{dJ_n}{dx} = \frac{(N_{nt} + N_{pt}) \sigma_p \sigma_r (1-r_n) J}{\sigma_p (1-r_n) + \sigma_n r_n} \]  

(4.45)
Figure 31. Normalized hole and electron current distributions under two different $R_{po}$. $R_{po} = J_p / J$, $J$ is the total current density and $J_p$ is the hole injection current density at SiO$_x$/Si$_3$N$_4$ interface. $\lambda$ is the effective trapping length.
where

\[ r_n = \frac{J_n}{J} \]

Again, assuming the capture cross section of electrons and holes are equal, integrating Eq. (4.45) results in

\[ J_n = \frac{J}{1 - r_{nL} \left( \frac{T_N - x}{\lambda} \right)} \left( 1 + \frac{r_{nL}}{e^{\frac{T_N}{V_x} e^{\frac{T_N}{\lambda}}}} \right) \]

where \( T_N \) is the nitride thickness and \( r_{nL} \) is the electron current injection ratio at the nitride/gate interface, i.e. \( r_{nL} = \frac{J_n}{J} \). Since \( J_p(0) + J_n(0) = J \), Eqs. (4.43) and (4.46) can be used to find the relationship between \( r_{po} \) and \( r_{nL} \)

\[ r_{po} = \frac{1}{1 + \frac{r_{nL} \left( \frac{T_N}{\lambda} \right)}{1 - r_{nL} \left( \frac{T_N}{\lambda} \right) e^{\frac{T_N}{V_x} e^{\frac{T_N}{\lambda}}}}} \]

This result indicates for each particular stressed current or voltage experiment that once the charge transport reaches steady state, hole injection current at the oxide/nitride interface and electron injection current at the nitride/gate interface are fixed values dependent on each other.

The location where the hole current equals the electron current can be determined by setting \( J_p \) equal to \( J_n \) in Eqs. (4.43) and (4.45), which yields
To find the trapped charge distribution, Eq. (4.33) can be rewritten as

$$\frac{N_{pt}-N_{pt}^{t}}{N_{pt}} = \frac{\sigma_n J_n}{\sigma_p J_p}$$

Substituting $J_n$ and $J_p$ into the above equation yields

$$p_t(x) = \frac{N_{pt}}{1-r_{po} x/\lambda} \frac{1}{1 + \frac{r_{po}}{1-r_{po}} e^{r_{po}} x/\lambda}$$  \hspace{1cm} (4.49)$$

The trapped electron distribution can be obtained by substituting $J_n$ and $J_p$ into Eq. (4.34), which yields

$$n_t(x) = \frac{N_{nt}}{1-\frac{r_{po}}{1-r_{po}} e^{-x/\lambda}}$$  \hspace{1cm} (4.50)$$

It is interesting to note that under negligible detrapping condition the trapped charge distributions have the same wave shape as the current distributions for both electrons and holes.

To solve for the electric field distribution, Poisson's equation is employed. The integral of both trapped hole and trapped electron concentration yields

$$\int_0^\infty p_t(x') dx' = N_{pt} \left[ x-\lambda \ln \frac{r_{po}+(1-r_{po})\exp\left(\frac{x}{\lambda}\right)}{r_{po}} \right]$$  \hspace{1cm} (4.51)$$
Integration of Poisson's equation will yield the electric field distribution

$$E(x) = E_0 + \frac{q}{\varepsilon_n} \left[ (N_{pt} - N_{nt}) x - \ln \left( \frac{r_{po} + (1 - r_{po}) e^{x/\lambda}}{1 - r_{po} + r_{po} e^{-x/\lambda}} \right) N_{nt} \lambda \right]$$

(4.53)

If gate bias is a constant, the contact field at both interfaces would not be the same as the average field. However, if DC current stress instead of the DC voltage stress is applied to the gate, then the contact field at the oxide/nitride interface will be a fixed value provided that the stored charge at the silicon/oxide interface and oxide bulk does not change with time. Once the contact field is a constant, the electric field at the nitride/gate interface will also be a fixed value, which is given by

$$E(T_N) = E_0 + \frac{q}{\varepsilon_n} \left[ (N_{pt} - N_{nt}) T_N - \ln \left( \frac{r_{po} + (1 - r_{po}) e^{T_N/\lambda}}{1 - r_{po} + r_{po} e^{-T_N/\lambda}} \right) N_{nt} \lambda \right]$$

(4.54)

The electric field distribution is shown in Fig. 32. The position of the maximum electric field $x_{EMM}$ can be obtained from the Poisson's equation

$$\left. \frac{dE}{dx} \right|_{x_{EMM}} = \frac{q}{\varepsilon_n} (p_t - n_t) = 0$$

(4.55)
which gives \( p_t = n_t \) at \( x_{ENM} \). Substituting \( p_t \) and \( n_t \) from Eqs. (4.49) and (4.50) into the above equation yields

\[
\frac{N_{pt}}{1 - r_{po} x_{ENM}/\lambda} = \frac{N_{nt}}{1 + \frac{r_{po}}{1 - r_{po}}} e^{-x_{ENM}/\lambda} \tag{4.56}
\]

Rewriting Eq. (4.56) gives the \( x_{ENM} \) as

\[
x_{ENM} = \lambda \ln \left[ \frac{N_{pt}}{N_{nt}} \left( \frac{1}{1 - r_{po}} \right) \right] \tag{4.57}
\]

As the above equation indicates, when \( r_{po} \) increases hole traps will be injected farther into the nitride layer and therefore a larger \( x_{ENM} \) is obtained. However, if \( r_{po} \) decreases a significant part of the electron flow will pass through the nitride and reach the hole injection interface and force the maximum electric field \( E_{NM} \) to be close to the anode, as depicted in Fig. 32.

The maximum electric field can be obtained by substituting \( x_{ENM} \) into Eq. (4.53). After some manipulation, the maximum electric field \( E_{NM} \) is

\[
E_{NM} = E_o + \frac{q}{r_N} \ln \left( \frac{N_{pt} r_{po}}{N_{nt} (1 - r_{po})} \right) \tag{4.58}
\]
Figure 32. Typical electric field distribution plots for nitride layer with negligible detrapping. $\Delta E = E - E_0$, where $E_0$ is the contact electric field at $\text{SiO}_2/\text{Si}_3\text{N}_4$ interface.
4.3.2 Trapping and Detrapping without Recombination

When the nitride layer is very thick or there is small possibility that the electron and hole trap regions are overlapped, then recombination is less likely to occur. In such a case we can neglect the recombination terms, and Eqs. (4.11) to (4.14) will be changed to

\[ \frac{1}{q} \frac{dJ}{dx} + \frac{\sigma_p J_p}{q} (N_{p^+} - P_t) = <e_p>J_p \]  

(4.59)

\[ - \frac{1}{q} \frac{dJ}{dx} + \frac{\sigma_n J_n}{q} (N_{n^-} - N_t) = <e_n>J_n \]  

(4.60)

\[ \frac{\sigma_p J_p}{q} (N_{p^+} - P_t) = <e_p>J_p \]  

(4.61)

\[ \frac{\sigma_n J_n}{q} (N_{n^-} - N_t) = <e_n>J_n \]  

(4.62)

If we change variables by letting

\[ \frac{q \phi_{p^+}}{kT} = A_p \]  

(4.63)

\[ \frac{q \phi_{n^-}}{kT} = A_n \]  

(4.64)

\[ \frac{q \beta}{kT} = B \]  

(4.65)
then the Poole-Frenkel (P-F) equations will become

\[
\langle e_p \rangle = \nu_p \exp(B/\varepsilon - A_p)
\]

\[
\langle e_n \rangle = \nu_n \exp(B/\varepsilon - A_n)
\]

Substituting the P-F equations into Eqs. (4.59) to (4.62) gives

\[
\frac{dJ_p}{dx} + \sigma_p J_p(N_{pt} - p_t) = q_p \nu_p \exp(B/\varepsilon - A_p)
\]

(4.66)

\[
- \frac{dJ_n}{dx} + \sigma_n J_n(N_{nt} - n_t) = q_n \nu_n \exp(B/\varepsilon - A_n)
\]

(4.67)

\[
\sigma_p J_p(N_{pt} - p_t) = q_p \nu_p \exp(B/\varepsilon - A_p)
\]

(4.68)

\[
\sigma_n J_n(N_{nt} - n_t) = q_n \nu_n \exp(B/\varepsilon - A_n)
\]

(4.69)

The above four equations imply that the current densities are the same through the nitride layer, i.e.

\[
J_p(x) = J_p = \text{const.}
\]

\[
J_n(x) = J_n = \text{const.}
\]

The trapped hole distributions can be solved by combining Eqs. (4.68) and (4.69). The trapped hole distribution is

\[
N_{pt} = \frac{\sigma_p J_p N_{pt}}{\sigma_p J_p + q_p \nu_p \exp(B/\varepsilon - A_p)}
\]

(4.70)
and the trapped electron distribution is

$$n_t = \frac{\sigma_n J_n N_{nt}}{\sigma_n J_n + q \nu_n \exp(B/E - A_n)}$$  \hspace{1cm} (4.71)

In order to simplify this equation, the capture cross section and the attempt-to-escape frequency of electrons and holes can be assumed to be equal. Under such conditions, Poisson’s equation yields

$$\frac{\left[\sigma_p + q \nu_p \exp(B/E - A_p)\right]}{\left[\sigma_n + q \nu_n \exp(B/E - A_n)\right]} dE = \frac{q \sigma}{\varepsilon} dx$$

(4.72)

Kapoor [74] observed that electron traps have deeper energy levels when compared with the hole trap energy level. Therefore

$$\phi_{pt} < \phi_{nt}$$

which means that the constant $A_n$ should be greater than $A_p$. Furthermore, although investigators have different opinions about the dominant type of current inside the dual-dielectric MNOS system, $J_n \neq J_p$ has been reported in most cases. The I-V curves shown in Fig. 33 serve as one example. Based on the above reasoning, Eq. (4.72) can not be further simplified. Integration of Eq. (4.72) gives

$$x = \frac{\varepsilon_n}{q \sigma} \int_{E_0}^{E} \frac{\left[\sigma_p + q \nu_p \exp(B/E' - A_p)\right]}{\left[\sigma_n + q \nu_n \exp(B/E' - A_n)\right]} dE'$$

(4.73)
Figure 33. Typical I-V curves for $I_N$ and $I_p$ with two different dielectrics thickness.
This integral equation form of the electric field can be solved by using a numerical method (e.g. Simpson’s composite rule [77]). The trapped hole and electron charge densities can then be calculated from Eqs. (4.63) and (4.64).

The saturated electric field or the maximum electric field could be obtained by setting dE/dx = 0 in Eq. (4.72). With exp(-A_p) = a and exp(-A_n) = b, substitution of a and b into Eq. (4.72) gives

\[
\frac{J_{pNnt}}{J_{nNnt}} = \frac{\sigma J_p^{qV} \exp(BV_{nnt})}{\sigma J_n^{qV} \exp(BV_{nnt})} \quad (4.74)
\]

Further manipulation yields the maximum electric field

\[
E_{nm} = \left[ \frac{1}{B} \ln \left( \frac{\sigma J_p^{qV} \left( \frac{N_{nt} - N_{pt}}{bJ_pN_{pt} - aJ_nN_{nt}} \right)}{qV} \right) \right]^2 \quad (4.75)
\]

The equation shown above indicates that the peak electric field will be an undefined value or infinity if \( N_{nt} = N_{pt} \) or \( bJ_pN_{pt} = aJ_nN_{nt} \). Also, the following condition has to be satisfied

\[
\frac{N_{nt} - N_{pt}}{bJ_pN_{pt} - aJ_nN_{nt}} > 0 \quad (4.76)
\]

A thorough investigation of Eqs. (4.70) and (4.71) indicates that the condition \( bJ_pN_{pt} = aJ_nN_{nt} \) will result in \( N_{nt} = N_{pt} \) and vice versa. If \( N_{nt} = N_{pt} \), Eq. (4.74) implies that in order to have the peak electric field the current densities \( J_p \) and \( J_n \) can not be arbitrarily chosen, the trap depth \( \phi_{pt} \) and \( \phi_{nt} \) will affect the relationship between \( J_p \) and \( J_n \) as
Since $\phi_{nt}$ is usually larger than $\phi_{pt}$ for the nitride layer, Eq. (4.77) indicates that $J_n$ will be far larger than $J_p$ if $N_{nt}$ equals $N_{pt}$, this is almost like the one-carrier (hole) injection case in which only hole trapping is significant.

If $N_{nt}$ larger than $N_{pt}$, Eq. (4.76) implies that

$$\exp\left(\frac{q\phi_{pt}}{kT}\right) \frac{J_n}{J_p}$$

Eq. (4.78) implies that $J_n$ is negligible, and again only hole injection is significant.

Owing to the different polarity of the stored charges, it is not surprising that the slope of the electric field distribution will have a different sign near the anode and cathode electrodes. For example, if a gold-gate capacitor with p-type substrate is under negative gate biasing, the hole injection near the anode result in a positive slope of the electric field distribution. At the other end, electron injection from the cathode tends to reduce the electric field near the gate, so that the slope is negative near the cathode. Hence, modification of
Eq. (4.73) is necessary in order to solve for the $E$ field. Simpson's rule can still be applied if the following change is made

$$x = \frac{E}{q\sigma} \int_{\frac{J_p}{N_p}}^{E_{en}} \left[ \sigma J_p + q \exp(B/E' - A_p) \right] \left[ \sigma J_n + q \exp(B/E' - A_n) \right] \, dE'$$

(4.79)

for $x < x_{ENH}$ and

$$x = \frac{E}{q\sigma} \int_{\frac{J_p}{N_p}}^{E_{ENH}} \left[ \sigma J_p + q \exp(B/E' - A_p) \right] \left[ \sigma J_n + q \exp(B/E' - A_n) \right] \, dE'$$

(4.80)

for $x > x_{ENH}$, where $x_{ENH}$ is the location where the electric field reaches a saturation or a maximum value. An example of the electric field distribution is shown in Fig. 34.

In Eq. (4.73), the contact field $E_0$ is not a random value, in fact, it should be gate voltage dependent. Although the electric field distribution plotted in Fig. 34 is based on $E_0 = 1.5$ MV/cm, similar shaped electric field distributions are also obtained for $E_0$ ranging from 1 to 2 MV/cm. For most cases, the electric field increases very fast and almost reaches saturation within 1000 Å, then, a nearly constant electric field along the nitride layer for more than several μm. Meanwhile, the decreasing of the electric field due to the trapped electrons can not be found. One explanation of this non-decreasing electric field is that the trapped hole charges compensate the trapped electron charges along the whole nitride layer, hence the electric field
Figure 34. Typical electric field distribution for the negligible recombination case.

\[
\begin{align*}
\beta &= 2.8672E-4 \text{ J/V-cm} \\
\phi_{pt} &= 1.1 \text{ eV} \\
\phi_{nt} &= 2.0 \text{ eV} \\
E_0 &= 1.5E6 \text{ V/cm} \\
N_{pt} &= 9E18 \text{ cm}^{-3} \\
N_{nt} &= 8E18 \text{ cm}^{-3} \\
\text{Area} &= 1.22E-3 \text{ cm}^2 \\
E_{NM} &= 2.038638E6 \text{ V/cm} \\
V_{th} &= 1E7 \text{ cm/sec} \\
\varepsilon_n &= 7E_0 = 6.195E-13 \text{ F/cm} \\
\sigma &= 1E-13 \text{ cm}^2 \\
V &= 2.5E13 \text{ sec}^{-1} \\
I_p &= 1uA, I_n = 0.2uA \\
N_c &= N_v = 2.5E19 \text{ cm}^{-3}
\end{align*}
\]
distribution is almost like that of the single carrier injection case. A plot of the trapped charge distribution base on Eqs. (4.70) and (4.71) indicated that a space-charge free region does not exist inside the nitride layer, instead, the trapped hole and electron charges almost maintain the constant value through the nitride layer, as depicted in Fig. 35.

In the DC stress case, the average electric field usually ranges from 1 to 15 MV/cm, while in our simulation it is almost impossible to generate reasonable data with dielectric thickness less than 500 Å and still have electric field around 10 MV/cm. Table 5 lists several parameters and the resulated $E_{NH}$ and $x_{ERM}$. All the data imply that the two-carrier charge transport model with no charge recombination is not suitable for modeling the charge transport in thin dielectric devices.
Figure 35. Typical hole and electron trap density distributions for the negligible recombination case
Table 5. $E_{EM}$ and $x_{EM}$ for no recombination case

<table>
<thead>
<tr>
<th>$J_p$ (μA)</th>
<th>$J_n$ (eV)</th>
<th>$\phi_{pt}$ (eV)</th>
<th>$\phi_{nt}$ (eV)</th>
<th>$N_{nt}$ (cm$^{-3}$)</th>
<th>$N_{pt}$ (cm$^{-3}$)</th>
<th>$E_o$ (MV/cm)</th>
<th>$E_{EM}$ (MV/cm)</th>
<th>$x_{EM}$ (Å)</th>
<th>$\phi_F$ (eV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.2</td>
<td>1.1</td>
<td>2</td>
<td>9E18</td>
<td>8E18</td>
<td>1</td>
<td>3.821665</td>
<td>2639.4053</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>1.4</td>
<td>1.1</td>
<td>2</td>
<td>9E18</td>
<td>8E18</td>
<td>1</td>
<td>3.821665</td>
<td>2639.4053</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>1.6</td>
<td>1.1</td>
<td>2</td>
<td>9E18</td>
<td>8E18</td>
<td>1</td>
<td>3.821665</td>
<td>2639.4053</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>1.8</td>
<td>1.1</td>
<td>2</td>
<td>9E18</td>
<td>8E18</td>
<td>1</td>
<td>3.821665</td>
<td>2639.4053</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>1.1</td>
<td>1.1</td>
<td>2</td>
<td>9E18</td>
<td>8E18</td>
<td>1.5</td>
<td>3.821665</td>
<td>2416.1138</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>1.1</td>
<td>1.1</td>
<td>2</td>
<td>9E18</td>
<td>8E18</td>
<td>2</td>
<td>3.821665</td>
<td>2204.4610</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>1.1</td>
<td>1.1</td>
<td>2</td>
<td>9E18</td>
<td>8E18</td>
<td>3</td>
<td>3.821665</td>
<td>1836.3841</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>1.1</td>
<td>1.1</td>
<td>2</td>
<td>9E18</td>
<td>8E18</td>
<td>3.5</td>
<td>3.821665</td>
<td>1691.2893</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>1.1</td>
<td>1.1</td>
<td>2</td>
<td>9E18</td>
<td>8E18</td>
<td>3.8</td>
<td>3.821665</td>
<td>1618.8601</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>1.1</td>
<td>1.2</td>
<td>2</td>
<td>9E18</td>
<td>8E18</td>
<td>1</td>
<td>5.625267</td>
<td>3770.8902</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>1.1</td>
<td>1.3</td>
<td>2</td>
<td>9E18</td>
<td>8E18</td>
<td>1</td>
<td>7.776407</td>
<td>5090.0981</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>1.1</td>
<td>1.4</td>
<td>2</td>
<td>9E18</td>
<td>8E18</td>
<td>1</td>
<td>10.275086</td>
<td>6595.2768</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>1.1</td>
<td>1.5</td>
<td>2</td>
<td>9E18</td>
<td>8E18</td>
<td>1</td>
<td>13.121304</td>
<td>8285.5966</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>1.1</td>
<td>1.1</td>
<td>2</td>
<td>9E18</td>
<td>8.2E18</td>
<td>1</td>
<td>3.717862</td>
<td>3183.1476</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>1.1</td>
<td>1.1</td>
<td>2</td>
<td>9E18</td>
<td>8.4E18</td>
<td>1</td>
<td>3.589308</td>
<td>4065.9709</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>1.1</td>
<td>1.1</td>
<td>2</td>
<td>9E18</td>
<td>8.6E18</td>
<td>1</td>
<td>3.416119</td>
<td>5764.8873</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>1.1</td>
<td>1.1</td>
<td>2</td>
<td>9E18</td>
<td>8.8E18</td>
<td>1</td>
<td>3.136551</td>
<td>10532.2046</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>1.1</td>
<td>1.1</td>
<td>2</td>
<td>9E18</td>
<td>8.9E18</td>
<td>1</td>
<td>2.318788</td>
<td>19287.4034</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>1.1</td>
<td>1.1</td>
<td>2</td>
<td>9E18</td>
<td>8.99E18</td>
<td>1</td>
<td>2.089767</td>
<td>142030.9576</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>1.2</td>
<td>1.1</td>
<td>2</td>
<td>9E18</td>
<td>8E18</td>
<td>1</td>
<td>2.675166</td>
<td>1199.2228</td>
<td>7</td>
<td></td>
</tr>
<tr>
<td>1.4</td>
<td>1.1</td>
<td>2</td>
<td>9E18</td>
<td>8E18</td>
<td>1</td>
<td>2.675166</td>
<td>1199.2228</td>
<td>7</td>
<td></td>
</tr>
<tr>
<td>1.6</td>
<td>1.1</td>
<td>2</td>
<td>9E18</td>
<td>8E18</td>
<td>1</td>
<td>2.675166</td>
<td>1199.2228</td>
<td>7</td>
<td></td>
</tr>
<tr>
<td>1.8</td>
<td>1.1</td>
<td>2</td>
<td>9E18</td>
<td>8E18</td>
<td>1</td>
<td>2.675166</td>
<td>1199.2228</td>
<td>7</td>
<td></td>
</tr>
<tr>
<td>1.1</td>
<td>1.1</td>
<td>2</td>
<td>9E18</td>
<td>8E18</td>
<td>1.5</td>
<td>2.675166</td>
<td>1051.9143</td>
<td>7</td>
<td></td>
</tr>
<tr>
<td>1.1</td>
<td>1.1</td>
<td>2</td>
<td>9E18</td>
<td>8E18</td>
<td>2</td>
<td>2.675166</td>
<td>922.7422</td>
<td>7</td>
<td></td>
</tr>
<tr>
<td>1.1</td>
<td>1.1</td>
<td>2</td>
<td>9E18</td>
<td>8E18</td>
<td>2.5</td>
<td>2.675166</td>
<td>819.7877</td>
<td>7</td>
<td></td>
</tr>
<tr>
<td>1.1</td>
<td>1.1</td>
<td>2</td>
<td>9E18</td>
<td>8E18</td>
<td>2.6</td>
<td>2.675166</td>
<td>802.8267</td>
<td>7</td>
<td></td>
</tr>
<tr>
<td>1.1</td>
<td>1.2</td>
<td>2</td>
<td>9E18</td>
<td>8E18</td>
<td>1</td>
<td>3.937687</td>
<td>1747.637</td>
<td>7</td>
<td></td>
</tr>
<tr>
<td>1.1</td>
<td>1.3</td>
<td>2</td>
<td>9E18</td>
<td>8E18</td>
<td>1</td>
<td>5.443485</td>
<td>2390.785</td>
<td>7</td>
<td></td>
</tr>
<tr>
<td>1.1</td>
<td>1.4</td>
<td>2</td>
<td>9E18</td>
<td>8E18</td>
<td>1</td>
<td>7.192560</td>
<td>3126.294</td>
<td>7</td>
<td></td>
</tr>
<tr>
<td>1.1</td>
<td>1.5</td>
<td>2</td>
<td>9E18</td>
<td>8E18</td>
<td>1</td>
<td>9.184813</td>
<td>3953.226</td>
<td>7</td>
<td></td>
</tr>
<tr>
<td>1.1</td>
<td>1.1</td>
<td>2</td>
<td>9E18</td>
<td>8.2E18</td>
<td>1</td>
<td>2.602504</td>
<td>1442.2236</td>
<td>7</td>
<td></td>
</tr>
<tr>
<td>1.1</td>
<td>1.1</td>
<td>2</td>
<td>9E18</td>
<td>8.4E18</td>
<td>1</td>
<td>2.512516</td>
<td>1836.0531</td>
<td>7</td>
<td></td>
</tr>
<tr>
<td>1.1</td>
<td>1.1</td>
<td>2</td>
<td>9E18</td>
<td>8.6E18</td>
<td>1</td>
<td>2.391284</td>
<td>2591.8691</td>
<td>7</td>
<td></td>
</tr>
<tr>
<td>1.1</td>
<td>1.1</td>
<td>2</td>
<td>9E18</td>
<td>8.8E18</td>
<td>1</td>
<td>2.195586</td>
<td>4702.5286</td>
<td>7</td>
<td></td>
</tr>
<tr>
<td>1.1</td>
<td>1.1</td>
<td>2</td>
<td>9E18</td>
<td>8.9E18</td>
<td>1</td>
<td>2.011232</td>
<td>8554.9948</td>
<td>7</td>
<td></td>
</tr>
</tbody>
</table>
CHAPTER 5

RESULTS AND ANALYSIS

Most researchers believed before 1975 that the conduction current inside the nitride is due to electron flow. Later, some researchers started to consider the hole flow dominant inside the nitride layer, but no one could explain why the current is either electron or hole dominant. It was not until 1977 that Svensson proposed the dual-carrier model. Since then, little evidence has been shown to prove this theory. In the following experiment, two-carrier charge transport phenomena will be demonstrated experimentally through $I-t$, $V-t$, $I-V$, and $C-V$ curves. Observation of the behavior of electrical conduction is explained with transport processes of electron and hole flow in the nitride layers of nonvolatile memory devices. Analytical solutions based on the two-carrier charge transport model derived in Chapter 4 are also presented and compare with the experimental results. A detailed analysis investigating two-carrier flow will be discussed in Chapter 6.

5.1 Current Distribution and Energy Band Diagram

The major electron flow in silicon dioxide has been reported in the literature [78]. This one-carrier flow phenomenon can easily be explained using an energy band diagram. For a MOS device, the electron and hole barrier heights between the silicon substrate and the oxide layer were determined to be $3.1 \text{ eV}$ and $4.8 \text{ eV}$, as indicated in Fig. 15.
This large energy barrier height, 4.8 eV, will almost inhibit hole injection from the silicon substrate into the silicon dioxide under the gate bias [79]. Also, gamma ray and X-ray studies which generate e-h pairs in SiO₂ show that holes have very low mobility in SiO₂.

For dual-dielectric capacitors consisting of a thin oxide and 100 Å to 400 Å of nitride, the energy band diagram is different from that of a pure oxide. The ultra thin oxide (<43 Å) is used only to reduce the interface charge and is still within the tunneling distance. Since electrons and holes can easily tunnel through the oxide into the oxide/nitride interface, the energy barrier heights for electrons and holes at the silicon/oxide interface can be perceived as directly between the silicon substrate and the nitride. The electron and hole energy barrier heights were determined to be 2.05 eV and 1.95 eV respectively, as shown in Fig. 15. The nearly equivalent energy barrier heights indicates that both electron and hole injection are likely to happen.

While two-carrier flow has been observed in the past [27], [30], [80]-[81], no detailed physical explanation was given. In the discussion that follows, we will analyze C-V and I-t data to explain how two-carrier charge transport occurs under different gate polarities and different gate materials.

5.1.1 Gold-Gate Capacitors

A shift of the flat-band voltage is due to charge trapping in the dielectric layer. When a negative voltage or a negative current is applied to a gold-gate capacitor with p-type substrate, holes accumulate near the interface of the Si/SiO₂ and some of these holes will tunnel
through the oxide into the nitride bulk. The injection process may occur within a few micro seconds, but redistribution of trapped charge in the nitride takes longer. Figure 36 shows C-V plots for gold-gate capacitors with 20 Å oxide and 104 Å nitride. A negative current stress with an amplitude of 100 nA had been applied to the gate for different time periods before the C-V measurements were taken. A 104 Å thick nitride is so thin that a 500 second stress has almost caused the charge trapping to reach saturation, as indicated in Fig. 36.

Trapped charge will build up the localized field and change the electric field distribution within the nitride layer. As reported by Chang [46], holes injected from the substrate tend to increase the electric field at the trapping wave front. Once the induced field is high enough, the electron energy gap at the gate electrode reduces, which favors more electron injection from the gate. Therefore, the charge transport mechanism of MNOS devices is actually a two-carrier transport system. For the constant current stress curves depicted in Figs. 37 through 40, it is obvious that the gate voltages monitored during the -100 nA current stress almost reach steady state within 400 seconds. Since the gate voltage change equals the flat-band voltage shift (Appendix B), Eq. (B-12) gives

$$\Delta V_{FB}' - \Delta V_{FB} = - \frac{Q_p'}{\varepsilon_n} (T_p' - \bar{x}_p') + \frac{Q_n'}{\varepsilon_n} \bar{x}_n' + \frac{Q_p}{\varepsilon_n} (T_p - \bar{x}_p) - \frac{Q_n}{\varepsilon_n} \bar{x}_n$$

(5.1)

where $Q_p'$, $\bar{x}_p'$, $Q_n'$, and $\bar{x}_n'$ are total charges and charge centroids of electrons and holes after electrical stressed for a time interval $t'$. $Q_p$, $\bar{x}_p$, $Q_n$, and $\bar{x}_n$ are total charges and charge centroids of electrons
Figure 36. HF-CV curves for gold-gate capacitors with nitride/oxide thickness of 20/104 Å, obtained after a -100 nA gate current stress under different stress time.
Figure 37. Constant current stress $V$-$t$ curves for gold-gate capacitor with nitride/oxide thickness of 20/295 Å

Figure 38. Constant current stress $V$-$t$ curves for gold-gate capacitor with nitride/oxide thickness of 20/387 Å
Figure 39. Constant current stress V-t curves for gold-gate capacitor with nitride/oxide thickness of 30/99 Å.

Figure 40. Constant current stress V-t curves for gold-gate capacitor with nitride/oxide thickness of 20/206 Å.
and holes after electrical stressed for a time interval \( t \). Also

\[ Q'_p = 2 \rho'_p \times \bar{x}'_p \quad \text{and} \quad Q'_n = 2 \rho'_n \times \bar{x}'_n \quad (5.2) \]

\[ Q_p = 2 \rho_p \times \bar{x}_p \quad \text{and} \quad Q_n = 2 \rho_n \times \bar{x}_n \quad (5.3) \]

where \( \rho'_p \) and \( \rho_p \) are trapped hole charge densities and \( \rho'_n \) and \( \rho_n \) are trapped electron charge densities.

If we assume that the trapped charge attains its maximum value immediately after injection, then, \( \rho'_p = \rho_p \), and \( \rho'_n = \rho_n \).

Equation (5.1) gives

\[
\Delta V_{FB'} - \Delta V_{FB} = \frac{2\rho'_p \bar{x}'_p}{\varepsilon_n} (\bar{x}'_p - T_N) + \frac{2\rho'_n \bar{x}'_n}{\varepsilon_n} (\bar{x}'_n - \bar{x}_n') + \frac{2\rho_p \bar{x}_p}{\varepsilon_n} (T_N - \bar{x}_p) - \frac{2\rho_n \bar{x}'_n^2}{\varepsilon_n} \quad (5.4)
\]

Furthermore, if we also assume that the trapped charge density of electrons and of holes are equal, Eq. (5.4) yields

\[
\Delta V_{FB'} - \Delta V_{FB} = \frac{2\rho'_p \bar{x}'_p}{\varepsilon_n} (\bar{x}'_p - T_N) + \frac{2\rho'_n \bar{x}'_n}{\varepsilon_n} (\bar{x}'_n - \bar{x}_n') + \frac{2\rho'_p \bar{x}_p}{\varepsilon_n} (T_N - \bar{x}_p) - \frac{2\rho'_n \bar{x}'_n^2}{\varepsilon_n} \quad (5.5)
\]

If charge injection reaches steady state soon after the bias is applied, it is reasonable to assume that \( \Delta V_{FB'} - \Delta V_{FB} = 0 \), and Eq. (5.5) becomes

\[
\bar{x}'_n^2 - \bar{x}_n^2 = (\bar{x}'_p - \bar{x}_p) (T_N + \bar{x}'_p + \bar{x}_p) \quad (5.6)
\]

Equation (5.6) implies that in steady state if \( \bar{x}'_p = \bar{x}_p \) then \( \bar{x}'_n = \bar{x}_n \).

However, if \( \bar{x}'_p \neq \bar{x}_p \), electron charge centroid \( \bar{x}'_n \) and \( \bar{x}_n \) would not be the same either, more of the electrons have to be injected from the gate.
electrode, otherwise, the steady state condition can not be maintained. Although the electrons and holes are not in equilibrium during charge injection, the negative flat-band voltage shift shown in Fig. 35 clearly indicates that the net charge stored in the dual dielectric is positive, which is consistent with the previous argument that the energy barrier favors hole flow.

When a positive voltage is applied to the gate, the surface of the p-type substrate will be depleted and an inversion layer will be created. The electron carriers forming the inversion layer are generated through thermal generation of electron-hole pairs at the silicon substrate. If the external bias is not high enough, it is expected that concentration of electrons at the surface will be very small, so that when electrons are tunneling into the nitride layer from substrate the energy barrier for hole injection from the gate electrode does not change because the buildup field due to this small amount of the trapped electrons is small also. That trapped electrons can not induce hole injection does not mean that hole flow does not participate in the conduction. On the contrary, since there is only a 1.95 eV barrier between the Au Fermi level and the valence band of the nitride, the unlimited source of holes will supply hole injection when a positive gate bias is applied. The C-V shift shown in Fig. 41 indicates a net negative stored charge, which can be explained with the aid of the flat-band voltage equation. If we assume that there is no charge change within the oxide and at the interface, the flat-band voltage shift can be expressed as
Figure 41. HF C-V shift of gold-gate capacitor, obtained after 20 nA constant current stress with different stress time.
Although $p_p > p_n$ due to the positive gate bias, we can not be sure that $\Delta V_{FB}$ must be negative. The small electron surface concentration at the silicon interface will limit the electron charge centroid $x_n$ of the injected electrons to be located near the $SiO_2/Si_3N_4$ interface, hence, $T_N - x_n = T_N$. Since the hole charge centroid $x_p$ is also small under low-level injection, if we assume that $x_n = x_p$, a positive $\Delta V_{FB}$ is likely to exist, provided that $p_n \times T_N$ is larger than $p_p \times x_p$. This charge transport argument is verified if we consider the C-V shift for a longer time period. Then injected holes from the gate propagate deeper into the nitride, resulting in an increase of charge centroid $x_p$ reducing the flat-band voltage shift. This reduction of the flat-band voltage is presented in Fig. 41.

5.1.2 Aluminum-Gate Capacitors

The aluminum gate dual-dielectric capacitor has also been extensively used in investigation of charge trapping phenomenon in MNOS devices. Since electrons at the gate electrode have less energy barrier, they have a higher probability of being injected from the gate into the nitride bulk. In the C-V shifts of the aluminum-gate MNOS capacitors shown in Fig. 42, measurements were taken soon after samples were stressed by a positive 20 nA constant gate current. Since positive gate voltage is unlikely to inject holes from the aluminum-gate electrode into the nitride layer, conduction is more likely due to electrons injected from the substrate. The net trapped electron charge,
Figure 42. HF C-V shift of aluminum-gate capacitor, obtained after 20 nA positive constant current stress with different stress time.
which results in a positive flat-band voltage shift, is also indicated in Fig. 42.

If the gate voltage is negative, the charge transport phenomena will be quite different. The negative bias which causes accumulation of holes on the silicon surface will induce hole trapping near the anode, and the unlimited electron source at the cathode will supply electron injection. Since both carriers contribute to conduction in the nitride bulk, unless the charge transport kinetics reach an equilibrium state, a nonsaturated C-V shift is likely to occur.

5.1.3 Poly-Gate Capacitors

In modern VLSI technology, polysilicon has been adopted for many purposes, such as replacing the metal in device fabrication and use as a mask for self-alignment. When used as polysilicon gate devices, the polysilicon is assumed to be so heavily doped that it is degenerate and the Fermi level of the gate electrode is pegged at either of two band edges [41]. For the N+ poly-gate used in our devices, the Fermi level is so close to the silicon conduction band that the charge transport kinetics of the N+ poly-gate capacitors is similar to that of aluminum-gate capacitors. Figures 43 through 44 show C-V plots of SNOS capacitors with a 34 Å pad oxide and a 303 Å LPCVD nitride observed after negative current stress. In low level current stress, the C-V curves shift to the left as depicted in Fig. 43, while when stressed with a moderate current level (Fig. 45), the C-V curves shift to the right (Fig. 44). These results clearly indicated that both electrons and holes contribute to conduction current and the dominant trapping
Figure 43. HF C-V shift of N+ poly-gate capacitor, obtained after 0.2 nA negative constant current stress with different stress time.

Figure 44. HF C-V shift of N+ poly-gate capacitor, obtained after 60 nA negative constant current stress with different stress time.
Figure 45. Constant current stress V-t curves for N+ poly-gate capacitor
species is a function of the biasing amplitude.

The C-V plot used in explaining the charge transport mechanism under positive gate current stress is not available, due to the limitation of the constant current stress method and the material itself. As mentioned previously, the electron minority carrier density at a p-type silicon surface is small under positive current stress. The density will be further decreased at the oxide/nitride interface once electron tunneling occurs through the 34 Å oxide. Since small electron density corresponds to large resistance, a large gate voltage is required to maintain constant current. Therefore, dielectric breakdown is likely to happen even before the current is raised to the specified constant value. Nevertheless, a capacitor with pure nitride dielectric can be used to investigate the two-carrier transport model.

Illustrated in Figs. 46 and 47 are C-V plots of a p-type N+ poly-gate SNS capacitor. Under -40 nA stress, the curves shift to the left after 500 second stress and then gradually shift back, reaching saturation as stress time approaches 3000 second. The curve for -100 µA stress current indicates a completely different result. This different result is expected and can be explained as follows. Under low current stress the holes being injected into the nitride will initially stay near the injection interface. As time goes by, holes will propagate more deeply into the nitride. The small amount of electrons at the gate contact also penetrate into the nitride, resulting in a reduced flat-band voltage shift, as illustrated in Fig. 47. Since the negative current source at the gate electrode provides sufficient electrons during large current stress, unless trapped holes have a significant
Figure 46. C-V shift of N+ poly-gate capacitor with pure nitride dielectric under -100 nA constant current stress with different stress time.

Figure 47. C-V shift of N+ poly-gate capacitor with pure nitride dielectric under -40 nA constant current stress with different stress time.
concentration, the trapped electrons will dominate the net C-V shift as longer stress time will inject more charge and give a deeper electron distribution. Hence, the C-V characteristic keeps on shifting to the right, as shown in Fig. 46. This different trapping phenomena also appears in V-t curves, as shown in Fig. 48, where $V_g$ increases under low-field stress and decreases under high-field stress.

Similar arguments also apply to the N+ poly-gate SNS capacitors with n-type substrate. Figure 49 shows a C-V plot for a 280 Å nitride capacitor fabricated inside the N well of a CMOS device. Under positive current stress, carriers accumulating on the silicon surface are electrons, while at the gate electrode the positive voltage does not seem to have any significant contribution to hole injection from the N+ polysilicon. As a result, only electrons will propagate through the nitride from the gate; hence, a C-V plot will certainly indicate a right shift before the charge trapping reaches saturation. If the external current is high enough, hole injection is likely to occur as depicted in Fig. 50, where $V_g$ shows a decreased curve under high field stress. During high field stress, the localized electric field inside the nitride layer will be changed significantly due to the trapped electrons. The localized field will lower the energy barrier at the gate electrode and favor hole injection from the gate electrode. An example is shown in Fig. 51 for the case of constant voltage stress. Similar electric field redistribution has also been discovered and explained by the negative constant voltage stress I-t turnaround curve of the Au-gate capacitor [46].
Figure 48. Typical V-t curves of p-type N+ poly-gate SNS capacitor under negative current stress.
Figure 49. C-V shift of a N+ poly-gate capacitor with pure nitride dielectric under 100 nA gate bias
Figure 50. Typical V-t curves of n-type N+ poly-gate SNS capacitor under positive current stress.
Figure 51. Typical turnaround curve of a poly-gate capacitor with constant voltage stress
5.2 Constant Voltage Stress

In Section 5.1, a dual-carrier charge transport model was demonstrated with the aid of an energy band diagram and high frequency C-V and constant current measurement data. In this section, additional evidence of dual-carrier flow is presented using constant voltage stress measurement.

With constant voltage stress, the voltage between the anode and cathode has a fixed value but the electric field distribution along the dielectric bulk varies. For example, when a negative gate voltage is applied to a N+ poly-gate capacitor with p-type substrate, holes accumulate at the silicon/oxide interface and some of these will tunnel into the nitride. Based on Gauss's Law, the electric field at the hole trapping charge wavefront will be increased and electrons injected from the cathode tend to reduce the electric field at the nitride/gate interface. Since the total applied voltage $V$ is a constant, electric fields at the cathode and anode have to be lower than the average nitride field $E_{AVE}$ ($E_{AVE} = V/T_N$). A schematic illustration of the electric field distribution is shown in Fig. 52. A similarly shaped electric field distribution has been reported [46] for the space-charge free case. However, since the applied field does not need to be very large to cause two-carrier flow, a space-charge free region is therefore not necessary. If one-carrier flow dominates then the electric field at the cathode or anode does not need to be lower than $E_{AVE}$, as indicated in Figs. 53 and 54.
Figure 52. Schematic diagram of the electric field distribution with two-carrier charge trapping
Figure 53. Schematic diagram of the electric field distribution with hole trapping dominant

Figure 54. Schematic diagram of the electric field distribution with electron trapping dominant
The peak electric field resulting from two-carrier flow at the nitride bulk has been pointed out to be one possible factor contributing to dielectric breakdown [46]. Actually, the peak electric field is not necessarily caused by two-carrier flow. As Figs. 52 and 53 indicate, if the applied voltage is high enough, single-carrier flow will also form a peak electric field inside the dielectric bulk and will lead to dielectric breakdown. In Section 5.1, it was pointed out that under constant current stress, both electron and hole carriers participate in the charge trapping kinetics inside the nitride bulk. Unless one-carrier flow (usually holes) is purposely blocked to reduce the leakage current, the peak electric field at the nitride bulk would result from two-carrier flow. In the following discussion, both one-carrier and two-carrier charge trapping under constant voltage stress will be discussed.

5.2.1 Gold-Gate Capacitor

The tunneling probability of the carriers depends on the number of free carriers available, availability of trap sites, and the energy that the carriers possess. A negative bias does not favor electron injection from the gold gate; however, electrons can still be injected from the gate if the trapped hole at the anode can build up the field enough to lower the electron energy barrier [46]. The I-t curves in Fig. 55 indicated that the turnaround kinetics happened within a few seconds after the gate biasing started. Under moderate bias ($V_c = -15$ V), holes were trapped first and then electron injection started, resulting in a slow turnaround. At low field stress
Figure 55. I-t curves of the gold-gate capacitors with dielectric thickness of 20/206 Å under negative voltage stress
(V_o = -6 V), although electron current also participates in conduction, most of the trapped charge is holes. This conclusion is verified by a continuously decreasing I-t curve. The corresponding C-V plots are shown in Figs. 56 and 57. At V_o = -15 V, holes were trapped first, so that the C-V curve shifts to the left at 500 seconds. As time passes, electrons begin to be injected and now screen the effect of hole trapping, so that the C-V curves shift to the right as indicated in Fig. 56. When the gate bias reduces, hole trapping kinetics becomes the major current mechanism inside the nitride and the C-V curves keep on shifting to the left, as shown in Fig. 57. The C-V curves for the stressed samples shown in Figs. 56 and 57 show a change in the capacitance value. One possible reason for this decrease is that charges pileup at the gate/nitride interface, changing the effective dielectric thickness. But the main reason for this capacitance decrease is the effective gate area loss, resulting from air bubbles formed at the gate surface during electrical stress [46].

5.2.2 N⁺ poly-gate capacitor

Since the N⁺-poly gate has a Fermi energy level close to the aluminum Fermi level, the injection condition of the N⁺ poly-gate capacitor is similar to that of the aluminum-gate capacitor.

A positive gate bias does not seem to favor injection of either type of carrier. However, a high voltage gate bias will certainly produce significant band bending and cause carrier tunneling. Since electrons are the minority carrier at the p-type substrate, the tunneling phenomenon is not significant and the C-V shift is very small,
Figure 56. C-V plots of gold-gate capacitors with dielectric thickness of 20/206 Å under negative 15 V stress

Figure 57. C-V plots of gold-gate capacitors with dielectric thickness of 20/206 Å under negative 6 V stress
as illustrated in Fig. 58.

Under negative gate bias, tunneling of both kinds of carrier are likely to occur. However, under low-field stress holes tunnel more readily into the nitride. A possible reason for this effect is that the energy barrier to holes tunneling from band to band is 1.95 eV, slightly less than the 2.05 eV energy barrier height of electrons. The left shift C-V curve of Fig. 59 shows this effect. If the bias is very great, both carriers can be easily injected from both electrodes, but the right shift of the C-V curves indicates that electron trapping is dominant. A reduction of the hole trapping is due to the 30 Å oxide which might diminish the effective tunneling probability of the holes. Under moderate voltage stress both types of carrier participate in conduction. The turnaround curve at $V_g = -11$ V, shown in Fig. 60, clearly indicates this phenomenon.

5.3 Role of Thick Oxide in Nonvolatile Memory Devices

Oxide has been used as an insulator in IC fabrication for many years. The oxide layer can also be used as part of EPROM and EEPROM memory devices besides its many usages such as providing surface passivation, isolating one device from another, serving as a mask against implant or diffusion of dopant into silicon, acting as a component in MOS structures, and providing electrical isolation of multilevel metalization systems [82]. Since nitride has a large trapping density, a thick oxide on top of the nitride layer or within the nitride/silicon interface can serve as a good insulator, preventing leakage current through the nitride layer.
Figure 58. C-V plots of N+ poly-gate capacitors with dielectric thickness of 34/303/0 Å under 25 V stress

Figure 59. C-V plots of N+ poly-gate capacitors with dielectric thickness of 34/303/0 Å under -10 V stress
Figure 60. Typical I-t curves of N+ poly-gate capacitors with dielectric thickness of 34/303/0 Å under negative voltage stress
Shown in Fig. 61 are C-V plots of p-channel capacitors with a 280 Å nitride and 130 Å top oxide. Under positive gate bias, electrons will tunnel into the nitride layer on the silicon surface. However, if hole flow exists, then the shift of the C-V curve would be random. Whether the C-V curves shift to the right or left depends on the type of net trapped charge and charge centroid. We find an almost constant and positive C-V shift in Fig. 61, which indicates that hole injection from the gate electrode is unlikely to happen. Figure 62 illustrates an associated I-t curve for this case. The dramatic decrease of conduction current is due to the trapped electrons which shield the external electric field and reduce further electron injection. Similar curves also are observed for the 150 Å pad oxide case, as shown in Figs. 63 and 64.

5.4 In Search of the Clue

The experimental results described in Sections 4.1 to 4.3, represent a substantial effort to determine the trapping phenomena and explain two-carrier charge transport kinetics inside the nitride layer. It has been pointed out that the charge trapping condition depends on both the material and the gate bias, i.e., different polarities of bias current and different types of substrate will result in different trapping phenomena, as shown in Figs. 65 and 66. Even with the same type of substrate and thickness of the dielectric material, constant current and constant voltage stress do not give the same trapping results as shown in Figs. 67 and 68. By comparison of C-V curves of stressed samples with C-V curves of virgin devices, the net trapped
Figure 61. C-V plots of N⁺ poly-gate capacitors with n-type substrate and 0/280/130 Å dielectric thickness under 30 V stress

Figure 62. I-t curves of the n-type substrate N⁺ poly-gate capacitors with dielectric thickness of 0/280/130 Å under 30 V stress
Figure 63. I-t curves of the p-type substrate N⁺ poly-gate capacitors with dielectric thickness of 150/250/0 Å under -32 V stress

Figure 64. I-t curves of the p-type substrate N⁺ poly-gate capacitors with dielectric thickness of 150/250/0 Å under +32 V stress
Figure 65. C-V plots of n-type substrate N+ poly-gate capacitors with dielectric of thickness of 0/280/0 Å, taken after stress for 5000 second under different positive current stress.

Figure 66. C-V plots of p-type substrate N+ poly-gate capacitors with dielectric thickness of 0/280/0 Å, taken after stress for 5000 second under different negative current stress.
Figure 67. C-V plots of p-type substrate N+ poly-gate capacitors with dielectric thickness of 34/303/0 Å, taken after stress for 5000 second under different negative current stress.

Figure 68. C-V plots of p-type substrate N+ poly-gate capacitors with dielectric thickness of 34/303/0 Å, taken after stress for 5000 second under different negative voltage stress.
charge for both constant voltage and current stress can be determined and is listed in Table 6.

Since both carriers are injected at the same time, unless one carrier is purposely blocked, all effort to analyze the charge centroids and the trapping charges with numerical calculation would be very difficult.

In the above analysis, we did not consider interface charge or charge leakage. Leakage of trapped charge is a serious problem in memory devices, and some people believe the presence of charge leakage is due to the change of the interface traps [73]. Because interface charge easily tunnels into the nitride under high-field stress, it is difficult either to isolate the interface charge from the nitride bulk charge or to use charge pumping to measure the interface change of charge.

5.4.1 Flat-band voltage change under constant voltage stress

Charge redistribution inside the dielectric can cause error during the high frequency C-V measurement, which affects interpretation of the type of net trapped charge. Two factors cause this problem: first, trapped charge is not guaranteed to stay at the same location; secondly, back tunneling might change the trapping history of the trapped charge. Consequently, a C-V shift does not indicate the true concentration of the trapped charge due to the external stress. Nevertheless, the phenomenon of two-carrier charge trapping can also be demonstrated without performing any C-V measurement. The method of finding the flat-band voltage shift based on the I-V plot was developed by Chang [46].
### Table 6: Summary of charge trapping with both positive and negative bias

<table>
<thead>
<tr>
<th>Gate (Oxide/Nitride thickness (Å))</th>
<th>(+)bias</th>
<th>Net Trapping</th>
<th>(-)bias</th>
<th>Net Trapping</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Au</strong> (20/206, 20/295)</td>
<td>20 nA</td>
<td>e</td>
<td>-100 nA</td>
<td>h</td>
</tr>
<tr>
<td></td>
<td>10 V</td>
<td>h</td>
<td>-15 V</td>
<td>h</td>
</tr>
<tr>
<td></td>
<td>20 V</td>
<td>e</td>
<td>-6 V</td>
<td>e</td>
</tr>
<tr>
<td><strong>Al</strong> (20/206, 20/295)</td>
<td>20 nA</td>
<td>e</td>
<td>-20 nA</td>
<td>e → h</td>
</tr>
<tr>
<td></td>
<td>10 V</td>
<td>e</td>
<td>-17 V</td>
<td>e → h → e</td>
</tr>
<tr>
<td></td>
<td>20 V</td>
<td>h</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>N+-poly</strong> (34/303/0)</td>
<td></td>
<td>-0.2 nA</td>
<td>h</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>-60 nA</td>
<td>e</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>-50 μA</td>
<td>h</td>
<td></td>
</tr>
<tr>
<td></td>
<td>25 V</td>
<td>e</td>
<td>-10 V</td>
<td>h</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>-25 V</td>
<td>e</td>
</tr>
<tr>
<td><strong>(0/280/0)</strong></td>
<td></td>
<td>-40 nA</td>
<td>h</td>
<td></td>
</tr>
<tr>
<td></td>
<td>100 nA</td>
<td>e</td>
<td>-100 μA</td>
<td>e</td>
</tr>
<tr>
<td></td>
<td>18 V</td>
<td>h → e</td>
<td>-18 V</td>
<td>h</td>
</tr>
<tr>
<td><strong>(0/280/130)</strong></td>
<td>30 V</td>
<td>e</td>
<td>-30 V</td>
<td>h → e</td>
</tr>
</tbody>
</table>

*: n-type substrate
We adopt this idea in the following analysis; however, precise equations are presented for two-carrier charge injection.

Figures 69 and 70 show I-V relations for p- and n-channel SNS capacitors plotted using Poole-Fenkel coordinates. The normalized electric field in the nitride is defined by $E = \frac{V_g}{t_{eq}}$, where $V_g$ is the gate voltage and $t_{eq}$ is the equivalent oxide thickness, i.e. $t_{eq} = t_{ox} + (T_n \times e_{ox}/\varepsilon_n)$. For $I/E$ ranging from 100 to $10^6$ (pA/(MV/cm)), the curves exhibit a linear relationship. A linear Poole-Frenkel plot has also been reported in the literature [83]. The current has been attributed to the Fowler-Nordheim (F-N) mechanism at lower electric fields and changes to the Poole-Frenkel (P-F) mechanism at higher electric fields for stacked ONO dielectric devices. A similar Poole-Frenkel plot with current density as the y axis is shown in Fig. 71.

The empirical exponential relation

$$J = A \exp\left[\frac{B}{E}\right] \tag{5.8}$$

can be used to fit the J-E data. The constant $A$ is a function of the activation energy. By curve fitting, the constants $A$ and $B$ are found to be 0.014409 A/cm² and 6.7823 V/(cm/V) respectively. The average electric field can be found by subtracting the flat-band voltage and silicon surface potential from the gate voltage and is

$$E = \frac{(V_g - V_{FB} - \phi_s)}{t_{eq}} + \frac{Q_{ss}}{\varepsilon_{ox}} \tag{5.9}$$

Solving Eq. (5.8) for $E$ and substituting into Eq. (5.9) gives the flat-band voltage
Figure 69. Poole-Frenkel plots of I-V curves for p-channel SNS capacitors under both biasing polarities

Figure 70. Poole-Frenkel plots of I-V curves for n-channel SNS capacitors under both biasing polarities
Figure 71. Modified Poole-Frenkel plot for n-channel SNS capacitor under negative bias
\[ V_{FB} = V_0 + \left[ \frac{1}{B} \ln \left( \frac{J}{A} \right) \right]^2 T_s \] (5.10)

in which \( \phi_s \) and \( Q_{ss} \) are assumed negligible and \( J = I/\text{Area} \). Based on the above equation, the flat-band voltage can be directly calculated from the current density once the constants \( A \) and \( B \) are experimentally determined. An example of finding the flat-band voltage \( V_{FB} \) from the I-t data of a SNS capacitor is shown in Figs. 72 and 73. The I-t data shown in Fig. 72 were recorded during constant voltage stress with different voltage amplitudes. The average fields are -12.9 MV/cm, -10 MV/cm and -7.1 MV/cm respectively. The gate area of the devices is 1.22x10^{-2} cm^2. The I-t curve under -12.9 MV/cm stress indicates a fast decrease following a gradual increase in a standard turnaround two-carrier injection case. However, for -10 MV/cm and -7.1 MV/cm low-field stress cases, dual-carrier injection is not significant. In the transformed \( V_{FB} - t \) curves of Fig. 73, a decrease of the flat-band voltage at -12.9 MV/cm bias clearly indicates hole trapping. The gradual increase of the flat-band voltage also indicates electron injection after times larger than 200 seconds. The turnaround curve can not be observed at low-field stress cases, in which only hole injection can be detected. Although the data shown in Fig. 73 can not be used to distinguish trapped electrons from trapped holes, a turnaround \( V_{FB} \) curve is indeed evidence of two-carrier injection kinetics. Since the low field did not show electron injection, this means that the trapping phenomena is also gate-voltage dependent.
Figure 72. Typical I-t curves of the SNS capacitors under negative bias.
Figure 73. $V_{FB}$-t curves transformed from the I-t curves shown in Fig. 72
5.4.2 Effective charge change under constant voltage stress

The flat-band voltage can be written in terms of the total charge density and its centroid in the single-carrier trapping case. For charge trapping inside the nitride dielectric, since both carriers can be injected and stored, the complete expression for the flat-band voltage includes carrier charge densities \( Q_p \) and \( Q_n \) and charge centroids \( \bar{x}_p \) and \( \bar{x}_n \) for both holes and electrons and is given by

\[
V_{FB} = \frac{Q_{ss}}{\varepsilon_{ox}} - \frac{Q_p}{\varepsilon_n} (T_N - \bar{x}_p) + \frac{Q_n}{\varepsilon_n} \bar{x}_n
\]  

(5.11)

Combining Eqs. (5.8) and (5.9) and eliminating \( V_{FB} \) and \( Q_{ss} \) yields

\[
Q_p (T_N - \bar{x}_p) - Q_n \bar{x}_n = \varepsilon_n \left[ \phi_{ns} - V_{eq} - \frac{j}{B - 1} \ln \left( \frac{J}{A} \right)^2 \right]
\]  

(5.12)

A normalized charge \( Q_{eff} \) relating to the total charges and charge centroids of electrons and holes

\[
Q_{eff} = Q_p \left( 1 - \frac{\bar{x}_p}{T_N} \right) - Q_n \frac{\bar{x}_n}{T_N}
\]  

(5.13)

can be used to simplify Eq. (5.10). Again, Eqs. (5.10) and (5.11) can be used to find the effective charge if the I-t data are known. Shown in Fig. 74 is the associated \( Q_{eff} \) of Fig. 72. When the applied field is -12.9 MV/cm holes were injected into nitride first and then electron injection dominates the charge transport inside the nitride, as illustrated by the gradual shift toward the more negative \( Q_{eff} \) value. For the low-field stress cases, hole injection dominates the charge.
Figure 74. Effective charge calculated from the I-t data shown in Fig. 72.
transport, as indicated by the gradual increase of the positive $Q_{\text{eff}}$ in Fig. 74.

5.5 Analysis of constant current stress result

Shown in Figs. 75 through 78 are C-V curves of gold-gate MNOS capacitors with different nitride thickness. These curves were taken after constant current stress was applied for 600 seconds. The related V-t curves are shown in Figs. 79 to 82. Table 7 lists the change of the flat-band voltage in Figs. 75 to 78. The stressing currents were from -1 nA to -10 μA. The flat-band voltage shift $\Delta V_{FB}$ is plotted against the stress current $I$ and is shown in Fig. 83. For current less than 100 nA, each curve can be fitted with a straight line. The linear lines for small stressing currents confirm that holes dominate charge transport under low-level current stress for gold-gate MNOS capacitors [46]. While for current larger than 1 μA, electron current injected from gate electrode participates in the carrier flow and reduces the flat-band voltage shift. Consequently, the linear relationship between $\Delta V_{FB}$ and gate current $I$ can not be satisfied, as can be seen in Fig. 83.

In the analysis of hole flow in MNOS capacitors, Chang [46] indicated that the flat-band voltage shift can be expressed in terms of the nitride thickness $T_n$ by $\Delta V_{FB} = A(T_n - B)$, where $A$ and $B$ are constants. A plot based on the experimental data shown in Table 7 illustrates similar results when the current is less than 1 μA, as depicted in Fig. 84. The reason for this restriction is as follows: at low current stress, all the curves show a negative flat-band voltage shift, while
Figure 75. Typical C-V shifts of gold-gate MNOS capacitors with dielectric thickness O/N of 20/100 Å, obtained after constant current stress for 600 seconds.

Figure 76. Typical C-V shifts of gold-gate MNOS capacitors with dielectric thickness O/N of 20/200 Å, obtained after constant current stress for 600 seconds.
Figure 77. Typical C-V shifts of gold-gate MNOS capacitors with O/N of 20/300 Å, obtained after constant current stress for 600 seconds.

Figure 78. Typical C-V shifts of gold-gate MNOS capacitors with O/N of 20/400 Å, obtained after constant current stress for 600 seconds.
Figure 79. V-t curves for gold-gate MNOS capacitors with O/N of 20/100 Å

Figure 80. V-t curves for gold-gate MNOS capacitors with O/N of 20/200 Å
Figure 81. V-t curves for gold-gate MNOS capacitors with O/N of 20/300 Å

Figure 82. V-t curves for gold-gate MNOS capacitors with O/N of 20/400 Å
Table 7  Results of the flat-band voltage shift after 600 seconds current stressing for Au-gate devices

<table>
<thead>
<tr>
<th>Nitride (Current)</th>
<th>100 Å</th>
<th>200 Å</th>
<th>300 Å</th>
<th>400 Å</th>
</tr>
</thead>
<tbody>
<tr>
<td>-1 nA</td>
<td>-0.1067 V</td>
<td>-2.9227 V</td>
<td>-4.608 V</td>
<td>-7.0933 V</td>
</tr>
<tr>
<td>-10 nA</td>
<td>-0.5733 V</td>
<td>-2.9867 V</td>
<td>-4.736 V</td>
<td>-7.3067 V</td>
</tr>
<tr>
<td>-100 nA</td>
<td>-0.7333 V</td>
<td>-3.0293 V</td>
<td>-5.632 V</td>
<td>-7.4667 V</td>
</tr>
<tr>
<td>-1 µA</td>
<td>-1.1733 V</td>
<td>-2.8160 V</td>
<td>-4.800 V</td>
<td>-6.6667 V</td>
</tr>
<tr>
<td>-10 µA</td>
<td>-1.2 V</td>
<td>-1.8773 V</td>
<td>-3.904 V</td>
<td>-3.9467 V</td>
</tr>
<tr>
<td>-100 µA</td>
<td>--</td>
<td>-1.2800 V</td>
<td>--</td>
<td>--</td>
</tr>
</tbody>
</table>
Figure 83. Flat-band voltage shifts recorded after different current stressing
Figure 84. Flat-band voltage shifts versus nitride thickness
the less negative voltage shift at higher current stress indicates that electrons start to dominate the charge trapping. It seems that a parabolic equation is more appropriate to describe the relationship between the flat-band voltage shift and the nitride thickness, as shown in Fig. 84.

5.6 Numerical Simulation

For an arbitrary space charge distribution $\rho(x)$ within the dielectric, the flat-band voltage shift is given by

$$AV_{FB} = -\frac{1}{C_0} \left[ \frac{1}{d} \int x \rho(x) dx \right]$$  \hspace{1cm} (5.14)

where $x$ is measured from the metal/nitride interface, $C_0$ is the dielectric capacitance per unit area, and $d$ is the dielectric thickness.

Consider the negligible detrapping case of the dual-carrier charge transport inside the nitride layer, the flat-band voltage shift can be obtained by changing the coordinates of Eqs. (4.49) and (4.50) and substituting both equations into Eq. (5.14).

$$AV_{FB} = -\frac{1}{\varepsilon_N} \int_0^{T_N} x q \left[ \frac{N_{nt}}{r_p} \left( \frac{x-T_N}{\lambda} \right) - \frac{N_{pt}}{1-r_p} \left( \frac{T_N-x}{\lambda} \right) \right] dx$$

$$= \frac{q}{\varepsilon_N} \int_0^{T_N} x \left[ \frac{N_{nt}}{1 + \frac{r_p}{1-r_p} \frac{T_N-x}{\lambda}} - \frac{N_{pt}}{1 + \frac{1-r_p}{r_p} \frac{x-T_N}{\lambda}} \right] dx$$

$$\hspace{1cm} (5.15)$$
If we define a new function

\[ f(x) = x \left[ \frac{N_{nt}}{r_{po} \left( x - T_n \right) / \lambda} - \frac{N_{pt}}{1 + 1 - r_{po} \left( T_n - x \right) / \lambda} \right] \]

and a new variable

\[ h = T_n / 2 \]

the integral form of the flat-band voltage shift due to trapped charge in Eq. (5.15) can be solved using Simpson's composite rule [77], and is

\[ \Delta V_{FB} = \frac{q}{\epsilon_n} \frac{h}{6} \left[ f(0) + 4f\left(\frac{h}{2}\right) + 2f(h) + 4f\left(\frac{3h}{2}\right) + f(T_n) \right] \]

(5.16)

A typical plot of the \( \Delta V_{FB} \) with respect to different nitride thickness \( T_n \) and different hole current injection ratio \( r_{po} \) is depicted in Fig. 85, where the parameters: \( 1 \times 10^{-13} \) cm\(^2\) for the capture cross section, \( 9 \times 10^{18} \) cm\(^{-3}\) for \( N_{pt} \), \( 8 \times 10^{18} \) cm\(^{-3}\) for \( N_{nt} \), \( 7 \epsilon_o \) for the nitride dielectric constant, and 58.8235 \( \AA \) for the effective trapping depth \( \lambda \) have been chosen. Since the trapped charge distributions of \( p_t(x) \) and \( n_t(x) \) have the same shape as the current density distributions of \( J_p(x) \) and \( J_n(x) \), large \( r_{po} \) also imply higher \( p_t \) value near the anode, so that the flat-band voltage shift \( \Delta V_{FB} \) is negative, while for small \( r_{po} \), \( n_t \) becomes larger near the anode as compared to the \( n_t \) under large \( r_{po} \), hence, the effective \( \Delta V_{FB} \) becomes more positive.
Figure 85. Analytical solutions of the flat-band voltage shift versus different nitride thickness
For a gold-gate MNOS device with p-type substrate, the dominant hole flow is observed under negative gate bias, therefore, it is expected that $r_{po}$ will be very high. The analytical solutions with $r_{po}$ ranging from 0.9 to 0.98 are shown in Fig. 86, the parabolic shape of the curves confirm our theory that unless the charge transport is only due to one-carrier injection, it is not appropriate to assume a linear relationship between $AV_{FB}$ and $T_N$.

Since charge is also stored at the oxide bulk and at both silicon/oxide and oxide/nitride interface, a complete analytical solution of the $AV_{FB}$ for a MNOS capacitor has to include this oxide charge. If we assume that the interface charge is uniform across the oxide layer, the flat-band voltage shift due to this oxide charge can be expressed as

$$AV_{FB} = -\frac{1}{\varepsilon_{ox}} \int_{T_N}^{T_N+t_{ox}} \left[ x-T_N \left( 1 - \frac{\varepsilon_{ox}}{\varepsilon_N} \right) \right] \rho_{ox}(x) dx$$

$$= -\frac{qP_{ox}}{\varepsilon_{ox}} \left[ \frac{t_{ox}}{2} + T_N \frac{\varepsilon_{ox}}{\varepsilon_N} \right]$$  (5.17)

where $\rho_{ox} = q\rho_{ox}$. If we assume that $\rho_{ox} = 9 \times 10^{18}$ cm$^{-3}$, $\varepsilon_N = 7\varepsilon_o$, and the thin oxide of MNOS capacitor is 20 Å, the flat-band voltage shift due to the oxide charge is found to be: -1.943 V for 400 Å nitride, -1.478 V for 300 Å nitride, -1.0132 V for 200 Å nitride, and -0.5483 V for 100 Å nitride. The analytical solutions of the total flat-band voltage shift due to the trapped charge inside the oxide and nitride layers of MNOS devices are depicted in Fig. 87, which resemble the experimental results shown in Fig. 84.
Figure 86. Analytical solutions of the flat-band voltage shift versus different nitride thickness with higher $r_{po}$.
FLAT-BAND VOLTAGE SHIFT OF MNOS VS. NITRIDE THICKNESS

$\lambda = 58.82353 \text{ Å}$
$\sigma = 1 \times 10^{-13} \text{ cm}^2$
$\beta = 2.867 \times 10^{-4} \text{ J/V-cm}$
$N_{pt} = 9 \times 10^{18} \text{ cm}^{-3}$
$N_{nt} = 8 \times 10^{18} \text{ cm}^{-3}$
$\epsilon_n = \gamma\epsilon_0 = 6.195 \times 10^{-13} \text{ F/cm}$

Figure 87. Analytical solutions of the flat-band voltage shift for gold-gate MNOS capacitors
5.7 A Double Turnaround Curve

It has been established in Section 5.1 that the injection current is determined by the applied field. The conduction current through the dielectric may be hole current, electron current, or both. A turnaround curve is clear evidence of dual-carrier flow. Shown in Fig. 88 are the I-t curves of the gold-gate MNOS capacitors under negative voltage stress. The nitride thickness is 400 Å and the oxide thickness is 20 Å. A magnified plot of the curve at $V_g = -30$ V indicates a turnaround curve (Fig. 89), while the curve at $V_g = -25$ V indicates a double turnaround curve (Fig. 90), the first turnaround occurred at 20 seconds after stress began and the second turnaround occurred at a stress time equal to 60 seconds. Both a turnaround curve and a two-turnaround curve are clear evidence of dual-carrier flow. Since holes are not really injected from the substrate under negative bias, the current injection could be more complicate than we thought. A deeper consideration of this carrier injection is given in next chapter.
Figure 88. Typical I-t curves of gold-gate MNOS capacitors under negative voltage stress
Figure 89. Typical turnaround curve
Figure 90. Typical two-turnaround curve
CHAPTER 6

DISCUSSION

Charge transport kinetics inside thin silicon-nitride nonvolatile memory devices is a complex process and a true understanding is extremely difficult. This is not only because trapping and detrapping of trapped charges can vary both with time and position in the nitride film, but also because both electrons and holes participate in carrier transport inside the nitride. The charge centroid \( \bar{d} \) and the total trapped charge \( Q_t \) usually determined in the conventional one-carrier model can still be found for the two-carrier model. Nevertheless, to identify the hole and electron concentrations is almost impossible, as Eqs. (5.11) and (5.12) indicate that no obvious experimental method can be used to separate \( \bar{Q}_p \) and \( x_p \) from \( \bar{Q}_n \) and \( x_n \).

Charge trapping phenomena for memory devices with different structures under different biasing conditions have been introduced in Chapter 5. A detailed investigation of the dependence of electron and hole flow on the energy band diagram and the validity of the two-carrier model will be given in the following discussion. Furthermore, the time-dependent two-step dielectric breakdown resulting from the buildup of the localized peak electric field caused by charges trapped inside the dual dielectric will also be explored.
6.1 Electron and hole flow

For conduction current in a crystal, electrons can only contribute appreciably to conduction if there are available neighboring empty levels into which they can go [84]. When an electron is excited from a filled band to an empty band, the level occupied by the electron is left vacant, so that other electrons may move into it. In an applied electric field, the position left unoccupied moves in a direction opposite to that which an electron would move and so appears to have a positive charge. In the case of conduction inside a crystal with many impurities, electrons migrating from one atom to the next without energy change will correspond to the movement of a positive hole in the valence band. Meanwhile, an electron detached from a bond and placed on a distant impurity atom cloud will correspond to an electron in the conduction band. For both a pure crystal and a crystal with impurities, hole flow is induced from the migration or injection of the electrons, but physically the transport mechanism of "hole flow" does not exist. 

For Si$_3$N$_4$ dielectrics, several researchers [6], [73], [85] postulated that different trap levels reside in the forbidden energy band, but no physical explanation of the structure was given. In the study of defect and impurity states in silicon nitride, Robertsen [86] found that the Si-Si $\sigma$ state lies in the middle of the forbidden band and could be a long-time hole trap, while the silicon dangling bond lying just below the conduction band could act as a very efficient electron trap.

If we assume three trap levels inside the forbidden band [30], the energy band diagram, shown in Fig. 91, indicate the possible excitation
Figure 91. Energy band diagram and the possible electron injection paths
paths of electrons from lower to higher states. Also shown are the possible electron capture paths. However, electron migration at the same trap level is not included. Since the transition probability for each step is different, if there are more than three trap levels, the transition path would be very complicated. When an electron trap is occupied by an electron, it becomes negatively charged, and a positive C-V shift will indicate electron trapping. If an electron trap has positive charge by itself, the capture of an electron will neutralize the trap. When a neutral hole trap loses an electron it becomes positive and the C-V measurement indicates a negative shift. A strict distinction between electron current and hole current is almost impossible; but, if we define these two carrier flows based on the trap levels, then electron current can be defined as electron flow along the trap levels close to the nitride conduction band and hole flow as the current along the trap levels close to the nitride valence band.

6.2 Metal-gate MNOS devices

6.2.1 MNOS devices under positive bias

When a positive voltage is applied to an aluminum-gate capacitor, electrons will be emitted or migrate from the impurity valence band. If we assume a Poole-Frenkel conduction mechanism in the nitride, these valence band electrons will propagate through the nitride by electron-capture and electron-emission process. Since the positive bias will form an inversion layer at the p-type substrate, electrons accumulating on the substrate surface will contribute to the Poole-Frenkel conduction. If the applied bias is high enough, then the electrons in
the silicon valence band will also participate in the nitride conduction via energy trap levels at the silicon/nitride interface or the nitride bulk trap levels, which are at a tunneling distance from the silicon [37]. If the bias is not very high, then electrons in the silicon valence band do not contribute to the conduction current, as shown in Figs. 92 and 93, where gate current and substrate current do not show significant change under low reverse bias at the substrate. Movement of the valence band electrons will also cause positive trap charge. In order to distinguish between electron injection from the silicon substrate and electron emission from the impurity valence band, we consider carrier flow from the gate to be hole flow and that from the substrate surface as electron flow as indicated in Fig. 94. There are other types of tunneling [87] which can inject carriers into the nitride from the silicon interface. For example, trap-assisted tunneling, needing relatively small field to bring empty states at a remote energy within tunneling range is one example. Another example is Fowler-Nordheim injection, which is limited to the high-field stress case.

If the gate is gold, as shown in Fig. 94, less electron injection from the substrate is expected since the work function of gold is greater than that of aluminum. Comparison of Fig. 41 and Fig. 42 indicates that for gold-gate MNOS capacitors after the stress time is larger than 100 seconds less electrons would have been trapped by the nitride layer. Consequently, the rightward shift of the C-V curve due to electron injection is smaller than that of the aluminum-gate MNOS capacitors.
Figure 92. Typical I-V plot of the N+ poly-gate SONOS FET with variable reverse bias at substrate

Figure 93. Typical I-V plot of the N+ poly-gate SNOS FET with variable reverse bias at substrate
Figure 94. Energy band diagram of MNOS devices under positive bias
6.2.2 MNOS Devices under negative bias

Most authors agree that holes are the dominant charge carriers with negative gate polarity [31], [34]-[35], [37], [88]. Hole trapping phenomena with negative bias is observed in our experiments. The net positive C-V shift, indicating electron trapping, is also shown in Figs. 44, 46, 66, and 67 for negative current stress and Figs. 61, and 68 for negative voltage stress.

Two-carrier charge transport is the same as explained in Section 6.2.1. However, instead of being injected from the substrate, electrons are injected from the gate electrode and from the impurity valence band. Also, if the substrate is n-type silicon, part of the applied negative voltage drop appears across the depletion region of the silicon substrate, so the effective field across the dielectric is not as large. When a negative electric field is applied to the MNOS dielectric, some of the charge at the impurity valence band will be emitted. Both negative and positive trapped charges can be created. Also, electrons injection from the gate electrode will neutralize some of the positive trapped charge and increase the rightward shift of the C-V curves. With either p- or n-type substrates, the energy band diagram shown in Fig. 95 indicates that two-carrier injection is likely to occur. Consequently, it is not surprising to find that the direction of movement depends on which shift dominates. The turnaround I-t curve [46] for the gold-gate capacitor indicates that net positive charge is trapped first and then electrons start to be injected into the nitride. This is further evidence that the trapping phenomenon is really both two-carrier transport and also a time-dependent process.
Figure 95. Energy band diagram of MNOS devices under negative bias
Since the aluminum gate has a higher Fermi energy level than the gold gate, electrons at the aluminum contact would have larger probability of tunneling into the nitride. Hence, the flat-band C-V curve should indicate greater magnitude of rightward shift for the aluminum-gate capacitor under negative bias.

6.3 N+ poly-gate MNOS devices

6.3.1 Injection under positive bias

Like metal-gate capacitors, poly-gate devices show similar phenomena related to two-carrier charge transport. The only change is that polysilicon sitting between the nitride and the aluminum may change the injection carrier concentration at the nitride/poly interface and therefore change the carrier tunneling probability.

Shown in Fig. 96 is the energy band diagram of the poly-gate device under consideration. Because the Fermi level of aluminum is almost same as the polysilicon conduction band, if aluminum is used on metalization, under positive bias, minority carriers at the N+ poly/nitride interface will be repelled and electrons at the N+ poly start to flow towards the positive power supply. Meanwhile, injection of electrons from the substrate and the migration and emission of the valence band electrons from impurities will participate in the current conduction inside the nitride layer, causing both positive and negative charge trapping. However, electrons supplied from the substrate can easily be trapped so that the C-V curves indicate a toward right shift, besides some of the electrons will neutralize the positive trapped charge so that the negative C-V shift can not be observed, as shewn in
Figure 96. Energy band diagram of N+ poly-gate devices under positive bias
Fig. 49.

If the metalization is gold instead of aluminum, a Schottky barrier is formed at the polysilicon and metal interface and reduces electron flow into the gold contact. Nevertheless, current conduction and charge trapping phenomena inside the nitride layer should be the same if both the gold/SNOS and aluminum/SNOS devices have the same voltage across the SNOS layers.

6.3.2 Injection under negative bias

Figure 97 shows the energy band diagram of a N+ poly-gate capacitor with the aluminum contact having a negative bias voltage. With negative bias, most of the ionized charge of the highly doped impurities are repelled and accumulate at the nitride/poly interface. Some are emitted into the nitride. Although the electron concentration near the silicon surface is very large, this does not guarantee that the polarity of net trapped charge will be negative because hole injection from the gate electrode is also likely to occur, as indicated in Figs. 43 and 44. In fact, charge trapping does not only depend on the carrier concentrations near both sides of the dielectric layers, trap energy levels, available trapping sites, temperature, and fabrication process all are factors which will affect the trapping result.

Since the Schottky barrier between N+ poly and metal will be increased under negative bias, if gold is used as the metal contact, a higher accumulation of electrons at the nitride/poly interface might raise the electron trapping probability at the nitride bulk, but this is still not guaranteed.
Figure 97. Energy band diagram of N+ poly-gate devices under negative bias
6.4 I-V Asymmetry

For poly-silicon/nitride/silicon (SNS) devices, since the structure is symmetrical, conduction current through the dielectric under different polarities is expected to be similar. However, the conduction characteristics are not exactly the same. The asymmetrical I-V curve of dual dielectrics has been observed [15], [25], [89]-[90] and physically explained by Yau [80] using a dual-carrier model. However, the data used in Yau’s analysis was taken with thick oxide, dual-dielectric devices, in which one carrier is blocked or only partially permitted to flow by a thick blocking oxide. In the following discussion, we will focus on pure nitride dielectric devices, and both p- and n-channel transistors are employed. Test results are shown in Figs. 98 and 99. The voltage and electric field relationship used by Yau [80] is still valid as long as the gate voltage is high enough so that the voltage drop at the silicon is negligible for both accumulation and depletion cases. Without the oxide layer, if we assume that the interface charge is negligible, the equivalent nitride electric field \( E_{n\text{eq}} \) could be simplified to \( V_g/T_n \). Sample results of the I-V measurement for the 280 Å nitride SNS devices are given in Table 8.

From the data shown in Table 8, the \( +V_g \) fields for the nitride dielectric is higher than \( -V_g \) fields for the nitride, which is totally different from Yau’s [80] report where \( +E_{n\text{eq}} < -E_{n\text{eq}} \). We believe that these contradictory observations are a result of differences in the dielectric system. In Yau’s experiment hole carrier flow was blocked by the thick oxide; therefore, the carrier supply of the thick-oxide dual dielectric at the cathode and anode are different from that of the pure
Figure 98. I-V curves of n-channel poly-gate SNS transistor under both positive and negative gate bias
Figure 99. I-V curves of p-channel poly-gate SNS transistor under both positive and negative gate bias.
| $|I_g| (\text{A})$ | P-channel | N-channel |
|-------|--------|--------|
|       | $+V_g (\text{V})$ | $-V_g (\text{V})$ | $+V_g (\text{V})$ | $-V_g (\text{V})$ |
| 1E-13 | 4.95 | 3.31 | 6.31 | 2.96 |
| 1E-12 | 7.65 | 5.32 | 7.94 | 5.31 |
| 1E-11 | 9.19 | 7.26 | 9.47 | 7.35 |
| 1E-10 | 11.08 | 9.53 | 11.70 | 9.58 |
| 1E-09 | 13.38 | 12.19 | 14.5 | 12.25 |
| 1E-08 | 15.87 | 14.87 | 17.33 | 14.89 |
| 1E-07 | 18.29 | 17.36 | 20.22 | 17.39 |
| 1E-06 | 20.76 | 19.87 | 23.71 | 19.98 |
| 1E-05 | 22.96 | 22.21 | 29.32 | 22.38 |
| 1E-04 | 25.18 | 24.60 | - | 25.37 |
The result that $+V_g > -V_g$ can be explained using an energy band diagram. For n-channel devices, negative bias will cause accumulation on the silicon surface. Negative bias favors electron injection from the N+ poly gate. With two large carrier supplies, the conduction current can easily reach a specific value with smaller applied negative voltage. If the applied gate voltage is positive, minority carriers in the inversion layer can be supplied by the N+ drain and source diffusion. Since there is a work function difference, the absolute value of the positive voltage has to be larger than that of the negative voltage in order to have the same conduction current pass through the dielectric.

In addition, the I-V curves of the p-channel device shown in Fig. 99 indicates similar results. Under negative gate bias, the cathode at the gate can easily supply electrons to be injected from the gate into the nitride layer. If the gate bias is positive, the n well can supply substantial numbers of electrons from the substrate. Some of these will be injected into the dielectric. However, the injection conditions for positive and negative biases are different even with the same voltage. Consequently, a larger voltage is required for the positive bias to have the same specific current value.

6.5 Two components of tunneling current in SNS structures

In Section 6.4, the current-voltage asymmetry due to different current injection levels of holes and electrons has been discussed. In this section, the validity of the carrier type determined by
Ginovker's [27] method will be explored.

Typical step I-t curves for $I_p$, $I_n$, and $I_g$ are shown in Fig. 100, 101, and 102. On the one hand, minority carrier current is relatively close to the gate current when the silicon surface is inverted, as shown in Figs. 100 and 101. On the other hand, if the gate bias causes accumulation of the majority carriers on the silicon surface, the gate current will be close to either the substrate current or the drain diffusion current, as illustrated in Fig. 102. During surface inversion, current due to minority carriers is about four orders of magnitude larger than current due to the majority carriers, which has been reported [91] and is also verified here. Either majority or minority carriers dominate the current through the nitride layer. The gate current $I_g$ is the sum of the drain current $I_p$ plus the n-well current $I_n$, which is based on Kirchoff's current law, provided that there is no leakage current or current multiplication.

Figure 100 shows I-t plots of gate current $I_g$, drain current $I_p$, and substrate current $I_n$ of a p-channel SNSFET with -18 V negative bias. The gate current illustrates a turnaround curve, which has the same shape as indicated in Section 5.4 for p-type SNS capacitors and has been explained as dual-carrier flow. The $I_p$ drain current indicates a similar configuration, in which the negative sign of $I_p$ means that hole carriers are flowing out of the P+ drain diffusion. A detailed current distribution is shown in Fig. 103, where thermal electron-hole pair generation current $I_{pn}^b$, and the drain diffusion current $I_{pn}^h$ are registered by the drain current $I_p$, the electron charge that flows through the dielectric $I_e^*$ and the drain current $I_p$ are registered by
Figure 100. Typical transistor I-t curves of $I_o$, $I_N$, and $I_P$ recorded during negative 18 V stress
Figure 101. Typical transistor I-t curves of $I_g$, $I_m$, and $I_p$ recorded during negative 22.5 V stress.
Figure 102. Typical transistor I-t curves of $I_g$, $I_h$, and $I_p$ recorded during positive 18 V stress
Figure 103. Current distribution of p-channel test transistor circuit
the gate current $I_g$, and the substrate current $I_n$ is the sum of the electron charge that passes through the dielectric $I_g^*$ plus electron-hole pair generation current $I_{R}^*$. If the gate voltage is not as high as in Fig. 101, then when external bias is applied to the device some depleted valence band electrons recombined with holes at the silicon/nitride interface, because the depleted valence band electrons decreased in number during the constant voltage stress $I_p$ is reduced initially. As time goes by, trapped holes inside the dielectric enhanced the injection of electrons from the gate electrode, which also increase the hole recombination current at the silicon/nitride interface, so that $I_p$ increases gradually. Although the conduction current inside the nitride layer is the result of electron flow, most electrons passing through the interface and depletion region would be captured by electron traps. Furthermore, some electrons might be captured by defects or holes at the $n$ well before reaching the $N+$ contact. As a result, $I_n$ decreases. If the external bias is as high as indicated in Fig. 101, then the large external field will not only cause significant migration of valence band electrons, a large amount of electrons are also injected from the gate electrode into the nitride layer at the same time. The large recombination current at the silicon/nitride interface will increase the drain current $I_p$ significantly. Even though a lot of holes and electrons recombine inside the nitride layer, the surviving electrons that could contribute to $I_n$ increase in number. Hence, both $I_p$ and $I_n$ increase, as shown in Fig. 101. If the bias voltage becomes positive, both $I_p$ and $I_n$ will decrease, owing to a small change of the electron concentration at the silicon surface. An example is shown in Fig. 102.
From the above arguments we can conclude that the information received from the I-t curves is based on what happens at the silicon and dielectric interface, which does not represent what happens inside the nitride dielectric [37]. Hence, the conclusion of either hole or electron flow dominant the conduction current inside the nitride layer based on the experimental results using Ginovker's [27] method is somewhat unreliable.

6.6 Nitride breakdown

6.6.1 Breakdown Mechanism

As pointed out in Chapters 4 and 5, the peak electric field inside the nitride layer due to two-carrier trapped charges might be very high; therefore, during external stress, permanent damage is likely to occur if the peak electric field is larger than the dielectric strength. There are two methods of identifying breakdown paths through the dielectric. One technique involves smearing a liquid crystal on the dielectric surface of the poly-gate devices. The liquid crystal will reveal those points where abnormal heat is generated owing to the localized defect breakdown. Such points could also be identified by using gold as the gate metal [46]. Figure 104 shows a scanning electron microscope (SEM) micrograph of the cross section of a gold-gate MNOS capacitor. The destructive breakdown which forms bubbles on the metal-gate surface (Fig. 105) is clearly indicated. The material sitting on top of the two hillocks has been found to be gold by means of X-ray diffraction. Although some air bubbles may exist between the gold and the silicon-nitride layer, as illustrated in the transmission
Figure 104. SEM micrograph of the cross section of a gold-gate MNOS capacitor

Figure 105. Bubble formation at the surface of a gold-gate MNOS device
electron microscope (TEM) micrograph in Fig. 106, the material under the
two hillocks in the SEM micrograph implies that bubbles may not simply
form at the gold and silicon nitride interface. Therefore, it is
not appropriate to use gold for the self-healing technique in studying
dielectric breakdown. Damage under the gold indicates that the breakdown
phenomenon might occur at the silicon and dual-dielectric interface or
inside of the dual-dielectric bulk.

Two kinds of nitride breakdown are observed in thin oxide MNOS
capacitors: instantaneous breakdown and time-dependent breakdown. When
the applied voltage is so large that the electric field across the
dielectric is higher than the nitride dielectric strength, carrier
multiplication due to impact ionization will result in instantaneous
breakdown. Since both instantaneous and time-dependent breakdown can
happen at the same voltage level, we believe that instantaneous break­
down is a result of a bad metal contact, which reduces the effective
gate area, and hence, increases the injection current density and
causes impact ionization. Therefore, dielectric breakdown for devices
with good metalization contact should be time dependent.

Two commonly cited breakdown models used in explaining time-
dependent breakdown in SiO₂ are the critical charge model [39] and the
impact ionization model [40]. Under constant voltage stress both the
critical charge model and the impact ionization model can explain
breakdown in thin nitride dielectrics. Although dielectric breakdown
is mainly a high field phenomenon and the impact ionization model seems
inadequate to explain low-field thin-nitride wearout [46], the peak
electric field resulting from trapped charge might be very high and
Figure 106. TEM micrograph of the cross section of a gold-gate MNOS capacitor
impact ionization is then likely to occur even with low-field stress.

6.6.2 Two-Step MNOS Dual-Dielectric Breakdown

Dual-dielectric breakdown of thin-oxide MNOS devices involves a breakdown of silicon dioxide and silicon nitride. The major tunneling process in the nitride layer is via carrier hopping, in which the electric field for the Poole-Frenkel tunneling process does not need to be very high. On the contrary, the tunneling mechanism in the oxide layer is Fowler-Nordheim tunneling, so the electric field plays an important role [46] in oxide tunneling. Under high field stress, the electric field buildup at the oxide layer might be higher than the external field due to charge pileup at the interface. Impact ionization will easily cause oxide breakdown. In fact, if the breakdown occurs at the MNOS dual dielectrics, oxide breakdown should take place before nitride breakdown.

Although some of the charges that pileup at the oxide/nitride interface will tunnel into the nitride layer, they can easily pass through the nitride layer by trapping and detrapping without causing serious damage to the dielectric material. Hence, impact ionization is unlikely to happen at the nitride layer. However, since the external field is applied to both the oxide and the nitride layer, breakdown of the oxide layer will accordingly increase the effective field across the nitride. When the field is very high or is larger than the critical field of the nitride layer [30], [40] none of the charges can be trapped and a space-charge free region is formed at the nitride bulk [46], [92]. Therefore, Poole-Frenkel tunneling is unlikely to happen, and eventually
impact ionization will cause the nitride breakdown.

The two-step breakdown process in gold-gate MNOS capacitors under constant voltage stress is illustrated in Fig. 107. Here the first abrupt increase of the gate current at 3450 seconds corresponds to oxide breakdown and the second increase at 4070 seconds corresponds to nitride breakdown. A similar breakdown process also is observed for the constant current stress example shown in Fig. 108. Here the first decrease of the gate voltage with -140 \( \mu \)A bias at 160 seconds corresponds to oxide breakdown, and the second decrease of the gate voltage at 405 seconds corresponds to nitride breakdown. Since different biasing conditions will result in different charge distributions at the interface and bulk of the dual dielectrics, the two-step breakdown process may not be as significant as indicated in Fig. 107 where the external gate current is only -10 \( \mu \)A. One possibility for this phenomenon is that the breakdown took place at the same time for both dielectric layers.

The breakdown mechanism is mainly a material property of the dielectric, thus different gate materials should not affect the breakdown phenomena even though they do affect the charge transport kinetics inside the dielectric. If the gate is aluminum instead of gold, a two-step dielectric breakdown should also be observed. Test results indicating a two-step breakdown phenomenon for both gold- and aluminum-gate MNOS devices with dual-dielectric thickness of 20/387 \( \AA \) are shown in Fig. 109.

Since the breakdown phenomena might be associated with either a bad metal contact or a silicon defect breakdown, dual-dielectric
Figure 107. I-t curves showing typical two-step breakdown of a gold-gate MNOS capacitor.

Figure 108. V-t curves showing typical two-step breakdown of the gold-gate MNOS capacitors.
Figure 109. I-t curves showing typical two-step breakdown of both gold- and aluminum-gate MNOS capacitors
breakdown may not be the only reason for the occurrence of breakdown in MNOS capacitors. However, the patterns of two significant current jumps for all of the curves shown in Fig. 109 are fairly similar and the only explanation for this phenomenon is that the breakdown takes place at both the oxide and the nitride layers. As for the observed small variations along the I-t curves in the same figure, they result from defect breakdown at the silicon and dual dielectrics, which do not cause significant breakdown paths.
Chapter 7

Conclusions and Future Studies

Dual-carrier charge transport mechanism in thin nitride films has been experimentally demonstrated. Observations on electrical conduction and flat-band voltage shift are also interpreted with transport processes of electron and hole flows in thin nitride layer of MNS and MNOS devices. Further, both constant current and constant voltage stress were implemented as the major investigation tools for the charge transport kinetics. Analytical expressions are derived for the charge trapping properties of the nitride dielectric. Also, a steady-state, two-carrier charge transport model is developed for investigating the charge trapping mechanism inside the nitride layer. With the help of this model, an explanation has been proposed for the observed two-step breakdown behavior of MNOS dual-dielectric capacitors. These results are to be presented at the Fall 1986 Electrochemical Society meeting [93].

As a result of the experiments performed, the following conclusions can be drawn

a) Charge transport kinetics inside thin LPCVD nitride is actually a two-carrier flow mechanism.

b) Hole flow is actually induced by migration of valence-band electrons at the impurity trap levels or by injection of free
electrons from the gate electrode. Electron current is defined as carrier flow along the trap levels close to the nitride conduction band, and hole current is carrier flow along the trap levels close to the nitride valence band.

c) The type of the dominant charge carrier in silicon nitride nonvolatile memory devices is determined not only by the dielectric properties but also by the gate materials, the substrate types, the biasing polarities, and the biasing amplitudes.

d) Only when electrons are injected from the substrate do the experimental results reveal a net negative charge trapping, regardless of the substrate type. Otherwise, the net trapped charge can be either positive or negative, depending on the stress time and bias voltage.

e) Trapped electron and hole spatial distributions as well as the electric field distribution inside the nitride region of nonvolatile memory structures are modeled directly using basic differential equations governing carrier transport in the nitride dielectric material. From the calculated results, the trapped charge and electric field distribution as well as the charge centroid and flat-band voltage can be qualitatively and quantitatively determined.

f) The two-carrier trapped charge distribution causes a peak field to develop in the nitride film, which can be related to the onset of dielectric breakdown and damage in the device structures.
g) Since destructive breakdown of the nitride layer might result in a change of the dielectric structure and the bubbles formed at the gold-gate capacitor may not just be created between the gold and nitride interface, the purpose of using gold for self healing may not be appropriate.

h) A two-step dielectric breakdown of MNOS capacitors is proposed. Under high field stress the electric field built up at the oxide layer might be very high, so that impact ionization will cause oxide breakdown first. The breakdown of the oxide layer then increases the effective field across the nitride, and eventually this will result in nitride breakdown by impact ionization.

Several directions of further research are possible for improved understanding of charge transport properties and dielectric breakdown in thin silicon nitride films

1) The development of data sampling technique is clearly required, so that the trapping charges can be recorded from C-V measurements before back tunneling of the trapped charge occurs.

2) A detailed description of the charge transport formulation consisting of three or more impurity and defect trapping levels is desirable for understanding characteristics of nitride charge trapping.

3) Further study of the interface and thin oxide charge trapping properties is necessary to determine the precise mechanism of charge transport and dielectric breakdown of MNOS dual
4) A time dependent model is really needed, since the trapped charge concentration and position are time dependent, note Fig. 74, as well as all C-V shifts.

5) Additional work in the area of investigation of thin nitride dielectric breakdown employing scanning transmission electron microscope (STEM) appears to be promising.
APPENDIX A

GENERAL CASE OF DUAL-CARRIER FLOW

Since the electrical experiment will provide some macroscopic information but not the microscopic details, the theoretical derivation is certainly required to help understand the phenomenon of steady-state charge transport in the nitride dielectric. In this Appendix, certain assumptions will be made in order to obtain close form expressions for the two-carrier charge distribution.

Rewriting Eqs. (4.11) to (4.14) yields

\[ \frac{1}{q} \frac{dJ_p}{dx} + \frac{\sigma_p J_p}{q} (N_{p^t} - p_t) + \frac{\sigma_p J_n}{q} n_t = v_p \exp \left[ - \frac{q}{kT} (\phi_{p^t} - \beta/E) \right] p_t \] (A-1)

\[ - \frac{1}{q} \frac{dJ_n}{dx} + \frac{\sigma_n J_n}{q} (N_{n^t} - n_t) + \frac{\sigma_n J_p}{q} p_t = v_n \exp \left[ - \frac{q}{kT} (\phi_{n^t} - \beta/E) \right] n_t \] (A-2)

\[ \frac{\sigma_p J_p}{q} (N_{p^t} - p_t) = v_p p_t \exp \left[ - \frac{q}{kT} (\phi_{p^t} - \beta/E) \right] + \frac{\sigma_n J_n}{q} p_t \] (A-3)

\[ \frac{\sigma_n J_n}{q} (N_{n^t} - n_t) = v_n n_t \exp \left[ - \frac{q}{kT} (\phi_{n^t} - \beta/E) \right] + \frac{\sigma_p J_p}{q} n_t \] (A-4)

For these equations, we can also assume that the capture cross section and the attempt-to-escape frequency for electron and hole traps are
equal, i.e.

\[ \sigma_p = \sigma_n = \sigma \]
\[ \nu_p = \nu_n = \nu \]

When combining Eqs. (A-1) to (A-4), we obtain a relationship indicating that the spatial rate of change of the hole current is the reverse of the spatial rate of change of the electron current, which is the same as that of the electron and hole currents at the depletion region of the p-n junction, i.e.

\[ \frac{dJ_p}{dx} = - \frac{dJ_n}{dx} \quad (A-5) \]

With \( i = \exp(A_p) \) and \( j = \exp(A_n) \), Eqs. (A-1) to (A-4) can be further simplified to

\[ \frac{dJ_p}{dx} + \sigma J_p (N_p t - P_t) + \sigma J_p n_t = \frac{q \nu}{i} p_t \exp(B/E) \quad (A-6) \]

\[ - \frac{dJ_n}{dx} + \sigma J_n (N_n t - n_t) + \sigma J_n p_t = \frac{q \nu}{j} n_t \exp(B/E) \quad (A-7) \]

\[ \sigma J_p (N_p t - P_t) = \sigma J_p n_t + \frac{q \nu}{i} p_t \exp(B/E) \quad (A-8) \]

\[ \sigma J_n (N_n t - n_t) = \sigma J_n p_t + \frac{q \nu}{j} n_t \exp(B/E) \quad (A-9) \]
Rearranging Eq. (A-8) and substituting $J_n$ by $J_n = J - J_p$, $J_p$ can be expressed in terms of $p_t$ and $E$ as

$$J_p = \frac{p_t}{N_{pt}} \left[ J + \frac{q\nu}{\sigma i} \exp(B/E) \right]$$

(A-10)

From Eq. (A-10) the trapped hole charges can be expressed in terms of $J_p$ and $E$ as

$$p_t = \frac{J_p N_{pt}}{q\nu} \frac{\exp(B/E)}{J + \frac{q\nu}{\sigma i}}$$

(A-11)

$J_n$ can be interpreted as a function of $n_t$ and $E$ by rewriting Eq. (A-9) as

$$J_n = \frac{n_t}{N_{nt}} \left[ J + \frac{q\nu}{\sigma j} \exp(B/E) \right]$$

(A-12)

Since $J_p + J_n = J$, combining Eqs. (A-6) and (A-7) and solving for $n_t$ yields

$$n_t = \frac{J - J_p}{N_{pt}} \frac{p_t q\nu}{N_{pt} \sigma i} \exp(B/E)$$

(A-13)

$$n_t = \frac{\frac{J - J_p}{N_{pt}} N_{nt}}{q\nu \exp(B/E) + \frac{q\nu}{\sigma j}}$$

(A-14)

$n_t$ can also be found from Eq. (A-12) as
By plugging Eqs. (A-11) and (A-14) into Poisson's equation, the electric field distribution can be related to the hole current density as

$$\frac{dE}{dx} = \frac{q}{\varepsilon_n} \left[ \frac{J_{p,N_{pt}}}{q\exp(B/E)} - \frac{(J-J_p)N_{nt}}{q\exp(B/E)} \right]$$

(A-15)

Substituting Eqs. (A-11) and (A-14) into Eq. (A-6) yields

$$\frac{dJ_p}{dx} = \frac{\sigma J_p N_{pt}}{q\exp(B/E)} + \frac{\sigma J_p N_{nt}}{q\exp(B/E)} + \frac{q\exp(B/E)J_p}{i(J + \frac{q\exp(B/E)}{\sigma I}) - \sigma J_p N_{pt}}$$

$$- \frac{\sigma J_{nt}J_p}{q\exp(B/E)}$$

(A-16)

Equations (A-14) and (A-15) should be solved first in order to obtain trapped charge distribution. Since Eqs. (A-14) and (A-15) are two differential equations with two unknowns: $E(x)$ and $J_p(x)$. Numerical method using the Taylor polynomials [77] can be applied to find these two quantities, provided that the boundary conditions can be found experimentally. Once $J_p(x)$ and $E(x)$ are found, the trapped charge distribution can be obtained from Eqs. (A-11) and (A-14).
APPENDIX B

RELATION BETWEEN $\Delta V_g$ and $\Delta V_{FB}$ DURING CHARGE INJECTION

In the electrical stress experiments, charges are injected into the dielectric. The stored charge inside the dielectric not only causes a flat-band voltage shift, but alters the whole electrical system. A common question raised here is how to relate the field change to the flat-band voltage shift.

In the following discussion of the field change caused by charge trapping inside the MNOS dual dielectric, we derive the flat-band voltage change $\Delta V_{FB}$ and biasing voltage change $\Delta V_g$ by taking into account both the silicon/oxide, oxide/nitride interface charges and the bulk space charges of oxide and nitride layers. The terminologies along with their units used in this section are defined in Table 9.

Maes and Overstraeten [94] calculated the flat-band voltage shift as a result of the trapping electron concentration, but they did not consider the flat-band voltage change caused by the trapping of positive charges. Since nitride has the property of dual-carrier flow, the flat-band voltage should also include the effect of trapped hole charges.

If a negative voltage is applied to a p-channel MNOS capacitor, the flat-band voltage $V_{FB}$ will be [94]

$$V_{FB} = \Phi_{ns} - \frac{\bar{Q}_{ox} \epsilon_{ox} \epsilon_{n} \tau_{n}}{\epsilon_{ox}} - \frac{Q_p}{\epsilon_{n}} (T_n - x_p^-) + \frac{Q_n}{\epsilon_{n}} x_n^- \tag{B-1}$$
### Table 9 Definitions of variables and coefficients

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{FB}$</td>
<td>flat-band voltage shift (V)</td>
</tr>
<tr>
<td>$\phi_{ms}$</td>
<td>work function difference (V)</td>
</tr>
<tr>
<td>$\tilde{Q}_{ox}$</td>
<td>effective oxide charge at silicon/nitride interface (C)</td>
</tr>
<tr>
<td>$Q_{ox}$</td>
<td>oxide charge (C)</td>
</tr>
<tr>
<td>$t_{ox}$</td>
<td>oxide thickness (cm)</td>
</tr>
<tr>
<td>$T_N$</td>
<td>nitride thickness (cm)</td>
</tr>
<tr>
<td>$Q_p$</td>
<td>trapped hole charge inside the nitride (C)</td>
</tr>
<tr>
<td>$\tilde{X}_p$</td>
<td>charge centroid of trapped holes inside the nitride (cm)</td>
</tr>
<tr>
<td>$Q_n$</td>
<td>trapped electron charge inside the nitride (C)</td>
</tr>
<tr>
<td>$\tilde{X}_n$</td>
<td>charge centroid of trapped electrons inside the nitride (cm)</td>
</tr>
<tr>
<td>$\phi_s$</td>
<td>surface potential of silicon substrate (V)</td>
</tr>
<tr>
<td>$V_{ox}$</td>
<td>voltage cross the oxide layer (V)</td>
</tr>
<tr>
<td>$V_N$</td>
<td>voltage cross the nitride layer (V)</td>
</tr>
<tr>
<td>$\rho_p$</td>
<td>charge density of trapped holes inside the nitride (C/cm$^3$)</td>
</tr>
<tr>
<td>$\rho_n$</td>
<td>charge density of trapped electrons inside the nitride (C/cm$^3$)</td>
</tr>
<tr>
<td>$\tilde{Q}_{ox^o}$</td>
<td>oxide impurity charge (C)</td>
</tr>
<tr>
<td>$Q_p^o$</td>
<td>positive charge inside the nitride layer before stress (C)</td>
</tr>
<tr>
<td>$Q_n^o$</td>
<td>negative charge inside the nitride layer before stress (C)</td>
</tr>
<tr>
<td>$E_{si}(-t_{ox})$</td>
<td>substrate electric field at silicon/oxide interface (MV/cm)</td>
</tr>
<tr>
<td>$E_N$</td>
<td>electric field of the nitride layer (MV/cm)</td>
</tr>
<tr>
<td>$E_{ox}$</td>
<td>electric field of the oxide layer (MV/cm)</td>
</tr>
</tbody>
</table>
If the virgin device has a lot of impurities inside of the oxide/nitride interface and the bulk, we can express the flat-band voltage in terms of those impurities

\[ V_{FB}^0 = \phi_{ms} - \frac{Q_{ox}^o R_{ox}}{\varepsilon_{ox}} + \frac{Q_p^o x_p^o}{\varepsilon_n} + \frac{Q_n^o x_n^o}{\varepsilon_n} - \left( \frac{Q_{ox}^o + Q_p^o}{\varepsilon_n} \right) T_n \]  

(B-2)

The total voltage drop across the MNOS capacitor will be

\[ V_g = \phi_{ms} + \phi_b + V_{ox}(t) + V_n(t) \]  

(B-3)

During stress, the electric field at any point of the bulk nitride can be found in terms of the trapped charges

\[ \varepsilon_n E_n(x,t) = \varepsilon_{ox} E_{ox}(0,t) + \int_0^x \rho_p(x',t) dx' - \int_{T_n}^x \rho_n(x',t) dx' \]  

(B-4)

The voltage drop crossing the nitride layer is obtained by integrating Eq. (B-4)

\[ V_n(t) = \int_0^{T_n} E_n(x,t) dx \]

\[ = - \varepsilon_{ox} E_{ox}(0,t) - \frac{Q_p(t)}{\varepsilon_n} (T_n - x_p(t)) + \frac{Q_n(t)}{\varepsilon_n} x_n(t) \]  

(B-5)

where

\[ Q_p(t) = \left[ x_p(t) \right]^{-1} \int_0^{T_n} x_p(x,t) dx \]  

(B-6)

\[ Q_n(t) = \left[ x_n(t) \right]^{-1} \int_{T_n}^0 x_p(x,t) dx \]  

(B-7)
The voltage drop across the oxide layer can also be derived as a function of the oxide trapped charges. Since

$$\varepsilon_{ox} E_{ox}(x,t) = \varepsilon_{si} E_{si}(-t_{ox},t) + \int_{-t_{ox}}^{x} \rho_{ox}(x,t) \, dx \quad (B-8)$$

then

$$V_{ox}(t) = - \int_{-t_{ox}}^{0} E_{ox}(x,t) \, dx = - E_{si}(-t_{ox},t) \frac{\varepsilon_{si}}{\varepsilon_{ox}} t_{ox} - \frac{\tilde{Q}_{ox}(t)}{\varepsilon_{ox}} \quad (B-9)$$

where

$$\tilde{Q}_{ox}(t) = \left(t_{ox}\right)^{-1} \int_{-t_{ox}}^{0} x \rho_{ox}(x,t) \, dx \quad (B-10)$$

We can further assume $\tilde{Q}_{ox}(t)$ includes interface charge $Q_{it}$ and the fixed charge $Q_{f}$ as well. Substitution of equations (B-5) and (B-9) into (B-3) gives

$$V_{o}(t) = \Phi_{ms} + \phi(t) - E_{si}(-t_{ox},t) \frac{\varepsilon_{si}}{\varepsilon_{ox}} t_{ox} - \frac{\tilde{Q}_{ox}(t)}{\varepsilon_{ox}}$$

$$- E_{ox}(0,t) \frac{\varepsilon_{ox}}{\varepsilon_{n}} Q_{p}(t) - \frac{Q_{n}(t)}{\varepsilon_{n}} x_{p}(t) - \frac{Q_{n}(t)}{\varepsilon_{n}} x_{n}(t) \quad (B-11)$$

Since

$$\varepsilon_{ox} E_{ox}(0,t) = \varepsilon_{si} E_{si}(-t_{ox},t) + Q_{ox}(t) \quad (B-12)$$

where

$$Q_{ox}(t) = \int_{-t_{ox}}^{0} \rho_{ox}(x,t) \, dx$$
Equation (B-11) can be summarized as

\[ V_g = \Phi_{ms} + \Phi_s(t) - \left( \frac{\varepsilon_{ox}}{\varepsilon_{ox}} E_{ox}(0, t) - Q_{ox}(t) + \tilde{Q}_{ox}(t) \right) \frac{t_{ox}}{\varepsilon_{ox}} \]

\[ \quad - E_{ox}(0, t) \frac{Q_p(t)}{E_n} - \frac{Q_n(t)}{E_n} (T_N - \bar{x}_p(t)) + \frac{Q_n(t)}{E_n} \overline{x}_N(t) \]  \hspace{1cm} (B-13)

For the flat-band condition \( E_{G1}(-t_{ox}, t) = 0 \) and \( \Phi_s(t) = 0 \), so that

\[ Q_{ox}(t) = \frac{\varepsilon_{ox} E_{ox}(0, t)}{\varepsilon_{ox}} \]

Under such condition Eq. (B-13) reduced to

\[ V_{FB} = \Phi_{ms} - \frac{\tilde{Q}_{ox}(t)}{\varepsilon_{ox}} - \frac{Q_{ox}(t)}{E_n} T_N - \frac{Q_p(t)}{E_n} (T_N - \bar{x}_p(t)) + \frac{Q_n(t)}{E_n} \overline{x}_N(t) \]  \hspace{1cm} (B-14)

Rearranging Eq. (B-11) yields

\[ V_g(t) = \Phi_{ms} + \Phi_s(t) - \left( \frac{\varepsilon_{ox}}{\varepsilon_{ox}} E_{ox}(0, t) - \frac{Q_{ox}(t)}{E_n} T_N \right) \frac{t_{ox}}{\varepsilon_{ox}} \]

\[ \quad - E_{ox}(0, t) \frac{Q_p(t)}{E_n} - \frac{Q_n(t)}{E_n} (T_N - \bar{x}_p(t)) + \frac{Q_n(t)}{E_n} \overline{x}_N(t) \]  \hspace{1cm} (B-15)

Combining equation (B-14) and (B-15) gives

\[ V_g(t) - V_{FB}(t) - \Phi_s(t) \]

\[ = - E_{ox}(0, t) \left[ \frac{t_{ox}}{E_n} + \frac{T_N}{E_n} \right] + \frac{\tilde{Q}_{ox}(t)}{\varepsilon_{ox}} t_{ox} + \frac{Q_{ox}(t)}{E_n} T_N \]  \hspace{1cm} (B-16)
For a small variation of the gate voltage change caused by the trapped charges, Equation (B-16) can be expressed as

\[ 
\Delta V_g(t) - \Delta V_{gb}(t) = - \Delta E_{ox}(o,t) \left[ \frac{\varepsilon_{ox}}{t_{ox} + \frac{T_n}{\varepsilon_n}} \right] + \frac{\Delta Q_{ox}(t)}{\varepsilon_{ox}} t_{ox} + \frac{\Delta Q_{ox}(t)}{\varepsilon_{ox}} T_n 
\]

(B-17)

where the surface potential change can be neglected for the accumulation condition. Therefore, \( \Delta \Phi_s = 0 \).

Since the oxide bulk will trap some charge, thick oxide (\( \geq 30 \, \text{Å} \)) and thin oxide (\( \leq 30 \, \text{Å} \)) layers will cause different change of \( \Delta V_g \).

1) For thick oxide MNOS devices:

During charge injection, some charges will be trapped inside the oxide, hence

\[ \Delta Q_{ox}(t) \neq 0, \Delta Q_{ox}(t) \neq 0 \text{, and } \Delta E_{ox}(o,t) \neq 0 \]

Equation (B-17) yields

\[ \Delta V_g(t) = \Delta V_{gb}(t) - \Delta E_{ox}(o,t) \left[ \frac{\varepsilon_{ox}}{t_{ox} + \frac{T_n}{\varepsilon_n}} \right] + \frac{\Delta Q_{ox}(t)}{\varepsilon_{ox}} t_{ox} + \frac{\Delta Q_{ox}(t)}{\varepsilon_{ox}} T_n \]

(B-18)

2) For thin oxide MNOS devices:

For thin oxide devices, charges will easily be injected from the silicon substrate through the oxide into the nitride layer by direct tunneling. Thus, we can assume that the charge distribution remains at the same value and is uniformly distributed inside of the oxide, so that
\[ \Delta Q_{ox}(t) = 0, \Delta Q_{ox}(t) = 0, \text{ and } \Delta E_{ox}(o,t) = 0 \]

Equation (B-17) yields

\[ \Delta V_{g}(t) = \Delta V_{FB}(t) \quad (B-19) \]

i.e., during constant current stress, the change of the flat-band voltage shift resulting from trapped charge can be found directly from the gate voltage change.
REFERENCE


45. Motorola Corp., Austin, Texas.


77. R.L. Burden et al., NUMERICAL ANALYSIS, second edition.


84. R.A. Smith, SEMICONDUCTORS, 1959.


