ELECTRICAL CHARACTERISTICS OF THE
SILICON NITRIDE-GALLIUM ARSENIDE INTERFACE

DISSERTATION

Presented in Partial Fulfillment of the Requirements for
the Degree Doctor of Philosophy in the Graduate
School of the Ohio State University

By

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* * * * * *

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CHAPTER I.

INTRODUCTION

In the rapid advance of the semiconductor industry over the last two decades, silicon has emerged as the most important material. Silicon can be purified to a very high degree by relatively simple methods so that high purity material is readily available at low cost. In the 1960's the III-V compounds have attracted increased attention. Of these materials gallium-arsenide (GaAs) is the most serious competitor to silicon. The major advantages of GaAs over silicon as a transistor material are:

1. greater energy gap allowing operation at higher temperatures,
2. high electron mobility giving theoretically higher frequency response, and
3. a direct band gap providing much shorter recombination time.

The materials technology of GaAs is, however, much more difficult than silicon. Because of the volatility of arsenic from the compound, refinement is much more difficult than for the elemental semiconductors. Only recently has such new technologies as liquid encapsulation [34] been developed. It is to be expected that as research and development continue on this important material high purity, economical substrates will be achieved.
Hand-in-hand with the predominate use of silicon as a transistor material has been the great utilization of silicon dioxide (SiO$_2$) as a dielectric, insulating, and passivating material. This is, of course, a natural consequence of the ease by which silicon dioxide can be thermally grown on silicon. SiO$_2$ has been, moreover, effective as an impermeable diffusion mask for the impurities commonly employed to dope silicon devices.

In the metal-oxide-silicon (MOS) technology the SiO$_2$-Si interface has been widely studied, and the successful solution of surface state and ionic contamination problems has resulted in the rapid growth of this technology.

As important as silicon and silicon dioxide have been and remain to be today, these materials have some obvious limitations particularly in the area of surface field effect transistors (FETs). The following formulae hold for these devices in the linear region [40]:

\[
I_D = \frac{W}{L} \mu C_{ins} \left[ V_G - V_T \right] V_{DS} \quad (1-1)
\]

\[
g_m = \frac{W}{L} \mu C_{ins} V_{DS} \quad (1-2)
\]

\[
f_o = \frac{\mu V_{DS}}{L^2} \quad (1-3)
\]

where $I_D$ is drain current; $g_m$ is the transconductance; $f_o$ is the maximum frequency of operation; $W$ and $L$ are channel width and length respectively; $C_{ins}$ is the capacitance of the gate insulator.
per unit area; $V_G$ is the gate voltage; $V_T$ is the threshold voltage; $V_{DS}$ is the drain to source voltage; and $\mu$ is the effective channel mobility.

In order to maximize $I_D$, $g_m$, and $f_o$, it is desirable to have the largest possible value of $\mu$. The value of $\mu$ depends on the mobility, $\mu_b$, of the bulk substrate material — being always less than $\mu$ because of surface scattering. The value of $\mu$ is typically one half that of $\mu_b$. It is obvious then that GaAs with its high electron mobility is potentially a better substrate material for FETs than silicon. With MOS digital integrated circuits commonly used in today's technology, for example, logic speeds are limited by the RC time constants resulting from channel resistance and node capacitance. A GaAs n channel FET could operate, therefore, at speeds approaching twenty times that of the comparable p channel MOS-FET now being used.

Concerning silicon dioxide, there are limitations to its effectiveness as a passivating layer. It is not as impermeable to such contaminants as sodium, water, and oxygen as would be desired. $SiO_2$ also fails to mask many important diffusants such as zinc and gallium. For these reasons there has recently been a great deal of attention [1-33] focused on amorphous silicon nitride ($Si_2N_x$) as a passivating and masking film partly or fully replacing silicon dioxide. Silicon nitride is much more impervious to diffusants of all kinds than silicon dioxide. For example, 2000 Å of thermally grown $SiO_2$ does not mask Ga, while
1000 Å of Si$_3$N$_4$ completely masks Ga at 1100°C for many hours [22]. In addition, the use of silicon nitride as an insulator in a metal-nitride-semiconductor (MNS) FET increases the transconductance and drain current compared to SiO$_2$ by 50% because of its higher dielectric constant.

The above discussion hopefully has lead the reader to the conclusion that a GaAs FET utilizing silicon nitride as the gate insulator would have considerable advantage over the MOS-FET. Before such an MNS FET can be realized, however, a great deal of investigation into the Si$_3$N$_4$-GaAs interface must be made.

It is the purpose of this work to investigate and characterize the Si$_3$N$_4$-GaAs interface with particular attention to those properties which would affect the achievability of a GaAs MNS-FET. The Si$_3$N$_4$ films are pyrolytically deposited from SiH$_4$ (silane) and NH$_3$. The GaAs is <111> plane. Major emphasis is placed on p material since an n channel enhancement-mode device would be desired to utilize the high electron mobility of GaAs.

Since this research is to invade an area of which very little is known, the goal is to investigate major parameters such as flat-band voltage, time constants of trapped charge, impurity redistribution, effects of ionic charge, in an effort to see how these may be affected by processing techniques. More particularly it is hoped that information gained herein of the Si$_3$N$_4$-GaAs interface will help clear the way to fabrication of practical metal-nitride-semiconductor (MNS) FETs on GaAs substrates for use as logic gates.
and/or bistable memory elements. It has been reported, for example, that there is a hysteresis effect in the Si$_3$N$_4$-Si system [16]. This effect is also present in the Si$_3$N$_4$-GaAs system, and receives much of the attention of this work.

The metal-insulator-semiconductor (MIS) capacitor was used as the principal device for this investigation. The presence of hysteresis effects with trapping of charge in the insulator necessitates that this C-V data be taken very carefully to give meaningful results. Surface state densities for the best p and n type samples are given.
CHAPTER II.

MIS CAPACITANCE THEORY

It has long been realized that the metal-insulator-semiconductor (MIS) structure is a powerful research tool in the study of semiconductor surfaces. The capacitance versus bias (C-V) characteristics of these devices contain information about substrate doping; ionic charge present; density and frequency response of surface states; and the presence and nature of traps near the insulator-semiconductor interface.

The theory of MIS capacitors has been presented by many authors [43-44], and hundreds of articles have been written on the metal-insulator-semiconductor system. An extensive bibliography has been given by E. S. Schlegal [41-42]. Only a brief review of MIS capacitor theory is presented here with the aim of establishing the notation and emphasizing that part of the theory that is especially important in interpreting the experimental results of the MIS, metal-nitride-gallium arsenide (semiconductor), capacitors to be presented.

Figure 1 shows a schematic representation of a MIS capacitor, and Figure 2 shows the energy band diagram for a MIS capacitor with p type semiconductor and a positive voltage applied to the metal field plate. It is assumed throughout this work that the
FIGURE 1. SCHEMATIC REPRESENTATION OF AN MIS CAPACITOR
FIGURE 2. BAND DIAGRAM OF MIS CAPACITOR WITH P TYPE SEMICONDUCTOR AND POSITIVE APPLIED VOLTAGE.
semiconductor is held at reference (ground) potential. In Figure 2:

\[ \begin{align*}
V & = \text{total applied voltage} \\
\phi_m & = \text{metal work function} \\
V_{\text{ins}} & = \text{voltage drop across the insulator} \\
\chi_{\text{SC}} & = \text{electron affinity of the semiconductor} \\
\psi_S & = \text{surface potential} \\
\psi_F & = \text{potential of the Fermi level}
\end{align*} \]

Although Figure 2 is referred to as an energy diagram, it is common to also label potentials on the diagram - it being understood that the energy is given in electron volts.

A very simple and powerful expression relating capacitance to voltage for the MIS structure can be found from Gauss's law:

\[ -Q_{\text{tot}} = \varepsilon_{\text{ins}} E_{\text{ins}} = \varepsilon_{\text{ins}} \frac{(V - \psi_S)}{d} = C_{\text{ins}} (V - \psi_S) \quad (2-1) \]

where \( C_{\text{ins}} \) is the insulator capacitance per unit area and \( Q_{\text{tot}} \) is the total charge per unit area in the semiconductor or near the interface, and \( \varepsilon_{\text{ins}} \) is the dielectric constant of the insulator. The differential capacitance is

\[ C = -\frac{dQ_{\text{tot}}}{dV} = C_{\text{ins}} (1 - \frac{d\psi_S}{dV}) \quad (2-2) \]

Equation (2-2) shows that the capacitance is determined completely by \( C_{\text{ins}} \) and by the manner in which the surface potential changes with a change in applied voltage.
\( \psi_s \) results from bending of the energy bands in the semiconductor near the insulator-semiconductor interface. This bending of the bands is required so that charge is available to satisfy Gauss' law, i.e., to terminate (begin) the electric field. Under the action of an ac test signal this charge must adjust at the frequency of the test signal. Under those conditions where very little band bending is required to provide (or remove) a large number of charge carriers the surface potential changes very little and

\[
\frac{d\psi_s}{dV} = 0
\]

so that

\[ C = C_{\text{ins}} \]

This is, of course, the situation existing when the insulator is sandwiched between two metal plates. It is also the situation existing in the MIS structure for strong accumulation or for inversion when minority carriers can respond to the signal. In the presence of a large depletion region, however, \( \psi_s \) must change a relatively large amount to accommodate the termination of the electric field so that \( \Delta\psi_s \) may be comparable to \( \Delta V \) or

\[
\frac{d\psi_s}{dV} \rightarrow 1
\]
and \( C \) goes to a very small value. This is the situation in inversion at high frequencies (i.e., when the minority carriers cannot follow the signal). Equation (2-2) thus predicts the general form of the familiar high and low frequency C-V curves. Only high frequency curves are to be used in this investigation. Figure 3 shows a theoretical C-V curve for a p substrate with the accumulation, depletion and inversion regions indicated. It is assumed that \( \Phi_{MS} \) is zero.

Implicit in the above discussion is the fact that charge required to terminate the electric field exists only in the semiconductor. It is quite possible, however, that interface states also enter into the process. By "interface states" is meant those states at the interface or in the insulator near the interface which can communicate with the semiconductor at the frequency of the test signal. To the extent that these states can exchange charge in response to the applied ac signal, charge in the semiconductor need adjust a lesser amount. Again Equation (2-2) gives qualitatively the effect such states will have on the C-V curves. If the interface states can respond (i.e., exchange charge across the interface) at the test frequency \( \frac{d\psi_s}{dV} \) will be less than if the states could not respond and the value of the C at any voltage where \( \frac{d\psi_s}{dV} \) is important will be larger than the value obtained at a frequency sufficiently high that no states can follow. This is shown in Figure 4, where the lower curve (\( f^* \)) is the true high frequency curve. In the region of
Figure 3. Theoretical C-V Curve for P Substrate.
FIGURE 4. C-V CURVES AT THREE FREQUENCIES SHOWING EFFECT WHEN SURFACE STATES CAN FOLLOW SIGNAL

$\frac{f_3}{f_2} > f_1$

Normalized Capacitance

Negative Bias  0  Positive Bias
strong accumulation the presence of interface states can have little effect since $\frac{d\psi_S}{dV}$ is already very small.

From the above discussion it is clear that to use a high frequency C-V plot to evaluate a MIS structure the frequency must not only be sufficiently high that the minority carriers cannot follow the signal, but so high that the "fast" interface states cannot follow the signal. In the case of silicon dioxide grown thermally on silicon this effect is often unnoticed, since the interface states generally do not follow typical test frequencies in the 10 KC to 100 KC range. When the insulator is deposited pyrolytically, however, there may be a large density of "fast" interface states as will be seen in the experimental data which follows. It is necessary, therefore, in taking a C-V plot to check the curve at higher frequencies to insure that the fast states are truly "frozen out."

Although a family of C-V curves at different frequencies such as depicted in Figure 4 gives some qualitative information as to the frequency response of the fast states present, it is not possible to determine in a direct manner the density of surface states as a function of frequency (i.e., the density of states having response as fast as a given frequency). This can be seen by further development of Equation (2-2). First, rewriting (2-2) in the form:

$$C = C_{ins} \left(1 - \frac{1}{\frac{d\psi}{dV}}\right)$$  \hspace{1cm} (2-3)
and neglecting the metal-semiconductor work function difference, the applied voltage \( V \) can be written

\[
V = \psi_S + V_{SS} + V_{SC}
\]  

(2-4)

where

\[
V_{SS} = \frac{Q_{SS}}{C_{ins}} \quad \text{and} \quad V_{SC} = \frac{Q_{SC}}{C_{ins}}
\]

are the voltage equivalents of the charge in the surface states and in the semiconductor, respectively. In other words, \( V_{SS} \) and \( V_{SC} \) represent the integral of the electric field in the insulator which terminates (begins) on charge in surface states and in the semiconductor, respectively. Combining (2-3) and (2-4) gives

\[
C = C_{ins} \frac{\frac{dV_{SC}}{d\psi_S} + \frac{dV_{SS}}{d\psi_S}}{1 + \left( \frac{dV_{SC}}{d\psi_S} \right) + \left( \frac{dV_{SS}}{d\psi_S} \right)}
\]

(2-5)

The theoretical differential capacitance could be calculated from (2-5) if \( V_{SC} (\psi_S) \) and \( V_{SS} (\psi_S) \) were both known. Although \( V_{SC} (\psi_S) \) can be found by applying Poisson's equation to find \( Q_{SC} (\psi_S) \), \( V_{SS} \) as a function of \( \psi_S \) cannot be found directly since the energy distribution and the effective capture cross section of the surface states are unknown. If, however, the surface states cannot follow the applied signal, (2-5) reduces to the familiar form
or replacing \( V_{SC} \) by \( \frac{Q_{SC}}{C_{ins}} \) yields the equivalent form

\[
C^\infty = C_{ins} \frac{\frac{dV_{SC}}{d\psi_S}}{1 + \frac{dV_{SC}}{d\psi_S}}
\]

\[
(2-6)
\]

\[
C^\infty = C_{ins} \frac{\frac{dQ_{SC}}{d\psi_S}}{C_{ins} + \frac{dQ_{SC}}{d\psi_S}}
\]

\[
(2-7)
\]

\( Q_{SC} \) as a function of \( \psi_S \) can be found by solving Poisson's equation, and since \( C_{ins} \) can be measured in strong accumulation, the theoretical high frequency C-V plot can be found [43-44].

Since a large number of samples were to be evaluated in this investigation, a computer program was written. The steps followed are outlined in the Appendix.

In general, the experimental C-V curve will not coincide with the theoretical curve. The displacement \( \Delta V \) (see Figure 5) between the two curves for a particular value of \( C \) indicates the total charge present near the insulator-semiconductor interface exclusive of \( Q_{SC} \). If \( \Delta V \) is equal for all values of \( C \) (hence, all values of \( \psi_S \)) the experimental curve is merely a translation of the theoretical curve. A shift of this type can be caused by a difference in metal-semiconductor work function, \( \phi_{MS} \), or by the presence of charge which is independent of \( \psi_S \), such as metal ions which are ionized for all values of \( \psi_S \). If there are
FIGURE 5. DISPLACEMENT BETWEEN EXPERIMENTAL AND THEORETICAL C-V CURVES.
surface states present, moreover, the experimental curve will be
distorted such that the offset $\Delta V$ is not the same for all values
of $C$ (or $\psi_S$). If the total apparent charge present as a function
of $\psi_S$ is found and this relationship is differentiated with
respect to $\psi_S$, the result is the equivalent surface state charge
density (coulombs per unit area per unit voltage) as a function
of $\psi_S$. It is clear that the effect of $\psi_{NS}$ and any ions present
will be eliminated by the differentiation. They affect directly
the actual flatband voltage (or the threshold voltage of an MIS
transistor) but can be neglected in determining the surface state
charge density.

At this point a further clarification as to the information
that can be gained from a family of high frequency C-V curves
such as depicted in Figure 4 should be made. Following a
procedure outlined by Zaininger [44], after the true high
frequency ($C^o$-V) plot has been made the value of $\psi_S$ for each
value of applied bias is known. This relationship is independent
of the frequency since the average charge in surface states or in
the semiconductor is dependent only on the bias. For each bias
setting the value of $\frac{dV^{SC}}{d\psi_S}$ is found from (2-6), namely,

$$\frac{dV^{SC}}{d\psi_S} (\psi_S) = \frac{C^o}{C_{ins} + C^o}$$

Equation (2-5) can then be solved at each bias and for a given
frequency, $\omega$, to yield
\[
\frac{dV_{SS}}{d\psi_S}(\psi_S, \omega) = \frac{C_n(\omega) - C_n^\infty}{[1 - C_n(\omega)] [1 - C_n^\infty]} \tag{2-9}
\]

where

\[
C_n(\omega) = \frac{C(\omega)}{C_{\text{ins}}} \quad \text{and} \quad C_n^\infty = \frac{C^\infty}{C_{\text{ins}}}
\]

Using the relation

\[
\frac{dV_{SS}}{d\psi_S} = \frac{1}{C_{\text{ins}}} \frac{dQ_{SS}}{d\psi_S} \tag{2-10}
\]

and combining (2-9) with (2-10)

\[
\frac{dQ_{SS}}{d\psi_S} = \frac{C(\omega) - C_n^\infty}{[1 - C_n(\omega)] [1 - C_n^\infty]} \tag{2-11}
\]

The effective energy density of surface states as a function of \(\psi_S\) and \(\omega\) is

\[
\frac{dN_{SS}}{d\psi_S} = \frac{C(\omega, \psi_S) - C_n^\infty(\psi_S)}{\epsilon[1 - C_n(\omega, \psi_S)] [1 - C_n^\infty(\omega, \psi_S)]} \tag{2-12}
\]

In (2-12) \(\frac{dN_{SS}}{d\psi_S}\) is the effective density of surface states which can follow the ac signal up to the measurement frequency \(\omega\). No information as to the spatial distribution or captive cross section of the interface states is given, however, so that the usefulness of the information gained would not, for the purposes of this work, seem to justify the use of this procedure.
Qualitative information to be gained from the C-V plots at different frequencies is, nonetheless, very important.

In order to be able to properly evaluate the experimental results to be presented below, it is essential to have a clear understanding of the direction the C-V curve is shifted by the presence of charge in the insulator. Consider, for example, an MIS capacitor with p type substrate. Assume that $\phi_{MS}$ is zero, and that there are no surface states. With no applied bias the sample is in the flatband condition. Now let positive charge be introduced in the insulator near the insulator-semiconductor interface. This charge could represent metal ions or charge trapped in the insulator. The resulting energy band diagram is shown in Figure 6. The presence of the positive charge creates a negative image charge both on the metal field plate and in the semiconductor. Note from the bending of the bands in Figure 6 that the electric field is negative in the insulator and positive in the semiconductor. In this manner both macroscopic charge neutrality is achieved, and the integral of the electric field is zero, which it must be in the absence of an applied voltage.

The sample can be restored to the flatband condition by the application of a negative bias. This is shown in Figure 7. In this condition the electric field exists only in the insulator. The required bias is simply...
**FIGURE 6. EFFECT OF POSITIVE CHARGE IN INSULATOR.**
(a) ENERGY BAND DIAGRAM
(b) ELECTRIC FIELD (APPROX.)
FIGURE 7. FLATBAND CONDITION UNDER NEGATIVE BIAS WITH POSITIVE CHARGE PRESENT.

(a) ENERGY BAND DIAGRAM
(b) ELECTRIC FIELD (APPROX.)
\[ V = -\frac{Q}{C_{\text{ins}}} \]  

(2-13)

where \( Q \) is the charge in the insulator (in coulombs/area) and is taken to be at the interface. The error given by Equation (2-13) will be small if the charge is near the interface.

In the presence of the positive charge near the interface, the flatband condition occurs not at zero applied voltage but at a negative bias given by (2-13). It is clear then that the C-V curve is shifted towards more negative values of bias. This is equally true whether the substrate is p or n type.

In the case of negative charge in the insulator near the insulator-semiconductor interface, the inverse of the situation described above exists and the C-V plot is shifted towards more positive bias.
The vapor deposition of $\text{Si}_3\text{N}_4$ has been accomplished by the ammonolysis of both silicon tetrachloride and silane [5]. The reaction between silane ($\text{SiH}_4$) and ammonia ($\text{NH}_3$) has been favored recently since the use of silicon tetrachloride and ammonia results in the formation of ammonium chloride and polymeric intermediate products. Films deposited using $\text{SiH}_4$ and $\text{NH}_3$ are reported to be amorphous at deposition temperatures below 900°C [7] with deposition possible down to 650°C [9]. The vapor pressure of As over GaAs is given for four-atom and two-atom molecules of arsenic vapor in the range 950° to 1200°K by Drowart and Goldfinger [35] as

$$\log P_{\text{As}_4} \text{ (atm.)} = - \frac{19320}{T} + 11.43$$

and

$$\log P_{\text{As}_2} \text{ (atm.)} = - \frac{17340}{T} + 9.86$$
Using these results as a guide, it was anticipated that amorphous films of Si$_3$N$_4$ could be deposited at the low end of the SiH$_4$-NH$_3$ temperature range (e.g., 650 to 750°C) without appreciable loss of arsenic from the GaAs surface. Deposition in the range 800 to 900°C most commonly used with silicon substrates would necessitate the use of arsenic over-pressure which would both complicate the system and add an unknown factor to the Si$_3$N$_4$ film.

Hydrogen and nitrogen have been used as a carrier or diluting gas with the SiH$_4$-NH$_3$ system. Nitrogen was chosen for this work primarily for the sake of safety since no distinct advantage of one gas over the other has been reported. Hydrogen has been used by some researchers [6] to suppress the premature decomposition of SiH$_4$ which decomposes at about 500°C. Since the substrate temperature was to be around 700°C and R.F. heating of a small susceptor was to be employed, this factor was not thought to be significant. This proved indeed to be the case when depositions were made. Brown, et al, [29] on the other hand suggests that the use of hydrogen as a carrier might increase the possibility of inclusion of excess and chemically bonded H in the Si$_3$N$_4$ film.

Since nitrogen was to be used as a carrier gas, the SiH$_4$ was purchased diluted with nitrogen - 96% N$_2$, 4% SiH$_4$. The
semiconductor grade mixture was obtained from the Matheson Company. The ultra high purity (99.999%) NH\textsubscript{3} was also purchased from Matheson.

The N\textsubscript{2} carrier was taken off from tanks of semiconductor grade liquid N\textsubscript{2} purchased from the Mineweld Company.

A schematic of the deposition apparatus used is shown in Figure 8. All tubing from gas sources to the quartz reaction tube were teflon. Flow meters were stainless steel. A two-way valve allowed the NH\textsubscript{3} and SiH\textsubscript{4} to be turned from exhaust to the quartz reaction tube to start deposition. N\textsubscript{2} was allowed to flow through this two-way valve to exhaust as well as through the quartz tube at all times when depositions were not being made. In this manner the system did not have to be pumped down or otherwise purged. Gaseous HCl was installed for in situ etching.

The quartz reaction tube was 30 m.m. I.D. The susceptor was formed from a graphite cylinder one inch in diameter and 5/8" long. The cylinder was cut in half (lengthwise) to form a 1" x 5/8" horizontal surface upon which the sample was laid. A hollow quartz tube served as a handle for the graphite susceptor.

A thermocouple rod passed down the hollow quartz handle into the graphite susceptor. The leads from the thermocouple connected to a Research Inc., Thermae 6000 Temperature Controller. The controller output, by means of an interfacing circuit, controlled the D.C. plate voltage of a 1 KW, 475 KC Ther-Monic induction heating unit. Nulling accuracy of the controller was 15 µ volts
FIGURE 8. SCHEMATIC REPRESENTATION OF DEPOSITION APPARATUS
or about \(10^\circ C\) (chromel-Alumel thermocouple). The temperature could thus be controlled very accurately.

There are some important advantages of an R.F. induction furnace over the less expensive resistance furnace. In the R.F. furnace the susceptor is heated directly and quickly so that the quartz tube is cool everywhere except in the immediate vicinity of the susceptor. The R.F. coil can be water cooled, furthermore, to help cool this section of the tube. In this manner contamination from the tube walls is minimized. Also, it is possible to visually monitor the film growth and by observing the color changes to repeat desired film thickness quite accurately (± 100 Å at 1000 Å) even though process parameters are changed over a wide range.

In addition to the direct reaction of silane with ammonia giving

\[
3 \text{SiH}_4 + 4 \text{NH}_3 \rightarrow \text{Si}_3\text{N}_4 + 12 \text{H}_2
\]

since silane readily decomposes to give

\[
\text{SiH}_4 \rightarrow \text{Si} + \text{H}_2
\]

the reaction

\[
3 \text{Si} + 4 \text{NH}_3 \rightarrow \text{Si}_3\text{N}_4 + 6 \text{H}_2
\]

is to be expected. The last two reactions suggest that all the free silicon may not be converted to \(\text{Si}_3\text{N}_4\) resulting in excess
silicon in the film.

Table I gives the results of a preliminary test on several samples at different $\text{NH}_3$ to $\text{SiH}_4$ ratios. All substrates were n type GaAs (III plane, $3.8 \times 10^{16}$ Te doped). Deposition temperature was $725^\circ\text{C}$ with an $\text{N}_2$ carrier flow of 5 cu. ft./hr. The etch test was made in 49% HF acid at room temperature. The relative dielectric constant given in the table is the average of three to five samples. The scatter was about ±5% between samples and was probably due mostly to error in the thickness measurement.

Table I

<table>
<thead>
<tr>
<th>Flow Rate of $\text{NH}_3$ (cc/min.)</th>
<th>Vol. Ratio $\text{NH}_3$ to $\text{SiH}_4$</th>
<th>Etch Rate (Å/min.)</th>
<th>$\epsilon_r$</th>
<th>Max. Field Strength (v/cm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>18</td>
<td>5:1</td>
<td>300-350</td>
<td>7.9</td>
<td>$5 \times 10^6$</td>
</tr>
<tr>
<td>30</td>
<td>25:1</td>
<td>800-1000</td>
<td>6.3</td>
<td>$9 \times 10^6$</td>
</tr>
<tr>
<td>60</td>
<td>62.5:1</td>
<td>800-1000</td>
<td>6.2</td>
<td>$1.1 \times 10^7$</td>
</tr>
<tr>
<td>290</td>
<td>80:1</td>
<td>800-1000</td>
<td>6.1</td>
<td>$2.9 \times 10^7$</td>
</tr>
<tr>
<td>290</td>
<td>121:1</td>
<td>800-1000</td>
<td>6.15</td>
<td>$2.8 \times 10^7$</td>
</tr>
</tbody>
</table>
Thickness was measured by interference fringes and by means of a Bausch and Lomb Spectrophotometer (Model 505). Aluminum dots nominally .020 inch in diameter and approximately 10,000 Å thick were evaporated through a mask onto the Si₃N₄ film to allow capacitance measurement. Only a slight difference is seen in the etch rate, dielectric constant and maximum field strength for films deposited with NH₃ to SiH₄ ratios of 25 to 1 or greater. The relative dielectric constant appears to decrease somewhat and the field strength increases as the NH₃:SiH₄ ratio increases. Both effects appear to saturate at high ratios. The film deposited at 5:1, however, shows a distinct difference in all three parameters. Other workers [4,5,8,29] have reported Si₃N₄ films deposited at 900-1100°C on silicon to have etch rates of 150-300 Å/min. in 49% HF. Their results also show higher etch rates for lower deposition temperatures. The etch rates of 800-1000 Å/min. given here for a deposition temperature of 725°C are in good agreement with their findings. The relatively low etch rate of 300-350 Å/min. for the 5:1 film suggests that this film contains excess silicon. This agrees also with the conclusion of Bean, et al. [7] that a 5:1 ratio is silicon rich. It is interesting to note that Saxena and Thai [24] reported etch rates of 340 Å/min. with films deposited at 400°C from NH₃ and SiH₄ in a glow discharge. The ratio of NH₃ to SiH₄ was not reported, however. The higher dielectric constant and lower field strength for the 5:1 film here also would seem to support
the conclusion that the film is silicon rich.

The results given in Table I indicate that good Si$_3$N$_4$ films having field strength of $10^7$ volts per cm. or greater are achieved at NH$_3$ to SiH$_4$ ratios above 25 to 1. It will be shown in Chapter IV that the electrical interface properties of the Si$_3$N$_4$-GaAs system are quite dependent on this ratio, with ratios of 49:1 and 62:1 giving significantly different results.

**Sample Preparation**

The GaAs wafers used in this investigation were purchased from Bell and Howell Research Labs. The wafers were .020 inch thick. The p type material was <111> oriented, zinc doped. Hall measurement of one wafer showed a hole mobility of 232 cm$^2$/v. sec. and a carrier concentration of $1.41 \times 10^{17}$ cm$^{-3}$, which was in agreement with the supplier's data for the ingot of 237-240 cm$^2$/v. sec. and $0.85 - 1.76 \times 10^{17}$ cm$^{-3}$. The n type material was also <111> oriented, tellurium doped, showed an electron mobility of 6600 cm$^2$/v. sec. and a carrier concentration of $3.84 \times 10^{16}$ cm$^{-3}$.

The wafers were first hand lapped on an iron plate using 9 μ aluminum oxide in an oil slurry to obtain a dull, smooth surface. They were then mounted on a polishing block and polished on a wheel covered with a polishing cloth (Buehler Ltd., No. 40-7618). A 1/2% solution of bromine in methanol was dripped onto the cloth to effect the chemical polishing. This method of polishing
GaAs was first reported by Sullivan and Kolb [36]. The wafers were polished to a mirror finish. They were then scribed by a diamond scribe and broken into chips approximately 1/4" square.

The chips were prepared for deposition of the Si$_3$N$_4$ by ultrasonic cleaning in trichloroethylene and acetone and rinsing in methanol. It was found that the ultrasonic cleaning caused cleaving of microscopic pieces from the edges of the chip. These were removed by swabbing lightly with a cotton swab dipped in methanol. After rinsing in methanol, the chips were rinsed in deionized water having a resistivity greater than 15 megohms. They were then etched for 20 seconds in an etch consisting of HCl, H$_2$O$_2$ and H$_2$O in volume ratio 3:1:1. The chips were again rinsed in the deionized water; blown dry with high purity N$_2$, and put on the graphite susceptor in the quartz tube of the R.F. furnace. N$_2$ flowed through the tube until the deposition temperature was reached at which time the SiH$_4$ and NH$_3$ gases were switched to the tube to begin the deposition. The color changes were clearly visible as the Si$_3$N$_4$ deposited. Nearly all samples tested had film thickness in the 850 to 1050 Å range (dark blue to blue).

After deposition of the Si$_3$N$_4$, the susceptor was allowed to cool in N$_2$ to near room temperature, and the chip was removed from the furnace. Aluminum dots were then evaporated onto the chip through a metal mask. The dots were nominally 10 and 20 mil in diameter. The aluminum was approximately 10,000 Å thick.
Since C-V measurements were to be made on the MNS (metal-nitride-semiconductor) capacitors a contact resistance at the substrate (i.e., the back contact) of less than 100 ohms was adequate. Indium was applied to the back of n type chips with a soldering iron. This gave a contact resistance of less than $10^3$ ohm/cm$^2$. Contact to the p type chips could be made by evaporating silver onto the back side of the chip and sintering in argon at 500°C for 15 minutes. This gave a contact resistance of about 9 ohm/cm$^2$. In order to eliminate the need for evaporating silver onto the chips, however, an alloy of 30\% Ag - 70\% Ga was made. This alloy could be applied to the chips with a soldering iron, and gave a contact resistance only slightly greater than the sintered silver. Contact resistance for the 1/4 inch samples was 20-50 ohms which was acceptable.

C-V Measuring Techniques

The chips were placed on the stage of a micromanipulator for making the C-V tests. The stage was gold plated and provided the electrical contact to the substrate. A .010 inch beryllium-copper wire probe was lowered into position to make contact with the aluminum dot field plate. A resistance heating element and thermocouple inserted into the stage allowed controlled heating of the chip for elevated temperature tests.

Leads from the probe station were connected to the appropriate test instrument. Most measurements were made with
a Boonton Electronics Model 75C Capacitance Bridge which has a frequency range of 5 to 500 KC.

A preliminary test could be made on the samples by connecting the leads to a Tektronix Model 130 LC meter which converted the capacitance to a voltage which was applied to the y deflection circuit of an x-y plotter. Bias voltage was applied to the sample and to the x deflection circuit of the plotter. This enabled a quick method of obtaining a C-V plot at 100 KC test frequency.

Measurements at higher frequencies were made on a Boonton type 250A RX Meter which has a frequency range from .5 to 250 Mc. Use of this meter necessitated mounting a chip platform and wire probe directly on the meter terminals (see Figure 9).

All measurements were made in the dark.
FIGURE 9. DETAILS OF CHIP PLATFORM ON RX METER
CHAPTER IV.

EXPERIMENTAL RESULTS ON P TYPE SUBSTRATES

An Overview

The first C-V curves obtained on p substrates showed two prominent characteristics, presence of fast surface states and a field induced hysteresis.

The presence of fast surface states is indicated by the curves of Figure 10. For this sample a test frequency of 1.5 Mc was required to "freeze out" the fast states - frequencies above 1.5 Mc yielding the same curve. The NH$_3$ to SiH$_4$ ratio for deposition of the Si$_3$N$_4$ was 25:1. At higher NH$_3$ to SiH$_4$ ratios the frequency response of the fastest states decreased until at a ratio of 55:1 the surface states for good samples could not follow a 500 Kc signal. This is shown in Figure 11. A comparison of Figures 10 and 11 shows, moreover, a difference in the energy position of those states which could respond to 100 Kc but not 500 Kc. In Figure 10 the greatest difference between the 100 Kc and 500 Kc curves is in the inversion region (i.e., in the region of minimum capacitance). In Figure 11, however, the greatest difference between the 100 and 500 Kc curves lies in the accumulation and depletion regions. This
Capacitance (pfd)

G-34
830 Å Si₃N₄ on
1.4 x 10¹⁷ P type GaAs
Dep. Temp. = 725°C
NH₃:SiH₄ = 25:1
Area = 2.2² x 10⁻³ cm²

FIGURE 10. C-V PLOT SHOWING FAST STATES.
Figure II. C-V curves showing fast states in depletion region.
Indicates that whereas the fastest states lie near or above midgap (the inversion position of the Fermi level) for the sample of Figure 10, they lie in the lower half of the band gap (the depletion and accumulation position of the Fermi level) for the sample of Figure 11. A frequency of 500 Kc was sufficiently high to freeze out all fast states for nearly all films deposited at NH$_3$ to SiH$_4$ ratios of 55:1 or greater and for some films deposited at ratios as low as 49:1.

Another difference between the curves of Figure 10 and those of Figure 11 is that the curves of Figure 11 are shifted toward more negative voltages. This shift was found to be generally true as the NH$_3$ to SiH$_4$ ratio was increased. The position of the curve will be treated in greater detail below. It will be shown that in addition to the NH$_3$:SiH$_4$ ratio the shift of the curve is also dependent on the rate of cooling after deposition or annealing and to the field induced hysteresis effect.

Figure 12 shows a C-V plot made on an x-y plotter. The voltage sweep was 5 volts/sec. so that both curves were swept out in about 15 seconds. The curve swept from left to right lies some eight volts to the left, i.e., toward more negative voltage, than the return sweep from right to left. This field induced hysteresis has been reported in the case of Si$_3$N$_4$ deposited on Si [15,16] and is also present for the Si$_3$N$_4$-GaAs system.
Normalized Capacitance

FIGURE 12. C-V CURVES SHOWING HYSTERESIS.
The significance of this hysteresis can hardly be over emphasized. If stable MNS FET's are to be realized the hysteresis must be eliminated or minimized to acceptable levels. The hysteresis effect might, on the other hand, be utilized to give a FET with two stable states, i.e., a memory device. The hysteresis received, therefore, the major emphasis of this investigation.

Another effect that should be mentioned at this point, is the apparent reduction of the relative dielectric constant from annealing. This effect is shown in Figure 13. Curves A and B were made after deposition of the Si$_3$N$_4$ and evaporation of the aluminum field plates. Curve C was made after an anneal for 15 minutes in Argon at 400°C. There is an apparent 4.5% reduction in the dielectric constant as a result of the annealing. Annealing tests in N$_2$ rather than argon gave no detectable difference. No further reduction in dielectric constant was effected by repeating the annealing or increasing the temperature (up to 500°C) or the time beyond 15 minutes. While some effect could be obtained at annealing temperatures as low as 200°C, further reduction in dielectric constant could often be achieved up to 400°C. The amount of the reduction was somewhat erratic, varying generally from a maximum of 5% at low NH$_3$:SiH$_4$ ratios (i.e., 25:1) to undetectable change at the highest ratio (121:1). There was no indication of a change in the area of the aluminum field plates or in their adherence.
FIGURE 13. EFFECT OF ANNEALING ON C-V PLOT.
to the $\text{Si}_3\text{N}_4$. The most conclusive evidence of a change in the $\text{Si}_3\text{N}_4$ film is given by a change in the hysteresis effect as a result of annealing. This will be shown below. The results suggest that the annealing might involve the bonding of excess silicon in the film. It was shown in Table I, Chapter III, for example, that the dielectric constant decreased as the $\text{NH}_3:\text{SiH}_4$ ratio increased. One would expect, as was found, a reduction in the annealing effect as the $\text{NH}_3$ to $\text{SiH}_4$ ratio was increased.

The Hysteresis Effect - Trap Filling

Returning to Figure 12, it is clear that the displacement of the two curves indicates either a transfer of charge across the $\text{Si}_3\text{N}_4$-GaAs interface, or a movement of charge within the $\text{Si}_3\text{N}_4$. The direction of the curve shifting is, however, in the wrong direction to be explained by movement of charge within the $\text{Si}_3\text{N}_4$. After the bias is swept to the most negative voltage, for example, the return curve lies to the left, indicating, as discussed in Chapter II, the movement of positive charge to the interface. Positive charge in the $\text{Si}_3\text{N}_4$ would not move toward the interface, however, with negative bias on the field plate. A completely analogous argument applies to negative charge in the insulator. It must be concluded that charge moves across the semiconductor-insulator interface and is trapped. The direction of the curve shifting, as well as the recovery times involved can be explained, at least in a qualitative way, by
such a trapping model. The difficulty in obtaining a quantitative model lies in the fact that no method has yet been devised to determine both the spatial and energy distribution of the traps. A great deal of insight can be gained, however, from the qualitative trapping model.

Figure 14(a) shows an energy band diagram of a MIS system at flatband. Traps are indicated near the insulator-semiconductor interface. Traps above the Fermi level are taken as being positive and empty,* while those below the Fermi level are considered to be full and neutral. If the metal is now biased more positively, the bands will be bent as shown in Figure 14(b). The field in the insulator, which terminates on negative charge in the semiconductor, is in a direction to cause tunneling of electrons into the insulator. If these electrons are captured by traps, the traps become neutral - or positive charge has been removed from the interface. If now the bias is restored to its original condition, the bands will not be flat as they were in Figure 14(a), but will be bent upward, indicating accumulation, as is shown in Figure 14(c). It will thus require the application of a more positive voltage to again obtain the flatband condition. Since the flatband condition represents one point on the C-V curve, it is clear that the

* The Fermi function is not so discontinuous as is suggested by this argument (except at zero temperature), but more is to be gained than lost, at this point, by the simplification.
FIGURE 14. FILLING OF TRAPS
application of a positive bias stress (in going from Figure 14(a) to 14(b)) shifts the C-V plot to the right or toward more positive voltages as discussed in Chapter II. This is in agreement with the shift of Figure 12.

Without knowing the exact spatial distribution of the traps, it is reasonable to assume that some traps are sufficiently near the interface to exchange charge rather quickly (e.g., in less than a second) while others farther from the interface are in such poor communication with the substrate as to be unable to exchange charge across the interface at fields below breakdown even after many days. Traps far removed from the interface can, however, exchange charge with the conduction band and valence band of the insulator.

If there is a very large density of traps near the interface, filling of these traps to equilibrium with the bias should occur much more quickly than if electrons must tunnel a greater distance. Consider, for example, filling of the traps of Figure 14(a); that is, the distribution of charge near the interface as a function of time as the equilibrium state of Figure 14(b) is obtained. Starting at the flatband condition of Figure 14(a), let a large positive bias be applied. The resulting charge distribution and electric flux density \( \mathbf{D} \) is as shown in Figure 15. \( Q_M \) and \( Q_T \) represent the positive charge on the field plate and in the unfilled traps. \( Q_N \) and \( Q_D \) represent minority carrier inversion
FIGURE 15. CHARGE DISTRIBUTION AND ELECTRIC FLUX DENSITY AT BEGINNING OF TRAP FILLING.
charge and depletion layer charge. The field is highest at the insulator-semiconductor interface and in a direction to allow tunneling of electrons into the insulator. As electrons tunnel across the interface, \( Q_N \) and \( Q_D \) decrease and \( Q_T \) decreases as the traps fill and are neutralized.

It has been implied to this point that all traps are positive when empty, but this will presently be shown to be in disagreement with experimental results. If there also exists traps which are neutral when empty and negative when filled, it is possible for most or all of the negative charge required to terminate the electric field to be trapped in the insulator. The limiting condition is depicted in Figure 16, where no field penetrates the semiconductor. If this limiting condition is reached, no more charge crosses the interface. The negative charge trapped in the insulator "screens" the electric field from reaching the semiconductor.

The charge trapped in the insulator under this condition is

\[
Q = C_{\text{ins}} V_B \tag{4-1}
\]

where \( V_B \) is the applied bias voltage. If the trapped charge remains entirely in the insulator when the bias is removed, the resulting shift in the flatband voltage (or in the C-V curve) is

\[
V'_{FB} = \frac{Q}{C_{\text{ins}}} \tag{4-2}
\]
FIGURE 16. CHARGE AND ELECTRIC FIELD FOR LIMITING CONDITION WHERE ALL FIELD TERMINATES ON NEGATIVE CHARGE IN TRAPS.
where $V_{FB}'$ represents the change in flatband voltage resulting from application and removal of the positive bias. In both (4-1) and (4-2) the assumption is made that the trapped charge is near the insulator-semiconductor interface. Combining (4-1) and (4-2) gives

$$V_{FB}' = V_B \quad (4-3)$$

Equation (4-3) is exactly correct, moreover, since the effect of the charge not being at the interface has been canceled out between (4-1) and (4-2).

The conditions for achieving (4-3) are: (1) complete screening of the field during positive biasing and (2) no escape of charge back across the interface after bias is removed. The result of (4-3) can be made more general by stating that if a plot of $V_{FB}'$ (or any other voltage representing curve shift) against $V_B$ is made the maximum slope is unity. The slope is less than unity when either or both of conditions (1) and (2) are not met. In particular, condition (1) can only be met if there is a sufficient density of traps available for trapping the charge required for complete screening.

If complete screening is achieved, the charge is in equilibrium with the applied bias, i.e., application of the bias for longer time will not produce greater shift of the C-V curve. If this condition is not achieved, equilibrium is established when sufficient negative charge has transferred across the
interface so that the field strength at the semiconductor is reduced to the point that no further net charge crosses the interface.

Figure 17 shows the "trap filling" response, as discussed above, for two samples. The Si$_3$N$_4$ film thickness of each is about 850 Å. In each case a positive 20 volt bias stress was applied and the shift of the C-V curve as a function of time was noted. The capacitance at flatband, which had previously been determined, was used as an indication of curve shift. The application of the bias stress was interrupted at each test point for about 10 seconds in order to determine how much the flatband voltage (i.e., the voltage required to yield flatband capacitance) had shifted. The shift in flatband voltage versus time is shown in Figure 17. It can be seen that whereas sample G-35 reached equilibrium in about two minutes with a shift of 5.7 volts, G-45 reached a shift of only 3.7 volts after an hour. G-35 was deposited at a NH$_3$:SiH$_4$ ratio of 49:1 at 725°C, whereas G-45 was deposited at a 62:1 ratio at 700°C. It can be concluded that whereas G-35 has a relatively high density of traps near the interface (i.e., within the tunneling distance) and/or the traps have a large electron capture cross section so that equilibrium is soon reached, G-45 has a lower density of states near the interface so that when equilibrium is finally reached the shift in flatband voltage is less. It is clear,
FIGURE 17. SHIFT OF FLATBAND VOLTAGE BY POSITIVE BIAS.
as will be emphasized below, that the amount of hysteresis is strongly affected by processing.

Nature of Traps

Returning now to the nature of the traps, that is, whether they are neutral or positive when empty, assume first that all traps are positive when empty. The presence of the positive traps (see Figure 14(a)) at flatband would cause flatband to occur at a more negative voltage than that dictated by difference in metal-semiconductor work function alone. This is indeed the direction that the curves are shifted. Figures 11 and 13 show flatband voltages of -15.6 and -6.5 respectively. Since the work function of the aluminum field plate is about the same as the electron affinity of GaAs (= 4 e.v.), $\phi_{MS}$ for the p substrate is equal to the difference between the conduction band and the Fermi level in the substrate and is negative. This is about 1.3 e.v. for the substrate used (doping of $1.4 \times 10^{17}$).

The remainder of the shift in Figures 11 and 13 (viz., -14.3 and -5.2 volts, respectively) could be due in part or whole to the presence of unfilled, positive traps. Any shift not due to traps could be attributed to ionic contamination or positive surface states at the interface.

Consider, however, the situation that exists when a positive bias stress is applied so as to fill the traps. The maximum negative charge that could cross the interface and be trapped
N-48

1050 Å Si₃N₄ on
3.8 x 10¹⁶
N type GaAs
Dep. Temp. = 700°C

FIGURE 18. C-V CURVE FOR N SUBSTRATE.
would exactly equal the positive charge of the previously unfilled traps. Thus, at most, the flatband voltage could be shifted back to the right until it reached -1.3 volts, exactly nullifying the original shift to the left. It is possible, however, to shift the flatband voltage much more than this. It is possible, for example, to shift the flatband voltage of the sample of Figure 13 from -6.5 to +1.5 by applying a +40 volt bias stress. Other samples showed even greater shifts, nor was there any indication that the amount of shift was saturating even at bias stresses approaching breakdown, as is shown below. It appears, then, that there are a great number of traps to be filled - so many that if they were all positive when empty the flatband condition would occur at extremely negative voltages.

In view of the above discussion, it could alternatively be assumed that all traps are neutral when empty. The shift to the left could then be attributed to ion contamination and/or positive surface states at the interface. Some insight as to the nature of these "surface states", e.g., dangling bonds, can be gained by examining the difference between C-V curves for p and n type substrates.

For the p substrates used here, the Fermi level lies very close to the valence band (within .1 e.v.) so that at flatband most of the energy gap lies above the Fermi level. For the n substrates, the Fermi level is about .125 e.v. below the conduction band, so that most of the energy gap is below the
conduction band, so that most of the energy gap is below the Fermi level at flatband. For n and p type samples processed in the same manner, the ionic contamination should be similar. Any significant difference in flatband voltage beyond that due to $\phi_{MS}$ should, therefore, reflect the nature of the surface states. The C-V curves for n substrates are, in fact, shifted to the right giving positive flatband voltages. A typical curve is shown in Figure 18. This strongly suggests that the surface states are negative when below the Fermi level, thus accounting for the difference between curves on p and n substrates. The same states would be neutral for p samples where they are nearly all above the Fermi level at flatband.

The positive charge causing the shift of C-V curves on p substrates must be accounted for by ionic contamination and/or by positive, empty, traps. As was pointed out earlier, however, the shift of the curves can be affected by the NH$_3$:SiH$_4$ ratio which should vary trap density but not ion contamination - ionic contamination being more dependent on sample preparation and cleanliness of the apparatus. It follows that some traps must be process dependant and positive when unfilled.

In summary, it appears that there are two types of traps in the Si$_3$N$_4$ near the interface - one type being neutral when empty and the other being positive when empty. Surface states at the interface seem to be negative when below the Fermi level, and account for the difference in curve location on p and n type substrates.
The Hysteresis Effect - Trap Emptying

The filling of traps involves electrons crossing the semiconductor-nitride interface and being captured by traps, as discussed above. This phenomenon accounts for the right-most curve of Figure 12. As the bias voltage sweeps out to +20 volts traps fill, so that the return path (right to left) is displaced to the right (i.e., toward positive voltage) indicating a net increase of negative charge at the interface.

The complementary part of the cycle is completed as the bias swings negative. The bias is then in a direction to raise the energy levels of the traps (see Figure 19) allowing trapped electrons to tunnel back to the semiconductors. The left-most curve of Figure 12 is a result of this trap emptying. As the bias is swept negative to -20 volts, traps empty as electrons tunnel back to the semiconductor. The subsequent sweep from left to right is displaced to the left, indicating a net gain of positive charge.

In addition to the emptying of those traps which at flatband lie above the Fermi level, it is possible that some traps which are below the flatband Fermi level also empty as they are raised in energy by the negative bias. When the negative bias is released these latter traps must fill before flatband is again achieved.

Establishing an Equilibrium Condition

The discussion above has pointed out the nature of the
FIGURE 19. ENERGY BAND DIAGRAM WITH LARGE NEGATIVE BIAS TO ALLOW TRAP EMPTYING.
hysteresis cycle - filling of traps with positive bias, emptying of traps with negative bias. Before quantitative measurement could be made on the samples, however, it was necessary to establish an equilibrium or reference condition. In particular, the "zero bias, equilibrium capacitance" (ZBEC) would be the value of capacitance at zero bias when the sample is in complete thermal equilibrium. Considerable care must be exercised in practice to obtain this equilibrium condition. Since the value of the ZBEC is unknown, one can be assured of having achieved the true equilibrium only by waiting a sufficiently long time. Any procedure outlined for returning the sample to the ZBEC* should, moreover, be repeatable. Such a procedure can only be drawn up after examination of the relaxation times involved in returning the sample to equilibrium.

Figure 20 shows the relaxation after filling of traps for two representative samples. \( V_{FB} \) represents the change in flatband voltage from its value prior to application of the positive bias. Two different relaxation curves for each sample are given. The \( \text{NH}_2: \text{SiH}_4 \) ratio for the samples G-35 and G-45 are 49:1 and 62.5:1 respectively. As will be seen below, these ratios are in the range to minimize hysteresis effects.

* The term ZBEC will be used interchangeably to denote "zero bias equilibrium capacitance" and "zero bias equilibrium condition. The meaning should be clear from context.
Shift in Flatband Voltage
vs.
Log Time

FIGURE 20. RELAXATION AFTER FILLING OF TRAPS BY POSITIVE BIAS.
It is apparent from the straight line plots of Figure 20 that,

\[ \Delta V_{FB} = -A \log t \]

with \( A \) in the range 0.5 to 0.7 for \( t \) in minutes. All samples tested showed similar relaxation curves. There was no apparent correlation between the \( \text{NH}_3: \text{SiH}_4 \) ratio and the value of \( A \). The relaxation of filled traps is very slow. For an initial shift of 6 volts in flatband voltage, and using a value of 0.6 for \( A \), \( 10^{10} \) minutes would be required for relaxation back to equilibrium. This is nearly 20,000 years.

Ross and Wallmark [38] have developed a model for the emptying of traps from Si\(_3\)N\(_4\) to a silicon substrate by tunneling through a very thin (< 35 \( \AA \)) layer of SiO\(_2\). A logarithmic dependence on time is predicted. In obtaining that result the assumption is made that the transfer of charge across the interface does not effect the electric field strength in the insulator so that the transition probability for electrons to tunnel back to the semiconductor is independent of time. In the relaxation being described here this assumption is not valid, however, since the electric field is determined solely by the charge in the nitride (and \( \phi_{MS} \)) and cannot be taken as constant as the charge transfers back across the interface. The problem is complicated by the fact that the spatial distribution of the traps is not known. The potential distribution near the
Interface is therefore also undetermined. A further consideration is that the Si$_N$$_4$ film is amorphous so that the energy band configuration near the interface might well be considerably different than the simple model commonly used.

In contrast to the extremely long time required for the traps to empty with no applied bias, they could be emptied in a short time by the application of a negative bias. A typical plot of this resetting of $V_{FB}$ as a function of time is shown in Figure 21. Notice in Figure 21 that $V_{FB}$ does not return to zero but goes to negative values. In terms of the C-V plot of Figure 22, the following sequence has occurred:

1. Starting at "equilibrium" curve A, a positive bias is applied which shifts the curve to the position marked B as traps fill.

2. A negative bias is applied which moves the curve from B to C, overshooting the equilibrium position A.

In going from position B to C, not only have the traps that were filled by application of the positive bias been emptied, but also some traps which lie below the Fermi level at equilibrium have been emptied. It is to be expected that these latter traps would fill exponentially, the dominant process being described by

$$\frac{dn_t}{dt} = \Lambda n(n_{t'} - n_t)$$
FIGURE 21. RE-EMPTYING OF TRAPS BY APPLICATION OF NEGATIVE BIAS.

G-A4A
900 Å Si,N₄
on
P type GaAs

\[ V_{FB} = 6.7 \text{ at } t = 0 \]

\[ \text{Bias} = -20V \]

\[ \text{Bias} = -30V \]

Length of Time Negative Bias is Applied (seconds)
FIGURE 22. SHIFT OF C-V CURVE SHIFT WITH POSITIVE AND NEGATIVE BIAS STRESS
where \( n_t \) is the density of filled traps, \( N_t \) is the total density of filled traps at equilibrium, \( n \) is the density of conduction band electrons, and \( A \) is a capture constant. Figure 23 shows this recovery for three samples. The shift in flatband voltage is given by

\[
V_{FB}^t = V_o e^{-t/\tau}
\]

Typical values for \( \tau \) are 5-15 minutes for the samples in the dark. If the light from a microscope lamp is turned on the sample, moreover, \( \tau \) can be greatly reduced. A value of 24 seconds for \( \tau \) is shown for sample C-35 illuminated in this manner. The light increases the density of conduction band electrons \( n \) in the \( Si_3N_4 \), thus decreasing the time required to fill the traps \( (1/\tau = An) \).

At this point a procedure for establishing a ZBEC can be given:

1. Apply a negative bias for five minutes. A bias of -30 volts for \( Si_3N_4 \) films in the 850-1000 Å range is adequate. All traps above the Fermi level will empty, as will some traps below the Fermi level.

2. Remove all bias for 45 minutes to allow traps below the Fermi level to fill.

By using this procedure, a repeatable ZBEC could be obtained. In taking C-V data, bias was adjusted first to obtain negative points, bias was returned to zero to re-establish ZBEC and the
Figure 23. Filling of traps after removal of negative bias.
positive points then taken.

Effect of NH$_3$ : SiH$_4$ Ratio on Hysteresis

A detailed investigation was made to determine how the hysteresis varies as the NH$_3$ : SiH$_4$ ratio changed. Over a hundred samples were investigated. As a means of comparison, the zero bias equilibrium capacitance (ZBEC) was carefully established for each good sample as outlined above. Using this zero bias capacitance as a reference, positive bias stress was first applied to the sample and then the voltage ($V'_o$) required to again achieve the reference capacitance was noted. This cycle was repeated for a given positive bias until no further voltage shift was obtained. In this manner the amount of shift in the C-V curve for a given bias stress was found. The flatband capacitance could also have been used as the reference point, but the ZBEC was more convenient since it could be found directly by measurement. A complete C-V curve was taken for those samples to be studied in detail.

Prior to testing, all samples were annealed in Argon for 15 minutes at 400°C. As mentioned above, this resulted in a slight reduction in dielectric constant. A direct indication that the annealing produced an internal change in the film is seen by the curves of Figure 24. The two curves show the shift in C-V plot versus positive bias stress as processed and after annealing, respectively. The amount of shift is seen
G-35
850 Å Si₃N₄
on 1.4 × 10¹⁷ P GaAs
NH₃:SiH₄ = 49:1
Dep. Temp. = 725°C

As Processed

After 15 min.
Anneal in
Argon at 400°C

FIGURE 24. EFFECT OF ANNEALING ON CURVE SHIFT
to be considerably reduced by the annealing.

Figure 25 shows the shift in C-V plot, as determined by monitoring the voltage \(V_o\) required to obtain the ZDEC, as a function of bias stress for seven representative samples. Film thicknesses for the samples were 900 Å ± 10%. The samples can be divided into two groups, those deposited at Ni\(_3\):SiH\(_4\) ratios above or below about 50:1. Samples deposited at ratios below about 50:1 at both 700°C and 725°C showed a relatively large amount of shift at low bias stress, with the rate of shift reducing at higher bias. Samples deposited at ratios above 60:1 at 700°C showed the reverse effect, i.e., lower shift at low bias stress and a great deal of shift as the bias voltage was increased. A ratio of about 55:1 gave a nearly linear plot - intermediate to the two groups.

It was found that depositions at 725°C at ratios above 60:1 did not give good C-V plots. Little or no change in capacitance versus bias was found, although the films had good physical appearance and good field strength (\(> 10^7\) V/cm). Judging from the thickness of the films, the capacitances were always low. This indicated that the samples were so heavily inverted that it was impossible to achieve accumulation. It was found that by reducing the temperature to 700°C good curves could be obtained at high ratios. The C-V plots were still displaced toward negative voltages as shown by Figures 26 and 27 for ratios of 78.5:1 and 121:1.
Figure 25. Effect of NH$_3$ to SiH$_4$ ratio on amount of curve shift.
G-50B
NH₃:SiH₄ = 78.5:1
1050 Å Si₃N₄ on P type GaAs
Dep. Temp. = 700°C

FIGURE 26. C-V CURVE FOR 78.5:1 NH₃ TO SiH₄ RATIO
FIGURE 27. C-V CURVE FOR 12:1 NH$_3$ TO SIH$_4$ RATIO

$V_{FB} = -37 \text{ V}$

Dep. Temp = 700°C
Looking at Figure 25 in greater detail, it is clear that processing has a very pronounced affect on the spatial density of traps, i.e., the density of traps as a function of distance from the insulator-semiconductor interface. Samples G-25, G-26, G-34, and G-35 exhibit two to three times as much shift as the other samples at a bias of 10 volts. Since the bias at each value was repeatedly applied until no more shift was obtained, it must be concluded that G-25, G-26, G-34, and G-35 have a much greater (two to three times) density of traps within the tunneling distance than do the other samples. This is also in agreement with the discussion relating to Figure 17 above where it was concluded that G-35 had a much higher density of traps near the interface than G-45.

At higher bias (> 25 volts) samples G-34 and G-35 show a decreasing amount of shift - indicating a decreasing density of traps. Implicit in this conclusion is that the capture cross section of the traps is not a determining factor. Since the traps empty very slowly, and the bias is applied until equilibrium is achieved, it can be assumed that traps have ample time to fill - the process being limited by trap density and not by capture cross section or time.

In contrast to G-34 and G-35, samples G-45, G-49, and G-50 show an increasing amount of shift with increasing bias. At high bias the slope of these curves approach unity. As discussed
above a slope of unity is the limiting condition and indicates that equilibrium is being reached by charge screening. This can only occur if there is a sufficient density of traps to capture the charge. Samples G-45, G-49, and G-50 appear to have a high density of traps at greater distance from the interface.

A further indication of this difference in trap density versus distance from the interface is shown by Figure 28 which shows the initial relaxation (emptying of traps) after removal of a positive bias. The first data point for each curve was taken about one second after the positive bias was removed. The shift in flatband voltage \( V_{FB} \) was then noted as a function of time. It can be seen that the initial relaxation for G-35 is faster than for G-45. After ten minutes there is little difference in the two relaxation rates - the shift in flatband voltage being logarithmic in time (see Figure 20). It can be seen that initially a greater percentage of the charge crosses back across the interface in the case of G-35. The flatband voltage for G-35 shifts from 9 volts to 5 volts within 4 minutes indicating that 45% of the trapped charge relaxes back across the interface. For G-45 only 25 percent of the initially trapped charge transfers back after some eight minutes.

It is clear that the trap distribution is strongly process
$V_{FB} = \text{Shift in Flatband Voltage (volts)}$

**FIGURE 28. INITIAL RELAXATION AFTER TRAP FILLING.**
Depositions were made from 650°C to 725°C at \( \text{NH}_3 : \text{SiH}_4 \) ratios ranging from 25:1 to 300:1. Best results were obtained at a \( \text{NH}_3 : \text{SiH}_4 \) ratio of about 60:1 at 700°C. These samples show low hysteresis at fields below \( 2 - 3 \times 10^6 \) volts per cm. Higher \( \text{NH}_3 : \text{SiH}_4 \) ratios (up to at least 121:1) give about the same amount of hysteresis at low fields, but the C-V curves for these samples are increasingly shifted toward negative voltages as discussed above (see Figures 26 and 27). At fields above \( 3 - 4 \times 10^6 \) there is evidence of a great deal of charge trapping - with samples having higher \( \text{NH}_3 : \text{SiH}_4 \) ratios (about 75:1) generally showing somewhat greater effect (see Figure 25). Figure 29 shows the improvement in hysteresis at low fields (< \( 3 \times 10^6 \)) for one of the best samples (G-45) processed at 700°C at a \( \text{NH}_3 : \text{SiH}_4 \) ratio of 62:1 over the best sample (G-35) obtained at 725°C. Both curves were made at 100 Kc on an X-Y plotter.

In an attempt to further reduce or eliminate the hysteresis, tests were made using both in situ HCl gaseous etching and a stronger liquid etch at the end of the cleaning process.

The gaseous HCl etch was made in the quartz reaction chamber at 600°C. The HCl was diluted in \( \text{N}_2 \) to a ratio of 1 cc/min. to 2.5 liters/min. of \( \text{N}_2 \) and the HCl turned on for only 15-60 seconds. An etch of two minutes produced triangular etch pits. No reduction in the hysteresis was found for any of these samples.
FIGURE 29. C-V CURVES SHOWING HYSTERESIS IMPROVEMENT.
A liquid etch of \( H_2O_2:H_2SO_4:H_2O \) in volume ratio 1:3:1 was tried as a substitute for the \( H_2O_2:HCl:H_2O \) etch (also 1:3:1) used on all other samples as a final step in pre-deposition cleaning (refer to Chapter III). This is a relatively strong etch removing 5 microns per minute [39]. This etch, even after a few seconds, left a less polished surface and gave very poor results.

Temperature Effects

It was pointed out above that after the filling of traps by means of a positive bias stress the emptying of the traps is very slow - being logarithmic with time. Tests were made to determine if the traps could be emptied by elevating the temperature of the sample.

The first test involved carefully establishing the ZBEC for the sample and then applying a positive bias to fill the traps. This shifted the C-V curve 5-10 volts. The sample was then placed in a furnace with an argon atmosphere and heated to 200°C for 15 minutes. After cooling the sample to room temperature, it was found that the traps had emptied, but the curves did not always return to the initial ZBEC condition. The C-V curves were shifted toward positive voltage (see Figure 30). If the test was repeated, however, the results were the same; i.e., the curves returned to the same place but not to the initial position. In Figure 30 Curve A was taken
FIGURE 30. C-V CURVE BEFORE AND AFTER TEMPERATURE CYCLE TO EMPTY TRAPS.
before the first temperature cycle and Curve B after the temperature cycle. The shift indicates that some negative charge was left in the traps. Increasing the time to several hours and the temperature up to 500°C gave essentially the same results. It should be remembered that all the samples had previously (i.e., after processing) been annealed in argon at 400°C. It was thought that the difference in voltage for ZBEC must be due to a difference in the rate of cooling. In annealing after processing the samples were heated to 400°C for 15 minutes and the furnace was then turned off - the samples cooling down with the furnace in about 3 hours. This was done (at least originally) merely as an expedient since the samples could cool down unattended. After the temperature cycle to empty the traps, on the other hand, the samples were moved to the cool end of the furnace where they cooled in a few minutes. It was indeed found that if the samples were cooled down slowly after the trap emptying test (by turning off the furnace) the ZBEC was repeated within experimental error. This provides, then, another method of emptying the traps and establishes the validity of the ZBEC as a repeatable reference condition. By allowing the samples to cool slowly thermal equilibrium could be maintained, whereas a rapid cooling left a non-equilibrium condition with charge remaining in the traps.

A second test was made by heating the column of the probe station. In this manner the curve shift could be observed as
the temperature was elevated. The ZBEC was first established, and \( V'_o \) (the voltage required to maintain the zero bias equilibrium capacitance) was recorded vs. temperature. Each temperature value was maintained until the value of \( V'_o \) stabilized (this required about 5 minutes). Figure 31 gives the results for two samples. It is interesting that the curves for these samples cross here as they did in the case of positive voltage stress (see Figure 25). The value of \( V'_o \) increases in the positive direction as temperature increases (the C-V curve would likewise shift toward positive voltages). This indicates that a net increase of negative charge crosses the semiconductor-nitride interface and is trapped in the insulator. This result can be explained by electrons in the GaAs being thermally stimulated into the conduction band of the nitride and then dropping into traps - equilibrium being reached when the resulting field balances the electron flow. Again it can be concluded that G-35 has a greater density of traps near the interface.

The results of the first test above can now be better explained. When the samples are heated the traps can fill rather than empty. If the traps were previously filled by application of positive bias they fill further or empty somewhat as required to come into equilibrium at the higher temperature. If the sample is cooled slowly the traps empty during cooling and reach room temperature in thermal
FIGURE 31. SHIFT IN ZERO BIAS EQUILIBRIUM CAPACITANCE AT ELEVATED TEMPERATURE.
equilibrium. If the sample is cooled quickly, the traps cannot respond at the cooling rate and the sample is not in thermal equilibrium upon reaching room temperature. In this latter case it was found that the traps could be emptied by applying negative bias as described earlier in establishing the ZBEC. It was necessary, however, to apply the negative bias for a much longer time (15-30 minutes) to empty the traps (compare with Figure 21 for emptying of traps filled electrically). This indicates that the filled traps were farther from the interface. This is in agreement with the concept that the traps were filled from the conduction band during the thermal cycle allowing deeper penetration into the nitride.

The temperature instability indicated in Figure 31 would seriously limit the usefulness of a GaAs FET as an amplifying device, a logic gate, or as a bistable memory element. The shift in threshold voltage for such a FET would be about 2 volts over the temperature range of 75 to 135°F. Another 2 volt shift could be expected from the use of (for example) a 15 volt gate signal for G-45, the best sample (see Figure 25).

A third test was made to determine if there was any ion migration in the $Si_3N_4$. The ZBEC was established and the samples heated with -30 volts bias to 350°F for 4 hours. The bias was left on and the samples cooled slowly (approximately 2°F/min.) to room temperature. The bias was then removed and the samples allowed to return to equilibrium,
i.e., the hysteresis effect of the -20 volt bias was allowed to relax (see Figure 23). This was repeated with a bias of +20 volts, but because of the long time required for traps to empty due to the positive bias, the traps were emptied by applying -20 volts for 5 minutes after the sample returned to room temperature. This necessity of canceling out the field and temperature induced hysteresis limits the accuracy of the test somewhat. A shift in C-V curve of .5 volt due to ion migration should be detectable. No evidence of ion migration was found in the two samples (g-35 and G-45) tested.

**Density of Surface States**

Because of the hysteresis effect in these samples, the concept of surface state density does not have its usual meaning. In the normal situation (e.g., grown silicon dioxide on silicon) surface state density is a function of surface potential but is not dependent on the past history of the sample. The situation here is different, however, since the shape of the C-V curve is a function of the direction in which the voltage is varied. Figure 32 shows two curves for the sample (G-45) exhibiting the least amount of hysteresis at low fields. Curve A was taken by varying the voltage in the negative and the positive direction starting each time from zero volts in the equilibrium condition. This was the standard procedure used in taking C-V curves as discussed above. Curve B
was taken by first adjusting the voltage to +25 volts and then taking data as the voltage was decreased back through zero to negative voltages. The dotted curve in Figure 32 is Curve B shifted next to Curve A. Curve B is somewhat steeper than Curve A. This is due to the fact that the traps were first filled before taking Curve B. Since the traps empty very slowly until negative voltages are reached, this curve gives the minimum effect of hysteresis as far as determining surface state density. The fact that the curve is shifted to the right of the equilibrium Curve A does not effect surface state density measurements. Such a shift is analogous to that produced by a non zero $\phi_M$ and has no effect on surface state density as was discussed in Chapter II.

Curve C in Figure 32 is the calculated theoretical C-V curve for values of $\psi_S$ ranging from 0 to +1.1 volts. This corresponds to the Fermi level going from .1 volt above the valence band ($\psi_S = 0$) to .2 volts below the conduction band ($\psi_S = 1.1$). The surface state density was calculated from Curves B and C and is shown in Figure 33. $N_{SS}$ is the effective density of surface states per square centimeter per unit voltage. $N_{SS}$ is in the $10^{12}$-$10^{13}$ range - being highest for low values of $\psi_S$. Values of $\psi_S$ between 0 and .1 volt correspond to negative values of the applied voltage. The emptying of traps in this region could account for the large increase in $N_{SS}$. The lowest value of $N_{SS}$ is $1 \times 10^{12}$ for
Capacitance (pfd)

Capacitance (pfd)

Applied Voltage (volts)

FIGURE 32. C-V CURVES FOR BEST P TYPE SAMPLE

G-45
900 Å Si₃N₄
on P type GaAs
NH₃:SiH₄ = 62.5:1
Dep. Temp. = 700°C
Freq. = 500 KC
FIGURE 33. SURFACE STATE DENSITY FOR BEST P SAMPLE
\( \psi_s \) of .4-.5 volts.

### Impurity Redistribution

Table 2 gives the calculated impurity doping density for eight samples. The calculation was based on the depletion approximation which assumes uniform doping to a depth equal to at least the maximum penetration of the depletion layer (see Appendix for details on the calculation). The measured

<table>
<thead>
<tr>
<th>Sample</th>
<th>( \text{NH}_3: \text{SiH}_4 )</th>
<th>Dep. Temp.</th>
<th>Doping Density (per cm(^2))</th>
</tr>
</thead>
<tbody>
<tr>
<td>G-34</td>
<td>25:1</td>
<td>725°C</td>
<td>( 2.94 \times 10^{17} )</td>
</tr>
<tr>
<td>G-35</td>
<td>49:1</td>
<td>725°C</td>
<td>( 2.40 \times 10^{17} )</td>
</tr>
<tr>
<td>G-44</td>
<td>55:1</td>
<td>700°C</td>
<td>( 3.10 \times 10^{17} )</td>
</tr>
<tr>
<td>G-45</td>
<td>62.5:1</td>
<td>700°C</td>
<td>( 2.62 \times 10^{17} )</td>
</tr>
<tr>
<td>G-49</td>
<td>121:1</td>
<td>700°C</td>
<td>( 2.41 \times 10^{17} )</td>
</tr>
<tr>
<td>G-50</td>
<td>78.5:1</td>
<td>700°C</td>
<td>( 2.43 \times 10^{17} )</td>
</tr>
<tr>
<td>G-51</td>
<td>62.5:1</td>
<td>700°C</td>
<td>( 2.64 \times 10^{17} )</td>
</tr>
<tr>
<td>G-52</td>
<td>62.5:1</td>
<td>700°C</td>
<td>( 2.93 \times 10^{17} )</td>
</tr>
</tbody>
</table>
bulk doping density was $1.41 \times 10^{17}$. All samples show greater doping density after deposition of the Si$_3$N$_4$ than the measured bulk value. The substrates were zinc doped.

**Summary**

The predominate characteristic of the Si$_3$N$_4$-GaAs interface for p type substrates is the presence of hysteresis due to the filling and emptying of traps in the Si$_3$N$_4$ near the interface. The spatial distribution of these traps from the interface is strongly dependent on the NH$_3$:SiH$_4$ ratio. The amount of this hysteresis was minimized to less than 2 volts for fields below $1.7 \times 10^6$ volts/cm for the best sample. Best results were obtained at a deposition temperature of 700°C and a NH$_3$:SiH$_4$ ratio of 62.5:1.

The relaxation (emptying) of filled traps is extremely slow and logarithmic in time. Recovery times as long as 20,000 years at 25°C are indicated. The refilling of traps to equilibrium after a large negative bias is exponential in time with time constants of a few minutes in the dark.

It appears that traps in the Si$_3$N$_4$ are of two types—neutral when empty (of an electron) or positive when empty. The latter type accounts for the "positive shift" of C-V curves for samples on p substrates. Surface states at the interface appear to be negative when below the Fermi level and account for the opposite shift for samples on n type substrates.
A method was found for obtaining repeatable C-V measurements. This involves the establishing of a zero bias equilibrium condition. This condition could be achieved by relaxation after the application of a negative bias or by a slow cooling after heating to 200°C.

The use of gaseous HCl as an in situ etch and of a stronger (\(\text{H}_2\text{O}_2:\text{H}_2\text{SO}_4:\text{H}_2\text{O}\)) liquid etch gave no improvement or poorer results, respectively.

There was no indication of ion migration at elevated temperatures. There was, however, evidence of trap filling as the temperature was raised, resulting in a temperature induced hysteresis.

Some further reduction in the amount of hysteresis caused by voltage and temperature is needed before stable logic gates or bistable memory devices can be fabricated from GaAs-Si\(_2\)N\(_4\) FET's.

Surface state density for the best sample was in the \(10^{12}-10^{13}\) range. Calculated impurity doping for several samples indicates an increase in doping at the surface from a bulk value of \(1.41 \times 10^{17}\) to \(2.4-2.6 \times 10^{17}\) (per cm\(^3\)).
CHAPTER V.

EXPERIMENTAL RESULTS ON N TYPE SUBSTRATES

General

Depositions on N type substrates were made at 700°C at NH$_3$:SiH$_4$ ratios ranging from 25 to 121 to 1. These samples show a very large effect of fast surface states. Figure 34 shows a sample for which a frequency of 1.5 Mc was required to "freeze out" the fast states. The flatband voltage is +20 volts. As in the case of p type samples, depositions made at higher NH$_3$ to SiH$_4$ ratios (62.5 and above) gave surface states that could not respond at 500 Kc.

Figure 35 shows C-V curves for six representative samples. There is considerable difference in samples deposited at the same NH$_3$ to SiH$_4$ ratio, as for example, N30 and N33. N type samples showed much poorer repeatability than p type samples. The flatband voltage for these samples occurs at normalized capacitance values of .905 to .935 for film thickness ranging from 800 to 1200 Å. It can be seen that most samples have flatband voltages greater than 22 volts - corresponding to field strengths greater than 2-3 $\times$ 10$^6$ volts/cm.

The curve for sample N47 is of particular interest since
FIGURE 34. C-V CURVES FOR N SAMPLE SHOWING EFFECT OF FAST SURFACE STATES.
FIGURE 35. NORMALIZED C-V CURVES FOR SAMPLES ON N SUBSTRATES
it lies above the other samples, i.e., it approaches higher values of capacitance at lower voltages, indicating a lower surface state density over much of the band gap. N47 and N60 were processed alike but in a manner different than the other samples shown. In each case the temperature was first taken to 725°C for one minute with nitrogen flowing (5 cu. ft./hr.). The temperature was then lowered to 700°C (in about 15 seconds) and NH₃ and SiH₄ were then turned into the quartz tube to effect the deposition. Although this test was repeated several times, the result obtained with N47 could not be repeated. Other samples processed in this manner gave results similar to samples processed at the same NH₃ to SiH₄ ratio but without the initial pre-heat to 725°C (e.g., compare N60 and N46).

It cannot be concluded, therefore, that the pre-heat cycle produced the improved result obtained in N47. There are sufficient differences between other samples processed alike (e.g., compare N30 and N33), moreover, to suggest that some other factor or factors such as surface finish was responsible. N47 was taken from a different wafer, for example, than the other samples processed with the 725°C preheat (the wafer used for N47 was exhausted). N30 and N33 were taken from the same wafer, however. It is also possible that such factors as differences in the cleaning, contaminants in the quartz tube or in the gases, etc., were responsible. No conclusions can be drawn.
Hysteresis Effects

Although the C-V curves for n type samples are quite different from those for p type samples, the hysteresis effect is very similar. As in the case of p samples, the C-V curves for n samples showed the effect of trap filling and emptying. Application of positive bias results in a shift of the C-V curve toward more positive voltages. The relaxation (trap emptying) was again found to be logarithmic with time. A relaxation rate of .5 to .6 volts per decade (see Figure 36) is in excellent agreement with that of p type samples. Again the traps could be emptied by the application of negative bias – a field of 2-3 x 10^6 volts/cm for 2-5 minutes being sufficient.

Figure 37 shows the shift in zero bias equilibrium capacitance for several samples. As in the case of p type samples, the shape of the curves are quite dependent on the NH_3 to SiH_4 ratio. Samples at low ratio show greatest shift at low fields, while samples having higher NH_3 to SiH_4 ratios (62.5:1 or greater) show the opposite effect. These results are in good agreement with those for p type samples. The curve for N47, interestingly, is noticeably different from the other samples deposited at 62.5:1.

Impurity Redistribution

Table 3 gives the calculated impurity doping for six n type samples. The calculation was based on the depletion approximation. The substrate was tellurium doped and had a measured doping density
FIGURE 36. RELAXATION AS TRAPS EMPTY.
FIGURE 37. CURVE SHIFT FOR N TYPE SAMPLES WITH POSITIVE APPLIED VOLTAGE.
of $3.8 \times 10^{16}$ (atoms/cm$^3$). As for p samples, the calculated values indicate an increase in doping density at the surface after deposition of the Si$_3$N$_4$.

Table 3

Calculated Doping Density for N Substrates

<table>
<thead>
<tr>
<th>Sample</th>
<th>NH$_3$:SiH$_4$</th>
<th>Dep. Temp.</th>
<th>Doping Density (per cm$^3$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>N30</td>
<td>25:1</td>
<td>700°C</td>
<td>$5.23 \times 10^{16}$</td>
</tr>
<tr>
<td>N33</td>
<td>25:1</td>
<td>700°C</td>
<td>$6.24 \times 10^{16}$</td>
</tr>
<tr>
<td>N46</td>
<td>62.5:1</td>
<td>700°C</td>
<td>$5.14 \times 10^{16}$</td>
</tr>
<tr>
<td>N47</td>
<td>62.5:1</td>
<td>700°C</td>
<td>$6.43 \times 10^{16}$</td>
</tr>
<tr>
<td>N60</td>
<td>62.5:1</td>
<td>700°C</td>
<td>$6.62 \times 10^{16}$</td>
</tr>
<tr>
<td>N64</td>
<td>121:1</td>
<td>700°C</td>
<td>$5.18 \times 10^{16}$</td>
</tr>
</tbody>
</table>

Density of Surface States

Figure 38 shows the experimental and theoretical curves for the n type sample exhibiting a C-V curve having the least deviation from the theoretical curve. The experimental curve was obtained by first adjusting the applied voltage to +30 volts (to fill the traps) and then taking data as the voltage was decreased back through zero to negative voltages. This procedure minimizes the
FIGURE 38. EXPERIMENTAL AND THEORETICAL CURVES FOR BEST N TYPE SAMPLE.

N47
1200 Å Si₃N₄
on 3.8 x 10¹⁶ N⁺ GaAs
NH₃:SiH₄ = 62.5:1
Dep. Temp. = 700°C
effect of hysteresis as was discussed in Chapter IV. The density of surface states (per cm², per volt) is given in Figure 39. The lowest surface state density occurs in the middle portion of the band gap and is $2 \times 10^{12}$. This is twice the lowest value obtained for the best p type sample.

Summary

The C-V curves for n type samples showed much less repeatability than curves for p type samples. The flatband voltage for all samples occurred at rather high positive voltages (> 15 volts). This is in contrast to negative flatband voltages obtained for p type samples. This difference suggests that the surface states are of the acceptor type (i.e., negative when below the Fermi level).

In contrast to the dissimilarity in C-V curves for n and p samples, the hysteresis effects were quite similar. As for p samples, the n samples show the effect of trap filling and emptying. Relaxation (emptying) of filled traps is again very slow and logarithmic in time. Again, the traps could be emptied in a few minutes by the application of a negative bias. The dependence of curve shift on the $\text{NH}_3: \text{SiH}_4$ ratio was in close agreement with results on p type samples. These results suggest that the hysteresis effects are similar for the two type substrates and are dependent on the $\text{Si}_3\text{N}_4$ deposition.

Surface state density for the best sample was in the $10^{12}$-$10^{13}$
**FIGURE 39. SURFACE STATE DENSITY FOR BEST N SAMPLE.**

Sample N47
1200 Å SiN
on $3.8 \times 10^{16}$ N GaAs
range - a low density of $2 \times 10^{12}$ occurring in the mid one third of the band gap. Calculated impurity doping for several samples indicates an increase in doping at the surface from a bulk value of $3.8 \times 10^{16}$ to $5-6 \times 10^{16}$. 
APPENDIX

Steps in Evaluating Theoretical C-V Curve

Given below are the steps used in formulating a computer program to determine the theoretical high frequency C-V curve for this work. The reader unfamiliar with this area is referred to references [43] and [44]. It is assumed that the following experimental data is available:

\[ C_{\text{max}} = C_{\text{ins}} \]
\[ C_{\text{min}} \]

Area of field plate

\[ n_i = \text{intrinsic carrier concentration} \quad (9 \times 10^{12}/m^3 \text{ for GaAs}) \]
\[ \varepsilon_S = \text{dielectric constant of substrate} \quad (12 \times \varepsilon_0 \text{ for GaAs}) \]
\[ T = \text{temperature (°K)} \]

1. Normalize \( C_{\text{max}} \) and \( C_{\text{min}} \) to MKS system (farads/m^3)
2. Find minimum value of semiconductor capacitance \( C_{S(\text{min})} \) from

\[ C_{\text{min}} = \frac{C_{\text{max}} C_{S(\text{min})}}{C_{\text{max}} + C_{S(\text{min})}} \]

\[ C_{S(\text{min})} = \frac{C_{\text{min}} C_{\text{max}}}{C_{\text{max}} - C_{\text{min}}} \]
3. Evaluate the doping density \(|N_A - N_D|\) at the surface (depletion approximation) by satisfying the equation

\[
C_S(\text{min}) = \frac{\varepsilon_S}{L_D} \left[ \frac{|N_A - N_D|}{2n_i} \right]^{1/2} \cdot \left[ 4 \ln \frac{|N_A - N_D|}{n_i} \right]^{-1/2}
\]

where

\[
L_D = \left[ \frac{KT}{q} \frac{\varepsilon_S}{2q n_i} \right]^{1/2}
\]

4. Determine the Fermi Level \(U_F\) from \(N_A - N_D = 2n_i \sinh U_F\)

5. For the accumulation and depletion regions and for the inversion region where \(|U_S| < 2|U_F|\) (weak inversion) the semiconductor capacitance \(C_s\) can be found as a function of surface potential \(\phi_S\) from

\[
C_s(\phi_S) = \frac{dQ_s}{d\phi_S}
\]

\[
= -\frac{2q}{KT} \left[ \frac{U_S}{U_F} \right]^2 n_i L_D \left\{ \frac{\sinh (U_S-U_F) + \sinh U_F}{2 [\cosh (U_S-U_F) - \cosh U_F + U_S \sinh U_F]} \right\}^{1/2}
\]

where

\[
U_S = \phi_S \frac{q}{KT}
\]

6. Evaluate total charge in semiconductor (per unit area) as a function of \(\phi_S\) from

\[
Q_s(\phi_S) = -\frac{U_S}{|U_S|} q n_i L_D \left\{ \frac{2 [\cosh (U_S-U_F) - \cosh U_F + U_S \sinh U_F]}{2 [\cosh (U_S-U_F) - \cosh U_F + U_S \sinh U_F]} \right\}^{1/2}
\]
7. For conditions of step 5 above, the theoretical capacitance \( \text{(C)} \) is

\[
C(\phi_S) = \frac{C_{\text{max}} C_S(\phi_S)}{C_S(\phi_S) + C_{\text{max}}}
\]

The dependence of applied voltage on \( \phi_S \) can be found from

\[
V_{\text{app.}}(\phi_S) = \frac{Q_S(\phi_S)}{C_{\text{max}}} - \phi_S
\]

For Strong Inversion \(|U_s| > 2|U_F|\):

8. Evaluate charge due to minority carriers from

\[
Q_n = -\frac{U_S}{|U_S|} q n_i L_D \int_{-U_F}^{U_S} \frac{e^{-U_F u} \frac{d}{du} \left\{ 2 \left[ \cosh (U-U_F) - \cosh U_F + U \sinh U_F \right] \right\}^{1/2}}{2 \left[ \cosh (U-U_F) - \cosh U_F + U \sinh U_F \right]}
\]

9. Find effective depletion layer width as a function of \( \phi_S \)

\[
X(\phi_S) = \frac{Q_S - Q_N}{q (N_A - N_D)}
\]

10. Find the semiconductor capacitance \( C_S \) from

\[
C_S(\phi_S) = \frac{\varepsilon_S}{X(\phi_S)}
\]

The dependence of applied voltage on \( \phi_S \) being

\[
V_{\text{app.}}(\phi_S) = \frac{Q_S(\phi_S)}{C_{\text{max}}} - \phi_S
\]
11. Determine the total theoretical capacitance from

\[ C(\phi_S) = \frac{C_{\text{max}} C_S(\phi_S)}{C_S(\phi_S) + C_{\text{max}}} \]
REFERENCES


