INFORMATION TO USERS

This manuscript has been reproduced from the microfilm master. UMI films the text directly from the original or copy submitted. Thus, some thesis and dissertation copies are in typewriter face, while others may be from any type of computer printer.

The quality of this reproduction is dependent upon the quality of the copy submitted. Broken or indistinct print, colored or poor quality illustrations and photographs, print bleedthrough, substandard margins, and improper alignment can adversely affect reproduction.

In the unlikely event that the author did not send UMI a complete manuscript and there are missing pages, these will be noted. Also, if unauthorized copyright material had to be removed, a note will indicate the deletion.

Oversize materials (e.g., maps, drawings, charts) are reproduced by sectioning the original, beginning at the upper left-hand corner and continuing from left to right in equal sections with small overlaps.

Photographs included in the original manuscript have been reproduced xerographically in this copy. Higher quality 6" x 9" black and white photographic prints are available for any photographs or illustrations appearing in this copy for an additional charge. Contact UMI directly to order.

ProQuest Information and Learning
300 North Zeeb Road, Ann Arbor, MI 48106-1346 USA
800-521-0600

UMI®
Roundtrip Design Strategy of High-Speed Delta-Sigma A/D Converters

DISSERTATION

Presented in Partial Fulfillment of the Requirements for the Degree Doctor of Philosophy in the Graduate School of The Ohio State University

By

Jian-Yi Wu, BSEE, MSEE

* * * * *

The Ohio State University

2001

Dissertation Committee:
Professor Steven B. Bibyk, Adviser
Professor Mohammed Ismail
Professor Joanne DeGroat

Approved by
Professor Steven B. Bibyk
Adviser
Department of Electrical Engineering
ABSTRACT

With the advance of process technologies, analog circuits are integrated with digital circuits to form system-on-a-chip (SoC). Compared with digital circuits, the sizes of analog circuits are small. However, their development time usually dominates time-to-market of products, since analog circuits are sensitive to noises and circuit nonidealities. Redesign is necessary when process technologies migrate, but design reuse is not easy for analog circuits. Therefore, very limited synthesis exists in analog circuit design and makes development time longer than that in digital circuits.

In order to accelerate analog circuit design, design strategies are proposed to reduce redundant efforts and improve designers’ productivity. The strategies also offer some required design procedures that are important in circuits. Traditional top-down design strategy is not sufficient for analog circuits. Analog behavioral modeling and some backtrackings are required to ensure desired performance in different design stages. Therefore, roundtrip design strategy (top-down design and bottom-up verification) with enhanced behavioral models is proposed to minimize the unnecessary tasks in designing analog circuits. There are three accomplishments in this dissertation:
1. A novel behavioral model for Delta-Sigma modulators is invented to combine time domain analysis with noise effects. With updated simulation results (transient analysis and AC analysis) from circuit simulators, virtual tests from behavioral simulations can help designers find potential problems in early design stages. Design margins for parameter variation from statistical information are also maintained in this model.

2. A high-resolution (14-bit) high-speed (2-Msamples/s) Delta-Sigma modulator is designed, modeled and fabricated in AMI 0.5um CMOS technology to demonstrate the roundtrip design flow.

3. This behavioral model is implemented in different popular computer tools/languages: MATLAB, VHDL-AMS, Java and C/C++. By following brief comparisons at the end of this dissertation, designers can choose suitable tool/language to build their own behavioral models based on their needs.
This is dedicated to my wife and my son
I would like to thank Prof. Steven B. Biblyk, my adviser, for his thoughts and
guidance throughout my research. I wish to thank Prof. Mohammed Ismail for his
suggestions in my studies. Many thanks go to Prof. Joanne DeGroat for being on my
committee and reading my dissertation. Special thanks should go to Mr. James Cheng
for helping me build behavioral models in different computer languages. I am indebted
to all the IE members for their help during my research. Finally, I am particularly
appreciative of my wife, Ming-Liang Cheng, for her unceasing encouragement and my
son, Andy Wu, for bringing numerous joys in my daily life.
VITA

October 23, 1970 .............................. Born - Taipei, Taiwan, R.O.C.

June, 1993 ........................................ B.S. Electrical Engineering,
                          The National Cheng-Kung University,
                          Tainan, Taiwan, R.O.C.

1993-1995 ...................................... Second Lieutenant,
                          The R.O.C. Army.

1995-1996 ...................................... Engineer, The Media Company,
                          Taipei, Taiwan, R.O.C.

1996-1998 ...................................... M.S. Electrical Engineering,
                          The Ohio State University,
                          Columbus, Ohio, U.S.A.

1998-1999 ...................................... Graduate Research Assistant,
                          The Ohio State University,
                          Columbus, Ohio, U.S.A.

1999-2000 ...................................... Engineer, Intel,
                          Chandler, Arizona, U.S.A.

2000-present ................................. Graduate Research Assistant,
                          The Ohio State University,
                          Columbus, Ohio, U.S.A.

PUBLICATIONS

Research Publications

Jian-Yi Wu and Steven B. Bibyk, "Weaver Architecture With Bandpass Delta-Sigma
A/D Converters". Proceedings of 1998 Midwest Symposium on Circuits and Systems,

**FIELDS OF STUDY**

Major Field: Electrical Engineering

Studies in:

- Topic 1 Circuits and Electronics
- Topic 2 Communications and Signal Processing
TABLE OF CONTENTS

Abstract ................................................................................................................................. ii
Dedication .............................................................................................................................. iv
Acknowledgments ................................................................................................................ v
Vita ........................................................................................................................................ vi
List of Tables ....................................................................................................................... xi
List of Figures ................................................................................................................... xii

Chapters:

1. Introduction ................................................................................................................ 1
   1.1 Obstacles in Mixed-Signal Circuit Design ................................................ 1
       1.1.1 High Sensitivity to Circuit Noise and Nonidealities ................ 2
       1.1.2 Long Simulation Time of Circuit Simulators .................... 3
   1.2 Design Strategy ........................................................................................ 4
       1.2.1 Top-down Design Flow .................................................. 4
       1.2.2 Roundtrip Design Flow .................................................. 5
   1.3 Roundtrip Design Flow with Enhanced Analog Behavioral Model . 6

2. Modeling of Delta-Sigma Modulators ................................................................ 10
   2.1 Proposed Structure of Analog Behavioral Model .................................. 10
   2.2 Second-Order Delta-Sigma Modulator in Boser’s Structure ............ 11
   2.3 Finite Oversampling Ratio ..................................................................... 12
   2.4 Finite Opamp Gain ............................................................................... 13
   2.5 Integrator Model .................................................................................... 15
2.5.1 Integrating Phase .......................................................... 17
2.5.2 Sampling Phase .............................................................. 18
2.5.3 Capacitance Variation ....................................................... 19
2.5.4 Gain Variation in Opamp .................................................. 22
2.5.5 Combinations of Nonlinearities ......................................... 22
2.6 Comparator Model .............................................................. 25
2.7 Switch Model ....................................................................... 27
2.7.1 Charge Injection and Clock Feedthrough from Switches ...... 27
2.7.2 Harmonic Distortion in Switches ....................................... 33
2.7.3 Waveform Delay Caused by On-Resistance of Switches ...... 34
2.8 Fabrication Nonidealities ...................................................... 35
2.8.1 Parameter Shifting ........................................................... 36
2.8.2 Mismatches ................................................................. 36

3. Noise Analysis ........................................................................ 38
3.1 Spectrum of Delta-Sigma Modulators ................................... 38
3.2 Switch Noise ......................................................................... 39
3.3 Opamp Noise ......................................................................... 41
3.4 Jitter Noise ........................................................................... 43
3.5 Summary of Nonideal Effects in Delta-Sigma Modulators .... 47

4. Design Example for 14-bit 16 kS/s Delta-Sigma A/D Converter ... 48
4.1 Architecture Selection .......................................................... 48
4.2 Behavioral Modeling Designing ............................................. 49
4.3 Parameter Initialization ........................................................ 49
4.4 Behavioral Simulation .......................................................... 49
4.5 Circuit Component Implementation ........................................ 51
4.5.1 Opamp Design ............................................................... 51
4.5.2 Switch Design ............................................................... 53
4.5.3 Comparator Design ......................................................... 55
4.6 Verification .......................................................................... 57
4.7 Expected Performance with fabrication variation .................. 57

5. Design Example for 14-bit 2-Msamples/s High-Speed Delta-Sigma A/D Converter ........................................................................ 63
5.1 Circuit Parameter Initialization ............................................. 63
5.1.1 Integrator Parameters ...................................................... 64
5.1.2 Comparator Parameters ................................................... 69
5.1.3 Switch Parameters .......................................................... 69
<table>
<thead>
<tr>
<th>Section</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>5.1.4 Capacitor Parameters</td>
<td>71</td>
</tr>
<tr>
<td>5.1.5 Jitter Noise</td>
<td>71</td>
</tr>
<tr>
<td>5.2 Behavioral Simulations</td>
<td>73</td>
</tr>
<tr>
<td>5.3 Circuit Component Implementation</td>
<td>77</td>
</tr>
<tr>
<td>5.3.1 Opamp Implementation</td>
<td>78</td>
</tr>
<tr>
<td>5.3.2 Switch Implementation</td>
<td>84</td>
</tr>
<tr>
<td>5.3.3 Integrator Implementation</td>
<td>85</td>
</tr>
<tr>
<td>5.3.4 Comparator Implementation</td>
<td>85</td>
</tr>
<tr>
<td>5.4 Verification</td>
<td>87</td>
</tr>
<tr>
<td>5.5 Bottom-Up Verifications</td>
<td>88</td>
</tr>
<tr>
<td>6. Conclusions and Recommendations</td>
<td>95</td>
</tr>
<tr>
<td>6.1 Conclusions</td>
<td>95</td>
</tr>
<tr>
<td>6.2 Recommendations</td>
<td>96</td>
</tr>
<tr>
<td>6.2.1 Modeling in MATLAB</td>
<td>96</td>
</tr>
<tr>
<td>6.2.2 Modeling in VHDL-AMS</td>
<td>97</td>
</tr>
<tr>
<td>6.2.3 Modeling in Java</td>
<td>100</td>
</tr>
<tr>
<td>6.2.4 Modeling in C/C++</td>
<td>101</td>
</tr>
<tr>
<td>6.2.5 Summary</td>
<td>101</td>
</tr>
</tbody>
</table>

Bibliography | 103 |
# LIST OF TABLES

<table>
<thead>
<tr>
<th>Table</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.1 Summary of nonideal effects in Delta-Sigma modulators</td>
<td>47</td>
</tr>
<tr>
<td>4.1 Simulation specifications in analog behavioral model in MATLAB</td>
<td>51</td>
</tr>
<tr>
<td>4.2 Simulation specifications in analog behavioral model in MATLAB</td>
<td>59</td>
</tr>
<tr>
<td>4.3 Summary of performance in the 2nd-order Delta-Sigma A/D converter</td>
<td>62</td>
</tr>
<tr>
<td>5.1 Parameters for initialization</td>
<td>65</td>
</tr>
<tr>
<td>5.2 Summary of initialized parameters</td>
<td>72</td>
</tr>
<tr>
<td>5.3 Tolerance for capacitor mismatch with maximum SNR 1dB drop</td>
<td>77</td>
</tr>
<tr>
<td>5.4 Summary of circuit parameters verified by behavioral simulations</td>
<td>81</td>
</tr>
<tr>
<td>5.5 Circuit parameters of comparator from PSPICE</td>
<td>86</td>
</tr>
<tr>
<td>5.6 Summary of circuit parameters from behavioral and PSPICE simula-</td>
<td>88</td>
</tr>
<tr>
<td>tions</td>
<td></td>
</tr>
<tr>
<td>5.7 Summary of bottom-up verifications for the performance of 4th-order Delta-Sigma A/D converter</td>
<td>94</td>
</tr>
</tbody>
</table>
## LIST OF FIGURES

<table>
<thead>
<tr>
<th>Figure</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.1</td>
<td>Some required simulations in opamp design</td>
<td>2</td>
</tr>
<tr>
<td>1.2</td>
<td>Circuit diagram of the 1st-order Delta-Sigma Modulator</td>
<td>3</td>
</tr>
<tr>
<td>1.3</td>
<td>Simulation result of 1st-order DSM with PSPICE</td>
<td>4</td>
</tr>
<tr>
<td>1.4</td>
<td>Block diagram of top-down design flow in [1]</td>
<td>5</td>
</tr>
<tr>
<td>1.5</td>
<td>Block diagram of roundtrip design flow</td>
<td>6</td>
</tr>
<tr>
<td>1.6</td>
<td>Proposed functions of analog behavioral model to accelerate analog circuit design for A/D converters</td>
<td>8</td>
</tr>
<tr>
<td>1.7</td>
<td>Proposed design flow for converting system specifications to circuit specifications by behavioral simulations</td>
<td>9</td>
</tr>
<tr>
<td>2.1</td>
<td>Proposed structure of analog behavioral model for integrators</td>
<td>11</td>
</tr>
<tr>
<td>2.2</td>
<td>Block diagram of 2nd-order $\Delta$-$\Sigma$ modulator with Boser's structure</td>
<td>12</td>
</tr>
<tr>
<td>2.3</td>
<td>Resolution vs. OSR with Boser structure</td>
<td>13</td>
</tr>
<tr>
<td>2.4</td>
<td>Modified block diagram of 2nd-order $\Delta$-$\Sigma$ modulator with finite opamp gain</td>
<td>14</td>
</tr>
<tr>
<td>2.5</td>
<td>Power spectral density of 2nd-order $\Delta$-$\Sigma$ modulator with gain = $\infty$ and 100</td>
<td>15</td>
</tr>
<tr>
<td>2.6</td>
<td>Block diagram of switched capacitor integrator</td>
<td>16</td>
</tr>
</tbody>
</table>
4.10 Power spectral density from analog behavioral model in PSPICE ........................................ 58

4.11 Power spectral density of the output of 2nd-order modulator from behavioral simulation with noise consideration ......................................................... 59

4.12 Power spectral density of intermodulation test ................................................................. 60

4.13 Block diagram of 3-stage comb filter with 128 downsampling .......................................... 61

4.14 SNR, SNDR, SFDR of 2nd-order Delta-Sigma A/D Converter ........................................ 61

4.15 Harmonic distortions of 2nd-order Delta-Sigma A/D Converter ........................................ 62

5.1 the block diagram of MASH211 structure ........................................................................... 64

5.2 Relationship of SNR with open-loop gain and oversampling rate ...................................... 67

5.3 Relation between $V_{out}$ and $A_0$ ...................................................................................... 68

5.4 Relationship of SNR with open-loop gain and oversampling rate ...................................... 70

5.5 Power spectral density of the Delta-Sigma modulator with $f_{in} = 156.25kHz$, $f_s = 40MHz$, $A_{in} = 0.25V$ and $\Delta = 1V$ ......................................................... 74

5.6 SNR and SNDR of the Delta-Sigma A/D converter with $f_{in} = 156.25kHz$, $f_s = 40MHz$, $\Delta = 1V$ and $M = 20$ ................................................................. 75

5.7 Power spectral density of the Delta-Sigma modulator with $f_{in} = 156.25kHz$, $f_s = 40MHz$, $A_{in} = 0.25V$, $\Delta = 1V$ and improved open-loop gain .................................. 76

5.8 Power spectral density of the Delta-Sigma modulator with $f_{in} = 156.25kHz$, $f_s = 40MHz$, $A_{in} = 0.25V$, $\Delta = 1V$, $g_m = 2.1mA/V$ and $I_o = 370uA$ ........................................ 77

5.9 SNR and SNDR of the Delta-Sigma A/D converter with $f_{in} = 156.25kHz$, $f_s = 40MHz$, $\Delta = 1V$ and $M = 20$ ................................................................. 78

5.10 SNR and SNDR of the Delta-Sigma A/D converter with $f_{in} = 156.25kHz$, $f_s = 40MHz$, $\Delta = 1V$ and $M = 20$ in slow corner .............................................. 79

5.11 SNR and SNDR of the Delta-Sigma A/D converter with $f_{in} = 156.25kHz$, $f_s = 40MHz$, $\Delta = 1V$ and $M = 20$ in fast corner ............................................... 80

xv
5.12 Circuit diagram of fully differential folded cascode opamp with gain boosting .................................................. 82
5.13 Transconductance and output currents of fully differential folded cascode opamp with gain boosting .................. 82
5.14 Relation of $V_{out}$ and $A_{0}$ of fully differential folded cascode opamp with gain boosting .................................. 83
5.15 Phase margin and unity gain frequency of fully differential folded cascode opamp with gain boosting .................. 84
5.16 Noise analysis of fully differential folded cascode opamp with gain boosting .................................................. 85
5.17 Power spectral density of switch harmonic distortion .......... 86
5.18 Circuit diagram of latch comparator with preamplifier .......... 87
5.19 Result comparison of MATLAB and PSPICE for switched-capacitor integrator .................................................. 89
5.20 Power spectral density derived from PSPICE with 256-point Hanning window FFT .............................................. 90
5.21 Predicted power spectral density of 4th-order Delta-Sigma modulator with noises ............................................. 91
5.22 Intermodulation test of 4th-order Delta-Sigma modulator with noises ............................................................... 91
5.23 Predicted SNR, SNDR and SFDR of 4th-order Delta-Sigma A/D converter ............................................................. 92
5.24 Predicted harmonic distortions of 4th-order Delta-Sigma A/D converter ............................................................... 92
5.25 SNR in different process corners of 4th-order Delta-Sigma A/D converter ............................................................. 93
5.26 Layout for the 4th-order Delta-Sigma modulator ................. 93
6.1 Simulation time of 4th-order Delta-Sigma modulator in C/C++, Java, VHDL-AMS and MATLAB (only for my research) ........................................... 97

6.2 Simulation result of 4th-order Delta-Sigma modulator in VHDL-AMS 99

6.3 Simulation result of 4th-order Delta-Sigma modulator in VHDL-AMS 99

6.4 Power spectral density of 4th-order Delta-Sigma modulator with 16384-point Hanning window FFT ......................................................... 100

6.5 Simulation result of 4th-order Delta-Sigma modulator in Java ........ 101
CHAPTER 1

INTRODUCTION

This chapter discusses design strategies for mixed-signal circuit design. Top-down design flow is not suitable for analog circuits. Roundtrip design flow (top-down design and bottom-up verification) with enhanced behavioral models is proposed to overcome long simulation time for analog circuit design and reduces the chance of repeating circuit simulations for proper circuit parameters.

1.1 Obstacles in Mixed-Signal Circuit Design

With the advance of process technology, analog circuits can be integrated in digital circuits to form a mixed-signal system on a chip (SoC). According to [1], the percentage of analog/mixed signal circuits in SoC in 1999 increases by 11% compared with the percentage in 1997. Although the size of analog circuits is smaller than that in digital circuits, it often takes longer development time to design analog circuits. Therefore, a good design strategy is necessary for analog circuit designers to reduce development time. Before discussing the design strategy, we need to investigate what are the problems for designing analog circuits.
1.1.1 High Sensitivity to Circuit Noise and Nonidealities

The information of digital circuits is generated and discriminated above (or 1) or below (or 0) some threshold values. If information magnitude is strong enough and the threshold values are well chosen, the circuits are insensitive to noise and circuit nonidealities. However, the information carried in analog circuits exists in the magnitude of voltage, current etc. Any minor interference in magnitude directly causes a change in the information. Therefore, analog circuits are comparatively sensitive to noise and circuit nonidealities. It leads to the fact that there are more circuit specifications in analog circuits than the specifications in digital circuits in order to specify the functions of circuit components. Figure 1.1 shows some required simulations in opamp design. Actually, if designers modify the circuits for meeting some specifications, very often some other specifications will change. It is necessary to recheck whether the other specifications still meet the requirements or not.

![Figure 1.1: Some required simulations in opamp design](image-url)
1.1.2 Long Simulation Time of Circuit Simulators

Circuit simulators (like SPICE) have good accuracy but long simulation time when circuit size is large [2] [3] [4]. Figure 1.2 shows the circuit diagram for 1st-order Delta-Sigma modulator. In Figure 1.2, a fully differential opamp is used as the switched-capacitor integrator. Sampling capacitors $C_s$, integrating capacitors $C_i$ and feedback capacitors $C_f$ are equal to $5pF$. The sampling frequency is $128KHz$ with $1KHz$ sinusoidal input signal. Simulation result is indicated in Figure 1.3. The simulation time for $5ms$ (5 periods of sine wave) transient analysis takes more than 6 hours in Pentium III 500MHz PC with 256 MB RAM. For spectral measurement, only $0.005 \times 128000 = 640$ samples are obtained. If the downsampling rate is 64, only 10 samples are derived after decimation stage. The number of samples is insufficient to obtain the detailed behaviors of low frequency components (usually several Ksamples needed).

![Circuit diagram of the 1st-order Delta-Sigma Modulator](image)

Figure 1.2: Circuit diagram of the 1st-order Delta-Sigma Modulator
1.2 Design Strategy

Design strategy is applied to minimize efforts of design engineers and to increase the yield rate of products. Therefore, in the design flow, not only are circuit nonidealities considered, but also mismatch and parameter shifting due to process conditions are emphasized. The design strategies discussed in this section are top-down design flow and roundtrip design flow.

1.2.1 Top-down Design Flow

Top-down design flow is widely used in digital circuit design [4]. The system is divided into several blocks based on their functions (behaviors). Designers can write hardware description language (HDL) to simulate the behaviors of the blocks. Synthesis and automatic layout functions are often available according to the libraries. The design flow, which reuses the designs in libraries to form the circuits of the whole system, enables designers to finish design projects in short time. But for analog circuits, this design flow is not suitable because of the following reasons:
1. The specifications of analog circuits are not easy to specify from system requirements. Repeatedly using circuit simulators is sometimes unavoidable to decide these parameters within some range.

2. Analog circuit libraries for synthesis are not popular because of sensitivity to circuit nonidealities and process variation \[1\]. Different process technologies often cause analog circuit designers to redesign the circuit components.

3. In Figure 1.4, designers should ensure that analog circuits still meet the required performance when design stages change. Therefore, backtrackings are necessary in the design flow \[1\].

![Figure 1.4: Block diagram of top-down design flow in \[1\]](image)

### 1.2.2 Roundtrip Design Flow

Roundtrip design flow includes not only top-down design flow but also backtrackings from lower stages to upper stages. These backtrackings are used to ensure that when design proceeds to later stages, the performance of the system still meets the
requirements. Figure 1.5 show the block diagram of roundtrip design flow. Although roundtrip design flow includes top-down design and bottom-up verification procedures, it still has the following problems:

1. In bottom-up verification, what kind of tools can be used in performance evaluation? If circuit simulators are used, long simulation time will make circuit simulators impractical when time to market is emphasized.

2. If behavioral simulations are used to estimate system performance, how do we find the balance point between accuracy and simulation time [4]?

![Figure 1.5: Block diagram of roundtrip design flow](image)

1.3 Roundtrip Design Flow with Enhanced Analog Behavioral Model

In order to overcome the problems mentioned in previous sections, the enhanced analog behavioral model is proposed as shown in Figure 1.6. The main functions are indicated as follows:
1. The behavioral simulation helps designers specify the circuit parameters in order to avoid using circuit simulators repeatedly [5].

2. The behavioral simulation needs to reveal the system performance in which designers are interested [3].

Based on the functions mentioned above, more detailed design flow is shown in Figure 1.7. In Figure 1.7, architecture selection is the first step in the flow. Then according to the architecture, designers can build their own analog behavioral models for simulation to find the potential circuit parameters. After these parameters are specified, circuit components are implemented to meet the requirements. If the circuit parameters are not achievable, designers need to find possible trade-offs in circuit parameters and possible circuits. Re-running the behavioral simulations for verifying the new parameters is necessary before circuit implementation. If designers cannot find any circuit to achieve desired performance, they have to reconsider different architectures. After all circuit components are implemented, a short period of circuit simulation for the whole structure may be helpful to verify the behavioral model. The worst case is that the behavioral model is not accurate enough. In this case, designers need to modify the models and return to early design stage. If the result is correct, designers can update the circuit parameters in the behavioral model. The purposes of parameter update are discussed as follows:

1. To find potential problems in early design stage: Designers can update the circuit parameters from process corners and mismatch to find potential problems for the whole performance before test chips are tested [6].
2. To generate sufficient data for other designers: For Delta-Sigma A/D converters, designers of the modulators can use the behavioral model to generate sufficient data for designers of decimation stage as for the digital spectral measurement.

3. To protect manufacturer's IP: The behavioral model can be used by customers for evaluating the performance without reveal detail circuitry.

In this dissertation, a novel behavioral model is introduced in Chapter 2 in time domain analysis. Noise effects, which are critical but sometimes ignored, are analyzed in Chapter 3 to enhance insufficiency in transient analysis. Two design examples are demonstrated in this research. A single stage 2nd-order Delta-Sigma Modulator is designed in Chapter 4. A multi-stage 4th-order Delta-Sigma Modulator in Chapter 5. Chapter 6 concludes the results of this research and different computer tools/languages are used in the behavioral model to help designers choose wisely based on their needs.

Figure 1.6: Proposed functions of analog behavioral model to accelerate analog circuit design for A/D converters
Figure 1.7: Proposed design flow for converting system specifications to circuit specifications by behavioral simulations
CHAPTER 2

MODELING OF DELTA-SIGMA MODULATORS

This chapter demonstrates the nonideal effects in Delta-Sigma modulators and the methods to model these phenomena. A new behavioral model of Delta-Sigma modulators is proposed for designers to fulfill roundtrip design procedure. The power spectral density of the 2nd-order Delta-Sigma modulator is used to indicate the effects of the nonidealities.

2.1 Proposed Structure of Analog Behavioral Model

In Chapter 1, the requirements for analog behavioral model is sufficient accuracy, short simulation time and high expandability. In order to achieve the goals, by using SC integrators as the example, the proposed structure of analog behavioral model for integrators is shown in Figure 2.1. The advantages of the structure are indicated as follows:

1. Noises are expressed as the input sources of the integrator. When high-order Delta-Sigma modulators are desired, with little modification, designers can easily cascade several integrator models and add or delete noise sources depending on the required accuracy to trade off simulation speed.
2. Model modification is easily achieved. If designers like to change jitter noise model, only old subroutine is replaced with new one without severe modification.

Designers can fulfill the structure in Figure 2.1 with any tools like C/C++, Verilog-A, VHDL-AMS and MATLAB. MATLAB is used in this dissertation because of powerful DSP toolbox and is well known by engineers not only in circuit designers.

Figure 2.1: Proposed structure of analog behavioral model for integrators

2.2 Second-Order Delta-Sigma Modulator in Boser’s Structure

2nd-order Delta-Sigma A/D converter is widely used in audio application. Figure 2.2 shows the block diagram of 2nd-order Delta-Sigma modulator with Boser's structure [7]. This structure is very efficient because of the following two reasons:

1. No feedback capacitors are used in the structure. Smaller layout area, less thermal noise and higher speed can be achieved.
2. The first-stage integrator can be used as the second-stage integrator. It can reduce development time for circuit designers and mask designers. For testing chip, only one opamp design is used. Thus, it also saves time for test engineers.

The disadvantage is that the coefficients are not optimal for bit resolution. But it is still a very good example to investigate the phenomena of circuit nonidealities.

![Block diagram](image)

Figure 2.2: Block diagram of 2nd-order Δ-Σ modulator with Boser's structure

### 2.3 Finite Oversampling Ratio

The transfer function in Figure 2.2 can be derived as:

\[
V_{\text{out}}(z) = S_{TF}(z)V_{\text{in}}(z) + N_{TF}(z)E(z)
\]

\[
= \frac{z^{-2}}{P(z)}V_{\text{in}}(z) + 4\frac{(1 - z^{-1})^2}{P(z)}E(z)
\]

(2.1)

where \(E(z)\) is the z transform of quantization noise and \(P(z) = z^{-2} + 2z^{-1}(1 - z^{-1}) + 4(1 - z^{-1})^2\). When sampling frequency \(f_s\) is much larger than signal frequency \(f_{\text{in}}\) (or oversampling ratio (OSR or \(M\), is defined as \(\frac{f_s}{2f_{\text{in}}}\)), \(z^{-1}\) is close to 1 and \(|P(z)|\) is close to 1. Therefore, the signal transfer function \(S_{TF}\) is only 2 sampling clock delays and the noise transfer function \(N_{TF}\) works as a 2nd-order high-pass filter.
With the assumption that quantization noise is uniformly distributed between $-\frac{f_s}{2}$ and $\frac{f_s}{2}$, SNR (Signal-to-Noise Ratio) is evaluated in (2.2) with 1-bit stream output. Figure 2.3 shows the relation of resolution and oversampling rate with Boser’s structure. From the figure, if 17-bit resolution is desired, $OSR$ is at least 256.

$$SNR = 50 \log(OSR) - 17.16 \text{ dB} \quad (2.2)$$

![Figure 2.3: Resolution vs. OSR with Boser structure](image)

2.4 Finite Opamp Gain

The block diagram in Figure 2.2 is implemented with switched capacitor circuits. In order to fulfill top-down design procedure, we need to consider circuit nonidealities.
For example, if we add the finite opamp gain \((A_0)\) into consideration, the block diagram in Figure 2.2 will be modified as shown in Figure 2.4.

![Block Diagram](image)

**Figure 2.4:** Modified block diagram of 2nd-order \(\Delta \Sigma\) modulator with finite opamp gain

\[
V_{\text{out}}(z) = S_{TF}(z)V_{\text{in}}(z) + N_{TF}(z)E(z) = \frac{(A_0/2)z^{-1}}{Q(z)} V_{\text{in}}(z) + \frac{4(1 - (A_0+1)/A_0 + 1/2)z^{-1}}{Q(z)} E(z) \tag{2.3}
\]

where \(Q(z) = (A_0/2z^{-1})^2 + 2(A_0/2z^{-1})(1 - (A_0+1)/A_0 + 1/2z^{-1}) + 4(1 - (A_0+1)/A_0 + 1/2z^{-1})^2\).

By using the model in Figure 2.4, we can investigate the effect of finite \(A_0\) to \(\Delta \Sigma\) modulator. Figure 2.5 indicates that finite \(A_0\) increases inband noise floor. However, even though the opamp gain is only 100 V/V (or 40dB), the accumulated noise in signal band has little influence on SNR (103dB and 101dB). This is a good attribute because when opamps are designed to operate fast (in high current), short channel effect is unavoidable and makes output resistance very low. From (2.3), we can conclude that in this \(\Delta \Sigma\) modulator, what we need is fast opamp to support high sampling frequency, not high gain opamp.
In order to estimate settling errors caused by finite gain-bandwidth and slew rate in an integrator, we need to know the behaviors of the integrator first. Figure 2.6 shows the block diagram of switched capacitor (SC) integrator. $\phi_1$ and $\phi_2$ are two nonoverlapped clocks.

In order to investigate the settling behavior, the small signal model of SC integrator is shown in Figure 2.7. In Figure 2.7, $C_L$ is the sum of parasitic capacitance, opamp capacitance and load capacitance. Maximal output current ($I_o$) is limited by the driving capability of the opamp. Therefore, after the input voltage of the opamp

Figure 2.5: Power spectral density of 2nd-order $\Delta-\Sigma$ modulator with gain $= \infty$ and 100

2.5 Integrator Model

In order to estimate settling errors caused by finite gain-bandwidth and slew rate in an integrator, we need to know the behaviors of the integrator first. Figure 2.6 shows the block diagram of switched capacitor (SC) integrator. $\phi_1$ and $\phi_2$ are two nonoverlapped clocks.

In order to investigate the settling behavior, the small signal model of SC integrator is shown in Figure 2.7. In Figure 2.7, $C_L$ is the sum of parasitic capacitance, opamp capacitance and load capacitance. Maximal output current ($I_o$) is limited by the driving capability of the opamp. Therefore, after the input voltage of the opamp
Figure 2.6: Block diagram of switched capacitor integrator

$V_a$ exceeds $\frac{I_o}{g_m}$, the output voltage is limited by the slew rate. In this region, the transconductance is zero because of fixed $I_o$ (no current increment).

Figure 2.7: Small signal model of SC integrator with slew rate limitation

In most of opamp designs, the maximal charge current and discharge current are not always the same. In Figure 2.8, the maximal output current for charging $C_L$ is
\( I_o^- \). The maximal output current for discharging \( C_L \) is \( I_o^+ \). \( V_a^+ \) and \( V_a^- \) are upper and lower boundaries of opamp input voltage without slew rate limitation (linear region).

![Diagram](image)

**Figure 2.8: Transconductance with slew rate limitation**

We can start the equations for transient analysis of integrator. The whole analysis is based on [8] but adds the nonideality \( C_{in} \) as input capacitance of the opamp. In order to avoid ambiguity, we call the period that \( \phi_1 \) is high as sampling phase and the period that \( \phi_2 \) is high as integrating phase. Each period is assumed \( T_s / 2 \) (50% duty cycle). After simplifying the equations, we can obtain:

### 2.5.1 Integrating Phase

When \( V_a^- \leq V_a(0^+) \leq V_a^+ \) (in linear region):

\[
V_a(t) = Ae^{-\frac{g_{eq} t}{C_{eq}}} + B \tag{2.4}
\]

, where \( B = -\frac{1}{g_{eq} R_{eq}} \left[ \frac{C_s}{C_l} V_{in}(n - 1) + V_{out}(n - 1) \right] \), \( A = V_a(0^+) - B \), \( C_{eq} = C_S + C_{in} + C_L (1 + \frac{C_s + C_{in}}{C_l} \) and \( g_{eq} = g_m + \frac{C_s + C_{in} + C_l}{C_l R_o} \).
When $V_a(0^+) > V_a^+$:

$$t_{op} = -\frac{C_{eq}}{g_{eq} - g_m} \ln \left[ \frac{V_{a}^+ - B_1}{V_a(0^+) - B_1} \right]$$ (2.5)

1. If $0 < t \leq t_{op}$, $V_a(t) = A_1 e^{-\frac{g_{eq} - g_m}{C_{eq}} t} + B_1$.

2. If $t_{op} < t \leq \frac{T_0}{2}$, $V_a(t) = (V_a^+ - B)e^{-\frac{g_{eq}}{C_{eq}} (t-t_{op})} + B$.

, where $B_1 = -\frac{C_i}{C_S + C_{in} + C_I} [I_o R_o + C_S V_{in}(n-1) + V_{out}(n-1)]$ and $A_1 = V_a(0^+) - B_1$.

When $V_a^- > V_a(0^+) $:

$$t_{on} = -\frac{C_{eq}}{g_{eq} - g_m} \ln \left[ \frac{V_a^- - B_2}{V_a(0^+) - B_2} \right]$$ (2.6)

1. If $0 < t \leq t_{on}$, $V_a(t) = A_2 e^{-\frac{g_{eq} - g_m}{C_{eq}} t} + B_2$.

2. If $t_{on} < t \leq \frac{T_0}{2}$, $V_a(t) = (V_a^- - B)e^{-\frac{g_{eq}}{C_{eq}} (t-t_{on})} + B$.

, where $B_2 = -\frac{C_i}{C_S + C_{in} + C_I} [I_o R_o + C_S V_{in}(n-1) + V_{out}(n-1)]$ and $A_2 = V_a(0^+) - B_2$.

The relation of $V_a(t)$ and $V_{out}(t)$ can be expressed as:

$$V_{out}(t) = C_S + C_{in} + C_I V_a(t) + C_S V_{in}(n-1) + V_{out}(n-1)$$ (2.7)

### 2.5.2 Sampling Phase

Assuming the drooping of the integrator is ignored, $V_{out}(n)$ is derived as:

$$V_{out}(n) = V_{out}(n - \frac{1}{2}) - V_a(n - \frac{1}{2})$$ (2.8)

In MATLAB, simple equations are used to fulfill the following functions:

function $V_a = V_a-func(V_{ini}, B_{const}, t_{period}, T_{stew}, g_{trans}, C_{eq})$

$$V_a = (V_{ini} - B_{const}) e^{-\frac{g_{eq}}{C_{eq}}(t_{period} - T_{stew})} + B_{const}$$
function $V_{out} = V_{out-func}(V_a, V_{in}(n-1), V_{out}(n-1))$

$$V_{out} = \frac{C_S + C_{in}}{C_I} V_a + \frac{C_S}{C_I} V_{in}(n-1) + V_{out}(n-1)$$

In the linear region, $V_a$ is defined as $V_a-func(V_a(0^+), B, \frac{T_S}{2}, 0, g_{eq}, C_{eq})$. In the other two cases, we can use $V_a-func(V_a^+, B, \frac{T_S}{2}, t_{op}, g_{eq}, C_{eq})$ and $V_a-func(V_a^-, B, \frac{T_S}{2}, t_{on}, g_{eq}, C_{eq})$.

The equations above allow designers to model the effects caused by slew rate and finite gain bandwidth. The phenomenon of slew rate effect in Delta-Sigma modulator is shown in Figure 2.9. Because slew rate is proportional to maximal output current ($I_o$), we can observe the phenomenon of slew rate effect by limiting maximal output current. From Figure 2.9, the lower slew rate (smaller $I_o$) causes larger harmonic distortion than higher slew rate (larger $I_o$). Because unity gain bandwidth is equal to $\omega_u = \frac{\omega_{-3dB}}{\beta_0} = \frac{g_{eq}}{C_{eq}C_{eq}}$ and $g_{eq} \approx g_m$ ($R_o$ is large), we can find in Figure 2.10 that lower $g_m$ raise in-band noise floor.

### 2.5.3 Capacitance Variation

Figure 2.11 shows two types of feedback loops in the integrators of ΔΣ Modulator. The first type of integrator is that sampling signal path and feedback signal path share the same capacitor $C_S$. The other is each path has its own capacitor. The general equation of a capacitor can be expressed as:

$$C = C_0(1 + \alpha v + \beta v^2 + \ldots)$$

(2.9)

If the capacitors are implemented in double poly capacitors, $C \approx C_0(1 + \alpha v)$. For the first type of integrator, according to charge conservation,
Figure 2.9: Slew rate limitation for 2nd-order Delta-Sigma Modulator

\[
\int_{V_{in}}^{b_n V_R} C_S 0 (1 + \alpha v) dv + \int_{V_{n-1}}^{V_n} C_{f0} (1 + \alpha v) dv = 0
\]

\[\Rightarrow V_n = (V_{n-1} + g_i V_{in} - b_n g_i V_R) + \frac{1}{2} \alpha (V_{n-1}^2 + g_i V_{in}^2 + g_i V_R^2 - V_n^2) \tag{2.10}\]

, where \( g_i = \frac{C_{S0}}{C_{f0}} \), \( b_n \) is the output bit stream of the modulator and \( V_R \) is feedback voltage. If \( \alpha = 0 \), the output voltage without capacitor variation \( V_{n(org)} \) is derived as :

\[V_{n(org)} = V_{n-1} + g_i (V_{in} - b_n V_R) \tag{2.11}\]

For a double-poly capacitor, \( \alpha \) is usually very small (several tens ppm), we can substitute \( V_{n(org)}^2 \) in (2.11) into \( V_n^2 \) in (2.10) for simplifying the equation:

\[V_n \approx V_{n(org)} + \frac{1}{2} \alpha (V_{n-1}^2 + g_i V_{in}^2 + g_i V_R^2 - V_{n(org)}^2) \tag{2.12}\]
In (2.12), we find that the variation of capacitance generates harmonic distortion for $V_n$. For the other feedback structure, we can obtain the similar equation as follows:

$$V_n \approx V_{n_{(org2)}} + \frac{1}{2} \alpha (V_{n-1}^2 + g_i V_i^2 + k g_i V_R^2 + V_{n_{(org2)}}^2)$$

(2.13)
\[ V_{n(\text{org2})} = V_{n-1} + g_t(V_{in} - b_n k V_R) \] and \( k = \frac{C_F}{C_G} \). Actually, In MATLAB, it is not necessary to write two scripts for (2.12) and (2.13). We can find that (2.12) is a special case in (2.13) when \( k = 1 \).

### 2.5.4 Gain Variation in Opamp

In Figure 2.11, we choose the structure with the feedback capacitor \( C_F \) as an example. For the consideration of finite opamp gain, the transfer function is modified as follows:

\[
V_o(n) = \frac{A g_t}{A + 1 + g_t(1 + k)} V_i(n - 1) + \frac{(A + 1)}{A + 1 + g_t(1 + k)} V_o(n - 1) \tag{2.14}
\]
\[
V_i(n) = \frac{1}{C_S} (C_S V_{in}(n) - C_F b_n V_R) = V_{in}(n) - k b_n V_R \tag{2.15}
\]

, where \( g_t = \frac{C_S}{C_I} \) and \( k = \frac{C_F}{C_S} \).

Considering \( A = A_0(1 + \alpha V_o + \beta V_o^2) \) and assuming that \( A_0 \) is very large, the following equation is obtained [9]:

\[
V_o(n) \cong V_o(n - 1) + g_t[V_i(n - 1) - C_n + \alpha V_o(n)C_n + \beta V_o^2(n)C_n] \tag{2.16}
\]
\[
C_n = \frac{V_i(n - 1) + (1 + k)V_o(n)}{A_0}
\]

From (2.17), we find that gain variation in opamps causes harmonic distortion. Because in Delta-Sigma modulators, open-loop gain of opamps may not be very large, (2.17) is used only for explaining the phenomenon of gain variation. In the next subsection, the more accurate model will be derived.

### 2.5.5 Combinations of Nonlinearities

Several nonidealities are introduced in previous sections for SC integrators. However, it is a real challenge to combine each nonideal effect to form a single integrator.
model. Let’s start with the settling behavior for SC integrator shown in Figure 2.12 at integrating phase. Basically, $V_{out}(t)$ can be divided into two parts:

$$V_{out}(t) = V_{transient}(t) + V_{steady}$$  \hfill (2.17)$$

![Settling behavior for switched capacitor integrator](Graph.png)

Figure 2.12: Settling behavior for switched capacitor integrator

From the previous sections, the transient voltage can be simplified as the following equation if $R_o$ is large.

$$V_{transient\left(\frac{T_S}{2}\right)} = \frac{C_S + C_{in}(V_a(0^+) - B)}{C_I} e^{-\frac{\alpha_{eq}\cdot T_S}{2}}$$

for $V_a^- \leq V_a(0^+) \leq V_a^+$

$$= \frac{C_S + C_{in}(V_a^+ - B)}{C_I} e^{-\frac{\alpha_{eq}\cdot T_S}{2} - t_{op}}$$

for $V_a^+ < V_a(0^+)$

$$= \frac{C_S + C_{in}(V_a^- - B)}{C_I} e^{-\frac{\alpha_{eq}\cdot T_S}{2} - t_{on}}$$

for $V_a(0^+) < V_a^-$  \hfill (2.18)$$
Steady-state voltage is obtained when time is approximating to infinity as shown in Fig. 2.12. We can also consider capacitance nonlinearity and gain variation in the steady state.

\[
V_{\text{out}}(n) = \frac{A_0 g_i}{g_i(1+k) - g_p + A_0 + 1} [V_{\text{in}}(n) - 1 - k b_{n-1} V_R] \\
+ \frac{A_0 + 1 - g_p}{g_i(1+k) - g_p + A_0 + 1} V_{\text{out}}(n-1) \\
+ \frac{1}{2} \gamma_1 [g_i (V_{\text{in}}^2(n-1) + k V_R^2) + V_{\text{out}}^2(n-1) - V_{\text{out}}(n)^2] \\
= V_{\text{steady(temp)}} + \frac{1}{2} \gamma_1 \text{[Harmonic parts]}
\]

where \( g_p = \frac{C_2}{C_1} \) and \( V_{os} \) is the DC offset voltage of opamp. In (2.19), \( V_{\text{out}}(n)^2 \) is replaced by \( V_{\text{steady(temp)}}^2 \) for simplifying the equation. Because \( \gamma_1 \) is very small, we assume the ideal capacitors in the integrators and use the second order approximation for opamp gain \( A = A_0(1 + \alpha V_{\text{out}}(n) + \beta V_{\text{out}}^2(n)) \). Usually, \( A_0 \) is large and \( \alpha \) and \( \beta \) are very small. In addition, the error caused by \( V_{\text{transient}}(t) \) is usually below 1%. Therefore, \( V_{\text{out}}(n) \approx V_{\text{steady(temp)}} \) and \( A \approx A_0(1 + \alpha V_{\text{steady(temp)}} + \beta V_{\text{steady(temp)}}^2) \). The output voltage caused by gain variation \( \Delta V_{\text{out}}(n) \) is approximated as:

\[
\Delta V_{\text{out}}(n) \approx \frac{A g_i}{g_i(1+k) - g_p + A + 1} V_i(n - 1) \\
+ \frac{A + 1 - g_p}{g_i(1+k) - g_p + A + 1} V_{\text{out}}(n - 1) - V_{\text{steady(temp)}}
\]

\( V_i(n - 1) \) in (2.20) is equal to \( V_{\text{in}}(n-1) - k b_{n-1} V_R + (1 + k) V_{os} \). The steady state solution in (2.17) is \( V_{\text{steady}} = (2.19) + (2.20) \). The integrator model is very easy to build in MATLAB. Fig. 2.13 shows the simulation results of switched capacitor integrator in MATLAB and PSPICE.
Figure 2.13: Simulation results of switched capacitor integrator

2.6 Comparator Model

In Delta-Sigma modulator, the requirements for comparators are high speed, not high resolution [10]. Therefore, simple comparators are usually used to increase the speed. Here, we only discuss two nonidealities of comparators: offset voltage and hysteresis. Figure 2.14 shows the nonideal effects caused by offset voltage and hysteresis in the comparator of Boser's 2nd-order structure. Even if the offset voltage increases from -0.1 V to 0.1 V, there is no significant degradation in SNDR. It is a very good merit. It means that sizes of the transistors in the comparators are not necessary to be large to reduce mismatch factor for random offset voltage [11]. Delta-Sigma modulators are comparatively more sensitive to hysteresis. Hysteresis causes
quantization noise floor arise in Figure 2.15. Therefore, some techniques are needed to reduce hysteresis.

Figure 2.14: Offset voltage and hysteresis in the comparator of 2nd-order DSM

Figure 2.16 shows the circuit diagram of latch comparator. In the figure, the function of M1 to M10 is track-and-latch stage. Two inverters are used to sharpen the output waveforms. The NOR gate latch keeps the value of the comparator when $\phi_1$ is low. If offset voltage is a critical issue, a pre-amplifier can be added before the latch. It also prevents kickback effect. In MASH structures, kickback effect may cause extra distortion for the following noise shaping. Therefore, latch comparator with low gain preamplifier [12] may be desired.

Another important phenomenon in comparators is hysteresis. For ideal comparators, they are memoryless. That is, the high-to-low trigger voltage $V_{H+}$ (or $V_{on}$) should be the same as the low-to-high trigger voltage $V_{H-}$ (or $V_{off}$). However, it is not true for real comparators. In Figure 2.16, if $\phi_1$ is kept high during the simulation
as shown in Figure 2.17, we can obtain hysteresis of this comparator in Figure 2.18. The voltage between $V_{on}$ and $V_{off}$ is up to several hundred mVs. If 1.024-MHz clock is applied to reset the comparator periodically, $V_{on}$ and $V_{off}$ will reduce to uV range.

2.7 Switch Model

Switch nonidealities are very important in SC integrators. The nonidealities discussed here are charge injection and clock feedthrough, harmonic distortion due to signal dependency and waveform delay in SC integrators.

2.7.1 Charge Injection and Clock Feedthrough from Switches

Charge injection is caused from the channel charge injecting to drains and sources of transistors when switches turn off. Figure 2.19 shows that channel charge goes to
both sides of the n-type transistor when the clock \( (V_G) \) falls. The error causes voltage drop in signal samples and deteriorates bit accuracy at the digital output.
In order to explicitly model the phenomena of charge injection, Figure 2.19 is implemented with circuit simulator. We can find that during the hold state, there is 30 mV error with 1-volt DC input signal like Figure 2.20 with $\frac{W}{L} = \frac{2\mu m}{1\mu m}$ NMOS switch and $C_L = 1pF$. When 100 KHz sinusoidal wave is applied as the input as shown in Figure 2.21 with the same dimension of the NMOS transistor, it is observed that charge-injection voltage is signal-dependent and is expressed as:
\[ V_{ch} = \frac{\gamma Q_{ch}}{C_L} = \frac{\gamma W L C_{ox} (V_G - V_S - V_{th})}{C_L} \]  

(2.21)

where \( \gamma \) is the percentage of channel charge, which goes to the capacitor \( C_L \).

Actually, \( \gamma \) is difficult to model in behavior simulation because it is concerned with capacitance of drain and source of the transistor and clock slopes. The simulation result of charge injection in circuit simulators may not be accurate. However, designers can adjust \( \gamma \) to leave the proper margin.

![Charge-injection voltage for the n-type switch with DC input](image)

Figure 2.20: Charge-injection voltage for the n-type switch with DC input

Basically, there are three methods to reduce charge injection in the switched-capacitor integrator: PN switch, half-sized dummy transistor [13] [12] and delay clock scheme [12] with fully differential opamp. Actually, these three methods can be used at the same time in the SC integrator.
Figure 2.21: Charge-injection voltage for the n-type switch with sine input

PN switch is the easiest method to reduce charge injection voltage. The concept is that PMOST and NMOST generate different types of channel charge. When switch is turned off, these charges will be reduced and $V_{ch}$ is:

$$V_{ch} = \frac{\gamma_n W_n L_n C_{ox} (V_{G1} - V_S - V_{thn}) - \gamma_p W_p L_p C_{ox} (V_S - V_{G2} + V_{thp})}{C_L} \tag{2.22}$$

Because of the difference in $\gamma_n$ and $\gamma_p$, mismatch in PMOST and NMOST and parameter variation during process, elimination of $V_{ch}$ is impossible with this method. But undoubtedly, $V_{ch}$ is reduced compared with only NMOST switch.

Figure 2.22 shows the circuit diagram of n-type switch with half-sized dummy. The source and drain of the dummy are connected together to compensate the channel charge from the previous n-transistor. If we do not consider any layout problems like parasitic capacitance, the simulation result is shown in Figure 2.23. In Figure 2.23, when input waveform arises, the tracking waveform cannot catch up the speed of

31
input waveform. This is because the resistance of n-transistor dramatically increases in this region. In order to overcome this problem, PN-type switch with dummy can be applied to reduce resistance from rail to rail. The simulation result indicates in Figure 2.24.

![Circuit diagram of n-type switch with half-sized dummy](image)

Figure 2.22: Circuit diagram of n-type switch with half-sized dummy

![Simulation result of n-type switch with half-sized dummy](image)

Figure 2.23: Simulation result of n-type switch with half-sized dummy
Delay clock with fully differential structure is indicated in [12]. Please see the reference for more information.

### 2.7.2 Harmonic Distortion in Switches

The distortion in a switch is caused from the on-resistance, which is dependent on signal amplitudes. If the switch is implemented by PN MOST, the on-resistance can be expressed as:

\[
R_{onn} = \frac{1}{\beta_n(V_{gs} - V_{thn} - \frac{V_{ds}}{2})} \quad (2.23)
\]

\[
R_{onp} = \frac{1}{\beta_p(V_{ds} - V_{gs} + V_{thp})} \quad (2.24)
\]

\[
R_{on} = \left(\frac{1}{R_{onn}} + \frac{1}{R_{onp}}\right)^{-1} \quad (2.25)
\]

For normal operation, \( R_{on} \) is very small compared with the impedance of \( C_s \). \( V_{ds} \) is close to zero and can be ignored. \( V_{s} \) is approximated to \( V_{in}(t) \). We can find that the resistance of \( R_{on} \) is a function of \( V_{in} \). It will introduce harmonic distortions in the
modulator. In order to demonstrate the distortion, Figure 2.25 shows the sampling capacitor and on-resistances of switches when \( \phi_1 \) is high. The voltage across sampling capacitor \( (C_S) \) is indicated as follows:

\[
V_c(t) = \frac{V_{in}(t)}{j\omega C_S Z_t} \approx \frac{V_{in}(t)}{2j\omega R_{on} C_S + 1}
\]  

(2.26)

where \( Z_t = R_{sw1} + R_{sw2} + \frac{1}{j\omega C_s} \). In order to simplify the equation in (2.26), we make assumption that \( R_{on2} = R_{on1} = R_{on} \).

![Figure 2.25: switch resistance when \( \phi_1 \) is high](image)

2.7.3 Waveform Delay Caused by On-Resistance of Switches

For high-speed Delta-Sigma modulator, the \( R_{on} \) could cause settling problems in SC integrators. For example, in \( \phi_1 \) phase, designers must ensure the delay from \( 2R_{on}C_S \) will not affect settling. It can be modeled as:

\[
V_{out}(t) = V_{in}(1 - e^{-\frac{1}{2R_{on}C_S}t})
\]  

(2.27)

If \( \tau_{rc} = 2R_{on}C_S \) and -100 dB in the settling error is required to ensure performance. Then, at least 11.5 \( \tau_{rc} \) is needed in \( \phi_1 \) phase.
Figure 2.26: Switch distortion test for sine input with $f_{in}=160\text{kHz}$, $f_s=20.48\text{MHz}$, $C_S=1\text{pF}$ and $A_{in}=0.4\text{V}$

In integrating phase, the on-resistance may cause the waveform delay at the output of SC integrator. Figure 2.27 shows the delay waveform according to different on-resistances in switches. Reducing $C_S$ will increase switch noise. It is not wise because low noise design is also important in Delta-Sigma modulators. Therefore, for high-speed application, large-sized switches are necessary for low resistance.

## 2.8 Fabrication Nonidealities

Fabrication nonidealities are critical issues, which make the functions of circuits different from simulation results. In order to avoid these nonidealities to cause any failure in the circuit functions, we need to make the designs more robust to them. In this section, nonidealities considered here are parameter shifting and mismatches.
2.8.1 Parameter Shifting

Because of fabrication nonidealities, circuit parameters will change from their nominal values. Therefore, reserving design margins to pass some process corners is necessary. Designers can make parameters changed based on circuit simulators. For example, open-loop gain (69.7 dB in Typical Corner) may vary from 75 dB in Slow Corner to 65 dB in Fast Corner. If these corners are $3\sigma$ corners, they ensure about 99.7% yield rate with variation within this range.

2.8.2 Mismatches

Mismatch in switch causes charge injection in differential-mode voltage in the fully differential integrator structure. Usually, the mismatch problem is not serious because sampling capacitors are sufficiently large to reduce the effect. In addition, bottom-plate sampling and delay clock scheme can be used to make charge injection
signal-independent. Therefore, mismatch problem in switches introduces the effect like offset voltage in the differential structure and Delta-Sigma modulators have very good immunity on it.

Capacitor mismatches causes gain error of the integrators. The effects are shown in Figure 2.28. The curves in Figure 2.28 is accumulated quantization noise in power spectral density. Basically, the floor of quantization noise changes due to different mismatch factors. In-band SNR could be better or worse. The sensitivity to gain error depends on the structures of Delta-Sigma modulators. Usually, signal stage structures have better tolerance on gain errors than MASH has. If the structure is sensitive to gain error, capacitor size must be large enough to reduce the mismatch problem.

Figure 2.28: Noise floor change due to capacitor mismatch
CHAPTER 3

NOISE ANALYSIS

Noises and uncertainties are unavoidable interference in electronic devices. Therefore, noise analysis is very important for system or circuit designers. In this chapter, switch noise, opamp noise and jitter noise will be introduced in order to model their behaviors reasonably. Actually, noises are also the fundamental limitation in Delta-Sigma A/D converter for bit resolution [14].

3.1 Spectrum of Delta-Sigma Modulators

Figure 3.1 shows the noise floor of Delta-Sigma modulator. Flicker noise dominates the low frequency in Region I. If signal frequencies are not located in this region, very simple high-pass filters at the decimation stage can remove the noise. If signals in this region are also important, chopper stabilizer and correlation double sampling technologies can be applied to remove low frequency noise [15].

Region II is where the main signal is located. Frankly speaking, jitter noise is also one kind of thermal noise. But it comes from external clock waveform generator like VCO. Here, thermal noises is limited to the noises generated from internal Delta-Sigma Modulator like switches and opamps. The noise power sets SNR or SNDR the upper boundary for bit resolution. In addition, bandwidth and bit resolution are two
trade-off factors in Delta-Sigma modulators. If designers want to increase bandwidth without losing too much resolution, it is suggested to choose bandwidth around the corner in Region II and Region III, like the thick-dotted line in Figure 3.1.

![Figure 3.1: the power spectral density of noise floor in Delta-Sigma modulator](image)

### 3.2 Switch Noise

Switch noise is very important noise in switched capacitor circuits. In some low noise opamp design, switch noise is dominant noise. In order to introduce the noise behavior, Figure 2.25 in Chapter 2 is redrawn here. The power spectral density of switch noise in Figure 3.2 is [12]:

\[ S_{th} = 4KTR_{on} \]  

(3.1)

In (3.1), \( K \) is Boltzmann's constant. \( T \) is absolute temperature. Assume \( R_{on1} = R_{on2} = R_{on} \). After filtered by on-resistance and sampling capacitor, the noise power will change to:

39
Figure 3.2: Model for sampling phase in switched capacitor circuit

\[ P_{sw} = \int_{-\infty}^{\infty} S_{th} \frac{1}{\sqrt{1 + (\frac{f}{f_0})^2}} |2df = \frac{KT}{C_S} \tag{3.2} \]

where \( f_0 = \frac{1}{4\pi f_{on} C_S} \). Assuming the power is uniformly distributed within \(-\frac{f_s}{2}\) and \(\frac{f_s}{2}\), we can derive noise power in signal bandwidth as:

\[ P_{sw(inband)} = \frac{KT}{C_S f_s} \times 2f_{in} = \frac{KT}{C_S M} \tag{3.3} \]

\( M \) is oversampling rate and \( f_{in} \) is signal bandwidth. From (3.3), we can find that large \( C_S \) and high \( M \) can reduce switch noise. For high-speed application, oversampling rate has its limitation. Although increasing sampling capacitance will reduce settling speed in integrators, we can still increase current (power) and reduce resistance to compensate the loss of speed.
Another interesting thing in (3.3) is that $P_{sw(\text{inband})}$ is independent of on-resistances of the switches. It seems to give designers more freedom to choose the value of on-resistance. However, on-resistance is concerned with settling error and signal-dependent harmonics. More details have been discussed in Chapter 2.

Feedback capacitor $C_F$ is sometime necessary in Delta-Sigma modulators. If we take $C_F$ into consideration, we obtain another noise source with power $\frac{KT}{C_F}$. For reducing simulation complexity, this noise is combined with (3.2) by assuming two noise sources are uncorrelated:

\begin{equation}
V_{sw}^2 = \frac{KT}{C_S} + \frac{KT}{C_F} \frac{C_F^2}{C_S^2} = \frac{KT}{C_S}(1 + k)
\end{equation}

$k$ is equal to $\frac{C_F}{C_S}$. One thing, which is very important and easy to overlook, is that for speed consideration, we should not include feedback capacitors in the modulators, especially in the first stage integrator. For noise consideration, feedback capacitor shows its disadvantage from (3.4), especially in the first stage integrator. Few designers address these problems but many designs still avoid them as in [7] [16] [17] [18]. Therefore, if new coefficients are necessary to use design high-speed Delta-Sigma modulator, it is wise to choose feedback coefficients the same as sampling coefficients to share the sampling capacitors in the first stage.

3.3 Opamp Noise

Figure 3.3 shows the opamp noise in switched capacitor integrator. Because there are two phase clocks with different input and load conditions, opamp noise is modeled as [19]:

41
\[ V_{n1}^2 = \frac{4}{3} \frac{KT}{C_{eq1}} (1 + n_t) \]  
\[ V_{n2}^2 = \frac{4}{3} \frac{KT}{C_{eq2}} (1 + n_t) \]  

where \( V_{n1}^2 \) and \( V_{n2}^2 \) are noise powers at \( \phi_1 \) and \( \phi_2 \) respectively. \( C_{eq1} = C_{in} + C_{L1}(1 + \frac{C_{in}}{C_I}) \). \( C_{eq2} = C_{S} + C_{in} + C_{L2}(1 + \frac{C_{S} + C_{in}}{C_I}) \). \( n_t \) is noise equivalent factor. The output noise is expressed as:

\[ V_{out}(z) = z^{-1} V_{n1}(z) \left( \frac{C_{in} + C_I}{C_I} \right) + \frac{z^{-1/2}}{1 - z^{-1}} V_{n2}(z) \frac{C_S}{C_I} \]  

Figure 3.3: Opamp noise in switched capacitor integrator

The main function of the integrator in Figure 3.3 is \( \frac{C_S z^{-1}}{1 - z^{-1}} \). In order to simplify the model, we can try to find the equivalent noise as:
\[ V_{in,n}(z) = (1 - z^{-1})V_{n1}(z)\left(\frac{C_{in} + C_I}{C_S}\right) + z^{1/2}V_{n2}(z) \]  

(3.8)

In (3.8), \( V_{n1} \) is filtered by a high pass filter. Assume signal bandwidth is much less than sampling frequency. Therefore, the second term is the dominant noise in signal bandwidth. The input equivalent noise power is:

\[ V_{in}^2 = \frac{4}{3} \frac{K T}{C_{eq2}} (1 + n_t) \]  

(3.9)

If we consider feedback capacitors, (3.9) is modified to:

\[ V_{in}^2 = \frac{4}{3} \frac{K T}{C_{eq2}} (1 + k)^2 (1 + n_t) \]  

(3.10)

\[ C_{eq2}' = C_S (1 + k) + C_{in} + C_{L2}(1 + \frac{C_S(1+k)+C_{in}}{C_I}) \] and \( k = \frac{C_F}{C_S} \).

Now, by combining (3.4) and (3.10), the total thermal noise power referred to input node is:

\[ V_{thermal}^2 = V_{sw}^2 + V_{in,n}^2 \]  

(3.11)

For fully differential structure, the input referred thermal noise voltage is \( \sqrt{2V_{thermal}^2 n(t)} \). \( n(t) \) is a random variable with zero mean and unity standard deviation.

3.4 Jitter Noise

Figure 3.4 shows the circuit diagram for 2 phase clocks with two delay clocks for SC integrators. The sampling noise caused by temperature introduces clock jitters. Clock jitters are important, especially for high-speed applications, because they exist
at the beginning of the signal path and directly deteriorate the in-band SNR of Delta-Sigma modulators.

![Circuit diagram for 4 phase clocks](image)

Figure 3.4: Circuit diagram for 4 phase clocks

Clock jitters result in non-uniform sampling. Supposing that the input signal is sinusoidal, we can model the effect of clock jitter in the following equation [7]:

\[
x(t + \delta) - x(t) \approx \delta \frac{d}{dt} x(t) = 2\pi f_{in} \delta A_{in} \cos(2\pi f_{in} t)
\]  

(3.12)

where \( A_{in} \) is the amplitude of the input signal and \( f_{in} \) is the signal frequency. \( \delta \) is the sampling error and assumed Gaussian random processing with standard deviation \( \Delta \tau \). Figure 3.5 indicates the effect of clock jitters.

Figure 3.6 indicates the power spectral density with or without clock jitters. In order to make the effect from clock jitters easier to observe, \( \Delta \tau \) is assumed a very large value, \( 1 \times 10^{-6} \) \( \text{s} \). For 1-KHz input sine and 256-KHz sampling frequency, the SNR values are measured 83.62 dB (without clock jitters) and 64.76 dB (with clock jitters). Clock jitters raise the low-frequency noise floor, which may affect the design for high resolution DSM.
Figure 3.5: Clock jitters for the sinusoidal wave as the input signal

Figure 3.6: Comparison in power spectral density w/o clock jitters for the sinusoidal wave as the input signal
Jitter noise is an important limitation for high-speed high resolution A/D converter. Even worse, from (3.12), it increases when signal frequency arises. The power of the signal $P_{in}$ is $\frac{A^2_{in}}{2}$ and the jitter noise power ($P_{jn}$) is indicated in (3.13). The SNR is shown in Figure 3.7 with the equation in (3.14) and different $\Delta \tau$. In Figure 3.7, if 14-bit Delta-Sigma A/D Converter with 1 MHz bandwidth is desired, $\Delta \tau$ must be less than 0.1 ns.

$$P_{jn} = \frac{1}{T_{in}} \int_0^{T_{in}} (2\pi f_{in} A_{in} \delta cos(2\pi f_{in} t))^2 \, dt$$
$$\approx 2(\pi f_{in} A_{in} \Delta \tau)^2$$

(3.13)

$$SNR_{jn} = 10\log\left(\frac{P_{in}}{P_{jn}}\right) = 10\log\left(\frac{1}{(2\pi f_{in} A_{in} \Delta \tau)^2}\right)$$

(3.14)

Figure 3.7: SNR relation between jitter noise and bandwidth with sinusoidal input and different $\Delta \tau$
3.5 Summary of Nonideal Effects in Delta-Sigma Modulators

Table 3.1 shows the summary of nonideal effects in Delta-Sigma modulators from Chapter 2 and Chapter 3. Personally, I feel it very useful because some nonidealities can be focused on for improvement when undesired results are obtained.

<table>
<thead>
<tr>
<th>Nonideality</th>
<th>Effect</th>
</tr>
</thead>
<tbody>
<tr>
<td>Finite DC gain</td>
<td>Inband noise floor increases</td>
</tr>
<tr>
<td>Gain nonlinearity</td>
<td>Harmonic distortion</td>
</tr>
<tr>
<td>Slew rate</td>
<td>Harmonic distortion</td>
</tr>
<tr>
<td>Finite gain bandwidth</td>
<td>Inband noise floor increases</td>
</tr>
<tr>
<td>Thermal noise</td>
<td>Noise floor increases</td>
</tr>
<tr>
<td>Comparator</td>
<td></td>
</tr>
<tr>
<td>Hysteresis</td>
<td>Quantization noise increases</td>
</tr>
<tr>
<td>DC offset</td>
<td>No obvious effect</td>
</tr>
<tr>
<td>Switch</td>
<td></td>
</tr>
<tr>
<td>Nonzero on-resistance</td>
<td>Quantization noise increases</td>
</tr>
<tr>
<td>Signal dependence in resistance</td>
<td>Harmonic distortion</td>
</tr>
<tr>
<td>Thermal noise</td>
<td>Noise floor increases</td>
</tr>
<tr>
<td>Capacitor</td>
<td></td>
</tr>
<tr>
<td>Nonlinearity</td>
<td>Harmonic distortion</td>
</tr>
<tr>
<td>Mismatch</td>
<td>Noise floor changes</td>
</tr>
<tr>
<td>Clock</td>
<td></td>
</tr>
<tr>
<td>Jitter</td>
<td>Noise floor increases</td>
</tr>
</tbody>
</table>

Table 3.1: Summary of nonideal effects in Delta-Sigma modulators
CHAPTER 4

DESIGN EXAMPLE FOR 14-BIT 16 KS/S DELTA-SIGMA A/D CONVERTER

This chapter demonstrates the design of single-stage 2nd-order Delta-Sigma modulator to achieve 14-bit 16-kS/s performance. Simulation results from PSPICE are used to verify only circuit connection and performance without noise effects. Top-down design and bottom-up verification make design more immune to circuit nonidealities.

4.1 Architecture Selection

In order to achieve 14-bit resolution with 16 KS/s digital output rate (DOR), 2nd-order Delta-Sigma modulator is sufficient with oversampling rate around 128 [7]. The sampling rate will be 2.048 MHz. For sub-micron CMOS technology, analog circuits (especially opamps) can achieve the desired performance. I proposed to use switched capacitor integrators because performance is more ensured compared with other technologies like switched current and continuous-time circuits. Folded cascode opamps are applied according to better linearity in gain variation to suppress harmonic distortions. Fully differential is used to reduce common-mode nonidealities and low frequency noises. Single stage structure is preferred because there is no stability problem in the second-order structure. In addition, single stage has more immunity
in circuit nonidealities than a MASH structure. The structure is used because there is no feedback capacitor and the die size can be reduced. Another advantage is that once the first-stage integrator is designed, the second integrator can be the same if power consumption is not critical.

4.2 Behavioral Modeling Designing

When the architecture is selected, behavioral model can be designed. Chapter 2 and Chapter 3 have detail information to build designers' own behavioral models.

4.3 Parameter Initialization

Parameter initialization needs the information of fabrication technology and the background of circuit design in order to obtain reasonable values for the parameters. The equations in [7] [10] [12] can help designers to find possible parameter values although some assumption may not always be true. For example, in [7], the power of quantization noise is calculated under the assumption that quantization noise is uniformly distributed within \(-\Delta\) and \(\Delta\). The power spectral density of settling error may not be uniformly distributed within the range of \([\varepsilon_{\text{max}}, \varepsilon_{\text{max}}]\). In Figure 4.2, we can find this assumption is not true for quantization noise. But designers still can use these equations to reduce the range of possible parameters.

4.4 Behavioral Simulation

Behavioral simulations are executed to find possible circuit parameters because they are much faster than circuit simulators. Based on designers' necessities, different parameters are found during the simulations. For example, some designers may focus on the parameters of less power consumption. Some designers may choose smaller
Figure 4.1: Quantization noise test of 2nd-order Delta-Sigma modulator with Boser's structure

Figure 4.2: Noise amplitude and spectrum of 2nd-order Delta-Sigma modulator with Boser's structure

noise factors in order to achieve high-speed high-resolution design. Table 4.1 shows a possible result of circuit parameters.
<table>
<thead>
<tr>
<th></th>
<th>Integrator1</th>
<th>Integrator2</th>
<th>Comparator</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_s$</td>
<td>1 pF</td>
<td></td>
<td>$V_{o}(\text{comp})$</td>
</tr>
<tr>
<td>$C_t$</td>
<td>2 pF</td>
<td></td>
<td>$V_{\text{hi}}$</td>
</tr>
<tr>
<td>$C_c$</td>
<td>1 pF</td>
<td></td>
<td>$V_{\text{lo}}$</td>
</tr>
<tr>
<td>$C_{\text{in}}$</td>
<td>150 fF</td>
<td></td>
<td>$\gamma_{\text{cl}}$</td>
</tr>
<tr>
<td>$g_m$</td>
<td>150 uA/V</td>
<td></td>
<td>$\alpha$</td>
</tr>
<tr>
<td>$I_{o+}$</td>
<td>25 uA</td>
<td></td>
<td>$\beta$</td>
</tr>
<tr>
<td>$I_{o-}$</td>
<td>-25 uA</td>
<td></td>
<td>$\delta_t$</td>
</tr>
<tr>
<td>$n$</td>
<td>15</td>
<td></td>
<td>$\gamma_{\text{cl}}$</td>
</tr>
<tr>
<td>$V_{\text{os}}$</td>
<td>10 mV</td>
<td></td>
<td>$V_{\text{ref}+}$</td>
</tr>
<tr>
<td>$A_0$</td>
<td>70 dB</td>
<td></td>
<td>$V_{\text{ref}-}$</td>
</tr>
<tr>
<td>$R_{\text{sw(max)}}$</td>
<td>3.5 kohm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\gamma_{\text{m}}$</td>
<td>50 ppm</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 4.1: Simulation specifications in analog behavioral model in MATLAB

4.5 Circuit Component Implementation

After simulation results meet the required performance, circuits can be implemented according to the parameters. The following subsections indicate the details of designs about opamps, switches and comparator.

4.5.1 Opamp Design

Opamp design is the most important task in designing Delta-Sigma modulators. In order to ensure performance and reduce interference, fully differential opamps are usually used in the design. The first parameter addressed is the transconductance of...
the fully differential opamp as shown in Figure 4.3. In Figure 4.3, The charge and discharge are 30 nA with the slope (gm) 323 nA/V.

Figure 4.3: Transconductance of fully differential opamp

Figure 4.4 shows the frequency response of the opamp. The DC gain is about 70 dB. Unity gain frequency \( f_{\text{ubdB}} \) is 19.3 MHz. Phase margin (PM) is 71°.

In real opamps, voltage gain is varied with output voltage. Figure 4.5 shows the relation of open loop gain to output voltage for fully differential opamp. In order to reduce nonlinearity, the range of output voltage is limited within \(-0.7 \text{ V to } 0.7 \text{ V}\) \((-1.5 \text{ V to } 1.5 \text{ V for differential mode})\), where minimum 70-dB gain is guaranteed. If we use \( A = A_0(1 + \alpha V_{\text{out}} + \beta V_{\text{out}}^2) \) for approximation, \( \alpha \) is around \(-5.4 \times 10^{-4}\) and \( \beta \) is around \(-0.6\).
4.5.2 Switch Design

PSPICE is used to simulate switch resistance and noise with $C_S = 1 \text{ pF}$ and n-type switch. Figure 4.6 shows the simulation results of switch on-resistance and the root spectral density of switch noise. It is observed that the resistance of the n-type switch is not constant and increases dramatically when input voltage is close to positive supply voltage 1.65 V. It means that time constants will change dramatically according to different amplitudes of input signal. Another problem is that because resistance is dependent on input signal, the switch noise is also signal-dependent on account of the equation $S_n = 4kTR_{on}$. The root spectral density is derived when input voltage is 0 V.
Figure 4.5: Relation between output voltage and open-loop gain of fully differential opamp

Figure 4.6: On resistance and noise of n-type switch
In order to overcome the problems above, PN MOST's are used in parallel position. Figure 4.7 indicates that the resistance and noise of pn switch. The advantages are discussed in Chapter 2 and shown as follows:

1. The resistance of pn switch is smaller than that of n-type switch or p-type switch.

2. The variation of resistance with input signal in pn switch is much less than that in n-type switch or p-type switch.

3. The input range of pn switch can achieve positive supply voltage and negative supply voltage.

By hand calculation, $f_{-3dB} = \frac{1}{2\pi R_{on}C_S} = \frac{1}{28\pi \times 3kOhm \times \frac{1}{1pF}} = 53.05 MHz$ at $V_{in} = 0$ V. $S_n = 4KTR_{on} = 4 \times 1.38e^{-23} \times 300^oK \times 3kOhm = 4.968e^{-17}V^2/Hz$ or $-163dB$. Compared with PSPICE results $f_{-3dB} = 51.9 MHz$ and $S_n = -165 dB$ in Figure 4.7, the results are close to each other.

4.5.3 Comparator Design

In Delta-Sigma Modulator, the specifications are relaxed because what we need is a high-speed comparator instead of high-resolution comparator. A simple latch comparator is used here only for one-bit quantizer. Figure 4.8 shows the circuit diagram of latch comparator. In the figure, the function of M1 to M10 is track-and-latch stage. Two inverters are used to sharpen the output waveforms. The NOR gate latch keeps the value of the comparator when $\phi_1$ is low. Because offset voltage is not a critical issue, a pre-amplifier stage can be avoided. Periodical reset is applied to reduce hysteresis of the comparator.
Figure 4.7: On resistance and noise of pn switch

Figure 4.8: Circuit diagram of latch comparator
4.6 Verification

In order to verify the result of analog behavioral model, PSPICE is used to obtain 4096-point FFT with Hanning window from the Delta-Sigma modulator. Meanwhile, after updating the circuit parameters from PSPICE in to an analog behavioral model, the same point FFT is derived to compare the both results. From Figure 4.9 and Figure 4.10, they have almost the same noise floor and the exactly the same signal strength.

![Power spectral density from analog behavioral model in MATLAB](image)

Figure 4.9: Power spectral density from analog behavioral model in MATLAB

4.7 Expected Performance with fabrication variation

After verification of the behavioral model, designers can use behavioral simulation to predict the system performance for the DSM and the potential problems. The simulation parameters of behavioral model are listed in Table 4.2 after changing the hysteresis. The offset voltages in the opamp and comparator are set to reasonable
values by considering fabrication nonidealities in Monte Carlo simulations. The power spectral density is shown in Figure 4.11. Figure 4.11 indicates that the lowest noise floor is dominated by thermal noise and jitter noise. Offset voltage causes DC component in the spectrum. Intermodulation phenomenon is demonstrated in Figure 4.12. The inband (<8kHz) harmonics are less than 87 dB under the circumstances shown in Figure 4.12.

Decimation filter used in this paper is only 3-stage comb filter with 128 downsampling shown in Figure 4.13 [20]. If the gain attenuation of the passband is concerned, multi-rate scheme and compensation filter can be applied for better performance [21]. After $SINC^3$ comb filters and 128 downsampling, the digital output rate (DOR) is 16 Ksamples/s. The information about SNR, SNDR, SFDR and total harmonic distortion are obtained in Figure 4.14 and Figure 4.15 by combining analog behavioral model and digital behavioral model for performance verification. Dynamic
Table 4.2: Simulation specifications in analog behavioral model in MATLAB

<table>
<thead>
<tr>
<th>Integrator1</th>
<th>Integrator2</th>
<th>Comparator</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>1 pF</td>
<td>V_{comp}</td>
</tr>
<tr>
<td>C2</td>
<td>2 pF</td>
<td>V_{in}</td>
</tr>
<tr>
<td>C3</td>
<td>1 pF</td>
<td>V_{out}</td>
</tr>
<tr>
<td>Cm</td>
<td>100 pF</td>
<td>V_{out}</td>
</tr>
<tr>
<td>gm</td>
<td>320 uA/V</td>
<td>Jitter Noise</td>
</tr>
<tr>
<td>f1</td>
<td>30.1 uA</td>
<td>gamma</td>
</tr>
<tr>
<td>f2</td>
<td>-29.8 uA</td>
<td>Beta</td>
</tr>
<tr>
<td>m</td>
<td>11.5</td>
<td>1.82e-2</td>
</tr>
<tr>
<td>V_{in}</td>
<td>5 mV</td>
<td>alpha</td>
</tr>
<tr>
<td>A_{in}</td>
<td>75.96 dB</td>
<td>beta</td>
</tr>
<tr>
<td>R_{in}</td>
<td>3.5 kOhm</td>
<td>gamma_{ci}</td>
</tr>
<tr>
<td>gamma_{ci}</td>
<td>50 ppm</td>
<td>alpha</td>
</tr>
<tr>
<td>alpha</td>
<td>1.82e-2</td>
<td>beta</td>
</tr>
<tr>
<td>beta</td>
<td>-0.2176</td>
<td></td>
</tr>
</tbody>
</table>

Figure 4.11: Power spectral density of the output of 2nd-order modulator from behavioral simulation with noise consideration
range (DR) is equal to 87.1 dB (14.2 bits). Here, Total Harmonic Distortion (THD) is defined as follows:

\[
\text{THD} = 20\log_{10}\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2 + V_7^2}}{V_1}
\]  

(4.1)

Mismatch in capacitors causes gain errors for the integrators. From the simulation, the A/D converter can tolerate 5% capacitor variation without dropping below 14-bit resolution. The performance of the 2nd-order Delta-Sigma A/D converter are summarized in Table 4.3.
Figure 4.13: Block diagram of 3-stage comb filter with 128 downsampling

Figure 4.14: SNR, SNDR, SFDR of 2nd-order Delta-Sigma A/D Converter
Figure 4.15: Harmonic distortions of 2nd-order Delta-Sigma A/D Converter

<table>
<thead>
<tr>
<th>Performance</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_s$</td>
</tr>
<tr>
<td>$f_{in}$</td>
</tr>
<tr>
<td>DOR</td>
</tr>
<tr>
<td>DR</td>
</tr>
<tr>
<td>SNR (Peak)</td>
</tr>
<tr>
<td>SNDR (Peak)</td>
</tr>
<tr>
<td>SFDR (Peak)</td>
</tr>
<tr>
<td>2nd HD (Min)</td>
</tr>
<tr>
<td>3rd HD (Min)</td>
</tr>
<tr>
<td>THD (Min)</td>
</tr>
<tr>
<td>Intermodulation</td>
</tr>
<tr>
<td>Mismatch in C</td>
</tr>
</tbody>
</table>

Table 4.3: Summary of performance in the 2nd-order Delta-Sigma A/D converter
CHAPTER 5

DESIGN EXAMPLE FOR 14-BIT 2-MSAMPLES/S HIGH-SPEED DELTA-SIGMA A/D CONVERTER

This chapter demonstrates the details of design procedure for high-speed Delta-Sigma A/D converter. In Chapter 4, single-stage 2nd-order Delta-Sigma A/D converter is used as an example. In this chapter, multi-stage 4th-order MASH211 structure will be applied to achieve high-speed high-resolution ADC.

5.1 Circuit Parameter Initialization

The MASH211 structure is indicated in Figure 5.1 [16]. According to the design flow in Chapter 1, we need to design behavioral model for this structure. In Figure 5.1, we can find that the circuit components will be SC integrators, switches and comparators. The detail models are in Chapter 2. Therefore, we can start at the stage of initializing circuit parameters.

Table 5.1 shows the parameters, which are necessary to initialize in the behavioral models. Before executing behavioral simulations, we need to know the reasonable values first.
5.1.1 Integrator Parameters

Equation method is used to find the possible range. In order to consider the relationship of in-band SNR with finite open-loop gain of opamp ($A_0$) and oversampling rate ($M$), quantization noise power at the modulator output is [16]:

$$P_Q = \frac{\Delta^2}{2} \left[ \frac{4\pi^2 \mu_1^2}{3M^3} + \frac{4\pi^4 \mu_3^2}{5M^5} + \frac{4\pi^6 (1 + 2\mu_4)}{9M^9} \right]$$ (5.1)
<table>
<thead>
<tr>
<th>Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sampling frequency</td>
</tr>
<tr>
<td>Signal frequency</td>
</tr>
<tr>
<td>Integrator</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>Comparator</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>Switch</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>Capacitor</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>Clock</td>
</tr>
</tbody>
</table>

Table 5.1: Parameters for initialization

$\Delta$ is feedback voltage of Delta-Sigma modulators. $\mu_1 = \frac{0.25}{A_{o1}}, \mu_2 = \frac{1}{A_{o3}}$ and $\mu_4 = \frac{1}{A_{o4}}$.

From Equation (5.1), we can find that the power of quantization noise is reduced by increasing oversampling rate. In addition, lower open-loop gain is acceptable.
for higher stage modulator. Assuming input sine wave is $A_{in} \sin(2\pi f_{in}t)$, the signal power is $\frac{A_{in}^2}{2}$. By using SIMULINK model shown in Figure 5.1, we can find that the maximal SNR will occur when $A_{in}$ is 0.8A (overload point). In-band SNR can be expressed as:

$$SNR_{max} = 5.84 - 10 \times \log_{10} \left[ \frac{4\pi^2 \mu_1^2}{3M^3} + \frac{4\pi^4 \mu_2^2}{5M^5} + \frac{4\pi^8 (1 + 2\mu_3)}{9M^9} \right]$$  \hspace{1cm} (5.2)

First, we assume that the same opamp is used for all 4 integrators. Therefore, $A_{o1} = A_{o2} = A_{o3} = A_{o4} = A_0$. Figure 5.2 can give designers potential ranges to choose $A_0$ and $M$. If we need a maximum signal bandwidth 1MHz with 14-bit resolution and $M = 20$, $A_0$ is only around 50 dB. Sampling frequency is about $20 \times 2f_{in} = 40MHz$.

Assume maximum open-loop gain $A_{max}$ is 70 dB and minimum gain is 60 dB in order to have 10 dB margin. By using second-order polynomial to approximate the gain variation $A_0 = A_{max} (1 + \alpha V_{out} + \beta V_{out}^2)$, we can obtain $\alpha = 0$ and $\beta = -0.6838$.

The relation of $A_0$ and $V_{out}$ is shown in Figure 5.3. For fully differential structure, because input range and output range are doubled, $\beta$ is changed to -0.171.

If 14-bit resolution and 1MHz signal bandwidth are required, we need to pay attention to switch noise $(\frac{KT}{C_s})$. The in-band noise power due to switch noise is about $\frac{KT}{MC_s}$. The noise power is doubled because the fully differential opamps are going to use. But SNR is still improved by 3 dB due to input signal voltage doubled. The in-band SNR according to switch noise will be:

$$SNR_{sw} = 10 \log_{10} \left( \frac{0.64 \Delta^2}{KT \cdot MC_s} \right)$$  \hspace{1cm} (5.3)

66
Figure 5.2: Relationship of SNR with open-loop gain and oversampling rate

For example, $\Delta = 1V$ and $T = 300^\circ K$. In order to leave design margin, 15 bit resolution needs 0.51 pF for $C_S$. 16 bit resolution needs up to 2pF. Because large sampling capacitors will slow down integrator speed, $C_S$ is carefully chosen. Here, $C_S$ is decided to 1 pF. Therefore, $C_I$ is 4pF. For convenience, $C_L$ is assume 1 pF. Then $C_{eq} = 2.25pF$, and we temporally ignore input parasitic capacitor $C_{in}$ of opamps.

Another thermal noise in integrators is from opamps. The power is derived in Chapter 3 for $V_{opm}^2 = \frac{4kT(1+n_e)}{C_{eq}}$. (5.4) shows SNR associated with opamp noise. For fully differential structure, input signal voltage and noise powers are doubled. If 15 bit margin is necessary, $n_t$ must be less than 2.3. Here we can choose $n_t = 1$. 
Now we can try to decide the ranges of transconductance \((g_m)\) and maximum output current \((I_o)\) of the opamp. Because \(f_s\) is 40 MHz and SC integrators are operated in two nonoverlapped clock waveforms, assuming 50% duty cycle for these two clocks, we can find that each time slot of capacitor charging or discharging is 12.5 ns. If bottom-plate sampling and delay clock scheme are used [12], only around 10 ns is allowed for settling. We can consider that the maximum input step is 1.8 V \((\Delta + A_{in(max)})\). In Chapter 2, the equations have already been derived and now re-written as follows:

\[
SNR_{opn} = 10 \log_{10} \left( \frac{0.64 \Delta^2}{\frac{4}{3} KT (1 + n_z) M C_{eq}} \right) \tag{5.4}
\]

\[
t_0 = \frac{C_s V_{in}}{SR} - \frac{C_{eq}}{g_m} \tag{5.5}
\]
Here, \( SR \) is the slew rate of the integrator with the value of \( \frac{I_o}{C_L} \) assuming that output current flows in and out of \( C_L \) (actually not). Using 5ns is for slewing region and linear region respectively, we can obtain \( t_0 \) is 5ns, \( \frac{T_x}{2} \) is 10ns and assume \( E_{settle} = 0.1\% \). After numerically solving (5.5) and (5.6), we can derive \( I_o = 161.4\mu A \) and \( g_{m} = 1.767mA/V \).

Offset voltage consists of systematic offset voltage and random offset voltage \[11\]. Usually, systematic offset voltage is very small. Random offset voltage caused by fabrication nonidealities dominates the offset voltage. Because it is not signal dependent, Delta-Sigma modulator is not sensitive to it. In addition, signal bandwidth usually excludes DC component. We can assume 10 mV in this stage and find more detail in statistical method.

5.1.2 Comparator Parameters

From simulation results in Chapter 2, Delta-Sigma modulators are not sensitive to DC offset in comparators. But they are comparatively more sensitive to hysteresis. We can use any reasonable value for hysteresis. For example, \( V_{H+} = 10mV \) and \( V_{H-} = -10mV \) for 20-mV hysteresis.

5.1.3 Switch Parameters

Switch parameters concerned here is on-resistance, charge injection and clock feedthrough. Because fully differential structure is used here, we can temporarily
ignore these effects caused by charge injection and clock feedthrough. Usually PN MOST switches are used to obtain better signal swing range. In high-speed applications, on-resistance of switches can cause harmonic distortion and settling errors as shown in Chapter 2. Before estimating the size of switches, we need to know process information first. For example, $V_{cc} = 2.5V$, $V_{ss} = -2.5V$, $A_{in} = 0.8V$, $K_p = 58.1uA/V^2$, $K_n = 19.2uA/V^2$, $V_{th0p} = -0.89V$, $V_{th0n} = 0.69V$, $\gamma_p = -0.58\sqrt{V}$, $\gamma_n = 0.48\sqrt{V}$ and $\phi_0 = 0.34V$.

![Switch distortion test for $f_s=1$ MHz, $f_i=40$ MHz, $C_s=1pF$, $A_i=0.8V$, and $W/L=32$](image)

**Figure 5.4:** Relationship of SNR with open-loop gain and oversampling rate

From Figure 5.4, because gate-to-source voltage and body effect of the PN switch cause on-resistance signal dependence, output voltage stored in the sampling capacitor...
is deteriorated with harmonic distortion. The harmonic distortion is suppressed to below -100 dBc by choosing large switch size $\frac{W}{L} = 32$. Maybe some one may ask, "Why don't we connect the source of the P MOST to its nwell to eliminate body effect?" In opamp design, this is reasonable because the nwell of P MOST can be inversely biased to avoid leakage. But in a switch, we cannot ensure the highest voltage will always be the source in P MOST. Therefore, the nwell in P MOST is connected with VCC to ensure its performance.

The other issue is about the incomplete settling caused by time constant $R_{\text{sw}}C_S$. Because it is the first-order settling error, we can express it as $e^{-\frac{T_S}{2R_{\text{sw}}C_S}}$. In switched capacitor integrators, $R_{\text{sw}} = 2R_{\text{on}}$ because two switches are connected in series. From Figure 5.4, we find that the maximum resistance is about 480 ohm. Then, we find that the settling error is about 0.003%, which is sufficient for Delta-Sigma modulators.

5.1.4 Capacitor Parameters

The values of capacitors for $C_S$, $C_I$ and $C_L$ have been decided in the subsection of integrator parameters because they are concerned about speed and noise power. Here, we can find the capacitor variation due to charge voltage. Because double-poly capacitors will be used for implementation, it is reasonable to assume that $\gamma_c \approx 50\text{ppm}$ for $C = C_0(1 + \gamma_c V_c)$. Mismatch factor is temporarily assumed zero and will be discussed later.

5.1.5 Jitter Noise

In order to decide the maximum tolerance for jitter noise, we can look at Figure 3.7 in Chapter 3. Because the maximum signal bandwidth is 1 MHz with 14-bit resolution, from Figure 3.7, the standard deviation of jitter noise $\Delta \tau$ must be no
more than 10 psec. It means that high quality clock waveform generator is required to meet the performance. But if the frequencies of input signals are not close to 1 MHz, larger standard deviation of jitter noise can be tolerated.

By concluding the discussion in previous sections, the initialized parameters are listed in Table 5.2.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sampling frequency fs</td>
<td>40 MHz</td>
</tr>
<tr>
<td>Bandwidth BW</td>
<td>1 MHz</td>
</tr>
<tr>
<td>Integrator Open-loop gain (A0)</td>
<td>70dB</td>
</tr>
<tr>
<td>Transconductance (g_m)</td>
<td>1.767 mA/V</td>
</tr>
<tr>
<td>Max. output current (Io)</td>
<td>161.4 uA</td>
</tr>
<tr>
<td>Gain variation (alpha, beta)</td>
<td>0, -0.171</td>
</tr>
<tr>
<td>Parasitic capacitor (Cin)</td>
<td>0</td>
</tr>
<tr>
<td>Thermal noise (n)</td>
<td>1</td>
</tr>
<tr>
<td>DC offset (V_{os(op)})</td>
<td>10 mV</td>
</tr>
<tr>
<td>Comparator L-to-H trigger voltage (V_{h-})</td>
<td>10 mV</td>
</tr>
<tr>
<td>H-to-L trigger voltage (V_{h+})</td>
<td>-10 mV</td>
</tr>
<tr>
<td>Switch On-resistance (Ron)</td>
<td>480 ohm</td>
</tr>
<tr>
<td>Settling error (E_{settle})</td>
<td>0.003%</td>
</tr>
<tr>
<td>Thermal noise</td>
<td>&lt;-15bits</td>
</tr>
<tr>
<td>Capacitor Nonlinearity (gamma_c)</td>
<td>50 ppm</td>
</tr>
<tr>
<td>Mismatch None</td>
<td></td>
</tr>
<tr>
<td>Clock Jitter (dtau)</td>
<td>10 ps</td>
</tr>
</tbody>
</table>

Table 5.2: Summary of initialized parameters
5.2 Behavioral Simulations

After parameters have been initialized, behavioral simulations are run for parameter modification. By using the parameters listed in Table 5.2, we can obtain the power spectral density of the Delta-Sigma modulator with $f_{in} = 156.25kHz$, $f_s = 40MHz$, $A_{in} = 0.25V$ and $\Delta = 1V$ shown in Figure 5.5 with 16384-point FFT and Hanning window. We use $A_{in} = 0.25V$ instead of $A_{in} = 0.8V$ because we need to ensure input signal will not overload the modulator, especially since the behavioral model has not yet specified the overload point. In Figure 5.5, the simulation reveals that main performance with 1 MHz-signal bandwidth is limited by quantization noise floor. Meanwhile, the second harmonic and the third harmonic are less than signal strength by 92 dB and 72 dB respectively.

After $SINC^5$ filters and downsampling, SNR, SNDR and SFDR are observed from Figure 5.6. Dynamic range (DR) is about 85.7 dB (13.94 bits). Maximum SNR is 82.25 dB. Maximum SNDR is 72.5 dB. Maximum SFDR is 86.5 dB. The overload point is about 0.75 V.

The circuit specifications seem to meet the requirements, which we set for the A/D converter at the beginning of this chapter. However, the behavioral simulation does not include process nonidealities to the result. In addition, the harmonic distortions in Figure 5.5 will deteriorate performance if bandwidth is reduced for high resolution. In order to reduce harmonic problems, we can recall Table 3.1 in Chapter 3 for the possible factors, which cause these harmonics. Because high open-loop gain can suppress gain variation that induces harmonics, we can increase $A_0$ to 80 dB and investigate the power spectral density again. Figure 5.7 shows the power spectral density of the Delta-Sigma modulator with $f_{in} = 156.25kHz$, $f_s = 40MHz$, $A_{in}$ =
0.25V, Δ = 1V and improved open-loop gain 80 dB. We can find that almost no improvements on these harmonic distortions. The second harmonic and the third harmonic are still less than signal strength by 93 dB and 72 dB respectively.

We can try to increase transconductance $g_m$ and output current $I_o$ for reducing settling errors. If we increase $g_m$ to 2.1 mA/V and $I_o$ to 370 μA, the power spectral density is shown in Figure 5.8. The second harmonic is less than signal by 99 dB. The third harmonic is reduced less than signal by 98 dB. Figure 5.9 shows the information about SNR, SNDR and SFDR. SNR = 86.6dB. SNDR = 82.9 dB. SFDR = 93.5 dB. DR is 86.7 dB (14.1 bits). The overload point is at 0.8 V.

Before we start to implement the circuits, we need to know the tolerance of process variations. For example, $g_m$ decreases by 30% at the same time but $A_o$ increases by
Figure 5.6: SNR and SNDR of the Delta-Sigma A/D converter with $f_{in} = 156.25\, kHz$, $f_s = 40\, MHz$, $\Delta = 1V$ and $M = 20$

3dB (slow corner), or $g_m$ increases by 30% at the same time but $A_0$ decreases by 3dB (fast corner). $I_o$ is assumed almost constant because the current bias is from the high quality bandgap current reference. Figure 5.10 and Figure 5.11 show the relation of SNR, SNDR and SFDR with process corners. Figure 5.10 shows SNR=86dB, SNDR=82.5dB, SFDR=92.7dB and DR=87.3dB. Figure 5.11 shows SNR=86dB, SNDR=83.2dB, SFDR=93dB and DR=84.5dB. Basically, this design is not very sensitive to process variation.

Capacitor mismatch causes gain error. Although MASH is more sensitive to capacitor mismatch, it is still more insensitive compared with other types of A/D converters. In order to make result comparison, we can exclude noise model first and change different capacitor values in any capacitors, which we are interested in. Here,
Figure 5.7: Power spectral density of the Delta-Sigma modulator with \( f_{in} = 156.25kHz, f_s = 40MHz, A_{in} = 0.25V, \Delta = 1V \) and improved open-loop gain sampling capacitors in each stage are used to investigate the tolerance of capacitor mismatch. Table 5.3 shows the tolerance for capacitor mismatch with maximum SNR 1dB drop. For double ploy capacitors, the matching factors are usually around 0.1\% range [22]. The matching requirements are not very restrictive even in the MASH structure [16].

If power consumption is critical, designers can reduce the power consumption in the second, third and fourth integrators respectively. However, different opamp designs will take more development time and more efforts in the testing chips. In order to achieve the balance point, the first integrator use the opamp with higher performance. The other integrators use the opamp with relaxed requirements. Table 5.4 lists the circuit parameters verified by behavioral simulations.
Figure 5.8: Power spectral density of the Delta-Sigma modulator with $f_{in} = 156.25\, kHz$, $f_s = 40\, MHz$, $A_{in} = 0.25\, V$, $\Delta = 1\, V$, $g_m = 2.1\, mA/V$ and $I_o = 370\, \mu A$

![Power spectral density graph]

Table 5.3: Tolerance for capacitor mismatch with maximum SNR 1dB drop

<table>
<thead>
<tr>
<th>Modulator</th>
<th>C mismatch</th>
</tr>
</thead>
<tbody>
<tr>
<td>1st Modulator</td>
<td>0.7 %</td>
</tr>
<tr>
<td>2nd Modulator</td>
<td>1.2 %</td>
</tr>
<tr>
<td>3rd Modulator</td>
<td>5 %</td>
</tr>
</tbody>
</table>

5.3 Circuit Component Implementation

Table 5.4 shows the circuit parameters after behavioral simulations. According to these parameters, we can find proper circuits to fulfill the Delta-Sigma modulator.
Figure 5.9: SNR and SNDR of the Delta-Sigma A/D converter with $f_m = 156.25kHz$, $f_s = 40MHz$, $\Delta = 1V$ and $M = 20$

Some items like parasitic capacitor $C_{in}$ and opamp noise will be specified through circuit simulators.

5.3.1 Opamp Implementation

The most important circuit in a switched capacitor integrator is opamp. Class A type opamp is used in order to suppress the nonlinearity of open loop gain. In addition, speed and signal swing ranges are also very important to the integrator. Telescopic structure may be the fastest type of opamps, but limited swing ranges in the feedback operation. Two-stage opamp is slower but has very wide output range [23]. In this design case, we are not going to use these two types of opamps. Folded cascode opamp is used in this case because it has moderate speed and swing range.

78
Figure 5.10: SNR and SNDR of the Delta-Sigma A/D converter with \( f_{in} = 156.25 kHz \), \( f_s = 40 MHz \), \( \Delta = 1V \) and \( M = 20 \) in slow corner

In order to increase the speed of the opamp, short-length transistors are used to reduce capacitance in signal path. High currents are necessary to increase slew rate. Therefore, output resistance (open-loop gain) is decreased. In order to overcome this problem, we have the following methods to increase the gain:

1. Increase the length of transistors: Because the relation of \( R_o \propto \frac{L}{I_D} \), we can increase \( L \) to compensate the loss of gain due to large \( I_D \). However, for maintaining the same aspect ratio, \( W \) should be also increased and it causes dramatically increasing in parasitic capacitance, which reduces the speed and phase margin.

2. Increase cascode stage: This decreases the output swing range and deteriorates SNR especially for low voltage applications.
Figure 5.11: SNR and SNDR of the Delta-Sigma A/D converter with \( f_{in} = 156.25kHZ \), \( f_s = 40MHz \), \( \Delta = 1V \) and \( M = 20 \) in fast corner

3. Use two-stage structures: Two-stage structures increase output swing range and gain, but reduce speed of the opamps. They also need more power consumption and maybe compensation capacitors, which also reduce the speed.

4. Use gain-boosting structures: Gain-boosting structures cost more power consumption and circuit complexity. It might cause settling problems [24] if the auxiliary amplifiers are not well designed.

Here, I choose gain-boosting structures to increase the open loop gain and carefully design the boosting stages. Figure 5.12 shows the circuit diagram of fully differential folded cascode opamp with gain boosting. According to [25], the unity gain frequency of boosting stages should be larger than the \(-3dB\) frequency.
### Table 5.4: Summary of circuit parameters verified by behavioral simulations

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Behavioral Model</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sampling frequency</td>
<td>( fs )</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>( BW )</td>
</tr>
<tr>
<td>Signal frequency</td>
<td>( fin )</td>
</tr>
</tbody>
</table>

#### Integrator
- Open-loop gain (\( As : \text{dB} \)) | 70 | 60 |
- Transconductance (\( g_m : \text{mA/V} \)) | 2.1 | 1.7 |
- Max. output current (\( Io^+, Io^- : \text{uA} \)) | 370, -370 | 240, -240 |
- Gain variation (alpha, beta) | 0, -0.2 | 0, -0.2 |
- Parasitic capacitor (\( \text{Cin : pF} \)) | 250 | 250 |
- Thermal noise (\( n \)) | 1 |
- DC offset (\( V_{os(op)} \)) | 10 mV |

#### Comparator
- L-to-H trigger voltage (\( V_{th^+} \)) | 20 mV |
- H-to-L trigger voltage (\( V_{th^-} \)) | -20 mV |

#### Feedback Voltage
- \( \Delta \) and \( -\Delta \) | 1 V and -1 V |

#### Switch
- On-resistance (\( \text{Ron(max)} \)) | 320 ohm |
- Settling error (\( \text{Esettie} \)) | < 1.6e-7 |
- Thermal noise | < 15 bits |

#### Capacitor
- Nonlinearity (\( \text{gamma_c} \)) | 50 ppm |
- Mismatch | Table 1 |

#### Clock
- Jitter (\( \text{dtau} \)) | 10 ps |

The transconductance of the opamp is measured when the output of the opamp is shorted as shown in Figure 5.13. The maximal output current (\( I_o^+ \)) is 409.3\( \mu \)A and \( I_o^- \) is -410.5\( \mu \)A. \( g_m \) is equal to 2.48mA/V. It meets the requirements in Table 5.4. The input capacitance \( C_{in} \) is measured as 208 fF.

The relation of \( V_{out} \) and \( A_0 \) is indicated in Figure 5.14. The maximal open-loop gain is 75.89dB with very flat gain variation from -2.5V to 2.5V (differential output). If higher performance is expected for the A/D converter, designers can change the
Figure 5.12: Circuit diagram of fully differential folded cascode opamp with gain boosting

Figure 5.13: Transconductance and output currents of fully differential folded cascode opamp with gain boosting
feedback voltage $\Delta = \pm 1.25V$ to increase the swing range. For this design, we still keep $\Delta = \pm 1V$ because the performance achieves 14-bit resolution.

![Relation of $V_{out}$ and $A_0$](image)

Figure 5.14: Relation of $V_{out}$ and $A_0$ of fully differential folded cascode opamp with gain boosting

Figure 5.15 shows the phase margin and unity gain frequency of fully differential folded cascode opamp with gain boosting. The phase margin is $71.6^\circ$ and the unity gain frequency is 336.6 MHz with 1-pF load. Figure 5.16 shows the noise analysis for the opamp. The low frequency band is dominated by flicker noise, which is $-10$ dB/decade with increasing of frequency. The function of differential structures can greatly reduce low frequency noise. The mid-frequency noise is dominated by thermal noise, which is $-20$ dB/decade with increasing of frequency. It is one of the fundamental noises, which dominate the noise floor in Delta-Sigma modulators. The
-3dB frequency is about 115.2 kHz; that is, noise bandwidth is \( \frac{\pi}{2} f_{-3dB} \approx 181\text{kHz} \). The output noise root spectral density [12] is \( 11.2\mu V/\sqrt{\text{Hz}} \) (or input referred root spectral density: \( 3.6\,nV/\sqrt{\text{Hz}} \)). The equivalent noise factor \( n_t \) is 0.457.

![Figure 5.15: Phase margin and unity gain frequency of fully differential folded cascode opamp with gain boosting](image)

The gain-boosted opamp is used only at the first integrator to achieve high gain, low nonidealities and good phase margin with large output current. The opamps in other integrators can tolerate more nonidealities and noises. Therefore, the opamps in Figure 5.14 without gain boosting are used and output currents are reduced to \( 0.6I_{o1} \) due to capacitor reduction.

### 5.3.2 Switch Implementation

Figure 5.17 indicates the harmonic distortion caused by signal dependence of on-resistance of switches. In order to suppress the harmonic distortion, PN MOST switches are chosen to ensure 100 dBc below signal strength within the bandwidth.
In Figure 5.17, the aspect ratio \( \frac{W}{L} \) of P MOST is \( \frac{48}{0.8} \) and the aspect ratio \( \frac{W}{L} \) of N MOST is \( \frac{30}{0.6} \). The resistance variation is between 117 Ohm and 137 Ohm with 156.25-kHz sine input and amplitude 1 V.

### 5.3.3 Integrator Implementation

After opamp and switches are designed, we can start to design switched-capacitor integrators. By using bottom-plate sampling and delay clock scheme, non-inverting switch capacitor is designed insensitive to parasitic capacitance and charge injection.

### 5.3.4 Comparator Implementation

The details of comparators are discussed in Chapter 2. Because MASH211 is more sensitive to comparator nonidealities, preamplifier is added in front of latch comparator [12] to reduce hysteresis and kickback effects. Figure 5.18 shows the circuit diagram of the latch comparator with preamplifier. The preamplifier consists
Hamionic distortion caused by switch resistance with $f_s = 156.250$ kHz and $A_{in} = 1$ V.

Figure 5.17: Power spectral density of switch harmonic distortion of a differential input stage with diode connected active loads. Low voltage gain of the preamplifier avoids large time constant to reduce the speed of the comparator. Table 5.5 lists the parameters of the comparator implemented with PSPICE. $t_{rd}$ and $t_{fd}$ meet the requirement ($< \frac{t_{rd}}{2} = 12.5$ ns). Hysteresis is measured after periodical reset: $0 < V_{H+} < 5mV$ and $-5mV < V_{H-} < 0$.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rise delay time (ut)</td>
<td>1.69 ns</td>
</tr>
<tr>
<td>Fall delay time (ut)</td>
<td>1.73 ns</td>
</tr>
<tr>
<td>L-to-H trigger voltage ($V_{H+}$)</td>
<td>$0 &lt; V_{H+} &lt; 5mV$</td>
</tr>
<tr>
<td>H-to-L trigger voltage ($V_{H-}$)</td>
<td>$0 &gt; V_{H-} &gt; -5mV$</td>
</tr>
</tbody>
</table>

Table 5.5: Circuit parameters of comparator from PSPICE
Table 5.6 summarize the circuit parameters from behavioral and PSPICE simulations. The circuit parameters meet the requirements of those from behavioral model because they are higher gain, faster and less noise and nonlinearities.

5.4 Verification

Figure 5.19 shows the result comparison from MATLAB and PSPICE after the circuit parameters have been updated. These results are close to each other only with uV difference. In order to outline the performance of the circuits, PSPICE is used to generate 256 bits at the modulator output to obtain the rough power spectral density shown in Figure 5.20. But the simulation time exceeds more than two days. Figure 5.20 indicates that the 4th-order shaped noise dominates inband noise floor. The dotted line shows the accumulated noise including harmonic distortions. Because
<table>
<thead>
<tr>
<th>Parameters</th>
<th>Behavioral Model</th>
<th>PSPICE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sampling frequency</td>
<td>$f_s$</td>
<td>40 MHz</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>$f_{in}$</td>
<td>1 MHz</td>
</tr>
<tr>
<td>Signal frequency</td>
<td>$f_{in}$</td>
<td>156.25 kHz</td>
</tr>
<tr>
<td>Integrator</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Open-loop gain ($A_e$: dB)</td>
<td>70</td>
<td>60</td>
</tr>
<tr>
<td>Transconductance ($g_m$: mA/V)</td>
<td>2.1</td>
<td>1.7</td>
</tr>
<tr>
<td>Max. output current ($I_{ov}$, $I_{io}$: uA)</td>
<td>370, -370</td>
<td>240, -240</td>
</tr>
<tr>
<td>Gain variation (alpha, beta)</td>
<td>0, -0.171</td>
<td>0, -0.171</td>
</tr>
<tr>
<td>Parasitic capacitor ($C_{in}$: pF)</td>
<td>250</td>
<td>250</td>
</tr>
<tr>
<td>Thermal noise ($n$)</td>
<td>1</td>
<td>0.457</td>
</tr>
<tr>
<td>DC offset ($V_{dc}$)</td>
<td>10 mV</td>
<td>~0</td>
</tr>
<tr>
<td>Comparator</td>
<td></td>
<td></td>
</tr>
<tr>
<td>L-to-H trigger voltage ($V_{th}$)</td>
<td>10 mV</td>
<td>$V_{th}$ &lt; 5 mV</td>
</tr>
<tr>
<td>H-to-L trigger voltage ($V_{th}$)</td>
<td>-10 mV</td>
<td>$-5 mV &lt; V_{th}$</td>
</tr>
<tr>
<td>Feedback Voltage</td>
<td>$\Delta$ and $-\Delta$</td>
<td>1 V and -1 V</td>
</tr>
<tr>
<td>Switch</td>
<td></td>
<td></td>
</tr>
<tr>
<td>On-resistance ($R_{on(max)}$)</td>
<td>320 ohm</td>
<td>137 ohm</td>
</tr>
<tr>
<td>Settling error ($E_{set}$)</td>
<td>&lt; 1.6e-7</td>
<td>&lt; 1.6e-16</td>
</tr>
<tr>
<td>Thermal noise</td>
<td>&lt; 15bits</td>
<td>&lt; 15bits</td>
</tr>
<tr>
<td>Capacitor</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Nonlinearity ($gamma_c$)</td>
<td>30 ppm</td>
<td>30 ppm</td>
</tr>
<tr>
<td>Clock</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Jitter (dtau)</td>
<td>10 ps</td>
<td>-</td>
</tr>
</tbody>
</table>

Table 5.6: Summary of circuit parameters from behavioral and PSPICE simulations

The points for FFT calculation are not sufficient, we can find the dotted line is not smooth. At 1 MHz and 10 MHz, the accumulated noise is about -83.8 dB and 0.18 dB respectively (-85.4 dB and 0.4 dB in behavioral simulation with 16384-point FFT).

5.5 Bottom-Up Verifications

After updating the circuit parameters derived from PSPICE to the behavioral model, designers can obtain the power spectral density with sufficient data (16384-point FFT) in short time. Because transient analysis does not include noise in the simulation of Figure 5.20, Figure 5.21 indicates the power spectral density of 4th-order Delta-Sigma modulator with noises and the random offset voltage is reasonably
The inband noise is dominates the noise floor as we predict. The intermodulation test is estimated under that $f_{in1} = 156.25kHz$, $f_{in2} = 468.75kHz$ and $A_{in1} = A_{in2} = 0.25V$. The result is shown in Figure 5.22. After the decimation filter ($SINC^5$ filter and 20 downsampling), Potential SNR, SNDR and SFDR are estimated indicted in Figure 5.23 after 10 simulation runs are averaged. Figure 5.24 shows the predicted harmonic distortions of the 4th-order Delta-Sigma A/D converter.

This behavioral model can also estimate performance due to process variation. After we update the circuit parameters with the different corners, SNR is estimated in Figure 5.25 with typical, $3\sigma$ slow and $3\sigma$ fast. There is no obvious deterioration in
Figure 5.20: Power spectral density derived from PSPICE with 256-point Hanning window FFT

bit resolution for process variation. Figure 5.26 shows the layout of the Delta-Sigma modulator. The center part of Figure 5.26 consists of 4 integrators with guard ring protection. In order to avoid the clock signals across the guard ring, clock signals are arranged around the chip and different voltage sources are used to avoid interference. Table 5.7 summarizes the bottom-up verifications for the performance of 4th-order Delta-Sigma A/D converter
Figure 5.21: Predicted power spectral density of 4th-order Delta-Sigma modulator with noises

Figure 5.22: Intermodulation test of 4th-order Delta-Sigma modulator with noises
Figure 5.23: Predicted SNR, SNDR and SFDR of 4th-order Delta-Sigma A/D converter

Figure 5.24: Predicted harmonic distortions of 4th-order Delta-Sigma A/D converter
Figure 5.25: SNR in different process corners of 4th-order Delta-Sigma A/D converter

Figure 5.26: Layout for the 4th-order Delta-Sigma modulator
<table>
<thead>
<tr>
<th>Performance</th>
</tr>
</thead>
</table>
| fs          | 40 MHz  
| fin         | 156.25 kHz  
| DOR         | 2 Msamples/sec  
| DR          | 87.72 dB (14.28 bits)  
| SNR (Peak)  | 86.43 dB  
| SNDR (Peak) | 85.4 dB  
| SFDR (Peak) | 100.4 dB  
| 2nd HD (Min)| -100.6 dB  
| 3rd HD (Min)| -107.6 dB  
| THD (Min)   | -97.6 dB  
| DR in corners | slow: 87.46 dB; fast: 86.9 dB  
| Intermodulation | Figure 5.22  
| Mismatch in C | Table 5.3  

Table 5.7: Summary of bottom-up verifications for the performance of 4th-order Delta-Sigma A/D converter
CHAPTER 6

CONCLUSIONS AND RECOMMENDATIONS

This chapter concludes the achievements in previous chapters. Most of the circuit behavior models are implemented in MATLAB in this dissertation. But MATLAB may not be the best choice in roundtrip design flow. In this Chapter, MATLAB, VHDL-AMS, Java and C/C++ will be discussed to fulfill behavioral simulations for future development.

6.1 Conclusions

In order to summarize the discussions and achievements in the previous chapters, conclusions are made as follows:

1. Roundtrip design strategy is introduced to reduce time-to-market and ensure desired performance in different design stages. Detailed procedure of converting system specifications to circuit specifications by behavioral simulations is proposed in Chapter 1.

2. A new behavioral model for Delta-Sigma modulators is proposed to fulfill time-domain simulations with noise effects. This model is designed to combine the
results from transient analysis and noise analysis in circuit simulators. By ar­
ranging some circuit nonidealties as input sources, minimal modifications can
be achieved when designers cascade high order Delta-Sigma modulators with
accuracy and simulation time consideration. In addition, process corners and
statistic information can be included in the behavioral simulations to leave de­
sign margin before circuit components are implemented. Chapter 2 and Chapter
3 discuss the details of the behavioral model.

3. A 14-bit 16-ksamples/s single stage Delta-Sigma modulator (Chapter 4) and a
14-bit 2-Msamples/s multi-stage Delta-Sigma modulator (Chapter 5) are used to
demonstrate the roundtrip design flow. The multi-stage Delta-Sigma modulator
is fabricated in AMI 0.5um CMOS technology.

6.2 Recommendations

In this section, MATLAB, VHDL-AMS, Java and C/C++ are discussed for im­
plementing the behavioral model proposed in this research. The simulation time for
different sample numbers is shown in Figure 6.1. Hopefully, designers can choose
wisely based on their need by using these guidelines.

6.2.1 Modeling in MATLAB

MATLAB is a very popular mathematics tool and widely used by engineers. Pow­
erful DSP toolbox makes it easy to evaluate the spectrum of pulse density streams
at the outputs of modulators. The behavioral model proposed in this dissertation is
initially implemented in MATLAB. However, when spectral average and high down-
sampling rate are necessary in the design, designers may need faster simulation speed,
especially in repeatedly using the behavioral simulations for converting system specifications to circuit specifications.

### 6.2.2 Modeling in VHDL-AMS

VHDL-AMS is standardized with IEEE VHDL 1076.1 in 1999 [26]. The powerful capability for simulating mixed-signal circuits in single kernel simplifies design and verification of both analog and digital circuits. Impressively, it can solve DAE (Differential Algebraic Equation) in continuous time domain and co-simulate with SPICE netlists. For roundtrip design procedure, it is used to perform behavioral simulations. After circuit parameters are specified, designers can implement circuit components based on the results. In bottom-up verification, multi-level abstraction from circuit results helps designers to update behavioral models for whole system simulation.
The simulation tool used for VHDL-AMS is SMASH. The circuit specifications are listed in Table 5.6 in Chapter 5. Figure 6.2 shows the proposed VHDL-AMS behavioral model for 4th-order Delta-Sigma modulator. Two packages are used to include the circuit nonidealties and circuit specifications. Package_dsm_function is implemented with the functions to model nonidealties. Designers can include any function in the package for the circuit entities dependent on the simulation time and accuracy. In this application, the first integrator is the most sensitive component in the whole circuit. Therefore, all functions are included in the first integrator model. The models of other integrators only apply a subset of the first integrator model. Circuit specifications are listed in the package, Package_circuit_spec. Parameter shifting effects on the circuit specifications are considered based on process corners, Monte Carol information and layout netlist extraction to make designs more robust to process variations.

The result of behavioral simulation is shown in Figure 6.3. In Figure 6.3, clock_in, comparator_bit_out1, comparator_bit_out2 and comparator_bit_out3 are digital waveforms (either 1 or 0) and represent 40 MHz clock, first, second and third comparator outputs respectively. If 0.125V 156.25 KHz sine is used as the input signal (0.25 V for differential mode), the output of the first integrator (int_out_inter1) roughly shows the sinusoidal waveform. The waveform is more randomized at the output of the fourth integrator output (int_out_inter4). Power spectral density is derived in Figure 6.4 by using built-in FFT function in SMASH [27] with 16384 points and Hanning window.

Although VHDL-AMS has very powerful functions for mixed signal circuit design, one problem is the speed of behavioral simulation. With the same behavioral model,
Figure 6.2: Simulation result of 4th-order Delta-Sigma modulator in VHDL-AMS

Figure 6.3: Simulation result of 4th-order Delta-Sigma modulator in VHDL-AMS
the simulation time in VHDL-AMS is only a little faster than that in MATLAB. If high oversampling ratio is desired in the Delta-Sigma modulator, it will take some time to obtain sufficient points for FFT after downconversion.

The first possible future work is to use VHDL-AMS and SPICE to form multi-level mixed-signal circuit design. In order to increase the speed of simulation, designers may pre-solve the DAE in analog behavioral models to reduce the calculation of the simulator. Reasonable trade-off with accuracy and simulation time can also improve the speed in multi-stage circuits.

6.2.3 Modeling in Java

Java is a platform-free language and widely used in the world. It makes it possible that the same source codes of behavioral models can be executed in Unix systems or Window systems. The simulation result is shown in Figure 6.5. The speed of
behavioral simulations is faster than the speed in MATLAB (only for my research case) by more than 40 times when sample number is 32K.

![Simulation result of 4th-order Delta-Sigma modulator in Java](image)

Figure 6.5: Simulation result of 4th-order Delta-Sigma modulator in Java

### 6.2.4 Modeling in C/C++

C/C++ is a very powerful computer language. In my research, the model built in C/C++ has the fastest simulation speed (faster than the speed in MATLAB (only for my research case) by more than 50 times when sample number is 32K). Today, more and more behavioral models are used in C/C++ (like System C). Possible future work is to structure C codes to make them close to hardware descriptions.

### 6.2.5 Summary

In modeling Delta-Sigma A/D Converters, because of downsampling at the digital output, behavioral simulations need to take some time to collect sufficient data.
for spectral measurement. In addition, to avoid spectral glitches, averaging several spectral data is necessary to reduce the effects. Therefore, high-speed behavioral simulations are strongly desired when the models increase in complexity for deep submicron SoC. System C may be the best choice for acceptable speed and circuit modeling for mixed signal systems such as Delta-Sigma modulators.
BIBLIOGRAPHY


