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DESIGN TECHNIQUE OF FRACTIONAL-\(N\) DELTA-SIGMA FREQUENCY SYNTHESIZER FOR WIRELESS COMMUNICATION IN 0.5\(\mu\)m SILICON GERMANIUM

DISSERTATION

Presented in Partial Fulfillment of the Requirements for the Degree Doctor of Philosophy in Graduate School of The Ohio State University

By

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ABSTRACT

This dissertation presents the design of RF synthesizer by the fractional-\(N\) Delta-Sigma modulation technique in 0.5\(\mu\)m Silicon Germanium BiCMOS process. Key merits of the fractional-\(N\) Delta-Sigma frequency synthesizer have been discussed in detail. A dual-loop scheme of phase-locked loop frequency synthesis topology is adopted for wide-range and very fast frequency acquisition. Delta-Sigma modulator provides fractional divide number control with shaped passband noise, which alleviates the disturbance of random white noise from fractional number control and provides fine frequency step for applications.

Two prototype fractional-\(N\) frequency synthesizers demonstrate good performance, low power consumption, and high level integration achieved with this proposed design approaches and SiGe IC process. Handset synthesizer prototype achieves a low phase noise of -108dBc/Hz at 100kHz offset and a low side band spur of -85dBc at 1.6MHz offset with 18mA current consumption, 1.5GHz carrier frequency. The measured results fully satisfy the system requirements of personal digital communication (PDC) and wireless integrated network sensors (WINS) applications. Basestation synthesizer prototype has a very fast locking time of 67\(\mu\)s for 100MHz frequency switching and achieves a low in-band phase noise of -94dBc/Hz at 10kHz offset with
13mA current consumption, which can be applied to many standards of mobile RF communications.
Dedicated to my family and Whuei-Wen
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CHAPTER 1

INTRODUCTION

The recent bloom in the mobile telecommunications market has captured the interest of almost all electronic and communication academic institutes and industry worldwide. Applications such as pagers, cordless phones, analog/digital cellular phones, and satellite communication have created this enormous wireless market [1]-[15].

The use of wireless products has rapidly increased in recent decades. New wireless communication systems have been developed to meet the needs of this market. The wireless market not only exists in the personal communications realm [1]-[10], but extends into the home with facilities such as Bluetooth [12], and homeRF [15]. Moreover, wireless products are being applied to the Internet market causing another wireless revolution in human history [14], [15].

The consumer nature of this market puts a premium on low-cost, low-power, high-volume implementations of radio functions that are currently implemented using integrated circuit technologies. As a result, new circuit technologies have been sought to allow the increased integration of radio transmitters and receivers, along with new
radio architectures that take advantage of such advances. The rest of this chapter will present the overview of this dissertation.

1.1 Research Objective

One of the key issues in wireless communication is frequency synthesis. Local oscillators (LO) are provided for up/down conversion of transmitting/receiving signals. The oscillators used in RF transceivers are usually embedded in a synthesizer environment so as to achieve a precise definition of LO frequency. Frequency synthesizer design still remains one of the challenging tasks in RF transceivers because it needs to meet very stringent requirements [16]-[30].

Design techniques for frequency synthesis are explored in this work. Several circuit designs for frequency synthesis will be compared. The main focus of this research is to implement the key circuit blocks of a synthesizer while staying within certain performance requirements. By using a BiCMOS SiGe process, an optimal frequency synthesis technique is demonstrated experimentally, resulting in a low-power, small die with good phase noise performance.

1.2 Organization

This dissertation focuses on design issues related to an integrated frequency synthesizer. The most important elements of the frequency synthesizer design are analyzed in this work.
In Chapter 2, the different frequency synthesis techniques are discussed. In telecommunication systems, frequency synthesis can only be implemented with phase-locked loop (PLL) techniques because of the high frequency operational requirements.

In Chapter 3, the emphasis is on the phase noise properties of the conventional PLL. A simple linear model is presented to aid in the understanding of the theoretical analysis. The agreement between the theoretical model and experimental results are studied in a later chapter.

The settling behavior of the PLL is introduced in Chapter 4. The settling of the system is dependent on the nonlinear components in the phase-locked loop, making the settling behavior of the nonlinear feedback system not easily predicted. The voltage controlled oscillator (VCO) is the nonlinear component that may dominate the settling behavior. The tradeoff of the settling is analyzed for every aspect of the PLL.

In Chapter 5, a most advanced design technique of fractional-N frequency synthesis is reviewed. Delta-Sigma modulation is applied to fractional-N control in the frequency synthesizer. This technique provides a precise, small frequency step size for the frequency synthesis. The noise shaping characteristics in the close-in frequency of the PLL reduces the disturbance of the phase noise in the voltage controlled oscillator output.

The circuit implementations of the two dividers and the RF input buffer are described in Chapter 6. Bipolar current mode logic (CML) topology is used for the dividers and the buffer.

In Chapter 7, the phase/frequency detector and charge pumps are implemented with BiCMOS technology. Single loop and dual loop versions of the phase/frequency detector are analyzed for their tradeoffs in settling time.
In Chapter 8, two silicon prototypes are presented with experimental results. The first prototype silicon is used for mobile handsets, and the second prototype silicon is applied to basestation for wireless network communication. Analysis of the frequency synthesizer design is reviewed for applications. A conventional s-domain PLL model is applied for loop analysis. The theoretically predicted results are very close to the experimental results.

Chapter 9 concludes the dissertation with a discussion of possible future research questions.
CHAPTER 2

FREQUENCY SYNTHESIS TECHNIQUES IN RF COMMUNICATIONS

Frequency synthesis is a combination of system elements that results in the generation of one or many frequencies from one or few reference sources. Frequency synthesis techniques depend very much on the required frequency range and the material properties at the designated frequencies.

In this chapter, the most common frequency synthesis techniques are categorized, according to their applied frequency ranges:

a. Phase-Locked Loop (PLL) for several MHz to around 5GHz

b. Direct Digital Synthesis (DDS), or crystal oscillator and single transistor RLC oscillator in the analog counterpart, for a frequency range of 1MHz to 50MHz

c. Operational amplifier RC oscillator circuit for less than 1MHz

d. Other techniques such as Dielectric Resonator oscillator for frequencies higher than 5GHz in microwave applications

For RF telecommunication applications, the most frequent ranges for frequency synthesis spread from several tens of MHz to less than 5GHz. Phase-locked
loops and direct digital synthesis are introduced in this chapter, as well as, the proper frequency synthesis technique for RF communication is determined.

2.1 Phase-Locked Loop

Phase-locked loops (PLLs) are analog/mixed-mode building blocks used extensively in many analog and digital systems. PLLs are widely used in clock recovery for data communication and digital systems. Another field where PLLs are used is in television and wireless communication systems for channel selection, or in the demodulation of frequency-modulated signals.

Nowadays, PLL has recently become the most significant analog/mixed-mode block in many electronic systems due to their reliability for frequency synthesis, even though they have several drawbacks that have been understood for decades.

2.1.1 Basic Topology and Operating Principle

![General phase-locked loop](image)

Figure 2.1: General phase-locked loop
A phase-locked loop is a feedback system that operates on the excess phase of nominally periodic signals, i.e., the feedback operation in the loop automatically adjusts the phase of the locally generated signal $y(t)$ to the phase of the fixed incoming reference signal $x(t)$. As shown in Figure 2.1, a PLL is composed of a phase detector (PD), a low pass filter (LPF) and a voltage-controlled oscillator (VCO). The PD serves as a phase error amplifier in the feedback loop, thereby minimizing the phase difference between $x(t)$ and $y(t)$. The loop is considered "locked" if the phase difference is constant with transient time, which results from the equivalence of input reference and output VCO frequencies.

In this locked condition the PLL operates as follows. The phase detector discriminates a constant phase difference between input reference and output VCO, whose dc value is proportional to this constant phase difference. The low pass filter suppresses high frequency components from the PD output. The resultant dc component is allowed to control the VCO to produce the desired frequency. The VCO oscillates at a frequency equal to the input reference frequency with a constant phase difference. Therefore the LPF generates a proper control voltage for the VCO.

In Figure 2.2, the PLL is initially locked and then experiences a small negative frequency step at $t_0$. Since the input reference frequency of $x(t)$ is momentarily less than the output VCO frequency, $x(t)$ accumulates phase slower than $y(t)$ does, and the PD generates increasingly wider pulses which discharge current from the loop filter. These pulses create a decreasing dc voltage at the output of the LPF. The VCO frequency is decreased by this reduced dc voltage. As the frequency difference between the reference signal and the VCO output get closer, and eventually equivalent, the width of the PD
pulses increases slightly in advance, and then returns to a slightly smaller width than the
phase difference at $t_0$.

\[ X(t) \]
\[ y(t) \]
\[ \text{PD output} \]
\[ \text{LPF output} \]

Figure 2.2: State response of phase-locked loop

A phase-locked loop is a "memory" system that requires a finite time to respond
to its reference change. Additionally, the loop state variables change dimensions. The
phase difference is converted to a voltage or current by the phase detector. Then the time
domain information of these pulses is transferred into a dc control voltage for the voltage-
controlled oscillator. Finally the voltage of LPF output is converted to phase by the VCO.

In the loop-locked condition, the VCO output frequency is exactly equal to the reference
frequency regardless of the magnitude of the loop gain. This is an extremely important
property that will vanish with only a frequency detector instead of a full phase/frequency
detector.
Phase-locked loops provide elegant solutions for several common problems, such as frequency synthesis, clock recovery, jitter reduction, and skew suppression. In RF communication systems, a phase-locked loop is employed to provide a small, precise step of frequency variation for channel selection, called frequency synthesis. Also clock recovery for data synchronization, as in data transmission and reception in optical communication systems, is provided for simply by a PLL. A communication channel of a digital signal processing system always experiences timing jitter, which manifests itself as variation during periods of the waveform. The corruption of the signal due to timing jitter cannot be removed or recovered by clipping and amplification. A PLL is used to reduce the jitter. In a digital IC, skew results from driving huge capacitance and interconnect capacitance. This exhibits itself as a significant delay between on-chip clocks and inter-chip timing, a phenomenon known as skew. A PLL can be used for timing alignment. The theoretical analysis of the basic operation and principle of a phase-locked loop is formulated in the following sections.

2.1.2 Theoretical View of Phase-Locked Loop

![Figure 2.3: Classical (Integer-N) phase-locked loop](image-url)
In practical applications, to reduce the operating frequency of the phase detector, a divider is placed in the feedback path between VCO output and phase detector input, as indicated in Figure 2.3. Compared with analog techniques used in the infancy of frequency synthesis [33], the digital PLL is dominantly used in wireless communication. Several important PLL parameters are introduced below for latter reference. The parameters are those usually used to describe the specification and behavior of a PLL.

**Phase Noise** - The measured merit of the signal quality. Phase noise and jitter are manifestations of the same phenomenon with the former being in the frequency domain and the latter in the time domain. Phase noise can be specified in a variety of ways: sec rms in terms of timing jitter, frequency modulation noise (Hz rms) or spectral distribution density (dBc/Hz). Spectral distribution density is the most widely used in documentation. In the behavioral description of jitter, several types of jitter exist. This is explained in the phase noise analysis.

**Spurious Signal/Dynamic Range** - A measure of the deterministic, discrete and periodic interfere noise in spectrum, which is called "spurs". Spurious noise is part of the noise spectrum, not related to the signal carrier itself. Usually, spurs are measured by dBc to carrier power.

**Frequency Tuning Range** - The total frequency bandwidth needed for the applications. For example in the US, AMPS, North American cellular standards, TDMA, and CDMA all have the same bandwidth, 25MHz. The frequency tuning range of a PLL is primarily limited by the VCO tuning range in circuit implementation.
**Frequency Tuning Step Size** - The smallest frequency increment size, usually specified by channel spacing in an integer-$N$ PLL. Channel selection of the transceiver is "frequency-synthesized" with this frequency tuning step size. An example is the 200kHz step size required by the GSM cellular system.

**Locking/Settling Time** - A measure of the time that the PLL takes to tune the VCO frequency from one to another within a certain frequency resolution. The frequency resolution is defined by a specified frequency tolerance from the final target frequency. For example, the PLL is locked in 400µs with 1kHz resolution.

**Loop Bandwidth** - The measure of the dynamic speed of the feedback loop. It is described by unity gain bandwidth of the open loop frequency response of the PLL. Loop bandwidth is a significant parameter when optimizing the performance of phase noise, spurs and locking time.

Two frequency synthesizer architectures are commonly used in applications nowadays, integer-$N$ and fractional-$N$ synthesizers. The two implementations are slightly different due to the randomization of fractional division in the main divider $(\pm N)$, as shown in Figure 2.3. Here a classical integer-$N$ synthesizer is used for analysis example. More details of fractional-$N$ synthesizer are revealed in later sections.

In Figure 2.3, the PLL circuit performs frequency multiplication, through a negative feedback path, to generate the output frequency, $f_{\text{vco}}$, in terms of the reference frequency, $f_{\text{ref}}$:

$$f_{\text{vco}} = f_{\text{ref}} \cdot \frac{N}{R} \quad (2.1)$$
A reference frequency is provided to the phase detector for comparison of the divided VCO frequency. The reference frequency is typically divided by a factor of R in an R divider block. In a "locked state," the VCO frequency must be equal to the above equation, thus programming the N divider with a new division number can change the VCO output frequency, resulting in a VCO that can be tuned through the overall band of interest. The only constraint of this integer-N architecture is minimum channel spacing equal to $f_{\text{vco}} = \frac{f_{\text{ref}}}{N}$. As long as the loop is locked, the VCO output will have the same frequency resolution as the reference frequency, which is typically dependent on an external crystal oscillator. For example, with a reference frequency of 30kHz and an N division number of 33000, the VCO output frequency is 990MHz. Assuming that the frequency resolution of the oscillator is 1ppm, the output of the VCO is accurate to ± 990Hz around a 990MHz carrier frequency.

The problem in this integer-N PLL is trade-off between phase noise and settling time when N becomes large. The phase detector noise is the most dominant close-in phase noise source, assuming that the R/N dividers and the crystal oscillator have low enough phase noise to be neglected. When division number N is large, it becomes a limiting factor of close-in phase noise at the VCO output. Thirty thousand is a typical division number used in today's cellular communication systems with a 30kHz reference. This division number will increase 90dB up to the phase detector noise floor. If the close-in phase noise is expected to be extremely low enough, the division number needs to set as low as possible. Unfortunately this division number is fully dependent on the channel spacing and VCO output frequency. Additionally the divided-by-R reference frequency
can be seen as a spurious signal and modulated by VCO, generating its harmonics. So a narrow bandwidth loop filter is necessary to suppress this modulated signal appearing at the VCO output. On the other hand, the narrower the bandwidth of the loop filter is, the longer the resulting settling time is. Those are the drawbacks of integer-\(N\) phase-locked loop.

A technique called fractional-\(N\) frequency synthesis has recently emerged to resolve the above limitation. This is accomplished through the use of a randomized division number, \(N\), during the locked state of frequency synthesis. The original fractional-\(N\) idea is based on Gibbs and Temple’s work in 1978 [34]. The value of the main divider is switched between \(N\) and \(N+1\). Over a long period of time, an average fractional division ratio can be realized as \(N + \frac{K}{F}\), according to the following equation;

\[
f_{vco} = f_{ref} \cdot (1 + \frac{K}{F}) \cdot N
\]

where \(K\) is the fractional channel of operation and \(F\) is the fractional modulus (i.e. fractional resolution); \(K, F, N\) are integers.

The phase detector can operate at a frequency higher than the channel spacing and can achieve frequency resolution for the channel spacing requirement. So the switching speed of this fractional-\(N\) frequency synthesizer is increased by the large loop filter bandwidth. The channel spacing is fully specified by the fractional operation of the \(N\) divider with a lower division ratio resulting in low close-in phase noise from the phase detector.
The four basic blocks of the PLL circuit are the VCO, the main (+N) and reference (+R) dividers, the phase frequency detector and the loop filter. Usually the loop filter and the VCO are excluded outside the die of the dividers and the phase frequency detector to prevent switching noise coupling to them. The loop filter is quite large for an integrated circuit in most applications. Recently, the integration of the VCO and loop filter has been carried out using improved design techniques and IC technologies [16], [17], [19], [20], [22], [23], [25]-[29].

2.1.3 Fundamental PLL Mathematical Model

The PLL shown in Figure 2.3 can be analyzed by a mathematical model. The qualitative descriptions and models of each main block in the PLL will be explained before going through the corresponding mathematical analysis. In the PLL all of the major blocks other than the R-divider are within the loop. There are two characteristics of the blocks within the PLL loop that need to be included in the analysis to determine the general behavior of this entire negative feedback loop, their open-loop and closed-loop functions.

Since different dimensions are used to translate through the internal states of the PLL, the loop behavior is determined by the phase information of the reference and VCO output frequencies. In Figure 2.3, G is an intermediate gain stage for translating the different tuning ranges between the loop filter and the VCO. Usually amplifier-based circuits can implement this gain stage. Here assume unity values for R and G for simplicity. A linear model of the PLL is shown in Figure 2.4 for easy analysis.
For the N-ratio and R-ratio divider blocks, the input signal frequency or phase is divided by the set ratio. Obviously the phase noise of these two blocks is $20 \cdot \log_{10}(N)$ or $20 \cdot \log_{10}(R)$ dB lower than the phase noise of their input signals. The phase detector behaves like a linear phase error comparator. When the phase error of the two inputs increases linearly, the output dimension of the phase detector also increases linearly. Here assume that the gain of the phase detector is $K_{pd}$. Usually the phase detector with a charge pump pours, or sinks, the current to charge, or discharge, the loop filter. Thus $K_{pd}$ can be expressed as $\frac{I_{cp}}{2\pi}$, where $2\pi$ is normalization factor. Another approach uses the output voltage swing of a charge pump to characterize the phase detector gain as $\frac{V_{swing}}{2\pi}$.

The loop filter can be seen as an impedance transformation between the phase detector and the VCO. The transformation is easily synthesized by simple passive electrical circuits theory analyzed in the frequency domain. As the function of the VCO, the voltage output of the loop filter is translated to the frequency domain. Sometimes, a current-controlled oscillator is also used sometimes in PLL design. Voltage-to-frequency transferred gain is adopted in this design and analysis.

On the basis of Figure 2.3, 2.4, the N divider divides the VCO frequency, hence the phase of the VCO, by a factor of N. Assume that the phase detector gives a linear output current proportional to the difference of $\Phi_{\text{ref}}(t)$ and $\Phi_{\text{o}}(t)$. Taking the Laplace transform for time to frequency transformation, the output of the phase detector is given by:
Figure 2.4: Linear PLL model

\[ \Phi_e(s) \cdot K_{pd} = (\Phi_{ref}(s) - \frac{\Phi_o(s)}{N}) \cdot K_{pd} \]  \hspace{1cm} (2.3)

\[ \Phi_o(s) = \Phi_e(s) \cdot K_{pd} \cdot H(s) \cdot \frac{K_{vco}}{s} \]  \hspace{1cm} (2.4)

where \( K_{pd} \) is measured in units of V/rad, and \( K_{vco} \) is in units of rad/V. The PLL is depicted as a standard feedback network with a forward transfer path and a feedback transfer path. The open loop transfer function is expressed as;

\[ OL(s) = \frac{K_{pd} \cdot K_{vco} \cdot H(s)}{N \cdot s} \]  \hspace{1cm} (2.5)

This open loop transfer function will be used in the study of the loop response to phase noise and transients.
Noise from the reference signal and noise generated in the VCO, represented by \( \Phi_{\text{ref}}(s) \) and \( \Phi_{\text{vco}}(s) \) respectively, contribute most of the phase noise in the PLL. The noise transfer function is calculated as follows:

\[
\Phi_{o_{-\text{ref}}}(s) = \frac{K_{pd} \cdot K_{vco} \cdot H(s)}{N \cdot s + K_{pd} \cdot K_{vco} \cdot H(s)} \cdot \Phi_{\text{ref}}(s) \tag{2.6}
\]

\[
\Phi_{o_{-\text{vco}}}(s) = \frac{N \cdot s}{N \cdot s + K_{pd} \cdot K_{vco} \cdot H(s)} \cdot \Phi_{\text{vco}}(s) \tag{2.7}
\]

\( \Phi_{o_{-\text{ref}}} \) and \( \Phi_{o_{-\text{vco}}} \) are the phase noise portions at the output of the VCO, and \( K_{pd} \cdot K_{vco} \) is called loop gain of the PLL. The loop filter has a first order function of \( \frac{1}{1 + \frac{s}{\omega_{lp}}} \) for a voltage input signal. \( K_{lp} \) is the dc gain of the low pass filter and set to unity for now.

\[
\Phi_{o_{-\text{ref}}}(s) = \frac{K_{pd} \cdot K_{vco} \cdot \omega_{lp}}{N \cdot s^2 + N \cdot \omega_{lp} \cdot s + K_{pd} \cdot K_{vco} \cdot \omega_{lp}} \cdot \Phi_{\text{ref}}(s) \tag{2.8}
\]

\[
\Phi_{o_{-\text{vco}}}(s) = \frac{N \cdot s^2 + N \cdot \omega_{lp} \cdot s}{N \cdot s^2 + N \cdot \omega_{lp} \cdot s + K_{pd} \cdot K_{vco} \cdot \omega_{lp}} \cdot \Phi_{\text{vco}}(s) \tag{2.9}
\]

A simple power spectral density plot of the phase noise contribution from the VCO and the reference signal is shown in Figure 2.5. The units in Figure 2.5 are not scaled. This
indicates that the noise transfer function of the VCO is a high-pass function and the reference signal is amplified by the closed-loop function of the PLL. Therefore, the VCO noise contributes a large portion of the total phase noise around the crossover frequency and far-end frequency, $\omega_c$, which is the unity gain frequency of the open-loop transfer function in Equation (2.5). On the other hand, the reference signal contributes a large amount of the phase noise in close-in frequency. The total phase noise is dominated significantly by these two noise sources. In a later chapter, a more detailed analysis of the phase noise will be introduced.

![Figure 2.5: Spectral density of phase noises from the VCO and reference signal](image)

It is obvious that in the denominator of Equations (2.8) and (2.9) the VCO contributes one pole and the low-pass filter contributes another. The denominator is easily converted to a familiar form in control theory, $s^2 + 2 \cdot \zeta \cdot \omega_n \cdot s + \omega_n^2$, where $\zeta$ is the damping factor and $\omega_n$ is the natural frequency of the PLL system. The natural frequency,
\( \omega_n \) is derived as \( \sqrt{\frac{\omega_{lp}}{N} \cdot K_{pd} \cdot K_{vco}} \) and the damping factor \( \zeta \) is derived as \( \frac{1}{2} \sqrt{\frac{N \cdot \omega_{lp}}{K_{pd} \cdot K_{vco}}} \).

The settling behavior of the PLL is determined by these two important parameters. More details will be explored in a later chapter.

The key issues of PLL behavior are addressed briefly in this section. To better understand the PLL, phase noise and locking behavior will be the main topics in this research design.

### 2.2 Direct Digital Frequency Synthesizer

In direct digital frequency synthesis (DDS), the digital values of the waveform stored in a memory create the sinusoidal wave by a reference clock. The simplified DDS diagram is shown in Figure 2.6. DDS is composed of a linear phase accumulator, a SINE and COSINE look-up table or phase-to-amplitude converter, a digital-to-analog converter, and a low pass filter.

![Figure 2.6: Direct digital synthesizer](image)

Figure 2.6: Direct digital synthesizer
2.2.1 Operation Theory

The sinusoidal waveform is typically presented in terms of its amplitude form, such as \( a(t) = \sin(\omega t) \) or \( a(t) = \cos(\omega t) \). However, it is difficult to generate a pure linear sinusoidal wave from this except through piece-wise construction. On the other hand, the angular information of sinusoidal wave is linear in nature. The angular rate is dependent on the frequency of the signal by the traditional definition: \( 2\pi f \). The phase rotation for the clock period can be determined as \( \Delta \text{phase} = \omega dt = 2\pi ft \). Assuming that the timing change of reference clock is \( dt = \frac{1}{f_\text{ref}} \), the output frequency of DDS would be shown in Equation (2.10).

\[
f_o = \frac{\Delta \text{phase} \cdot f_\text{ref}}{2\pi}
\]

The DDS can be implemented by using this simple principle. The basic operating principles of each building block are introduced.

The phase accumulator is a variable-modulus counter that increments the number stored in it each time it receives a clock pulse. When the counter overflows it wraps around, making the phase accumulator output contiguous. The control word of the phase accumulator sets the modulus of the counter effectively determining the size of the increment in the phase accumulator per clock cycle. The larger the added increment, the faster the accumulator overflows. This results in a higher output frequency. Sinusoidal
waves repeat themselves in a $2\pi$ phase range. The accumulator scales the range of the phase numbers into a multi-bit digital word. The $\Delta \text{phase}$ is scaled into a range of number from 0 to $2^j - 1$. As shown in Equation (2.10), fractional division is easily obtained by DDS. Also, if the $\Delta \text{phase}$ is equal to the least significant bit, then $\Delta f = \frac{f_r}{2^j}$ is called the resolution of the DDS. For example, the phase accumulator word length of 32 bits can be chosen to achieve a frequency resolution of 0.00349Hz at the clock rate of 150MHz. The phase noise of such high precision DDS is extremely low.

To covert the linear phase information to sinusoidal amplitude, a SINE or COSINE look-up table is used. Since the amount of the look-up table memory required to encode the entire width of the accumulator is prohibitive [35], a smaller number is used. For instance, 12 significant bits are used out of 32 bits input at the accumulator. The phase resolution of 12 bits results in a spurious performance of $-72\text{dBc}$ due to the truncation of the phase accumulator input. As a rule of thumb, one or two more bits are chosen at the input of the phase-to-amplitude converter than at the DAC input. This would make the spurious performance, due to the truncation of the phase accumulator, low enough compared to the resolution of the DAC.

On the other hand, for low power dissipation, the word length of each algorithm should be minimized. Thus optimization of DDS performance involves a trade-off between word length and sinusoidal spectral purity, frequency resolution. A straightforward implementation of the sinusoidal wave requires a $2^j \times 10$-b ROM, whose access time reduces the maximum DDS clock frequency. A sine memory compression technique has been applied to reduce the size and access time of the look-up table ROM.
The most elementary technique stores only a quarter radian of the sinusoidal information in the ROM and generates the full range of the sinusoidal wave by exploiting the symmetry of the quarter sinusoidal wave.

The digital sinusoidal wave output of the DDS clock drives a high-speed digital-to-analog converter that constructs the sinusoidal amplitude information in analog form. The sampled DAC output follows the Nyquist rate theorem. Specifically, alias signals (images) occur at the multiples of the reference clock frequency below or beyond the fundamental frequency. In the frequency domain, the alias images are prominent and the relatively high energy level is determined by the roll-off of the sinc function, depending on the frequency relationship of the fundamental and reference frequency. The alias signal can even appear in the order of the $-3\text{dB}$ frequency range. Therefore, a low pass filter is necessary to suppress the alias images. Increasing the accuracy comes at the expense of the high-speed performance in the DAC. The DDS permits the phase to be set by setting the number in the accumulator. It can change the frequencies very rapidly and can obtain fine frequency resolution.
2.3 The Comparison of PLL and DDS

The following items are the main differences between PLL and DDS.

- **Phase-Locked Loop**
  - Switching speed between frequencies and frequency resolution depends on the loop filter.
  - Phase noise mainly depends on the design of the loop filter, reference clock and VCO.
  - A feedback loop system with a very non-linear component, VCO.

- **Direct Digital Synthesizer**
  - High resolution in a range of sub-Hz.
  - Fast switching speed by digital tuning.
  - Extremely low phase noise.
  - Highly complex and power hungry.

The phase-locked loop is inherently slower than other types of frequency synthesizers because of its negative feedback loop characteristics. Programming the division number of the N-divider results in a slow change of the VCO tuning range as the loop acquires its steady-state operation. The switching speed is dependent on the loop bandwidth that is limited to one-tenth of the reference frequency at least for spurs suppression. The PLL block design is undertaken carefully, since low frequency noise is generated by the loop components, other than the VCO, and is modulated with the VCO. Poor design would corrupt the output phase noise spectrum. The VCO contributes far-end
phase noise beyond the loop bandwidth; therefore a high quality VCO is required for meeting the far-end noise requirement. Many limitations are introduced on top of the design criteria in integer-$N$ PLL. In the most recent decade, a modified PLL called a fractional-$N$ frequency synthesizer has been widely used in applications because of its flexibilities in loop bandwidth, fractional division and phase noise performance. This type of frequency synthesizer is considered only.

Although DDS can have fast frequency switching and fine frequency resolution due to its feedforward architecture and digital tuning operation, the high-speed and highly linear performance of its digital/analog components limits its RF frequency applications. The last two analog components, the DAC and the low pass filter, will easily introduce non-linearity of the synthesized sinusoidal wave. This increases the design difficulty in DDS.

Another possible integration technique has been proposed for both high frequency operation and fast frequency switching. It is called “Direct Digital Frequency Synthesis (DDFS)” [37]. The main advantage of this technique is a fixed PLL frequency. The loop bandwidth can be optimized for noise since the reference frequency is free. The output frequency can be changed rapidly and in small intervals by changes of the DDS synthesized frequency in the digital domain. On the other hand, DDFS suffers from a limited frequency tuning range because of the low bandwidth of the incorporated DAC. With a high-speed DAC requirement, the purity of the output spectrum and power consumption become important issues when increasing the tuning range. An expanded architecture, called a “dual-loop indirect synthesizer” [38], has more freedom than a standard PLL. Its drawback is the fact that its topology requires accurate quadrature
phases, low harmonic distortion, and well-matched mixers in both PLLs. To reduce the problem of a single-side-band (SSB) mixing process, the mixer is placed inside one loop of the two PLLs such that the loop filter in the first PLL can suppress the harmonics.

In the above section, the conventional PLL and DDS are discussed for their advantages and drawbacks for certain applications. Most recently, Razavi used the combination of a PLL and DDS for frequency synthesis [38]. Their advantages have been combined for low RF frequency noise and fine frequency step tuning. A monolithic dual loop synthesizer is proposed by Yan and Luong for GSM receivers [29], which have one of the most stringent phase noise requirement in wireless communications. These developments in the design of frequency synthesizers reflect the importance of frequency synthesis in wireless applications.

In this work, a fractional-\(N\) Delta-Sigma synthesizer is chosen for frequency synthesis in communications systems. This phase-locked loop has advantages in its less complex hardware and high frequency step resolution. Its credits for the higher switching speed and lower phase noise for RF applications has been accounted. Its frequency synthesis can be applied to a majority of existing communication standards. This type of frequency synthesizers provides flexibility in the loop filter design and reference clock frequency. Also, Delta-Sigma modulation minimizes the fractional spurs, definitely reducing the contamination of the spectrum purity for telecommunications.
CHAPTER 3

PHASE NOISE PROPERTIES OF PHASE-LOCKED LOOP

In this chapter, the phase noise of a phase-locked loop is introduced and examined for its influence on the PLL performance. The resultant noise model will be translated into the circuit level. The work in this chapter focuses on a detailed examination of each noise source in the PLL system.

The total noise in a phase-locked loop is broken down into three important contributing blocks, the VCO, the reference clock and dividers, and the phase frequency detector. Here noise descriptions of these blocks are examined and analyzed in order to make a sophisticated prediction of the PLL design. The far-end phase noise is completely dominated by the VCO noise effects. Alternately, the close-in phase noise is contributed to by several noise sources resulting from more complicated circuitry. Therefore, the phase noise estimation hardly ever relies on the simulation tools. Hand-calculation helps the understanding of the first-cut design, and will help in comparing the established noise model with the linear approach and the experimental results discussed in the later chapters.
3.1 Phase Noise

An oscillator example is used for explanation of the phase noise. Noise injected by its constituent devices and by external sources may influence the frequency and amplitude of the output signal. In most cases, the disturbance of the amplitude is negligible or unimportant. Random deviation of the frequency can be viewed as random variation in the period or deviation of the zero crossing points from their ideal position in the time domain. Many different literatures have discussed the many side considerations that impact the theory of phase noise [39]-[46].

A nominally periodic sinusoidal signal, \( A \cdot \cos(\omega \cdot t + \phi_n(t)) \), is written, where \( \phi_n(t) \) is a random excess phase that represents the variation in the period. Assuming that the random excess phase is very small, then this periodic signal approaches this expression: \( A \cdot \cos(\omega \cdot t) - A \cdot \phi_n(t) \cdot \sin(\omega \cdot t) \). Easily seen in the equation, the random

![Phase Noise Spectrum in an Oscillator](image)
phase is translated into the frequency domain around the carrier frequency of $\omega_c$ as noise (see Figure 3.1). The phase noise spectrum exhibits “skirts” around the carrier frequency. Usually, a unit bandwidth at an offset frequency, with respect to the carrier frequency, is defined for phase noise calculation and the noise power within the defined bandwidth divided by the carrier power is the phase noise of the carrier, dBc/Hz quantitatively. Simple mathematical processes have been introduced for phase noise mechanisms [39]-[46].

Why does the phase noise become a measure merit of the PLL performance in RF communication systems? Considering the transceiver in an RF communication system, local oscillation signals are needed for both transmission and receive chains. Usually, the frequency synthesizers are the generators of the local oscillation signal. For example, in a receive chain, the down-converted signal can be extracted and recovered by a channel select filter for the prevention of interferer corruption. As the phase noise skirt appears in the local oscillator, it is mixed with the down-converted signal and interferes into the baseband. The skirt effect in the baseband causes the pollution of the down-converted signal due to the extended noise skirt of the down-converted interferes to the signal, and reduces the signal-to-noise ratio of the receive chain. The bit error rate of the digital receiver detection may increase [47], [48]. This example explains the importance of low phase noise performance in PLLs or frequency synthesizers.
As mentioned above, a PLL inputs both the local oscillation signal and the phase noise into the mixers of the transceivers. Therefore, minimizing the phase noise of the PLL is one of the significant issues in design. The linear macro noise model of the PLL system is shown in Figure 3.2. The noise-generating blocks include reference clock, reference clock divider (R-divider), main divider (N-divider), phase frequency detector, low pass filter and VCO. Assume that all noises are small enough, when compared with the useful signal in the corresponding block, that they can be translated to Laplace form directly. Also assume that all noises are random by nature and uncorrelated, the superposition of the spectral density is used for all noises. This is very useful for the understanding of the phase noise contributions from each block in the PLL.
In reality, the noise model of each block may be built experimentally or mathematically [49]. The equation of the noise model at close-in frequencies is shown as;

\[
S_{\text{o,n}}(f) = S_{\text{ref,n}}(f) \cdot \left(\frac{N}{R}\right)^2 + \left[ S_{\text{rd,n}}(f) + S_{\text{nd,n}}(f) + \frac{S_{\text{pd,n}}(f) + S_{\text{lp,n}}(f)}{K_{\text{pd}}^2}\right] \cdot N^2
\]  

(3.1)

This equation is an approximate of the output phase noise at close-in frequencies. Here the focus of the phase noise analysis is put on the close-in frequency range where the complexity is located. So, as easily seen in Equation (3.1), the close-in phase noise is correlated to the division ratio of the N and R dividers, and the phase detector gain. The phase noise can be reduced with a large phase detector gain and a large division number of the R-divider. The larger the divided number of the N-divider is, the more phase noise that appears around the carrier frequency. This is very important for the integer-N PLL design, especially in narrow band communication systems. Usually, the reference clock frequency cannot exceed the channel bandwidth; a large division number of the N-divider is required. This large division number limits low close-in phase noise in the integer-N PLL. The fractional-N PLL will be introduced to overcome this drawback of the integer-N PLL. The VCO phase noise is high-pass filtered at the close-in frequency range (see Equation (2.9)) and dominates the out-bandwidth frequency range. The phase noise is explicitly described in the frequency domain (see Figure 2.5).
3.2 Phase Noise of the Building Blocks in PLL

Phase noise of the VCO is one of the most important noise sources in the PLL system. Sophisticated noise analysis and discussion of the VCO has been done in many papers [36]-[46]. The focus of this work is on the balanced design of the PLL rather than individual blocks; so brief discussion is made for the phase noise of the VCO as follows. Basically, the phase noise of the VCO can result from the structure portion, non-linearity portion and substrate/power supply noise portion. Many different VCO structures have been analyzed and implemented for low phase noise and high resonant frequency [50]-[60]. For RF applications, the most commonly used topology of a VCO is an LC resonator with positive feedback active devices, and its extensions, due to their good high frequency performance and good noise performance. The ring oscillator at RF levels has raised interest among complementary metal-oxide semiconductor (CMOS) IC designers because it is simple, fast and readily yields output phases in quadrature. The mismatch of the active devices in the VCO can create an unbalance resonance signal in the operation. The VCO also modulates with external tones and noises, so the nonlinear frequency components will appear in the output of the VCO. The phase-locked loop must typically operate from the global supply and ground buses, thus it experiences the noise from both substrate and power supply. This noise manifests itself as jitter at the output of the PLL. Typically the contribution of the electronic devices noise in the VCO is much less than the noise due to the substrate and power supply. Usually the differential configuration of the VCO is used for reducing the noise effects from the substrate and power supply. All of the noises are modulated within the VCO and appear at its output as phase noise.
These noise considerations make the integration of the VCO with the other parts of the frequency synthesizer difficult. In most of the customer applications the VCO still stands individually, apart from the rest of the frequency synthesizer.

Several sources can result in phase noise of the VCO, such as random walk noise and flicker noise of the electronic devices in the VCO itself [43], [45]. The small disturbance from the power supply rail will easily raise the phase noise of the VCO. The model can be easily expressed by,

\[ S_{\text{vco-no}}(\omega) = \frac{\Gamma_{\text{rms}}^2}{q_{\text{max}}^2} \cdot \frac{1}{4 \cdot \omega^2} \]  

(3.2)

\( \Gamma_{\text{rms}} \) is the impulse sensitivity function [45]. Additionally, the noise of the electronic devices is modulated by the VCO and becomes a portion of the phase noise at the VCO output. The mathematic model [45] can be the follow equation,

\[ S_{\text{vco-f}} = \frac{c_0^2 \cdot K_f \cdot I_{g}^2 \cdot \text{N}_{\text{stage}}}{4 \cdot \omega^3} \]  

(3.3)

Not only the substrate and power supply noise affects the noise performance of the VCO, but also does the input buffer stage noise of the reference clock. The time domain jitter can be modeled as a function of the jitter distribution multiplied by the
proportion of the noise magnitude and supply voltage. By the autocorrelation of timing jitter, the spectral density of the power supply noise can be calculated as the expression;

\[
S_{\text{sp}}(\omega) = \frac{\Psi_s^2}{2} \cdot \frac{1}{V_{\text{sp}}^2} \cdot \frac{N_{\text{sp}}}{2}
\]  

(3.4)

where \(\Psi_s^2\) is the rms noise factor of the power supply, \(N_{\text{sp}}\) is the noise floor of the power supply and \(V_{\text{sp}}\) is the supply voltage. A battery or regulator can be used to support the power supply line. The noise floor can be measured as \(-138\text{dB}\) by a reference voltage regulator in present market products.

Provided that both \(N\) and \(R\) dividers are themselves internally noiseless, the input signal noise injected into them is decreased by \(20 \cdot \log_{10}(N)\) or \(20 \cdot \log_{10}(R)\) at the respective output. Since the noise performance of both dividers is difficult to analyze because of the more complicated circuits of those dividers. Usually large, power hungry of the CMOS devices is necessarily used for low noise design.

The phase detector is in the feed-forward path of the PLL (see Figure 3.2), noise in this block is amplified by the close loop transfer function. Therefore low noise is critical in the phase detector design. The simplest topology of the phase detector is a mixer, which operates as an exclusive-OR function. The noise of a bipolar transistor is usually much lower than that of CMOS equivalent. The output noise of the mixer can be seen as the sum of the noise floor of the input signal plus the noise figure of the mixer [61]. The noise figure of the mixer-based phase detector can be up to 15dB. Approximately speaking, the two-port phase detector can contribute 3dB noise figure
more than one port model. The flicker noise portion is ignored for simplicity; the noise equation is,

\[ S_{pd}(\omega) = NF_{pd} \cdot \frac{No}{2} \]  \hspace{1cm} (3.5)

The loop filter also contributes noise into the VCO tuning lines, which is then modulated by the VCO operation as part of the phase noise. Two configurations of filters are commonly used in the loop filter design. One is composed of passive resistors and capacitors; the other is designed by using operational amplifier (opamp) and passive devices. The reason to use the RC-opamp type filter is the large tuning range of the VCO, when the tuning range of the VCO exceeds the power supply rail of the integrated circuits on chip. In fact the opamp contributes more noise than passive devices do. The very low frequency flicker noise can possibly become the dominant phase noise source at the very close-in frequency of the VCO output. To lower the flicker noise of the opamp, more power consumption in it may be necessary. The following analysis does not include the opamp, assuming that the tuning range of the VCO is matched to the loop filter output.

The thermal noise of the first-order loop filter with one zero visible at the output of the VCO can be expressed as;

\[ S_{\phi}(s) = i_n^2 \cdot R^2 \cdot K v^2 \cdot \frac{(s + \frac{1}{RC})^2}{s^4} \]  \hspace{1cm} (3.6)
where $\overline{I_n^2}$ is the noise spectral density, $RC$ is the timer constant of the zero and $Kv$ is the gain of the VCO.

The above equations of the noise model for each block of the PLL [62] are applied into the linear small noise signal model. The noise of the VCO itself and the noise injected into the VCO, such as filter noise, should be shaped by the PLL as a high-pass function. The divider noise and the phase detector noise are seen to inject into the PLL close loop. This noise contribution is similar to the Delta-Sigma modulator operation [63].
The input-output close loop transfer function of the PLL is obtained from Chapter 2, and is simply expressed as the following equation;

\[ H_{\text{PLL}}(s) = \frac{\omega_n^2}{s^2 + 2 \cdot \zeta \cdot \omega_n \cdot s + \omega_n^2} \]  

(3.7)

The VCO noise transfer function is easily derived from Equation (3.7) as \(1 - H_{\text{PLL}}(s)\). So the phase noise of the PLL can be composed of two portions: high-pass noise portion and low-pass portion. The plot of the noise transfer function of the VCO and the input referred noise is shown in Figure 3.3. In Figure 3.4, total phase noise of the PLL is shown. Assuming that the first-order filter is used; the loop bandwidth of the PLL is 10kHz, and the damping factor is 0.7. Figure 3.4 indicates that the phase noise in the close-in frequency is dominated by the noise of the input stages, such as the reference clock, and phase frequency detector. The noise is amplified by the loop gain. The phase noise of the VCO is high-pass filtered. The phase noise around the loop bandwidth and at the far-end frequency is dominated totally by VCO noise. The frequency index means the power of 10, which translates the unit of the x-axis to frequency (Hz). Here, for simplicity, the phase noise of the main divider (÷N) is not considered. The N-division factor is going to amplify the input noise of the reference clock, phase detector, etc (see Equation (3.1)).

Although the case is more complicated in the real design, the purpose of this analysis is to understand the phase noise distribution from each block of the PLL. Indeed this simply builds the effective noise model for the PLL design.
Figure 3.4: The noise spectrum of the PLL
CHAPTER 4

SETTLING BEHAVIOR OF PHASE-LOCKED LOOP

In addition to phase noise, the settling time of the PLL is an important parameter in telecommunication systems. The settling is dependent on the loop behavior of the PLL. Similar to a feedback amplifier, such as a buffer configuration, the settling can be analyzed through its step response. The accuracy of the settling is also correlated to the loop gain of the PLL. The frequency resolution of the VCO output is affected by this factor.

However, a high order system (>2) is difficult to analyze by equation only. More results are obtained with behavioral simulation. The basic understanding of the settling is going to help the higher order system. A second order system is used as an example in this chapter.

4.1 The Stability and The Settling Behavior

As is well known in feedback control systems, the poles of the denominator determine the stability of a closed-loop system. To be stable, the poles of the system must be located on the left half of the s-plane. Any pair of complex conjugate poles on the imaginary axis gives rise to sustained sinusoidal oscillation. Poles on the right half of the
s-plane result in a growing oscillation. In the design of the PLL, the poles of the loop transfer function must be on the left half of the s-plane. This is the first criterion in the design.

As long as the loop is stable, the settling behavior is fully dependent on the loop bandwidth and the damping factor. Together they decide the settling time of the PLL. For example, the denominator of the two-pole system can be expressed as:

\[
(1 + \frac{s}{\omega_{p1}}) \cdot (1 + \frac{s}{\omega_{p2}}) = s^2 + \frac{\omega_n}{Q} \cdot s + \omega_n^2
\]  

(4.1)

Here \( Q \) is called the quality factor of the poles, and \( \omega_n \) is called pole frequency. A geometric interpretation of the pole frequency is the radial distance of the poles. The quality factor \( Q \) is interpreted as the pole frequency divided by twice distance of poles from the imaginary axis on the s-plane. If the poles are on the imaginary axis, \( Q \) is infinite. \( Q \) determines the damping behavior of the step response. The higher \( Q \) is, the larger the overshoot ripples are. Usually this results in a larger settling time. The frequency response is flatter with small \( Q \) value. \( Q \) is translated to the inverse proportion of two times damping factor \( \zeta \).
Figure 4.1: The settling behavior of the PLL with different damping factors

Using Equation (3.7) for the settling analysis, the input is a step response. The output response is shown with different damping factors in Figure 4.1. The best settling case appears with $Q = 1.414$ ($\zeta = 0.707$). As $Q$ increases, the ripple of the settling gets higher. The above case is only for the basic settling behavior of the feedback loop system, such as feedback amplifier, filter or PLL. What is the actual interaction between damping factor and filter bandwidth or loop gain of the PLL? It is very useful to build this information for the fast-switching PLL design.
4.2 Optimal Settling and Filter Bandwidth/Loop Gain of PLL

For simplicity, the second order system is still used to analyze the relation of the settling and filter bandwidth/loop gain of the PLL. From Equations (2.8) and (3.7), it is found that, there is a slight difference between these equations, if the divided-by-N factor of the main divider is counted. At this moment, the divided-by-N factor is ignored as unity. Two equations are easily matched for the relation among damping factor and filter bandwidth and loop gain. The equations are expressed as,

\[ \omega_n = \sqrt{\omega_{lp} \cdot K_{pd} \cdot K_{vco}} \]  \hspace{1cm} (4.2)

\[ \zeta = \frac{1}{2} \cdot \sqrt{\frac{\omega_{lp}}{K_{pd} \cdot K_{vco}}} \]  \hspace{1cm} (4.3)

Obviously, for a fast-switching PLL, the loop bandwidth of the PLL should be enlarged; meaning a larger filter bandwidth and loop gain. The damping factor is the root proportion of the filter bandwidth and loop gain ratio. In order to obtain the larger loop bandwidth with an optimal damping factor, the increasing factors of the filter bandwidth and the loop gain should be kept the same for maintaining an optimal damping factor. Thus the PLL can have a fast and optimal settling. The real cases are more complicated than this case. The VCO gain is hard to control in the implementation; the fast-switching design can be completed with the increased filter bandwidth and increased phase detector gain. If the divided-by-N factor of the main divider is included, the loop bandwidth of the
PLL is reduced by a factor of square-root of N while the damping factor is increased by the same amount. Therefore this N-factor implementation damages the fast settling behavior of the PLL. The filter bandwidth and loop gain can be increased for the purpose of maintaining the loop bandwidth of the PLL for fast settling. However, the damping factor may be increased because of this increased filter bandwidth (see Equation (4.4), (4.5)). Here three cases of the PLL settling are shown in Figure 4.2.

\[ \omega_n = \sqrt{\frac{\omega_{lp} \cdot K_{pd} \cdot K_{vco}}{N}} \]  
(4.4)

\[ \zeta = \frac{1}{2} \cdot \sqrt{\frac{N \cdot \omega_{lp}}{K_{pd} \cdot K_{vco}}} \]  
(4.5)

The solid line is the settling behavior of the PLL with a 1kHz loop bandwidth, \( N = 1 \), and \( \zeta = 0.707 \). The dashed line is the settling behavior of the PLL with a 4kHz loop bandwidth, \( N = 1 \), and \( \zeta = 0.707 \). In this case, the filter bandwidth and loop gain of the PLL are increased with the same ratios while maintaining the damping factor \( \zeta \). The settling time of the dashed-line case is faster than that of the solid-line. If \( N = 4 \) is considered with 4kHz loop bandwidth, the filter bandwidth and loop gain are increased by a factor of two each. Based on Equations (4.4) and (4.5), the damping factor is increased by a factor of two. The dash-dot line represents this case. When compared with the dashed-line case, the settling time is almost the same. When the settling accuracy is taken into account, the settling time may be different for these two cases. Nonetheless,
from these three cases it has been shown that the loop bandwidth of the PLL seriously impacts the settling time. The larger the loop bandwidth of the PLL is, the faster its settling time is. The unity-gain bandwidth of the loop filter becomes the dominant factor for fast switching design. Comparing the same frequency bandwidth with different damping factors shows that the damping factor definitely impacts the settling time with the same frequency resolution. The example is shown in Figure 4.3.

Figure 4.2: The settling behavior of the PLL with different damping factors/bandwidth
Figure 4.3: The damping behavior of the PLL

As explained in the previous section, when the poles of the PLL are close to the origin the PLL has slow settling time (see Figure 4.4). Here the PLL uses a conventional phase frequency detector. In more advanced PLL or frequency synthesizer design, fast-switching aid circuitry is added for faster acquisition [30]-[32]. The acquisition aid circuitry complicates the analysis of the settling behavior of this kind of PLL because its stability must also be considered under some circumstances.
Figure 4.4: Normalized pole locations of the different PLL transfer functions
CHAPTER 5

FRACTIONAL-N FREQUENCY SYNTHESIS WITH DELTA SIGMA MODULATOR

Fractional-$N$ frequency synthesis has been used in telecommunication systems in the last decade. Fractional-$N$ frequency synthesis techniques allow very narrow channel spacing relative to the output frequency, large bandwidth in the PLL relative to the channel spacing, and high output frequency relative to the processing technology used in the IC. Consequently, the availability of a low noise, low spurious-frequency form of fractional-$N$ division has had a significant impact on the performance of the low cost frequency synthesizers used in consumer products.

In a fractional-$N$ frequency synthesizer, the output frequency can vary by a fraction of the input reference frequency. By using fractional-$N$ division, the wider loop bandwidth for a given channel spacing allows faster settling time and reduces the phase noise requirements imposed on the VCO [18], [21], [22], [30]. Pulse swallowing, phase interpolation, Wheatley random jittering and Delta-Sigma modulation are several techniques implemented to achieve fractional-$N$ division [64].
Each technique has its advantages and disadvantages. Pulse swallowing is prone to spurious frequencies. Phase interpolation requires precision analog components, such as a DAC and delay converter. Wheatley random jittering introduces broadband noise to the main divider output. More digital accumulators are necessary for Delta-Sigma modulation, which depends on the order of the modulator. Considering the performance of the techniques, Delta-Sigma modulation technique is not prone to spurious frequencies, has no precise analog components required and does not introduce broadband noise into the divider output. Although the complexity of the hardware is higher than other techniques, today’s IC process technology helps to reduce the hardware size of the modulator by shrinking the transistor size and increasing transistor density. In this work, fractional-$N$ frequency synthesis with Delta-Sigma modulation is chosen for radio frequency communication applications.

![Delta-Sigma modulator](image)

Figure 5.1: Delta-Sigma modulator
5.1 Delta-Sigma Modulator

Before going to fractional-\(N\) frequency synthesis, Delta-Sigma modulation [63] is introduced so as to provide a clear picture of both its advantage over other techniques, and its performance impact.

The general Delta-Sigma modulator is shown in Figure 5.1. The advantage of a Delta-Sigma modulator is that noise shaping can obtain low baseband noise for high resolution [65]-[67]. Recently, this oversampling technique has been applied to high-speed applications [69]-[72]. The input signal \(U(n)\) is subtracted with the feedback sampled signal, integrated, and sampled by the quantizer to the output. The quantization noise, \(e(n)\), is shaped by the feedback loop. The simple equations are expressed as following.

\[
STF(z) = \frac{Y(z)}{U(z)} = \frac{H(z)}{1 + H(z)} \tag{5.1}
\]

\[
NTF(z) = \frac{Y(z)}{e(z)} = \frac{1}{1 + H(z)} \tag{5.2}
\]

Here STF means signal transfer function and NTF is noise transfer function. \(H(z)\) is the loop filter. Note that the zeros of the noise transfer function are the poles of the loop filter. In other words, when the \(H(z)\) approaches infinity, the noise transfer function goes to zero. This indicates that the baseband noise is shaped as a high-pass characteristic.
The signal transfer function has unity gain with infinity $H(z)$; therefore, the identical input signal can be recovered at the modulator output. The output $Y(z)$ of the modulator is easily expressed as,

$$Y(z) = STF(z) \cdot U(z) + NTF(z) \cdot e(z)$$  

(5.3)

The identical signal appears at the output with unity gain $STF(z)$ and the quantization noise is shaped by a high-pass noise transfer function. A low-pass filter can be applied to eliminate the high frequency components in the output spectrum. The application of Delta-Sigma data conversion is for very high-resolution application with low frequency band. Simply speaking, the higher order the loop filter is, the higher the signal-to-noise ratio (SNR) is. On the other hand, the stability of the modulator is a challenge in the design [63], [73], [74].

Delta-Sigma data conversion has been widely used in many audio and communication systems, and can be applied to analog-to-digital or digital-to-analog conversion. Two common architectures are single-loop multi-feedback and multi-stage-noise-shaping (MASH). Using high-order single-loop multi-feedback makes it difficult to control the stability of the modulator. The loop filter is difficult to design because of the sensitivity of the coefficients. Also the stability is signal dependent; maximum signal input range within the reference voltage is restricted to ensure the stability. Single-loop architecture is less prone to idling tones. These idling tones may seriously affect SNR and are difficult to eliminate in applications.

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MASH architecture has advantage of the stability with high SNR [75]; the maximum input range is almost equal to full range of 1’s densities. Perfect coefficient matching is required between analog and digital differentiator in ADC design. Imperfect matching may result in the leakage of noise and tones into the baseband. MASH architecture is an optimal candidate for digital modulator design since perfect matching can be implemented by using digital circuit operation. With multi-bit digital quantization, the digital modulator can achieve very high resolution with negligible baseband noise. Therefore, MASH digital modulator is chosen for fractional-N control in the fractional-N frequency synthesizer. Figure 5.2 is the spectrum example of a 4th-order digital modulator with dc input. Obviously, the low frequency noise level is very low and a low-pass filter
can be applied after the digital modulator to remove most of the high frequency noise and tones. A similar operation is applied to the fractional-$N$ frequency synthesizer. This will be explained in the later section.

The digital modulator implementation is implemented with CMOS transistors, which has been addressed in many literatures [63], [76], [77]. The digital synthesis tools can be used with the built-in digital cell library for this purpose.

### 5.2 The Operation of Fractional-$N$ Frequency Synthesizer

The earliest concept of the fractional-$N$ frequency synthesizer was based on the pulse remover [34]. Modern implementation of this fractional-$N$ architecture operates on a different principle. Figure 5.3 is the fractional-$N$ frequency synthesizer using a dual modulus divider. In the later circuit design of the main divider, the same concept is used.

![Figure 5.3: Fractional-$N$ frequency synthesizer using dual-modulus divider](image)
If the prescaler divides by \(N\) for \(A\) pulses of VCO and by \(N+1\) for \(B\) pulses, then the equivalent divide ratio is \((A+B)/(A/N+B/(N+1))\). The divide ratio can be varied between \(N\) and \(N+1\) in fine steps by choosing proper \(A\) and \(B\). Compared with integer-\(N\) frequency synthesis, the reference clock frequency is not limited by the smallest frequency step. With reference clock frequency in the range of tens of megahertz, the loop bandwidth of a fractional-\(N\) synthesizer can be as high as a few hundred kilohertz, yielding a fast-lock transient as well as suppressing the VCO close-in phase noise. The small division ratio lowers the reference and phase detector phase noise. The fractional-\(N\) synthesizer suffers from the fractional spurs, because the phase difference between the reference and feedback signal will grow every period of the reference clock frequency until it returns to zero when the divide-by-\(B\) operation occurs. Thus the phase detector produces progressively wider pulses that create the ramp waveform at the output of the LPF. From the frequency domain view, if the VCO output is equal to \((N+f)\)\(f_{\text{ref}}\), \(N\) is the integer number, \(f\) is the fractional number and \(f_{\text{ref}}\) is the reference clock frequency. The output of the LPF is a repetitive ramp waveform with a period of \(1/(f_{\text{ref}})\). Such a waveform would modulate the VCO and generate the sidebands at the multi \(f_{\text{ref}}\) frequencies with respect to the carrier frequency [78].

Fractional spurs are an important consideration in the design of the fractional-\(N\) frequency synthesizer with a dual-modulus divider. An efficient method is to randomize the choice of the modulus such that the average division number is still given by \(N+f\). The most efficient approach is Delta-Sigma modulation for randomization of the fractional spurs. By this approach, randomized white noise of close-in frequency is
shaped into the high frequency offsets and the loop filter of the PLL attenuates their noise energy. Therefore, Delta-Sigma randomization effectively helps to convert the fractional spurs into very small white noise. As shown in Figure 5.3, a Delta-Sigma modulator controls the dual modulus for randomization. In Razavi [47], a simple spectrum analysis of the Delta-Sigma fractional-N technique shows an interesting phenomenon. Assume that $Q(f)$ is the quantization noise in the frequency domain, the power spectral density is expressed as:

$$S_{nf}(f) = \frac{f_{\text{out}}^2}{(N + f)^2} \cdot \frac{|Q(f)|^2}{N^2}$$  \hspace{1cm} (5.4)

$S_{nf}(f)$ is the quantization noise at the output of the main divider, and $f_{\text{out}}$ is the VCO frequency. The VCO noise is attenuated by a factor of the division number, so is the quantization noise. In fact, the quantization noise of the Delta-Sigma modulator is too small to pollute the phase noise. How serious is the impact of the idling tones in the Delta-Sigma modulation? In certain architectures, idling tones are inherent in Delta-Sigma modulation [63]. It is difficult to eliminate those tones completely. Idling tones can be seen as a part of the quantization noise. According to Equation (5.4), idling tones are also attenuated by a factor of N at power of 2. Usually, the idling tones at the baseband are not a threat for the fractional-N synthesizer due to their negligible level.

With the Delta-Sigma fractional-N frequency synthesis, insufficient attenuation of the out-band frequency may result in the residue of the quantization noise at high frequency offsets. As a rule of thumb, the loop filter is always designed one order higher.
than the order of the modulator. This is somewhat impractical for many applications because of the instability of high-order PLL design.

The description of integer/fractional-\(N\) PLL in frequency domain is shown in Figure 5.4. It is easy to see the step size of the fractional-\(N\) PLL that is smaller than that of the integer-\(N\) PLL. This reduces the factor of \(N\)-division for better phase noise suppression. The fractional-\(N\) frequency synthesis with Delta-Sigma modulation not only is used in normal frequency synthesis for LO, but also can be used for built-in GMSK/GFSK pulse shaping of data transmission [22], [21]. In this work, straight fractional-\(N\) frequency synthesis with Delta-Sigma modulation is implemented.

Figure 5.4: The frequency discrepancy of integer/fractional-\(N\) synthesizer
CHAPTER 6

FREQUENCY DIVIDERS

The operating frequency of the frequency synthesizer is totally dependent on the function of the main divider. The main divider and reference divider also contribute to the phase noise of the frequency synthesizer. The noise of the dividers needs to be as low as possible to avoid amplification from the high division ratio of the main divider (see Equation (3.1)). A SiGe BiCMOS process is used for this design. The strength of bipolar transistor and current mode logic (CML) topology is emphasized for this high frequency and low noise application. A much lower frequency operation is usually required in the reference divider, which is designed on the basis of CMOS logic due to its static, low stand-by power consumption.

6.1 Basic Digital Cells of the Radio Frequency Divider

Two popular contemporary bipolar digital logic families are transistor-to-transistor logic (TTL) and emitter-coupling logic (ECL). ECL/CML is the fastest digital technology available. High speed is achieved by operating all transistors in their active
region, thus avoiding storage time delays. CML keeps the logic signal swing relatively small, reducing the time required to charge and discharge the various loads and parasitic capacitances. In addition to its high speed, its fully differential logic topology is relatively immune to common-mode noise, particularly from the power supply and ground.

The followings are several basic CML designs for the main divider. A simple introduction is made of its operation and function. In the divider design, the most commonly used digital cells are latches and AND/NAND gates, XOR gates, etc. Figure 6.1 is a latch in CML topology.

![Figure 6.1: Bipolar ECL latch](image)

Figure 6.1: Bipolar ECL latch
During the track phase, the differential pair consisting of Q1 and Q2 is enabled and operates as a differential amplifier. When the latch mode is enabled, the current generated by the current source is diverted to the differential pair consisting of Q3 and Q4. The outputs of the differential pair, Q3 and Q4, are connected to the high impedance output nodes in a cross-coupled manner resulting in positive feedback. When positive feedback is enabled, the initially small differential voltage is amplified to a certain logic range. Usually, the logic voltage swing is around 200mV to 400mV with a low voltage supply. The input impedance of differential pair Q3 and Q4 may be lower than the output impedance of the differential pair Q1 and Q2 due to the base-emitter capacitance. An intermediate buffer stage can be added to drive the low impedance node and various load capacitances. In this design, low impedance is preferred in the signal path for very high-speed operation. The loading resistor is designed to allow for enough signal swing and for proper impedance. Also the load from the next circuit stage is almost consistent with a certain type of digital logic. The intermediate buffer stage adds a substantial amount to the power consumption of each latch. The latch circuit is the most populous component in the divider design.

A AND/NAND gate is shown in Figure 6.2. The function is performed with the transient change of the inputs. Basically this circuit topology operates as an AND function. When both inputs of h and l are high logic level, current is diverted to transistors of Q1 and Q3. It makes the output Q as high logic and Qb as low logic. When one of the inputs is low logic level, the current of the current source is routed through either the transistors Q2 and Q3 or the transistor Q4 only. The low logic level occurs at the output Q. When both inputs are low logic level, the current of the current source is
directed only to the transistor Q4. The low logic level appears at the output Q. Thus this circuit performs an AND function. NAND functionality is easily obtained by swapping the outputs of Q and Qb.

Another CML gate is the XOR/XNOR function. The circuit topology is very simply an analog multiplier form (XOR function), and can easily be used for the phase detector [79]. By swapping the outputs the counterpart logic function, XNOR, is obtained. The CML topology of digital cells introduced here can operate normally with a minimum 2.5 Volt power supply. For lower power supply application, Razavi, Ota, and Schwartz [80] is suggested for design guide.

Figure 6.2: Bipolar ECL NAND/AND gate
6.2 RF Divider

The main divider is the first component connected to VCO output. Its function is to divide the VCO frequency down to the comparable frequency of the reference clock. Depending on the application, the division ratio should be wide enough to cover the frequency range. The most commonly used divider architecture is a pulse swallow divider with dual modulus prescaler or its extensions [47], [81]-[84]. Many different dividers have been introduced for the same purpose in a number of works [18], [85], [86]. The divider architecture proposed by Vaucher et. al. is used in this design [86]. Its simple and straightforward implementation and wide division range are suitable for this application.

The performance of the main divider is mostly dependent on the prescaler design. The prescaler design should be simple and straightforward with low noise and low power consumption during radio frequency operation. The most common implementation is a cascading divided-by-2 divider to reduce the VCO frequency, paired with a synchronized counter for the remaining division. If the VCO output frequency is too high to offer low enough frequency operation for the synchronized counter, the prescaler needs to be designed with a more efficient method. Here Vaucher et. al. [86] provides a candidate for a modular programmable prescaler. The implementation in it gives a wide integer division range with minimum divider cells. The architecture of the multi-modulus divider is shown in Figure 6.3. The modular structure consists of a chain of divide-by-2/3 divider cells connected like a ripple counter [87]. This structure is characterized by the absence of long delay loops, as feedback lines are only present between adjacent cells. This local
feedback enables simple optimization of the power dissipation. Another advantage is that the topology of the individual divide-by-2/3 divider cells is the same, therefore facilitating layout work. If the strobe nodes of each cell share a common strobe signal [88], then high power consumption results due to the high requirements on the slope of the strobe signal, which is in combination with the high load presented by all cell in parallel.

The prescaler operates as follows: Assume that the node of mod\(_n\) is enabled all the time. Once in a period of one division, the last cell on the chain generates the signal mod\(_{n-1}\). This signal propagates “enable” through the chain, which is re-clocked by each cell along the way. Provided that the programmable inputs \( p \) are set to 1, an active mod signal enables the cell divided by 3 in one division cycle. Hence, a chain of \( n \) divided-by-2/3 cells provides an output signal with a division number of

\[
\frac{f_{\text{out}}}{f_{\text{in}}} = \frac{1}{p_0 + 2 \cdot p_1 + 2^2 \cdot p_2 + \cdots + 2^{n-2} \cdot p_{n-2} + 2^{n-1} \cdot p_{n-1} + 2^n}
\]

(6.1)

![Diagram](image-url)

Figure 6.3: Programmable prescaler
Equation (6.1) shows that all integer division ratios range from $2^n$ (if all $p_n = 0$) to $p_0 + p_1 \cdot 2 + p_2 \cdot 2^2 + \cdots + p_{n-1} \cdot 2^{n-1} + 2^n$ (if all $p_n = 1$). The extension of the division ratio on the main divider can be obtained by combination with a synchronized counter.

The realization of the divide-by-2/3 cells is depicted in Figure 6.4. The cell is composed of two functional blocks. The prescaler logic divides the input frequency $f_{in}$ either by 2 or by 3, and is controlled by the end-of-cycle logic. The output frequency $f_o$ is connected to the next cell of the prescaler chain. The end-of-cycle logic determines the momentaneous division ratio of the cell, based on the state of the modin and $p$ signals. The modin signal becomes active once in a division cycle. At that moment, the state of the $p$ input is checked. If $p$ equals one, the end-of-cycle logic forces the prescaler to swallow one extra period of the input signal. The cell divides by 3. If $p$ equals zero, then the cell stays in division by 2 mode. The end-of-cycle logic re-clocks the modin signal of the proceeding cell in the prescaler chain.

The circuit implementation of the divide-by-2/3 cells is based on the digital cells presented in section 6.1. Unlike CMOS rail-to-rail logic operation, Bipolar CML has a limitation on the low voltage operation. Three stacked bipolar transistors with loading and biasing resistors can have a minimum 2.5 Volt power supply operation, and all transistors should be within the active region in normal operating mode. Therefore, AND logic is not combined with latch circuitry to maintain a low power supply. The biasing network is comprised of two devices, one bipolar transistor on top of the biasing resistor.
The base of the bipolar transistor is connected to inverse PTAT that provides inverse bias voltage with temperature variation. The biasing resistors are scaled with the different operating ranges of the divide-by-2/3 cells for high-speed performance and low current consumption.

The main divider is comprised of two blocks, prescaler and counter, to extend the division ratio (see Figure 6.5) [31]. The prescaler has an asynchronous clock for each divide-by-2/3 cells to facilitate high-speed operation and power saving. After the VCO frequency is divided to a certain frequency range, the synchronized counter can be easily used for extension of the divide number. Although the power consumption of synchronized counter is high due to the loading in each clock cycle, the timing jitter/phase noise can be reduced by synchronized clock operation of the counter.

Figure 6.4: The divided-by2/3 cell of the prescaler chain
The VCO frequency inputs into the prescaler, and the prescaler output, $p_o$, acts as the clock of the counter. Counter output toggles the prescaler through the mod$_{in}$ signal enabling the divide number of the prescaler within a period cycle of prescaler output signal. The final output frequency of the main divider is $F_q$. The last mod$_0$ signal triggers a trigger flip-flop to send this divided signal for phase/frequency comparison. The total division number is programmed with a string of bits composed of an MSB of k-bit control and an LSB of m-bit control. The total number of division bits is $m+k$. For example, a main divider composed of a 4-bit programmable prescaler and a 6-bit counter has total 10-bit programmable range. The MSB of total division bits is the MSB of the 6-bit string on the counter; the LSB of total division bits is the LSB of the 4-bit string on the prescaler. The duty cycle of the final divided signal is the timing of the input frequency divided-by-$2^4$. The total decimal number of the main divider can be expressed.
as the following equation: \( N = 2^{n_{pr}+1} + 2^{k+m} + 2^{k+m-1} + 2^{k+m-2} + \ldots + 2^1 + 1 \). The offset \( 2^{n_{pr}+1} \) comes from the inherent division of the prescaler and counter; \( n_{pr} \) means the stages of the prescaler.

The circuit simulation results of the prescaler are shown in Figures 6.6 and 6.7. The simulation results agree with the expected theory. Each divider cell receives a mod\( _{in} \) signal and gives a mod\( _o \) signal with a clock delay of the previous output signal. The final output signal \( f_o \) maintains the duty cycle of the input signal \( f_{in} \). The simulation results of the main divider are shown in Figure 6.8 and 6.9. The counter toggles the mod\( _a \) lines and the prescaler releases two narrow pulses at the final output \( f_o \).

The circuit implementation is based on fully differential topology. This reduces the common mode noise disturbance from the power supply line and substrate coupling. Several emitter follower buffers are used on the critical nodes of the main divider to provide sufficient driving current to the next CML circuits.
Figure 6.6: Divided-by-17 transient states of the prescaler with 4 stage dividers
Figure 6.7: Divided-by-21 transient states of the prescaler with 4 stage dividers
Figure 6.8: Divided-by-50 transient states of the main divider
Figure 6.9: Divided-by-50 transient states of the prescaler
6.3 RF Input Buffer Amplifier

The RF input buffer has three purposes. The first is to match impedance from the VCO output to the main divider. The second is to provide gain to compensate for the losses of impedance matching. The third is to provide sufficient driving capability for the divider logic. The adopted topology is shown in Figure 6.10. Basically, this is a two-stage composed of a unity gain buffer and a gain stage. This two-stage amplifier has only open loop characteristics without any compensation, unlike some multi-stage amplifiers [89], so the stability of this buffer amplifier is not an issue for this application. Usually, the feedback factor may result in instability in high frequency design, especially with small parasitic effects. The simple solution is adopted to prevent this difficulty of the design in radio frequency application.

![Figure 6.10: RF buffer amplifier](image)

Figure 6.10: RF buffer amplifier
6.3.1 Impedance Matching

The function of the first-stage buffer is to provide impedance matching. In high frequency operation, several methods have been offered for impedance matching [90], including shunt and series feedback networks, and on-chip passive devices. For the simplicity of design, an on-chip inductor is not considered because of its adverse quality control effects and die size. So resistors and capacitors are the candidates. An active device BJT is chosen for the input buffer because of its high frequency/low noise performance.

Figure 6.11(a) is a BJT emitter follower topology. Figure 6.11(b) is the small-signal model of the emitter follower. The input impedance of the emitter follower can be expressed as follow;

Figure 6.11: Emitter follower (a) circuit and (b) small-signal model
\[ Z_{in} = r_\pi + R_L \cdot (1 + \beta) \]  \hfill (6.2)

Where \( \beta \) is the current gain of the BJT and \( R_L \) is the load resistance, including the output resistance of the current source transistor. The capacitances of the BJT are not included, provided that they have negligible impact on the performance. The BJT operates in the active region, so the output resistance of the BJT is much higher than the input resistance of \( r_\pi \). The load resistance or the input resistance of the next stage dominates \( R_L \). Therefore, the input impedance of the emitter follower is enhanced by the emitter degenerated resistance through the current gain of the BJT. The input impedance of the emitter follower can be designed to be high enough.

The feedback network design for impedance matching will be examined. Shunt and series feedback network are proposed for impedance matching (Figure 6.12). The emitter degenerated resistor boosts the input impedance of the emitter follower. Based on Equation (6.2), the input impedance of the emitter follower varies with the process corners. In high input impedance case, variations from the process may not be very important to performance. If the required input impedance is low enough, then process variation may impact the performance significantly. \( r_\pi \) usually varies from around 10k to 30k ohms. A certain amount of resistances from the transistor geometry limits very low input impedance available.
Another method to use shunt feedback resistance between the base and the collector of the BJT is shown in Figure 6.12(b). While similar to Figure 6.11(b), the small signal model of Figure 6.12(b) includes a resistor between the signal input and ac ground. This indicates that the shunt resistance affects the input impedance by paralleling Equation (6.2). If the topology of the emitter follower in Figure 6.12(b) is adopted, the shunt resistance dominates the total input impedance of the emitter follower. The input impedance equation is displayed as:

\[ Z_{in} = R_f \parallel [r_n + R_L \cdot (1 + \beta)] \]  \hspace{1cm} (6.3)
For example, the input impedance of the RF buffer amplifier requires 100 ohms. In circuit implementation, the second term of Equation (6.3) is as high as several tens to hundreds ohms. If a 100 ohms $R_f$ is given in Equation (6.3), then $R_f$ is the only term to control the input impedance of the emitter follower. Usually, the input impedance requirement for the RF application is low to several tens ohms. The shunt-feedback matching network is adopted in this design to minimize the process variation in the input impedance. Of course, the variation of the passive device in the process may be up to ±20%. This issue will be used in the layout consideration.

The other issue for the impedance matching of the emitter follower is the package and bonding wire. Looking at components up to the BJT input base, the impedance transfers through pad capacitances, bonding wire, and then package pins. This is well modeled in the simulation to reduce their nonlinear effect in silicon implementation. In Figure 6.13, $C_p$ and $C_{pad}$ are the parasitic capacitances of the transistor base and pad; $R_t$ is the resistance of the metal wire, and $L_b$ is the bonding wire inductance.

![Figure 6.13: Simplified input impedance diagram](image-url)

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The simulated input impedance of the emitter follower is shown in Figure 6.14. The input impedance decreases with an increase of the operating frequency. In ideal impedance, matching the image part of the input impedance should be zero because the inductance and capacitance cancel each other. Simulation shows the non-ideal parasitic capacitance is not serious enough to destroy the input impedance. The variation of the input impedance goes from 99 ohms down to 89 ohms over the entire operating frequency range. The input impedance is easily designed through exchange of the resistor $R_f$. The resistor size can be changed from 100 ohm to 1k ohm for different specifications.

![Figure 6.14: Input impedance simulation](image-url)
6.3.2 Gain Stage and Output Buffer

The gain stage is composed of a gain stage and an output buffer. The intermediate gain stage not only provides sufficient gain to compensate the loss from non-ideal impedance matching, but also amplifies the input VCO signal to drive the CML circuits.

The gain stage is in fact a differential pair as seen in Figure 6.15. The differential pair is chosen for its high-speed performance. If the cascode gain stage is used, a parasitic pole results from the parasitic capacitance of the emitter of the cascode BJT. This moves 3dB frequency down and drops the gain. On the other hand, the cascode transistor physically limits the voltage swing on the internal nodes, especially with low voltage power supplies. Usually, a 200mV to 400mV peak-to-peak swing is necessary to drive CML circuits, a differential pair with a larger bias current is chosen for this gain stage.

![Figure 6.15: The intermediate gain stage](image-url)
The emitter follower topology is used in the output buffer stage design. In addition, to providing sufficient driving capability, the tail current of the second buffer stage is made larger to ensure a fast charge and discharge of the bases of the subsequent CML circuits for high-speed operation. This output emitter follower also provides the common-mode voltage level shifting. The ac and transient simulations are shown in Figure 6.16 and 6.17 for the entire RF buffer amplifier frequency range.

Figure 6.16: Frequency response of the RF buffer amplifier
6.4 Reference Divider

The reference divider is placed in front of the phase detector and the main divider. The reference divider provides the programmable division for the reference clock of the phase detector, which gives the adjustable advantage in the PLL design. On the other hand, the noise in the reference divider is amplified by the PLL and may become the dominant part of the close-in phase noise. The phase noise of this reference divider has to be considered carefully. Most of the reference dividers are designed with CMOS technology for low power consumption. The problem with CMOS transistors is that they
have higher noise performance than CML because of their low transcondutance. The single-input/output operation is difficult in giving a good performance on common mode noise immunity.

In this design, the programmable reference divider is based on the synchronized counter topology. The synchronized clock reduces the timing jitter in the reference divider. The variation of the process and temperatures can easily create very slight timing shift between digital cells, which will cause jitter at the output of the counter. Such timing jitter can raise the phase noise of the reference divider. The jitter translates to the frequency domain and becomes the part of the flicker noise. The impact of such phase noise will be analyzed in a later chapter. The simplified diagram of the reference divider is shown in Figure 6.18. Q is the output of the divider; div is an M-bit control word equal to the divide number and ck is the synchronized clock. Dash-line block can be cascaded for extension of the divide number.

![Simplified diagram of the reference divider](image_url)

**Figure 6.18 Simplified diagram of the reference divider**
CHAPTER 7

PHASE FREQUENCY DETECTOR/CHARGE PUMP

The function of the phase frequency detector is to compare the reference frequency with the divided VCO frequency and identify lead and lag of the phase for the charge pump. The charge pump follows the up and down pulses from the phase frequency detector to charge and discharge the loop filter with a constant current. Through the charge and discharge of the loop filter, the tuning voltage of the VCO adjusts the VCO output frequency. The target frequency is locked by the entire loop until the charge pump current does not change the tuning voltage of the VCO. Many parameters, including tracking range, acquisition range, loop gain and transient response depend on the properties of the phase frequency detector employed in the phase-locked loop.

7.1 Phase Frequency Detector

Several different phase frequency detectors have been used in phase-locked loop design, Gilbert cell multipliers, edge-trigger R-S latches, or edge-triggered, resettable D flip-flops. In this application, only Gilbert cell and edge triggered, resettable D flip-flops
are discussed. Before going into the detailed circuit design, typical phase/frequency acquisition is explained below.

Figure 7.1 shows the operation of the typical phase frequency detector. If the frequency of the reference signal (REF) is different than the divided VCO signal (DIV), the phase frequency detector releases pulses to either accelerate or attenuate the frequency operation of the VCO. In Figure 7.1(a), the frequency of reference signal is faster than the frequency of the divided VCO signal, thus the phase frequency detector produces the output pulses at \(Q_a\) and \(Q_b\) stays at the logical zero at all times. When the phase of the reference signal leads the phase of the divided VCO signal, the phase frequency detector gives an up signal at \(Q_a\). When the phase of the reference signal lags the phase of the phase of the divided VCO signal, the phase frequency detector gives a down signal at \(Q_b\) (see Figure 7.1(b)). If the phase of the reference is equal to the phase of the divided VCO signal, the very narrow up and down signals of the phase frequency detector drive the charge pump simultaneously and a high impedance state appears at the input of the loop filter due to the sink and source current equivalence of the charge pump. This is the typical phase/frequency comparison operation used in modern PLL design. This type of the phase frequency detection with the charge pump is called “3-state phase detection” — logic 0, 1 and high impedance. In practicality, the charge pump may leak during the high impedance mode due to the mismatch of the sink and source transistors. This causes the reference sideband spurs in the output spectrum.
In a phase detector with a Bipolar Gilbert cell [79], the function of the Gilbert cell is the same as an XOR gate. All transistors of the Gilbert cell operate in the active region with a phase tracking range from 0 degree to 180 degrees. The average output is
dependent on the duty cycle of the inputs; this effect manifests itself as a static phase error of the PLL. A PLL employing such a phase detector exhibits amplitude-dependent static and dynamic behavior. If the input frequencies of the Gilbert cell phase detector are different, the average output is zero, which means that the Gilbert cell cannot be used as a frequency detector. So an extra frequency detector/frequency locking aid is necessary for the PLL with a Gilbert-cell phase detector. The advantage of using the XOR function for phase detection is to reduce the rising/falling edge disturbance of the power supply, subtract coupling noise, and to eliminate the dead zone of the phase detector due to the delay of the digital logic gates.

From a noise analysis of the phase frequency detector, Bipolar and CMOS technology have entirely different noise performances. Usually, a bipolar phase frequency detector has low noise. This reduces the contribution of the phase noise from phase detector in the entire PLL. Contrarily, CMOS phase frequency detector has poor noise performance. This may impact a low phase noise PLL design significantly as explained in phase noise analysis.

From a power consumption perspective of the phase frequency detector, a CMOS implementation has very low static dc current consumption and a low power supply voltage. CMOS gates need a rail-to-rail swing to operate, whose transient time must be as short as possible for noise performance. This means that sharp rising and falling edges are necessary with large aspect ratios of the transistor gates.

To simplify the phase noise solution in this design, bipolar transistors are used for the phase detector. The minimum supply voltage is 2.5V with stacked bipolar digital technology. The single-loop/dual-loop adoption of PLL is discussed for further analysis.
The difference between single-loop and dual-loop implementation is in the combination of the phase detector and frequency detector. In single-loop implementation, the phase detector and frequency detector are combined so as to have identical charge and discharge currents for the loop filter. In frequency acquisition mode the locking speed is based on the update capability of the phase frequency detector. If very fast locking is requested, extra fast acquisition circuitry is needed. The dead zone can be resolved by fine design in the phase frequency detector [20], [33]. However the single-loop implementation is the most general topology for PLL design.

In dual-loop implementations [31], [32], [91], [92], the phase detector and the frequency detector are separated. In this case, the PLL may have two different settling behaviors during frequency acquisition and phase acquisition modes. The locking speed may be improved in the frequency acquisition period by using a larger charge/discharge current. The phase of the loop must be sufficient to maintain the loop stability during the frequency acquisition period with large current, otherwise the loop will never lock during the acquisition. This definitely complicates the PLL system design.

The advantage of the dual-loop implementation is described and analyzed by Hill and Cantoni [91], [92]. This kind of the phase-locked loop is called a “Steered Frequency Phase Locked Loop (SFPLL)”. There are three key advantages of the SFPLL. The output frequency is the input reference frequency (or very close to input reference frequency) when no frequency residue appeared (Assume unity feedback in this case). The range of the frequencies to which the SFPLL can lock is confined to a small and controllable region around the input reference frequency. And finally the VCO phase noise can be
reduced and the loop bandwidth is made less dependent on the block parameters for a particular class of the SFPLL.

On the basis of Hill and Cantoni's analysis [91], [92], when the phase detector output equals zero the SFPLL always tracks the reference frequency. Also, due to the finite phase error appearing at the output of the phase detector, the SFPLL can lock into a restricted frequency range. The extent of the range is well determined by the ratio of the phase detector gain and frequency detector gain. In theory, provided that the reference source is free from the phase noise, the type II SFPLL is used to achieve the desired loop bandwidth and reduce the phase error due to the VCO noise to an insignificant level. In summary, the VCO of the PLL usually needs to have a very accurate free running frequency and have a very low phase noise; the SFPLL can achieve the same performance independent of the quality of the VCO.

Several dual-loop PLLs have been proposed and implemented [31], [32]. Experimentally, they achieved better locking time than that of the single-loop PLL. A dead zone is simply created by the frequency detector when the PLL loop is transitioning to lock mode. Figure 7.2 shows the operation principle of the dual-loop PLL (SFPLL). The dual-loop is built with two separated paths, PD/CP1 and FD/CP2. The phase detector (PD) is dimensioned for in-lock operation, which operates at all times. The frequency detector (FD) is dimensioned for the fast/wide-locking operation, which is only activated during VCO tuning actions. PD and FD can be built with the same PFD topology instead of two different circuitries. In Figure 7.2, a dead zone is established for the fine-settling acquisition mode. The PLL will request two step acquisitions before the loop will be locked. In the fast frequency acquisition mode, both PD and FD are on at the same time.
The second charge pump (CP2) gives a large charge/discharge current for the loop filter. At this moment, the PLL has a much larger loop bandwidth and less phase margin that may drive it into instability. After the reaching in-phase range of the PD, the built-in dead zone of the FD is activated by internal circuitry. The PD takes over the final settling with locked condition of the PLL. Therefore, a dual-loop PLL has capability to achieve much faster locking compared to the single-loop PLL. The dead zone also allows a smooth transition after the frequency acquisition to avoid the glitch effects, so that sudden disturbances of the VCO tuning voltage are avoided.

Vaucher [31] and Yang and Liu [32] have implemented an adaptive PLL for fast acquisition. Both of them have applied the above principal but with a slight circuitry difference. Both of the implementations encounter the finite output impedance of the PD charge pump that may shift the phase error origin to both positive and negative sides. This simply raises asymmetrical settling for PLL. Of course, this asymmetrical settling does not have such a significant impact in the spectral purity. Ideally, if the up and down signals of FD match, then the charge pump releases the same amount of the current charging and discharging the loop filter. The up and down signals of FD have very different behaviors because of the phase error of PLL. The asymmetrical settling also results from the mismatch between the gates of two up and down paths in the FD. In Figure 7.2, the slipping transition of the PD and FD is not shown for simplicity.
If the XOR type phase detector is applied on the phase detector design, then the origin of the phase error $\theta$ is at $\pi/2$ rather than zero. This implies that the dead zone is shifted with the origin of the XOR PD. If the origin of the PD shifts beyond the dead zone of the FD, the PLL will never be locked.
Figure 7.3 shows the locked-in condition of the PD charge pump with the input signals REF and DIV. Ideally, the pumping up and down current should be the same to maintain a balanced tuning voltage for the VCO. The offset of the current may cause the frequency shift of the VCO, but the feedback of the PLL will cancel the offset current by equalizing the up and down energy through the time domain. Compared to the rising/falling edge trigger PD, the offset leakage of the charge pump is less in the XOR case.

In Figure 7.3, the dead zone needs to be created with the overall DIV signal duty cycle. The XOR phase detector starts the in-lock of the PLL, since the rising edges of both REF and DIV signals overlap. The in-lock condition is continuous within the entire
duty cycle of the DIV signal. The unlock condition of the PLL occurs until the duty cycle of the DIV signal is no longer overlapped with the rising edge of the REF signal. This phenomenon defines the dead zone of the FD_dz. Two AND gates are added with a simple frequency detector to create the required dead zone, similar to the ideas presented in Martin et.al. [93] and IBM [98]. One AND gate is connected to the REF signal and the up signal of the frequency detector. The output of this AND gate is the UP signal for the FD_dz. Another AND gate is connected to the inverted DIV signal and down signal of the frequency detector, the output of this second AND gate is the DN signal of the FD_dz. Through the transient states of the FD_dz, it is very easy to understand the dead zone operation.

![Figure 7.4: FD implementation with dead zone](image)

Figure 7.4: FD implementation with dead zone
The phase detector is implemented with bipolar transistors. The balance CML is used for fully differential inputs from the reference and divided VCO signal (see Figure 7.5.) The level shift circuitry is needed for CML signal level transfer. Current mode DACs are used for the programmable charge pump currents.

Figure 7.5: The phase detector
7.2 Charge Pump

The charge pump provides the currents to source or sink the loop filter for the VCO frequency tuning. Having a neutral state, an ideal charge pump combined with a phase frequency detector provides an infinite DC gain with a passive filter. This can result in an unbounded pull-in range for higher order PLLs, if the input range of the VCO is not limited. As long as the phase detector and charge pump are ideal, the static phase error is zero. Static phase error results from the current mismatch. The current mismatch of the charge pump in a PLL generates a phase offset that increases the spurs in the VCO output signal. Also, the phase offset reduces the locking range in wide range PLLs with a dual loop scheme (frequency locking loop and phase locking loop).

In the locked-in mode of a PLL with conventional PFDs, the charge pump sinks and sources loop filter at the same time [47]. In this case, the impedance mismatch of the sink and source transistors generates a current mismatch because of the drain-source voltage variation between the reference current mirror transistor and the output current mirror transistor. The phase offset can be given by

\[ \Phi_e = 2\pi \cdot \frac{\Delta t_{on}}{T_{ref}} \cdot \frac{\Delta i}{I_{cp}} \]  

(7.1)

where \( \Phi_e, \Delta t_{on}, T_{ref}, I_{cp} \) and \( \Delta i \) are the phase offset, the turn on time of the PFD, the reference clock period, the charge pump current and current mismatch of the charge pump, respectively. The amount of the reference spur can be given approximately by
Therefore, the conventional charge pump may have >10% current mismatch with −55 dBc reference spurs [94]. In many communication systems, the reference spurs can be seen as interference if the spurs have strong energy. These spurs will deteriorate the spectral purity of the down/up conversion signals in transceiver chain. Either sizing the charge pump devices or using gain boosting in charge pump can enhance the impedance of the charge pump. Of course, sizing the charge pump devices for the required impedance may not be practical in the silicon implementation. Conventional gain boosting is not particularly compatible with a low voltage supply because of the common-mode voltage swing in error amplifiers.

The attenuation of the reference sideband harmonics is determined by the reference frequency in addition to the loop filter. The filter bandwidth is much less than the reference frequency in the fractional-N case. The reference spurs of fractional-N synthesizer are definitely reduced to an ignorable level for applications. Larger disturbances due to the reference source in the VCO tuning line can be tolerated. The turn-on time of the charge pump current also raise the reference spurs due to the current mismatch in the charge pump. Based on Equation (7.1) and (7.2), this current mismatch results in phase error. The phase error is translated to the reference spurs by the VCO gain through the tuning voltage. The second right-hand-side term indicates the attenuation provided by the dominant pole of the loop filter. The shorter the turn-on time
and the current mismatch of the charge pump are, the less the reference spurs will be. Also, a small VCO gain with a high tuning voltage range brings down the reference spurs. Equation (7.2) is applied with a 3rd-order PLL. 4th-order PLL with one extra pole has better reference spur attenuation by approximately 20dB. The actual case can achieve better with an inward shift of the extra pole.

The charge pump operation is heavily related to the operation of the phase frequency detector. The in-lock mode of the PLL is the performance with the balance of the sink and the source currents at timing difference as shown in Figure 7.3. This is different from the other source/sink magnitude-matched PFD. The advantage of this XOR function is that the PD adjusts the phase offset with timing difference for sink and source energy matching. The current mismatch of the charge pump can be relaxed in this type of design. Also, using bipolar switches instead of CMOS switches has an advantage on the switching time and clock charge injection. CMOS switches need almost rail-to-rail operation to turn on and off. The charge/discharge time of the gate–source capacitance decides the speed of the timing. Compared with bipolar switch, CMOS switch is slower. Additionally, CMOS switch has charge injection problems, unlike the bipolar switch that is always in an active region. The charge injection of CMOS switches gives the reference spurs as previously explained [47].

Figure 7.6 shows the charge pump implementation. Actually, it is a simple current mirror. The phase detector with bipolar switches controls the switching of the charge pump; the charge injection problem has been eliminated.
Figure 7.6: The charge pump

Other issues need to be considered in this charge pump. First, the charge pump is implemented with BiCMOS technology. The base current may raise the current mismatch at the charge pump output. Usually, using another bipolar transistor between the base and collector of the transistor Q1 can reduce the base current leakage [79]. The additional bipolar transistor helps to create a square current gain factor for minimization of the current mismatch between reference and output transistors. The problem encountered here is the two-staked bipolar transistor limits the current matching accuracy when the VCO tuning voltage is in the lower rail of supply voltage. This will easily raise a large
current mismatch at the charge pump output. Since bipolar transistor needs 0.5V at the collector-emitter for sufficient active-region operation, NMOS has lower drain-source voltage for saturation operation. The size of an NMOS current mirror for large charge pump current may be enormous, so npn-bipolar current mirror is adopted with non 1-to-1-ratio scale to compensate for the base current leakage. Pnp-bipolar transistors are not available in this SiGe process.

Second, any current mismatch in the high impedance mode (see Figure 7.3) becomes dc offset at the charge pump output. This may cost a very small phase shift in the VCO tuning, but not enough to cause a very significant impact in the design. Cascoded PMOS transistors can be added as in Figure 7.6 (dashed-line transistors) for impedance enhancement.

In the dual-loop scheme of the PLL, the FD is always shut down after the PD tracks the phase close enough to the in-lock. The charge pump of the FD is not necessary for very good accuracy in frequency steer mode. The charge pump/PFD current can be programmable with current mode DACs.
CHAPTER 8

PROTOTYPE EXPERIMENTS

8.1 Low-Power Handset Synthesizer

The first silicon prototype of two frequency synthesizers has been implemented with a SiGe 0.5μm BiCMOS process. In this BiCMOS process, 5 metal layers are available, especially a thick, top analog metal layer for RF design. Npn-bipolar transistors have a 40-60GHz $f_t$ with low noise. CMOS transistors have a 0.5μm minimum length.

The first prototype frequency synthesizer is applied to a mobile digital communication system. The signal-to-noise ratio of the down/up conversion signal is very sensitive to the phase noise of the synthesizer. LO phase noise mixes with strong interference coming from other bands. The skirt of the LO may causes a deterioration of desired signal in bit error rate (BER) increase. Another consideration in the LO are spurs at the output of the synthesizer. Those spurs mix with the desired signal into the wanted frequency and easily damage the linearity requirement. How to design the proper phase noise and spurs characteristics of the fractional-$N$ frequency synthesizer for LO is based on the above two considerations.
To see the strengths of the fractional-$N$ frequency synthesizer, let's return to the integer-$N$ frequency synthesizer. The limitations of the integer-$N$ frequency synthesizer are low loop bandwidth and a low reference clock as well as channel spacing. The loop filter is relied on to attenuate the reference spur and its harmonics. If the loop filter bandwidth of the frequency synthesizer is very close to the reference clock frequency, the reference spur and its harmonics cannot be efficiently attenuated by loop filter. Strong reference spurs will deteriorate the linearity requirement. With a small loop filter bandwidth, the locking time may not be sufficient to meet the worst case requirement. Only an increase of the phase detector gain (charge pump current) can increase the loop bandwidth of the frequency synthesizer. Nevertheless, this also increases the power consumption of the frequency synthesizer and may even increase the reference spurs due to the huge current mismatch in charge pump.

The advantage of the fractional-$N$ frequency synthesizer eliminates the above drawbacks of the integer-$N$ frequency synthesizer. Since the fractional division ratio can be implemented with a larger reference clock frequency that is much larger than the channel spacing, the loop filter can effectively attenuate the reference spurs. Additionally, the loop filter bandwidth is very flexible for the locking time as long as the reference spurs can be reduced to a certain accepted level.

In this application, -94 dBc phase noise at 40kHz offset is required with a 1.5GHz carrier frequency. In the phase noise spectrum of the frequency synthesizer, close-in portions of the phase noise are contributed by PLL, other than VCO as explained in a previous chapter. Several design perspectives should be taken under consideration, such as loop bandwidth and noise contribution from each PLL building block. This makes i-
band phase noise very difficult to control. Phase noise of the VCO dominates out-of-band noise. Here, VCO phase noise is used to achieve the phase noise requirement instead of the in-band phase noise. A 3rd-order loop filter is planned for this 4th-order frequency synthesizer. A stable PLL is needed from first-cut design of the loop filter. The simulated VCO gain and desired charge pump gain are needed for the loop stability design.

Two prototypes of handset synthesizer silicon have been implemented: synthesizer breakout and integrated synthesizer/VCO. The circuit block testing is implemented by reading the individual components functions, such as reference divider output and main divider output. The VCO module is alone with printed circuit board (PCB).

The implemented VCO core has a positive feedback active device and a pair of the on-chip resonant tank with analog tuning and digital band tuning scheme in [95]. The VCO module has two output frequencies with divided-by-2 and divided-by-4 dividers. The on-chip LC resonant tank can occupy a large amount of die space if a low VCO frequency is required. Thus the VCO is designed with high oscillation frequency and provides dividers for low divided oscillation frequency. The free-running frequency of the VCO core is around 3GHz with 12% tuning range. The measured VCO phase noise with divided-by-2 divider is shown in Figure 8.1.

The resonator Q is improved by the IC technology; IBM SiGe process offers a 4um thick aluminum layer to improve the passive component losses. The digital tuning is composed of 4 MOSFET varactors with 4-bit control lines. The VCO core also has an analog frequency control line for its usage in the high precision phase-locked loop. The advantage of the digital tuning scheme is that analog VCO gain is reduced, so the VCO is
less sensitive to the transmission of the power supply noise. The devices of the VCO are noise-isolated by deep-trenches. Since the focus of this work has been on the frequency synthesizer, more VCO details are not discussed here but can be found in the references [39]-[46]. The VCO can be used for multi-standard telecommunication systems because of its low phase noise, wide tuning range performance. This VCO consumes 10mA current.

![Phase noise of the VCO](image)

**Figure 8.1: Phase noise of the VCO**

### 8.1.1 Theoretical Design and Simulation

Going back to the loop analysis of the PLL, the VCO gain spreads from 35MHz/V to 75MHz/V with 4 digital band tuning and the charge pump gain is
programmable from 150µA to 600µA. The divided ratio is set to 440 with 1.6MHz update frequency of phase detector. The divided-by-4 output of the VCO is connected to the main divider inputs (RF buffer). The open loop function of the phase-locked loop is necessary for loop analysis as mentioned in Chapter 2. With a high-order loop filter, the open loop function is more complicated. We neglect to show this equation, the same design procedure in Chapter 2 is applied. The close loop function of the phase-locked loop has 4 poles and 1 zero. A mathematical tool, “MATHCAD,” is used for equations and plots. The loop stability is determined by the locations of the 4 poles in the s-plane. The only zero is provided to bring up the phase margin of the close loop function.

Figure 8.2: The pole and zero locations with different VCO gains
Figure 8.2 is the pole and zero locations of the phase-locked loop with maximum and minimum VCO gains. This analysis shows that the varied VCO gain would not result in the instability of the phase-locked loop. The slight difference of pole locations may only cause different settling behavior. In Figure 8.3, the pole and zero locations with different phase detector gains are shown. All poles are kept on the left-hand plan for stability.

![Diagram of pole and zero locations](image)

**Figure 8.3:** The pole and zero locations with different charge pump currents

Based on the above stability analysis, the loop filter is chosen. Many literatures and articles describe the synthesis of the loop filter [16], [20], [96], [97]; similar sizes of the loop filters are obtained with different approaches.
Another design parameter, locking time, is difficult to obtain from equations. The macro model simulation of the PLL is used to provide the close results. However, the mathematical model still provides enough views for the preliminary analysis in locking behavior of the high-order PLL. A step response is used for the locking behavioral analysis. In a phase-locked loop, the internal states are being changed with different dimensions. The final equation of the input and output phase errors only represents the tracking behavior; the same behavior appears in the real phase-locked loop. The mapping between these two cases is hard to build.

Figure 8.4 shows the different locking times with different slewing due to the charge pump current. The solid line has the smallest charge pump current. Apparently, the locking time is extremely limited by the slewing because of the slow charge rate of the loop filter. In the mathematical model simulation, the output of the PLL system follows the input ramp until approaching the final frequency and then the loop settling becomes a small signal analysis about the loop bandwidth of the PLL. The dash line and dash-dot line represent the same locking time with different slewing behaviors. This means that the locking time is no longer limited by charging the loop filter but limited by the loop characteristics. The dash-dot line case has a higher Q in its transfer function than the dash line case. Although the charge pump current is large enough to avoid the slewing of the loop, the high Q ripple just increases the small signal settling time. Too much Q may result in an insufficient phase margin and the loop suffers from oscillation.
Figure 8.4: The locking behaviors of the mathematical model

Figure 8.5: The Verilog-A macro model simulation for locking time
In Figure 8.5, a locking time simulation of the PLL using the macro models is shown. The simulation result is around 940μs within ±1kHz frequency resolution. This simulation is based on real case scaling at internal and input/output nodes, so the results are quite close to the measurement. The synthesizer has two-step settling behavior due to the dual-loop design.

The phase noise analysis is based on the linear small signal model of the PLL. The estimated phase noise of each block is extracted from the circuit simulation results. The quantization noise of Delta-Sigma modulator is theoretically analyzed. Figure 8.6 is the estimated phase noise plot of the frequency synthesizer with maximum charge pump current. The phase noise (green line) of the main divider dominates at close-in frequency. Since bipolar transistors are used for the phase detector, the noise contribution is quite low as the pink line shows. A low noise high quality crystal oscillator is adopted (the black line). The main divider consumes only 3.1mA for 1.5GHz maximum carrier frequency. The phase noise of the main divider can be reduced with more current consumption.

The out-of-band noise is dominated by the VCO phase noise. At the far-end frequency, the loop filter attenuates the quantization noise. Moving the far-end pole inward can reduce the residue of the quantization noise. The loop bandwidth of the frequency synthesizer is around 2-3kHz. Figure 8.7 is the phase noise plot with minimum charge pump current.
Figure 8.6: The estimated phase noise of handset frequency synthesizer at divide-by-4 divider output (maximum charge pump current)

Figure 8.7: The estimated phase noise of handset frequency synthesizer at divide-by-4 divider output (minimum charge pump current)
8.1.2 Experimental Results of Handset Synthesizer

The breakout experiment measurements are shown in Figures 8.8 and 8.9. A 3kHz loop bandwidth is designed for the target phase noise. Since this frequency synthesizer is designed for a handset application, the power consumption has to be as low as possible. If the synthesizer needs much lower phase noise inside the bandwidth, the power consumption of each block will be higher. Only 3.1mA current is consumed in the main divider, 1.5mA in phase frequency detector with charge pump, 1.27mA current in the reference divider, and less than 2mA for Delta-Sigma modulator. At the same time, the loop bandwidth is designed to have a small enough locking time. Figure 8.8 and 8.9 are the phase noise of the divided-by-4 VCO output with minimum and maximum charge pump gains respectively. It is easy to see that the out-band phase noise is perfectly dominated by the phase noise of the VCO. The larger charge pump gain helps lower the in-band phase noise as expected, as the loop bandwidth of the frequency synthesizer changes from 1kHz with the minimum current to 3kHz with the maximum current.

The frequency range at divided-by-4 VCO output is used for RX LO and divided-by-2 VCO output is used for TX LO. In this design case, the phase frequency detector operates at 1.6MHz; the carrier frequencies of RX and TX are around 700MHz and 1.5GHz. The fractional spurs may appear around 700kHz and its harmonics. Since the Delta-Sigma modulator randomizes the fractional spurs, the narrow band loop filter can deeply reduce them. Fractional-$N$ synthesis is widely credited for a wide-band application, however the advantage of the fractional-$N$ synthesizer for narrow-band application is shown here. In this strategy of narrow-band application, as long as fractional spurs are
out of the desired frequency range, the fractional-$N$ synthesizer gives much flexibility to the LO design. Only RX LO cases are shown in Figure 8.8 and 8.9. Unsurprisingly, the TX LO case has 6dB higher phase noise due to the extra factor of 2 between the VCO dividers.

The measurement results are very close to the estimated results. The measured close-in phase noise with maximum charge pump current has a 2-3dB different from the estimated phase noise. The difference may result from other noisy sources, such as I/O buffers, interface circuitry and substrate coupling. The measured phase noise with minimum charge pump current is more than 5dB different from the estimated noise. This is due to the estimated noise in the phase detector. The estimated phase detector noise used in this case was the same as the case with maximum charge pump current. Definitely, the less charge pump current there is, the noisier the phase detector. According to the frequency floor plan, the fractional spurs should appear around 700kHz and its harmonics. The 2kHz loop filter has sufficient attenuation for those reference spurs, and the Delta Sigma modulator averages most of the fractional spurs into white noise. The fractional spurs are not stringent limitations on the applications of the fractional-$N$ Delta-Sigma frequency synthesizer.
Figure 8.8: Measured phase noise of handset frequency synthesizer with minimum charge pump current

Figure 8.9: Measured phase noise of handset frequency synthesizer with maximum charge pump current
Figure 8.10 is the phase noise measurement at the divided-by-2 output with a 10kHz loop bandwidth design. The phase noise jumps up slightly around 400kHz because of the quantization noise of the Delta Sigma modulator. A loop filter with wider zero-gain bandwidth cannot attenuate the quantization noise effectively, although the locking time is reduced with large loop bandwidth. The phase noise of the design in Figure 8.10 still meets the requirement at the 40kHz offset. In Figures 8.8 - 8.10, many small spikes appear at the close-in frequency measurements. These are due to the measurement equipment and environment. This disturbance totally disappeared in the integrated synthesizer/VCO chip.

Figure 8.10: Measured phase noise of handset frequency synthesizer at divide-by-2 divider output with maximum charge pump current
A quieter spectrum of the integrated synthesizer/VCO is shown in Figure 8.11. The carrier frequency is up-converted with another LO 388MHz, then down-converted by a divided-by-2 divider to 959MHz frequency. Figures 8.12 and 8.13 are the spectrum of the integrated synthesizer/VCO using different span frequency. They show that the fractional-N frequency synthesizer can provide a very clean spectrum. In Figure 8.13, the reference spurs at the double side band offset of 1.6MHz are less than -85dBc referred to the carrier. Compared with an integer-N synthesizer, the loop filter design of the fractional-N synthesizer is more relaxed in terms of the stability and side-band attenuation. Figure 8.14 and 8.15 show the locking time measurement and die picture. Table I concludes the results of the low power handset frequency synthesizer.
Figure 8.12: The spectrum of handset frequency synthesizer with 1MHz span

Figure 8.13: The spectrum of handset frequency synthesizer with 4MHz span
Figure 8.14: Locking time measurement of handset frequency synthesizer breakout

Figure 8.15: Die picture of low-power handset frequency synthesizer
### Table 8.1: The performance of handset frequency synthesizer

<table>
<thead>
<tr>
<th>RF Input Frequency of Handset Synthesizer</th>
<th>1.2GHz</th>
</tr>
</thead>
</table>
| Phase Noise of Integrated Synthesizer/VCO | -108 dBc/Hz @ 100kHz  
-129 dBc/Hz @ 1MHz |
| Sideband Spurs | -85dBc @ 1.6MHz |
| Power Consumption | < 8mA  
(Synthesizer only w/o VCO) |
| Supply Voltage | 2.5V-3.3V |
| Die Area | 1.08mm × 1.40mm |
| Technology | SiGe 0.5µm AM |

#### 8.2 Fast-Locking Low-Power Basestation Synthesizer

The second silicon prototype of two frequency synthesizers also has been implemented with a SiGe 0.5µm BiCMOS process for wireless network application. This wireless network basestation is using frequency hopping spread spectrum as its communication protocol, and is installed outdoors with a high voltage battery. The above two conditions make the requirement of fast-locking and low-power for this basestation synthesizer. Particularly, the entire basestation relies on only one frequency synthesizer for transmission and receive of signals. This imposes fast-switching function required with sub-100µs between transmission and receive modes.
A VCO module with a high output carrier power is required, which is mounted on printed circuit board (PCB). The high power VCO signal is injected to the chip of the frequency synthesizer through an on-board transformer. For prototype testing, a 1.1GHz-1.4GHz VCO is provided. RF input buffer amplifier of this basestation synthesizer has a fully differential input impedance of 200 ohms, and has a wide input sensitivity from −15dBm to 5dBm. Since this frequency synthesizer requires low in-band phase noise and fast locking time, a high reference clock of 30MHz and a wide loop bandwidth of 100kHz are designed for the frequency synthesis requirement.

This PLL system adopts the same design approach as the handset synthesizer does. A 3rd-order passive loop filter is synthesized for testing purpose.

### 8.2.1 Experimental Results of Basestation Synthesizer

Figure 8.16 shows the phase noise measurement. This frequency synthesizer achieves a low in-band phase noise of −94dBc at 10kHz offset by using 1.25mA charge pump current. In this prototype design, the charge pump provides a programmable current on chip, which provides a possibly extreme low phase noise of −100dBc/Hz at in-band frequency by using a larger charge pump current. In Figure 8.17, the frequency synthesizer achieves a reference spur of −60dBc at 30MHz offset frequency. Moving the 3rd parasitic pole of loop filter can reduce the reference spur, but increases locking time. Figure 8.18 shows the locking time measurement by using 4.375mA frequency detector current. This frequency synthesizer achieves a locking time of 67μs for 100MHz frequency switching. Frequency acquisition aid current in frequency detector
accomplishes very fast locking time simply. Table II concludes the measured results of the fast-locking low-power basestation frequency synthesizer. The original operating frequency of the main divider was designed from 800MHz to 2.5GHz. The silicon measurement shows 2GHz maximum frequency operation of the main divider. The cause of this frequency degradation is due to the parasitic capacitance of the main divider. This can be improved by considering more careful layout issues. Figure 8.19 shows the die picture of the basestation synthesizer. An extra ultra-fast-locking aid circuitry is indicated on the most left part of the die picture, which is not used in the measurement due to the facilitation of microprocessor.

Figure 8.16: Measured phase noise of basestation frequency synthesizer with 1.25mA phase detector current
Figure 8.17: Measured spectrum of basestation frequency synthesizer with 100MHz span

Figure 8.18: Measured locking time of basestation frequency synthesizer with 4.375mA frequency detector current
Figure 8.19: Die picture of fast-locking basestation synthesizer

<table>
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<th>RF Input Frequency of Basestation Synthesizer</th>
<th>2GHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Phase Noise</td>
<td>-94 dBC/Hz @ 10kHz</td>
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<tr>
<td>Sideband Spurs</td>
<td>-60 dBC @ 30MHz</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>&lt; 13mA (Synthesizer only w/o VCO)</td>
</tr>
<tr>
<td>Supply Voltage</td>
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</tr>
<tr>
<td>Die Area</td>
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</tr>
<tr>
<td>Technology</td>
<td>SiGe 0.5μm AM</td>
</tr>
</tbody>
</table>

Table 8.2: The performance of basestation frequency synthesizer
Chapter 9

Conclusions

Nowadays radio frequency consumer products, including radios, televisions, personal computers and mobile phones, flood almost every home on the earth. Evolution of digital communication systems has brought about new digital modulation schemes that allow very efficient use of the available bandwidth, and guarantee excellent quality in most conditions. The new millennium brings a new wireless revolution to home facilities and outdoor activities, such as Bluetooth, wireless LAN, WCDMA 3G, and GPS. They are emerging in corners of human life.

Advanced microelectronics has been a determining factor in this evolution. Submicron IC technology has resulted in DSP chips with more computing power. The RF front end has shifted from discrete component implementation to a few ICs, and even to single-chip solutions. This allows a large cut in the size, cost, and power consumption. The choice of technology is very important to these factors. GaAs has very good frequency performance, but is too expensive in terms of product cost. Bipolar transistors are a good alternative, but are impossible with huge digital integration. So BiCMOS technology is the best choice for RF transceivers nowadays. High-frequency, low-noise Bipolar transistors can be used in high frequency blocks and CMOS transistors can be applied to the mixed-mode circuits (analog baseband and ADC/DAC) and digital logic.
In this work, BiCMOS SiGe technology is chosen for the synthesizer implementation. The advantages of SiGe BiCMOS are higher frequency and lower noise performance in Bipolar transistors compared to their conventional Bipolar transistor cousins. A thick analog metal (AM) is also provided for RF passive components such as inductors with low loss and high Q. This tremendously helps the integration of the RF analog/mixed mode circuits to achieve good performance.

9.1 Present Design Review

Basically, an RF transceiver consists of three main blocks: the receiver, the transmitter and the LO frequency synthesizer. There are many challenges in the design of each block. This work emphasizes the frequency synthesizer. The phase-locked loop synthesizer topology is adopted and studied because of its good high frequency performance and has been analyzed in Chapters 2, 3, 4. An advanced frequency synthesis technique, “Delta-Sigma fractional-N”, is applied to a PLL based synthesizer. The study and analysis of this fractional-N frequency synthesizer has been reviewed in Chapter 5. The breakout and integrated versions of the fractional-N Delta-Sigma frequency synthesizer have been implemented to investigate their advantages.

This work concentrates on the design technique of the frequency synthesizer. The most challenging parts are the VCO and main divider. Both of the blocks must operate at GHz with low noise performance. Two entire frequency synthesizers are implemented with a SiGe BiCMOS process that has 40-60GHz f_t and low noise performance. The main dividers of handset synthesizer and basestation synthesizer have maximum 1.2GHz and
2GHz input bandwidths with low (3.1mA and 8.5mA) power consumption respectively. The multi-modulus prescaler and the synchronized counter are the two main blocks in main divider design. The main dividers are the most power-consumed block in the frequency synthesizers so as to suppress the noise. An RF buffer amplifier in front of the prescaler provides both the input impedance matching and gain for the VCO output signal. The design implementation has been described in Chapter 6.

In Chapter 7, dual-path phase frequency detector is adopted for phase and frequency comparison. Fast and wide locking is provided by a frequency-steered topology. A specific dead zone is set to allow for the fine settling of the PLL. Switching MOS transistors of the charge pump are avoided to eliminate MOS charge injection into the loop filter.

The experimental results of two prototype frequency synthesizers are shown in Chapter 8. The design analysis has been approved with the measurements. An integrated experiment of the handset synthesizer provides the feasibility of the on-chip VCO solution. The experiment of the basestation synthesizer demonstrates very fast locking time for 100MHz frequency switching with low in-band phase noise. Digital Delta-Sigma modulator is implemented with CMOS transistors for integration. The clock of the modulator can be provided internally by either main divider output or reference divider output. The power consumption of the digital modulator is adjusted with update frequency of the phase detector.
9.2 Challenges and Future Research

With the present design prototypes of the fractional-$N$ frequency synthesizer, we demonstrate the design technique on BiCMOS SiGe process. Although the performance is sufficient for use in many applications and wireless standards, several challenges still remain for future development. Two issues are demanded in the future integration market: low power and small die. According to certain phase noise and high frequency performance specifications, the high drawn current ensures the performance. The debate on the low power is eventually going into the enhancement of the circuits and the usage of the low supply voltage. The adoption of conventional CML topology limits the reduction of the supply voltage with targeted performance. BiCMOS SiGe process has the advantage on the low noise and high frequency Bipolar transistor. The low supply voltage operation can be achieved by using CMOS logic gates; on the other hand, CMOS source-coupling logic (SCL) topology introduces the consideration of low frequency flicker noise with high current consumption. CMOS transistors with low supply voltage may not offer high speed as its high supply voltage version does. The low voltage CML topology should be considered as the next candidate for power saving and performance. Additionally, low voltage operation means a lower SNR, particularly with regulation for voltage translation of standard battery, as the other RF/analog blocks can still rely on the standard voltage.

The more advanced submicron BiCMOS SiGe processes help shrink the die size of CMOS circuitry. In analog parts design, PMOS is widely used with npn-Bipolar transistors due to the lack of the pnp-Bipolar transistors. For example, large PMOS
devices are necessary to allow the large charge pump current; small npn-Bipolar devices have high current tolerance density. How to efficiently combine MOS and Bipolar becomes a good topic for smaller die design.

The 4th-order Delta Sigma modulator is over-designed for the required noise performance, which though ensures a minimum quantization noise for the frequency synthesizer. The power consumption of the modulator can be reduced by usage of a 3rd-order modulator with a quarter power saving over the 4th-order modulator.

Locking time is another important character of the frequency synthesizer. The frequency switching has to achieve within a certain frequency resolution during the minimum time slot of the communication protocol. This design work has nonlinear acquisition aid embedded in the phase frequency detector, which complicates the locking behavior. It will be interesting to have more research done on nonlinear locking and leading to an improved design.

Two complete LO fractional-N frequency synthesizers show the feasibility of integration in a SiGe BiCMOS process with low phase noise and low power consumption. Together with advances in the different transceivers, the integrated fractional-N frequency synthesizers enable the universal/multi-standard objective of providing LOs on a single-chip transceiver.
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