Design of A Double-End Sourced Multi-Chip Power Module 
and A High Power-Density Three-Phase Inverter

DISSERTATION

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Abstract

The silicon carbide (SiC) MOSFET has been widely studied over the past decade due to its superior characteristics compared with the conventional silicon (Si) MOSFET. The SiC MOSFET significantly lowers switching losses with its fast switching speed, while its high-voltage blocking capability contributes to a large reduction in on-status resistance, which reduces power losses and improves the efficiency of the system. The capability to operate SiC devices at high temperatures greatly simplifies the thermal management of the system and increases the power density.

Due to limitations in the current-handling capability of single bare dies, power modules—where multiple bare dies are put into small packaging to provide improved performances—are commonly adopted in high-current applications. The conventional power module packaging that is designed for Si devices, however, will degrade the performance of the SiC device and will limit the device from being fully utilized. For these reasons, the objective of this work is to achieve improved performance in multi-chip SiC MOSFET power modules.

The contributions of this work may be summarized as follows: First, the study proposes an improved design for wire-bonded multi-chip SiC MOSFET power modules. The proposed structure, called a double-end sourced (DES) layout, adopts two pairs of DC bus terminals and sources the power module symmetrically from two ends. The structure
provides each MOSFET in the module with two paralleled commutating loops and greatly reduces power-loop inductance. In addition, the symmetrical structure of the DES layout successfully mitigates the imbalance of the power loops between the parallel MOSFETs and allows for consistent performance of the power module. This study examines the performance of the proposed DES layout both in simulations and experiments and compares the proposed layout’s performance with that of a conventional baseline layout. During the double-pulse tests, the DES layout showed much lower voltage overshoot during the turn-off transient stage due to the layout’s reduced power-loop inductance. The dynamic-current sharing during the turn-on transient stage was also greatly improved because of the balanced power loops due to the DES layout. This improved switching performance contributes to lower and more evenly distributed power losses among the paralleled SiC MOSFETs, which improves the efficiency of the power module and makes the paralleled devices equally fully utilized. The study also evaluates the thermal performance of the power modules. In the simulation, for example, the DES layout demonstrated a more than 15 percent reduction in the size of the heatsink while maintaining the same highest junction temperature as the baseline layout; the temperature was also more evenly distributed within the power module. An experimental continuous power test was conducted in which the two layout modules were setup in the same full-bridge converter, with each module consisting of one half-bridge. The DES layout showed a much lower temperature increase compared with the baseline layout under the same operating conditions as well as a higher power-handling capability with the same temperature increases.
The study’s second contribution is to propose a simplified circular-loop model for rapid estimation of the near-field radiation noise that is exhibited by the power module. In the study, the magnetic field was calculated on a measurement plane above the power module, which was then verified by experimental measurement using near-field probes and a spectrum analyzer. The DES layout was found to decrease the peak magnetic field level; more importantly, it generated less magnetic flux in the area in which the gate-driver board was placed. This indicates that the DES layout will lead to lower radiative interference to the power electronics in the layout’s surrounding environment.

The work’s third contribution is to propose a three-phase inverter that accommodates this unique structure. The design ensures that each single-phase module is symmetrically sourced from the DC bus-bar. In addition, the design increases the compactness of the inverter system by incorporating a vertical-integrated DC link and sandwiching the gate-driver board between the DC bus-bar and the power modules. The power stage of this three-phase inverter weights ~705 grams and is successfully operated at 300 V DC input voltage with 0.85 modulation index and 70 A peak output current. This allowed the tested power density to attain up to 21.9 kVA/kg. Finally, the efficiency of the three-phase inverter was evaluated; it was found to attain a peak efficiency of 98.9 percent.

In summary, this work presents a new layout for multi-chip SiC MOSFET power modules and demonstrates improved performance compared with conventional designs. A prototype of the three-phase inverter that adopts the DES layout power modules was built with a power density of 21.9 kVA/kg and 98.9 percent peak efficiency.
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Fields of Study

Major Field: Electrical and Computer Engineering
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Chapter 1. Introduction

Silicon carbide (SiC) devices have been the subject of a great deal of attention over the past several years; their superior performance over their predecessors, silicon (Si) semiconductors, has made SiC devices a promising candidate for electronic uses within automobile and aerospace industries, among others [1-2]. Compared with Si devices, the higher band-gap energy of SiC materials provides several desirable characteristics within modern power-electronic applications. For example, these new devices significantly increase the critical electrical field strength, which enables the devices to have higher voltage-blocking capabilities with an even thinner die thickness. Due to this reduced thickness, the on-state resistance of the device will be much smaller, thus contributing to reduced power loss and improved efficiency. In addition, the elevated maximum junction temperature of SiC devices can greatly simplify thermal management and can reduce the size of the heatsink, which pushes its power density to a higher level [3-6]. The characteristics of SiC versus Si materials are summarized in Table 1.1 [7].

Given that the size of a single die is usually limited to a range of square millimeters (thus limiting the current that a single device can handle), the power modules are usually adopted within high-power and high-current applications, since the paralleled devices in a module can provide increased current-handling capabilities. Conventional power module packaging is no longer suitable for SiC devices, however, since the characteristics of SiC materials have changed dramatically compared with those of Si. For example, conventional
packaging has large power-loop inductances (consisting of the switching device, the device’s freewheeling diode, and the DC capacitor), and since SiC devices have a much higher switching speed, large voltages will be generated across the stray inductance during the switch-off transient stage [8-11]. This induced voltage, together with the DC voltage, will be added across the switching device, thus causing excessive switching losses and threatening the safe operation of the device. A new power module packaging is therefore required to accommodate the need for high-voltage blocking, high-speed switching, and high-temperature operating capabilities.

Table 1. 1 SiC and Si Characteristics Comparison.

<table>
<thead>
<tr>
<th>Electrical Property</th>
<th>Si</th>
<th>SiC (4H)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Band Gap Energy (eV)</td>
<td>1.12</td>
<td>3.28</td>
</tr>
<tr>
<td>Critical Electrical Field (MV/cm)</td>
<td>0.29</td>
<td>2.5</td>
</tr>
<tr>
<td>Electron Mobility (cm²/VS)</td>
<td>1200</td>
<td>800</td>
</tr>
<tr>
<td>Hole Mobility (cm²/VS)</td>
<td>490</td>
<td>115</td>
</tr>
<tr>
<td>Thermal Conductivity (W/cmK)</td>
<td>1.5</td>
<td>3.8</td>
</tr>
<tr>
<td>Maximum Junction Temperature (°C)</td>
<td>150</td>
<td>600</td>
</tr>
</tbody>
</table>
1.1 Review of Power Module Packaging

1.1.1 Wire-bonded Structure

The wire bonding technique is the most widely used approach in power module packaging due to its easy implementation, high maturity, and cost effectiveness [12-14]. Figure 1.1 shows the cross-section structure of the wire-bonded power module. The direct-bonded copper (DBC) substrate is composed of three layers. The top layer is made of copper and consists the circuit traces of the power module. The current will flow in this layer based on the circuit design. The bottom layer is also a copper layer and is usually used as an interface to attach the module onto a baseplate by soldering. The middle layer is made of ceramic materials and function not only as an insulation layer that electrically separates the top and bottom layers, but also as a good thermal conductor to extract heat from top layer to the bottom layer. The most widely recognized and discussed ceramic materials for DBC substrates are listed and compared in Table 1.2 [8].

![Figure 1.1 Cross-Section Structure of a Wire-Bonded Power Module.]
Table 1. 2 DBC Substrate Ceramic Materials.


<table>
<thead>
<tr>
<th>Ceramic materials</th>
<th>Thermal conductivity (W/mK)</th>
<th>CTE* (ppm/K)</th>
<th>Flexural strength (MPa)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Al₂O₃ (99%)</td>
<td>33</td>
<td>7.2</td>
<td>345</td>
</tr>
<tr>
<td>AlN</td>
<td>150-180</td>
<td>4.6</td>
<td>360</td>
</tr>
<tr>
<td>BeO</td>
<td>270</td>
<td>7</td>
<td>250</td>
</tr>
<tr>
<td>Si₃N₄</td>
<td>70</td>
<td>3</td>
<td>932</td>
</tr>
</tbody>
</table>

* Coefficient of Thermal Expansion. CTE of SiC is 3 ppm/K.

Among all the four ceramic materials, silicon-nitride (Si₃N₄) [15-16] has almost the same coefficient of thermal expansion (CTE) as SiC, which means it poses the least force stress at the interface between the substrate and bare dies when the temperature is raised. In addition, its highest flexural strength provides highest thermal cycling reliability and lifetime. However, the material cost of Si₃N₄ substrate is much higher and its slightly lower thermal conductivity does not provide optimal thermal performance. Beryllium oxide (BeO) [17] provides the highest thermal conductivity, but its hazardous nature to the human body has limited the usage. Aluminum-nitride (AlN) [19-25] and alumina (Al₂O₃) [26-27] are the two most widely used materials for DBC substrates. Compared with Al₂O₃, AlN possess better thermal characteristics and has closer CTE with SiC material. That makes AlN preferred and adopted in high-temperature applications. On the other hand, Al₂O₃ provides the most cost-effective approach and is widely used in power modules where sufficient thermal management is provided.
As seen in Figure 1.1, the bare die is attached onto the DBC substrate by soldering. And the connection between the bare die’s top surface and the circuit traces on the DBC substrate is achieved through bonding wires. Bonding wires that are made of gold (Au), copper (Cu), and aluminum (Al) are commonly found in wire-bonded packaging [17, 22, 26, 28-29]. In applications where high current is required, bonding wires as wide as 20 mils will be used to increase the current-handling capability.

Despite its wide implementation, the bonding wires will introduce large stray inductance to the power module. The effect of the stray inductance that exists in the power loop is thoroughly studied in [8-11]. During the turn-off transient of the device, the load current that goes through the device drops at a fast speed and will introduce an induced voltage across the stray inductance. This induced voltage will be added on the DC voltage and poses on the switching device, causing high voltage stress on the device and excessive switching losses.
1.1.2 Planar Structure

The SiC MOSFET significantly increases the switching speed compared with its Si predecessor. It means that it takes a shorter time to turn-on and turn-off the device, and higher voltage will be induced on the stray inductance during switching transients. The device will sustain higher voltage stress and higher switching losses will be generated as well. Therefore, for SiC MOSFET applications, the stray inductance must be minimized to improve the dynamic response of the device and the efficiency of the power module.

Figure 1.2 Planar Packaging Structure.


Figure 1.2 shows the structure of a planar power module [9]. As seen, instead of using the bonding wires, the interconnection of the planar structure is achieved by adopting another DBC substrate and attaching its copper layer onto the top contact terminals of the devices. Due to the wider traces of the DBC copper layer, the power-loop stray inductance is significantly reduced compared with the wire-bonded structure, and hence providing a
superior dynamic performance [30-35]. In addition, the additional DBC substrate provides an another path for heat dissipation. This double-side cooling capability helps to extract heat more effectively out of the module, and hence enable the power module to handle more current at a given thermal requirement, significantly increasing the power density of the module.

Figure 1. 3 Planar Packaging Structure Fabrication Process.


The fabrication process of the planar structure is well explained in [30], and is demonstrated in Figure 1. 3. To simply summarize the fabrication process, the bare dies are first positioned and attached onto the DBC substrate through sintering process. Then an insulation material is applied to cover the device’s guard rings area, preventing electrical breakdown on the edges of the devices. It is followed by the bonding of the lead frames on the different top contact pads of the devices. In this step, pressure has to be carefully applied on the device and DBC substrate in order to achieve solid bonding quality, and it also involves multiple implementation of insulation layer and sintering process. As seen, the device has to be solderable on both the top and bottom contact pads so that the planar
structure can be achieved. However, the commonly available bare dies in the market are usually with aluminum finish on the top contact pads. It cannot be soldered or sintered with traditional methods, and hence metal deposition has to be applied before the die attachment can be realized.

As seen, the die attachment is extremely important in the fabrication process, especially for the top contact pads. Given that the size of the gate and source pads of the device is usually small, the bonding area has to be carefully controlled to keep sufficient clearance. The silver particle paste is a promising and widely studied die-attachment material for the planar structure [36-41]. First, the silver particle paste can keep its shape during the sintering process. It is easy to align the paste with the top contact pads and do not need to worry that the paste will melt and break the clearance during the sintering process. The height of the paste can be easily controlled to match the level of the rest components of the power module, which makes it easier to form the connection to the top contact pads of the bare dies. Second, the planar structure involves multiple sintering process, which requires that the melting point of the after-process material has to be higher than the processing temperature so that the previously attached contact pads will not be affected by the ongoing attachment process. And the silver particle paste is made of silver powder and organic materials, and its melting point will be significantly increased after vaporing the organic components during the sintering process.
1.1.3 Hybrid Structure

As discussed, the planar structure can realize minimized power-loop stray inductance by eliminating the usage of bonding wires. However, it involves complicated and complex fabrication process, and the bare dies that can be soldered on both the top and bottom contact pads are not widely available in the market. Therefore, aimed at simplifying the process and at the same time keeping a relatively low stray inductance, a hybrid packaging structure was proposed [11].

![Hybrid Packaging Structure](image)

Figure 1.4 Hybrid Packaging Structure.


Figure 1.4 shows the structural details of a hybrid packaging [42]. As the same with the wire-bonded structure and planar structure, the bare dies are attached onto a DBC substrate. Meanwhile, a multilayer printed circuit board (PCB) is used. Before the PCB is soldered onto the DBC substrate, windows are cut on the PCB so that the bare dies can be
embedded and exposed after soldering. Finally, the circuit is completed by bonding wires connecting the top contact pads of the device and the top copper trace on the PCB.

The hybrid structure provides several benefits. First, it simplifies the fabrication process compared with the planar structure. Instead of multiple sintering process, the PCB and the bare dies can be soldered onto the DBC substrate in a single time. And the wire-bonded interconnection avoids the complicated metal deposition step and simplifies the die attachment process. Second, the PCB provides flexibility to have complicated circuit traces. It can reduce the footprint of the power module by contracting the circuit into different layers overlapping with each other. However, the reliability of the hybrid structure has not been verified and will be a big concern at raised temperatures. As is well known, the coefficient of thermal expansion (CTE) of PCB materials is relatively large compared with the bare dies and DBC substrate. This big difference will generate large stress force on the interconnections and may cause the de-attach of the bonding wires from the PCB copper traces, threatening the safety operation of the power module.
1.2 Motivation and Objectives

As discussed previously, although the planar module packaging can achieve minimized power-loop inductance, the packaging’s extremely complicated and time-consuming fabrication process is not practical for most applications. In addition, because the hybrid module packaging is a relatively new concept, researchers have yet to verify the technique’s interconnection reliability at raised temperatures, which means that the process will not likely be widely applied in the near future. On the other hand, although wire-bonded module packaging suffers from large stray inductance, its simple fabrication process and high level of reliability mean that it is still prevalent in the market. The purpose of this research is thus to design a new layout that may achieve significant reductions in power-loop inductance while at the same time maintaining the advantages of wire-bonding technology.

Another problem that this research seeks to solve is inconsistent performance among the paralleling devices within a power module. Due to the different locations of the devices within a power module, the length of each power loop will vary, which means that the paralleling devices will have unbalanced power-loop inductances. These unbalanced power loops will cause variations in individual devices’ performance, such as unbalanced dynamic-current sharing and voltage stress. This, in turn, will cause some of the paralleling devices to not be fully utilized, while others will operate under stressed working conditions. The new proposed layout attempts to minimize this inconsistent performance brought about by unbalanced power loops.
1.3 Thesis Organization

The remainder of thesis is organized as follows: Chapter 2 discusses design considerations and introduces various factors that will affect the power module’s dynamic performance; it then presents the double-end sourced layout. Chapter 3 discuss the performance of the DES layout in detail, including descriptions of the simulations and experiments on dynamic performance, thermal performance, and near-field radiation performance. The improved performance is demonstrated via comparisons with a baseline layout. Finally, the chapter presents a full-bridge converter built with the DES layout power modules, and it tests the converter. Chapter 4 presents a proposed three-phase inverter that adopts the DES layout power modules; a continuous power test is conducted, and estimates are provided on the layout’s power density. A temperature-based efficiency-estimation method is then proposed in order to evaluate the efficiency of the three-phase inverter. Finally, Chapter 5 summarizes this thesis and presents possibilities for future work.
Chapter 2. Power Module Design and Fabrication

2.1 Design Considerations

2.1.1 Effect of Power-loop Stray Inductance

The power loop consists of the switching device, its freewheeling diode, and the DC capacitor. It is also called the commutation loop because the load current is periodically commutated between the switch and the diode. During the short commutating period which could be as short as several nano-seconds, the power loop observes a high-speed changing current and will generate a high induced voltage across its parasitic inductance, which will have a big influence on the circuit performance. Figure 2.1 shows a demonstrative model of a commutation circuit, where the load is modeled with a constant current source. When the MOSFET is on, the current will flow from the positive DC bus, through the current source and MOSFET, and goes back to the negative DC bus; while when the MOSFET is off, the current will circulate in the loop consisting the diode and the current source. As the MOSFET keeps switching on and off, the load current will periodically commutate between the MOSFET and the diode. Depending on the locations, the stray inductance can be classified into the drain-to-source inductance or the common-source inductance.
Figure 2. 1 Power-loop Stray Inductance.

Figure 2. 2 Gate Loop During Turn-on Period.
A. Common-source Stray Inductance

As seen in Figure 2.2, the stray inductance \( L_{ss} \) is not only part of the gate-drive circuit, but also it is included in the power loop. Since it is located at the source terminal of the MOSFET and shared between the gate-loop and power-loop circuits, it is usually called the common-source inductance.

The effect of the common-source inductance on the performance of SiC MOSFETs are thoroughly studied in [43-46]. As is well described in the papers, the turn-on transient starts with the rise of the gate voltage \( V_{gate} \). After \( V_{gate} \) has increased to its plateau voltage \( V_{plateau} \), the current \( I_d \) that goes through the MOSFET begins to rise. And this changing current in the common-source inductance will introduce an induced voltage, and its polarity is such that it works against the increasing current, as is shown in Figure 2.2. Hence the gate-loop Kirchhoff’s voltage equation can be expressed as (2.1),

\[
V_{gate} = V_{gs} + V_{L_{ss}} = V_{gs} + L_{ss} \frac{dI_d}{dt}
\]

(2.1)

where \( V_{gs} \) is the voltage across the gate and source terminals of the MOSFET, and \( I_d \) is the power-loop current. As seen, the voltage that is introduced by the common-source inductance will lower the actual voltage that is applied on the gate and source terminals of the MOSFET, and slows down the turn-on transient of the MOSFET. And this extended turn-on time will result in excessive switching losses.

During the turn-off transients, the gate voltage \( V_{gate} \) begins to drop from its maximum value. At the end of its plateau period, the load current \( I_d \) starts to decrease and will induce a voltage \( L_{ss} \frac{dI_d}{dt} \) across the common-source inductance. This voltage will be added on \( V_{gate} \), and cause an increase on \( V_{gs} \). Since at this time the device has not totally
been turned off, this rise on $V_{gs}$ will not cause a miss-trigger, but will delay the turn-off transient and generate excessive switching losses.

Delays on both turn-on and turn-off transients are observed in [43], and it is accompanied with significant increase on the turn-on and turn-off switching losses. Therefore, the common-source inductance has to be minimized to achieve better dynamic performance and reduce the losses of the devices.
B. Drain-to-source Stray Inductance

Stray inductances exist in the copper traces and bonding wires that connects the terminals and contact pads of the devices, and they can be represented with a single drain-to-source inductance \( L_{DS} \) as is shown in Figure 2. 3. During the turning off, the power-loop current will drop from its rated value to zero in a short period. The stray inductances will contour this change of current by inducing a voltage whose polarity tries to keep the current unchanged, as is shown in Figure 2. 3. And the power-loop Kirchhoff’s voltage equation can be written as (2. 2).

\[
V_{DC} = V_{ds} - V_{ss} - V_{L_{ds}} = V_{ds} - (L_{ss} + L_{ds}) \cdot \frac{dI_d}{dt}
\]  

(2. 2)

As seen, the drain-to-source inductance, together with the common-source inductance, will cause an excessive voltage stress across the drain and source terminals of the MOSFET. This voltage is the spike that is usually observed during the turning off of the switching devices, and this voltage overshoot is in proportional with the sum of the common-source and drain-to-source stray inductances. In addition, the excessive stray inductance brought by \( L_{DS} \) and \( L_{ss} \) will slow down the change of current in the power loop, and causes excessive turn-off switching losses to the system.

Reference [47] show that the voltage overshoot during the turn-off transient increases with growing drain-to-source inductance. But while its turn-off switching loss increases accordingly, the turn-on switching loss drops and makes the total switching loss almost the same. Therefore, both the common-source inductance and drain-to-source inductance will affect the dynamic performance of the MOSFET, and the switching losses are more determined by the common-source inductance.
Figure 2. 3 Power Loop During Turn-off Period.
2.1.2 Kelvin-Source Structure

As discussed in the previous section, the common-source inductance of a MOSFET has a big influence on the performance of the device. Not only does it slow down the turn-on and turn-off transients, but also it greatly affects the total switching losses. Therefore, a structure, called Kelvin-source connection, is proposed, and its internal connection and schematic are shown in Figure 2. 4(a) [48] and 2. 4(b), respectively.

As seen in Figure 2. 4(a), the source terminals of the MOSFET are connected to the source pad (S) on the substrate through wide bonding wires, which are represented with thick black lines. In addition, there is a thinner bonding wire that connects the source terminal to another pad (SS), and makes this MOSFET a four-terminal (D, S, G, and SS) device. Terminal G and SS consist Kelvin-source connection, and its schematic is shown in Figure 2. 4(b). The stray inductance that is involved in the gate loop (G-SS) is represented with \( L_{gs} \), and the inductance in the power loop is denoted with \( L_{DS} \) and \( L_{S} \). As discussed previously, at switching transients, a voltage will be induced across the inductance \( L_{S} \) due to the fast changing current. However, this time this voltage drop does not affect the voltage distribution of the gate loop, since it is no longer a part of the gate loop. In other words, Kelvin source decouples the gate loop from the power loop, and stabilizes the applied effective voltage across the gate and source terminals during switching transients. The improved dynamic response has been identified with the implementation of Kelvin source, and the switching losses are greatly reduced [49].
(a)
([48] 650 CoolMOS C7 Gold in TOLL package, Infineon.)

(b)

Figure 2. 4 Kelvin-Source Structure. (a) Internal Connection. (b) Schematic.
2.1.3 Switch Cell

Power modules are usually built in two different forms, single phase-leg (half bridge) module or three-phase (six pack) module, and they are all composed of upper-leg switch(es), upper-leg diode(s), lower-leg switch(es), and lower-leg diode(s). For a long time, the upper-leg switch and upper-leg diode (or lower-leg switch and lower-leg diode) are grouped and treated as the fundamental element of power modules. So, when doing the module packaging, this fundamental element is replicated and placed in corresponding locations depending on the layout design. For example, Figure 2. 5 [10] illustrates the schematic of a full-bridge converter that is consisted of this anti-parallelled switch-and-diode elements, which is covered in blue areas. The switch devices and diodes are denoted with $S_x$ and $D_x$ ($x=1, 2, 3, 4$), respectively, and $L$ represents the stray inductances that exist at different locations of the half-bridge circuit. Among all those stray inductances, $L_{cx}$ and $L_{ex}$ ($x=1, 2, 3, 4$) are associated with the die and the bonding wires, they are the stray inductance that exists within the anti-parallelled fundamental element. On the other hand, $L_{xU}$ and $L_{xL}$ ($x=1, 2, 3, 4$) represent the stray inductances that are outside the switch-and-diode pair, which exist in the DC bus terminals and the traces that connecting the devices. Due to this configuration, large stray inductances are introduced between the upper and lower anti-parallelled pairs, as is shown with red inductors in Figure 2. 5, which increases the power-loop inductance and hence cause high voltage stress and resonance in the circuit.
In order to reduce the power-loop inductance of the power module, a concept of switch cell (SC), P-cell and N-cell specifically, was proposed in [10]. Instead of grouping the switch with its anti-paralleled diode, the SC builds a new fundamental element by putting the switching device in close proximity with its freewheeling diode. Figure 2. 6 shows the same full-bridge converter, but this time with the newly proposed SCs, with P-cells covered in pink and N-cells in blue. Since the commutation of current is conducted between the switch and its freewheeling diode, the SCs eliminates the routing between these two devices and hence eliminates the stray inductance that used to exist in the
conventional power module layout. And, as a result, suppressed LCR resonance and voltage stress were observed [10].

Figure 2. 6 Full-bridge Converter Consist of Switch Cells.

2.2 Power Module Layout Design

2.2.1 A Baseline Power Module Layout

Switch cells have demonstrated improved dynamic performance during switching transients, and based on [10-11, 15] a baseline layout for multi-chip SiC MOSFET power module is firstly designed and studied. Figure 2. 7(a) and 2. 7(b) shows the schematic and internal layout of the baseline power module.

As seen from Figure 2. 7, six SCs are paralleled to form a half-bridge power module, with three of them are P-cells with upper-leg MOSFETs and the rest three are N-cells with lower-leg MOSFETs, and the DC-input and AC-output terminals are placed at the two ends of the module. The Kelvin source structure is adopted to separate the gate loop with the main power loop, so that the common-source inductance is minimized and improved switching performance would be achieved. In addition, in order to further reduce the power-loop stray inductance, a decoupling capacitor is integrated into the power module to enclose the power loop and exclude the inductance brought by the terminals or leads from affecting the main power loop. And, as a result, lower voltage overshoots will be expected.
Figure 2. 7 Baseline Layout Power Module. (a) Circuit Schematic. (b) Internal Layout.
The stray parameters of the baseline layout are firstly extracted in a finite element analysis software, Q3D Extractor namely, and the results are presented in Figure 2. 8. The switching cells are covered in different colors as is shown in Figure 2. 8(a), and their power-loop inductances are shown with the corresponding color bar in Figure 2. 8(b). As seen, the SC D1-M4, which is placed close to the DC terminals, has a smallest stray inductance of 8.70 nH. As the distance between the SC and the DC terminals increases, the power-loop inductance raises gradually. As a result, the SC M3-D6, which is at the far end of the module, exhibits a largest power-loop inductance of 20.63 nH. In high-speed switching applications, every nano-Henry stray inductance counts and will make a big difference on the circuit performance at such short switching transients. Therefore, not only the large power-loop inductance of the baseline layout will generate high voltage overshoot, but also such big difference on the power-loop inductances will cause in-consistent performances among the paralleled MOSFET.
Figure 2. 8 Baseline Layout Power-loop Inductance. (a) Circuit Schematic with SCs. (b) Stray Inductance of Each Power Loop.
2.2.2 Double-end Sourced Power Module Layout

In order to lower the stray inductance and minimize the unbalance between the paralleled power loops, this research proposes a new double-end sourced (DES) layout for multi-chip power modules. Figure 2. 9(a) shows the internal structure of the proposed layout, where, in addition to the DC terminals and decoupling capacitor on the right, another pair of DC bus-bar is adopted at the left end of the module. This newly added DC bus-bar provides each SC with an additional switching path, making each SC have two switching loops in parallel and effectively reduce the equivalent power-loop inductance. For example, for SC M3-D6, the long power loop that connects the decoupling capacitor $C_{d1}$ gives it a large stray inductance in the baseline layout; however, the additional path provides a much shorter loop and, when paralleled, the equivalent power-loop inductance will be greatly reduced compared with that of the single loop.

Figure 2. 9(b) shows the schematic of the DES layout with each SC covered in different colors, and Figure 2. 9(c) presents the comparison of the power-loop inductances between the two layouts. The DES layout makes the first improvement on the power-loop inductance, where the highest stray inductance of all the SCs are reduced from 20.63 nH to 7.97 nH. Secondly, instead of a significant increase on the stray inductance, the DES layout minimizes the variations on the power-loop inductance among the paralleled SCs, and restrains the difference from 11.93 nH that are observed in the baseline layout to 1.95 nH. Therefore, with the reduced stray inductance and more balanced power loops, the DES layout is expected to see smaller voltage stress on the switching devices and more consistent performances between the paralleled MOSFETs.
Continued

Figure 2. 9 DES Layout Design. (a) Internal Structure. (b) Circuit Schematic with SCs. (c) Comparison of Stray Inductance of Each Power Loop.
Figure 2. 9 continued
2.3 Power Module Fabrication

2.3.1 Substrate Fabrication

The packaging process starts with the substrate design and fabrication, and the direct-bond copper (DBC) substrate is most widely used in power module packaging. A DBC substrate is usually composed of three layers, and they use different materials and have different functions. The top layer is made of pure copper, which is usually covered with Ni/Ag or Ni/Au finishes to protect it from oxidation, and it is where the devices are attached. The middle layer is made of ceramic materials, such as Al₂O₃ and AlN, and functions as an electrical insulation but thermal conduction layer. It prevents the current from flowing out of the top copper plate, and extract the heat that is generated on the top layer to the bottom layer, which will be attached to a heatsink to maximize the heat dissipation.

As seen in Figure 2. 10(a), before a circuit is applied to this layer, it is a whole piece of copper that could be as thick as 0.4 mm. Depending on the function of the power module, circuit are designed and applied on the top copper layer, where the unwanted copper will be etched off this layer and, as a result, the whole piece of copper is made into islanded copper areas, as is shown in Figure 2. 10(b).
Figure 2. 10 DBC Substrate Top View. (a) Without Circuit Applied. (b) With Circuit Applied.
2.3.2 Screen Print and Die Attachment

The silver paste is selected as the die attachment material for the following reasons. 1) Silver is a perfect conductor in both electrical and thermal domain, and will not introduce significant electrical or thermal resistance to the system; 2) The silver paste is perfect for screen printing, which a mature and easy method that has been long used for module packaging; 3) Unlike some solders which will melt when soldering, the silver paste will keep its shape and hold the dies tight during this process, ensuring that the devices will not move around or tilt during curing; 4) The silver paste’s operating temperature is higher than its curing temperature, which means, once cured, the silver paste will not degrade when the temperature rises again to the curing temperature, making it perfect for multiple soldering applications.

Figure 2.11 Stencil for Screen Printing.
The silver paste has to be applied to the locations where the bare dies will be later placed, and with certain and uniform thickness. This is because if the silver paste is too thin, it will not provide enough holding strength for the device; but if the paste is too thick, it will introduce excessive electrical and thermal resistance, degrading the performance of the power module. Therefore, a stainless steel stencil with meshes in designated areas is adopted to ensure the silver paste is uniformly applied onto the substrate, as is shown in Figure 2. 11. The substrate is placed underneath the stencil, and as the silver paste is squeegeed from one side to another on the stencil, some of them are pushed into the mesh and left on the substrate. As shown in Figure 2. 12, after screen printing the silver paste is applied uniformly on the designated areas, and the bare dies will be later placed on the top and cured following a specific temperature profile.
2.3.3 Wire Bonding

Due to its high simplicity and maturity, the wire bonding technique is adopted to make interconnections between the top contact pads of the bare dies and the DBC substrate. In this research, aluminum wires with 10-mil diameter is used and the bonding is conducted with a manual wire-bonder shown in Figure 2.13. During the bonding process, the wire is pressed against the contact pad by the bonding tip/wedge, ultrasonic acoustic vibrations are applied locally to form a solid joint between the contacting surfaces. The pressing force, vibration power, and bonding time have to be carefully controlled to make solid bonding and not break the device. Figure 2.14 shows the enlarged picture of devices with bonded wires.
Figure 2. 13 Manual Wire Bonder.

Figure 2. 14 Detailed Bonding Wires.
2.3.4 Encapsulation

If without any protection, the devices inside a power module will be exposed to the working environment. The dust and moisture will in direct contact with the devices, which will degrade its performance and shortens its lifetime. Therefore, a layer of encapsulant has to be applied to isolate those devices to improve the resistance to the harsh environment. Encapsulants usually come in two parts, and they are stored in two separate tubes as is shown in Figure 2. 15.

![Figure 2. 15 Encapsulant Package.](image)

Before using, the two liquid parts have to be thoroughly mixed. During this process a plenty of air bubbles will be trapped into the mixture, and they will generate voids in the cured encapsulant and affect its insulation strength. Therefore, a degassing step has to be implemented before the mixture could be applied. As shown in Figure 2. 16, the
encapsulant is put into a degassing pot, and bubbles could be easily identified in the mixture before degassing. As the process begins, a pump starts to extract the air out of the pot and gradually create a vacuum environment. During this process, the air that is trapped in the mixture starts to emerge and rise to the surface of the liquid mixture. Due to the decreasing pressure in the pot, the bubbles expand and grow, and after a certain point they break and the degassing process is complete. The degassed mixture is then poured onto the power module and cured following a temperature profile, and the packaging is complete.

Figure 2. 16 Degassing Process.
2.4 Conclusion

The stray inductance plays an important role in the dynamic performance of the power module. Therefore, the main consideration when designing the module layout is to minimize the power-loop inductance. The switch cell concept is adopted to minimize the distance between the MOSFET and its freewheeling diode; the Kelvin source structure is incorporated to decouple the gate-loop inductance from the power-loop inductance; and the DC decoupling capacitor is integrated into the module to close the power loop, eliminating the influence of the stray inductance of the lead frames on the switching performance of the devices.

The proposed DES layout provides paralleled commutation loops for each MOSFET of the module, significantly reduces the equivalent power-loop inductance compared with the baseline layout. In addition, the DES layout balances the power loops among the paralleled MOSFETs, and consistent performances are expected.
Chapter 3. Power Module Performance Validation

3.1 Static Performance Characterization

Two SiC MOSFET power modules rated at 1200 V/60 A are fabricated in the lab following the packaging process that is discussed in Chapter 2, one with the baseline layout and the other with DES layout, and the prototype is shown in Figure 3.1 (only the DES layout is shown here). And before the fabricated power modules are used for power tests, the static characterization has to be performed on the modules to make sure that the devices are not broken during the fabrication process, all the wire-bonds and leads are solid attached and connected, and no excessive resistance is introduced to the power module.

Figure 3.2 shows the test setup, where the terminals of the MOSFETs under test are connected to a fixture that is designed for discrete devices. And in order to obtain the static characterization of a single device, the rest two paralleling devices in the same half-leg are shorted at the Kelvin source terminals. Figure 3.3(a) and 3.3(b) presents the threshold voltage characteristics and output characteristics of the MOSFETs, respectively, and for demonstrative purpose only the three lower-leg MOSFETs (specifically M4, M5, and M6 as is shown in Figure 2.7) of the baseline and DES layout are shown in Figure 3.3.

Figure 3.3 shows that the threshold voltage (defined at 10 mA load current) of the six MOSFETs varies from 3.16 V to 3.3 V, and the voltage drop (at 20 A load current) across the drain and source terminals varies between 1.78 V to 1.86 V.
Figure 3. 1 1200 V/ 60 A SiC MOSFET Power Module with DES Layout.

Figure 3. 2 Static Characterization Setup.
Figure 3. Static Characterization of MOSFETs. (a) Threshold Voltage Characteristics. (b) Output Characteristics.
3.2 Dynamic Performance Validation

3.2.1 Introduction

The double-pulse test (DPT) is a method that is widely used to evaluate the dynamic performance of a switching device [50-51]. By applying two pulsing signals to the gate terminal of the device, both the turn-on and turn-off transients can be obtained. It captures the changes of the current that goes through the device and the voltage drop across the device during the short switching period, which is an indicator of the circuit’s dynamic performance.

Figure 3. 4(a) [52] shows the schematic of a DPT setup. A freewheeling diode is connected in series with the switching device that is under test, and together with a load inductor, it provides a path for the load current during the off period of the switching device. The DC source provides the power to raise the load current to a certain level, and the DC capacitor is responsible for providing the pulsing energy during the switching transients. The gating signals to the switching device is given in Figure 3. 4(b) [52], as well as the current going through the device and the voltage drop across the terminals. Starting from $t_1$, a high gating signal is applied to the device, connecting the load inductor to the DC source. Under this constant voltage, the current goes through the inductor and the device begin to raise at a constant rate, as is shown with $I_{DS}$. After a certain amount of time, when the load current reaches the aimed value, the gating signal is removed at $t_2$ and the device is turned off. The current in the load inductor cannot change abruptly, so it pushes its current to the freewheeling diode and forced the diode to turn on. This current will freewheeling in this inductor-diode loop for a short period, and since the resistance of this loop is negligible, the current during this time interval will be kept almost constant. At $t_3$, 

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the switching device is turned on again with the second pulsing signal, and the current that goes through the freewheeling diode is transmitted back to the switching device. And the current at $t_3$ is almost the same with that of $t_2$ because the loss in the inductor-diode loop is negligible. Finally, the device is turned off at $t_4$ and the DPT is complete.

As seen, at time point $t_2$ and $t_3$, the DPT perfectly represents the switching performance in the turn-off and turn-on transients, respectively, under desired operation DC voltage and load current. Therefore, with the DPT provides a simple and detailed analysis for evaluating the dynamic performance of the switching device.
Continued

Figure 3.4. Double-pulse Test. (a) Test Schematic. (b) Test Waveforms.

Figure 3. 4 continued (b)
Figure 3. 5. Baseline Layout Double-pulse Test Schematic.
Figure 3. 6. DES Layout Double-pulse Test Schematic.
3.2.2 Switching Test Simulation

Based on the power-loop stray inductance that is obtained previously, as is illustrated in Figure 2.8 and Figure 2.9, the circuit model for the baseline layout and the DES layout is built in LT Spice and is presented in Figure 3.5 and Figure 3.6, respectively. The switching test simulation is conducted at 400 V/60 A on the lower-leg MOSFETs, specifically M4, M5, and M6. Figure 3. 7(a) shows the simulated results of the voltage across the paralleling MOSFETs during module’s turn-off transient. In this switching period, the stray inductance will generate induced voltage across itself that is proportional to its inductance, which will be added onto the MOSFET and result in voltage overshoot. In the baseline layout, the three MOSFETs experience higher voltage stress due to their large power-loop inductances, with the highest reaches up to 105 V. On the other hand, the reduced stray inductance of the DES layout, as is shown in Figure 3. 7(a), successfully lowered the voltage stress to 64 V. Moreover, an 18 V voltage difference between the three MOSFETs is observed in the baseline layout. This is caused by the unbalanced power loops of the baseline layout which raises the stray inductance rapidly from 8.7 nH (M4) to 18.18 nH (M6), as is shown in Figure 2.9. But the symmetrical DES layout minimizes this inconsistency to 3 V.

Figure 3. 7(b) illustrates the current-sharing between the three MOSFETs during the turn-on period. Because of the unbalanced power-loop inductances of the baseline layout, the MOSFET with a smaller stray inductance (M4) tends to switch faster, drawing more current through itself, whereas M6 which is slowed down by its large stray inductance conducts much lower current during this turning-on transient. On the other hand, in the DES layout, the identical power-loop inductances shared by the three MOSFETs make the
dynamic current distributed more evenly among the devices, minimizing the difference from 15 A to 2 A. Figure 3. 7 reveals that the reduced and balanced power-loop inductances brought by the DES layout will contribute to lowered overshoots and consistent performances among the paralleling MOSFETs, which can not only reduce the excessive switching loss but also extend the operation range of the module without damaging the devices.

Figure 3. 8 shows the switching energy comparison between the two layouts. The DES layout helps eliminate the excessive switching loss that is generated by the large overshoot voltage and poor current-sharing of the baseline layout, reducing the total switching energy from 575.4 uJ to 546.1 uJ. In addition, the consistent performances in the DES layout minimizes the switching energy difference among the paralleling MOSFETs from 10.7 uJ to 7 uJ.
Figure 3. 7 Simulated Transient Performance. (a) Turn-off Voltage. (b) Turn-on Current.
Figure 3. 8 Switching Energy Comparison.
3.2.3 Experimental Double-pulse Test

A DPT is conducted at 300 V/60 A to illustrate the transient performances, and the result is shown in Figure 3.9. Higher voltage overshoots are observed across the three paralleling MOSFETs in the baseline layout, exhibiting 52 V, 62 V, and 70 V, respectively. It verifies the idea that its rapidly increasing stray inductance will cause large voltage stress and in-consistent performances. On the other hand, the DES layout succeeds lowering the voltage stress to 44 V, 48 V, and 44 V, respectively, and reducing the difference from 18 V to 4 V. The low-frequency component of the waveforms is caused by the oscillation on the DC capacitor.

Figure 3.9 Experimental Turn-off Voltage Overshoot.
3.3 Thermal Performance Validation

3.3.1 Thermal Performance Simulation

In Figure 3.8, we have extracted the switching loss of each paralleled MOSFETs in the baseline layout and the DES layout. And together with the simulated steady status current distribution, the total power loss on each MOSFET can be calculated. Therefore, the thermal performance of the two layouts can be evaluated with the help of thermal simulation tools.

The simulation model is built in FloTHERM, as is shown in Figure 3.10. The power MOSFETs are modeled as heat sources with constant power losses, whose value is obtained in the previous simulation results. The MOSFETs are placed on a three-layer DBC substrate, with copper layer on the top and bottom and ceramic layer in the middle. And the whole module is placed on a plate-fin heatsink. The cooling fan is modeled in 2D and outputs a constant air-flow rate. The whole system is simulated in an environment of 25 °C. The simulation is conducted as the following: a) the previously obtained total power loss of each switching device is assigned to the constant heat sources in the thermal model; b) the cooling conditions are kept the same for the baseline layout and the DES layout, for example the air flow rate and the size of the cooling fan; c) the heatsinks for both layouts are kept the same, except for the length of the cooling fin; d) the fin length of the heatsink in the baseline layout and DES layout is adjusted individually so that the highest temperature inside each module reaches up to 150 degrees Celsius.

Figure 3.11 shows the simulation results based on the conditions that are mentioned above. In the baseline layout, the highest temperature rise is observed on the top right MOSFET. And the temperature difference between the paralleled devices is 20 degrees
Celsius. On the other hand, the DES layout reduces this difference to 12 degrees. This is because, as is illustrated in Figure 3. 8, the lowered power-loop inductance and the balanced power loops brought by the DES layout not only reduces the excessive switching losses, but also distributes the power losses more evenly among the paralleled devices. Therefore, the temperature rises on each device are expected to be identical in the DES layout. But for the baseline layout, the in-consistent performance between the paralleled devices results in much higher temperature rise on some of the devices than the rest. So with the same heatsinks, the highest temperature of the baseline layout is expected to be higher than that of the DES layout. In other words, if the thermal management is implemented such that the highest temperature of the two layouts are kept the same, the heatsink size of the DES layout is expected to be smaller than that of the baseline layout. And it is verified in Figure 3. 11, where the DES layout reduces the fin length of the heatsink from 23 millimeters to 19.5 millimeters while keeping the same highest temperature rise.

As is indicated with the results shown in Figure 3. 11, the paralleled devices are better utilized in the DES layout. It significantly increases the compactness of the system by shrinking the size of the thermal management, which will greatly improve the power density of the system.
Figure 3. 10 Thermal Simulation Model.

Figure 3. 11 Heatsink Comparison under the Same Thermal Requirement.
3.3.2 Experimental Thermal Test

A continuous power test is conducted to illustrate the improved thermal performance of the DES layout. The thermal simulation demonstrates that the DES layout requires a shorter fin length while keep the same highest junction temperature with that of the baseline layout. However, in the lab it is hard to cut the fin to a certain length so that the DES layout and the baseline layout have the same highest temperature rises. Therefore, an alternative comparison method is adopted.

Figure 3. 12(a) shows the setup of the continuous power test. The DES layout is placed on the left, and it is connected to a double-end DC bus-bar so that the symmetrical structure is achieved. On the other hand, the baseline layout is placed on the right, and it is sourced from the DC bus through the single-side bus-bar on its left. And the AC output terminals of the two modules are connected to the two terminals of a load inductor, which consist the basic structure of a single-phase converter. In other words, the DES layout and the baseline layout each consist one half-bridge of a full-bridge DC-AC converter. By doing this setup, it ensures that the operating conditions for the two layouts are the same, and the difference that will be observed is contributed by the layout design.

The first test is conducted in a natural cooling condition, with the cooling fans turned off. The two modules with different layouts are attached onto two identical heat sinks, as is shown in Figure 3. 12(b), so that the cooling conditions for the two layouts are kept the same. The DC voltage is set to 300 V, and the modulation index is carefully adjusted to obtain varied output current.
Figure 3. 12 Continuous Power Test Setup. (a) Overview. (b) Front View.
Figure 3. 13 Output Current under Natural Cooling and 1 kW Output Power.

Figure 3. 14 Thermal Results under Natural Cooling and 1 kW Output Power. (a) Thermal Image over the Test Setup. (b) Detailed DES Layout Thermal Distribution. (c) Detailed Baseline Layout Thermal Distribution.
Figure 3. 14 continued

(a) Numbers in Celsius

(b) 71.6 72.1 71.5
    M4   M5   M6

    M1   M2   M3
    71.0 71.6 71.2

(c) Numbers in Celsius

    86.7 86.5 85.3
    M4   M5   M6

    M1   M2   M3
    85.8 85.9 84.9
Figure 3. 15 Output Current under Natural Cooling and 1.25 kW Output Power.

(a) Thermal Image over the Test Setup. (b) Detailed DES Layout Thermal Distribution. (c) Detailed Baseline Layout Thermal Distribution.

Figure 3. 16 Thermal Results under Natural Cooling and 1.25 kW Output Power. (a) Thermal Image over the Test Setup. (b) Detailed DES Layout Thermal Distribution. (c) Detailed Baseline Layout Thermal Distribution.
Figure 3. 16 continued

(b)

(c)
With natural cooling condition, the full-bridge converter is firstly tested at 300 V DC input voltage and a modulation index of 0.3. The generated output current reaches up to 24.4 A peak, as is shown in Figure 3. 13, making the total output apparent power of 1 kVA. Figure 3. 14(a) presents the thermal image that is captured with a thermal camera overlooking the full-bridge converter test setup. The DC bus-bars for the two layout modules are illustrated with the dashed lines. And the DES layout module is shown on the left and the baseline layout module is shown on the right. It is not hard to notice that the temperature of the DES layout lays in the yellow and light green region, while the temperature of the baseline layout is in the orange region representing a higher temperature rise. The detailed temperature distribution within the DES layout and the baseline layout is presented in Figure 3. 14(b) and 3. 14(c), respectively. As can be seen, under the same operating and cooling conditions, the highest temperature in the DES layout is 72.1 degrees Celsius while the baseline layout reaches up to 86.7 degrees. This indicates that the baseline layout generates higher power losses than the newly proposed DES layout. As discussed in the previous chapters, the paralleled commutating loops of the DES layout significantly reduces the equivalent power-loop stray inductance and mitigates the in-consistent performances among the paralleled devices. It lowers the overshoot on both the turn-off voltage and turn-on current, hence reducing the total switching loss of the power module and contributes partially to the temperature difference that is shown in Figure 3. 14. This initial temperature difference that is cause by the switching loss further causes the difference of the on-status resistance of the two layout modules, since the on-status resistance of SiC MOSFET is highly dependent on the junction temperature. As the temperature of MOSFET increases, its on-status resistance also increases and will generate
more power losses in the power module. In short, the excessive switching loss of the baseline layout initiates a higher temperature rise of the module, which raises the on-status resistance of the devices and feedbacks with higher power losses and temperature rise.

In the thermal simulation result that is presented in Figure 3.11, the paralleled MOSFETs show a big difference on the temperature rises due to the varied power losses assigned onto each device. But in the experimental test result shown in Figure 3.14, this big temperature difference is not observed. This is because the SiC MOSFET has positive temperature coefficient of on-status resistance, which means the on-status resistance will increase with higher junction temperature. Therefore, if one of the paralleled MOSFET is conducting more current due to the unbalanced power loops, it generates more power loss and tends to have a much higher temperature rise. As its temperature rises, its on-status resistance also increases. And this will reduce the current that goes through this MOSFET and re-direct the current into other paralleled devices. This dynamic balancing on the steady-status current will mitigates the temperature difference among the paralleled devices, and is not considered in the thermal simulation.

It has shown that under natural cooling condition and 1 kVA output apparent power, the temperature of the baseline layout reaches to around 87 degrees Celsius. So, the second test is designed to push the output power higher so that the DES layout module reaches the same temperature. At the same 300 V input DC voltage, the modulation index is tuned to 0.35. The peak output current is raised to 28.6 A, making the total output apparent power 1.25 kVA as is shown in Figure 3.15. Figure 3.16(a) shows the temperature image overlooking the test setup, and Figure 3.16(b) and 3.16(c) show the detailed temperature distribution within the DES layout and the baseline layout, respectively. As expected, the
DES layout demonstrates 15-degree lower temperature rise compared with the baseline layout. With 1.25 kVA output apparent power, the DES layout reaches almost the same temperature rise with the baseline layout that outputs 1 kVA apparent power, which is 25% increase in power density under the same cooling conditions. In other words, if the two layout modules are to output the same power rating, the heat sink for the DES layout will be anticipated smaller than that of the baseline layout while keeping the same highest temperature rise. This matches well with the thermal simulation result that is presented in Figure 3. 11.

The final test is conducted at full-load operation condition under forced-air cooling. The peak output current is raised to 58 A (the module is rated at 60 A) shown in Figure 3. 17, and the thermal image of the test setup is given in Figure 3. 18. Compared with the baseline layout whose temperature reaches 47.9 degrees Celsius, the DES layout only has 42 degrees. As seen, the three continuous power test has well verified the improved thermal performance of the proposed DES layout.
Figure 3. 17 Output Current under Force-air Cooling and Full Output Power.

Figure 3. 18 Thermal Image under Force-air Cooling and Full Output Power.
3.4 Near Field Radiation

As the switching speed and switching frequency increase, another concern rises on the electromagnetic interference that is exhibited by the power module on the sensitive electric components in its surrounding environment. For example, with the increasing compactness of the system, the gate drivers are more likely to put closely to the power module; if not handled properly, the interference would cause the malfunction of the driver and threaten the safety operation of the system. Therefore, this research further compares the near-field radiation exhibited by the two layouts.

3.4.1 Introduction

![Figure 3. 19 A Dipole Antenna and Its Magnetic Field.](image)

Figure 3. 19 [53] shows the structure of a classic dipole antenna. The time-varying current source represents the force that drives the current flowing in the antenna, and the dashed circles represent the magnetic field that is generated by the straight conductor. As is well known, when a constant current flow through a conductor, a steady magnetic field will be formed around the conductor. Its strength depends on the current magnitude and the distance from the observation point to the conductor, and this steady field does not propagate in the space. On the other hand, if the current that goes through the conductor is time-varying (for example a sinusoidal current), it will produce a time-varying magnetic field whose direction changes periodically at the same frequency as the conductor current, and the field can be predicted by the Maxwell equations shown in (3-1) and (3-2) [54].

\[ \nabla \times \mathbf{E} = -\mu_0 \frac{\partial \mathbf{H}}{\partial t} \]  \hspace{1cm} (3-1)

\[ \nabla \times \mathbf{H} = -\mu_0 \frac{\partial \mathbf{E}}{\partial t} \]  \hspace{1cm} (3-2)

This time-varying field can be either near field or far field depending on the distance from the observation point to the current conductor. There is no such a strict boundary that separates the near field and the far field, however, the most agreed upon understanding is that if the measuring point is within half wavelength (\( \lambda \)) of the signal then it is usually treated as the near field region. And, on the other hand, if the physical distance from the measuring point to the conductor is more than half wavelength, it is called the far field. And in our application, where the switching frequency is in tens of kilohertz range, we are more focused on what happens in the near field.

In a power module, the internal circuit can be treated as composed of individual short copper traces. As the switches turns on and off, the current that goes into those traces changes back and forth periodically. Therefore, the circuit of a power module can be treated
as a bunch of classic dipole antennas that are connected in certain patterns, as is shown in Figure 3. 20, and hence they will radiate energy into the space and cause interference to electronic components that are placed in its near surrounding environment. Therefore, this chapter studies and compares the near field radiation that the baseline layout and DES layout exhibit.

Figure 3. 20 Power Module Composed of Dipole Antennas.
3.4.2 Fast Modeling of Near Field Radiation

The calculation of the magnetic field surrounding a circuit can be done with finite element analysis (FEA) tools such as Maxwell 3D from ANSYS. However, the modeling and calculating process is time-consuming and requires the real geometry of the object to make a good estimation. Therefore, at the very beginning of the design process where a plenty of candidate layouts are under screening, this approach does not provide an intuitive and effective way of comparing between those candidates. This thesis proposes a simple method for fast estimating the near field radiation around a power module, and gives a rough idea of how the magnetic field will be distributed even without the detailed knowledge of the module layout.

Reference [54] studied the near field radiation of a buck chopper, and it demonstrated that the magnetic near-field mapping of a switching cell is similar to the one of a circular current loop. Therefore, a multi-chip power module can be modeled with multiple circular loops placed side-by-side. The modeling is proceeded in the following steps. First, the basic structure of the model is identified. Take the baseline layout as an example, as seen in Figure 3.21(a), the three lower-leg MOSFETs (it is the same for the upper-leg MOSFETs since they work in complementary mode with the lower-leg MOSFETs) and the DC terminals consist the basic structure of the baseline layout. It is highlighted with dark blue lines. And hence, three circular loops can be identified as is shown in Figure 3.21(b) with red arrows. Second, with the detailed circuit model that is presented in Figure 3.5, the time-domain current that goes through each SC can be obtained. This current is then transformed into frequency domain via Fast Fourier Transform (FFT) to obtain the magnitude of each current component under different
frequencies. They are represented as current sources $I_1$, $I_2$, and $I_3$ as is shown in Figure 3. 21(b). Finally, the direction and magnitude of the current of each circular loop $I_{CL}$ is determined based on Kirchhoff’s current law.

The same principle applies to the DES layout. In Figure 3. 22(a), the three lower-leg MOSFETs and the two pairs of DC terminals form the five pillars of the basic structure of the DES layout. Again, with the detailed circuit model shown in Figure 3. 6, the current sources $I_1'$ and $I_2'$ can be identified. Finally, the magnitude and direction of the four circular current loops is determined, as is shown in Figure 3. 22(b). And at this stage, the simplified circular current loop model is built. Figure 3. 23(a) shows an example of the time-domain current waveform that is obtained with the detailed circuit model, and its FFT result is given in Figure 3. 23(b).
Figure 3. 21 Circular Loops in the Baseline Layout. (a) Basic Circuit Structure. (b) Circular Loops and Current Distribution.
Figure 3. 22 Circular Loops in the DES Layout. (a) Basic Circuit Structure. (b) Circular Loops and Current Distribution.
Figure 3. 23 Example of a Current Waveform Obtained with the Detailed Circuit Model.
(a) Time Domain. (b) Frequency Domain.
The Biot-Savart law was used to calculate the B-field on a plane over the power module. The Biot-Savart law describes the magnetic field that is produced by a current-carrying conductor, and it is expressed in (3-3) [55],

\[
\mathbf{B}(\mathbf{r}') = \frac{\mu_0}{4\pi} \int \frac{\mathbf{I}d\mathbf{l} \times (\mathbf{r}' - \mathbf{r})}{|\mathbf{r}' - \mathbf{r}|^3}
\]

where \(\mathbf{r}'\) is a vector presenting the location of the point whose magnetic field is being computed, vector \(\mathbf{r}\) represents the location of the current-carrying element, and \(d\mathbf{l}\) is a vector whose magnitude is the length of the differential element of the current-carrying element and whose direction is the same with the current flowing in this element. \(I\) is the amount of current going through the element, and \(\mu_0\) is the magnetic constant.

![Figure 3.24 The Model Geometry.](image)

In our case, we want to calculate the magnetic field in a measurement plane above the power modules, which is produced by the simplified circular current loops that are demonstrated previously. Figure 3.24 shows the geometry of the model being computed, where a measurement plane is placed above a circular current-carrying loop whose radius
is R, at a height of Z. The x-axis and y-axis are perpendicular to each other, and their origin coincides with the projection of the center of the circular loop onto the measurement plane. T(x_T, y_T) represents a random point on the measurement plane whose magnetic field is being computed, and its angular degree to the x-axis is represented with θ. Therefore, any point in the circular loop can be represented as P(R·cosθ, R·sinθ, 0), and the measurement point can be represented as T(x_T, y_T, Z), and the vectors is expressed in the following:

\[ \mathbf{r} = (R \cdot \cos \theta, R \cdot \sin \theta, 0) \]  
\[ \mathbf{r}' = (x_T, y_T, Z) \]
\[ d\mathbf{l} = (-R \cdot \sin \theta, R \cdot \cos \theta, 0) \]

and

\[ \mathbf{r}' - \mathbf{r} = (x_T - R \cdot \cos \theta, y_T - R \cdot \sin \theta, Z) \]
\[ | \mathbf{r}' - \mathbf{r} | = \left( (x_T - R \cdot \cos \theta)^2 + (y_T - R \cdot \sin \theta)^2 + Z^2 \right)^{1/2} \]

Since we are concerned about the interference that is exhibited by the power module on the gate-driver board which will be placed closely above the module, the vertical component of the magnetic field is more important and is expressed in (3-9).

\[
B_z(x_T, y_T, Z) = \frac{\mu_0 I}{4\pi} \int_0^{2\pi} \frac{R(-R + y_T \cdot \sin(\theta) + x_T \cdot \cos(\theta))}{\left((R^2 + x_T^2 + y_T^2 + Z^2) - 2R(x_T \cdot \cos(\theta) + y_T \cdot \sin(\theta))\right)^{3/2}} d\theta
\]

With the current that is obtained with FFT, the magnetic field that is generated by a power module can be computed. The measurement plane is set at 10 millimeters above the power module substrate, and by applying all the values into equation (3-9), the magnetic field on the measurement plane is obtained and shown in Figure 3. 25(a) and 3. 25(b) for the baseline layout and DES layout, respectively. It illustrates that the DES layout
lowers the peak magnetic field from -44.2 dB to -47.6 dB. More importantly, the total magnetic flux that will interfere with the gate-driver board is significantly reduced. A dashed square is presented in Figure 3. 25 representing the region that the gate drivers will be placed on top of the power module. The DES layout reduces the flux in this region from 4.24e-9 Wb to 2.17e-9 Wb (generated by the switching-frequency current), indicating that the interference to the gating signals will be improved. Note that the switching-frequency component is taken as an example, but this method also applied at other frequencies.
Figure 3. 25 Simulated Magnetic Near Field. (a) Baseline Layout. (b) DES Layout.
3.4.3 Near Field Radiation Measurement

A signal and spectrum analyzer (Model R&S FSV) and a magnetic field probe (Model 7405) are used to experimentally measure the near field radiation that is exhibited by the power module. The principle of the near field measurement is based on Faraday’s Law, which says a voltage will be induced in a closed circuit when it is placed in a time-varying magnetic field, and its magnitude is proportional to the time rate of change of the magnetic flux it enclosed. Therefore, a circular loop is formed at the tip of the probe in order to pick up the magnetic field, and the induced voltage can be expressed as in (3-10) [55],

\[ V = 2\pi f \cdot B \cdot A \]  

(3-10)

where \( f \) is the frequency of the time-varying magnetic field, \( B \) is the magnetic flux density, and \( A \) is the area that the conductor encloses.

Figure 3.26 shows the test setup of the near-field radiation measurement. One baseline layout power module and one DES layout power module is used to build a full-bridge converter, with each power module forming the half-bridge. A 18×16-point grid was applied over each power module area, and, at each crossing point, the probe was placed horizontally to obtain the vertical component of the near-field noises. A 10-millimeter diameter probe is used to pin-point the magnetic strength at each measurement point, as is illustrated in Figure 3.27. The noise level at the switching frequency is extracted and mapped into the power module structure, and the noise mapping of the baseline layout and DES layout are presented in Figure 3.28(a) and 3.28(b), respectively. As seen, a hotspot is identified in the baseline layout, with a highest -43.8 dB. On the other hand, the mapping of the magnetic field over the DES layout shows a symmetrical shape, and lowers the
highest magnetic field to -46.6 dB. This distribution matches with the simulation results that we get from the simplified circular-loop model as is shown in Figure 3. 25, which illustrates that the circular current loop model can effectively predict the distribution of the magnetic field exhibited by multi-chip power modules, and this approach can be useful in fast estimating the near field radiation.

As is given in Figure 3. 29(a), a near-field probe with 30-millimeter diameter is placed in the central area of the power module. This is the area that the gate-driver board will be placed. Figure 3. 29(b) shows the measured frequency-domain noise level, where the black curve represents the baseline layout and the blue curve is for the DES layout. As seen, the DES layout not only reduces the noise level at the switching frequency from -24.6 dBmV to -39.24 dBmV, but also it exhibits lower radiation noises extending to MHz range. These lowered radiation noises will contribute to reduced interference from the power module to the gate-driver board.

This thesis only studies the effect of the magnetic field on the gate-driver circuit, which is generated by the high di/dt through the stray inductance. The electric field that is generated by the fast changing dv/dt will also have influence on its surrounding component. But this influence is negligible compared with that of the magnetic field due to the small coupling capacitance, and is hence not considered in this study.
Figure 3. 26 Near Field Radiation Measurement Setup.

Figure 3. 27 Near-Field Radiation Probing.
Figure 3. 28 Near Field Radiation Distribution. (a) Baseline Layout. (b) DES Layout.
Figure 3. 28 continued

(b) Noise Level (dB)

-46.6 dB
Figure 3. 29 Near-Field Radiation Influence on the Gate-Driver Board. (a) Probing. (b) Test Results.
3.5 Full-bridge Converter

A full-bridge converter was built using the DES layout power modules. The structure of the DES layout requires that the current is symmetrically fed into the power module. Therefore, the DC bus-bar must be carefully designed to keep this symmetry. As is shown in Figure 3. 30(a), the two half-bridge DES-layout power modules are placed at the two sides of the DC link, and are connected in the middle. An inductive load is connected to the AC terminals of the modules. The converter is successfully operated at 300 V DC input voltage, with rated 60 A peak current as is shown in Figure 3. 30(b).
Figure 3. 30 Full-Bridge Converter Full-Rating Operation. (a) Test Setup. (b) Test Results.
3.6 Conclusions

The proposed DES layout achieves a great reduction on the power-loop inductance. More importantly, it balances the power loops and provides consistent performances among the paralleled devices. Improved performances are obtained with the DES layout, which are verified with both the simulation models and experimental tests. The reduced power-loop inductance lowers the current and voltage overshoots during the switching transients and minimizes the switching losses. The consistent performance brought by the DES layout evenly distributes the power losses among the paralleled MOSFETs and results in even temperature rises within the module, making a compact thermal management possible and hence increasing the power density of the system. Moreover, lower near field radiation noise is obtained with the DES layout, which causes less problems when other electronic devices are placed in its near environment.
Chapter 4. A Three-phase Inverter Adopting the DES Layout

Power Modules

4.1 Three-phase Inverter Design

In the previous chapters, we have demonstrated the improved performances brought by the double-end sourced (DES) layout. The reduced power-loop stray inductance contributes to a better dynamic performance during the switching transients, significantly lowering the overshoot on the turn-off voltage and reducing the excessive switching losses of the power module. The symmetrical structure of the DES layout brings consistent performances among the paralleled MOSFETs, and makes the power losses more evenly distributed between the switching devices. This improved dynamic performance leads to a better thermal performance, where a higher power is obtained with the DES layout compared with the baseline layout under the same thermal management. Or a smaller sized heat sink is needed in the DES layout while keeping the highest temperature within the power module the same. In addition, the DES layout has shown a reduced near-field radiation level which will cause less interference to the gating signal.

The next step would be to implement the proposed DES layout into an inverter system. However, the problem is the conventional baseline layout power modules is sourced from the DC terminals from one side, and the current available inverter system is design to incorporate this conventional layout and will not fit the DES layout power modules. Therefore, a new inverter system should be proposed so that each DES layout
power module that is connected to the DC bus-bar can be sourced symmetrically from the two ends.

Figure 4. 1(a) shows the 3D drawing of the proposed three-phase inverter that adopts the DES layout power modules, where the major components of the inverter system are identified. Three power modules are used to form the basic structure, with each one functions as a single phase-leg. They are attached to three individual heat sinks and are placed side-by-side. The shared DC bus-bar is place over and cover the area of the three single-phase power modules, and the DC capacitors are designed to stand on top of the DC bus-bar. And the cooling fans are placed on one side of the inverter system, providing the three single-phase power modules with independent cooling paths. As is shown in Figure 4. 1(b), the whole inverter system takes about 200 millimeters long and 75 millimeters’ height.

This inverter design possesses several advantages. First, this design ensures that each DES layout power module that is connected to the DC bus-bar are sourced symmetrically from the two ends. Second, by putting the DC capacitors right on top of the DC bus-bar, this vertically integrated DC link design minimizes the footprint of the DC bus-bar and hence ensures the minimized size and weight on the DC bus-bar. This will increase the weight efficiency of the inverter and achieves higher power density. Third, the design provides each single-phase power module with independent and equal thermal management. In conventional three-phase inverter systems, the single-phase power modules are commonly placed in series along the air flow path. And as the air flows in its path, it picks up the heat that is generated by the power module it passes and in contact with. Therefore, the ambient temperature for the power module in the downstream will be
much higher than that in the upstream, which will cause the in-consistent performances between the power modules. And this design solves this problem by providing individual cooling path for each single-phase power module. Fourth, the space is reserved between the DC bus-bar and power modules for further integration of the gate-driver boards. The gate-driver boards are designed to be sandwiched into this space to achieve minimized gate-loop length and improved dynamic performance. Without occupying additional space, this design will further increase the compactness of the inverter and provides superior switching performance.

The inverter is fabricated in the lab, and the prototype is shown in Figure 4. 2.
Figure 4.1 Three-phase Inverter Design. (a) 3D Drawing of the Inverter. (b) Inverter Dimensions.
Figure 4.2 The Fabricated Three-phase Inverter.
4.2 Continuous Power Test

The fabricated three-phase inverter is put into a continuous power test setup, as is shown in Figure 4. 3. The DC bus is connected to a DC power supply with screw connections. Commercial gate-driver boards are used for test purpose, and the AC output terminals of the three single-phase power modules are connected to three inductors that are star-connected. The DC voltage is set at 300 V, and the switching frequency of the inverter is 20 kHz. Figure 4. 4(a) shows the test waveforms, showing that the inverter is successfully operated to output a peak current of 70 A. And Figure 4. 4(b) illustrate the temperature rise within a single-phase power module, with a highest temperature up to 57.8 degrees.

Figure 4. 3 Three-phase Inverter Continuous Power Test Setup.
Figure 4.4 Three-phase Inverter Continuous Power Test Result. (a) Output Current and Drain-to-Source Voltage. (b) Temperature Distribution within A Power Module.
In addition, the major components of the inverter system are weighted and the power density (in terms of weight) is estimated. Figure 4.5 shows the weight of the major components consisting the power stage of the inverter. The total weight of the power stage is decomposed and given in Table 4.1:

<table>
<thead>
<tr>
<th>Component Weight</th>
<th>Weight (gram)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Module, DC Bus and Capacitor, Heat Sinks</td>
<td>450</td>
</tr>
<tr>
<td>Gate-Driver Boards</td>
<td>129</td>
</tr>
<tr>
<td>Cooling Fans</td>
<td>126</td>
</tr>
</tbody>
</table>

As seen, the total weight of the inverter is 705 grams, and the output apparent power is estimated at 15.46 kVA based on the results shown in Figure 4.4(a). This makes the tested power density of the prototype to be 21.9 kVA/kg. Note that the test is conducted with a 300 V DC input voltage. And if the DC voltage is to be raised higher (the device is rated at 1200 V), a higher power density can be achieved.
Figure 4. 5 Major Components Weight Breakdown. (a) Weight of Power Modules, DC Bus and Capacitors, and Heat Sinks. (b) Weight of Gate Drivers (Commercial). (c) Weight of Cooling Fans.
Figure 4. 5 continued
4.3 Efficiency Estimation

4.3.1 Introduction

In this section, the efficiency of the fabricated three-phase inverter will be evaluated. As is well known, the efficiency of the power stage of the inverter system is hard to be accurately measured because of the pulsing signals on the output voltage. The output current of a three-phase inverter is continuous, which shows a relatively smooth sinusoidal waveform with switching-frequecy ripples added on the fundamental frequency. Since the switching frequency of the SiC MOSFET is usually set within hundreds of Kilo-Hertz and there is no sudden change in the output current, the requirement for the measurement tools (for example the current sensor and oscilloscope) on the sampling rate and bandwidth is relatively low. On the other hand, since the inverter is PWM controlled, the output voltage at the AC output terminal of each phase is pulsed signals with fast rising time and falling time. And in this application, the rising and falling time is within 10 ns to 20 ns, which requires at least 35 MHz bandwidth [56] and sampling time in Giga-samples per second range. And this poses a critical requirement on the measurement tools that are used to capture this fast changing signals.

The lab provides two methods to measure the efficiency of inverter systems. First, oscilloscope based method. In this approach, current probes and voltage probes are used to measure 1) the input DC voltage and DC current that is injected into the inverter, and 2) the output current and the pulsed voltage at the AC output terminal of each single phase. The current probe, Tektronix TCP0150, provides 20 MHz bandwidth and the voltage probe, Tektronix P5205A HV differential probe, has a bandwidth of 200 MHz. The
oscilloscope, Tektronix MDO4104-3, has a sampling rate of 5 GS/s. These should provide enough measurement bandwidth and sampling rate for a 200 Hz output frequency and 10 ns rising and falling time pulsing signals. However, the gain accuracy and DC accuracy of the voltage probe and the current probe is stated at 3% and 1% [57-58], respectively. This means the total error of the measured input and output power could reach up to 4%. And the test result based on this method cannot be treated reliable. The second approach is based on the power meter. It has the same principle as is explained in the oscilloscope-based method. The output AC current is measured with a transducer, and the pulsed output voltage is directly sent into the voltage-measurement terminals of the power meter. The current transducer used in the lab is LEM IT 700-S and has an accuracy of 0.3%, which is a big improvement compared with the current probes used for oscilloscope measurement. However, the power meter YOKOGAWA WT3000 only provides a 1 MHz bandwidth [59], much less than the required 35 MHz for the 10-ns rising and falling time. This means the fast switching transients of the SiC MOSFET cannot be captured, and the power losses during the switching periods will not be fully represented with the power meter. Hence, this power meter based method will cause a big mismatch between the measured efficiency and what happens in the running inverter system.
4.3.2 A Temperature Based Efficiency Estimation Method

As illustrated in the previous section, the oscilloscope based method and the power meter based method suffers either not enough accuracy caused by the current and voltage probes or not enough bandwidth of the measurement equipment. In order to minimize this measurement error, a temperature based efficiency estimation approach is proposed and adopted in this test.

The principle of the proposed approach is that the power loss of the power module will be reflected as heat that is generated on the device, and this heat will be further reflected as temperature rise of the inverter system. If we set a temperature observation point within the inverter system, the reading of the temperature at this point must correspond to the certain amount of the power losses in the power module. And this temperature reading changes linearly with the power losses (the forced-air cooling system can be treated as a linear system). Therefore, if we know this linear relationship between the total power losses of the module and the temperature reading at a specific location, the real-time loss can be extracted by reading the temperature at this point. In other words, this approach uses temperature as an indicator of the power losses in the power modules.

In order to achieve a better accuracy, the temperature observation point has to be located in the major heat dissipation path and as close as possible to the heat-generating devices, where the temperature change is significant with increasing power losses. And the approach is implemented in the following procedure.
A. Inverter System Setup

The setup of the inverter system is the same with the continuous power test and is shown previously in Figure 4.3. In addition, a thermal coupler is attached onto the heat sink, as is shown in Figure 4.6, whose reading will be indicating the power losses that are generated in the power module that is attached on the same heat sink. The thermal coupler is placed in the center of the heat sink, and its tip is attached to the root of the plated fins and is in contact with the base of the heat sink. This way, the thermal coupler is located in the major heat dissipation path, and is placed as close as possible to the heat source (the bare dies) to minimize the measurement error.

Figure 4.6 Front View of the Heat Sink and Attached Thermal Coupler.
B. Loss-Temperature Curve Acquisition

As discussed above, this approach is based on a known loss-and-temperature relationship. Therefore, this loss-temperature curve must be firstly obtained. In order to improve the accuracy of this approach, we want everything at this loss-temperature curve acquisition stage operate as close to the real-time operation conditions as possible. For example, the air flow rate of the cooling fans is kept the same, and we want to use the switching devices themselves to generate the power losses.

Figure 4. 7 shows the typical output characteristics of a SiC MOSFET [60]. As seen, the equivalent on-status resistance of the MOSFET can be controlled with the gate-to-source voltage. During the normal operation, the gate-to-source voltage is usually kept at 20 V to minimize the power losses on the device. But at this curve acquisition stage, the gate-to-source voltage is deliberately set to a lower level to increase the on-status resistance so that a full-range loss-temperature curve could be obtained.

Figure 4. 8 shows the schematic for obtaining the loss-temperature curve. As seen, the upper-leg MOSFET and lower-leg MOSFET are connected in series with a protective resistor, whose function is to limit the current that goes through the MOSFET, and together they are connected to a DC source. The two MOSFET are kept at on status by applying the same gate-to-source voltage, and the voltage drop across the devices and the current goes through the circuit can be controlled with the applied gate-to-source voltage. By measuring the current in the circuit and the voltage across the whole power module, as is illustrated in Figure 4. 8, the total loss in this power module can be calculated.
Figure 4. 7 Typical Output Characteristics of a SiC MOSFET.

([60] CPM2-1200-0080B Silicon Carbide Power MOSFET Datasheet, Cree.)

Figure 4. 8 Curve Acquisition Schematic.
After running the circuit for a while, the system will enter the steady status and the temperature reading from the thermal coupler will become constant. And this temperature will later represent the amount of the power losses in the power module at the current condition. Then the DC voltage is raised, and the temperature read again after entering the steady status. This step is repeated until the full power loss range is covered, and the loss-temperature curve is obtained and shown in Figure 4. 9. The solid line represents the experimentally measured curve, and the dashed line shows the curve fitting result. It can be seen that as the power loss of the module increases, the monitoring temperature rises linearly over the whole range. This matches well with our assumption, and with a measured temperature the corresponding power loss (variable x) can be determined based on this curve.

![Loss-Temperature Curve](image)

Figure 4. 9 Obtained Loss-Temperature Curve.
C. Efficiency Measurement

With the loss-temperature curve obtained in the previous section, the total losses, including the conductive loss and the switching loss, that are generated in the power module can be easily calculated with the temperature read at the observation point. The three-phase inverter shown in Figure 4. 3 is then operated at a DC input voltage of 300 V. The modulation index is gradually increased to raise the output current and the output apparent power, so is the total power losses in the power module. Figure 4. 10(a) shows the measured temperature as the output current increases. The numbers are then put into the curve-fitting equation that is obtained in Figure 4. 9 to calculate the power losses at each output current level, and the power losses to output current curve is presented in Figure 4. 10(b).

In Figure 4. 10(b), the blue curve shows the measured loss-to-current curve. In addition, the calculated power losses based on the datasheet and the simulation results that are obtained previously is also plotted and shown in yellow curve. As seen, the difference between the measured power losses and the calculated ones are within 5%, proving it a practical approach for estimating the power losses in a power module. The calculated power losses are also broken down into conductive loss and switching loss, as is shown with the orange and gray curves in Figure 4. 10(b), respectively.

The efficiency curve of the three-phase inverter is obtained by dividing the power losses of the power module by the output apparent power, and the efficiency to output power curve is presented in Figure 4. 11. The highest efficiency point happens at 35% of the full-load, reaching to 98.9%. And the efficiency at the full-load condition is 98.8%.
Figure 4. 10 Measured Power Losses. (a) Temperature-Current Curve. (b) Loss-Current Curve.
Figure 4.11 Three-phase Inverter Efficiency Curve.
4.4 Conclusion

A three-phase inverter design is proposed to accommodate the unique structure of the DES layout. It ensures that each power module is sourced symmetrically from the two ends by the DC bus-bar. The vertical integrated DC link design and the sandwiched gate-driver board structure minimizes the footprint of the inverter and increases the compactness of the system.

A prototype is fabricated in the lab, and takes about 705 grams’ weight. It is successfully tested at 300 V input DC voltage with an output power of 15.46 kVA. This makes the power density reach up to 21.9 kVA/kg. The power density can be even higher by pushing the current since the highest temperature is only 60 degrees and by increasing the DC bus voltage.

The efficiency of this three-phase inverter is evaluated with a temperature based approach. The loss-temperature curve is firstly obtained with the self-heating of the power module. Then the inverter is put into normal operation and the temperature rise is recorded. Based on the loss-temperature curve, the power losses of the inverter at a certain operation condition can be obtained. And hence the efficiency of the inverter can be calculated. The prototype reaches 98.9% highest efficiency at 35% of the rated load, and 98.8% at the full load.
Chapter 5. Conclusion and Summary of Contributions

This chapter summarizes the major contributions of this thesis.

First, the thesis proposes an improved wire-bonded power module with a double-end sourced (DES) layout for multi-chip SiC MOSFET power modules. The unique structure of this layout incorporates two pairs of DC bus terminals at the opposite ends of the power module. By using this layout, each MOSFET is provided with two paralleled commutation loops, thus significantly reducing the equivalent power-loop inductances. The symmetrical structure of the DES layout also successfully balances the power loops and allows for consistent performances to the paralleled switching devices.

The study conducted both simulation tests and experimental tests. Compared with the conventional baseline layout, the improved performances were observed using the DES layout and were demonstrated in the thesis. During the double-pulse test, the DES layout showed reduced overshoot voltage during the turn-off transient stage due to the layout’s lowered power-loop inductances. In addition, its balanced power loops successfully mitigated the unbalanced current-sharing among the paralleled MOSFETs during the turn-on period. This improved dynamic performance contributed to a 5 percent reduction in the total switching losses; more importantly, the losses were more evenly distributed among the paralleled devices due to the balanced power loops. The technique’s benefits were reflected in the thermal management of the power module. During the thermal test, the
simulation results showed a 15 percent reduction in the size of the heatsink using the DES layout compared with the baseline layout while maintaining the same output power. During the experimental test, in which the heatsinks and the cooling conditions were kept the same, the DES layout demonstrated 25 percent more power-handling capability than the baseline layout under the same temperature increases. When both layouts were operated at the rated power, the DES layout showed a six-degree-lower temperature increase than the baseline layout, thus indicating a better thermal performance using the DES layout.

Second, this thesis has developed a simple method to quickly estimate the near-field radiation level that is exhibited by a multi-chip power module. The thesis explained the steps required to obtain the circular current-loop model; the mathematical implementation was derived from the Biot-Savart law. The near-field radiation level was calculated on a measurement plane above the power module, and an experimental test was conducted to verify the calculation result. Both results showed that the DES layout reduced the peak magnetic field over the power module; more importantly, the total magnetic flux enclosed in the gate-driver area was found to have been lowered significantly, which indicates the existence of lower radiative interference within the gating signals.

Third, the thesis has proposed a high-power-density three-phase inverter design that adopts the DES layout. The design offers the following benefits: 1) each single-phase power module is symmetrically sourced from the DC bus, which accommodates the unique structure of the DES layout; 2) the vertical-integrated DC link design ensures a minimized footprint for the DC bus and is more efficient in terms of both weight and volume; 3) the sandwiched gate-driver board between the power modules and the DC link increases the
compactness of the system and further increases the power density of the inverter; 4) because the three single phases have independent cooling paths, the temperature increases are expected to be identical, and every module can be equally utilized to its maximum capability. The prototype weighs ~705 grams and was tested to an output power 15.46 kVA, which means that the prototype attains a power density of up to 21.9 kVA/kg. A temperature-based efficiency-estimation method was used to calculate the efficiency of the prototype; the prototype was found to achieve a highest efficiency of 98.9 percent, and an efficiency of 98.8 percent at the rated output power level.
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