Switched Capacitor Circuit Based Isolated Power Converters

DISSERTATION

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Abstract

Power converters with galvanic isolation are ubiquitous in today’s world, covering a wide range of applications. Traditionally, there are three general solutions to achieve the galvanic isolation in power converters, including the magnetic field-based isolation, electric field-based isolation, and optics-based isolation. This dissertation studies isolated power converters based on switched capacitor (SC) circuits, aiming to achieve high power density, high efficiency, and valid galvanic isolation performance that meet safety standards.

This work first explores the integration of transformer into SC circuits, in order to combine the benefits of both the transformer and the SC circuit into a single circuit. A bidirectional quasi-switched-capacitor (QSC) dc/ac circuit is therefore derived to replace traditional half bridge or full bridge circuit. The QSC dc/ac circuit features galvanic isolation, soft-switching capability, and reduced voltage stress on passive and active components. The circuit operation principles and characteristics are discussed.

Next, based on the QSC dc/ac circuit, an isolated QSC pulse-width-modulation (PWM) converter is proposed to serve as an auxiliary power supply in electric vehicles (EVs) or hybrid electric vehicles (HEVs), managing a bidirectional power flow between the high voltage (HV) battery and the low voltage (LV) dc bus. Reduced voltage stress on switches and transformer are resulted. A 1-kW converter prototype is built. The soft-switching peak
efficiency of the converter operating at 500 kHz switching frequency is 96% for the buck-mode operation, and 91% for the boost-mode operation.

Then, the small-signal model and controller design of the isolated QSC PWM converter are discussed. The small-signal model is derived by the method of state-space averaging, and its effectiveness is showcased by comparing its open-loop response simulation results to those of a detailed circuit model. For better line disturbance rejection, a closed-loop voltage controller with feed-forward compensation is designed. Experiment results from the 1-kW prototype with digital control verified the effectiveness of the closed-loop voltage control.

Next, an isolated QSC resonant converter is proposed for the isolated dc/dc conversion in off-line power supply applications. Full soft switching is achieved combining zero current switching (ZCS) on, near ZCS off, zero voltage switching (ZVS) on, and ZVS off within a wide load range, so the switching loss is minimized. A 90-W, 88-V/19-V, 700-kHz prototype is built with 100-V enhancement-mode Gallium Nitride (eGaN) field-effect transistors (FETs). The prototype achieves a power density of 172 W/inch³, and a flat efficiency curve with a peak value of 96%. Furthermore, a 65-W, two-stage, off-line power adapter is designed, where a 65-W, 380-V/19-V, 2-MHz isolated QSC resonant converter prototype is built with enhancement-mode GaN high electron mobility transistor (HEMTs). The 65-W QSC resonant converter prototype has an estimated high efficiency of 97.5%, and a high power density of 275 W/inch³.

At last, a semiconductor-based galvanic isolation solution for power converters is proposed. The isolation principle is fundamentally different from that of the traditional
solutions, including the magnetic field-based solution, electric field-based solution, and optics-based solution. It delivers the differential-mode (DM) load power via semiconductor switches during their ON states, while sustaining the common-mode (CM) voltage and blocking the CM leakage current with those switches during their OFF states. Enabled by wide bandgap (WBG) power devices and SC circuits, this solution potentially results in higher power density compared with traditional galvanic isolation solutions, and it can provide valid galvanic isolation performance that meets the safety standards. The operation principles, research motives, design challenges and solutions are discussed in details, respectively. A preliminary prototype is presented to showcase the DM power delivery performance and the CM isolation performance. Conclusions and recommendations for future work are presented.
Dedication

This document is dedicated to my family.
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Chapter 1. Introduction

1.1. Power Converters with Galvanic Isolation

Since the 1830s when Michael Faraday and Joseph Henry discovered electromagnetic induction independently, which laid the foundation for the following invention of the transformer in the 1870s, the history of research on power conversion with galvanic isolation has progressed. After over a century of evolution, power converters with galvanic isolation have become ubiquitous in today’s world, covering a wide range of applications. Typical examples include various off-line power supplies for laptops and desktops, LED drivers, vehicle on-board chargers, photovoltaic inverters, wireless power transfer, energy storage systems and micro grids, and power converters for utility applications such as solid-state transformers.

Galvanic isolation is the principle of isolating functional electrical subsystems to prevent common-mode (CM) current flow. However, in the meantime, the differential-mode (DM) energy or information still can be exchanged between the subsystems.

The reasons for galvanic isolation are manifold, including: 1) user safety - preventing accidental current from reaching ground through a human body; 2) breaking the ground loop when connecting electrical subsystems with different ground references; and 3) confining and suppressing the CM noise, which causes malfunctions in the DM energy or information exchange. Most off-line power converters are enforced to provide galvanic
isolation according to the industry safety standards (e.g., IEC60950), where the test methods with emphasis on CM isolation voltage and CM leakage currents are well defined.

Traditionally, there are three general solutions to achieve the galvanic isolation in power converters, including:

1) **Magnetic field-based galvanic isolation:** This solution achieves galvanic isolation by an air/magnetic-core transformer. In this solution, as shown in Fig. 1.1, the DM load power is delivered via the magnetic field established between the separate transformer windings. Meanwhile, the transformer effectively blocks the CM leakage current, with high CM impedance provided by the low parasitic CM capacitance across the windings. Most power conversion systems achieve galvanic isolation with this solution, and a well-known example is the isolated dc/dc power converters widely applied in various applications.

![Figure 1.1. Magnetic field-based galvanic isolation solution.](image)

2) **Electric field-based galvanic isolation:** This solution achieves galvanic isolation by employing ac-coupling isolation capacitors with low capacitance (in the pF~nF range)
to replace the transformer [1-13]. These capacitors can be either discrete capacitors, or electrode pairs with an insulator or semiconductor as the dielectric. As shown in Fig. 1.2, these isolation capacitors resonate with connected inductors to provide low impedance at high resonance frequency, so the DM load power flow around such frequency is delivered efficiently via the electric field established within the capacitors. Meanwhile, as these isolation capacitors perform high impedance at low frequency, the dc or line-frequency CM leakage currents are effectively blocked. This solution has been applied in grid-tied power conversion applications including the LED driver [1-4], battery charger [5-7], and power supply for liquid sterilization [8]. Traditionally, electric field-based galvanic isolation is also applied in isolated data transfer applications, such as the digital isolator [9-11] and isolated gate drive [12-13]. In such applications, high CM impedance is required and embodied as a CM transient immunity (CMTI) ratio to block CM noise in the presence of high CM $dV/dt$ (e.g. 50 kV/µs).

![Figure 1.2. Electric field-based galvanic isolation solution.](image-url)
3) **Optics based galvanic isolation:** This solution achieves galvanic isolation by decoupling the electrical systems with optics. It delivers the DM load power via light from the light emitter to the light receiver. Superior CM impedance and CM noise immunity can be achieved because of the low parasitic capacitance (multi-pF) coupling the light emitter and receiver. This solution is applied primarily in low-power (up to hundreds of mW) isolated data transfer over fiber optics or optocouplers [14-15]. Recently, its application has extended to the isolated power transfer within the power range up to 70 W [16], for isolated gate-drive power supply [17] and power supply for consumer quadcopter [16].

1.2. **Transformer Based Isolated DC/DC Power Converters**

To date, transformer based isolated dc/dc power converters are still the most widely employed solution to achieve galvanic isolation. For grid-tied applications, a line-frequency transformer can be added at the grid interface, but its large volume and heavy weight cause low power density. To improve the system power density and reduce the system cost, isolated dc/dc converters with high-frequency transformers are employed in increasingly in applications. Magnetic-core transformers with high permeability materials (e.g., Mn-Zn ferrite) generally are applied in isolated dc/dc converters in the switching frequency region between multi-kHz and multi-MHz. Typical application examples include: isolated dc/dc power converters [18-19]; energy storage systems and dc micro grids [20-22]; ac-ac converters [23-24]; solid-state transformers [25-27]; off-line power supplies [28-29]; LED drivers [30-32]; vehicle on-board chargers [33-36]; photovoltaic inverters [37-40]; isolated sensors [41-43]; digital signal isolators [44-46]; isolated gate
drives [47-49]; wireless power transfers [50-52]; and isolated PCB-mount dc/dc converters [53-55]. Air-core transformers have low permeability and thus are less effective to confine the magnetic field within a limited space. For this reason, it is used primarily for long-distance wireless power transfer applications. However, in the very-high-frequency (VHF) (i.e., 30-300 MHz) switching-frequency region, air-core inductors or magnetic-core inductors with low-permeability radio-frequency (RF) magnetic materials (for core loss reduction) are built to achieve improved converter power density [56-58].

The development of the isolated dc/dc power converters is driven continuously by the ever-escalating market demands for further improvements in efficiency, reduction of physical size and weight, and increase in maximum operating temperature.

Wide bandgap (WBG) power devices, such as Silicon Carbide (SiC) and Gallium Nitride (GaN) devices, are developed and applied to fulfill these emerging market needs. Compared with Silicon devices, the 3X wider bandgap of WBG devices enable them to operate under greater voltage stress per channel length, at higher temperatures, while switching at faster speeds and causing lower power loss. All of these attributes indicate that, by using WBG devices, smaller and more efficient power converters can be realized [59-63].

To maximize the benefits of WBG devices, low-voltage rating of the devices is preferred. This is because low-voltage rated devices are more efficient, as they have better figure of merits, which is the product of the on-resistance and the total gate charge [64-65]. However, most isolated dc/dc power converters in off-line power supplies and grid-tied inverters are built with traditional topologies, which impose high voltage stress (≥dc-bus
voltage) on switches. For low-power applications with the power rating below 90 W (e.g., the 65-W ac/dc power adapters), flyback converter and VHF resonant converters (e.g., the Φ2 resonant converter) are the main-stream topologies employed [66-76]. For applications with higher power ratings between 90 W and a few hundreds of kW (e.g., the level-II vehicle on-board chargers, the off-line power supplies above 90 W, and the solid-state transformers for utility applications), half-bridge or full-bridge circuit based dual-active-bridge (DAB) PWM converters and LLC resonant converters are the standard topologies most widely employed [18-40]. In practice, off-line power supplies and grid-tied inverters are commonly designed with a 400 V dc-bus voltage, so all the aforementioned traditional topologies require high-voltage (e.g., 600 V) rated devices, which is neither energy efficient nor power-density optimized.

Multi-level converters (in particular the modular multi-level inverter [77]) feature reduced voltage stress on switches, and they have been used with good success in high-efficiency, high-voltage utility applications. However, they typically have not been employed in lower voltage (i.e., < 600 V) applications such as grid-tied inverters and rectifiers, or dc-dc conversion, because of their control complexity, limited power density due to a large number of active switches and passive components.

To enable the wider use of low-voltage WBG devices within a simple structure of the transformer based isolated dc/dc power converters, new circuit topologies that can reduce the switch voltage stress are needed.
1.3. *Switched-Capacitor Circuits*

Switched-capacitor (SC) circuits contain only switching devices and capacitors. The absence of magnetic components helps to shrink the system volume and cost. To date, magnetic components still perform energy densities that are orders of magnitude lower than those of capacitors [3] [56-57] [78-82], as discussed in more detail in Chapter 5. As a result, there have been increased studies of SC circuits and electric field-based galvanic isolation.

Another benefit that SC circuits provide is that they can reduce the switch voltage stress, and thus enable the use of low-voltage switches. For example, in the basic Marx cell structure of a multi-level SC converter [83-84], the voltage stress on all switches equals the cell capacitor voltage, which is multiple times lower than the converter’s output voltage. This enables the high-voltage SC converters to be designed using all low-voltage switches.

However, traditional SC circuits provide no galvanic isolation. To enable galvanic isolation, electric field-based galvanic isolation using isolation capacitors also has been demonstrated in SC circuits [3-4]. However, it still require magnetic components (i.e. resonant inductors) together with an inverter circuit and a rectifier circuit, so limited power density results. As an alternative approach to separate and decouple the DM power flows, the SC isolation cell circuit has been introduced [85-86]. This circuit eliminates the magnetic components, and features a simple structure, small number of components, and easy control. However, the isolation capability of the circuit has not been evaluated in the literature. The circuit must be tested according to the industrial safety standards such as the...
IEC60950, to validate its isolation performance such as the CM isolation voltage and CM leakage current.

Challenges for SC circuits also exist in achieving a high voltage transfer ratio and voltage regulation. Power converters generally achieve a high voltage transfer ratio by means of a high turns-ratio transformer. This is another reason why a transformer is usually preferred. In SC dc/dc converters, a high voltage transfer ratio is achieved by cascading multiple SC stages. Typical examples include the Marx generator [83-84], the Cockcroft–Walton generator [87], the Dickson converter [88], and the SC isolation cell circuit-based voltage quadrupler [83-84]. By increasing the number of stages, the voltage transfer ratio increases, although a larger number of components and higher control complexity result as well. On the other hand, voltage regulation remains a challenge for SC dc/dc converters [89-90]. The existing methods of voltage regulation in SC converters are to adjust the converter equivalent resistance such that the converter functions as a linear regulator [91-92]. As a result, the SC converter efficiency suffers and it is always equal to or lower than the normalized voltage transfer ratio.

Recent developments of WBG semiconductors have yielded power transistors with greatly reduced on-state resistance, reduced parasitic capacitance, enhanced breakdown voltage, increased switching speed, and increased operating temperatures. To date, WBG devices have primarily served as drop-in replacements for their Si counterparts in conventional architectures, yielding only partial improvement compared to the ultimate potential of GaN, SiC, and other WBG devices. However, to further the improvement of
system power density, the unprecedented characteristics of WBG devices are bringing new opportunities for SC circuits.

1.4. Motivations of this Work

This dissertation studies the isolated power converters based on SC circuits, aiming to achieve high power density, high efficiency, and high CM isolation performance. Research in this work is performed in two directions as follows:

On one hand, this work further explores the integration of a transformer into SC circuits, and derives new circuit topologies of isolated dc/dc converters to combine the benefits of both the transformer and the SC circuits within a simple structure. In such topologies, the transformer provides galvanic isolation and a high voltage transfer ratio, while the SC circuits provide reduced voltage stress on active and passive components. This part of the research is presented in Chapters 2, 3, and 4.

On the other hand, this work explores the galvanic isolation directly provided by SC circuits, without integrating magnetic components. Recent developments of WBG semiconductors have yielded power transistors with greatly reduced on-state resistance, reduced parasitic capacitance, enhanced breakdown voltage, increased switching speed, and increased operating temperatures. To date, WBG devices have primarily served as drop-in replacements for their Si counterparts in conventional architectures, yielding only partial improvement compared to the ultimate potential of GaN, SiC, and other WBG devices. However, to further improve system power density, the unprecedented characteristics of WBG devices are bringing new opportunities for SC circuits, which are
impractical for Si devices. They potentially enable the SC circuits to achieve valid CM galvanic isolation that meet the industrial safety standards, while having high power density and high efficiency for DM power delivery. This part of the research is presented in Chapter 5.

As switches play critical roles in SC circuits, the unprecedented properties provided by the emerging WBG power devices are bringing new opportunities for the SC circuits.

1.5. Outline of this Dissertation

This dissertation is divided into six chapters as follows:

In Chapter 2, a quasi-switched-capacitor (QSC) dc/ac circuit is proposed to replace the traditional half/full-bridge dc/ac circuits in isolated dc/dc power converters. The circuit integrates a transformer into an SC circuit, combining the benefits of both parts. The circuit operation principles, features, and dc characteristics are analyzed and discussed. Then, based on the QSC dc/ac circuit, an isolated QSC pulse-width-modulation (PWM) converter is proposed to serve as an auxiliary power supply in electric vehicles (EVs) or hybrid electric vehicles (HEVs), managing a bidirectional power flow between the high voltage (HV) battery and the low voltage (LV) dc bus. Design guidelines are given, and a 1-kW, 500-kHz, 400-V/12-V, SiC/Si-based converter prototype is built and demonstrated. The experimental results are presented to validate the converter features and performance.

In Chapter 3, the small-signal modeling and controller design for the isolated QSC PWM converter are presented. The converter output power is regulated by switching-frequency modulation. A small-signal model of the converter in buck-mode operation is
derived by the method of state-space averaging. Open-loop simulation results from the derived small-signal model and a detailed circuit model are compared to highlight the effectiveness of the small-signal model. A closed-loop voltage controller with feed-forward compensation for the switching frequency is designed to improve the dynamic performance. Closed-loop simulation results from both the small-signal model and the detail circuit model, and the experiment results from a 1-kW prototype are provided to verify the closed-loop control.

In Chapter 4, an isolated QSC resonant converter is proposed for isolated dc/dc conversion in off-line power supply applications. Similar to the Φ2 resonant converter, the proposed converter operates most efficiently at a fixed switching frequency and duty ratio, and it features trapezoidal voltage waveforms on all switches. Full soft switching combining zero current switching (ZCS) on, near ZCS off, zero voltage switching (ZVS) on, and ZVS off is achieved within a wide load range, and therefore the switching loss is minimized. A 90-W, 88-V/19-V, 700-kHz prototype is built with 100-V enhancement-mode Gallium Nitride (eGaN) field-effect transistors (FETs). The transformer design and PCB layout are presented to minimize the transformer leakage inductance and stray inductance. The prototype achieved both a power density of 172 W/inch³, and a flat efficiency curve with a peak value of 96%.

In Chapter 5, the study of the semiconductor-based galvanic isolation is presented. This solution delivers the DM power via semiconductor power switches during their on states, while sustaining the CM voltage and blocking the CM leakage current with those switches during their off states. While it is impractical to implement this solution with Si
devices, the latest SiC devices and the coming vertical GaN devices, however, provide unprecedented properties and thus, can potentially enable the practical implementation. An isolated dc/dc converter based on the switched-capacitor circuit is studied as an example. The CM leakage current caused by the line input and the resultant CM touch current (TC) are quantified and compared with the limits in the safety standard, IEC60950. To reduce the TC, a low switch output capacitance and low converter switching frequency are necessary. Then, discussions are presented of the TC reduction approaches and the design considerations to achieve high power density and high efficiency. A 400-V, 400-W prototype based on 1.7-kV SiC MOSFETs is built to demo the DM power delivery performance and showcase the CM leakage current problem.

Chapter 6 summarizes the dissertation and provides an outlook of the future work.
Chapter 2. QSC DC/AC Circuit and Isolated QSC PWM Converter

2.1. QSC DC/AC Circuit

2.1.1. Circuit Descriptions and Operation Principles

A QSC dc/ac circuit is proposed to replace the traditional half/full-bridge dc/ac circuits in isolated dc/dc power converters. The circuit diagram is shown in Fig. 2.1, and the operation waveforms are shown in Fig. 2.2. The circuit combines a transformer (embodied as the transformer leakage inductance $L_s$ and transformer magnetizing inductance $L_m$) with two switched capacitors $C_2$ and $C_3$ that have identical capacitance. This circuit is derived by applying the traditional voltage tripler ac/dc circuit [93] in a reverse power-flow direction, and replacing the 3 diodes with 3 controllable switches. A pair of switches turn on and off synchronously, so they are both referred to as $S_2$. For an isolated dc/dc converter, the transformer leakage inductance cannot be ignored because: 1) it is unavoidable; 2) it limits the active output power capability; and 3) it causes freewheeling transients which leads to the ZVS on of the switches.

Figure 2.1. Proposed QSC dc/ac circuit.
At steady state, there are 4 switching modes within one switching cycle ($T_{sw}$). The brief descriptions of each switching mode are as follows:

**Mode 1.** ($t_1$-$t_2$): The input voltage source, $C_2$, $C_3$, and transformer are connected in series. $C_2$ and $C_3$ are charged. $V_{in}=2V_c-V_{an}$;

**Mode 2.** ($t_2$-$t_3$): $C_2$ and $C_3$ are connected in parallel with the transformer and load. $L_s$ releases its energy back to $C_2$ and $C_3$ via $S_2$. $V_c=V_{an}$;

**Mode 3.** ($t_3$-$t_4$): $C_2$ and $C_3$ are still connected in parallel with the load, and they are now discharged. $V_c=V_{an}$;

**Mode 4.** ($t_0$-$t_1$): The input voltage source, $C_2$, $C_3$, and the transformer are connected in series. $L_s$ releases its energy back to the input voltage source via $S_1$. $V_{in}=2V_c-V_{an}$.

The Mode 2 and 4 are the freewheeling modes where $S_1$ and $S_2$ operate in synchronous rectification mode. Because of the freewheeling currents, $S_1$ and $S_2$ have ZVS on.
2.1.2. *Dc Characteristics*

When the QSC dc/ac circuit is operated at high switching frequency, at steady state, the voltage ripples of $C_2$ and $C_3$ are small compared to their dc offset voltage, so $V_C$ is assumed to be constant. Because of the steady-state volt-second balance of $L_m$ and $L_s$, the voltage stress on $C_2$, $C_3$ and transformer are

\[ V_{C2} = V_{C3} = |V_{an}| = \frac{V_{in}}{3}. \]  
(2.1)

Accordingly, the voltage stresses on $S_1$ and $S_2$ are

\[ V_{S1(max)} = V_{S2(max)} = \frac{2V_{in}}{3}. \]  
(2.2)

The ac output voltages $V_{an}$ is

\[
V_{an}(t) = \begin{cases} 
-\frac{V_{in}}{3}, & 0 \leq t \leq \frac{T_{sw}}{2} \\
\frac{V_{in}}{3}, & \frac{T_{sw}}{2} < t \leq T_{sw}.
\end{cases}
\]  
(2.3)

At steady state, $C_2$ and $C_3$ are charged in series in one half switching cycle and discharged in parallel in the next half switching cycle. Because of the ampere-second balance of $C_2$ and $C_3$, there exists a dc-offset current ($I_{dc-Ls}$) in both $L_m$ and $L_s$. To simplify the calculation of $I_{dc-Ls}$, the zero-state-response (ZSR) of the circuit branch composed of $L_m$, $L_s$ and $R$ is studied. In time domain, in each half switching cycle, the current change of $L_s$ in response to an applied unit-step voltage $2V_{in}/3$ is

\[
\Delta I_{Ls}(t) = \frac{2V_{in}}{3L_s} - \frac{2V_{in}}{3(L_m + L_s)} \cdot \left[ 1 - e^{-\frac{R}{L_s} \frac{R}{L_m} t} \right] + \frac{2V_{in}}{3(L_m + L_s)} t, \quad 0 \leq t \leq \frac{T_{sw}}{2}.
\]  
(2.4)
Assume $I_{Ls}=I_{Ls}(t)$ at $t_0$ and $t_4$, the ampere-second balance of $C_2$ or $C_3$ within one switching cycle is expressed as

$$\int_0^{T_{sw}} [I_{Ls}(t_4) - \Delta I_{Ls}(t)]dt + \frac{1}{2} \int_0^{T_{sw}} [I_{Ls}(t_4) - \Delta I_{Ls}(t)]dt = 0.$$  \hspace{1cm} (2.5)

Based on (2.4) and (2.5), the instantaneous value of $I_{Ls}$ at $t_2$ and $t_4$ can be calculated, and thus $I_{dc\_Ls}$ is derived as

$$I_{dc\_Ls} = \frac{2V_{in}}{L_s} - \frac{2V_{in}}{L_m + L_s} + \frac{4V_{in}}{9(\frac{R}{L_s} + \frac{R}{L_m})} \cdot \left( e^{\frac{-R}{L_s}} + e^{\frac{-R}{L_m}} \right),$$

$$\frac{4V_{in}}{9(\frac{R}{L_s} + \frac{R}{L_m})^2} \cdot \left( e^{\frac{-R}{L_s}} + e^{\frac{-R}{L_m}} \right) - 1 + \frac{V_{in}T_{sw}}{18(L_m + L_s)} - \frac{\Delta I_{Ls}(T_{sw})}{6}.$$  \hspace{1cm} (2.6)

The voltage across $L_m$ is

$$V_{Lm}(t) = \begin{cases} \frac{V_{in}}{3} - \frac{2V_{in}}{3} e^{\frac{-R}{L_s} (t \cdot T_{sw})}, & 0 \leq t \leq \frac{T_{sw}}{2} \\ \frac{V_{in}}{3} - \frac{2V_{in}}{3} e^{\frac{-R}{L_m} \left( \frac{T_{sw}}{2} - t \right)}, & \frac{T_{sw}}{2} < t \leq T_{sw} \end{cases}.$$  \hspace{1cm} (2.7)

Based on (2.7), the active output power is calculated as

$$P_o = \int_0^{T_{sw}} V_{Lm}(t)^2 \frac{dt}{RT_{sw}} = \frac{V_{in}^2}{9R} + \frac{8V_{in}^2 L_s L_m}{9R^2 (L_s + L_m) T_{sw}} e^{\frac{-R}{L_s} \left( \frac{T_{sw}}{2} \right)} - \frac{4V_{in}^2 L_s L_m}{9R^2 (L_s + L_m) T_{sw}} e^{\frac{-R}{L_m} \left( \frac{T_{sw}}{2} \right)} - \frac{4V_{in}^2 L_s L_m}{9R^2 (L_s + L_m) T_{sw}}.$$  \hspace{1cm} (2.8)

To help understanding the $I_{dc\_Ls}$, a calculation example based on Matlab is presented. Assume $V_{in}=300\,\text{V}$, $L_m=500\,\mu\text{H}$, and $L_s=0.5\,\mu\text{H}$, which are the typical values for a 500 kHz
isolated dc/dc converter for the vehicle on-board auxiliary power supply application. The value of $I_{dc,Ls}$ at different output power and switching frequency is plotted in Fig. 2.3.

![3D graph showing steady-state $I_{dc,Ls}$ of the proposed QSC dc/ac circuit](image)

Figure 2.3. Steady-state $I_{dc,Ls}$ of the proposed QSC dc/ac circuit.

In practical design, like in the flyback converter case, a dc-offset current in $L_m$ either leads to a large flux swing range which causes a bulky core, or introduces an air gap which causes extra fringing-effect loss, lower coupling coefficient, and increased $L_s$. This problem is successfully solved in the proposed isolated QSC PWM converter, with an appropriate secondary-side rectifier circuit chosen to minimize this dc-offset current in $L_m$. 

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2.2. **Isolated QSC PWM Converter**

2.2.1. *Circuit Descriptions*

Based on the proposed QSC dc/ac circuit, an isolated QSC PWM converter is proposed. The converter schematic is shown in Fig. 2.4. The secondary-side circuit of the converter is a synchronous-rectifier, current-doubler circuit. This circuit functions as 2 interleaving buck converters, which leads to the following benefits: 1) minimized output current ripple due to the ripple-cancelling effect of $L_1$ and $L_2$; 2) low switch conduction losses due to the synchronous-rectification operation; 3) elimination of high-side switch drivers for $S_3$ and $S_4$; 4) balanced current stresses in $S_3$ and $S_4$; and 5) minimized dc-offset current in $L_m$.

![Schematic of the proposed isolated QSC PWM converter.](image)

In the proposed converter, the series-connected $L_1$ and $L_2$ are in parallel with $L_m$. The dc-offset current generated from the primary-side circuit exists in both $L_m$ and this secondary-side branch. However, since the dc resistance (DCR) of $L_1$ and $L_2$ is much smaller than that of $L_m$, the major part of the dc-offset current of $L_m$ is shifted to $L_1$ and $L_2$. This attribute of the converter helps to prevent the transformer core saturation without requiring any air gap. Also, as a result, $L_m$ can be ignored in the equivalent circuit, and thus
the circuit analysis can be simplified. Fig. 2.5 shows the converter’s equivalent circuit where all components are referred to the high-voltage (HV) side. The converter operates in buck mode when power flows from the HV side to the low-voltage (LV) side, and vice versa in boost mode.

![Equivalent circuit of the proposed isolated QSC PWM converter.](image)

**Figure 2.5.** Equivalent circuit of the proposed isolated QSC PWM converter.

### 2.2.2. Buck-mode, Hard-switching Operation Principles

In the buck mode, the converter operates with a symmetrical duty ratio ($D$), and a variable deadband ratio ($\delta$). In order to maximize the duration of synchronous rectification, $S_1$ and $S_4$ are controlled as a complementary pair, while $S_2$ and $S_3$ are controlled as another complementary pair. To be more general, the hard-switching operation is described first. The interval $t_1$-$t_9$ of Fig. 2.6 describes the various stages of buck-mode, hard-switching operation during one switching cycle ($T_{sw}$). One complete switching cycle is divided into 8 modes. In order to simplify the circuit analysis, the circuit parasitic parameters such as the output capacitance of the switches and the stray inductance in the circuit are not considered. $L_1$ and $L_2$ are assumed to have identical inductance. $\delta_1$, $\delta_2$, $\delta_3$ and $\delta_4$ are the
duration ratio of the short transients caused by $L_s$ storing and releasing energy. $I_{L_s}$ is the current of $L_s$. $I_{L1}$ and $I_{L2}$ are the currents of $L_1$ and $L_2$.

![Diagram of Buck-mode, hard-switching operation waveforms of the isolated QSC PWM converter.](image)

Figure 2.6. Buck-mode, hard-switching operation waveforms of the isolated QSC PWM converter.

To help understanding each mode, a set of corresponding annotated buck-mode circuit diagrams is given in Fig. 2.7 with a brief description of each mode as follows:
Figure 2.7. Switching mode diagrams of the Buck-mode, hard-switching operation in one switching cycle: (a) Mode 1: Current path between $t_1$-$t_2$, (b) Mode 2: Current path between $t_2$-$t_3$, (c) Mode 3: Current path between $t_3$-$t_4$, (d) Mode 4: Current path between $t_4$-$t_5$, (e) Mode 5: Current path between $t_5$-$t_6$, (f) Mode 6: Current path between $t_6$-$t_7$, (g) Mode 7: Current path between $t_7$-$t_8$, (h) Mode 8: Current path between $t_8$-$t_9$. (one cycle completes).

Continued
Figure 2.7: Continued
Figure 2.7: Continued

Mode 1. \((t_1-t_2)\): The input voltage source, \(C_2, C_3, L_s, L_1\) and \(L_2\) are connected in series. \(C_2\) and \(C_3\) are charged. \(L_1\) and \(L_s\) store energy, while \(L_2\) releasing its energy to the load;

Mode 2. \((t_2-t_3)\): \(L_s\) releases its energy back to \(C_2\) and \(C_3\), via \(S_3, S_4\) and the body diode of \(S_2\). \(L_1\) and \(L_2\) release their energy to the load;

Mode 3. \((t_3-t_4)\): The energy of \(L_s\) is completely released at \(t_3\). The body diode of \(S_2\) is reverse biased. \(L_1\) and \(L_2\) continue to release their energy to the load;

Mode 4. \((t_4-t_5)\): \(C_2\) and \(C_3\) are connected in parallel and they are discharged. \(L_1\) and \(L_2\) continue to release their energy to the load. Both \(V_{L1}\) and \(V_{L2}\) are clamped to the output voltage, so \(I_{Ls}\) increases quickly, transferring the current from \(S_3\) to \(S_4\). The body diode of \(S_3\) conducts because the current of \(L_2\) \((I_{L2})\) is larger than \(I_{Ls}\);

Mode 5. \((t_5-t_6)\): \(I_{L2}\) is equal to \(I_{Ls}\) at \(t_5\), so the current of \(S_3\) reaches 0 at \(t_5\). After \(t_5\), the body diode of \(S_3\) is reverse biased;

Mode 6. \((t_6-t_7)\): \(L_s\) releases its energy back to the input voltage source and \(C_1\), via \(S_3, S_4\) and the body diodes of \(S_1, L_1\) and \(L_2\) release their energy to the load;
Mode 7. \((t_7-t_8)\): The energy of \(L_s\) is completely released. The body diode of \(S_i\) is reverse biased. \(L_1\) and \(L_2\) continue to release their energy;

Mode 8. \((t_8-t_9)\): The input voltage source, \(C_2\), \(C_3\), \(L_s\), \(L_1\) and \(L_2\) are connected in series. Both \(V_{L1}\) and \(V_{L2}\) are clamped to the output voltage, so \(I_{Ls}\) increases quickly, transferring the current from \(S_4\) to \(S_3\). During this mode, the body diode of \(S_4\) conducts because the current of \(L_1\) \((I_{L1})\) is larger than \(I_{Ls}\). At \(t_9\), the current of \(S_4\) reaches 0 and its body diode becomes reverse biased.

2.2.3. Buck-mode, Hard-switching Operation Dc Characteristics

1) Voltage Stresses on the Transformer, \(S_1\) and \(S_2\)

Benefited from the primary-side QSC dc/ac circuit, the converter features reduced voltage stresses on the transformer and the switches \(S_1\) and \(S_2\). Due to the volt-second balance for \(L_s\), \(L_m\), \(L_1\) and \(L_2\) in one switching cycle, the voltage stresses on the transformer and the switched capacitors \(C_2\) and \(C_3\) are approximately

\[ |V_{an(max)}| = V_{C2} = V_{C3} = \frac{V_{in}}{3}. \]  \(\text{(2.9)}\)

Accordingly, the voltage stresses on the switches \(S_1\) and \(S_2\) are

\[ V_{S1(max)} = V_{S2(max)} = \frac{2V_{in}}{3}. \]  \(\text{(2.10)}\)

2) Output Voltage

As a result of the volt-second balance of \(L_2\) at steady state, the integration of the voltage across \(L_2\) \((V_{L2})\) in mode 1 equals to the integration of \(V_{L2}\) in the other 7 modes. In order to
simplify the analysis, $\delta_4$ is ignored since it is much smaller than $\delta$, so the output voltage ($V_{out}$) is derived as

$$V_{out} = \frac{L_2 \cdot (0.5 - \delta)}{L_S \cdot (0.5 + \delta) + L_2} \cdot \frac{V_{in}}{3N},$$

(2.11)

where $N$ is the transformer turns ratio.

2.2.4. **Buck-mode, Soft-switching Operation Principles and Criteria**

The converter has the capability to realize ZVS in the primary-side QSC dc/ac circuit and ZCS in the secondary-side rectifier circuit. To achieve the ZVS on of $S_1$ and $S_2$, the freewheeling current must continue to flow till the deadband intervals are over, which means the switching Mode 3 and Mode 7 must be skipped. Fig. 2.8 shows the major waveforms of the buck-mode, soft-switching operation.

![Figure 2.8. Buck-mode, soft-switching operation waveforms of the isolated QSC PWM converter.](image-url)
In Fig. 2.8, \(T_{sw}\delta_5\) is the freewheeling interval where \(L_s\) releases and stores its energy. During \(T_{sw}\delta_5\), either \(S_1\) or \(S_2\) is turned on to enable synchronous rectification which reduces the conduction loss. Based on the volt-second balance of \(L_1\), \(\delta_5\) is derived as

\[
\delta_5 = \frac{(V_{in} - 3N \cdot V_{out}) \cdot N^2 L_1 - 3N \cdot V_{out} \cdot (N^2 L_1 + L_s)}{2[3N \cdot V_{out} \cdot (N^2 L_1 + L_s) + (V_{in} - 3N \cdot V_{out}) \cdot N^2 L_1]}.
\] (2.12)

In one switching cycle, the integration of \(I_{Ls}\) equals to the integration of \(I_{dc,Ls}\) derived in (2.6). Therefore, the instantaneous values of \(I_{Ls}\) are derived as

\[
\begin{align*}
I_{Ls}(t_6) &= I_{dc,Ls} + \frac{V_{in}T_{sw}\delta_5}{6L_s} + \frac{\left(\frac{1}{3}V_{in} - NV_{out}\right)T_{sw}\left(\frac{1}{2} - \delta_5\right)}{2(N^2 L_1 + L_s)} \\
I_{Ls}(t_1) &= I_{dc,Ls} - \frac{V_{in}T_{sw}\delta_5}{6L_s} + \frac{\left(\frac{1}{3}V_{in} - NV_{out}\right)T_{sw}\left(\frac{1}{2} - \delta_5\right)}{2(N^2 L_1 + L_s)} \\
I_{Ls}(t_2) &= I_{dc,Ls} - \frac{V_{in}T_{sw}\delta_5}{6L_s} - \frac{\left(\frac{1}{3}V_{in} - NV_{out}\right)T_{sw}\left(\frac{1}{2} - \delta_5\right)}{2(N^2 L_1 + L_s)} \\
I_{Ls}(t_5) &= I_{dc,Ls} + \frac{V_{in}T_{sw}\delta_5}{6L_s} - \frac{\left(\frac{1}{3}V_{in} - NV_{out}\right)T_{sw}\left(\frac{1}{2} - \delta_5\right)}{2(N^2 L_1 + L_s)}
\end{align*}
\] (2.13)

Consequently, the output power \((P_o)\) is derived, and it is controlled by changing the switching frequency \((f_{sw})\). \(P_o\) can be calculated as

\[
P_o = \frac{W_o}{T} = \frac{\int_0^{T_{sw}} V_{Ls}^2 dt}{T} = \left[\frac{V_{in}^2}{9L_s} - \frac{(V_{in}^2 - 3N\cdot V_{in} \cdot V_{out})}{9(N^2 L_1 + L_s)}\right] \cdot \left(\frac{1}{2} - \delta_5\right) \cdot \delta_5 \cdot \frac{1}{f_{sw}}.
\] (2.14)

In the buck mode, the ZVS criteria for \(S_1\) and \(S_2\) are:

\[
\begin{align*}
I_{Ls}(t_6) &> 0 \\
I_{Ls}(t_2) &< 0
\end{align*}
\] (2.15)
The ZCS on and off of $S_3$ and $S_4$ can be achieved, by applying sufficient $L_s$ to suppress the slew rate of the current transferring between $S_3$ and $S_4$ during $T_{sw\delta}$. However, large $L_s$ will limit the converter’s output power capability, and cause voltage overshoots on the switches due to the resonance between $L_s$ and the output capacitance of the switches.

2.2.5. *Boost-mode, Soft-switching Operation Principles and Criteria*

Fig. 2.9 shows the major operation waveforms of the boost-mode, soft-switching operation. In the boost mode, the duty ratios of $S_1$ and $S_2$ are fixed at 50%. The duty ratios of $S_3$ and $S_4$ need be extended over 50%, to create on-state intervals overlapped with those of $S_1$ and $S_2$ (i.e., the $t_2$-$t_4$ and $t_5$-$t_7$ intervals in Fig. 2.9). In the overlapped intervals, the transformer leakage inductance stores and releases energy which is required for boost-mode power delivery.

![Figure 2.9. Boost-mode, soft-switching operation waveforms of the isolated QSC PWM converter.](image-url)
Similarly, in the boost mode operation, the voltage and current of $L_s$ during one switching cycle can be analyzed, and based on those information the converter output power in the boost mode operation can be derived as

$$P_o = \left[\frac{(V_{out}^2 - 3NV_{in}V_{out})}{9(N^2L_1 + L_s)} - \frac{V_{out}^2}{9L_s}\right] \cdot \left(1 - \delta_6\right) \cdot \delta_6 \cdot \frac{1}{f_{sw}}.$$ \hspace{1cm} (2.16)

where $\delta_6$ is

$$\delta_6 = \frac{(V_{out} - 3N\cdot V_{in}) \cdot N^2L_1 - 3N \cdot V_{in} \cdot (N^2L_1 + L_s)}{2[3N \cdot V_{in} \cdot (N^2L_1 + L_s) + (V_{out} - 3N \cdot V_{in}) \cdot N^2L_1]}.$$ \hspace{1cm} (2.17)

The ZVS criteria for $S_1$ and $S_2$ in the boost-mode operation are derived in a similar way to that of the buck mode, and can be written as:

$$\begin{cases} I_{Ls}(t_1) > 0 \\
I_{Ls}(t_4) < 0 \end{cases}.$$ \hspace{1cm} (2.18)

### 2.3. Design Guidelines for the Key Circuit Parameters

#### 2.3.1. Capacitance of $C_2$ and $C_3$

A simplified method is presented here to estimate the capacitance of $C_2$ and $C_3$, based on the allowable voltage ripple and the peak current of the two capacitors. The interval $t_5$-$t_6$ of the buck-mode, soft-switching operation is studied, because the current of $C_2 (i_{C2})$ reaches its peak value at $t_6$, and the voltage fluctuation across $C_2$ is maximum during this interval. Assuming $i_{C2}$ is constant and it is equal to $I_{Ls}(t_6)/2$ throughout the interval, and the ripple of $V_{C2}$ is 5%, the capacitance of $C_2$ and $C_3$ is calculated as
\[ C_2 = C_3 = \int_{t_5}^{t_6} i_{C_2} \cdot dt = \frac{(3 - 6\delta_5) \cdot T_{sw} \cdot I_{Ls}(t_6)}{4 \cdot V_{in} \cdot 5\%}. \] (2.19)

To help understand, an example is presented here. If \( f_s = 500 \text{ kHz}, \ V_{in} = 300 \text{ V}, \ V_{out} = 12 \text{ V}, \ N = 8/3, \ L_1 = 3.5 \ \mu \text{H}, \ L_s = 0.5 \ \mu \text{H}, \) the calculated result is \( C_2 = C_3 = 2.56 \ \mu \text{F}. \)

2.3.2. **Transformer Dc-bias Flux Density**

The transformer dc-bias flux density, together with the flux swing, decides whether the core will be saturated. Although the major part of the dc-offset current generated from the primary-side QSC dc/ac circuit is shifted from \( L_m \) to \( L_1 \) and \( L_2 \), there still exists some residual dc-offset current in \( L_m \) (\( I_{dc_{-}Lm} \)), which is

\[ I_{dc_{-}Lm} = I_{dc_{-}Ls} \frac{N^2(1 + L_2)}{N^2(1 + L_2) + L_m}. \] (2.20)

Accordingly, the dc-bias flux density of \( L_m \) (\( B_{dc_{-}Lm} \)) can be calculated as

\[ B_{dc_{-}Lm} = \frac{N_1 I_{dc_{-}Lm} \mu_\mu_0}{I_e}, \] (2.21)

where \( N_1 \) is the number of turns on the HV-side; \( \mu_0 \) is the absolute permeability; \( \mu_r \) is the relative permeability of the material; \( I_e \) is the effective length of the magnetic path.

2.3.3. **Average Currents of \( L_1 \) and \( L_2 \)**

In the proposed converter, \( L_1 \) and \( L_2 \) have unbalanced average currents because of the dc-offset current generated from the primary-side QSC dc/ac circuit. Consider the buck-
mode operation for example, following the reference directions of \( L_1 \) and \( L_2 \) signified in Fig. 5, the average currents of \( L_1 \) and \( L_2 \) (\( I_{dc\_L1} \) and \( I_{dc\_L2} \)) are written as

\[
\begin{align*}
I_{dc\_L1} &= \frac{1}{2} I_{\text{Load}} - NI_{dc\_Ls} \frac{L_m}{N^2(L_1 + L_2) + L_m} \\
I_{dc\_L2} &= \frac{1}{2} I_{\text{Load}} + NI_{dc\_Ls} \frac{L_m}{N^2(L_1 + L_2) + L_m},
\end{align*}
\]

(2.22)

where \( I_{\text{Load}} \) is the load current in the buck-mode operation.

### 2.4. Simulation Verification, Prototype Design and Experimental Results

#### 2.4.1. Simulation Verifications

A simulation model is built in PSIM to verify the circuit analysis. For the buck-mode operation, the simulation parameters are listed in Table 2.1. The on-resistance and the body-diode forward voltage of the MOSFETs are set according to the datasheets. In order to simply the analysis, the parasitic capacitance and parasitic inductance are not included in the simulation model. Fig. 2.10 shows the buck-mode, hard-switching steady-state simulation waveforms at \( P_o=1 \) kW (\( R_{\text{Load}}=0.144 \) Ω).

<table>
<thead>
<tr>
<th>( V_{in} )</th>
<th>( V_{out} )</th>
<th>( C_2 ), ( C_3 )</th>
<th>( C_4 )</th>
<th>( L_1, L_2 )</th>
<th>( L_s )</th>
<th>( L_m )</th>
<th>( N )</th>
<th>( f_{\text{sw}} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>300 V</td>
<td>12 V</td>
<td>11 μF</td>
<td>30 μF</td>
<td>3.5 μH</td>
<td>0.5 μH</td>
<td>450 μH</td>
<td>8:3</td>
<td>500 kHz</td>
</tr>
</tbody>
</table>
Figure 2.10. Steady-state simulation waveforms of the buck-mode, hard-switching operation of the isolated QSC PWM converter.

The aforementioned simulation model is used to verify the boost-mode operation capability. The simulation parameters are listed in Table 2.2. In the boost-mode operation simulation, the $N$ is changed to 8:2, and the $f_{sw}$ is changed to 300 kHz, while all other converter parameters remain the same. The LV side is powered by a voltage source, and the HV side is loaded with a resistor. Fig. 2.11 shows the boost-mode operation steady-state simulation waveforms at $\delta=0.08$ and $P_o=1$ kW ($R_{load}=90$ $\Omega$).

<table>
<thead>
<tr>
<th>$V_{in}$</th>
<th>$V_{out}$</th>
<th>$C_2$, $C_3$</th>
<th>$C_4$</th>
<th>$L_1$, $L_2$</th>
<th>$L_s$</th>
<th>$L_m$</th>
<th>$N$</th>
<th>$f_{sw}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>12 V</td>
<td>300 V</td>
<td>11 $\mu$F</td>
<td>30 $\mu$F</td>
<td>3.5 $\mu$H</td>
<td>0.5 $\mu$H</td>
<td>450 $\mu$H</td>
<td>8:2</td>
<td>300 kHz</td>
</tr>
</tbody>
</table>
The simulation results show that: 1) the voltage stresses on $S_1$ and $S_2$ are reduced to $2/3$ of the HV-dc-bus voltage; 2) the voltage stress on the transformer HV-side winding is reduced to $1/3$ of the HV-dc-bus voltage; 3) $S_1$ and $S_2$ operate in hard switching in Fig. 2.11; 4) $S_3$ and $S_4$ have reduced switching loss because of the low slew rate of switching currents; 5) the dc-offset current in $L_m$ is very small, and the unbalanced average currents in $L_1$ and $L_2$ match the analysis.

2.4.2. Prototype Design and Test Descriptions

A 1 kW prototype is built, as shown in Fig. 2.12. The specifications of the prototype are shown in Table 2.3. In the primary-side QSC dc/ac circuit, the CREE Silicon Carbide (SiC) MOSFET (CMF20120D) is applied for $S_1$ and $S_2$. In the secondary-side current-
doubler rectifier circuit, because of the high current rating, two Infineon Si OptiMOS (IPP075N15N3) FETs are applied in parallel for both $S_3$ and $S_4$.

![Diagram](image)

Figure 2.12. 1 kW prototype of the isolated QSC PWM converter.

Table 2.3. Specifications of the 1 kW prototype of the isolated QSC PWM converter.

<table>
<thead>
<tr>
<th>Item</th>
<th>Descriptions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ratings</td>
<td>$V_{HV}=300-400$ V, $V_{LV}=12$ V, $P_{out}=1$ kW, $f_s=500$ kHz</td>
</tr>
<tr>
<td>$S_1$, $S_2$</td>
<td>SiC MOSFETs (CREE CMF20120D)</td>
</tr>
<tr>
<td>$S_3$, $S_4$</td>
<td>Si OptiMOS FETs (Infineon IPP075N15N3)</td>
</tr>
<tr>
<td>Planar Transformer</td>
<td>$N=8:2$, $L_m=450$ µH, $L_s=0.8$ µH for the buck mode, $N=8:2$, $L_m=450$ µH,</td>
</tr>
<tr>
<td></td>
<td>$L_s=0.5$ µH for the boost mode.</td>
</tr>
<tr>
<td>Planar Inductors</td>
<td>$L_1=L_2=3.5$ µH</td>
</tr>
<tr>
<td>Capacitors</td>
<td>$C_2=C_3=11$ µF/450 V</td>
</tr>
</tbody>
</table>

The planar transformer is built with no air gap. Two planar inductors were built for $L_1$ and $L_2$. The core selected for the transformer and inductors is ER41/7.6/32-3F3. For $C_2$ and
2.2-µF/250-Vdc ceramic capacitors are selected, and \( C_2 = C_3 = 11 \mu F \). In the testing, a 800-µF film capacitor is added on the HV-dc-bus, and a 220-µF film capacitor is added on the LV-dc-bus. This setup is valid for the scenario of HEVs/EVs applications, where both the HV and LV dc buses have large capacitance.

In the experiments, power for the buck-mode test is provided by a Magna DC Power Supply TSA800-6, and power for the boost-mode test is provided by a NHR 9200 battery test system. Resistor banks are used as the load. The control is implemented with a Texas Instrument digital signal processor (DSP) (TMS320F2808). Test waveforms are recorded with two Tektronix oscilloscopes, and the efficiency is measured using a Yokogawa WT3000 power meter with a LEM Danfysik IT 700-S current transducer on the LV-side and an external current-shunt resistor on the HV-side.

2.4.3. Experimental Results

Fig. 2.13 (a) shows the experimental waveforms of the buck-mode, hard-switching operation, at the operation point where \( f_S = 500 \) kHz, \( V_{in} = 300 \) V, \( V_{out} = 12 \) V, and \( P_o = 971 \) W. Fig. 2.13 (b) shows the experimental waveforms of the boost-mode operation, at the operation point where \( f_S = 500 \) kHz, \( V_{in} = 12 \) V, \( V_{out} = 300 \) V, and \( P_o = 1016 \) W. It can be seen from Fig. 2.13 that: 1) the steady-state voltage stresses on \( S_1 \) and \( S_2 \) are reduced to 2/3 of the HV-dc-bus voltage; 2) the steady-state voltage stress on the transformer HV-side winding is reduced to 1/3 of the HV-dc-bus voltage; 3) hard-switching is resulted in the buck-mode because the deadband makes \( I_{Ls} \) discontinuous; 4) during the deadband, resonance exists between the transformer leakage inductance and the parasitic capacitance.
of the switches. The resonance causes circulating current, voltage ringing on the switches, EMI issues, and extra power loss.

![Waveform Diagram](image)

**Figure 2.13.** (a) Experimental results of the buck-mode, hard-switching operation, (b) Experimental results of the boost-mode, soft-switching operation.

Soft-switching operation is preferred to improve the efficiency and alleviate the aforementioned resonance. For the testing of the buck-mode, soft-switching operation: 1) a fixed 50% duty ratio with necessary deadband is applied for $S_1$ and $S_2$ to prevent shoot-through; 2) the output voltage is fixed at 12 V, and the output power increases with the input voltage. Fig. 2.14 show the experimental waveforms at the buck-mode, soft-switching operation point where $f_s=500$ kHz, $V_{in}=350$ V, $V_{out}=12$ V, $P_o=939$ W. It can be seen from Fig. 2.14 that the reduced voltage stresses on the switches and the transformer are achieved, and ZVS on is achieved for both $S_1$ and $S_2$. In addition, Fig. 2.14 (a) shows that average current of $L_s$ is 3.35 A, and the transient ratio $\delta$ is 0.083. Both of these values matched the analysis.
Figure 2.14. Experimental results of the buck-mode, soft-switching operation. (a) Drain-to-source voltages of $S_1$ and $S_2$, the voltage and current of the transformer HV-side winding, (b) Gate signals and drain-to-source voltages of $S_1$ and $S_2$.

Fig. 2.15 shows the drain-to-source voltages of $S_1$, $S_2$, $S_3$ and $S_4$ at: (a) the buck-mode, soft-switching operation point where $f_S=500$ kHz, $V_{in}=350$ V, $V_{out}=12$ V, and $P_o=939$ W; and (b) the boost-mode, soft-switching operation point where $f_S=500$ kHz, $V_{in}=12$ V, $V_{out}=280$ V, and $P_o=1046$ W.

It can be seen from Fig. 2.15 that: 1) between the off states of $S_3$ and $S_4$, there exists about 100 ns transient which reduces the switching loss of $S_3$ and $S_4$; 2) the ringing and voltage overshoot of $V_{DS(S3)}$ and $V_{DS(S4)}$ are caused by the resonance between the transformer leakage inductance and the parasitic capacitance of $S_3$ and $S_4$. To protect $S_3$ and $S_4$ from breakdown damage, RCD snubbers are added to $S_3$ and $S_4$, which introduces extra power loss.
Figure 2.15. Experimental drain-to-source voltage waveforms of $S_1$, $S_2$, $S_3$ and $S_4$ in the (a) buck-mode, soft-switching operation, and (b) boost-mode, soft-switching operation.

The efficiency curves of the converter with unfixed HV-dc-bus voltage in testing are shown in Fig. 2.16 (a), and the hard-switching efficiency curves of the 1 kW prototype with fixed HV-dc-bus voltages in testing are shown in Fig. 2.16 (b).

Figure 2.16. (a) Efficiency curves with unfixed HV-dc-bus voltage. (b) Hard-switching operation efficiency curves with fixed HV-dc-bus voltages. Continued
Fig. 2.16 (a) showcases the converter’s potential to achieve high efficiency with soft switching. The efficiency curves in Fig. 2.16 (b) are not optimized, since the design is not optimized and the converter operates in hard switching. However, it can be improved by better tuning of the circuit parameters, improving the circuit layout to reduce the circuit parasitic inductance, applying better magnetic component design and better control.

2.5. Conclusions

In this chapter, a QSC dc/ac circuit is proposed to replace the traditional half/full-bridge dc/ac circuits in isolated dc/dc power converters. The circuit combines a transformer and two switched capacitors, and therefore have the following features:

1) The voltage stresses on the switches are reduced to 2/3 of the dc-bus voltage;
2) The voltage stress on the transformer is reduced to 1/3 of the dc-bus voltage, and thus the transformer turns ratio is reduced by 2/3;

3) ZVS on can be achieved for all the switches;

4) A steady-state dc-offset current flows through the transformer.

Based on the QSC dc/ac circuit, an isolated QSC PWM converter is proposed, to serve as an auxiliary power supply in EVs/HEVs, managing a bidirectional power flow between the HV battery and the LV dc bus. The converter operation principle, soft-switching analysis, and simulation verification are presented. The features of the reduced voltage stress on the switches and the transformer are verified, and the dc-offset current in the transformer magnetizing inductance is minimized. Guidelines are given to estimate the key circuit parameters, including the capacitance of the switched capacitors, the transformer dc-bias flux density, and the average currents of the post-stage inductors.

WBG devices are selected for the proposed converter in order to shrink the size of passive components, provide high efficiency, and decrease the cooling requirement. A 1-kW prototype is built with SiC MOSFETs on the primary side and Si MOSFETs on the secondary side. The soft-switching peak efficiency of the converter operating at 500 kHz switching frequency is 96% for the buck-mode operation, and 91% for the boost-mode operation. The advantage of reduced voltage stresses makes the proposed isolated QSC PWM converter attractive to low-voltage rated switches, which are more efficient because of better figure of merit. Additionally, advantages of the new converter including reduced transformer turns ratio, reduced device count, high voltage transfer ratio, high efficiency,
and less control needs, make the proposed converter promising for high power applications with high power density.
Chapter 3. Small-signal Model and Controller Design of the Isolated QSC PWM Converter

3.1. Control Method Descriptions

To regulate the output voltage of the proposed isolated QSC PWM converter, the duty-ratio control, switching-frequency control, and the phase-shift control are considered as standard approaches [94-100]. The switching frequency control keeps a fixed duty ratio of 50% for HV-side switches, but regulates the converter’s output power by modulating the switching frequency. This control technique is essentially adjusting the duration of the switching intervals, and it enables soft switching over a wide load power range [96].

For resonant-type converters where switching frequency is used to control the output voltage, the methods based on Extended Describing Functions (EDFs) are used to derive the transfer functions in [101-104]. These methods are applicable for resonant-type converters rather than PWM converters. The reason is that, the ratio of the switching period to the system time constants is typically small for fast switching PWM converters, but not for resonant type converters [105-106]. In resonant-type converters the ac behavior is dominant [107]; however, in PWM converters, with the small ripple approximation, the Fourier series expansion for a finite length segment of a circuit waveform should be dominated by its dc term [106]. The state-space averaging method, whose basic principle is introduced in [108-109], is applied in the small-signal modeling of PWM converters in [110-
In this chapter, the small-signal model of the isolated QSC PWM converter in buck-mode operation is derived with the state-space averaging method. A closed-loop voltage controller with feed-forward compensation for the switching frequency is designed to improve the dynamic performance.

3.2. Small-signal Model of the Isolated QSC PWM Converter

3.2.1. Switching-mode Equivalent Circuit Descriptions and Small-signal Modeling

As shown in Fig. 2.8, the isolated QSC PWM converter in soft-switching, buck-mode, steady-state operation has 6 switching modes within one switching cycle ($T_{sw}$). These 6 switching modes are mapped into 4 switching-mode equivalent circuits, as shown in Fig. 3.1-Fig. 3.4. The HV-side current of the transformer ($i_{Ls}$), the currents of the post-stage inductors ($i_{L1}$ and $i_{L2}$), the voltage of the switched capacitor ($v_{C3}$), and the LV-dc-bus voltage ($v_{C4}$) are defined as state variables, which can be written as a vector

$$x(t) = \begin{bmatrix} i_{Ls}(t) \\ i_{L1}(t) \\ i_{L2}(t) \\ v_{C3}(t) \\ v_{C4}(t) \end{bmatrix}. \quad (3.1)$$

The differential equations that describe the system can be written as

$$K \cdot \dot{x}(t) = \begin{bmatrix} L_s & 0 & 0 & 0 & 0 \\ 0 & L_1 & 0 & 0 & 0 \\ 0 & 0 & L_2 & 0 & 0 \\ 0 & 0 & 0 & C_3 & 0 \\ 0 & 0 & 0 & 0 & C_4 \end{bmatrix} \cdot \frac{d}{dt} \begin{bmatrix} i_{Ls}(t) \\ i_{L1}(t) \\ i_{L2}(t) \\ v_{C3}(t) \\ v_{C4}(t) \end{bmatrix} = A_n \cdot \begin{bmatrix} i_{Ls}(t) \\ i_{L1}(t) \\ i_{L2}(t) \\ v_{C3}(t) \\ v_{C4}(t) \end{bmatrix} + B_n \cdot v_{in}(t) + D_n \cdot i_{out}(t),$$

where $K$ is the state-space matrix, $A_n$ is the coefficient matrix, $B_n$ is the input matrix, and $D_n$ is the direct-current matrix.
Fig. 3.1 shows the 1st switching-mode equivalent circuit of the converter during the interval $t_4-t_1$.

The matrices describing the 1st switching-mode equivalent circuit are

$$A_1 = \begin{bmatrix} 0 & 0 & 0 & 2 & 0 \\ 0 & 0 & 0 & 0 & -1 \\ 0 & 0 & 0 & 0 & -1 \\ -1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 1 & 0 & -\frac{1}{R} \end{bmatrix}, \quad B_1 = \begin{bmatrix} -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix}, \quad D_1 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 \end{bmatrix}. \quad (3.2)$$

Fig. 3.2 shows the 2nd switching-mode equivalent circuit of the converter during the interval $t_1-t_2$, with all the components referred to the HV side.

The matrices describing the 2nd switching-mode equivalent circuit are
\[
A_2 = \begin{bmatrix}
0 & 0 & \frac{2L_s}{N^2L_1 + L_s} & 0 \\
0 & 0 & -\frac{2NL_1}{N^2L_1 + L_s} & 0 \\
0 & 0 & \frac{-1}{N^2L_1 + L_s} & 0 \\
0 & \frac{1}{N} & 0 & -\frac{1}{R}
\end{bmatrix},
B_2 = \begin{bmatrix}
-\frac{L_s}{N^2L_1 + L_s} & 0 & 0 & 0 \\
\frac{NL_1}{N^2L_1 + L_s} & 0 & 0 & 0 \\
0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0
\end{bmatrix},
\]

\[
D_2 = \begin{bmatrix}
0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 \\
-1 & 0 & 0 & 0
\end{bmatrix}.
\]

Fig. 3.3 shows the 3\textsuperscript{rd} switching-mode equivalent circuit of the converter during the interval \(t_2-t_3\).

\[
D_3 = \begin{bmatrix}
0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 \\
-1 & 0 & 0 & 0
\end{bmatrix}.
\]

The matrices describing the 3\textsuperscript{rd} equivalent circuit are

\[
A_3 = \begin{bmatrix}
0 & 0 & 0 & 1 & 0 \\
0 & 0 & 0 & 0 & -1 \\
0 & 0 & 0 & 0 & -1 \\
-\frac{1}{2} & 0 & 0 & 0 & 0 \\
0 & 1 & 1 & 0 & -\frac{1}{R}
\end{bmatrix},
B_3 = \begin{bmatrix}
0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0
\end{bmatrix},
D_3 = \begin{bmatrix}
0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 \\
-1 & 0 & 0 & 0
\end{bmatrix}.
\]
Fig. 3.4 shows the 4th switching-mode equivalent circuit of the converter during the interval \( t_3-t_4 \).

![Figure 3.4. The 4th switching-mode equivalent circuit during the interval \( t_3-t_4 \).](image)

The matrices describing the 4th equivalent circuit are

\[
A_4 = \begin{bmatrix}
0 & 0 & 0 & -\frac{N L_s}{N^2 L_2 + L_s} \\
0 & 0 & 0 & -\frac{N L_s}{N^2 L_2 + L_s} \\
0 & 0 & 0 & 0 \\
0 & 0 & -\frac{1}{2N} & 0 \\
0 & 1 & 1 & -\frac{1}{R}
\end{bmatrix},
\]

\[
B_4 = \begin{bmatrix}
0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0
\end{bmatrix},
\]

\[
D_4 = \begin{bmatrix}
0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 \\
-1 & 0 & 0 & 0
\end{bmatrix}.
\] (3.6)

As shown in Fig. 2.8, in one switching cycle, the duration of both the 1st and the 3rd switching-mode equivalent circuits is \( \delta_5 T_{sw} \), and the duration of both the 2nd and the 4th switching-mode equivalent circuits is \((0.5-\delta_3)T_{sw}\). In the isolated QSC PWM, the ratio \( \delta_5 \) works as the duty ratio of traditional PWM converters. The control method is essentially
adjusting the duration of the switching intervals. The $\delta_s$ is adjusted indirectly by changing the switching frequency $f_{sw}$, according to equations (2.12) and (2.14). Therefore, the ratio $\delta_s$ is selected as the control variable in the modeling, whereas the $f_{sw}$ still contributes to the dc term of the output voltage.

Introduce the disturbance

$$< x(t) >_{T_s} = X + \hat{x}(t),$$

$$< v_{in}(t) >_{T_s} = V_{in} + \hat{v}_{in}(t),$$

$$< \delta_s(t) >_{T_s} = D + \hat{\delta}_s(t),$$

$$< i_{out}(t) >_{T_s} = \hat{i}_{out}(t).$$

(3.7)

where $X = [I_{ls} I_{l1} I_{l2} V_{c3} V_{c4}]^T$, which are the steady-state dc terms of the state variables that can calculated according to Chapter 2; $D$ is the steady-state dc term of $\delta_s$, which can be calculated based on (2.12) and (2.14); and $V_{in}$ is the steady-state dc term of the input voltage.

The ac small-signal (linear) state equation is derived as

$$K \cdot \frac{d \hat{x}(t)}{dt} = \left[ D \cdot \left( A_1 + A_3 \right) + \left( \frac{1}{2} - D \right) \cdot \left( A_2 + A_4 \right) \right] \cdot \hat{x}(t) + \left[ D \cdot B_1 + \left( \frac{1}{2} - D \right) \cdot B_2 \right] \cdot \hat{v}_{in}(t)$$

$$+ \left[ \left( A_1 + A_3 \right) \cdot \left( A_2 + A_4 \right) \right] \cdot X + \left[ B_1 - B_2 \right] \cdot \hat{\delta}_s(t) + D_1 \cdot \hat{i}_{out}(t)$$

(3.8)

The ac small-signal model of the isolated QSC PWM converter is described in equation group (3.9).
\[
\begin{align*}
sL_s \cdot i_{L_s}^\wedge (s) &= \lambda_1 \cdot v_{C3}^\wedge (s) - \frac{\lambda_1}{3} \cdot v_{in}^\wedge (s) \\
sL_1 \cdot i_{L_1}^\wedge (s) &= -2\lambda_2 \cdot v_{C3}^\wedge (s) - \lambda_4 \cdot v_{C4}^\wedge (s) \\
&\quad + \lambda_2 \cdot v_{in}^\wedge (s) + \lambda_5 \cdot \delta^\wedge (s) \\
sL_2 \cdot i_{L_2}^\wedge (s) &= \lambda_2 \cdot v_{C3}^\wedge (s) - \lambda_4 \cdot v_{C4}^\wedge (s) + \lambda_5 \cdot \delta^\wedge (s) \\
sC_3 \cdot v_{C3}^\wedge (s) &= -\frac{3}{2} \delta^\wedge (s) \cdot i_{L_s}^\wedge (s) + 2\lambda_3 \cdot i_{L_1}^\wedge (s) \\
&\quad - \lambda_3 \cdot i_{L_2}^\wedge (s) - \lambda_6 \cdot \delta^\wedge (s) \\
sC_4 \cdot v_{C4}^\wedge (s) &= i_{L_1}^\wedge (s) + i_{L_2}^\wedge (s) - \frac{1}{R} \cdot v_{C4}^\wedge (s) - i_{out}^\wedge (s) 
\end{align*}
\]

where

\[
\begin{align*}
\lambda_1 &= 3D + \frac{3L_s (0.5 - D)}{N^2 L_1 + L_s} \\
\lambda_2 &= \frac{NL_1 (0.5 - D)}{N^2 L_1 + L_s} \\
\lambda_3 &= \frac{1}{2N} (0.5 - D) \\
\lambda_4 &= \frac{1}{2} + D + N\lambda_2 \\
\lambda_5 &= -\frac{NL_1}{N^2 L_1 + L_s} \cdot \frac{V_{in}}{3} - \frac{L_s}{N^2 L_1 + L_s} \cdot V_{C4} \\
\lambda_6 &= \frac{3}{2} \cdot I_{L_s} + \frac{1}{N} \cdot I_{L_1} - \frac{1}{2N} \cdot I_{L_2}
\end{align*}
\]

Based on the derived small-signal model, the response of the state variable can be expressed as a linear combination of each perturbation. In particular, the transfer function of \( v_{C4} \) can be derived from (3.9) as

\[
v_{C4}^\wedge (s) = G_{v_{in}} (s) \cdot v_{in}^\wedge (s) + G_{v_{s}} (s) \cdot \delta^\wedge (s) - Z_{out}^\wedge (s) \cdot i_{out}^\wedge (s),
\]

(3.10)
where the input-to-output transfer function $G_{\text{vg}}(s)$ is

$$G_{\text{vg}}(s) = \frac{s^2 \lambda_2 C_3 L_1 + 3 \lambda_3 \lambda'_2 + \frac{\lambda_1 \lambda_4 \delta L_1}{L_s}}{s^4 C_4 C_3 L_1^2 + s^3 \frac{C_3 L_1^2}{R} + s^2 \left( \frac{3 \lambda_4 \delta C_4 L_1^2}{2L_s} + 5 \lambda_3 \lambda_2 C_4 L_1 + 2 \lambda_4 C_3 L_1 \right) + s L_1 \left( \frac{3 \lambda_4 \delta L_1}{2L_s} + 5 \lambda_3 \lambda_2 \right) + 9 \lambda_3 \lambda_4 \lambda_2 + \frac{6 \lambda_1 \lambda_4 \delta L_1}{2L_s}}$$

(3.11)

the control-to-output transfer function $G_{\text{vo}}(s)$ is

$$G_{\text{vo}}(s) = \frac{s^2 2 \lambda_4 C_3 L_1 + s \lambda_2 \lambda_4 L_1 + \frac{3 \lambda_3 \lambda'_4}{L_s} - 9 \lambda_3 \lambda_2 \lambda_5}{s^4 C_4 C_3 L_1^2 + s^3 \frac{C_3 L_1^2}{R} + s^2 \left( \frac{3 \lambda_4 \delta C_4 L_1^2}{2L_s} + 5 \lambda_3 \lambda_2 C_4 L_1 + 2 \lambda_4 C_3 L_1 \right) + s L_1 \left( \frac{3 \lambda_4 \delta L_1}{2L_s} + 5 \lambda_3 \lambda_2 \right) + 9 \lambda_3 \lambda_4 \lambda_2 + \frac{6 \lambda_1 \lambda_4 \delta L_1}{2L_s}}$$

(3.12)

and the output impedance $Z_{\text{out}}(s)$ is

$$Z_{\text{out}}(s) = \frac{s^3 C_1 L_1^2 + s \left( \frac{3 \lambda_4 \delta L_1^2}{2L_s} + 5 \lambda_3 \lambda_2 L_1 \right)}{s^4 C_4 C_3 L_1^2 + s^3 \frac{C_3 L_1^2}{R} + s^2 \left( \frac{3 \lambda_4 \delta C_4 L_1^2}{2L_s} + 5 \lambda_3 \lambda_2 C_4 L_1 + 2 \lambda_4 C_3 L_1 \right) + s L_1 \left( \frac{3 \lambda_4 \delta L_1}{2L_s} + 5 \lambda_3 \lambda_2 \right) + 9 \lambda_3 \lambda_4 \lambda_2 + \frac{6 \lambda_1 \lambda_4 \delta L_1}{2L_s}}$$

(3.13)

### 3.2.2. Simulation Verifications of the Small-signal Model

To verify the derived small-signal model, analysis results based on (3.10) are compared with the simulation results from a detailed circuit. To study the open-loop system response to an input voltage disturbance, a small-signal model based on the derived transfer functions is built in Matlab with the circuit parameters listed in Table 3.1 and a detailed circuit model is built in PSIM with the same circuit parameters listed
in Table 3.1. The input voltage steps from 300 V to 350 V, and the simulation results from the two models are presented and compared in the same plot in Fig. 3.5.

Table 3.1. Circuit parameters for the open-loop simulation of the isolated QSC PWM converter in response to a input voltage disturbance.

<table>
<thead>
<tr>
<th>$f_s$</th>
<th>$V_{C4}$</th>
<th>$C_2$, $C_3$</th>
<th>$C_4$</th>
<th>$L_1$, $L_2$</th>
<th>$L_s$</th>
<th>$R$</th>
<th>$N$</th>
</tr>
</thead>
<tbody>
<tr>
<td>500 kHz</td>
<td>12 V</td>
<td>11 µF</td>
<td>60 µF</td>
<td>3.5 µH</td>
<td>0.5 µH</td>
<td>0.36 Ohm</td>
<td>4</td>
</tr>
</tbody>
</table>

Figure 3.5. Open-loop simulation results from the small-signal model built in Matlab and the detailed circuit model built in PSIM in response to an input voltage disturbance.

To study the open-loop system response to a switching frequency disturbance, the aforementioned small-signal model built in Matlab and the detailed circuit model built in PSIM are assigned with the circuit parameters listed in Table 3.2. The switching frequency
steps from 300 kHz to 600 kHz, and the simulation results from the two models are compared again and shown in the same plot in Fig. 3.6.

It can be noted that the simulation results from the small-signal model are in line with those from the detailed circuit. Therefore, the small signal model is verified [105], [115-116].

Table 3.2. Circuit parameters for the open-loop simulation of the isolated QSC PWM converter in response to a switching frequency disturbance.

<table>
<thead>
<tr>
<th>$V_{in}$</th>
<th>$V_{C4}$</th>
<th>$C_2$, $C_3$</th>
<th>$C_4$</th>
<th>$L_1$, $L_2$</th>
<th>$L_s$</th>
<th>$R$</th>
<th>$N$</th>
</tr>
</thead>
<tbody>
<tr>
<td>300 V</td>
<td>12 V</td>
<td>11 µF</td>
<td>60 µF</td>
<td>3.5 µH</td>
<td>0.5 µH</td>
<td>0.36 Ohm</td>
<td>4</td>
</tr>
</tbody>
</table>

Figure 3.6. Open-loop simulation results from the small-signal model built in Matlab and the detailed circuit model built in PSIM in response to a switching frequency disturbance.
3.3. **Controller Design of the Isolated QSC DC/DC Converter**

3.3.1. **Controller Design**

It can be inferred from (2.14) and (2.14) that, the range of the $f_s$ swing in the closed-loop control can be shrunk by increasing $L_s$. A smaller range of the $f_s$ swing is preferred for the following reasons: 1) it is easier to design the transformer since the lower limit of the $f_s$ swing is determined by the transformer saturation flux density, while the upper limit of the $f_s$ swing is determined by the transformer self-resonance frequency; 2) when $f_s$ increases in light-load conditions, the increased switching loss will lead to lower efficiency.

Therefore, $L_s$ is increased for the closed-loop control verification, and the aforementioned small-signal model built in Matlab is assigned with the circuit parameters listed in Table III for analysis.

<table>
<thead>
<tr>
<th>$V_{in}$</th>
<th>$V_{C1}$</th>
<th>$C_2$, $C_3$, $C_4$</th>
<th>$L_1$, $L_2$, $L_s$</th>
<th>$R$</th>
<th>$N$</th>
</tr>
</thead>
<tbody>
<tr>
<td>300 V</td>
<td>12 V</td>
<td>11 µF, 300 µF</td>
<td>3.5 µH, 2.8 µH, 0.245 Ohm</td>
<td>8/3</td>
<td></td>
</tr>
</tbody>
</table>

Using the circuit parameters listed in Table 3.3, the pole-zero maps of the transfer functions $G_{v_1}(s)$ and $G_{v_0}(s)$ are plotted in Fig. 3.7. It can be seen from Fig. 3.7 that: 1) the system is stable since there is no right-half-plane (RHP) pole; 2) the $G_{v_0}(s)$ has a pair of RHP zeros, which indicates that the system is a non-minimum-phase system. Because of this pair of RHP zeros, the system dynamic response may be limited; 3) a pair of left-half-plane (LHP) poles is located very close to the imaginary axis, which means that the system
doesn’t have enough damping to suppress the input voltage disturbance, and the oscillation may occur.

Figure 3.7. Pole-zero maps of the transfer functions: (a) $G_{vq}(s)$, and (b) $G_{vI}(s)$.

Based on the previous analysis, a closed-loop voltage controller with feed-forward compensation for the switching frequency is proposed. The control purpose is to stabilize the output voltage. Because of feed-forward loop, the performance of the input voltage disturbance rejection can be greatly improved [115] [117]. The control structure of the isolated QSC PWM converter is shown in Fig. 3.8.
Inside the control plant, the function $G_\delta$ updates the ratio $\delta_5$, based on (2.12). The function $G_v$ generates part of the dc term ($V_{C4,f}$) of $v_{C4}$. It is derived based on (2.12) and (2.14), and expressed as

$$G_v = V_{C4,f} = \frac{-b + \sqrt{b^2 - 4ac}}{2a}, \quad (3.14)$$

where

$$\begin{cases}
a = 18NL_s^2 f_s \\
b = 6N^2 L_s L_1 f_s V_{in} + (6N^4 L_1 + 3N^2 L_s V_{in} R) \\
c = -V_{in}^2 N^3 L_1 R
\end{cases}$$
Outside the control plant, the function $G_f$ generates a feed-forward-compensation switching frequency $f_{FF}$, based on the input voltage and the reference output voltage. It is derived from the equation (2.14), and expressed as:

$$
G_f = f_{FF} = \left[ \frac{V_{in}^2}{9L_s} - \frac{(V_{in}^2 - 3NV_{in}V_{C4}^*)}{9(N^2L_1 + L_s)} \right] \cdot \left( \frac{1}{2} - \delta \right) \cdot \delta \cdot \frac{R}{V_{C4}^*}.
$$

(3.15)

where $V_{C4}^*$ is the reference output voltage.

The frequency-to-output transfer function $G_v(s)$ is not successfully derived, because the input voltage $v_{in}$ and switching frequency $f_s$ are not fully decoupled in the generation of the $\delta$, as shown in (2.14) and Fig. 3.8. So the PI compensator $G_c(s)$ is not designed based on the $G_v(s)$, but instead it is designed by the trail-and-error method, which is a common practice in industry. In the $G_c(s)$, increasing $K_p$ will add more damping into the system, and the response time will be reduced. However, a large $K_p$ might cause stability issue, because of the presence of the RHP zeroes in the $G_v(s)$. On the other hand, increasing $K_i$ will reduce the response time, but cause more ringing.

### 3.3.2. Closed-loop Simulation Verification

In the closed-loop control simulation, the aforementioned small-signal model built in Matlab and the detailed circuit model built in PSIM are assigned with the circuit parameters listed in Table 3.3. A 50-V step change of $v_{in}$ is introduced, and the simulation results from the two models are compared and shown in the same plot in Fig. 3.9.
Figure 3.9. Closed-loop simulation results from the small-signal model and the detailed circuit model in response to an input voltage disturbance.

To highlight the improved dynamic performance due to the feed-forward compensator, a group of simulation is conducted and compared. In the simulation, a step change in the input voltage is introduced. The open-loop response, closed-loop response with and without feed-forward compensator are compared, as shown in Fig. 3.10. The PI parameters are the same in the closed-loop simulations with and without the feed-forward compensation.
Figure 3.10. Simulation results of the open-loop response, closed-loop response with and without feed-forward compensation of the small-signal model in response to a disturbance of the input voltage.

Fig. 3.9 and Fig. 3.10 show that: 1) the closed-loop voltage control based on switching frequency regulation is realized; 2) it is proved that with the feed-forward compensation, the oscillation in the system is significantly damped and the response time is reduced. It is shown in Fig. 3.9 that there exist discrepancies between the system responses of the two models. Possible reasons for these discrepancies include that there exists parasitic circuit parameters in the detailed circuit model, the dc terms of the state variables which can be affected by $v_{in}$ are not updated in the small-signal model, and the numerical algorithms of
the software PSIM and Matlab are different since PSIM is based on the nodal analysis [118], whereas Matlab is based on the state-space analysis [119].

3.4. **Experimental Verifications**

3.4.1. **Experimental Setup Descriptions**

The 1-kW isolated QSC PWM converter prototype presented in section 2.42 is used for the experimental verifications. In the test setup, the input voltage source is a Magna dc Power Supply (TSA800-6). This power supply has limited output dynamic performance and cannot provide a fast step change in its output voltage because of its output capacitance. Also, in the prototype, there exist circuit parasitics such as the stray inductance and the stray resistance in the circuit, and these parasitics are affecting the dynamic response of converter.

The closed-loop control is implemented with a digitalized PI compensator in DSP (TMS320F2808). The diagram is shown in Fig. 3.11. The converter’s output voltage is measured using a voltage transducer which provides isolation. The sampling circuit is an analog circuit that provides signal amplification. The ADC module is the integrated in the DSP. The digital 2nd-order Butterworth filter has a cutoff frequency at 1 kHz. The \( G_c(z) \) is a discrete PI compensator. The \( f_{FF} \) is the feed-forward-compensation switching frequency. The digital pulse frequency modulation (DPFM) generates the gate signals for the power switches, with fixed 50% duty ratio but varying switching frequency. The isolators and gate drivers are the ICs that provide signal isolation and amplification for the gate driving currents.
3.4.2. Experimental Results

A closed-loop experiment with an input voltage disturbance is conducted. The initial operation conditions are as follows: $V_{in}=190$ V, $R=0.4$ Ohm, the duty ratio for the switches is 0.5 with a 70 ns deadband. A 20-V disturbance is introduced to the input voltage. The experiment results are shown in Fig. 3.12, and the zoomed-in waveforms before and after the disturbance are shown in Fig. 3.13 and Fig. 3.14.

Figure 3.11. Function blocks of the digital control implemented in DSP.

Figure 3.12. Closed-loop experiment waveforms with a 20-V input voltage step change.
The closed-loop experiment waveforms with a disturbance of the load current is shown in Fig. 3.15. The initial operation conditions are as follows: $V_{in}=150$ V, $N=8/3$, $f_s=280$ kHz for the first set of waveforms, and $V_{in}=210$ V, $f_s=500$ kHz for the second set of waveforms.
$R=0.67$ Ohm, $I_{\text{load}}=12$ A, the duty ratio for the switches is 0.5 with a 70-ns deadband. A 6-A load current disturbance is introduced when the load is suddenly reduced to $R=0.4$ Ohm.

![Diagram](image)

Figure 3.15. Closed-loop experiment waveforms with a load current step change from 12 A to 18 A.

It can be seen from Fig. 3.12-3.14 that: 1) to maintain a stable output voltage, the $f_s$ changed from 280 kHz to 500 kHz, and the closed-loop voltage control based on switching frequency regulation is verified; 2) there exists ringing in the transformer current waveform, and it is caused by the resonance between the $L_s$ and the output capacitance of $S_3$ and $S_4$. It can be seen from Fig. 3.15 that the output voltage is stabilized in spite of a load current disturbance, and the switching frequency variation is small because of the low output impedance of the converter.
3.5. **Conclusions**

In this chapter, the small-signal model and controller design of the isolated QSC PWM converter are presented. To maintain ZVS operation, the output power of the converter is regulated by the switching frequency modulation. This control method is essentially adjusting the duration of the switching intervals. A small-signal model of the converter is derived by the method of state-space averaging. Open-loop response simulation results from the derived small-signal model and a detailed circuit model are provided and compared. The simulation results showcase the effectiveness of the derived small-signal model.

For better performance of the input voltage disturbance rejection, a closed-loop voltage controller with feed-forward compensation for the switching frequency is designed to regulate the output voltage. Comparison of closed-loop simulation results from the small-signal model and the detailed circuit model verified the effectiveness of the closed-loop controller. With feed-forward compensations, the oscillation in the system can be significantly damped and the response time is reduced. Experiment results from a 1-kW prototype with digital control implemented in DSP verified the effectiveness of the closed-loop voltage control based on switching-frequency control.
Chapter 4. Isolated QSC Resonant Converter

In Chapter 2, the isolated QSC PWM converter is proposed and demonstrated. Though the turn-on loss of the converter is minimized with ZVS on, the turn-off loss still limits the capability of the converter to operate at higher switching frequency.

In this chapter, an isolated QSC resonant converter is proposed to further reduce the switching loss and thus improve the efficiency. It serves as a dc-dc transformer (DCX) in off-line power supply applications, operating in open loop at its fixed but optimal switching frequency and duty ratio.

This chapter is divided into five sections. Section 4.1 discusses the application background. Section 4.2 presents the descriptions and operation principles of the isolated QSC resonant converter. Section 4.3 presents the prototype design. Section 4.4 presents the simulation results and experimental results. Section 4.5 concludes this chapter.

4.1. Application Background

Consumer electronics (CE) such as laptops, smart-phones, and smart-pads are indispensable information-technology tools in today’s world. CE products require an external off-line ac/dc power adapter to power up the device or charge its internal battery with a universal line input. The outlook for the external ac-dc power supply market is expected to remain strong over the next several years increasing from $10.7 billion in 2014
to $14.9 billion in 2019, a compounded annual growth rate (CAGR) of 6.9% [120]. In this market, there exists ever-increasing demands for high power-density and highly energy efficient power supplies. Currently, available commercial products are based on the Silicon (Si) devices. For example, the state-of-art, Si-based, commercially available 90-W ac/dc power adapter product from AcBel is in the size of 5.27 inch$^3$, and the measured peak efficiency is 92 %. However, the growing consensus in the power electronics community is that Si devices cannot meet the needs of the future of power electronics [121-125]. This is driven by market demands for further improvements in efficiency, reduction of physical sizes, and an increase in maximum operating temperatures. The WBG power devices, such as the GaN high electron mobility transistor (HEMTs), are posed to satisfy these emerging market needs. The 3X wider bandgap of the GaN devices enable them to operate under greater voltage stress per channel length, at higher temperatures, while switching at faster speeds and causing lower power loss. All of these attributes indicate that by using GaN devices, smaller and more efficient ac/dc power adapters can be realized. For example, FINsix has announced a state-of-art, GaN-based, pre-order available 65-W ac/dc power adapter Dart, measuring 2.5 inch$^3$ and weighing 60 gram, which is 60~75% smaller than its conventional counterparts [120, 126, 127].

To maximize the benefits of GaN devices, low-voltage rating of the devices is preferred. This is because low-voltage rated devices are more efficient, as they have better figure of merits which is the product of on-resistance and total gate charge [64-65]. Currently, most power adapter products are based on traditional circuit topologies, including: 1) single-stage Flyback Power Factor Correction (PFC) circuit [66-68], 2) two-stage topology
composed of a Boost-PFC circuit and a Half-bridge LLC resonant converter [69-72], and 3) topologies based on Φ2 resonant converter [73-76]. All these topologies impose high voltage stress (≥dc-link voltage) on switches, and thus require high-voltage (e.g. 600-V) rated devices, which is neither energy efficient nor power-density optimized. For the two-stage topology, Buck-PFC circuit can be applied to lower the dc-link voltage to 80–90 Vdc, so as to reduce the voltage stress on switches in the downstream dc/dc stage [128-129]. It is demoed that a Buck-PFC based 90-W ac/dc power adapter achieved the size of 5.93 inch³ and the efficiency of 92.5 % [128].

For the downstream isolated dc/dc stage, to enable the use of low-voltage GaN devices, a QSC dc/ac circuit is proposed in Chapter 2. Comparing to half/full-bridge circuits, it reduces the voltage stress on switches by 1/3, and reduces the transformer turns ratio by 2/3. Based on it, a QSC PWM converter is derived in Chapter 2. However, even though with ZVS on, the turn-on loss of the converter could be minimized, the turn-off loss still limits the capability of the converter to operate at higher switching frequency.

In this chapter, a QSC resonant converter is proposed to address the aforesaid challenges. It serves as an isolated dc/dc converter, downstream to a PFC circuit, in off-line power adaptor applications. The converter is based on the QSC dc/ac circuit that provides reduced voltage stress on switches and transformer. It also features full soft switching combining both ZCS and ZVS within a wide load range, and it is operated most efficiently at fixed but optimal switching frequency and duty ratio. A 90-W, 88-V/19-V, 700-kHz prototype is built with 100-V enhancement-mode Gallium Nitride (eGaN) field-effect transistors (FETs). The transformer and PCB layout are designed to minimize the
leakage inductance and loop stray inductance. These circuit designs and methods yield high power density as well as high efficiency over a wide load range.

4.2. Circuit Descriptions and Operation Principles

4.2.1. Circuit Features and Operation Principles

The proposed isolated QSC resonant converter schematic is shown in Fig. 4.1. The operation waveforms are shown in Fig. 4.2. As shown in the operation waveforms, the converter has the following features:

1) Similar to the Φ2 resonant converter, the voltage waveforms of all switches in the isolated QSC resonant converter are trapezoidal, featuring ZVS on and off [130]. However, as the Φ2 resonant converter imposes the voltage stress on switch 2X higher than the input voltage, the isolated QSC resonant converter reduces the voltage stress on HV-side switches to 2/3 input voltage, and thus enables more choices of low-voltage GaN HEMTs.

2) Compared to half/full-bridge converters (e.g. the LLC resonant converter and the dual-active-bridge converter), the transformer turns ratio of the isolated QSC resonant converter is reduced by 2/3, which enables less number of turns of the winding, lower winding loss and lower transformer leakage inductance.

3) As discussed in details in the following content, by utilizing two types of circuit resonance, the converter achieves full soft switching combining both ZCS and ZVS within a wide load range, and therefore significantly reduces the switching loss.
Figure 4.1. Equivalent circuit of the isolated QSC resonant converter. $C_2$, $C_3$ and $C_4$ are the switched capacitors; $L_s$ and $L_m$ are the transformer leakage inductance and magnetizing inductance; and $L_o$ and $C_o$ compose the output filter. To analyze all switching transients within one switching cycle, the output capacitance of all the switches ($C_{oss1}$ and $C_{oss2}$) must be taken into consideration.

Figure 4.2. Operation waveforms of the isolated QSC resonant converter. Two types of resonance are utilized in operation, which exists in the active switching modes and dead-time modes respectively. As results, ZCS on and near ZCS off are achieved during the active switching modes, while ZVS on and off are achieved during the dead-time modes.
At steady state, the converter has 8 switching modes within one switching cycle ($T_{sw}$), as shown in Fig. 4.3 (a)-(h). In the figures, the red loops signify the current paths of which the resonance is determined by $L_s$; the blue loops signify the current paths of which the resonance is dominated by $L_m$.

Figure 4.3. The switching-mode diagrams of the continuous operation in one switching cycle, including: (a) Mode 1: current path between $t_0 - t_1$, (b) Mode 2: current path between $t_1 - t_2$, (c) Mode 3: current path between $t_2 - t_3$, (d) Mode 4: current path between $t_3 - t_4$, (e) Mode 5: current path between $t_4 - t_5$, (f) Mode 6: current path between $t_5 - t_6$, (g) Mode 7: current path between $t_6 - t_7$, (h) Mode 8: current path between $t_7 - t_8$ (one switching cycle completes). Continued
Figure 4.3: Continued
There are two types of resonance identified in operation. The first type causes resonant switching currents. It results in ZCS on and near ZCS off, and therefore significantly reduces the switching losses. Such resonance exists between the $C_2$, $C_3$, $C_4$, and $L_s$, and it happens in the active switching modes, including the Mode 1, 2, 5, and 6. The equivalent resonance path for Mode 1 and 2 are shown in Fig. 4.4 (a), and the equivalent resonance path for Mode 5 and 6 are shown in Fig. 4.4 (b).

The second type of resonance exists between the $C_{oss1}$, $C_{oss2}$, and $L_m$. It happens in the dead-time switching modes, including the Mode 3 and 7. The equivalent resonance path is
shown in Fig. 4.5. This type of resonance transfers the energy stored in the output capacitance of one switch to its complementary switch, recycling that energy which otherwise would be lost in the ZCS operation. This resonance leads to ZVS on and off of the switches, which furthermore improves the efficiency. It also helps slow down the $dv/dt$ of the switches, eliminate the voltage overshoot, and reduce the EMI noises.

![Figure 4.5. The equivalent resonant path after Laplace transformation to denote the second type of resonance during the dead-time switching modes, including Mode 3 and 7. Such resonance recycles the energy in switch output capacitance which otherwise would be lost in the ZCS operation, and thus results in ZVS on and off for all the switches.]

The converter is operated most efficiently when both aforesaid types of resonance are implemented. This requires the right timing of switching, which leads us to derive the optimal duty ratio and switching frequency.

4.2.2. Optimal Duty Ratio and Switching Frequency

To find the optimal duty ratio and switching frequency, the optimal duration of the active switching modes and the dead-time switching modes must be derived respectively, and the derivation is presented as follows. As shown in Fig. 3.4, in the equivalent resonant paths for the active switching modes, $L_m$ is ignored since it is much larger than $L_s$. Despite the initial voltages on $C_2$ and $C_4$, the current $I_{Ls}$ equals to 0 at both $t_0$ and $t_4$, so a lumped voltage source represents all the initial conditions for each case. In Mode 5 and 6, where
$S_2$ is turned on, the sum of the voltage drop across the $L_s$ ($V_{Ls}$) and the loop parasitic resistance $R_s$ ($V_{Rs}$) is

$$V_{Ls}(s) + V_{Rs}(s) = V_{S2} \cdot \frac{sL_s C_2 C_4 + R_s C_2 C_4}{s^2 L_s C_2 C_4 + sR_s C_2 C_4 + C_2 + 0.5 C_4}.$$  \hspace{1cm} (4.1)

The loop current resonates to 0 when the derivative of $V_{Ls}(t) + V_{Rs}(t)$ reaches 0, so the $V_{Ls}(t) + V_{Rs}(t)$ is derived with Inverse Laplace Transformation based on (4.1) as

$$V_{Ls}(t) + V_{Rs}(t) = \text{L}^{-1} \{ V_{Ls}(s) + V_{Rs}(s) \} = V_{S2} \cdot \left( e^{-at} \cos bt + \frac{a}{b} e^{-at} \sin bt \right),$$ \hspace{1cm} (4.2)

where

$$\begin{cases} a = R_s / 2L_s \\ b^2 = (C_2 + 0.5C_4) / L_s C_2 C_4 - R_s^2 / 4L_s^2 \end{cases}.$$

According to (4.2), the derivative of the $V_{Ls}(t) + V_{Rs}(t)$ is derived as

$$\frac{d[V_{Ls}(t) + V_{Rs}(t)]}{dt} = -V_{S2} \cdot \left( b + \frac{a^2}{b} \right) e^{-at} \sin bt.$$ \hspace{1cm} (4.3)

By equating (4.3) with 0, the optimal duration of the active modes ($T_{on\_sw}$) is derived as

$$T_{on\_sw} = \frac{2\pi}{b}.$$ \hspace{1cm} (4.4)

The minimum deadtime ($T_{db\_min}$) is required to complete Mode 3 and Mode 7. To simplify the analysis, the current of $L_m$ is assumed to have a triangular waveform, and the dc-offset current is ignored since it is very small compared to the ripple current. Then, the following equations are derived

$$I_{L\_pk} = \frac{V_{in}}{3L_m} \cdot \frac{T_{on\_sw} + T_{db\_min}}{2}, \quad T_{db\_min} = \frac{2V_{in} C_{ass1} + \frac{4V_{out} C_{oss2}}{N}}{I_{L\_pk}}.$$ \hspace{1cm} (4.5)
Based on (4.5), the $T_{db, min}$ can be derived as

$$T_{db, min} = \sqrt{\frac{12}{V_{in}} \left( V_{in} C_{oss1} + \frac{2V_{out} C_{oss2}}{N} \right) L_{m} + \frac{T_{on, sw}^2}{4} - \frac{T_{on, sw}}{2}}. \quad (4.6)$$

Based on (4.4) and (4.6), the optimal duty ratio ($D_{sw}$) and optimal switching frequency ($f_{sw}$) can be derived as

$$D_{sw} = \frac{T_{on, sw}}{2(T_{on, sw} + T_{db, min})}, \quad f_{sw} = \frac{1}{2(T_{on, sw} + T_{db, min})}. \quad (4.7)$$

4.2.3. Burst-mode Operation for Improved Light-load Efficiency

The converter efficiency is the losses compared to the output power delivered. In general, of the majority of losses, there are fixed losses like the driving losses and conduction losses that vary with the square of output power. In light-load conditions, the proportion of the fixed losses over the delivered power become large. Therefore for the light-load conditions, burst-mode control is employed to decrease the losses by periodically blocking the driving signals, as shown in Fig. 4.6, and thus improves the efficiency.

Moreover, to achieve as high efficiency as possible, during the burst-on time ($T_{on, br}$), the converter is desired to operate under the steady state of the highest efficiency load condition current ($I_{opt}$) [131].

$$D_{burst} = \frac{T_{on, br}}{T_{burst}} = \frac{T_{on, br}}{T_{on, br} + T_{off, br}} = \frac{I_R}{I_{opt}}. \quad (4.8)$$
During the burst-off time ($T_{off\_br}$), $C_4$ releases its energy to the load through the output filter ($L_o$ and $C_o$), and the $C_4$ begins to resonate with $L_o$ and $C_o$, which creates a periodical ripple in $V_{C4}$. The period of the ripple ($T_{rso}$) is derived as

$$T_{rso} = 2\pi \sqrt{L_o C_o C_4 / (C_o + C_4)} .$$

(4.9)

To optimize the switching transients during $T_{on\_br}$, the $T_{off\_br}$ must be integer ($n$) times of $T_{rso}$, so that $V_{C4}$ resonates back to the average output voltage ($V_o$) at the end of the $T_{off\_br}$. Based on (4.8) and (4.9), the burst period is derived as

$$T_{burst} = T_{on\_br} + T_{off\_br} = \frac{n I_{opt} T_{rso}}{I_{opt} - I_R} .$$

(4.10)

The burst-mode control also enables the output voltage control when the converter is operating at optimized duty ratio and switching frequency.
4.3. *Prototype Design*

To verify the circuit analysis, two prototypes of the QSC resonant converter are built, including a 90-W, 88-V/19-V, 700 kHz prototype, and a 65-W, 380-V/19-V, 2 MHz prototype. These isolated QSC resonant converters serve as the DCX in a power adapter with a two-stage structure, as shown in Fig. 4.7. In this structure, the DCX is operated at fixed but optimal switching frequency and duty ratio, while the Boost-PFC stage provides the voltage regulation.

![Diagram](image.png)

Figure 4.7. The two-stage structure of the 65-W power adapter for laptops.

High switching frequency is preferred to shrink the passive components and increase power density, so high resonant frequency of the circuit is required. To ensure underdamped switching currents for the ZCS operation during the active switching-mode intervals, in practical design, it requires: 1) low transformer leakage inductance, and 2) minimized stray inductance and stray resistance in power-loop layout.

4.3.1. *Planar Transformer Design*

The 90-W prototype design is discussed here as the example. In order to reduce the transformer leakage inductance, a center-tapped planar transformer with an interleaving
winding structure is designed, as shown in Fig. 4.8 (b). Aiming initially at a switching frequency at 1 MHz, the Ferrite material 3F45 from Ferroxcube is chosen for the magnetic core. Based on the material permeability and voltage stress on winding, the transformer turns ratio is designed as $N=3:2:2$. As discussed in [132], the leakage inductance can be estimated as:

$$L_{\text{leak}} = \mu_0 \cdot \frac{l_w}{b_w} \cdot 4\left[\frac{h_1 + h_2}{2} + h_\Delta\right],$$  \hspace{1cm} (4.11)

where $l_w$ is the length of each turn, $b_w$ is the width of each turn, $h_1$ and $h_2$ are the layer-thickness of the primary and secondary winding, and $h_\Delta$ is the height of insulator layer.

As (4.11) implies, in order to reduce the transformer leakage inductance, the winding traces are preferred to be designed with shorter length, larger width, and smaller thickness per turn. Meanwhile, the insulation layer is preferred to have smaller thickness. As shown in Fig. 4.8 (a), an ideal model without termination is analyzed first in ANSYS Maxwell 3D. The simulation results are: $L_m = 19 \mu H$, $L_s = 12 nH$.

![Figure 4.8. (a) ANSYS Maxwell 3D simulation model of the ideal planar transformer without termination and (b) the interleaving winding structure.](image-url)
Then, a detailed transformer model with vias connecting different layers, as shown in Fig. 4.9 (a), is built in ANSYS Q3D Extractor for termination inductance analysis. Two parts of stray inductance contribute to the total resonance inductance, including the stray inductance of the vias connecting different layers of the winding, and the resulted extra winding strip between the vias. These inductance are estimated respectively. The stray inductance of the extra winding strip can be estimated by the following equation [133]

\[
L_{\text{strip}} = 0.0002L\left[\ln\frac{2L}{W+H} + 0.2235\frac{W + H}{L} + 0.5\right] \mu H ,
\]

(4.12)

where \( L \) is the length of the strip, \( W \) is the width of the strip, and \( H \) is the thickness of the strip. For example, the estimated stray inductance of the strip highlighted in purple in Fig. 4.9 (a) is 6.3 nH.

In addition, to reduce the stray inductance caused by the vias connecting different layers of the transformer windings, an interleaving structure of the vias is applied, as shown in Fig. 4.9 (b). For each transformer winding, at places where different layers of the winding connect, interleaving rows of vias carrying opposite currents are placed with enough clearance distance for breakdown prevention. The paralleled vias in a row provide reduced resistance and reduced conduction loss. The interleaved rows of vias allow for reduced eddy and proximity effects, reducing the ac conduction losses. The stray inductance of the interleaving vias can be estimated by the following equation [134]

\[
L_{\text{via}} = \frac{\mu_0}{2\pi} L\left[\frac{3}{2} \ln\frac{s}{r} + \frac{1}{2} \ln 2\right] \mu H ,
\]

(3.13)

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where $s$ is the distance between 2 adjacent rows of vias, $r$ is the via-hole radius, and $h$ is the via length. For example, the estimated stray inductance of the vias shown in Fig. 4.9 (b) is 0.6 nH.

Figure 4.9. (a) Detailed simulation model of the planar transformer built in ANSYS Q3D Extractor for termination inductance analysis, (b) Interleaving vias of the planar transformer.
4.3.2. **PCB Layout**

Again, the 90-W prototype design is discussed here as the example. An 8-layer PCB is designed, where the power-loop traces and the planar transformer windings are integrated. The spacing between the PCB layers need to be large enough to meet the isolation requirement in the industrial safety standards. However, smaller spacing is preferred in order to reduce both the transformer leakage inductance and the stray inductance in layout. To meet the safety standards such as IEC60950, the spacing is required to be at least 400 µm. However, according to the standard IPC2221, the electric strength of the FR4 material is 39.4 kV/mm, so a 4-mil spacing is selected in this preliminary design, which is enough to withstand 4-kV isolation.

The power-loop stray inductance is also part of the resonance inductance. It slows down the switching speed, causing more switching loss [135-136], and thus needs to be minimized. In the PCB layout, the optimal layout for reduced stray inductance and resistance, as proposed in [136], is followed. Take the layout of $S_2$, $C_2$ and $C_3$ for example (shown in Fig. 4.10): 1) $S_2$, $C_2$ and $C_3$ are all placed on the top layer, with minimal spacing in between; 2) the transformer primary-side winding starts from the top layer and ends on the 2nd layer; 3) the switch currents flow to the transformer on the top layer, and returns on the 2nd layer. The current return path is located directly underneath the top layer’s power loop, allowing for the smallest physical loop size combined with field self-cancellation.
Figure 4.10. Optimal PCB layout of the switched capacitors and switches for reduced high frequency parasitic inductance and resistance in the power loop of the converter.

4.3.3. Output Rectifiers

The switches $S_3$ and $S_4$ operate as synchronous rectifiers (SR) to reduce the conduction loss. However, due to the high source-drain forward voltage of eGaN FETs, the propagation delay before turning on the device would lead to high conduction loss, which can be minimized by Schottky diodes in parallel [137]. In the design, $S_3$ and $S_4$ are paralleled with Si Schottky Diode PDS760, which are selected for its low forward voltage.

The 90-W prototype of the isolated QSC resonant converter is shown in Fig. 4.11. The circuit parameters are listed in Table 4.1. It includes the main circuit and gate-drive circuits, but doesn’t include the controller, the isolated power supplies for the gate-drive circuits, and the output filter. The power density of this preliminary prototype has reached 172 W/inch$^3$. 
Figure 4.11. A 90-W, 88-V/19-V, 700-kHz, isolated QSC resonant converter prototype.

Table 4.1. Specifications for the simulation model and experimental prototype of the 90-W, 88-V/19-V, 700-kHz, isolated QSC resonant converter

<table>
<thead>
<tr>
<th>Item</th>
<th>Descriptions</th>
<th>Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{in}/V_{out}$</td>
<td>Input voltage/output voltage</td>
<td>88 V/19 V</td>
</tr>
<tr>
<td>$f_{sw}$</td>
<td>Optimal switching frequency</td>
<td>700 kHz</td>
</tr>
<tr>
<td>$D_{sw}$</td>
<td>Optimal duty ratio</td>
<td>0.32</td>
</tr>
<tr>
<td>$C_2$, $C_3$, $C_4$</td>
<td>Switched capacitors</td>
<td>2.2 µF, ceramic 100 V</td>
</tr>
<tr>
<td>$L_s$, $L_m$</td>
<td>Planar transformer (integrated in the PCB)</td>
<td>Ferrite 3F45 from Ferroxcube, $L_m=16$ µH, $L_s=25$ nH, $N=3:2:2$,</td>
</tr>
<tr>
<td>$S_1$–$S_4$</td>
<td>Switches</td>
<td>EPC2016 (100 V/11 A), $S_3$ &amp; $S_4$ are in paralleled with schottky diode PDS760</td>
</tr>
<tr>
<td>$R_s$</td>
<td>Power-loop resistance</td>
<td>0.1 Ω @ 1 MHz</td>
</tr>
</tbody>
</table>

4.3.4. 65-W Prototype

A 65-W, 380-V/19-V, 2-MHz, isolated QSC resonant converter prototype is built for the power adapter dc/dc stage. It has an estimated high efficiency of 97.5%, and a high power density of 275 W/inch³. The PCB layout and prototype are shown in Fig. 4.12. Enhancement-mode GaN HEMTs from EPC are employed for its low but sufficient voltage
and current ratings, small package, and high figure of merit. As the QSC dc/ac circuit reduces the voltage stress on the switches, the steady-state voltage stress on the primary-side switches is only 267 V, so the 450-V, 4-A rated EPC2027 is chosen as the primary-side switches. The EPC2027 is with a 1.95 mm × 1.95 mm footprint, which is much smaller than the 600-V Si CoolMOS FETs and 600-V GaN HEMTs with similar or available, lowest current rating (10 A or so). The QSC dc/ac circuit in such power ratings is a niche application for the EPC2027, because such devices don’t have enough voltage margin when applied in half/full-bridge circuits with a 400-V dc bus. Unfortunately, this device is called off by EPC in Dec. 2015, after the prototype is built. On the secondary side, the 80-V, 31-A rated EPC2029 is chosen as the switches, operating as synchronous rectifier to reduce the conduction loss.

Figure 4.12. (a) PCB layout and (b) prototype of a 65-W, 380-V/19-V, 2-MHz isolated QSC resonant converter serving as the dc/dc stage of the 65-W power adapter for laptops.
4.3.5. Gate-drive Circuit Power Supply

The gate-drive circuit power supply for the switches in the power adapter is designed as follows: 1) auxiliary windings in the boost inductor and the isolation transformer are designed as shown in Fig. 4.13, to supply the gate-drive power during the continuous operation. The power from the auxiliary windings are rectified by schottky diodes, and then stored in the source capacitors ($C_{aux1}$, $C_{aux2}$, and $C_{aux3}$) of the gate-drive circuit power supply; and 2) during the start-up, large resistors are used to charge up $C_{aux1}$, $C_{aux2}$, and $C_{aux3}$, using the energy from the dc-bus capacitors or the switched capacitors $C_2$ and $C_3$.

![Figure 4.13. Auxiliary winding configurations to provide power for the gate-drive circuit in continuous operation of the power adapter.](image)

4.4. Simulation and Experimental Verifications

4.4.1. Simulation and Experimental Results of the 90-W Prototype

Two experiments are conducted to compare the operations with and without optimized duty ratio and switching frequency. The first experiment is conducted under the conditions: $V_{in}=88$ V, $P_o=90$ W, $D_{sw}=0.47$, and $f_{sw}=900$ kHz. Both the simulation and experimental waveforms are shown in Fig. 4.14. Since the switch currents and transformer current couldn’t be monitored in the prototype, only the voltage waveforms are recorded.
Figure 4.14. (a) The simulation waveforms and (b) the experimental waveforms of the voltage across the switches ($V_{ds,S1}$, $V_{ds,S2}$, $V_{ds,S3}$), the transformer primary-side winding voltage ($V_{an}$), the transformer primary-side winding current ($I_{Ls}$), and transformer primary-side-referred magnetizing inductor current ($I_{Lm}$). All waveforms are recorded in the operation condition: $V_{in}=88$ V, $P_o=90$ W, $D_{sw}=0.47$, and $f_{sw}=900$ kHz. Based on the analysis, in this case the $D_{sw}$ and $f_{sw}$ are not optimized, so ZVS on and off are not achieved.

Figure 4.15. (a) The simulation waveforms and (b) the experimental waveforms of the voltage across the switches ($V_{ds,S1}$, $V_{ds,S2}$, $V_{ds,S3}$), the transformer primary-side winding voltage ($V_{an}$), the transformer primary-side winding current ($I_{Ls}$), and transformer primary-side-referred magnetizing inductor current ($I_{Lm}$). All waveforms are recorded in the operation condition: $V_{in}=88$ V, $P_o=90$ W, $D_{sw}=0.32$, and $f_{sw}=700$ kHz. Based on the analysis, in this case the $D_{sw}$ and $f_{sw}$ are optimized, so ZVS on and off are achieved.
Following that, the second experiment is conducted, under the test conditions: $V_{in}=88$ V, $P_o=90$ W, $D_{sw}=0.32$, and $f_{sw}=700$ kHz. Both the simulation and experimental waveforms are shown in Fig. 4.15.

As shown in the Fig. 4.14 and Fig. 4.15: 1) the voltage stress on $S_1$ and $S_2$ are reduced to $2V_{in}/3$, and the voltage stress on the transformer is reduced to $V_{in}/3$ on the primary side; 2) ZVS on and off are not achieved in Fig. 4.14, but achieved in Fig 4.15. With optimized $D_{sw}$ and $f_{sw}$ applied, the switching loss is minimized; 3) In Fig. 4.14, the voltage overshoot and ringing on the switches at turning off are significant, which increases the risk of breakdown failure and the EMI noise. However, such ringing and overshoots are eliminated when optimized $D_{sw}$ and $f_{sw}$ are applied, as shown in Fig 4.15, which indicates more reliable operation and reduced EMI noise.

To verify the burst-mode control, simulation is conducted on the same circuit model in PSIM, and experiments are conducted on the 90-W prototype. The test conditions are: $V_{in}=75$ V, $D_{burst}=0.25$, $f_{burst}=41$ kHz, $P_o=10$ W. The simulation and experimental results are shown in Fig. 4.16 and Fig. 4.17, respectively.
Figure 4.16. Burst-mode operation simulation results of the isolated QSC resonant converter.

Figure 4.17. Burst-mode operation experimental results of the isolated QSC resonant converter.
As shown in the Fig. 4.17: 1) the strategy of selecting the $T_{off \_br}$ to be integer times of $T_{rso}$ is verified, and it matched the simulation results in Fig. 4.16; 2) in the $V_{an}$ waveform, it exhibits damping during the burst-off time, which is caused by the loop parasitic resistance. This damping gradually depletes the energy stored in the magnetics, so the converter will experience a start-up transient when switching back to the normal-mode operation. Further analysis and the delicate control to smoothly get through this transient needs to be discussed in future work.

The converter power loss and efficiency curves are shown in Fig. 4.18. It is shown that the power loss and efficiency are significantly improved with optimized $D_{sw}$ and $f_{sw}$ applied, as results a flat efficiency curve with a peak value at 96 % is achieved.

![Figure 4.18. Power loss and efficiency results of the prototype, in comparison between the operations with and without optimized $D_{sw}$ and $f_{sw}$.](image)
4.4.2. Preliminary Simulation Results of the 65-W Prototype

The simulation results of the 65-W prototype are shown in Fig. 4.19. Similar to the 90-W prototype presented in section 3.2.4, this 65-W prototype achieves reduced voltage stress on the switches and the transformer, as well as full soft switching combining ZVS and ZCS within in a wide load range. In the transformer winding design, inner shielding layers are added in between the primary side and secondary, to block the CM noise transmitted across the transformer windings [138-139]. In this way, less CM noise is seen at the line input, and thus the EMI filter size can be reduced. The testing of this prototype is still in progress.

Figure 4.19. Steady-state simulation waveforms of the 65-W, 380-V/19-V, isolated QSC resonant converter.
4.5. Conclusions

The isolated QSC resonant converter is proposed to serve as a DCX for the isolated dc/dc conversion in off-line power supply applications, offering high power density and high efficiency. Similar to the Φ2 resonant converter, the converter is operated most efficiently at fixed switching frequency and duty ratio applied, and it features trapezoidal voltage waveforms on all switches. Full soft switching is achieved combining ZCS on, near ZCS off, ZVS on, and ZVS off within a wide load range, so the switching loss is minimized. In addition, compared to half/full-bridge converters (e.g. the LLC converter and dual-active-bridge converter), the proposed converter reduces the voltage stress on primary-side switches to 2/3 of the input voltage, and thus enables more choices of low-voltage GaN devices, which are more efficient because of their better figure of merit. Furthermore, the converter reduce transformer turns ratio by 2/3, and thus enables less number of turns of the winding, lower winding loss and lower transformer leakage inductance, making it suitable for high-frequency operation. For demonstration, a 90-W, 88-V/19-V, 700-kHz prototype is built with 100-V eGaN FETs. The transformer design and PCB layout are presented to minimize the transformer leakage inductance and stray inductance. The prototype achieved a power density of 172 W/inch³, and a flat efficiency curve with a peak value of 96 %. Furthermore, a 65-W, two-stage, off-line power adapter is designed based on the isolated QSC resonant converter. A 65-W, 380-V/19-V, 2-MHz isolated QSC resonant converter prototype is built with Enhancement-mode GaN HEMTs. It has an estimated high efficiency of 97.5%, and a high power density of 275 W/inch³.
The proposed isolated QSC resonant converter is not limited to low-power applications. It also has the scalability to be applied in high-voltage, high-power applications. The reduced voltage stress on switches and transformer are of particular interest for high voltage converters such as the solid-state transformers, where challenges exist in the development and application of high-voltage (>10 kV) SiC power devices and also the insulation design of the high-voltage transformer. Efforts should be made thus in such directions to explore and expand the applications of the proposed converter.
Chapter 5.  Semiconductor-based Galvanic Isolation

This chapter presents the study of a transformational paradigm for galvanic-isolated power converters. The proposed galvanic isolation principle is fundamentally different from that of the traditional galvanic isolation solutions, such as the magnetic field-based solution, electric field-based solution, and optics-based solution. This solution delivers the DM load power via semiconductor switches during their ON states, while sustaining the CM voltage and blocking the CM leakage current with those switches during their OFF states. It is enabled by the unprecedented characteristics of WBG semiconductor power devices, and it fully utilizes those characteristics to yield significant circuit topology simplification, dramatic power density improvement, and effective galvanic-isolation that meets industry safety standards.

5.1.  Galvanic Isolation Requirements in the Safety Standard IEC60950

Isolated power converters must meet safety standard requirements to validate their galvanic isolation. IEC60950 is the most widely applied safety standard for power supplies today. It is intended for use with information technology, business, and telecom equipment. Other standards exist for other industries, such as IEC60065 for audio and video, IEC60601 for medical, IEC61010 for laboratory supplies, IEC61851 for electric vehicle charging systems, and others.
5.1.1. *Insulation Voltage Requirement*

IEC60950 defines five categories of insulation, including:

1) Functional insulation, which is only necessary for circuit operation. It is assumed to provide no safety protection.

2) Basic insulation, which provides basic protection against electric shock with a single level. Safety is provided by a second level of protection such as Supplementary insulation or protective earthing.

3) Supplementary insulation, which normally is used in conjunction with Basic insulation to provide a second level of protection in the event that the Basic level fails.

4) Double insulation, which is a two-level system, usually consisting of Basic insulation plus Supplementary insulation.

5) Reinforced insulation, which is a single-insulation system equivalent to Double insulation.

Electric circuits rely upon insulation for operator protection, but designing for safety requires the premise that anything can fail. Therefore, safety standards demand a redundant system with at least two levels of protection under the assumption that any single level may experience a failure, but the chance of two simultaneous failures in the same spot is so improbable that it represents an acceptable risk.

The general requirements are that a single level of insulation is acceptable if the circuit is not accessible, but wherever there are accessible components, they must be insulated from hazardous voltages by a Double-level system, and each level must meet the insulation
specifications appropriate to the application. One qualification to this statement is that one level of protection could be protective earth provided by a conductive grounded enclosure.

Categories are used to define different classes of circuits and the type of insulation needed for each, as:

1) Class I Equipment: Systems which use protective earthing (e.g., a grounded metal enclosure) as one level of protection and thus require only Basic insulation between the enclosure and any part at hazardous voltage.

2) Class II Equipment: The use of Double or Reinforced insulation to eliminate the need for a grounded metal enclosure as well as a grounded power plug.

3) Class III Equipment: Powered from a safety extra low voltage (SELV) source (≤ 42.4 V_{pk, ac} or 60 V_{dc}) with no potential for generation of hazardous voltages internally, and therefore, requiring only Functional insulation.

In IEC60950, the test voltages for the equipment insulation tests are specified. For most off-line power supplies, the test voltage is 1.5 kV_{ac, rms} for functional, basic-supplementary insulation, and 3 kV_{ac, rms} for reinforced insulation.

5.1.2. Touch Current and Protective Conductor Current Requirement

In IEC60950, touch current (TC) is defined as the electric current through a human body when it touches one or more accessible parts. As shown in Fig. 5.1 [140], if the circuit is unearthed, the current through the human body is "leakage" through stray or added capacitance across the isolation stage, which is the transformer in the figure. This current comes from a relatively high voltage, high impedance source, and its value is largely
unaffected by the operating voltage on the electronic circuit. In IEC60950, the TC is measured using an impedance network \( Z_{TC} \) as the measuring instrument, as shown in Fig. 5.2, which roughly simulates a human body.

![Figure 5.1. Touch current from a floating circuit (with unearthed output) [140].](image)

![Figure 5.2. TC measuring instrument – an impedance network to roughly simulate a human body [140].](image)

If the electronic circuit is earthed by protective earthing conductors, any leakage current from the isolation stage will be conducted to earth and will not pass through the human body. However, IEC60950 also has specified the limit for the protective conductor current (PCC), which is defined as the current flowing through the protective earthing conductor under normal operating conditions. In IEC60950, PCC is limited to 5% of the input current, for stationary, permanently connected equipment or stationary, pluggable equipment type B that has a protective earthing conductor.
5.2. **Background of Existing Galvanic Isolation Solutions and Research Motives**

As discussed in Chapter 1, traditionally, there are three general solutions to achieve galvanic isolation in power converters, including: 1) the magnetic field-based galvanic isolation; 2) the electric field-based galvanic isolation; and 3) the optics-based galvanic isolation. In addition, for PV inverter applications, transformerless inverter topologies and associated control schemes are proposed to limit the ground-loop current, which is a CM leakage current. The limitations of each solution are discussed below.

5.2.1. **Limitations of Magnetic Field-Based Galvanic Isolation**

Magnetic field-based galvanic isolation is provided either by air/magnetic-core transformers or by a coupled inductor with dc-bias current (such as the flyback converter transformer). Traditionally, most power conversion systems achieve galvanic isolation with this solution, as discussed in Chapter 1. For grid-tied applications, a line-frequency transformer may be added at the grid interface, but its large volume and heavy weight cause low power density. To improve the system power density and reduce the system cost, isolated dc/dc converters with a high-frequency transformer are employed in increasingly more applications. Magnetic-core transformers with high permeability materials (e.g., Mn-Zn ferrite) are generally applied in isolated dc/dc converters in the switching frequency region between multi-kHz and multi-MHz. Air-core transformers have low permeability and thus are less effective to confine the magnetic field within a limited space. For this reason, it is used primarily for long-distance wireless power transfer applications. However, in the VHF (30-300 MHz) switching-frequency region, air-core inductors or
magnetic-core inductors with low-permeability RF magnetic materials (for core loss reduction) are built to achieve improved converter power density [56-58].

In most cases, magnetic components are the largest and most expensive components in power electronic circuits and are responsible for a large portion of the power loss [78-82]. For a given converter topology, the values of magnetic components and capacitors and the total required energy storage vary inversely with the switching frequency, directly motivating increases in frequency to achieve miniaturization. However, the scaling of passive component size with frequency is a far more complex issue. In magnetic components, the scaling depends on winding loss effects, magnetic material core loss characteristics, and heat transfer limits, among other considerations. Currently, in the hundreds-of-kHz switching frequency region, the power density of transformers for isolated dc/dc converters has reached 0.07 W/mm³, and in the multi-MHz switching frequency region, the power density has reached 0.107 W/mm³ [141-142]. In efforts to further improve the power density, research on magnetic components has extended to a micro-fabricated on-chip or similar scale [78-80]. With a sufficiently small volume, the magnetics can be embedded in the substrate of the power circuit or within a secondary substrate and flip-bonded above the power circuit, helping to reduce the volume of the system. To date, though increased dramatically in the last two decades, energy densities of magnetic components are still orders of magnitude lower than those of capacitors [3] [56-57] [78-82], as shown in Table 5.1. This is mainly because that, for the inductors, energy is limited by the current limits, whether these arise from a thermal limit or magnetic saturation. As a result, magnetic components remain the bottleneck toward further
improvement of power density for isolated power converters. Furthermore, to build isolated
dc/dc converters based on transformers, multiple circuit stages are required aside from the
transformer, including an inverter circuit and a rectifier circuit, which all contribute to
system volume, power loss, and cost. For example, the state-of-the-art power density of
the LLC converter with a MHz matrix transformer and GaN HMETs achieves 0.05 W/mm$^3$
[142].

<table>
<thead>
<tr>
<th>Type</th>
<th>$f_{\text{max}}$ (MHz)</th>
<th>Power density per area (W/mm$^2$)</th>
<th>Energy density per volume (µJ/mm$^3$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Metacapacitor [3]</td>
<td>10</td>
<td>6260</td>
<td>625</td>
</tr>
<tr>
<td>Deep trench capacitor</td>
<td>10</td>
<td>4690</td>
<td>469</td>
</tr>
<tr>
<td>X7R MLCC ceramic capacitor</td>
<td>2</td>
<td>252</td>
<td>126</td>
</tr>
<tr>
<td>Metallized polymer film capacitor</td>
<td>2</td>
<td>12.7</td>
<td>6.3</td>
</tr>
<tr>
<td>Tantalum electrolytic capacitor</td>
<td>0.3</td>
<td>0.8</td>
<td>26</td>
</tr>
<tr>
<td>Aluminum electrolytic capacitor</td>
<td>0.3</td>
<td>0.8</td>
<td>26</td>
</tr>
<tr>
<td>Microfabricated air-core toroid inductor [78]</td>
<td>14.8</td>
<td>0.3</td>
<td>-</td>
</tr>
<tr>
<td>Microfabricated magnetic-core toroid inductor [78]</td>
<td>10.1</td>
<td>0.6</td>
<td>-</td>
</tr>
<tr>
<td>Microfabricated magnetic-core racetrack inductor [78]</td>
<td>5</td>
<td>0.46</td>
<td>-</td>
</tr>
</tbody>
</table>

5.2.2. Limitations of Electric Field-Based Galvanic Isolation

Electric field-based galvanic isolation has been applied for LED driver [1-4], battery
charger [5-7], and power supply for liquid sterilization [8]. Traditionally, electric field-
based galvanic isolation is also applied in isolated data transfer applications, such as the digital isolator [9-11] and isolated gate drive [12-13]. In such applications, high CM impedance is required and embodied as a CM transient immunity (CMTI) ratio to block CM noise in the presence of high CM $dV/dt$ (e.g. 50 kV/µs).

To meet the isolation safety standards (e.g., IEC60950), electric field-based isolated power converter needs to perform both high insulation voltage (1.5 kV$_{ac, \text{rms}}$ for the functional/basic/supplementary insulation, and 3 kV$_{ac, \text{rms}}$ for the reinforced insulation) and low TC or PPC. Bulky Y-type film capacitors have been chosen as the isolation capacitors for its high voltage rating and safety characteristics [1-2]. In [3], to achieve high power density, high cost 3 kV ceramic capacitors are utilized. In either case, inductors are still necessary in the power stage to create resonance. In addition, because an inverter circuit and a rectifier circuit are still required, there is no reduction of circuit stages. Thus, compared to the magnetic field-based solution, power density improvement of electric field-based isolation is quite limited.

5.2.3. Limitations of Optics-Based Galvanic Isolation

The optics-based galvanic isolation, especially the power over fiber [16, 17], provides the best CM performance. However, this solution suffers from low power density and low efficiency, which is much lower than those of transformer-based or capacitive coupling-based solutions. This is mainly because laser transmitters and receivers are bulky and inefficient. For example, a typical multi-junction photovoltaic-based receiver usually has
an efficiency lower than 50%. As power density and efficiency are key requirements for power electronic circuits, optic-based solutions are suitable only for niche applications.

5.2.4. *Limitations of Transformerless Grid-tied Inverters*

In PV inverter applications, the parasitic capacitance between the PV panel and the ground causes a CM leakage current, which must be limited in order to meet the industrial safety standards and codes, such as the IEC 60755, VDE 0126-1-1, and VDE-AR-N 4105. Transformerless inverter topologies and their control schemes are derived to reduce this CM leakage current [143-148]. The approach is to achieve constant CM voltage within the asymmetrical inductor-based topologies, or to implement dc or ac decoupling within the symmetrical inductor-based topologies. With such approaches applied, the CM leakage current of the inverter is successfully limited to tens of mA [143-148].

However, such approaches are not applicable to achieve galvanic isolation in general applications for two reasons. First, they focus merely on the CM leakage current reduction, while other galvanic isolation related issues such as the CM isolation voltage are not addressed. Secondly, when compared to with the limits in the safety standards for off-line power supplies, such as the IEC60590 and UL2202, it can be seen that the CM leakage current level after reduction with these approaches is still much higher than the general TC limits and PCC limits. Thus, more study is required to extend these approaches to other applications that require galvanic isolation.
5.3. **Semiconductor-based Galvanic Isolation**

5.3.1. **Basic Circuit Structure and Potential Benefits:**

This research proposes a semiconductor-based galvanic isolation solution. The basic idea of this solution, as shown in Fig. 5.3, is to deliver the DM load power via active ac semiconductor switches during their ON states, while sustaining the CM voltage and blocking the CM leakage current with those ac switches during their OFF states.

![Diagram](image)

*Figure 5.3. (a) Basic idea of the semiconductor-based isolation; and (b) an example of the ac switch with bidirectional blocking capability.*

A basic topology of the dc/dc converter with semiconductor-based galvanic isolation is presented in Fig. 5.4. It is the SC isolation cell circuit discussed in [85-86]. Two pairs of switches (S1 and S2 are in one pair, while S3 and S4 are in another pair) operate complementarily, so that the DM power flows are decoupled. Fig. 5.5 shows the two phases of the circuit in one switching cycle, with the DM and CM current flows signified, respectively. It shows that, at any time, the converter has at least a pair of switch turned
off, serving as the isolation barrier. The switch output capacitance is connected in series in the CM leakage current loop. The switches turned off serve to sustain the CM isolation voltage and switch output capacitance limits the CM leakage current. Such functions are very similar to those of the isolation capacitors in the electric field-based galvanic isolation shown in Fig. 1.2. However, while the electric field-based galvanic isolation suffers a continuous CM leakage current caused by the line input, the proposed solution suffers a repetitive pulse CM leakage current, which is relevant to the switching operation of the isolated dc/dc stage, as discussed in more detail in section 5.4.

![Diagram of SC isolation cell circuit](image)

Figure 5.4. The SC isolation cell circuit -- a basic topology of the dc/dc converter with semiconductor-based galvanic isolation (all switches are ac switches with bidirectional blocking capability).

![Diagram of DM and CM current flows](image)

Figure 5.5. DM and CM current flows in the SC isolation cell circuit in (a) Phase I, and (b) Phase II.
An application scenario of the proposed converter in off-line power supplies is illustrated in Fig. 5.6. The converter has a two-stage structure, including a rectifier stage with PFC function, and a dc/dc stage with the semiconductor-based galvanic isolation. The dc/dc stage works as a dc transformer (DCX). According to IEC60950, a human-body impedance network \((Z_{TC})\) is inserted to measure the touch current (TC, or \(I_{TC}\)), which is a CM leakage current caused by the line input.

![Diagram of the converter system](image)

Figure 5.6. An off-line power supply application of the semiconductor-based isolation.

Compared with isolated dc/dc converters with traditional magnetic fields or electric field-based galvanic isolation solutions, this dc/dc converter with semiconductor-based galvanic isolation has the following benefits.

1) It achieves direct isolated dc/dc conversion without using the inverter and rectifier circuits, resulting in a lower number of components.
2) It eliminates the magnetic components in the dc/dc stage, simplifying the structure and lowering the design and manufacturing complexity. More importantly, this solution can potentially achieve a higher power density. This is because capacitors perform much higher power density and energy density compared with magnetic components, and they also are easier to integrate into power modules with packaging techniques.

5.3.2. Challenges

The proposed method is based on SC circuits with ac switches. It looks simple, but has many challenges as discussed below.

The first challenge is the CM leakage current. In order to meet the safety standard requirements, the converter must limit the CM leakage current to a low level (e.g. $0.25 \text{ mA}_{\text{ac, rms}}$ TC limit in IEC60950). As discussed in details in section 5.4, the normal operation of the SC isolation cell circuit suffers an impulse CM leakage current at every turn-on event, because of the switch output capacitance. Therefore, the output capacitance of the switches needs to be very small. In addition, the switching frequency and size reduction of passive components in the circuit are limited.

The second challenge is the converter’s voltage transfer ratio. This challenge is addressed by stacking basic SC cells together or adapting more advanced SC circuit based converter topologies.

The third challenge is voltage regulation. As discussed in section 1.3, SC converters, including resonant SC converters, usually do not have good voltage regulation capability. Thus, to achieve good voltage regulation, new circuit topologies with semiconductor-based
galvanic isolation need to be derived. The voltage regulation also can be provided by other circuits in the system. Some possible solutions for both challenges 2 and 3 are presented in section 5.6.

The fourth challenge, which is the one challenge that has prevented the realization of semiconductor-based galvanic isolation, is the limited characteristics of traditional silicon (Si)-based power devices, including limited breakdown voltage, high ON resistance, high output capacitance, and low switching speed. The low breakdown voltage limits the isolation voltage rating. The high ON resistance limits the efficiency of the circuit. The high output capacitor provides a low impedance path for the CM mode current.

5.4. **CM Leakage Current Analysis**

5.4.1. **Isolation Voltage Stress in Off-line Power Supplies**

In off-line power supplies, the primary side of the isolated dc/dc stage is linked to the ac/dc stage, so in operation it has access to the ac line input. Meanwhile, a human body has access to the secondary side of the isolated dc/dc stage. The isolated dc/dc stage must sustain the CM isolation voltage, and provide high impedance to limit the TC or PPC.

During the operation of off-line power supplies, the isolation voltage stress across the isolated dc/dc stage varies. Fig. 5.7 shows the potentials at different terminals of the isolated dc/dc stage in off-line power supplies with a Boost PFC circuit. For the analysis of the isolation voltage stress on the dc/dc stage, it is assumed that: 1) the neutral power connection shares the same potential with the ground; and 2) the initial voltage drop across the $Z_{TC}$ is assumed to be zero. The second assumption is made because the pulse CM
leakage current is discontinuous and it damps to zero before every switching event. This mechanism is discussed in more detail in the following CM leakage current study in section 5.4.2.

In off-line power supplies with a Boost PFC, the dc-link ground rail has the earth potential during the positive half line cycle where the line voltage is positive, as shown in Fig. 5.7 (a) and (b). In the negative half line cycle where the line voltage is negative, the dc-link ground rail is applied with the line voltage, as shown in Fig. 5.7 (c) and (d). The dc-link is connected to the primary side of the isolated dc/dc stage. On the secondary side of the isolated dc/dc stage, depending on where the human body touches, the earth potential is applied to either the output positive rail or the output ground rail.

![Diagram](image-url)

Figure 5.7. Isolation voltage across the isolated dc/dc stage in off-line power supplies with a Boost PFC circuit. (a) and (b) are during the positive half line cycle where the line input voltage is positive; (c) and (d) are during the negative half line cycle where the line input voltage is negative. Continued
As a result, in a Class-I, off-line power supply with a Boost-PFC, if the output ground is earthed, the isolation voltage ($V_{CM}$) across the isolated dc/dc stage is as shown in Fig. 5.8. The voltage is zero during the positive half line cycle, but equal to the line voltage during the negative half line cycle.

![Isolation voltage across the isolated dc/dc stage in a Boost-PFC based, Class-I, off-line power supply with an earthed output negative rail.](image)

In off-line power supplies with a Totem-pole PFC, the dc-link ground rail has the earth potential during the positive half line cycle where the line voltage is positive, as shown in Fig. 5.9 (a) and (b). In the negative half line cycle where the line voltage is negative, the dc-link ground rail is applied with negative dc-link voltage, as shown in Fig. 5.9 (c) and (d).
(d). The dc-link is connected to the primary side of the isolated dc/dc stage. On the secondary side of the isolated dc/dc stage, depending on where the human body touches, the earth potential is applied to either the output positive rail or the output ground rail.

Figure 5.9. Isolation voltage across the isolated dc/dc stage in off-line power supplies with a Totem-pole PFC circuit. (a) and (b) are during the positive half line cycle where the line input voltage is positive; (c) and (d) are during the negative half line cycle where the line input voltage is negative.

As a result, in a Class-I, off-line power supply with a Totem-Pole PFC, if the output ground is earthed, the CM insulation voltage across the isolated dc/dc stage is as shown in Fig. 5.10. The voltage is zero during the line input positive half cycle, but equal to the negative dc-link voltage during the line input negative half cycle.
With the isolation voltage applied across the isolated dc/dc stage, the parasitic CM capacitance, which is the switch output capacitance in the proposed isolation solution, causes a CM leakage current. The analysis of the CM leakage current is as follows.

5.4.2. Generation mechanism of the CM leakage current

In the SC isolation cell circuit, a pulse CM leakage current is generated at every turn-on event, charging up the output capacitance of the switches. This energy, stored in the output capacitance, dissipates by the same switches in the next turn-on event. This mechanism is illustrated in Fig. 5.11, where the output capacitance of $S_1$ is charged up, while $S_3$ dissipates its own output capacitance energy that is stored earlier in the previous turn-on event. It is the major cause of the CM leakage current through human body or earth-connected protective conductors. To clarify, the CM leakage current we study in this work is caused only by this mechanism, whereas other portions of the CM leakage current caused by the parasitic CM capacitance to ground are out of the scope of discussion.
This pulse CM leakage current repeats at the switching frequency, resulting in an accumulated TC, which has an envelope in phase with the line input, as shown in Fig. 5.12. For analyzing the pulse TC ($I_{TC}$), the loop stray inductance ($L_{stray}$) and switch output capacitance ($C_{oss}$) all have zero initial conditions, and the CM isolation voltage is applied as a step input.

Figure 5.12. TC equivalent circuit and the accumulated TC profile, in a Boost-PFC based off-line power supply, when a human body touches the output ground (the circuit parameters are extracted in this case study, assuming 1.7-kV SiC MOSFET C2M1000170D).
5.4.3. Quantitative analysis of the TC

In the quantitative analysis of the $I_{TC}$, the DM voltage source and the capacitor $C_2$ and $C_3$ equivalent circuit in Figure 5.12 is assumed to have zero impedance for analysis simplification. Based on the equivalent circuit, the $I_{TC}$ at every turn-on event with an ideal step input voltage is described as:

$$
I_{TC}(t) = \frac{2V_{CM} e^{tR/L_{	ext{step}}}}{\sinh \left( \frac{t \cdot \sqrt{2C_{\text{oss}}(2C_{\text{oss}}R - 2L_{\text{stray}})}}{2L_{\text{stray}}C_{\text{oss}}} \right) \cdot \sqrt{2C_{\text{oss}}(2C_{\text{oss}}R - 2L_{\text{stray}})}}{2C_{\text{oss}}R^2 - 2L_{\text{stray}}}, \quad (5.1)
$$

where $V_{CM}$ is the magnitude of the CM voltage source at the turn-on moment; $L_{\text{stray}}$ is the loop stray inductance; $C_{\text{oss}}$ is the switch output capacitance; and $R$ is the 500-$\Omega$ resistance in the human-body impedance ($Z_{TC}$), which dominates the total series loop resistance.

The plots of the $I_{TC}$ with different values of $C_{\text{oss}}$ and $L_{\text{stray}}$ are shown in Fig. 5.13. It can be seen that: 1) larger $C_{\text{oss}}$ causes greater energy and RMS value of the $I_{TC}$, and thus is not preferred; 2) larger $L_{\text{stray}}$ increases the loop CM impedance and thus damps the $I_{TC}$. It reduces the peak current, but it does not reduce the RMS value of the $I_{TC}$, when the switching cycle is much larger than the circuit time constant.
A parametric study further explores the impact of $C_{oss}$ and switching frequency ($f_{sw}$) on TC. Switching circuit models are built in the Matlab, based on the equivalent circuits shown in Fig. 5.12, using ideal switches in parallel with a constant $C_{oss}$. The first study explores the impact of $C_{oss}$ on TC. The parameter settings are shown in Tab. 5.2, and the results are plotted in Fig. 5.14.

Table 5.2. Simulation parameters for studying the impact of $C_{oss}$ on $I_{TC}$ (embodied as the output voltage of $Z_{TC}$) in the basic SC isolation cell circuit.

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
<th>Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{ac}$</td>
<td>Line input (only the negative half line cycle applies as the CM voltage source)</td>
<td>60 Hz / 120 V$_{ac, rms}$</td>
</tr>
<tr>
<td>$L_{stray}$</td>
<td>Loop inductance</td>
<td>60 nH</td>
</tr>
<tr>
<td>$C_{oss}$</td>
<td>Switch output capacitance</td>
<td>30 pF – 10 nF</td>
</tr>
<tr>
<td>$f_{sw}$</td>
<td>Switching frequency</td>
<td>1 kHz</td>
</tr>
</tbody>
</table>
IEC 60950 limit for all equipment with accessible parts not connected to protective earth

IEC 60950 limit for hand-held equipment with Z_{TC} connected to protective earth conductor (if any)

Simulation result of the equipment without the protective earth conductor

Figure 5.14. RMS value of the Z_{TC} output voltage in the simulation of the basic SC isolation cell circuit. The equivalent circuit is shown in Fig. 5.12 and the circuit parameters settings listed are in Table 5.2.

The second study explores the impact of f_{sw} on TC. The same Matlab switching circuit models are used. The circuit parameter settings are listed in Tab. 5.3, and the results are plotted in Fig. 5.15.

Table 5.3. Simulation parameters for studying the impact of f_{sw} on I_{TC} (embodied as the output voltage of Z_{TC}) in the basic SC isolation cell circuit.

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
<th>Specifications</th>
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</thead>
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<tr>
<td>V_{ac}</td>
<td>Line input (only the negative half line cycle applies as the CM voltage source)</td>
<td>60 Hz / 120 V_{ac, rms}</td>
</tr>
<tr>
<td>L_{stray}</td>
<td>Loop inductance</td>
<td>60 nH</td>
</tr>
<tr>
<td>C_{oss}</td>
<td>Switch output capacitance</td>
<td>30 pF</td>
</tr>
<tr>
<td>f_{sw}</td>
<td>Switching frequency</td>
<td>1 - 100 kHz</td>
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</tbody>
</table>
Figure 5.15. RMS values of the $Z_{TC}$ output voltages in the simulation of the basic SC isolation cell circuit. The equivalent circuit is shown in Fig. 5.12 and the circuit parameter settings are listed in Table 5.3.

From Figures 5.14 and 5.15 it can be seen that TC increases as $C_{oss}$ or $f_{sw}$ increases. However, it is possible to meet the TC requirements in IEC60950. In order to reduce TC, it is preferred to have low $C_{oss}$ and low $f_{sw}$. Nevertheless, low $f_{sw}$ has a significant negative impact on the power density, as discussed in section 5.7. Therefore, the study continues to explore TC reduction approaches, as presented in the following section.

5.5. TC Reduction Approaches

5.5.1. Increasing the CM Impedance

The first approach is to block the TC with a larger CM impedance. CM chokes can be added to increase the CM impedance, and this is valid since the ac/dc stage of the off-line
power supply has EMI filters. However, as shown in Fig. 5.16, adding extra CM chokes with reasonable values (up to multi mH) into the TC loop does not cause any significant change of the TC. This is because the TC loop already has a dominating CM impedance, which is the 500-Ω resistance in the $Z_{TC}$. The added CM impedance can reduce the peak value of $I_{TC}$, as shown in Fig. 5.13. However, it does not reduce its RMS value when the switching cycle is much greater than the circuit time constant, so it does not reduce the output RMS voltage of $Z_{TC}$.

![Figure 5.16](image)

Figure 5.16. RMS values of the $Z_{TC}$ output voltage in the simulation of the basic SC isolation cell circuit. The equivalent circuit is shown in Fig. 5.12 and the circuit parameter settings are listed in Table 5.3.
Table 5.4. Simulation parameters for studying the impact of $f_{sw}$ on the $I_{TC}$ (embodied as the output voltage of $Z_{TC}$) in the basic SC isolation cell circuit.

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
<th>Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{ac}$</td>
<td>Line input (only the negative half line cycle applies as the CM voltage source)</td>
<td>60 Hz / 120 V_{ac, rms}</td>
</tr>
<tr>
<td>$L_{stray}$</td>
<td>Loop inductance</td>
<td>60 nH - 100 mH</td>
</tr>
<tr>
<td>$C_{oss}$</td>
<td>Switch output capacitance</td>
<td>30 pF</td>
</tr>
<tr>
<td>$f_{sw}$</td>
<td>Switching frequency</td>
<td>1 - 100 kHz</td>
</tr>
</tbody>
</table>

5.5.2. Bypassing the TC

The idea of this approach is to bypass the TC from the $Z_{TC}$ with a shunt path which has lower CM impedance, so that the TC sensed by the $Z_{TC}$ can be reduced.

One attempt is to add Y capacitors between the output ends and the earthing ground. This is, however, infeasible for equipment without the protective earthing conductor. In addition, there also exists a regulation on the ground fault current level, which sets a limit on the Y capacitance. Furthermore, because the output end where a human body touches is random, it is possible to form a diagonal connection between the CM voltage source and the $Z_{TC}$. If this happens, as shown in Fig. 5.17, the parallel CM-path circuit branches between points $C$ and $D$ are not symmetrical because of the switching sequence. In this case, instead of reducing the TC, additional TC will be resulted by the DM power delivery.
Figure 5.17. Unsymmetrical CM conduction path caused by the diagonal connection between the CM voltage source and the $Z_{TC}$, with Y capacitors added at the output. This results in additional TC caused by the DM power delivery.

Another attempt to bypass the TC from the $Z_{TC}$ is to add a shunt current source in parallel with the converter, as shown in Fig. 5.18.

Figure 5.18. Adding a shunt current source in parallel with the converter to bypass the $I_{TC}$ from the $Z_{TC}$. 
This added shunt current source compensates the $C_{oss}$ charging current by providing lower impedance for the CM leakage current to flow. As a result, it reduces the TC sensed by the $Z_{TC}$. A simulation is conducted in PSIM to verify this solution. This simulation is based on a detailed circuit model, where device parasitics are considered and each switch is composed of two MOSFETs in an anti-series connection. The simulation circuit parameters are shown in Table 5.5. The simulation results before and after adding this shunt current source are presented in Fig. 5.19.

Note that this is an effective approach to reduce the TC sensed by the $Z_{TC}$, so as to meet the IEC60950 requirements. However, this approach requires a high band-width current-sensing circuit and current source circuit, both of which are challenging to design and implement. In addition, the current source circuit is bridging the two isolated sides of the converter, and thus it also needs to sustain high insulation voltage, which is $3kV_{ac, rms}$ for the reinforced insulation.

Table 5.5. Simulation parameters for the shunt current source solution to reduce the TC of the basic SC isolation cell circuit.

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
<th>Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{ac}$</td>
<td>Line input (only the negative half line cycle applies as the CM voltage source)</td>
<td>60 Hz / 120 $V_{ac, rms}$</td>
</tr>
<tr>
<td>$L_{stray}$</td>
<td>Loop inductance</td>
<td>60 nH</td>
</tr>
<tr>
<td>$C_{oss}$</td>
<td>Switch output capacitance</td>
<td>30 pF</td>
</tr>
<tr>
<td>$f_{sw}$</td>
<td>Switching frequency</td>
<td>2 kHz</td>
</tr>
</tbody>
</table>
Figure 5.19. Simulation results (a) before and (b) after adding a shunt current source to bypass the TC from the $Z_{TC}$. 

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5.5.3. Preventing the TC Generation

The idea of this approach is to prevent the pulse TC generation at the turn-on event. To be more specific, it is to recycle the $C_{oss}$ energy dissipated in the switches, and to utilize that energy to charge up the $C_{oss}$ of the complementary switches during the dead time. Thus, it no longer draws energy from the CM voltage source to charge up the $C_{oss}$ at turn-on events, and therefore, the pulse TC can be eradicated. The principle is the same as the ZVS operation of traditional power converters. In the SC isolated cell circuit, if the ZVS operation can be achieved during the dead time as shown in Fig. 5. 20 (b), the $C_{oss}$ energy can be transferred to the complementary switches.

![Operation waveforms](image)

Figure 5.20. Operation waveforms (a) before and (b) after implementing the ZVS operation to prevent the TC generation.

However, in the SC isolated cell circuit, ZVS operation cannot be achieved naturally. This is because the load current does not flow into or out of the junction points between the complementary switch pairs (e.g., $S_1$ and $S_3$). It means there are no switching intervals where load currents can be used to discharge the $C_{oss}$ of one switch and charge the $C_{oss}$ of its complementary switch, as if in a phase leg of traditional half/full-bridge converters. In
fact, the attempt to achieve ZVS operation utilizing the load currents is to cycle the energy between $C_{oss}$ and the external CM voltage source. While this is infeasible because of the circuit structure, another external voltage source can be utilized to force ZVS operation.

The gate-drive power supply is chosen as the alternative voltage source. In the gate-drive circuit, auxiliary circuits are added to manually force the charging and discharging of the $C_{oss}$. As shown in Fig. 5.21, for each ac switch, two bidirectional current source circuits can be added into the gate-drive circuit. Equivalently, they serve as distributed current sources charging or discharging the $C_{oss}$, as shown in Fig. 5.22.

Figure 5.21. The solution to manually force ZVS operation by adding bidirectional current-source circuits in the gate drive to charge or discharge the switch $C_{oss}$.

The centralized current source solution shown in Fig. 5.18 is a feedback compensation for the TC reduction. It senses the TC online, and then generates a cancelling current to reduce the TC. However, the forced ZVS operation solution shown in Figures 5.21 and 5.22 is a feed-forward compensation. It generates the command for distributed current

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sources to charge the $C_{oss}$ voltage to the sensed $V_{CM}$, so that TC will be eliminated in the following switching events. Online $V_{CM}$ sensing or prediction is therefore required for this solution. As discussed in section 5.4.1, the $V_{CM}$ is predictable for Class I off-line power supplies with grounded output, so this feed-forward TC compensation is achievable.

Figure 5.22. Equivalent circuit to manually force ZVS operation with bidirectional current-source circuits in the gate drive to charge or discharge the switch $C_{oss}$.

Compared with the centralized current source solution shown in Fig. 5.18, this solution has its own pros and cons. The pros include: 1) because the charging and discharging are both implemented in the dead time, the bandwidth of the current source can be lower; and 2) there is no need for additional power supplies because the current sources share the same power supply of the gate-drive circuit. The cons are the challenges in the design and control of the current source circuits. These circuits must charge one switch and discharge its complementary switch simultaneously and the charging and discharging currents must be coordinated, otherwise additional TC will result, as discussed in detail below.
A series of analyses and simulations are conducted to investigate how the operation of the distributed current sources influence the TC. The first case studied is shown in Fig. 5.23. It is to enable the current sources to charge only two switches ($S_{31}$ and $S_{41}$) during dead time, without charging or discharging any other switches. The initial voltages across the switches are labeled in purple on top of the switches in the figure.

Figure 5.23. The first case studied to implement forced ZVS operation. It is only to charge two switches ($S_{31}$ and $S_{41}$) during the deadtime, without charging or discharging any other switches. The simulation results show that additional TC is generated.

In this case study, it can be seen from the simulation results that: 1) the $C_{oss}$ of $S_{31}$ and $S_{41}$ are not fully charged to $V_{CM}$; 2) the $C_{oss}$ of $S_{32}$, $S_{42}$, $S_{12}$, and $S_{22}$ are charged unintentionally, and the $C_{oss}$ of $S_{11}$ and $S_{21}$ are discharged unintentionally; and 3) an additional TC results in dead time as a result of the operation of the current sources. The reason behind the results is the KVL applied for the $V_{CM}$ and the voltage across all the
switches. Without coordinated discharging of the complementary switches (S_{11} and S_{21}),
the compensation current flows through Z_{TC}, which is against our intention.

The second case studied is shown in Fig. 5.24. It is to enable the current sources to
charge two group of switches (S_{31} and S_{32} in one group, and S_{41} and S_{42} in the other group)
during the dead time, without charging or discharging the other switches. The initial
voltage of the switches are labeled in purple on top of the switches in the figure.

![Figure 5.24](image)

Figure 5.24. The second case studied to implement forced ZVS operation. It is to charge
two group of switches together, without discharging any other switches. The results show
additional TC is generated.

In this case study, it can be seen from the simulation results that: 1) the \( C_{oss} \) of S_{31} and
S_{41} are not fully charged to \( V_{CM} \); 2) the \( C_{oss} \) of S_{12}, and S_{22} are charged unintentionally, and
the \( C_{oss} \) of S_{11} and S_{21} are discharged unintentionally; and 3) an additional TC results in
dead time as a result of the operation of the current sources. The same reason stands behind
the results, which is the KVL for the \( V_{CM} \) and the voltage across all the switches. It may
then be inferred that coordinated discharging of the complementary switches (S_{11} and S_{21}) must be implemented at the same time, which leads to a third case study.

The third case study is shown in Fig. 5.25. It charges two groups of switches (S_{31} and S_{32} in one group, and S_{41} and S_{42} in the other group) during dead time, and in the meantime discharges their complementary switches (S_{11} and S_{21}). The initial voltages of the switches are labeled in purple on top of the switches in the figure. In this case study, it can be seen from the simulation results that: 1) the voltages across S_{11} and S_{21} are fully transferred to S_{31} and S_{31}, so forced ZVS operation is successfully achieved; and 2) no additional TC is caused in the dead time. As a result, the touch current is eliminated in this case study.

![Image](image.png)

Figure 5.25. The third case studied to implement forced ZVS operation. It is to charge two group of switches together, while discharging their complementary switches. The results show the voltage across the switches is fully transferred, and the TC is eliminated.

Although the third case study shows that forced ZVS operation is achievable, the implementation of the distributed current sources is still challenging. Two types of current
source circuits are considered, including a switching-type current source circuit and a linear-type current source circuit. A switching-type current source circuit can be designed based on a bidirectional boost converter, as shown in Fig. 5.26. An enabling switch $S_{en}$ is required to turn on and off the current source, so as to prevent the continuous charging of $L_{com}$ when the main power-loop switch $S_x$ is closed (i.e., the $C_{oss}$ is shorted by $S_x$). However, the design of the converter is challenging for multiple reasons.

First, the switches in the boost converters must have the same breakdown voltage rating as the main power-loop switches, because the isolation voltage also is imposed on them. In order to meet the IEC60950 isolation voltage requirement, the breakdown voltage rating needs to be higher than 3 kV $ac, rms$ for reinforced insulation. Second, when built as a constant current source, the boost converter needs a large inductance and freewheeling path to shunt the inductor current. However, the converter is difficult to discharge the switch $C_{oss}$ with the large inductance. Third, the voltage ratio of the boost converter is high (>20), and voltage control is difficult with a capacitive load. Lastly, the switch $C_{oss}$ to be charged and discharged is non-linear, so the charging and discharging currents are difficult to coordinate.

![Diagram of Compensation Current-Source Circuit](image)

Figure 5.26. Example of a switching-type current source circuit, based on a bidirectional boost converter.

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On the other hand, a linear current source circuit can be designed based on BJTs operating in their saturation region. Such a current source is able to supply a relatively constant current despite the variation of output voltage. An example of a unidirectional linear current source using PSSI2021SAY is shown in Fig. 5.27. It can be switched on or off by controlling the enable pin (i.e., the IN/OUT pin). However, the linear current source only works when the input voltage is higher than the output voltage, so it is impossible to use the gate drive power supply (~20 V) to charge the switch $C_{oss}$ up to the line input voltage. In addition, the linear current source is a unidirectional circuit, so two sets of the linear current source circuits are necessary for charging and discharging, respectively. As a result, sixteen linear current source circuits are required in total for the entire SC isolated dc/dc converter, which increases the circuit complexity significantly.

![Figure 5.27. Example of a unidirectional, linear-type current source circuit.](image)

In summary, both the switching-type current source circuit and the linear-type current source circuit have their unique limitations in implementation to achieve the forced ZVS.
operation, which aims to fully eliminate the TC. However, in fact it does not necessarily need the complete elimination of TC to meet the IEC60950 requirements. Instead, it also works if the TC is partially compensated such that it is regulated below the TC limits in the IEC60950. This leads to the fourth solution, as discussed in detail below.

5.5.4. Partially Compensating the Switch $C_{oss}$ Charging Current

The idea of this approach is to partially compensate the switch $C_{oss}$ charging current at the turn-on transients, so that it draws less energy out of $V_{CM}$, and thus TC is reduced below the IEC60950 limits. To provide the compensation charging current, distributed current-source circuits are added to the gate-drive circuits, as shown in Figures 5.21 and 5.22.

The attempt to achieve ZVS operation is, in fact, to cycle the energy between $C_{oss}$ and the external voltage source, so the $C_{oss}$ energy is not lost. However, in this solution the $C_{oss}$ energy is not recycled, so an external voltage source is needed to repetitively transfer the energy to $C_{oss}$. For this reason, the solution to partially compensate the switch $C_{oss}$ charging current generates more power loss and thus, is less energy efficient.

To implement the compensation current source, a bidirectional boost converter can be designed, as shown in Fig. 5.26. However, as discussed in section 5.5.3, such a design has many limitations. Thus, a buck-boost converter-based current source circuit is proposed, as shown in Fig. 5.28. This circuit is unidirectional because it needs to supply only the compensation charging current ($I_{com}$) at the turn-on transients, so only one active switch ($S_{com}$) is needed. The negative power supply required by the circuit is generated from the
gate drive power supply, as they share the source of the main power-loop switch as the ground reference.

Figure 5.28. Example of a switching-type current source circuit based on the buck-boost converter, with the current flows signified at the S1 turn-on event.

The operation of waveforms of this current source circuit is shown in Fig. 5.29.

Figure 5.29. Operation of waveforms of the buck-boost current source circuit.
The key parameters of the circuit are derived as follows. After the switch $S_{com}$ is activated, the inductor current is charged up linearly. At $t_1$, the inductor current is charged up to:

$$I_{com}(t_1) = \frac{V_{CC} \cdot t_1}{L_{com}}.$$  \hfill (5.2)

At $t_1$, $S_{com}$ is turned off, and then $L_{com}$ starts to resonate with $C_{oss}$, transferring its energy to $C_{oss}$, until the voltage of $C_{oss}$ reaches $V_{CM}$. Assuming $C_{oss}$ has constant capacitance and its voltage is charged only with the energy from $L_{com}$, the total energy transferred from $L_{com}$ to $C_{oss}$ is:

$$\frac{L_{com} \cdot [I_{com}(t_1)]^2}{2} = \frac{C_{oss} \cdot V_{CM}^2}{2}.$$  \hfill (5.3)

Combining (5.2) and (5.3), the on time of the switch $S_{com}$ is derived as:

$$t_1 = \frac{V_{CM} \cdot \sqrt{L_{COM} C_{oss}}}{V_{CC}}.$$  \hfill (5.4)

In order to reduce the TC effectively, the energy transfer from $L_{com}$ to $C_{oss}$ should occur as quickly as possible. The resonance frequency between $L_{com}$ and $C_{oss}$ determines the energy transfer speed. Assuming that the energy transfer is completed within the voltage rise time ($t_f$) of the main-power-loop switch during the switching transient:

$$t_f = \frac{T_s}{4} = \frac{2\pi \cdot \sqrt{L_{com} C_{oss}}}{4}.$$  \hfill (5.5)
Based on (5.5), the $L_{com}$ to achieve the required energy transfer speed is:

$$L_{com} = \frac{\left(\frac{2f_c}{\pi}\right)^2}{C_{oss}}. \quad (5.6)$$

The simulation results of the buck-boost converter-based current source circuit are shown in Fig. 5.30. TC is partially compensated by the $I_{com}$ at the turn-on transients. Because of such compensation at every turn-on transient, the overall TC is reduced.

Figure 5.30. Operation waveforms of the buck-boost current source circuit.
5.6. **Extended Topologies with Semiconductor-based Galvanic Isolation**

5.6.1. **Isolated DC/DC Converter with a High Voltage Transfer Ratio**

The SC isolation cell shown in Fig. 5.4 is a basic topology without a voltage transfer ratio. It can serve as a basic building block to derive advanced topologies with high voltage transfer ratios. By stacking up these building blocks, an isolated converter with a 3X voltage transfer ratio is derived, as shown in Fig. 5.31.

![Diagram of isolated DC/DC converter](image)

Figure 5.31. (a) A 3X isolated boost dc/dc converter (where all switches are ac switches with bidirectional blocking) and (b) the two switching phases of the converter.

Following this idea, advanced SC circuits also can be modified to achieve galvanic isolation. For example, the Dickson converter can be modified into an isolated dc/dc converter, as shown in Fig. 5.32.
Figure 5.32. (a) A 4X isolated Dickson converter, and (b) the equivalent circuits of the two switching phases.

5.6.2. Isolated DC/DC Converter with Extended Isolation Voltage

The isolation voltage rating of the basic SC isolation cell circuit equals the switch breakdown voltage. To achieve a higher isolation voltage, isolated dc/dc converters can be derived from the basic SC isolation cell circuit. As shown in Fig. 5.33 (a), a converter is composed of several SC isolation cells connected in series. These cells take turns operating and delivering energy to the next one. The enabling signals of the cells are shown in Fig. 5.33 (b). This structure and control strategy enables a higher isolation voltage. A cell that
is not enabled has the same isolation voltage rating as the switch’s voltage rating. When it is enabled and begins to operate, it loses its isolation voltage blocking capability because its switch body diodes would conduct. However, out of the $n$ series-connected cells, there is only one cell operating at a time, so the other ($n-1$) connected cells will continue to provide the isolation voltage blocking capability.

The number $n$ needed in the converter depends upon the voltage rating of the switches. For example, to meet the 3 kV$_{ac, \text{rms}}$ reinforced isolation voltage requirement in IEC60950, if 1.2 kV rated switches are used, the converter needs four cells in series, to provide a 4.8 kV isolation voltage rating. If 4.5 kV rated switches are used, the converter needs only one cell.

**Figure 5.33.** (a) Isolated dc/dc converter with extended isolation voltage and the insulation test schematic; (b) enabling signals of the SC isolation cells ($n=3$, for example).
5.6.3. *Isolated DC/DC Converter with a Voltage Regulation Function*

The basic SC isolation cell circuit and the isolated dc/dc converters shown in Figures 5.31-5.33 all have fixed voltage transfer ratios, which lack the voltage regulation function. These converters can serve as the DCX in two-stage ac/dc or dc/ac converters, where the voltage regulation function is provided by the ac/dc or dc/ac stage. For applications where voltage regulation of the isolated dc/dc converter is needed, inductors must be integrated into the converter. Fig. 5.34 shows a derived buck-boost converter with semiconductor-based galvanic isolation. An additional switch S5 provides the freewheeling current path for the inductor during dead time.

![Diagram of an isolated buck-boost dc/dc converter with a voltage regulation function](image)

Figure 5.34. An isolated buck-boost dc/dc converter with a voltage regulation function (all switches are ac switches with bidirectional blocking capability).
5.6.4. *Isolated AC/DC converters and Isolated DC/AC converters*

Isolated ac/dc converters can be designed with a two-stage structure, including an ac/dc stage with PFC function, and a DCX with the semiconductor-based galvanic isolation, as shown in Fig. 5.35. Such converters can be used in off-line power supplies, such as the vehicle on-board charger, LED driver, power adapters for consumer electronics, etc.

![Diagram of an ac/dc converter](image)

Figure 5.35. Two-stage structure of an ac/dc converter.

Isolated dc/ac converters also may be designed with a two-stage structure, including a DCX with a semiconductor-based galvanic isolation, as shown in Fig. 5.36. Applications of such converters include the PV inverters.

![Diagram of a dc/ac converter](image)

Figure 5.36. Two-stage structure of a dc/ac converter.

5.7. *Design toward High Efficiency and High Power Density*

This section presents the design considerations of the basic SC isolation cell circuit, to achieve high efficiency and high power-density for the DM power delivery.
5.7.1. Switches

The first step of the design is to select switches for the converter. To meet the IEC60950 isolation voltage requirement, the switches must have high breakdown voltages to sustain 1.5 kV<sub>ac, rms</sub> for the basic and supplementary isolation, or 3 kV<sub>ac, rms</sub> for the reinforced insulation. In addition to the high breakdown voltage, the switches also need to have bidirectional blocking capability, because the applied isolation voltage in the test is bidirectional. For each ac switch, instead of using two discrete power devices in anti-series connection, it is preferred to use a single discrete device or device die with bidirectional blocking, to achieve lower device parasitics, a smaller footprint, and higher power density. In addition, to reduce the TC, the switches also need to have low output capacitance, as discussed in section 5.4.3.

To perform at high efficiency, the switches must have low on-resistance (<i>R_{ds,on}</i>), to reduce the conduction loss. The ideal converter efficiency is:

\[
\eta = \frac{R_{\text{load}}}{R_{\text{load}} + n \cdot R_{ds\_on}},
\]

(5.7)

where <i>R_{load}</i> is the load resistance and <i>n</i> is the total number of switches (<i>n</i>=8 if each ac switch is composed of two switches in anti-series connection).

In addition, it is preferred to have fast switching speed, to reduce the switching loss. Also, to perform high converter power density, the switches need to have high thermal conductivity and high maximum junction temperatures.

A comparison between the critical parameters of state-of-the-art SiC MOSFETs vs. Si MOSFETs/IGBTs is shown in Table 5.6. It can be seen that it is impractical to implement
the semiconductor-based galvanic solution with Si devices because they either cause low efficiency because of the high on-resistance, or cause excessive TC because of the large output capacitance. To apply multiple devices in parallel is a common practice to reduce the device on-resistance, but it will increase the switching loss and cause a higher TC because of the increased device output capacitance. The latest SiC devices, the coming vertical GaN devices [149-151], and the emerging bidirectional power devices [152] provide unprecedented properties, which potentially enable their practical implementation.

Table 5.6. Comparison between critical parameters of state-of-the-art SiC MOSFETs vs. Si MOSFETs/IGBTs.

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Material</th>
<th>Continuous Drain Current @ 25 °C</th>
<th>Drain-Source Breakdown Voltage</th>
<th>Drain-Source On-State Resistance (R&lt;sub&gt;ds_on&lt;/sub&gt;)</th>
<th>Output Capacitance (C&lt;sub&gt;oss&lt;/sub&gt;) @ V&lt;sub&gt;ds&lt;/sub&gt;=200 V</th>
</tr>
</thead>
<tbody>
<tr>
<td>C2M0025120D</td>
<td>SiC</td>
<td>90 A</td>
<td>1200 V</td>
<td>0.025 Ω</td>
<td>350 pF</td>
</tr>
<tr>
<td>CM75DU-24F</td>
<td>Si</td>
<td>75 A</td>
<td>1200 V</td>
<td>0.025 Ω</td>
<td>19000 pF</td>
</tr>
<tr>
<td>C2M1000170D</td>
<td>SiC</td>
<td>4.9 A</td>
<td>1700 V</td>
<td>1.1 Ω</td>
<td>191 pF</td>
</tr>
<tr>
<td>WPH4003</td>
<td>Si</td>
<td>2.5 A</td>
<td>1700 V</td>
<td>8.2 Ω</td>
<td>850 pF</td>
</tr>
</tbody>
</table>

5.7.2. Switching Frequency

The next step is to determine the switching frequency based on the output capacitance of the selected switches and the TC and PPC limits in IEC60950. As discussed in section 5.4.3, if no measures are taken to actively reduce the TC, the converter needs to operate at a low switching frequency to suppress the TC below the IEC60950 limits. However, a low switching frequency has significantly negative impacts on the power density and energy efficiency. At a low switching frequency, the converter requires higher energy stored in
the switched capacitors, and this leads to large capacitance of the switched capacitor and thus, lower power density. In addition, to achieve the same average DM output current, the RMS current of the switches and switched capacitors increases as the switching frequency decreases, which causes higher conduction loss and thus, lower efficiency. Nevertheless, as discussed in section 5.5, the switching frequency can be increased by adding auxiliary current source circuits to reduce the TC.

5.7.3. Passive Components

Once the switching frequency is selected, the switched capacitors \((C_2 \text{ and } C_3)\) of the SC isolation cell circuit can be designed based on the DM power delivery requirements. In operation, the energy transferred by the switched capacitor \(C_2\) is:

\[
\Delta E = \frac{C_2 \cdot V_1^2}{2} - \frac{C_2 \cdot V_2^2}{2} = C_2 \cdot V_{dc} \cdot \Delta V_{dc},
\]

where \(V_1\) and \(V_2\) are the \(C_2\) voltage before and after the energy transfer; \(V_{dc}\) is the average \(C_2\) voltage; and \(\Delta V_{dc}\) is \(C_2\) voltage ripple.

The energy transferred by \(C_2\) also is determined by the load power \((P_{load})\) within the half switching cycle \((T_{sw})\), as described in:

\[
\Delta E = \frac{P_{load} \cdot T_{sw}}{2} = \frac{P_{load}}{2f_{sw}}.
\]

Based on (5.8) and (5.9), the required capacitance of \(C_2\) is derived:

\[
C_2 = \frac{P_{load}}{2f_{sw} \cdot V_{dc} \cdot \Delta V_{dc}}.
\]
Choices of the state-of-the-art capacitors are listed in Table 5.1. All capacitor electrical characteristics should be considered in the capacitor selection, including the capacitance, voltage rating, current rating, ESR, ESL, and operation temperature.

The DM currents can be configured into two general patterns, including: (a) the hard-switching current pattern; and (b) the resonant current pattern with ZCS on and off [86], as shown in Fig. 5.37.

The equivalent circuit for the DM current loop is a series RLC circuit, where the loop resistance is a parasitic resistance of the PCB traces and the components, and the loop inductance is the stray inductance of the PCB traces and the components. The hard-switching current pattern can be achieved with a large capacitance of the switched capacitors. The resonant current pattern can be achieved when the switching frequency

Figure 5.37. Two DM current patterns including (a) the hard-switching current pattern, and (b) the resonant current pattern with ZCS on and off.

The equivalent circuit for the DM current loop is a series RLC circuit, where the loop resistance is a parasitic resistance of the PCB traces and the components, and the loop inductance is the stray inductance of the PCB traces and the components. The hard-switching current pattern can be achieved with a large capacitance of the switched capacitors. The resonant current pattern can be achieved when the switching frequency
matches the frequency of the resonance between the switched capacitors and the DM current loop inductance.

To achieve both high efficiency and high power density, it is preferred to operate the converter at a high switching frequency and achieve the resonant currents with ZCS on and off, with the TC actively suppressed to meet the safety standards. In this way, both the switching loss and conduction loss is minimized and a high power density is achieved.

5.8. Preliminary Prototype and Experimental Verifications

A preliminary 400-V, 400-W prototype of an SC isolation cell circuit is shown in Fig. 5.38. The specifications of this converter are shown in Table 5.7. The prototype is built to verify both the DM power delivery performance and the CM isolation performance. To verify the TC without the compensation current source circuits first, this preliminary prototype is built to work at 1 kHz.

Figure 5.38. A preliminary 400-V, 400-W prototype of the SC isolation cell circuit.
Table 5.7. Specifications of the preliminary SC isolation cell circuit prototype.

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{in}$</td>
<td>Input voltage rating</td>
<td>400 V</td>
</tr>
<tr>
<td>$P_{out}$</td>
<td>Output power rating</td>
<td>400 W</td>
</tr>
<tr>
<td>$C_1, C_2, C_3$</td>
<td>Input/output capacitors and switched capacitors</td>
<td>450-V/560-µF, Electrolytic</td>
</tr>
<tr>
<td>$L_{stray}$</td>
<td>Stray inductance</td>
<td>46 nH</td>
</tr>
<tr>
<td>$S_1$ to $S_4$</td>
<td>1.7-kV SiC MOSFET</td>
<td>C2M1000170D</td>
</tr>
<tr>
<td>$f_s$</td>
<td>Switching frequency</td>
<td>1 kHz</td>
</tr>
<tr>
<td></td>
<td>Prototype dimensions</td>
<td>83 mm×73 mm ×65 mm</td>
</tr>
</tbody>
</table>

5.8.1. DM power delivery test

The converter has hard-switching DM currents. The DM power delivery experimental waveforms are shown in Fig. 5.39. At low switching frequency (1 kHz), the switching loss is negligible. The conduction loss caused by the high on-resistance of the switches is the major loss of the converter. The converter efficiency curve is shown in Fig. 5.40.

![Waveform Diagram](image)

Figure 5.39. Experimental waveforms of the DM power delivery at 100-W output power.
Figure 5.40. Experimental DM power delivery efficiency of the prototype.

5.8.2. TC Measurement

A TC test is conducted with the SC isolation cell circuit prototype connected after a diode rectifier circuit, as shown in Fig. 5.41. The test is done without any auxiliary circuits to actively reduce the TC. The experimental waveforms are shown in Fig. 5.42.

Figure 5.41. TC test of the isoaltion cell circuit prototype in an off-line power supply application.
Figure 5.42. Experimental results of the TC measurement with a 120-V<sub>rms</sub> CM voltage source. The weighted touch current result is 0.24 mA, which meet the IEC60950 standard requirement (0.25 mA).

Fig. 5.42 shows that the weighted touch current result is 0.24 mA, which meet the IEC60950 standard requirement (0.25 mA). The test result is without any auxiliary circuits to actively reduce the TC.

5.8.3. Test of the TC Reduction Circuit

As discussed in 5.5.4, TC can be reduced by partially compensating the switch $C_{oss}$ charging current at the turn-on transients. To implement this solution, a set of buck-boost converter based current source circuits are designed and added to each switch, to charge up the switch $C_{oss}$. The circuit diagram is shown in Fig. 5.28 and repeated in Fig. 5.43. The test waveforms are shown in Fig. 5.44. By adjusting the pulse width of $S_{com}$, the $C_{oss}$ charging current supplied by the current source circuit can be modulated.
Figure 5.43. Auxiliary current-source circuit to partially compensating the current for charging the switch $C_{oss}$ at the turn-on transients.

Figure 5.44. Test waveforms of the auxiliary current-source circuit.
Fig. 5.44 shows that the added auxiliary current-source circuit can charge up the $C_{oss}$ of S2. With such auxiliary circuits functioning during converter’s operation, the TC can be reduced and thus improved CM isolation impedance can be achieved. Further tests are required to verify the effectiveness of this approach. This approach will enable the converter to operate at higher switching frequency and achieve higher power density, while meeting the safety standard requirements.

5.9. Conclusions

In this chapter, a semiconductor-based galvanic isolation solution is proposed for isolated power converters. The basic idea of this solution is to deliver the DM load power via active semiconductor switches during their ON states, while sustaining the CM voltage and blocking the CM leakage current with those semiconductor switches during their OFF states. To implement this idea, circuit topologies are derived from SC circuits, to deliver valid galvanic isolation performance (e.g. insulation voltage, touch current, and protective conductor current) that meets the safety standards (e.g. IEC60950).

The semiconductor-based galvanic isolation solution potentially enables much higher power density of isolated dc/dc converters, compared to traditional galvanic isolation solutions, including the inductive-coupling, capacitive-coupling, and optical-coupling based solutions. A review of those traditional galvanic isolation solutions is presented, and their power density limitations are discussed. The SC circuits employ only semiconductor switches and capacitors, and therefore results in the elimination of magnetic component, simple structure, and less number of components. To date, capacitors perform much higher
power density and energy density compared with magnetic components. In addition, capacitors and switches are also easier to be integrated into power modules with packaging techniques. As results, higher power density of isolated dc/dc converters is achievable with the proposed semiconductor-based galvanic isolation solution.

The solution looks simple, but has many challenges. On one hand, it needs to provide valid CM isolation performance that meets safety standard (e.g. IEC60950) requirements. This requires semiconductor power devices with high breakdown voltage (1.5 \( kV_{ac, \text{rms}} \) for basic and supplementary isolation, and 3 \( kV_{ac, \text{rms}} \) for reinforced insulation), bidirectional blocking capability, and low switch \( C_{oss} \). The comparison between the state-of-the-art Si power devices and WBG power devices shows that, it is impractical to implement the proposed solution with Si devices as they cause either low efficiency due to high on-resistance or excessive TC due to large \( C_{oss} \). However, the latest SiC devices and the coming vertical GaN devices provide unprecedented device properties as desired, which bring new opportunities for the practical implementation.

On the other hand, the proposed solution needs to provide high power density and high efficiency. As the switching frequency is limited by the TC requirement, conduction loss of switches and capacitors is a major part of the power loss, so low switch on-resistance and low capacitor ESR are required. The low switch on-resistance is another important reason why we need WBG power devices for this solution. Low switching frequency is not preferred as it significantly increase the size of capacitors, although it helps reducing the TC. As the switching frequency increases, effective TC reduction is needed, and different
approaches to reduce the TC are discussed in section 5.5. Auxiliary current-source circuits are designed and distributed to each switch, to compensate the $C_{oss}$ charging currents.

Other challenges for the proposed solution include a large voltage transfer ratio, voltage regulation function, and applications into isolated ac/dc and dc/ac power converters. To address these challenges, extended topologies are derived, as shown in section 5.6.

A preliminary prototype of the SC isolation cell is designed to verify the DM power delivery performance and the TC performance. The test results are presented in section 5.8. It is shown that TC results meet the IEC60950, and the designed auxiliary current-source circuits can effectively reduce the TC.
Chapter 6. Conclusions and Future Work

6.1. Conclusions

This dissertation studies isolated power converters based on SC circuits, aiming to achieve high power density, high efficiency, and high CM isolation performance. The major contributions of the work include:

1) This work first explores the integration of transformer into SC circuits, aiming to combine the benefits of both the transformer and the SC circuit into a single circuit. A bidirectional QSC dc/ac circuit is therefore derived to replace traditional half bridge or full bridge circuits. With a transformer integrated, the QSC dc/ac circuit provides galvanic isolation with a high voltage transfer ratio. The transformer also enables ZVS operation of the circuit. In addition, compared to traditional half bridge or full bridge circuits, the QSC dc/ac circuit reduces the voltage stress on switches to 2/3 dc-link voltage, and reduces the voltage stress on transformer and switched-capacitors to 1/3 dc-link voltage. The reduced voltage stress on switches enable more choices of low-voltage power devices which are more efficient because of better figure of merit. The reduced voltage stress on transformer enables lower transformer turns ratio, less number of turns of the winding, lower winding loss, and lower transformer leakage inductance.

2) Based on the proposed QSC dc/ac circuit, an isolated QSC PWM converter is proposed to serve as an auxiliary power supply in EVs/HEVs, managing a bidirectional...
power flow between the HV battery and the LV dc bus. The converter operation principles, ZVS operation analyses, simulation and experimental verifications are presented. The features of the QSC circuit including reduced voltage stress on switches and transformer are remained. Design guidelines are given to estimate the key circuit parameters, including the capacitance of the switched capacitors, the transformer dc-bias flux density, and the average currents of the post-stage inductors. A 1 kW prototype is built with SiC MOSFETs on the primary side. The soft-switching peak efficiency of the converter operating at 500 kHz switching frequency is 96% for the buck-mode, and 91% for the boost-mode.

3) The small-signal model and controller design of the isolated QSC PWM converter are presented. To maintain ZVS operation, the output power of the converter is regulated by the switching frequency modulation. This control method is essentially adjusting the duration of the switching intervals. A small-signal model of the converter is derived by the method of state-space averaging. Open-loop response simulation results from the derived small-signal model and a detailed circuit model are provided and compared. The simulation results showcase the effectiveness of the derived small-signal model. For better performance of the input voltage disturbance rejection, a closed-loop voltage controller with feed-forward compensation for the switching frequency is designed to regulate the output voltage. Comparison of closed-loop simulation results from the small-signal model and the detailed circuit model verified the effectiveness of the closed-loop controller. With feed-forward compensations, the oscillation in the system can be significantly damped and the response time is reduced. Experiment results from the 1-kW prototype with digital
control implemented in DSP verified the effectiveness of the closed-loop voltage control based on switching-frequency modulation.

4) An isolated QSC resonant converter is proposed to serve as a DCX for the isolated dc/dc conversion in off-line power supply applications, offering high power density and high efficiency. Similar to the Φ2 resonant converter, the converter is operated most efficiently at fixed switching frequency and duty ratio applied, and it features trapezoidal voltage waveforms on all switches. Full soft switching is achieved combining ZCS on, near ZCS off, ZVS on, and ZVS off within a wide load range, so the switching loss is minimized. The features of the QSC circuit including reduced voltage stress on switches and transformer are remained. For demonstration, a 90-W, 88-V/19-V, 700-kHz prototype is built with 100-V eGaN FETs. The transformer design and PCB layout are presented to minimize the transformer leakage inductance and stray inductance. The prototype achieved a power density of 172 W/inch³, and a flat efficiency curve with a peak value of 96 %. Furthermore, a 65-W, two-stage, off-line power adapter is designed based on the isolated QSC resonant converter. A 65-W, 380-V/19-V, 2-MHz isolated QSC resonant converter prototype is built with Enhancement-mode GaN HEMTs. It has an estimated high efficiency of 97.5%, and a high power density of 275 W/inch³. The proposed isolated QSC resonant converter is not limited to low-power applications. It also has the scalability to be applied in high-voltage, high-power applications. The reduced voltage stress on switches and transformer are of particular interest for high voltage converters such as the solid-state transformers, where challenges exist in the development and application of high-voltage (>10 kV) SiC power devices and also the insulation design of the high-voltage transformer.
Efforts should be made thus in such directions to explore and expand the applications of
the proposed converter.

5) A semiconductor-based galvanic isolation solution is proposed for isolated power
converters. The basic idea of this solution is to deliver the DM load power via active
semiconductor switches during their ON states, while sustaining the CM voltage and
blocking the CM leakage current with those semiconductor switches during their OFF
states. To implement this idea, circuit topologies are derived from SC circuits, aiming to
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On the other hand, the semiconductor-based galvanic isolation solution needs to provide high power density and high efficiency. As the switching frequency is limited by the TC requirement, conduction loss of switches and capacitors is a major part of the power loss, so low switch on-resistance and low capacitor ESR are required. The low switch on-resistance is another important reason why we need WBG power devices for this solution. Low switching frequency is not preferred as it significantly increase the size of capacitors, although it helps reducing the TC. As the switching frequency increases, effective TC reduction is needed, and different approaches to reduce the TC are discussed in section 5.5. Auxiliary current-source circuits are designed and distributed to each switch, to compensate the $C_{\text{oss}}$ charging currents.

Other challenges for the proposed solution include a large voltage transfer ratio, voltage regulation function, and applications into isolated ac/dc and dc/ac power converters. To address these challenges, extended topologies are derived, as shown in section 5.6.
A preliminary prototype of the SC isolation cell is designed to verify the DM power delivery performance and the TC performance. The test results are presented in section 5.8. It is shown that TC results meet the IEC60950, and the designed auxiliary current-source circuits can effectively reduce the TC.

6.2. Recommendations for Future Work

The future work can be continued following the two directions presented in this dissertation. On one hand, further study is required to explore the closed-loop control of the proposed isolated QSC converters. For the isolated QSC PWM converter, phase-shift control is a good control method candidate which needs to be studied and evaluated. With phase-shift control, the converter switching frequency is fixed, which is beneficial for EMI filter design. The active power is then regulated by the duty ratio and phase shift angle. In this case, the converter performs different ZVS operation range and voltage stress on active and passive components, which all require further study. For the isolated QSC resonant converter, closed-loop control also needs be explored. Control method candidates include the phase shift control, the on-off control employed by Φ2 VHF converter, and the switching frequency control employed by LLC resonant converter. For each control method, the relationship between the control variables and the converter output needs to be analyzed, and the control-to-output transfer functions must be modeled. The challenges to derive the transfer functions are the non-linearity of the equivalent circuit, as the switched capacitors change their connections from connecting in series to connecting in
parallel, or vice versa. The state-trajectory analysis of LLC resonant converter should be referred in studying the voltage and current transitions of the QSC resonant current.

On the other hand, further study is required for the proposed semiconductor-based galvanic isolation. On the component level, to pursue high CM isolation performance, high power density, and high efficiency, bidirectional WBG power devices with high voltage rating, low $C_{oss}$, and low on-resistance need to be developed. The vertical GaN HMETs are expected to provide such required characteristics, and next-generation ultra-wide bandgap devices are also good candidates on the horizon. On the circuit level, distributed current-source circuits are designed to compensate the switch $C_{oss}$ charging current so as to limit the TC. The control of these current-source circuits need to be studied and coordinated. It is expected that at high switching frequency, with elegantly controlled distributed current-source circuits, the converter can perform high CM impedance and low TC that meet the safety standards. On the system integration level, package techniques should be applied to build power modules which integrate WBG power devices and capacitors, to achieve lower parasitics, smaller footprint, and better thermal performance. With the research progress on all these different levels, semiconductor-based galvanic isolation will be demonstrated successfully.
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