Large Signal Modelling of AlGaN/GaN HEMT for Linearity Prediction

THESIS

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Abstract

This objective of this work is to develop predictive device modelling methodology to relate the physical behavior of AlGaN/GaN HEMTs with RF power amplifier parameters. The large signal performance of two 0.25µm×100µm GaN transistors—a standard HEMT with a recessed gate and a graded channel HEMT were analyzed at a frequency of 20 Ghz using the model. The devices are simulated in Silvaco Atlas TCAD with a velocity saturation model to obtain the high frequency two port network parameters. From these, the small signal circuit components of the device were extracted as a function of gate voltage, drain voltage and frequency. Harmonic balance simulations were performed in ADS to obtain the output power and linearity characteristics. The choice of bias points to maximize linearity from the device was explored.
Dedication

Dedicated to my parents for their unwavering love and support
Acknowledgments

There are many people to whom I am indebted for making my Masters in The Ohio State University an enriching experience.

First and foremost, I thank Prof. Siddharth Rajan, my advisor, through whose association over the last two years, the foundation of my understanding and interest in semiconductor devices has been laid. Prof. Rajan’s courses were some of the most challenging ones and motivated me to try and understand devices from an intuitive physical perspective rather than a mathematical one. I am grateful to him for having conceived the idea behind my work, his constant support, enthusiastic outlook on research and valuable guidance and suggestions regarding my projects. I thank Prof. Wu Lu for his time and suggestions during my thesis defense.

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# Table of Contents

Abstract .......................................................................................................................... ii
Dedication ....................................................................................................................... iii
Acknowledgments .......................................................................................................... iv
Fields of Study ............................................................................................................... v
Table of Contents ......................................................................................................... vi
List of Tables ................................................................................................................. viii
List of Figures ............................................................................................................... ix

Chapter 1: Introduction ................................................................................................. 1
  1.1 AlGaN/GaN HEMT device .................................................................................... 2
  1.2 Motivation ............................................................................................................ 6
  1.3 Organization of the thesis .................................................................................... 6

Chapter 2: AlGaN/GaN HEMT Small Signal Modelling ............................................. 8
  2.1 Silvaco Device Simulations .................................................................................. 9
    2.1.1 Velocity Saturation Model .......................................................................... 12
    2.1.2 Silvaco Device simulation results ................................................................. 14
  2.2 Small Signal Modelling ....................................................................................... 16
    2.2.1 Small Signal Parameter Extraction Methodology ........................................ 19
    2.2.2 Small Signal Extracted Parameters ............................................................ 23

Chapter 3: Large Signal Modelling of HEMT ............................................................ 28
  3.1 Nonlinearity Sources ......................................................................................... 28
    3.1.1 Nonlinear Transconductance ($g_m$) ........................................................... 29
    3.1.2 Nonlinear Capacitance ($C_{gs}$, $C_{gd}$ and $C_{ds}$) ........................................ 29
3.1.3 Nonlinear $g_{ds}$ .................................................................................................................. 30
3.2 Existing Large Signal Models ................................................................................................. 30
  3.2.1 Curtice Model ....................................................................................................................... 31
  3.2.2 Angelov Model ..................................................................................................................... 32
3.3 Large Signal Model used in this work .................................................................................... 32
  3.3.1 Nonlinear Charge Modelling .............................................................................................. 34
  3.3.2 Large Signal Modelling in ADS ......................................................................................... 34
3.4 Linearity Characteristics ......................................................................................................... 37
  3.4.1 $P_1$ dB gain compression point .......................................................................................... 38
  3.4.2 IIP3 ....................................................................................................................................... 39
  3.4.3 C/I ratio ............................................................................................................................... 39
  3.4.4 Adjacent Channel Power Ratio (ACPR) ........................................................................... 40
  3.4.5 Power Added Efficiency (PAE) .......................................................................................... 40
3.5 Harmonic balance simulations in Agilent ADS ...................................................................... 40
  3.5.1 Harmonic balance simulation convergence requirements ................................................. 42
  3.5.2 Harmonic balance simulations bias points ....................................................................... 43
3.6 Graded Channel HEMTs ....................................................................................................... 47
  3.6.1 Graded Channel HEMT Silvaco and Small Signal Results .............................................. 50
3.7 Results of harmonic balance simulations ............................................................................. 55
Chapter 4: Conclusion and Future Work ..................................................................................... 61
References ..................................................................................................................................... 64
Appendix A – Silvaco code for AlGaN/GaN HEMT .................................................................... 67
List of Tables

Table 1 : Models Used In Silvaco Code ................................................................. 12
Table 2: Standard HEMT Extrinsic Resistances...................................................... 23
Table 3 : Matching Network For HBS.................................................................... 41
Table 4: Graded HEMT Extrinsic Small Signal Parameters ..................................... 55
List of Figures

FIGURE 1: ALGAN/GAN HEMT ENERGY DIAGRAM ................................................................. 2
FIGURE 2: ALGAN/GAN HEMT CHARGE DISTRIBUTION ...................................................... 2
FIGURE 3: HEMT SMALL SIGNAL MODEL .............................................................................. 3
FIGURE 4: RECESSED ALGAN/GAN HEMT DEVICE STRUCTURE ........................................ 10
FIGURE 5: STANDARD HEMT CHARGE DENSITY ................................................................. 10
FIGURE 6: STANDARD HEMT BAND ENERGY DIAGRAM ..................................................... 11
FIGURE 7: I_{DS} VS V_{DS} FROM SILVACO FOR STANDARD HEMT ...................................... 14
FIGURE 8: I_{DS} AND G_{M} VS V_{GS} FOR STANDARD HEMT .................................................. 14
FIGURE 9: F_{T} OF STANDARD HEMT AT HIGH BIAS ............................................................ 15
FIGURE 10: F_{T} OF STANDARD HEMT AT LOW BIAS .......................................................... 15
FIGURE 11: MAXIMUM AVAILABLE GAIN OF STANDARD HEMT ....................................... 15
FIGURE 12: TWO PORT NETWORK ....................................................................................... 16
FIGURE 13: DAMBRINE’S SMALL SIGNAL MODEL OF A FET .............................................. 17
FIGURE 14: 22 ELEMENT DISTRIBUTED SMALL SIGNAL MODEL ...................................... 18
FIGURE 15: SMALL SIGNAL CIRCUIT EQUIVALENT USED IN THIS WORK ............................ 19
FIGURE 16: LINEAR FITTING TO DETERMINE C_{GS} ........................................................... 21
FIGURE 17: SMALL SIGNAL CIRCUIT EQUIVALENT OF UNBIASED FET ............................ 23
FIGURE 18: STANDARD HEMT C_{GS}(V_{GS},V_{DS}) ............................................................... 24
FIGURE 19: STANDARD HEMT C_{DS}(V_{GS},V_{DS}) ............................................................... 24
FIGURE 20: STANDARD HEMT C_{GD}(V_{GS},V_{DS}) ............................................................... 24
FIGURE 21: STANDARD HEMT $G_m(V_{GS}, V_{DS})$ ................................................................. 24
FIGURE 22: STANDARD HEMT $R_t(V_{GS}, V_{DS})$ ................................................................. 24
FIGURE 23: STANDARD HEMT $R_{GD}(V_{GS}, V_{DS})$ ............................................................... 25

FIGURE 24 : STANDARD HEMT $G_{DS}(V_{GS}, V_{DS})$ ............................................................... 25
FIGURE 25: STANDARD HEMT $T(V_{GS}, V_{DS})$ ................................................................. 25
FIGURE 26: STANDARD HEMT $I_{DS}(V_{GS}, V_{DS})$ ............................................................... 26
FIGURE 27: CURTICE LARGE SIGNAL MODEL .................................................................. 31
FIGURE 28: LARGE SIGNAL CIRCUIT EQUIVALENT OF THE HEMT ................................. 33
FIGURE 29: DEVICE MODELLED USING SDD IN ADS ..................................................... 35
FIGURE 30: LARGE SIGNAL CIRCUIT EQUIVALENT IMPLEMENTED USING SDD AND DAC ... 37
FIGURE 31 : P1 DB COMPRESSION POINT ........................................................................ 38
FIGURE 32 : INPUT THIRD ORDER INTERCEPT POINT ( IIP3) ................................................ 39
FIGURE 33 : ADS HARMONIC BALANCE SIMULATION SETUP ......................................... 42
FIGURE 34: LINEAR POWER AMPLIFIERS’ CONDUCTION ANGLES ................................. 44
FIGURE 35: LOADLINE OF STANDARD HEMT CIRCUIT EQUIVALENT .......................... 45
FIGURE 36: GM3 OF STANDARD HEMT ........................................................................... 47
FIGURE 37: GRADED CHANNEL HEMT DEVICE STRUCTURE ......................................... 48
FIGURE 38: GRADED HEMT ENERGY DIAGRAM .............................................................. 49
FIGURE 39: GRADED HEMT CHARGE DENSITY ................................................................. 49
FIGURE 40: GRADED HEMT $I_{DS}$ VS $V_{DS}$ ...................................................................... 51
FIGURE 41: GRADED HEMT $I_{DS}$ AND $G_m$ VS $V_{GS}$ ..................................................... 51
FIGURE 42: GRADED HEMT UNITY GAIN FREQUENCY ..................................................... 52
FIGURE 43: GRADED HEMT MAX AVAILABLE GAIN ......................................................... 52
FIGURE 44 : GRADED HEMT $C_{GS}(V_{GS}, V_{DS})$ ............................................................... 52
FIGURE 45: GRADED HEMT $C_{GD}(V_{GS}, V_{DS})$ ............................................................... 52
FIGURE 46: GRADED HEMT $G_M(V_{GS}, V_{DS})$ .................................................................53
FIGURE 47: GRADED HEMT $C_{DS}(V_{GS}, V_{DS})$ .................................................................53
FIGURE 48 : GRADED HEMT $R_I(V_{GS}, V_{DS})$ .................................................................53
FIGURE 49 : GRADED HEMT $R_{GD}(V_{GS}, V_{DS})$ .................................................................53
FIGURE 50: GRADED HEMT $G_{DS}(V_{GS}, V_{DS})$ .................................................................53
FIGURE 51: GRADED HEMT $T(V_{GS}, V_{DS})$ .................................................................53
FIGURE 52: GRADED HEMT $I_{DS}(V_{GS}, V_{DS})$ .................................................................54
FIGURE 53 : STANDARD HEMT O/P VS I/P POWER ............................................................56
FIGURE 54 : STANDARD HEMT GAIN VS INPUT POWER ..................................................56
FIGURE 55: STANDARD HEMT PAE ....................................................................................57
FIGURE 56 : STANDARD HEMT IIP3 ...................................................................................57
FIGURE 57 : STANDARD HEMT C/I RATIO ...........................................................................57
FIGURE 58 : GRADED HEMT O/P VS I/P POWER .............................................................58
FIGURE 59: GRADED HEMT GAIN VS I/P POWER ..........................................................58
FIGURE 60: PAE OF GRADED HEMT ..................................................................................59
FIGURE 61: GRADED HEMT IIP3 .........................................................................................59
FIGURE 62: GRADED HEMT C/I RATIO ...............................................................................59
FIGURE 63: IM3 OF STANDARD VS GRADED HEMT ......................................................60
Chapter 1: Introduction

With the rapid upsurge in the wireless communication market, research in microwave transistors is becoming increasingly important. Their performance requirements are also becoming more and more demanding in terms of wider bandwidth and higher efficiency. RF power amplifiers (PA) are considered to be one of the most challenging areas of design in the transmitter-receiver chain due to their high output power and linearity requirements. PA linearity can be improved either by adding external circuits, or by simply improving the design. Since the first technique involves several drawbacks like cost, size and effective bandwidth, there is an increasing interest for the direct optimization of the PA linearity in terms of the active device. [1].

GaN based RF power devices and amplifiers have made significant progresses over the last two decades. GaN and other III nitrides, in general have several characteristics such as high breakdown due to wide bandgap, high saturation velocity, high thermal conductivity and large sheet charge carrier density due to polarization engineering, which make them very good candidates for RF applications [2]. The high electron mobility provides low on-resistance that permits operation at high frequencies. Their potential capability in RF has been demonstrated by their high Johnson Figure of Merit and the Baliga Figure of Merit [3] as compared to silicon. The recent advances in epitaxial growth technology has led to the constant improvement of GaN based devices using SiN\textsubscript{x} passivation[4], field plate
technology[5], back-barrier structures to improve charge confinement[6] and growth on silicon carbide substrate that has excellent thermal properties.

1.1 AlGaN/GaN HEMT device

The high electron mobility transistor (HEMT) is a heterostructure field effect transistor. A wide bandgap material lies on a narrow bandgap material, which results in a conduction band offset as shown in Fig 1[7]. This results in high carrier concentration in a narrow region called the quantum well in the source drain direction. The wurtzite crystal structure of GaN produces a strong polarization field which is usually screened by counter ions in atmosphere. However, when terminated with another III-V material such as AlGaN to form a heterojunction, the net polarization acts as a further instigator to the conduction band offset, producing a very high sheet charge density of $2-4 \times 10^{13}$ in the form of a 2 dimensional gas (2DEG), shown in Fig 2[7]. Hence, the 2DEG is formed even without any intentional doping. It has been determined that the considerable number of electrons in the 2DEG are transferred from surface states to the heterojunction interface[8].

![Figure 1: AlGaN/GaN HEMT Energy Diagram](image1)

![Figure 2: AlGaN/GaN HEMT Charge distribution](image2)
As the requirement for higher bandwidth increases, the scaling of device dimensions is necessary in the form of making the gate length of the devices smaller. This may, however, lead to short channel effects which can significantly degrade the high frequency gain by increasing the output conductance, $g_{ds}$. Some of the important short channel effects that degraded the performance are dynamic parasitic resistances[9], underperforming saturation electron velocity [7] and transconductance collapse. All of these effects are discussed in greater detail in further chapters of this thesis.

Fig. 3[10] shows the 3-D small signal structure of the AlGaN/GaN HEMT. A brief overview of the most important small signal components is given as this lays the foundation for much of the discussions in the rest of the thesis.

![Figure 3: HEMT Small Signal Model](image-url)
Transconductance ($g_m$)

The intrinsic gain mechanism of the HEMT is provided by the transconductance. It is a measure of the incremental change in the output current $I_{ds}$ for a given change in the input voltage $V_{gs}$. The intrinsic $g_m$ can be expressed as shown in Eq.(1.1)

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}}$$

$g_m$ can also be expressed as ($v_{sat}$*$C_{gs}$/$L_g$). This is an important relationship showing that it strongly depends on the electron saturation velocity. High and flat transconductance is preferred for power amplifier design since that gives higher gain and linearity.

Extrinsic Resistances $R_s$, $R_d$ and $R_g$

These are included to account for the contact resistance of the ohmic contacts, the dynamic access resistance and any bulk resistance leading up to the active channel. $R_g$ results from the metallization resistance of the gate Schottky contact. These resistances are generally preferred to be lower as they can cause noise, power dissipation and non-linearity.

Capacitances $C_{gs}$, $C_{gd}$ and $C_{ds}$

The capacitances $C_{gs}$ and $C_{gd}$ reflect the change in the depletion charge with changes in $V_{gs}$ and $V_{gd}$ respectively. $C_{gs}$ is the larger quantity and usually about 10 times the size of $C_{gd}$ and $C_{ds}$. $C_{ds}$ accounts for the geometric capacitance effects between the source and drain electrodes. These capacitances usually determine the unity gain frequency of the device. They grow smaller as the device becomes smaller and have an inverse relationship with the maximum frequency of operation.
Output Conductance ($g_{ds}$)

The output conductance is a measure of the incremental change in output current $I_{ds}$ with the output voltage $V_{ds}$.

$$g_{ds} = \frac{\partial I_{ds}}{\partial V_{ds}}$$

(1.3)

As gate length is reduced, output conductance tends to increase in HEMTs, which is one of the predominant short channel effects. $G_{ds}$ is preferred to be small as high output resistance is required for a high gain and also to avoid reduction of unity gain frequency based on Eq. (1.2).

**Intrinsic transconductance Delay ($\tau$)**

The drain current, $I_{ds}$ does not respond to changes in the gate voltage instantaneously. The delay inherent to this process is described by the transconductance delay. It represents the time it takes for the charge to redistribute itself after a fluctuation of the gate voltage. It is inversely related to the unity gain frequency.

**Charging Resistances $R_i$ and $R_{gd}$**

These are charging resistances for the $C_{gs}$ and $C_{gd}$ capacitances. They scale with the gate-source length and the gate-drain length respectively and the lower they are, the faster the device becomes, as it reduces the charging time delay of the capacitors.
1.2 Motivation

Modelling of devices is essential to create in-built models which can be used directly as modules while incorporating them as part of an electronic circuit or a system. There has been much work done in the modelling of HEMTs in the last decade, where usually the experimental data is empirically modelled into equations that describe the behavior of the device. These in-built models can be simulated to provide information about the device’s performance in terms of gain, linearity and output power which are some of the most fundamental performance metrics. New HEMT devices from different materials, and using innovative epitaxial structures are created everyday, exceeding the performance of their predecessors. While the built-in models may work well for standard types of device structures, models that can be re-used for any kind of HEMT with distinctive, unusual behavior is the order of the day. Predictive modelling of linearity is an avid area of research for RF power amplifier applications, as it can save much time in the design and manufacturing process. It is a challenging task, especially at the Ghz-Thz range of frequencies at which devices are operated these days, as several high frequency and parasitic effects come to play. The motivation behind this work is to take a step in that direction, using the AlGaN/GaN HEMTs as prototypes.

1.3 Organization of the thesis

Chapter 1 gives an introduction about GaN based microwave devices, their device physics and applicability as RF power amplifiers and the motivation behind undertaking this modelling work.
Chapter 2 discusses the small signal parameter extraction approach for an AlGaN/GaN HEMT starting from modelling the device using Silvaco Atlas TCAD and using the TCAD results to obtain the small signal parameters over a wide range of bias points and frequencies. It discusses the results obtained from Silvaco and the small signal parameter extraction.

Chapter 3 details the large signal modelling work done in this thesis using Agilent ADS and the subsequent harmonic balance simulations. It explains about the motivation behind tailoring the transconductance of the device by using graded channel AlGaN/GaN HEMTs for higher linearity. It goes on to discuss the TCAD and small signal circuit results of the graded channel device and then compares the harmonic balance simulation results of the two devices in terms of output power density and linearity.

Chapter 4 is the conclusion of the thesis. It summarizes the work done and discusses the salient aspects and limitations of this project and suggests ways to overcome these limitations.
Chapter 2: AlGaN/GaN HEMT Small Signal Modelling

The primary goal of device modeling is to obtain the functional relationship between the basic quantities that define the behavior of that device. In an empirical modeling approach, the device is treated as a DUT (device under test) and its behavior to a stimulated signal is observed, measured and extrapolated. In a physical modeling approach, the performance of the device can be predicted from physical data describing the device. This data consists of material characteristics, carrier transport properties and the device geometry and epitaxy. The important aspect about this approach is that it describes the device operation in terms of the physics of the device. Its response can be calculated by solving a set of coupled nonlinear differential equations describing the charge transport and the electrical field of the device.

This work uses a bottom up modelling approach [11], where physical modelling is used to obtain the device level characteristics, which are plugged into a small signal circuit model. Circuit level modelling provides the advantage of understanding system requirements easier and gives more flexibility in manipulating the device parameters without having to go into the physics of it at every step. The modelling in this thesis has been performed based on data obtained from simulations rather than measurements. Hence, it assumes
certain idealities in the device behavior and is mainly focused on analyzing the device performance at more of an intrinsic level.

The following procedure has been used in this work to model the HEMT:

i. Silvaco ATLAS TCAD has been used to simulate the current-voltage characteristics and the small signal $S$ parameters by sweeping gate bias ($V_{gs}$), drain bias($V_{ds}$) and frequency.

ii. The bias dependent $S$ parameters have been used to obtain the intrinsic and extrinsic small signal parameters of the device as a function of $V_{gs}$ and $V_{ds}$ and frequency.

iii. A large signal circuit equivalent has been formulated for the device in which the device parameters have been fed into, using a look-up table model in Agilent ADS.

iv. Single tone and two tone simulations have been performed on the large signal model equivalent to extract the output power, gain and linearity characteristics of the device at the required operating frequency.

2.1 Silvaco Device Simulations

Device simulations were carried out using Silvaco Atlas TCAD under DC and RF operating conditions[12]. Fig. 4 shows the structure of the recessed gate Al$_{0.25}$Ga$_{0.75}$N/GaN HEMT that was simulated. Figs 5-6 show the device’s equilibrium charge distribution and energy band structure. The abrupt conduction band offset due to the hererostructure and the highly concentrated 2-D charge density can be seen clearly. It is a short channel highly scaled device with a gate length of 0.25 µm, a gate-source length of 0.5 µm and gate-drain length
of 2 µm. The gate-source length is kept smaller in order to minimize the source access resistance. The source access resistance can increase with increase in drain current due to the quasi-saturation of the electron velocity in the source region of the channel at high electric fields, leading to nonlinear transconductance [13].

Figure 4: Recessed AlGaN/GaN HEMT device structure

Figure 5: Standard HEMT charge density
The device has a 30 nm AlGaN barrier, and the gate has been recessed upto 20 nm, making the effective gate-channel distance 10 nm. Recessing alleviates gate leakage since the sheet charge density at the channel is lower than that of a standard case [14], which increases the threshold voltage effectively. In this case, it also helps the structure to maintain a sizeable aspect ratio, (Lg/d = 25), which is usually required for AlGaN/GaN HEMTs to combat with short channel effects[7]. A 50 nm GaN buffer follows the AlGaN barrier which is followed by a 1um GaN substrate. The contact resistance of the three electrodes was maintained at 0.2 Ω.mm. The device is passivated by silicon nitride.

The device was simulated across a gate-source bias range of 4 V starting from its pinch-off and over a drain-source bias range of 0 to 25 V. For each of those bias points, the frequency was swept from 0 to 70 Ghz, so as to obtain the unity gain frequency data as well as the S parameters as a function of the gate, drain voltages and frequency. The mesh was laid out accurately, to achieve convergence over this large bias range. Self-heating
effects, interface traps and gate leakage models were not incorporated in the code. Surface traps can cause DC to RF dispersion effects, which can only be analyzed through Pulsed I-V simulations. [15]. However, since these effects were not taken into consideration, only regular DC and RF simulations were performed. The Newton and Gummel methods were used as solvers. Table 1 shows the models that were incorporated in the simulation code for this device.

Table 1: Models used in Silvaco code

<table>
<thead>
<tr>
<th>Model</th>
<th>Purpose</th>
</tr>
</thead>
<tbody>
<tr>
<td>srh</td>
<td>The Shockley-Reed-Hall recombination model capturing the phonon transitions occurring with the forbidden bandgap of the semiconductor in the presence of a trap or a defect.</td>
</tr>
<tr>
<td>calc.strain</td>
<td>This model calculates the strain from the lattice mismatch and the piezoelectric polarization and applies it to the region.</td>
</tr>
<tr>
<td>Polar.scale</td>
<td>Specifies a constant scale factor multiplied by the calculated spontaneous and piezoelectric charges.</td>
</tr>
<tr>
<td>spontaneous</td>
<td>Includes the radiative recombination rates into the drift diffusion process.</td>
</tr>
</tbody>
</table>

2.1.1 Velocity Saturation Model

In many theoretical calculations [16], the peak electron velocity and the saturation electron velocity of the GaN channel were found to be around $2.5 - 3 \times 10^7$ cm/s and $1 - 1.9 \times 10^7$...
cm/s, respectively. However, from the total time delay analysis in recent ultra-scaled GaN HEMT results [17], the average electron velocity of the devices was found to be in the range from $1.1 \times 10^7$ to $1.5 \times 10^7$ cm/s. The parasitic charging delay was also found to be only less than $5 \sim 10\%$ of the total time delay. The carrier transport model suggested by Jacob Khurgin [18,19] based on the strong interaction between optical-phonon and electron carriers in 2DEG of GaN HEMT has bridged the discrepancy between predicted and measured velocity. The authors of [20] have implemented this model in 2-dimensional TCAD simulations and states that there was close agreement between simulations and experiments.

The velocity saturation model assigns the LO phonons related electron backscattering as the reason for the saturation of electron velocity. It also characterizes the electron distribution in the band with a shifted Fermi-Dirac distribution. The calculated solutions show that the saturation velocity is a strong function of carrier concentration as shown in Eq 2.1.

$$v_{sat}(n_s) = \frac{10^7}{0.38 + \left( \frac{n_s}{n_{s,0}} \right)^{0.45}}$$  \hspace{1cm} (2.1)

This optical Phonon Limited field and charge density dependent mobility model have been incorporated by [7] in the Silvaco TCAD code using a C-Interpreter file that is called as a function from the main source code. This velocity saturation model has been incorporated in all the Silvaco modelling done in this work as it models the I-V behavior and the collapse of $g_m$ due to increase in carrier concentration accurately.
2.1.2 Silvaco Device simulation results

Figs 7-8 show the $I_{ds}$-$V_{gs}$ and $I_{ds}$-$V_{ds}$ characteristics of the simulated device. The recessed structure allows a higher than typical threshold voltage of -2 V, and also leads to the sharp increase in $g_m$. Recessed structures have a higher $C_{gs}$, due to a smaller gate to channel distance, which leads to a peak $g_m$ of 600 mS/mm. A maximum drain current of 1.5 A/mm is obtained at a gate voltage of 2 V. Fig 8 also demonstrates the $g_m$ collapse after -1.5 V, the reason for which discussed in the previous section.

![Figure 7: $I_{ds}$ vs $V_{ds}$ from Silvaco for standard HEMT](image1)

![Figure 8: $I_{ds}$ and $g_m$ vs $V_{gs}$ for standard HEMT](image2)

Figs 9-10 show the current gain as a function of the frequency and indicate the unity gain frequency (where the current gain is 0 dB) for the device at different voltage biases. As the drain current increases, the unity gain frequency falls, which has been attributed to the increase in the dynamic source access resistance [13]. In this case, it can also be explained by the $g_m$ collapse at high drain current density.
Fig. 11 shows the maximum available gain of the device as a function of the frequency. Any amplifier derived using this device cannot have a gain higher than this intrinsic gain at a given frequency. This is used later to cross-check if the simulated gain characteristics of the device’s large signal model are in agreement with the gain in this plot.
2.2 Small Signal Modelling

Small signal models help analog and RF Engineers to examine the performance characteristics such as gain, nonlinearity and output power of devices at high frequencies. They provide a vital link between measured two port network parameters \((S, Z, Y)\) and the electrical processes occurring within the device. The \(S\) parameters or scattering parameters describe the electrical behavior of linear multi-port electrical networks when undergoing various steady state stimuli by electrical signals for various frequencies. Fig 12 shows how the \(S\) parameters are defined for a two port network.

![Two port Network](image)

In Eq. (2.2), \(a_1\), \(a_2\), \(b_1\) and \(b_2\) represent the voltages induced by the power transmitted and reflected from each port of the network. These give us a great amount of information about the intrinsic quantities of the device such as the capacitances, conductances and time delay.
They can be easily transformed to admittance or impedance parameters through which the voltage quantities can be converted to currents.

The equivalent circuit elements in the small signal model provide a lumped element approximation to some degree of the device physics. They can be scaled with gate width, which enables a designer to predict the performance of differently sized devices. An efficient small signal model should take into account the accuracy of the equivalent circuit model that can reflect the reliability of the model element extraction. Different small signal modelling methodologies and topologies have developed over the past two decades to help examine the performance of MESFETs and HEMTs. Fig 13 shows Dambrine’s small signal model of the FET [21] and Fig. 14 shows the most recent 22 element distributed model[22]. It indicates the evolution of the small signal model of the FET over time. With the progress of technology, more parasitic components have been taken into consideration to reflect the physics of the device over a wider bias and frequency range.

![Figure 13: Dambrine’s small signal model of a FET](image-url)
Based on Fig 13, Dambrine’s small signal circuit elements can be categorized into intrinsic and extrinsic elements:

(i) The intrinsic elements $g_m$, $g_d$, $C_{gs}$, $C_{gd}$, $C_{ds}$, $R_i$ and $\tau$, which are functions of the drain and gate bias.

(ii) The extrinsic elements $R_g$, $R_s$, $R_d$, $C_{pgi}$, $C_{pdi}$, $C_{gdi}$, $L_g$, $L_s$, and $L_d$ which are independent of the biasing conditions.

The 22 element distributed model topology takes into consideration the effect of $R_{gd}$ for the non-quasi static modelling of $C_{gd}$. Additionally, $C_{pgi}$, $C_{pdi}$, and $C_{gdi}$ account for the inter-electrode and crossover capacitances (due from air-bridge source connections) between gate, source, and drain. $C_{pga}$, $C_{pda}$, and $C_{gda}$ account for parasitic elements due to the pad connections, measurement equipment, probes, and probe tip-to-device contact transitions. [22]
In this work, since Silvaco does not account for parasitics of any form in its simulations and since gate leakage models have not been incorporated, the extrinsic parameters \( L_g, L_s, L_d, C_{pd}, C_{pg} \), all the inter-electrode capacitances and the gate current conductances have been ignored. Fig.15 shows the small signal model used in this work. It consists of the 8 intrinsic elements and the three extrinsic resistances each of which will be the sum of the respective contact resistance and the access resistance. The intrinsic elements as treated as bias-dependent, while the extrinsic resistances are treated constant with the bias.

![Small Signal circuit equivalent used in this work](image)

**2.2.1 Small Signal Parameter Extraction Methodology**

Based on Dambrine’s extraction methodology, after neglecting parasitics the small signal parameters could be extracted by the following procedure.
a. Transformation of extrinsic simulated $S$ parameters into $Z$ parameters and subtraction of $R_g, R_s$ and $R_d$ that are in series. This is the de-embedding of the extrinsic parameters from the overall circuit. The three extrinsic resistances are determined from the $Z$ parameters extracted from zero drain bias condition.

b. Transformation of $Z$ to $Y$ parameters in order to obtain the required intrinsic element matrix.

If the intrinsic device were to be treated as a two port network we can use the admittance parameters ($Y$) to characterize its electrical properties as follows:

\[
Y_{11} = R_i C_{gs}^2 \omega^2 + j\omega(C_{gs} + C_{gd}) \quad (2.3)
\]
\[
Y_{12} = -j\omega C_{gd} \quad (2.4)
\]
\[
Y_{21} = g_m - j\omega(C_{gd} + g_m(R_i C_{gs} + \tau)) \quad (2.5)
\]
\[
Y_{22} = g_{ds} + j\omega(C_{ds} + C_{gd}) \quad (2.6)
\]

However, Dambrine’s methodology makes an assumption while deriving Eq (2.3-2.6), that $\omega^2 C_{gs}^2 R_i^2$ is less than 0.01, which is valid only for frequencies smaller than 5 Ghz. For frequencies greater than that, using these equations directly will lead to unreliable results. To overcome this issue, the authors of [22] have come up with a method using linear regression that will account for the frequency dependent effect of the intrinsic elements at high frequencies. Using this technique, the intrinsic $Y$-parameters are formulated in a way where the optimal intrinsic element value can be extracted using simple linear data fitting.
The admittance of the intrinsic gate-source branch $Y_{gs}$ is given by

$$Y_{gs} = Y_{i,11} + Y_{i,12} = \frac{j\omega C_{gs}}{1 + j\omega R_i C_{gs}}$$  \hspace{1cm} (2.7)

A variable D can be defined as shown in Eq. 2.8 and find the instantaneous slope of the D vs $\omega$ curve at the required frequency, which will be the $C_{gs}$ at that frequency. Fig. 16 shows the plot of D vs $\omega$.

$$D = \frac{|Y_{gs}|^2}{\text{Im}[Y_{gs}]} = \omega C_{gs}$$  \hspace{1cm} (2.8)

![Figure 16: Linear fitting to determine $C_{gs}$](image)

Now that $C_{gs}$ is already known, $R_i$ can be extracted from a plot of A vs $\omega C_{gs}$ as seen in Eq. (2.8)

$$A = \frac{Y_{gs}}{\text{Im}[Y_{gs}]} = \omega R_i C_{gs} - j$$  \hspace{1cm} (2.9)
Similarly, the remaining 6 intrinsic parameters can be determined from the other \( Y \) parameters.

\[
Y_{gd} = -Y_{i,12} = \frac{j\omega C_{gd}}{1 + j\omega R_{gd} C_{gd}} \quad (2.10)
\]

\[
Y_{gm} = Y_{i,21} - Y_{i,12} = \frac{G_m e^{-j\omega \tau}}{1 + j\omega C_{gs}} \quad (2.11)
\]

\[
D = \left| \frac{Y_{gs}}{Y_{gm}} \right|^2 = \left( \frac{C_{gs}}{G_m} \right)^2 \omega^2 \quad (2.12)
\]

\[
D = \left( j\omega C_{gs} \right) \frac{Y_{gm}}{Y_{gs}} = G_m e^{-j\omega \tau} \quad (2.13)
\]

\[
Y_{ds} = Y_{i,22} + Y_{i,12} = G_{ds} + j\omega C_{ds} \quad (2.14)
\]

From Eq. (2.10), we can extract \( C_{gd} \) and \( R_{gd} \) similar to the way \( C_{gs} \) and \( R_i \) were extracted from Eq. (2.7) and (2.8). Eq. (2.12) gives \( g_m \) as the square of the slope of \( D \) vs \( \omega \). Eq. (2.13) gives \( \tau \) from a plot of the phase of \( D \) vs \( \omega \). And finally, Eq. (2.14) yields \( g_{ds} \) and \( C_{ds} \) from a plot of \( Y_{ds} \) vs \( \omega \).

The extrinsic parameters of the circuit – \( R_g \), \( R_s \) and \( R_d \) were extracted from \( Z \) parameters using Eq. 2.15, simulated under the bias conditions of \( V_{gs} = 0 \)V and \( V_{ds} = 0 \)V which is termed as the unbiased FET condition[23]. It will give precise equilibrium values, since the equivalent voltage controlled current source and the intrinsic part is disabled in this condition as shown in Fig. 17. Similar to the intrinsic parameters, these are also obtained by linear fitting to take the frequency dependent effect into consideration. Since, in reality \( R_g \) cannot be measured for a Schottky contact by any experimental methods, this extracted value is merely the gate contact resistance using which the Silvaco model was simulated.
Figure 17: Small signal circuit equivalent of unbiased FET

\[ \omega^2 \text{Re}[Z11] = \omega^2 [R_g + R_s] \]

\[ \omega^2 \text{Re}[Z12] = \omega^2 [R_s] \]  \hspace{1cm} (2.15)

\[ \omega^2 \text{Re}[Z22] = \omega^2 [R_d + R_s] \]

2.2.2 Small Signal Extracted Parameters

Table 2 shows the extracted extrinsic bias-independent resistances.

<table>
<thead>
<tr>
<th>Resistance</th>
<th>Value (Ω)</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_s )</td>
<td>5</td>
</tr>
<tr>
<td>( R_g )</td>
<td>4</td>
</tr>
<tr>
<td>( R_d )</td>
<td>23</td>
</tr>
</tbody>
</table>

\( R_d \) is higher than \( R_s \), which is justified by the fact that the drain-gate length of the device is 4 times the gate-source length. Using the small signal extraction technique, the bias dependent small signal parameters for the device were extracted at a chosen operating frequency of 20 Ghz. Figs 18-25 show the extracted intrinsic bias dependent parameters for the device.
$C_{gs}$ appears as a parallel plate capacitance whose plates are formed by the gate metal and 2DEG channel charge. This capacitance is determined by the depletion layer under the gate which extends all the way up to the heterojunction at very low voltages. Therefore, a rapid increase is found as it moves from the pinch-off region.

![Figure 18](image1.png) Standard HEMT $C_{gs}(V_{gs}, V_{ds})$

![Figure 19](image2.png) Standard HEMT $C_{ds}(V_{gs}, V_{ds})$
Figure 20: Standard HEMT \( C_{gd}(V_{gs},V_{ds}) \)

Figure 21: Standard HEMT \( g_{ml}(V_{gs},V_{ds}) \)

Figure 22: Standard HEMT \( R_{d}(V_{gs},V_{ds}) \)

Figure 23: Standard HEMT \( R_{gd}(V_{gs},V_{ds}) \)

Figure 24: Standard HEMT \( g_{ds}(V_{gs},V_{ds}) \)

Figure 25: Standard HEMT \( \tau(V_{gs},V_{ds}) \)
As the gate voltage increases, and current saturation occurs, there is no more change in the depletion region beyond a certain voltage and therefore, the $C_{gs}$ too stays relatively constant after -0.5 V. The lateral electric field established by the drain voltage, accelerates charge carriers in the channel. This results in a decrease of the depletion layer depth and therefore a gradual and small increase of $C_{gs}$ with drain voltage. $C_{gd}$ capacitance is originated in the extension of the depletion region into the gate-drain area. Since this extension of drain depletion region increases with drain voltage, smaller values of $C_{gd}$ too are obtained with increasing drain voltage. Since the depletion region is more near the drain than the source, $C_{gs}$ is almost an order higher than $C_{gd}$ and $C_{ds}$, as observed from the plots. $C_{gd}$ also increases rapidly with increasing gate voltage under low drain voltage conditions. Under these conditions, the depletion region is diminished and is uniformly distributed under the gate. [24].
The $g_m$ behavior is similar to the trend seen in Fig. 8. There is a sharp increase near pinch-off after which there is a collapse as it is related to the channel charge density and electron velocity.

$g_{ds}$ has small values in the saturation region as expected but increases with gate voltage at low drain voltages, due to the sharper rise of current with drain voltage. $R_i$ models the undepleted part of the channel under the gate, through which gate-source capacitance is charged [25]. It is approximately equal to the potential drop in this channel part and the drain current. Hence as predicted, it is high in the low drain current regime. Extension of the depletion region in the gate-drain area, due to increase in the drain-gate voltage, increases the required transit time for the electrons. This leads to $\tau$ rising with increasing drain voltage. The value of $\tau$ also matches the inverse of the unity gain frequency for this device at the respective bias points. The charging resistance $R_{gd}$ simulates the symmetrical distribution of the depletion region under the gate near the drain side. As drain current increases, the transit delay under the drain increases as explained before. Since $R_{gd}$ models this delay, it is appropriate that it increases at high gate and drain bias points. The drain current increases steadily from a pinchoff voltage of -2V with gate and drain bias till a point and then saturates at higher gate voltages. Fig. 26 is a 3D representation of the results shown in Fig. 7.
Chapter 3: Large Signal Modelling of HEMT

In addition to small signal modelling, the second goal of this work is to establish a nonlinear large signal model for the AlGaN/GaN HEMT. Device behavior is different in large-signal conditions compared to small signal. The small signal model accounts for the behavior which is linear around an operating point. Hence, linearity is of utmost importance in large signal modelling especially at high output powers. The main tool that has been used for this effort has been Agilent ADS. The basic premise is to formulate the large signal circuit equivalent using the extracted small signal model parameters and obtain information regarding the power output, gain compression, harmonic and intermodulation distortion. The large signal simulation relies on the use of a harmonic balance simulator, where the linear circuit is simulated in the frequency domain and the non-linear circuit is simulated in the time domain[26]. Before describing the large signal model used in this work, the important contributors to the non-linearity of the circuit have been discussed.

3.1 Nonlinearity Sources

Device non-linearity is one of the major sources of nonlinear behavior of microwave circuits. Gain compression and intermodulation products arising from the device’s second and third order non-linearity can cause distortion and affect the signal performance through the communication channel.
3.1.1 Nonlinear Transconductance ($g_m$)

The decreasing transconductance profile with increasing gate bias in standard HEMTs is believed to be one of the major causes of non-linearity in HEMTs.

For any device, the current can be expressed as a polynomial of the gate voltage.

$$I_{out} = I_0 + g_m V_{gs} + g_{m2} V_{gs}^2 + g_{m3} V_{gs}^3 + \ldots \quad (3.1)$$

Where $g_{m2}$ and $g_{m3}$ are the second order and third order differentials of $g_m$.

A nonlinear $g_m$ has significant components of $g_{m2}$ and $g_{m3}$. Since IM3 products are caused by the third order term, $g_{m3}$ plays a key role in determining the third order intermodulation distortion, and a high value can deteriorate the linearity. Additionally, frequency dependent dispersion for $g_m$ can be found at low frequencies due to surface traps and self-heating, which also affects the linearity.[27,28]

3.1.2 Nonlinear Capacitance ($C_{gs}$, $C_{gd}$ and $C_{ds}$)

When a linear signal having no other components except its fundamental frequency is applied to the input of the device, the voltage will generate charges on the gate to source capacitor[29], which is a function of the voltage as shown in Eq. (3.2)

$$Q(V_{gs}) = q_0 + q_1 \cdot V_{gs} + q_2 \cdot V_{gs}^2 + q_3 \cdot V_{gs}^3 + \cdots \quad (3.2)$$

$$C(V) = \frac{\partial Q}{\partial V} = q_1 + 2q_2 V + 3q_3 V^2 + \cdots = c_0 + c_1 V + c_2 V^2 + \cdots \quad (3.3)$$

From Eq. (3.3), it can be seen that the even order component of $C_{gs}(V_{gs})$ creates third order intermodulation distortion. Thus the current generated from this charge will consist of amplified versions of the third order components generated at the input. Since the charge
and the current both are nonlinear functions of $V_{gs}$, second order charge components of $Q(V_{gs})$ from Eq. (3.2) can get upconverted to third order distortion components too.[30]

As drain voltage increases, the depletion region by the drain gradually widens, which makes $C_{gd}$ a strongly nonlinear function of the gate to drain voltage ($V_{gd}$). $C_{gd}$ nonlinearity effects are usually lesser than $C_{gs}$ due to their smaller values, but are pronounced especially at output powers more than 25 dBm due to the high voltage swings at the drain node [31].

### 3.1.3 Nonlinear $g_{ds}$

As seen before, $g_{ds}$ varies with both gate and drain voltage. As the slope of the current with drain voltage in the saturation region is uneven, especially in short channel devices, it can cause non-linearity in ways similar to how $g_m$ causes non-linearity [30,31]. Small values of $g_{ds}$ are preferred as it will maximize gain, however they may not provide the best power match across the bias range. Load pull measurements and simulations are useful to find the optimum output impedance through constant VSWR contours for maximum power delivered, efficiency or linearity.

### 3.2 Existing Large Signal Models

Agilent ADS has in-built models of several widely known large signal circuit topologies, the most important ones being the Curtice Model [32,33] and the Angelov Model [34,35].
3.2.1 Curtice Model

The Curtice method or the CFET Model, which was originally developed for GaAs Field Effect Transistors (FETs), uses a third-order polynomial to model the $I_{ds}$ vs. $V_{gs}$ characteristics above the pinch-off voltage. Fig. 27 shows the CFET large signal model. The nonlinear $C_{gs}$ is modelled as a tangent hyperbolic function.

\[
I_d = (a_0 + a_1(V_{gs} - V_p) + a_2(V_{gs} - V_p)^2 + a_3(V_{gs} - V_p)^3)\tanh(\gamma V_{ds}) \tag{3.4}
\]

\[
C_{gs} = P05 + P01 \times \tanh(P02(V_{gs} + P04)) \tag{3.5}
\]

Figure 27: Curtice Large Signal Model [48]

[31] has shown that the Curtice model predicts the linearity characteristics of devices from 0-40 Ghz reasonably well, however, it ignores the $C_{ds}$ and $G_{ds}$ non-linearities of the device. These have to be separately added using an external equation-based ADS non-linear
element. The Curtice model simulates the effects of self-heating, gate leakage and DC to RF dispersion.

### 3.2.2 Angelov Model

The Angelov Model, developed by I. Angelov, models the drain current, $C_{gs}$ and $C_{gd}$ in a very similar way as the Curtice model. $C_{gs}$, $C_{gd}$ are continuous functions with voltages with well-defined derivatives in order to converge with harmonic balance simulations. The drain current includes a tanh dependency on the $V_{gs}$ polynomial as well, which gives a better fit at lower drain voltages compared to the Curtice model. It has a separate electro-thermal circuit too, to simulate self-heating. It is, however, a single pole model, and as discussed in the previous chapter, this can be detrimental at high frequencies, where there might be typically more than one pole before the frequency of operation. In fact, for the device in discussion, this model will not work as it has two poles before 20 Ghz. This can be seen from Fig.11. The drain current is expressed as [47]:

\[
I_{ds} = I_{pk} [1 + \tanh(\psi)][1 + \lambda V_{ds}] \tanh(\alpha V_{ds})
\]

where,

\[
\psi = P1 \times (V_{gs} - V_{pk}) + P2 \times (V_{gs} - V_{pk})^2 + P3 \times (V_{gs} - V_{pk})^3 + \ldots
\]

### 3.3 Large Signal Model used in this work

In all of the previously described models, the large signal modelling has been performed based on measured device data. Hence the effects due to trapping and self-heating have to be accommodated mandatorily, for which these in-built models have proved to be very useful. This work, on the other hand, employs the use of simulated data from Atlas TCAD,
which has assumed ideal behavior in terms of trapping and self-heating. Hence, in this work, instead of using a pre-existing in-built model, a self-defined large signal model has been created that has the capability of predicting the device behavior at its intrinsic level. Fig.28 shows the large signal equivalent circuit that has been used in this work. This was designed for a device width of 100 µm. It is directly drawn from the small signal model equivalent that was discussed previously, except for the difference that the capacitances have been implemented as charge sources. In a number of recent works [27], nonlinear capacitance-based large signal models were implemented directly instead of charge sources to avoid the problem of path-dependent integration. In nonlinear capacitance-based large signal models, DC spectral components will be generated unless terminal charge conservation conditions are specified. To avoid this unrealistic DC current flow in the implementation of these capacitance based large signal models, additional DC blocking capacitances need to be used.[24]

Figure 28: Large Signal Circuit Equivalent of the HEMT
3.3.1 Nonlinear Charge Modelling

As seen in Fig. 28, the nonlinear capacitances have been implemented as quasi-static gate charge sources \( Q_{gs} \) and \( Q_{gd} \). The non-quasi static effect of the channel charge is modelled with the two bias-dependent resistances \( R_{gd} \) and \( R_i \), which will account for the charging times of the depletion region capacitances[36]. [24] shows that if the modelling of these bias dependent charges is performed maintaining its symmetry with respect to the gate, it is a closer match to the small signal model discussed in the previous chapter and provides better convergence in nonlinear simulations. Thus, with a path dependent integration of these charge sources, \( Q_{gs} \) and \( Q_{gd} \) can be defined as the following:[37]

\[
Q_{gs}(V_{gs}, V_{ds}) = \int_{V_{gs}}^{V_{gs,0}} C_{gs}(V_{gs}, V_{ds,0})dV + \int_{V_{ds}}^{V_{ds,0}} C_{ds}(V_{gs}, V) dV
\]

(3.8)

\[
Q_{gd}(V_{gs}, V_{ds}) = \int_{V_{gs}}^{V_{gs,0}} C_{gs}(V_{gs}, V_{ds,0})dV - \int_{V_{ds}}^{V_{ds,0}} [C_{ds}(V_{gs}, V) dV + C_{gd}(V_{gs}, V)]dV
\]

(3.9)

3.3.2 Large Signal Modelling in ADS

The symbolically-defined device (SDD) is an equation-based component in ADS [38] that aids in quickly and easily defining custom, non-linear components. It is a multi-port device that can be modeled directly on a schematic. It is defined by specifying equations that relate port currents, port voltages, and their derivatives.

Fig.29 shows the large signal equivalent circuit of the HEMT modelled using a symbolically defined device[39,24]. It has been implemented with a 7 port SDD. Every term has an implicit, explicit or a weighting function expression. An explicit term is when
the quantity is directly equal to the listed expression and an implicit term is when the quantity is solved for, using the expression listed equated to zero. A weight of 0 denotes a resistance or a voltage usually, and a weight of 1 denotes a capacitance or an inductance. The weighting function with a weight of 2 denotes a time delayed quantity. Port 1 to 6 correspond to $Q_{gs}$, $Q_{gd}$, $R_i$, $R_{gd}$, $R_{ds}$ and $I_{ds}$ respectively. Port 7 has a 1 ohm termination, and a weighting function that enables us to obtain a delayed version of the input voltage, referencing to the small signal parameter, $\tau$.

Figure 29: Device modelled using SDD in ADS
This large signal model is a look-up table model implementation [40,24]. Each of these large signal device nonlinear parameters were written in the form of a data file for every corresponding $V_{gs}$ and $V_{ds}$, similar to a multidimensional array.

The Data Access Component (DAC) in ADS has been employed to assist in reading the data from the file and performing subsequent interpolation of the data. Fig. 30 shows the SDD along with the DACs for each component. The DAC is a general multi-purpose file reader. The independent variables (in this case $V_{gs}$ and $V_{ds}$) are specified and the DAC fits the required nonlinear data as a function of the independent variables. A cubic spline interpolation method has been chosen for each of the nonlinear components as it achieved the best possible fit for the data. This look-up table method of implementation saves a lot of time and complexity that would occur if each of the components were modelled as a polynomial and then fed into ADS as a nonlinear function of $V_{gs}$ and $V_{ds}$. In this case, several components such as $C_{ds}$ and $R_{gd}$ did not fit into polynomial based functions and had to be modelled using spline functions. The DAC serves that purpose effectively.
3.4 Linearity Characteristics

Before explaining about the harmonic balance simulations, a brief discussion about the important linearity performance metrics is essential. The most important linearity characteristics while evaluating a power amplifier’s performance are the intermodulation distortion expressed in the form of IIP3 (Input Third Order Intercept Point), the P1dB (Input Gain Compression Point), the carrier to intermodulation power ratio (C/I) and the adjacent channel power ratio (ACPR). A brief description of these characteristics are given below.
3.4.1 P1 dB gain compression point

At low-level input signals, an amplifier has a constant gain and linear behavior. However, as the input levels increase, the amplifier gets saturated and the output signal will no longer increase proportionally with the input signal. The input power level where the amplifier has 1 dB less linear gain due to saturation is defined as 1 dB compression point and it is considered as an important parameter for the linearity of a PA. Fig.31 indicates the P1dB input compression point on a plot of output power versus input power. The greater the value of the P1dB compression point, the higher the linearity, as it means that there is a greater input power range over which the amplifier can operate without entering the gain compression region.

Figure 31: P1 dB compression point
3.4.2 IIP3

The third order intermodulation distortion is always an unwanted component, which increases at one-third the rate of the input power. The input power at which the third order intermodulation component equals the fundamental output power is termed as input third order intercept point (IIP3) as shown in Fig.32. It should be noted that the IIP3 is usually an extrapolated point just for easy reference to estimate the linearity. Usually the highest input power at which the power amplifier is operated is well below the IIP3 point.

![Figure 32: Input third order intercept point (IIP3)](image)

3.4.3 C/I ratio

This is the ratio of the fundamental to the third order intermodulation power. While the IIP3 gives data about the linearity based on a singular point, the C/I ratio is a more reliable metric, since it provides data about the IM3 suppression at every input power level. It takes into consideration uneven third order intermodulation behavior which the IIP3 does not.
3.4.4 **Adjacent Channel Power Ratio (ACPR)**

Adjacent channel power ratio (ACPR) is the ratio of the average power in the main channel and any adjacent channels. It characterizes spectral regrowth in a communications system component, such as a modulator or an analog front end. Amplifier nonlinearity can cause spectral regrowth. ACPR calculations determine the likelihood that a given system causes interference with an adjacent channel. ACPR can be determined only if the large signal equivalent of the circuit is driven with modulated signals. If a distorted input modulated signal is fed to the device, the distortion can get worse or amplified due to the intrinsic nonlinearity present in the device. This AM-AM conversion is one of the main causes of adjacent channel power leakage[41].

3.4.5 **Power Added Efficiency (PAE)**

While the PAE is not a linearity metric, it is still one of the most important performance aspects of a power amplifier. The PAE has been discussed later in this chapter and hence, it is necessary to mention it. It is the ratio of the difference in the output and input power to the DC power consumed in the circuit.

3.5 **Harmonic balance simulations in Agilent ADS**

Harmonic balance is a frequency-domain analysis technique for simulating nonlinear circuits and systems. It is well-suited for simulating analog RF and microwave circuits, since these are most naturally handled in the frequency domain. Circuits such as power amplifiers, mixers and oscillators are best analyzed using harmonic balance under large
signal conditions. Harmonic Balance Simulation calculates the magnitude and phase of voltages or currents in a potentially nonlinear circuit. It can be used to compute quantities such as P1dB, third-order intercept (TOI) points, total harmonic distortion (THD), and intermodulation distortion components [38].

Fig. 33 shows the setup of the harmonic balance simulation for the device. Single tone analysis was performed at 20 Ghz, and two-tone analysis was performed at 20 Ghz and at 100 kHz offset from the same. An order of 3 was used for the simulation, meaning that power distribution and non-linearities up to the third harmonic frequency was taken into consideration. Since the setup consists of a 50 Ω termination at both the input and output side, matching networks have been designed in order to ensure maximum power transfer to and from the device and minimize the reflection losses. The matching networks also help to compare the behavior of different devices more easily if all of them are matched to the same input and output impedance. For the design of input and output matching networks, two optimization conditions were set in ADS using the optimizer tool for the large signal scattering parameters: S11 < -15 dB and S22 < -15 dB. Based on these conditions, for a given bias, the LC matching network values were calculated.

<table>
<thead>
<tr>
<th>Lumped Element</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>L_match_in</td>
<td>0.132 nH</td>
</tr>
<tr>
<td>C_match_in</td>
<td>0.529 pF</td>
</tr>
<tr>
<td>L_match_out</td>
<td>0.562 nH</td>
</tr>
<tr>
<td>C_match_out</td>
<td>0.075 pF</td>
</tr>
</tbody>
</table>
The input power source performs a power sweep from -30 dBm to 20 dBm. Two DC blocking/AC coupling capacitors of 100 pF have been added at the input and output nodes. The gate and the drain biases have been input through high DC feedthrough inductors of 1 uH. These DC feedthrough or RF choke inductors act as shorts at low frequency and also allow the drain voltage of the amplifier to swing up to twice of the drain bias provided.

3.5.1 Harmonic balance simulation convergence requirements

For good convergence of harmonic balance simulations, the derivatives of the components in the circuit must be well-defined and continuous. For this purpose, all the data fed into the large signal models had to be smoothed as it helps remove abrupt non-linearities.
without changing the function significantly. It eliminates points that are completely off from the interpolated trend of the plot. Additionally, the Krylov solver method was used as against the direct solver in ADS [38]. The Krylov method is intended for solving large circuits with many devices, non-linear components, and number of harmonics and therefore helped achieve better convergence. A disadvantage of using the look-up table method is that while the simulator performs the interpolation by itself, it cannot extrapolate to any data beyond the data points that have been given as an input [42]. This implies that for a 4V range of input bias, the maximum input power that can be fed into the circuit is less than 20 dBm, as the peak-peak swing must be kept within this voltage range. If it exceeds this range, the simulator will not allow convergence. Since the drain bias was defined was a larger number of points, convergence issues due to exceeding of power limits did not occur due to the drain node.

3.5.2 Harmonic balance simulations bias points

Since this modelling work is primarily focused on power amplifier applications, a brief discussion about the various classes of linear power amplifiers will put into perspective the choice of bias point for the Harmonic Balance Simulations. Class A, B, AB and C are the four types of linear power amplifiers. The important distinction between them is the amount of time the transistor conducts in a given time period or the conduction angle, which is shown in Fig. Class A amplifier is on throughout, Class B is on for exactly half the cycle, Class AB conducts for more than 50% but less than 100% of the cycle and Class C conducts for less than 50% of the cycle. Fig.34 shows the differences in the conduction
angle of the 4 classes. The main trade-off with respect to the conduction angle is between efficiency and linearity. The greater the conduction angle, the lower the efficiency but the better the linearity.

![Diagram showing conduction angles of classes A, B, AB, and C]

Figure 34: Linear power amplifiers’ conduction angles

Fig.35 shows the optimum loadline of the HEMT on a plot of drain current vs the drain voltage. The loadline helps determine the maximum output power than can be obtained for a given bias point and calculate the optimum output impedance for maximum power transfer. Fig.35 shows the bias points for the amplifier classes. Class A’s quiescent point is in the midpoint of the loadline so that the transistor is always on. The gate bias is fixed so that the lowest point of the input sine wave is always above the threshold voltage of the transistor. Class B is biased at exactly the threshold voltage so that only 50% of the input wave is available and Class AB is biased between these two classes. [43]
Since Class A’s input waveform is almost entirely a pure sine wave, there are hardly any other tones except the fundamental tone. As the amplifier moves from Class A, closer to Class B, the power in the second and third order tones increase, which is the cause of the steadily increasing non-linearity. To make Class B more linear, usually a harmonic termination is added at the output so that it resonates at the third order frequency of the fundamental. Class A can achieve a maximum of 50% efficiency, while Class B can achieve a maximum of 78.5% efficiency.

Since this work is directed at obtaining the linearity characteristics, the initial set of bias points were chosen to maximize linearity of the amplifier. Based on the previous section, this means that the right choice of bias point would be that of the Class A bias. Since the
threshold voltage of the device is -2 V and the gate bias range over which the data is available is till 2 V, the Class A gate bias point was chosen at 0 V. Several factors were taken into consideration to maximize the linearity:

i. Since the transistor has to be always on for Class A bias, the minimum value of the sine wave has to be close to -2 V. The limitation of table-based modelling gives an upper limit of 2 V, which means that the input power cannot exceed 20 dBm as stated previously.

ii. Similar analysis is performed for the drain bias. Usually the linearity increases as the drain bias increases, hence a high drain voltage of 15 V was chosen. Any higher than that might cause the output swing to exceed the limits beyond the maximum drain bias for which the look-up table model has been created.

iii. Since \( g_m, C_{gs}, C_{gd} \) and \( g_{ds} \) are the main sources of nonlinearity from the device, attempts were made to choose bias points in which nonlinearities caused by these parameters would be minimum. At 15 V drain voltage, \( g_{ds} \) and \( C_{gd} \) have nearly linear behavior as seen in Fig 18. Since \( C_{gs} \) generates third order non-linearity mainly from the second order component of \( V_{gs} \), biasing the transistor at a gate voltage about which the \( C_{gs} \) is anti-symmetric can help minimize the third order distortion. [31]. However, since \( C_{gs} \) does not have a symmetric distribution with respect to the gate voltage in a standard HEMT, choosing such a point in this case is not possible. To minimize \( g_m \) non-linearity, one of the possible ways to choose it would be to select a point where the \( g_{m3} \) is minimum.
Based on Fig. 36, gm3 is low around the 0-1 V range, hence 0V would be a good choice of bias point from this perspective too.

Before the results of the harmonic balance simulations are discussed, the motivation behind graded channel HEMT devices is explained, and the linearity results of both the devices are presented together to make it easier to compare their performance.

3.6 Graded Channel HEMTs

As mentioned in Chapter 2, the velocity saturation model developed by [20] and incorporated in this work, states that the saturation velocity decreases as the carrier concentration increases as shown in Eq.(2.1). Since the transconductance $g_m$ is directly proportional to the saturation velocity, the decrease in saturation velocity with the increase of carrier concentration, leads to the collapse of the transconductance. It was shown
previously in this chapter how the nonlinear $g_m$ can cause third order intermodulation distortion and gain compression.

We can state that a flat transconductance would definitely mitigate the nonlinearity. Hence, the rapidly dropping behavior of $g_m$ can be reduced if we spread the charge distribution of the 2DEG over a certain distance in polarization-graded AlGaN HEMTs. [44]. This can be achieved by grading the channel layer of the HEMT. A three dimensional electron gas arises from the polarization grading of the channel layer from GaN to low composition AlGaN layer, such that the polarization charge is smeared over the graded region [20]. This spreading of the carrier charge ensures that the saturation velocity does not reduce too much, thereby preventing the sharp gm collapse. The mobility of the structure with a graded AlGaN layer is also higher at the high gate voltage region. This is due to the higher polar optical phonon mobility and interface roughness mobility for the graded-layer structure. Hence, using the channel grading, we can obtain a transconductance profile that is flat over a larger range of gate bias. Fig. 38 shows the energy band diagram of the graded junction device shown in Fig. 37. The charge is spread over a longer distance and the abrupt notch in the conduction energy band is reduced compared to the standard case.

![Figure 37: Graded Channel HEMT Device Structure](image)
Fig. 37 shows the graded channel HEMT device that was simulated in Silvaco Atlas TCAD and subsequently, analyzed for small signal and large signal modelling. This is a short channel device too, with the same gate length of 0.25 µm, a gate-source distance of 0.5 µm.
and a drain-source distance of 1 µm. The 20 nm AlGaN barrier is graded from 0 to 30% followed by an 800 nm GaN buffer. The device has been designed so that the sheet charge density is $10^{13}$ /cm$^2$. This device is different from the recessed standard device analyzed previously in terms of the grading, the barrier thickness, and the source-drain distance. An analysis similar to the one performed for the previous device is presented for this device too, which helps us to compare how the change in the epitaxy affects the results from the Silvaco simulations and the small signal extraction procedure.

3.6.1 Graded Channel HEMT Silvaco and Small Signal Results

Figs (40-43) show the results from the Silvaco simulations. We see that in the graded channel HEMT, the pinch-off voltage is more negative than the conventional HEMT case because the conventional HEMT structure that was used, was recessed. This structure has a threshold voltage of -3V. The transconductance $g_m$ does not collapse as it does in the other case, due to the grading of the channel. It remains flat for a range of 2 V and then, in fact slightly increases. Due to this, it is seen that the current obtained for a given voltage is slightly higher than that of the standard channel HEMT. The peak $g_m$ is higher for the standard case due to the recessing.

The current gain vs frequency plots in Fig. 42 show that the unity gain frequency for the graded HEMT at gate voltages of around -1V is higher than that of the standard device. This is expected as the $g_m$ is higher for the graded case at this gate voltage ($f_t = g_m/(2\pi C_{gs})$). The maximum available gain in this case is around 13 dB which is 4-5 dB higher than the standard case, since the intrinsic gain of a device is $g_m r_o$ and since $g_m$ is close to twice of
the value of the standard HEMT’s transconductance at this bias, a gain increase of 3 dB is expected, assuming the output conductance does not change much. A second pole is observed in this case too, close to 20 Ghz.

Figure 40: Graded HEMT $I_{ds}$ vs $V_{ds}$

Figure 41: Graded HEMT $I_{ds}$ and $g_m$ vs $V_{gs}$
Similarly, Fig (44-51) show the small signal extracted parameters at 20 GHz of the graded channel device obtained with the same methodology described in Chapter 2. The high frequency drain current as seen in Fig.51 steadily increases with increasing gate bias, as compared to standard case where it saturates. The $g_m$, as expected is flat over the gate bias range, matching the Silvaco DC simulations closely. The $C_{gs}$ also shows a steadily
Figure 46: Graded HEMT $g_{m}(V_{gs},V_{ds})$

Figure 47: Graded HEMT $C_{ds}(V_{gs},V_{ds})$

Figure 48: Graded HEMT $R_{i}(V_{gs},V_{ds})$

Figure 49: Graded HEMT $R_{gd}(V_{gs},V_{ds})$

Figure 50: Graded HEMT $g_{ds}(V_{gs},V_{ds})$

Figure 51: Graded HEMT $\tau(V_{gs},V_{ds})$
rising behavior with the gate voltage, unlike the standard HEMT’s $C_{gs}$, where it saturates after 0 V. This is because the current does not saturate in the graded junction, due to which the width of depletion layer under the gate keeps changing for the range of gate bias that we monitor. This leads to the increasing $C_{gs}$ behavior. From a linearity perspective, this is better than the saturated behavior since it is possible to find a gate bias point about which the $C_{gs}$ is anti-symmetric, which will help mitigate third order intermodulation distortion.

The $R_i$ values and trend is very similar to the standard case, while the $R_{gd}$ is lower in the case of the graded HEMT, since the gate-drain length is smaller. The $g_{ds}$ and $C_{ds}$ exhibit very similar behavior as the standard HEMT, and are reasonably linear at high drain voltages. The $\tau$ is slightly smaller than the standard case for the graded case as the unity gain frequency is higher for the graded channel HEMT.
Table 4 shows the extracted extrinsic resistances for the graded channel HEMT small signal model. Only the $R_d$ is significantly different and lower from the standard case, since the gate-drain distance of the graded channel HEMT is smaller. After small signal parameter extraction, the same large signal circuit equivalent that was used for the standard HEMT was employed for this device too, to obtain the linearity characteristics.

Table 4: Graded HEMT extrinsic small signal parameters

<table>
<thead>
<tr>
<th>Extrinsic Resistance</th>
<th>Value (Ω)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_s$</td>
<td>5</td>
</tr>
<tr>
<td>$R_g$</td>
<td>4</td>
</tr>
<tr>
<td>$R_d$</td>
<td>9</td>
</tr>
</tbody>
</table>

3.7 Results of harmonic balance simulations

As mentioned in the previous section, the standard recessed HEMT device model was biased at 0V gate bias, 15 V drain bias and 88 mA of drain current. Fig. 53 shows the fundamental output power and the vs the input power for the recessed HEMT structure model. A gain of close to 8 dB is obtained, with a P1 dB compression point of 13 dBm. The gain is 1 dB lesser than the maximum available gain of the device simulated from Silvaco directly at 20 Ghz frequency. The maximum simulated power is 24 dBm which translates to 3 W/mm. [45] has reported 4.5 W/mm for a 0.25x100 μm$^2$ AlGaN/GaN HEMT at 20 Ghz, with a gain of around 11 dB and a gain compression point of 17 dBm input power. This shows that the simulated values are in the right ballpark, although a little lesser
than expected. The main reason for this could be the limited number of data points provided in the lookup table, which restricts the bias points over which the amplifier can operate.

Fig. 53 shows the efficiency of the amplifier. Owing to the fact that it is almost entirely operating in Class A, the power added efficiency is under 10% and very low. The main reason for this is the high current density of the device, which is 880 mA/mm. Biasing this transistor in deep Class AB will provide much higher efficiency with only limited loss of linearity.
Fig 56 shows the fundamental output power and the third order intermodulation distortion power as a function of the input voltage. The IIP3 can be determined as 27 dBm, which is 14 dBm higher than the P1 dB compression point. The IM3 power deviates from the ideal curve at input powers greater than 0 dBm indicating increasing non-linearity at those values. Fig. 57 shows the C/I ratio as a function of the input power. The IM3 suppression
at high input powers drops below 20 dBc due to relatively low gain. [46] reports an intermodulation distortion of -19 dBm at 10 dBm input power for a device of similar dimensions at 10 GHz which is quite close to the IM3 value of -16 dBm at 10 dBm input power in this work.

Fig.(58-62) show the harmonic balance simulation results of graded channel device. For the graded channel device, the bias points were chosen at 15 V drain bias, -1 V gate bias and 95 mA drain current. The maximum gain is around 11.8 dB, which is lower than the maximum available gain simulated through Silvaco. The gain from this device is higher as compared to the standard case by 3.5 dB since, the $g_m$ at the respective bias point is higher, owing to the transconductance collapse of the former. The 1 dB compression point is higher by around 1 dB, showing very slight improvement in linearity. The power added efficiency is also marginally higher than the former case, due to the higher output power that is achieved for nearly the same bias point, which is almost 5W/mm.

Figure 58 : Graded HEMT o/p vs i/p power

Figure 59: Graded HEMT gain vs i/p power
Figure 60: PAE of graded HEMT

Figure 61: Graded HEMT IIP3

Figure 62: Graded HEMT C/I ratio
The third order intermodulation distortion of the graded channel HEMT is shown to be significantly better in Fig. 63. While the IIP3 itself may be only 2 dBm higher, the average IM3 is nearly 5 dB lower than the standard case, and the intermodulation power is closer to the ideal line. This can be mainly attributed to the flat $g_m$ and the antisymmetric behavior of $C_{gs}$ about the gate bias point. The higher output power as well as the lower distortion gives an IM3 suppression of around 10 dB higher.
Chapter 4: Conclusion and Future Work

The goal of this thesis was to accept the device structure of an AlGaN/GaN HEMT as an input and create a methodology and blackbox that would provide information about the device’s linearity and power delivered as an output, completely through simulation work. The first step was to model a 0.25 µm x 100 µm device using Silvaco Atlas TCAD to obtain two port network parameters over a wide range of bias points and frequencies. The small signal parameters of the device were extracted as a function of the bias and frequency from the two port network parameters. The small signal circuit equivalent’s S parameter results were compared with TCAD S parameter results in order to validate the model. These small signal parameters were fed into a large signal circuit equivalent of the HEMT using a look-up table based model in Agilent ADS. Harmonic balance simulations at a high frequency of 20 Ghz were performed using the large signal circuit to obtain the output power and linearity characteristics of the device. Since the focus of the modelling was for RF linear power amplifier applications, the reasoning behind choosing Class A bias points for the operation of the device during harmonic balance simulations to maximize the linearity was also explored. The harmonic balance simulation results were compared to experimental results of similar structures that have been published over the last decade. Most of the simulated results have reasonable values, however, the output power density and achieved linearity are lower compared to the performance of current cutting edge GaN based
devices. The main reason for this is the constraint of the look-up table interpolation model that can operate over only a limited range of input powers, thus not providing information about the model at a high input power. Therefore, the model does not give a clear idea about the best possible performance of the device as it is bound by the data limitation issue. The harmonic balance simulations did not have good convergence in bias points other than Class A such as Class AB and Class B. To overcome this, the solution would be to train the model better using a much larger set of data points (bias and frequencies). [22] uses a technique called B-spline approximation which could be a possible solution to achieve convergence in all situations.

Furthermore, this work elaborated on the motivation behind the design of graded channel junctions and how they can improve the linearity of the device. The same model and methodology were used to obtain the power and linearity of a 0.25 μm graded channel device and the two results were compared and analyzed based on the physics of the device. The graded channel device did show better intermodulation distortion performance compared to the standard one, as expected, which the model was able to predict to a good degree.

The salient aspect of this work was that it was completely predictive device modelling without making use of any predefined large signal models. It also eliminates the need of using equations to model the small signal parameters and instead uses the capabilities of Agilent ADS to perform cubic spline fitting of the data, which can save a lot of time and
computational complexity. It aims at being re-suable by any kind of FET device, however as previously mentioned this would require more input data points and faster computational methods. Another important aspect is that since, it is completely simulation based, this model has not taken into consideration the effects of gate leakage, self-heating, package parasitics and traps-induced dispersion. While these effects are being mitigated currently using passivation, recessing, substrates with good thermal conductivities and other epitxial solutions, these can still cause significant distortion from the ideal outputs and could be taken into consideration for a more wholesome and accurate predictive modelling of the device.
References


Appendix A – Silvaco code for AlGaN/GaN HEMT

go atlas
simflags="-P 4"

Set VgStart=3
Set VgEnd=-8
Set Vd1=10
Set VgRF=-4
Set VdRF=10

Set pol=1

Set Lg=.25
Set Lgs=.5
Set Lgd=2
Set Lc=0.5

Set Ls0=-$Lg/2
Set Ls1=-$Lg/2-$Lgs
Set Ls2=$Ls1-$Lc

Set Ld0=$Lg/2
Set Ld1=$Lg/2+$Lgd
Set Ld2=$Ld1+$Lc

### x-dir mesh size
Set Lm1=5e-3
Set Lm2=1e-2
Set Lm3=5e-2
Set Lm4=1e-1

### The sample consisted of 1 um GaN buffer layer followed by a 30 nm Al(0.25)Ga(0.75)N layer
Set tAir=1
Set tBar1=30e-3
Set tBar2=0
Set tCh=50e-3
Set tsub=1

### Metal thickness
Set tOhmic=0.1
Set tGate=0.1
set t1=$tBar1
set t2=$t1+$tBar2
set t3=$t2+$tCh
set t4=$t3+$tsub

### Mesh size
set Tm1=5e-4
set Tm2=$t1/5
set Tm3=1e-2
set Tm4=4e-2
set Tm5=1e-1

# 1 Mesh

mesh
### Set x-dir meshes
x.m l=$Ls2 s=0.1
x.m l=$Ls1-5e-3 s=0.05
x.m l=$Ls1 s=50e-3
x.m l=$Ls0-50e-3 s=50e-3
x.m l=$Ls0 s=10e-3
x.m l=0 s=10e-3
x.m l=$Ld0 s=10e-3
x.m l=$Ld0+50e-3 s=50e-3
x.m l=$Ld1 s=50e-3
x.m l=$Ld1+5e-3 s=0.05
x.m l=$Ld2 s=0.1

### Set y-dir meshes
y.m l=$tAir s=0.1
y.m l=-0.2 s=0.1
y.m l=($tGate+0.05) s=0.1
y.m l=$tGate s=0.01
y.m l=0 s=1e-3
y.m l=$t1-1e-3 s=1e-3
y.m l=$t1 s=1e-3
y.m l=$t2 s=2e-3
y.m l=$t2+15e-3 s=2e-3
y.m l=$t3 s=2e-3
y.m l=$t3+10e-3 s=2e-3
y.m l=$t3+20e-3 s=0.1
y.m l=$t4 s=0.1
#\nregion num=1 material=Air  x.min=$Ls2  x.max=$Ld2  y.min=-$tAir  y.max=0
region num=2 material=SiN  x.min=$Ls2  x.max=$Ld2  y.min=-$0.2  y.max=0
region num=3 material=AlGaN  x.min=$Ls1  x.max=-0.125  y.min=0  y.max=30e-3
donor=1e15  polarization  polar.scale=$pol  calc.strain  x.comp=0.25
region num=4 material=AlGaN  x.min=-0.125  x.max=0.125  y.min=20e-3  y.max=30e-3
donor=1e15  polarization  polar.scale=$pol  calc.strain  x.comp=0.25
region num=4 material=AlGaN  x.min=0.125  x.max=0.125  y.min=0  y.max=30e-3
donor=1e15  polarization  polar.scale=$pol  calc.strain  x.comp=0.25
region num=5 material=GaN  x.min=$Ls1  x.max=$Ld1  y.min=30e-3  y.max=$t3
donor=1e15  polarization  polar.scale=$pol  calc.strain
region num=6 material=GaN  x.min=$Ls2  x.max=$Ld2  y.min=$t3  y.max=$t4
insulator  polarization  polar.scale=$pol  substrate

#OHMICS
region num=7 material=GaN  x.min=$Ls2  x.max=$Ls1  y.min=0  y.max=$t3
donor=1e21
region num=8 material=GaN  x.min=$Ld1  x.max=$Ld2  y.min=0  y.max=$t3
donor=1e21

##Electrodes

#Source
elec num=1 name=source  x.min=$Ls2  x.max=$Ls1  y.min=-$tOhm icy.max=0

#Drain
elec num=2 name=drain  x.min=$Ld1  x.max=$Ld2  y.min=-$tOhm icy.max=0

#Gate
elec num=3 name=gate  x.min=$Ls0  x.max=$Ld0  y.min=-$tGate
y.max=20e-3

## 3 Material
material kp.set2  pol.set2
material material=AlGaN  F.TOFIMUN=OP_gan5.lib
material material=GaN  F.TOFIMUN=OP_gan5.lib

##Contacts
contact name=source  resistance=200
contact name=drain  resistance=200
contact name=gate  workfunc=5.40  resistance=400
trap acceptor e.level=3.28 density=4e16 degen=4 sign=2.84e-15 sigp=2.84e-14 x.min=$Ls2 x.max=$Ld2 y.min=$t3 y.max=$t4

models srh fermi spontaneous print polar.scale calc.strain

## 4 Solution
method gummel newton carr=2 itlim=50 trap maxtrap=20 print
output con.band val.band charge polar.charge flowlines e.field e.velocity ex.velocity ey.velocity e.mobility e.temp band.par

Initial solve
solve init
save outf=standardalganganhemt.str

S Parameter RF Simulation
solve vdrain=10
solve vgate=-2
log outf=ganvd10vg-2.log master gains s.params inport=gate outport=drain
solve ac freq=10 fstep=10 mult.f nfstep=7
solve ac freq=1e9 fstep=1e9 nfstep=8
solve ac freq=1e10 fstep=5e9 nfstep=12
log off

Velocity Saturation Model C-Interpreter Function (written by Pil Sung Park)

```c
#include <stdio.h>
#include <stdlib.h>
#include <math.h>
#include <ctype.h>
#include <malloc.h>
#include <string.h>
#include <template.h>

/*
* Optical Phonon Limited field & charge density dependent mobility model
* based on General field dependent mobility model for electrons.
* TOtal FIeld Mobility (parallel and perpendicular field components)
* Statement: MATERIAL/MOBILITY
* Parameter: F.TOFIMUN
* Arguments:
* Eperp    [in] - perpendicular electric field (V/cm)
* Na       [in] - acceptor concentration (/cm^3)
* Nd       [in] - donor concentration (/cm^3)
* nconc    [in] - electron concentration (/cm^3)
*/
```
* Epar  [in] - parallel electric field (V/cm)
* TL   [in] - lattice temperature     (K)
* xcomp [in] - x-species fraction      (0-1)
* ycomp [in] - y-species fraction      (0-1)
* *mun  [return] - hole mobility (cm²/Vs)
* *dmundep [return] - derivative of *mun wrt Eperp
* *dmundepar [return] - derivative of *mun wrt Epar
* *dmundl [return] - derivative of *mun wrt TL
* *dmundn [return] - derivative of *mun wrt nconc

int tofimun(double Eperp,double Na,double Nd,double nconc,double Eparl,double TL,double
  xcomp,double ycomp,double *mun,double *dmundep,double *dmundepar,double
  *dmundl,double *dmundn)
{
  double n0 = 6e19;
  double alpha = 1;
  double vsat, mu0;
  double beta, a, b, c, d, da, db, dc, dd;

  vsat=alpha*1.0e7/(0.38+sqrt(nconc/n0));
  mu0=2200;
  /* mu0=3000/(1+3/(1+3*sqrt(nconc/n0))); */

  if(Eparl == 0)
  {
    *mun=mu0;
    *dmundepar = 0.0;
  }
  else
  {
    beta = 2.0;
    a = mu0*Eparl/vsat;
    b = pow(a,beta);
    c = 1.0 / (1.0 + b);
    d = pow(c,1.0/beta);
    *mun=mu0*d;
  }
  return(0);                /* 0 - ok */