DC Arc Fault Detection and Protection in DC Based Electrical Power Systems

Dissertation

Presented in Partial Fulfillment of the Requirements for the Degree Doctor of Philosophy in the Graduate School of The Ohio State University

By

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Abstract

DC based electrical power systems are required in many emerging applications, such as more electric aircraft, hybrid electric vehicle, photovoltaic power plant, residential microgrid, etc. A very challenging problem in dc systems is arc faults. They can be caused by loose connections or degraded insulation, where very small air gaps are created. The voltage difference across the small gap will initiate a plasma arcing channel with extremely high temperature. If not detected and extinguished in time, arc faults could endanger adjacent circuits and eventually cause fire hazards. Although it is very crucial to minimize the impact of dc arc faults through timely detection and extinguishing, the research topic of dc arc fault detection and system level protection has not been studied very closely before. It is quite recent that dc systems are being used extensively for power distribution. Moreover, modern energy sources and power electronics based loads in aforementioned applications also make this research topic more challenging.

This work proposes a novel detection scheme to improve the detection accuracy and to reduce unwanted false tripping. It has been achieved by investigating physical characteristics of the dc arc and analyzing the arc current signals. The voltage-current characteristics of the dc arc as well as the high frequency arc noise is modeled and analyzed. This model enables an accurate simulation study of the dc arc. A new detection scheme based on two arc signatures from both time domain and time-frequency
domain is proposed and verified through experiments. This strategy increases the detection accuracy and reduces the possibility of false trip. Moreover, the impact of dc arc to a larger system, e.g. a dc microgrid with multiple voltage sources and multiple resistive loads, is studied. The interactions between dc arc faults and two typical microgrid control strategies are also analyzed. The final portion of this research is focused on system level detection and protection. A comprehensive dc arc fault detection and protection scheme which can be integrated with the existing protection system of a dc microgrid is proposed in order to improve protection efficiency and minimize additional hardware/software installations.
This is dedicated to my family:
My husband, Mr. Luis Herrera;
My father, Mr. Enhui Yao;
My mother, Mrs. Yunxia Niu.
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Chapter 1: Introduction

DC electric power systems are being used extensively in many modern applications. With the development of renewable energy technology and power electronics applications, dc networks for power distribution have been studied to integrate renewable resources interfaced by power electronics [1]-[3]. Promising advantages can be brought by this development, but the challenges of introducing large number of dc components in power networks should not be overlooked, one of which would be dc arc fault. Fig. 1.1 shows several dc arc fault induced accidents or situations that could develop dc arc faults [4]-[6].

DC arc faults typically occur in the electrical systems that involve high voltage dc buses. For example, the Photovoltaic (PV) string inverter or dc bus is usually in the range of a few hundred volts, which makes the PV plants highly subject to dc arc faults [7]-[9]. Moreover, with the rapid evolution of the More Electric Aircraft (MEA) concept, the electrical system voltage in aircraft is increased from 28 Vdc to 270 Vdc or even higher. This is to optimize the power-to-weight ratio of an aircraft, meet greater electrical demand and improve efficiency of the energy supply system of the aircraft [10]. Similar high voltage dc buses can also be found in Electric Vehicles (EVs) or Hybrid Electric Vehicles (HEVs). An EV/HEV electrical system usually incorporates different voltage levels through various power electronics converters. The
electric motor voltage can be as high as 650 V and the nominal voltage of battery pack and the dc link voltage is usually around 300 V. Similar dc systems can also be found in data centers, telecom power supplies, electric ships, etc.

(a) Fire accident caused by dc arc in PV panels [4].
(b) Aging wires on airplanes [5].
(c) Arcing after EV crash [6].

Figure 1.1: Possible dc arc fault situations.

These dc networks containing high voltage dc buses and loads have a high potential to develop dc arc faults. If not detected and extinguished in time, the arc faults could spread to adjacent circuits and endanger the power sources, control systems, or even cause explosions in a confined space due to the growing arc pressure. Moreover, in dc networks most of the components including sources and loads are connected through power electronic circuits or converters. The Electro Magnetic Interference (EMI) noise from power electronic converter switching will further add difficulties in dc arc fault detection. Although it is very crucial to minimize the impact of dc arc faults through timely detection and extinguishing, the research topic of dc arc fault detection and system level protection has not been studied very closely before. It is quite recent that dc systems are being used so extensively for power distribution.
The arc fault detection has been studied extensively for ac electric power systems. However, these techniques cannot be adopted directly for dc systems for the following reasons. First of all, ac arc faults are intrinsically easier to detect and extinguish than dc arc faults because of their zero-crossing points. During the zero-crossing regions, the ac arcing will extinguish automatically and then reignite. Secondly, ac electric systems are very different from dc systems, in terms of the loadings, voltage sources, system topologies, and the number and types of power electronics circuits. These factors play a major role when developing techniques that can differentiate arc faults from normal operational conditions.

Some methods have been proposed for dc arc detection, however, there are still major challenges which remain unsolved and need further exploration. These challenges include more efficient fault detection and prevention from nuisance tripping. In this study, an experimental study of dc arc characteristics is conducted and factors such as dc source voltage, arc length, and arc current level are studied. The dc arc behavior under different conditions is examined to provide a solid foundation for future detection studies. Based on the experimental data, dc arc current signatures are presented based on both time and time-frequency domain analysis. A detection algorithm based on these signatures is proposed. Experiments are conducted to verify the detection method. This work is aimed at providing a comprehensive understanding of arcing behavior that could occur in dc networks, and proposing a method to detect dc arc faults.
1.1 Review on DC Arc Fault Detection

Although dc arc fault detection has been studied for the protection of electric vehicles, ships, and aircraft, it is still far less developed compared with the large amount of literature and patents on ac arc recognition [14]-[16]. However, with the developing trend of dc networks, as well as the new release of related standards requiring dc arc protection in PV installations, the research interest and demand of an efficient, simple, and cost effective dc arc detector is increasing rapidly [17] -[18]. Two standards related to dc arc fault detection in PV applications became available since 2011. The first is National Electric Code (NEC) 2011 article 690.11 where dc arc detection is required for systems with maximum voltage higher than 80 V [17]. The other is Underwriters Laboratories (UL) 1699B, which provides outline of requirements and test instructions of a dc arc fault interrupter for PV applications [18].

DC arc detection methods based on time domain signatures rely mostly on the arc current signal. They involve relatively simple calculation procedures but require more measures for nuisance tripping prevention. Statistical methods are adopted in [19] to identify an arc by studying the variance of the arc (voltage or current) signal. In [20], for automotive applications, voltage and current sensors at two different locations in the electrical circuit are utilized to detect anomalies caused by dc arcs. DC arc detection with time domain signatures is also seen in patents [21]-[24]. Current drop is used in [21] as a sign of a precursor to a dc arc so that it can be prevented right after the continuity is changed and before the arc fault is even developed. In [22], a fast change in the slope of voltage or current over time is considered as an arcing event. Moreover, [23] proposes a different detection method where the current will be
cut off momentarily and then connected back after sensing a current reduction. The current profile will be different when the current reduction is caused by an arc instead of normal operation. Lastly, in [24], parallel arcing is detected by examining the difference between maximum and minimum current values within a certain length of time. In addition, the series arc is detected by the change of average arc current within different time windows. This method indirectly introduces a strategy to prevent nuisance tripping from normal operational conditions and ambient noise.

Frequency domain signatures through Discrete Fourier Transform (DFT) are also widely applied. For example, the peak number of dc components from sliding window DFT or the movement of frequency component is shown in [25]. Likewise, in [26] a change of the current frequency spectrum is used as an evaluation parameter. This procedure assumes that when an arc occurs, the movement of frequency components is higher. Other dc arc detection methods based on frequency analysis are also seen in the literature [16], [27]. In [16], back propagation neural network analysis is used along with a Fast Frequency Transform (FFT) method in order to detect dc arc in spacecraft systems. Whereas in [27], using a wavelet packet based analysis, dc arc energy in different sub-bands is quantified into one variable by using the reconstruction coefficients in each band. These methods give insight into the frequency characteristics of a dc arc and also present the challenges in its detection, such as noise recognition, calculation time reduction, differentiation from load changes, etc.

Pattern recognition technology has also been proposed for dc arc detection. For example, one invention discussed the idea of using an Artificial Neural Network (ANN) to provide a normal model for arcing, to be compared after arcing features are extracted [25]. This invention proposes a comparatively new method for detection:
using ANN rather than a logical comparator with a threshold value, as in the earlier patents reviewed. However this patent only discussed the idea in a really brief way. It only discusses concepts. No actual implementation information, guidance or verification results are provided. To implement this idea, there is still a long way to go. For example, which kind of ANN to use has to be decided. Also, which few effective features can distinguish between normal conditions and arcing. How to establish the normal condition model also needs to be studied.

Nuisance tripping is one of the most important challenges of dc arc detectors. The measures applied by inventions to reduce or prevent nuisance tripping include: use multiple signatures instead of one; count the arcing events, up to a certain limit instead of giving an alert right after one arcing event indication. Threshold value selection is not usually addressed in patents even though some did mention the threshold value they recommended under certain applications. Considering that the threshold value is different under different operational conditions, it is easy to understand why threshold value selection is not thoroughly discussed. But some general guidance of how to set the threshold value would be helpful, which will be discussed in this work.

1.2 Motivations of the Work

The development of power electronics, renewable resources and other advanced technologies has opened a door to the possibility of using dc based electrical networks extensively, from generation to distribution. However, protection has been the bottleneck for wide implementation of dc networks. For transmission systems, the lack of dc circuit breakers is the major limitation. For distribution systems where the
voltage rating requirements of dc circuit breakers are lower, the major challenge for protection system design comes from many factors. Some of them are listed below:

- Increased possibility of dc arc fault due to higher dc voltage ratings and the difficulty in detecting series dc arc faults.

- Extensive usage of power electronics devices in modern dc systems increases ambient noises that may increase the possibility of false tripping.

- Enabled by power electronics technology, dc microgrids with multiple sources and multiple loads are adopted more than before. In contrast to dc distribution systems, dc microgrids usually adopt advanced control strategies to control and coordinate the power output of the multiple sources and the power flow within the network. The control strategy of dc microgrids can cause extra challenges to dc arc fault detection and localization, as well as the protection of other types of faults.

Based on the above analysis, one of the motivations in this work is to study the arc characteristics more in-depth. There was a burst of study of arc characteristics and arc modeling in the 1930s, when arc discharge was first discovered and methods to utilize arcs were being investigated. The arc discharge studied back then had a much higher arc current value than the current ratings used in modern lower voltage applications and a much longer arc length than the possible air gap caused by loosened connections or broken insulation in modern applications. Therefore, it is necessary to study arc discharge under the ratings and dimensions encountered in state-of-the-art applications.
Another motivation of this work is to establish fault signatures from characteristic study and develop better detection algorithms for dc arc faults. The detection algorithm should be able to distinguish arc fault from no-fault conditions. The algorithm should not send false detection signal due to environmental noises or normal operating conditions. The detection time should be within the requirements of industrial standards. The speed of detection is mostly determined by the computation load and the microprocessor adopted. The development of a better detection algorithm is oriented and motivated by the above guidelines.

The prevention of false tripping becomes more challenging with more complicated dc networks. For example, high frequency noise from a dc arc fault may propagate along the cable to adjacent branches and may cause mis-trigger. Therefore, the third motivation of this work is to provide a protection strategy that can localize dc arc faults in dc microgrids.

1.3 Chapter Review

Chapter 2 presents the characteristics study and modeling of a dc arc fault. A dc arc fault generating unit and testing circuit is established to acquire arc data under various conditions that emulate ratings used in many modern applications. The experimental arc data provides foundation for the rest of the dissertation. In this chapter, the relationship among basic arc parameters including arc voltage, arc current, arc length, and dc source voltage are studied. The V-I equation and Gaussian distribution model of a dc arc are then developed to describe the dc component and high frequency noise of an arc, respectively. The derived arc model is able to provide insights into fault signature study, and facilitate system level simulation study.
Chapter 3 investigates the fault signatures of dc arcs for fault detection. Arc signatures are used to represent the presence of an arc fault and to differentiate an arc fault from normal operational conditions as well as environmental noise. Computation of current change in a selected time window and discrete wavelet decomposition are applied to arc current waveforms. A time domain signature and a time-frequency domain signature are then proposed.

Chapter 4 presents a detection algorithm developed and implemented in a Digital Signal Processor (DSP) board. Strategies are applied to reduce and separate computation load by allocating most of the computation tasks in the interrupts of the DSP program to achieve reduced detection time. A parameter is introduced to customize the robustness against environmental noise based on application scenarios. The detection algorithm is then verified through multiple groups of experiments.

Chapter 5 presents arc fault detection and protection in dc microgrids or distribution systems. A generic ring type dc microgrid model with four buck converter sources and three resistive loads is applied to investigate the impact of dc arc fault within the system. Possible fault locations within a microgrid and their fault responses are analyzed and simulated. High impedance dc arc faults can cause the change of system operation points while the high frequency noise can propagate to adjacent source and load units. A system protection strategy is proposed based on the fault response pattern of each fault type.

Chapter 6 summarizes the research work in this dissertation and provides an outlook of future research topics.
Chapter 2: DC Arc Characteristics and Modeling

Based on the location with respect to the load, dc arc faults can be classified into two types: series and parallel. A series dc arc occurs when a connection is pulled apart while the circuit is on. It can be caused by intermittent connections in soldered joints, wire connections, or connectors. Series arc faults are considered to be more dangerous due to the potential for localized heating and the fact that overcurrent protection devices will not respond to fault currents below their trip rating. Thus, series arc faults will be the focus of this work.

2.1 Setup and Test Procedure

Table 2.1 summarizes the experimental conditions for dc arc tests. Experiments of the combination of five dc source voltage levels, four load current levels, and five arc lengths were carried out in order to examine their influence to arc characteristics. According to NEC 2011 article 690.11, PV systems with maximum voltage greater than 80 V should be equipped with equivalent arc fault protection. Therefore, five dc source voltage levels ranging from 75 V to 300 V are tested in order to cover the 80 V limit required by NEC and the 270 V dc voltage rating applied in aircraft applications. Moreover, the studied voltage range also covers part of the operating voltage range of EV inverters [10],[11],[17].
Table 2.1: Experimental conditions

<table>
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<tr>
<th>Electrodes material</th>
<th>Copper</th>
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<tr>
<td>Load type</td>
<td>Adjustable resistance</td>
</tr>
<tr>
<td>DC source voltage (V)</td>
<td>75, 120, 175, 240, 300</td>
</tr>
<tr>
<td>Load current (A)</td>
<td>3, 6, 15, 25</td>
</tr>
<tr>
<td>Gap length (in)</td>
<td>0.04, 0.06, 0.08, 0.10, 0.12</td>
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The selection of gap lengths studied is based on the size of possible loose connections. Gap length as small as 1 mm (0.04 in) is used to simulate the loose connections in automotive power systems [28]. Larger gap lengths can be expected on an airplane due to continuous vibration. The gap length studied is up to 0.12 in. The five gap length values studied are evenly distributed among the range (0.04 in, 0.12 in) to cover different possible loose connection lengths.

All the 100 sets of test data were acquired at room temperature and pressure. The copper electrodes used for arc generation are rod-type with a 0.252 inch diameter. Prior to each test, the surface of the electrodes was polished with sandpaper in order to remove the burns from the last arcing. In this study, the anode rod is held stationary while the cathode rod is moved apart by a stepper motor. The arc generating unit and a free burning arc are shown in Fig. 2.1.

Fig. 2.2 shows the diagram and picture of the entire experimental setup. The power supply is composed of a three phase variable transformer and a rectifier unit. The variable transformer is a Staco 6020E-6Y, with an input voltage of 480 V, an output voltage of 0-560 V, and a power rating of 67.8 kVA. The rectifier was built with three diode bridges and three parallel electrolytic capacitor groups. Each capacitor group consists of two 450 V capacitors connected in series. The load is formed by
a variable resistive load bank. In some of the tests, a boost converter is connected in parallel with the output capacitor of the rectifier. The converter can inject high frequency switching noise in order to simulate the EMI noise from power electronic circuits. In general, the source voltage, load current, gap length, and opening speed of the gap can be controlled independently.

All of the arc signals, including arc current and arc voltage, were recorded using the Yokogawa DL850V digital oscilloscope. This oscilloscope has an analog to digital conversion resolution of 16 bits and the sampling rate used for the tests was 200 kHz. The recording length was five seconds although the arc faults lasted longer. Both the onset of arc and the stable arcing were recorded.
Fig. 2.3 shows an example of a measured arc voltage trace and arc current trace. In this particular example, the dc source voltage is 80 V with a load current of 12.5 A. The load current is measured on the branch with resistive load and arc generator unit, as indicated in Fig. 2.2a. The rise of the arc voltage and the fall of the load current indicate the initiation of the arcing process. Before arcing happens, the measured current is load current which is determined by the dc source voltage and
load resistance. Once the arc happens, the load current will drop due to the insertion of arc impedance. This load current is also equal to the arc current.

Figure 2.3: Arc current and voltage traces.

In this study, the load current is adjusted by tuning the load resistance, while the arc current is not directly controlled. The actual arc current value will depend on factors including dc source voltage, gap length and load resistance. Therefore, the 4 current levels shown in Table 2.1, i.e. 3 A, 6 A, 15 A, 25 A, are referred to the load current before arcing occurs. However, the characteristic study and fault detection study will be based on the portion of the current waveform after arcing occurs, which is thus referred to as arc current. As can be seen from Fig. 2.3, the actual arc current value will be smaller than the indicated load current level.
2.2 Characteristic Study of Basic Arc Behavior

2.2.1 Arc Resistance

Fig. 2.4 shows the average arc resistance versus dc source voltage under different current levels. With the arc voltage and arc current measured, arc resistance can be calculated by dividing arc voltage with arc current at each data point. Due to the instability nature of arc phenomenon, the arc resistance will not be exactly constant as a regular resistor, and is then averaged throughout the stable burning period. Each point on the figure is obtained by averaging the arc resistance under five different gap lengths at specified load current level and dc source voltage level.

![Figure 2.4: Average arc resistance.](image)

It can be seen that the dc source voltage has a slight influence to the arc resistance. The load current has a more significant influence on the arc resistance especially when the current is low. The data point for a 75 V dc source voltage and 3 A load current is
not included in this figure since the arcing under this condition is not self-sustaining and is not comparable to the ones from steady arcing.

2.2.2 Arc Voltage

A plotting of the arc voltage versus dc source voltage is given in Fig. 2.5. In this figure, similar to the arc resistance, the arc voltage shows a stable flat trend with the increase of external dc source voltage.

![Figure 2.5: Average arc voltage.](image)

Standard deviation was applied to investigate the influence of dc source voltage and load current to the arc voltage. For each specific load current level and gap length, there are five arc voltage values obtained from five dc source voltages as specified in Table 2.1, i.e. 75 V, 120 V, 175 V, 240 V, 300 V. The standard deviation of the five arc voltage values is calculated and is represented by the error bar at each element in Fig. 2.6.
The length of the error bar shows how the arc voltage at different dc source voltages is different from each other. There are four curves corresponding to four load current levels tested. They represent the average value of the five arc voltage values. There is a clear gap between each curve which indicates a strong dependence of arc voltage to arc current. These curves show an overall trend of arc voltage increasing with larger gap length under all load current levels.

### 2.3 V-I Model of DC Arc

#### 2.3.1 Arc Modeling Methods

As a complex physical phenomenon, an equivalent arc model has been under investigation since the last century in order to better understand the arc behavior. Generally, there are two modeling approaches. The first is a numerical method using Finite Element Analysis (FEA) [29]-[30]. This approach applies a set of equations
describing the physical process of the dc arc such as the thermal dynamics and dielec-
tric properties using microscopic parameters. The typical procedure of establishing a
physical model of the dc arc takes into account the following aspects:

- Establish a set of assumptions about the arc property, to simplify the calculation
  and understanding;

- Establish a group of equations to describe the thermal plasma;

- Use Maxwell equations to describe the electromagnetic property of arcs;

- Consider the thermodynamic and transport properties of the arc based on chem-
  ical and kinetic equilibrium assumptions;

- Boundary conditions based on the geometry of the arc confinement;

- Coding with the above equations for computation.

The results of the FEA modeling provides the actual shape and size of the arc as
well as the development stages of the arc. Verification of a FEA model is conducted
by taking images of the actual arc with fast speed cameras and compare the images
with the FEA simulation results [31]-[32]. FEA involves complex computation and is
mostly adopted for understanding the physical characteristics of the arc in a micro-
scopic way. Applications of this method are to generate or control an arc for special
utilization purposes, such as dc arc torch and plasma for material processing.

The second method is an external characteristic model describing an arc with a
macroscopic equation to represent its electrical behavior [33]. This method models the
arc as a ”black box”: only the input and output electrical parameters are of interest,
such as the voltage across the arc and current through the arcing channel. This method is useful for understanding arc behavior as part of an electrical system, such as for fault detection purposes. This approach does not consider microscopic phenomena but requires large number of experiments to extract the proper V-I equation in a statistical way. In this subsection, the arc V-I equation is investigated.

2.3.2 Previous Study on DC Arc V-I Equation

The V-I equations change significantly under different arcing conditions. Factors such as current level, temperature, gap length will influence the V-I equation. Several V-I equations have been derived in previous studies, including the Ayrton equation, Steinmetz equation, Nottingham equation, Van and Warrington equation, Miller and Hildenbrand equation, and Paukerts equations, et al. A comprehensive review of these equations can be found in [33].

These equations were derived in an empirical way: summarized from a large number of experimental data. Different equations are derived from different test conditions of diverse applications, majority of which are for longer gap length or larger current compared to the test condition of this study. Table 2.2 summarizes some of the previous V-I equations and the relevant experimental conditions. The gap length and current level could influence the arc behavior greatly in the following way: for longer gap lengths, the actual arc length could be much larger than the gap length due to the convection force; while high current will make the arc more stable due to the higher temperature. Thus, it is important to specify the test conditions from which the empirical V-I equation is derived.
2.3.3 Modified Paukert V-I Equation

Among all the existing equations, the Nottingham equation covers the gap lengths of interest in this study. But in the Nottingham equation, the influence of gap length is not considered and it only shows sample current up to 10 A. The Stokes and Oppenlander equation covers the current of interest in this study but with a much larger gap length level. The current and gap length range discussed in this study are both covered by the Paukert equations. The Paukert equations provide different equations for different gap lengths without incorporating the gap length into the equation as an influencing factor.

Table 2.2: V-I equations in previous studies

<table>
<thead>
<tr>
<th>Name</th>
<th>Equation</th>
<th>Experiment conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ayrton equation</td>
<td>$V_{arc} = A + BL + \frac{C+DL}{I_{arc}}$</td>
<td>Carbon electrodes</td>
</tr>
<tr>
<td>Steinmetz equation</td>
<td>$V_{arc} = A + \frac{C(L+D)}{I_{arc}}$</td>
<td>Carbon and magnetite electrodes</td>
</tr>
<tr>
<td>Nottingham equation</td>
<td>$V_{arc} = A + \frac{B}{I_{arc}^n}$</td>
<td>$n$ is related to electrode material</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$L$: 0.039 to 0.39 in</td>
</tr>
<tr>
<td>Miller and Hildenbrand equation</td>
<td>$V_{arc} = A + \frac{B}{I_{arc}^n}$</td>
<td>$L$: 0.197 to 7.87 in</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_{arc}$: 5 to 50 kA</td>
</tr>
<tr>
<td>Paukert equation</td>
<td>$V_{arc} = \frac{a}{I_{arc}^n}$</td>
<td>$L$: 0.039 to 7.78 in</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_{arc}$: 0.3 to 100 kA</td>
</tr>
</tbody>
</table>

Based on the above discussion, the V-I equation of the Paukert form is selected to study. Moreover, considering that the arc voltage does change with gap length, as shown in the previous subsection, a model incorporating the influence of gap length is proposed based on the Paukert equation structure.
The arc voltage under different gap lengths and load current levels is shown in Table 2.3. These values are obtained by averaging the arc voltage under the five different dc source voltages. From the previous analysis of the dc source voltage impact, the influence of dc source voltage is assumed to be negligible here. Although only 20 sets of data are listed in Table 2.3, these data are extracted from 100 sets of test data.

Table 2.3: Arc voltage at different gap length and load current

<table>
<thead>
<tr>
<th></th>
<th>3 A</th>
<th>6 A</th>
<th>15 A</th>
<th>25 A</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.04 in</td>
<td>32.5600</td>
<td>27.3146</td>
<td>24.4735</td>
<td>22.8526</td>
</tr>
<tr>
<td>0.06 in</td>
<td>40.8396</td>
<td>35.6210</td>
<td>27.1918</td>
<td>24.2715</td>
</tr>
<tr>
<td>0.08 in</td>
<td>48.2458</td>
<td>40.1064</td>
<td>29.2487</td>
<td>25.6249</td>
</tr>
<tr>
<td>0.10 in</td>
<td>52.1582</td>
<td>42.0752</td>
<td>30.1503</td>
<td>28.5911</td>
</tr>
<tr>
<td>0.12 in</td>
<td>56.7833</td>
<td>42.1882</td>
<td>31.9032</td>
<td>30.6755</td>
</tr>
</tbody>
</table>

The Paukert V-I equation is of the following form:

\[ V_{arc} = \frac{a}{I_{arc}^b}, \]  

(2.1)

where \( a, b \in \mathbb{R} \). The exponential form of \( I_{arc} \) can be seen from linear interpolation of the measured V-I values in Fig. 2.7. In order to verify the dependence of \( a \) and \( b \) value on gap length, a curve fitting is applied to the arc voltage and load current under each gap length as opposed to fitting all the test data into one set of \( a \) and \( b \) values. The curve fitting results are shown in Table 2.4.

From Table 2.4, it is obvious that the values of \( a \) and \( b \) changes with the gap length level. The dependence of \( a \) and \( b \) value on gap length \( L \) can also be seen from
Fig. 2.7: the gaps between the five curves of the measured values are different. More specifically, the distance between 0.10 in and 0.12 in curves is much smaller than the distances between 0.04 in and 0.06 in curves. If only $a$ is related to $L$ as in previous equations mentioned in [33], the distances between adjacent curves would have been equal. This shows that $b$ is also related to $L$. Therefore, the following V-I equation

![V-I Plotting](image)

Table 2.4: Values of $a$ and $b$

<table>
<thead>
<tr>
<th></th>
<th>0.04 in</th>
<th>0.06 in</th>
<th>0.08 in</th>
<th>0.10 in</th>
<th>0.12 in</th>
</tr>
</thead>
<tbody>
<tr>
<td>$a$</td>
<td>38.28</td>
<td>54.30</td>
<td>67.81</td>
<td>72.66</td>
<td>78.38</td>
</tr>
<tr>
<td>$b$</td>
<td>0.1660</td>
<td>0.2496</td>
<td>0.3036</td>
<td>0.3055</td>
<td>0.3165</td>
</tr>
</tbody>
</table>
form is proposed with gap length integrated in both $a$ and $b$:

$$V_{\text{arc}} = \frac{a + cL}{I_{\text{arc}}^{b + dL}} \quad (2.2)$$

where again $a, b, c, d \in \mathbb{R}$ and $L$ represents the gap length. Through curve fitting with the experimental data, the following parameters are obtained to represent the V-I characteristics of the dc arc studied:

$$V_{\text{arc}} = \frac{20.19 + 526.2L}{I_{\text{arc}}^{0.1174+1.888L}} \quad (2.3)$$

In order to verify the accuracy of the above model, the arc voltage using (2.3) is calculated and plotted in Fig. 2.8 along with the measured values. The standard deviation of the five arc voltage values at different source voltages is calculated and is represented by the error bar with the mean value in the center. From Fig. 2.8, we can see that most of the calculated numbers correspond well with the measured numbers. The errors between calculated and average measured results are summarized in Table 2.5 where it can be seen that the largest error is about 10%.

Compared with [33], the gap length studied in this study has a much smaller range, which provides the possibility to study the influence of $L$ in smaller steps, with more details and make the equation more accurate under the specified testing condition.

The proposed equation is only meant to describe the arc V-I relationship under the tested conditions. These conditions are selected to cover most common arc fault conditions in power electronics systems with resistive loads and relatively low current amplitudes. The equation should not be used to predict V-I curve outside the tested range. As mentioned previously, the load current is used to approximate the arc current. It is important to note that this approach should not be used in systems
Figure 2.8: V-I model fitting results.

Table 2.5: Error between calculated and average measured values

<table>
<thead>
<tr>
<th></th>
<th>3 A</th>
<th>6 A</th>
<th>15 A</th>
<th>25 A</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.04 in</td>
<td>0.0246</td>
<td>0.0685</td>
<td>0.0007</td>
<td>0.0302</td>
</tr>
<tr>
<td>0.06 in</td>
<td>0.0163</td>
<td>0.0388</td>
<td>0.0192</td>
<td>0.0149</td>
</tr>
<tr>
<td>0.08 in</td>
<td>0.0387</td>
<td>0.0400</td>
<td>0.0294</td>
<td>0.0244</td>
</tr>
<tr>
<td>0.10 in</td>
<td>0.0028</td>
<td>0.0002</td>
<td>0.0539</td>
<td>0.0496</td>
</tr>
<tr>
<td>0.12 in</td>
<td>0.0058</td>
<td>0.0665</td>
<td>0.0291</td>
<td>0.1022</td>
</tr>
</tbody>
</table>

with fast varying $\text{di/dt}$. Moreover, this equation is derived with dc components of the arc voltage and arc current values. Therefore, it is not frequency-dependent.
2.4 Gaussian Distribution Model of Arc Noise

While V-I equation models the dc and slowly varying ac component, arc randomness also needs to be considered. In [34], zero-mean Gaussian noise function was used to describe the voltage fluctuation of arc, while [35] added a randomly generated value to the arc resistance equation. The rest of this subsection studies the noise in arc current more closely with quantitative analysis. The dc arcing channel is essentially a plasma discharge channel. In the plasma, the coulomb collision, where two charged particles interact through their own electric field, is common. The Coulomb collision effects are random in character and diffusive, which leads to a Gaussian probability distribution of the velocity about the average particle speed [36]. Since electric currents in plasma are flows of electrons, it is expected that the current also follows a Gaussian probability distribution.

Fig. 2.9 shows the Gaussian (Normal) distribution fitting of filtered arc current using a 1.5 kHz - 45 kHz bandpass filter. Fig. 2.9a represents the probability density function of filtered arc current with its Gaussian distribution curve, showing good agreement. The fitted Normal distribution function is given by:

\[ f_x = \frac{1}{\sigma \sqrt{2\pi}} e^{-\frac{(x-\mu)^2}{2\sigma^2}} \]  \hspace{1cm} (2.4)

where \( \mu \) is the mean value and \( \sigma \) is the standard deviation. For a zero-mean Gaussian distribution, \( \mu \) equals to zero. However, the Gaussian distribution curves shown in Fig. 2.9 show a small negative dc offset of around 0.05 A. This offset is caused by the design of the active bandpass filter.

As Fig. 2.9a is an example of 15 A arc current, Fig. 2.9b shows the Normal distribution fitting for all four different current levels: 3A, 6 A, 15 A, and 25 A. It
shows a clear quantitative relationship between the current level and $\sigma$. The comparison of current with and without arcing is presented in Fig. 2.9c. The noise from current without arcing data is mainly from the measurement noise and can also be described with a Gaussian distribution with a much smaller standard deviation. The measurement noise can be from background noise, current ripples from the rectifier, as well as the oscilloscope noise.

Even though this preliminary fitting has identified the relationship between the arc noise and dc current level, more accurate fitting is also needed. In order to do that, smaller current steps, e.g. 2 A, should be applied. Only with that, a more thorough and accurate equation can be obtained.

2.5 Summary

In this chapter, the characteristics of dc arcing are studied revealing the relationships among important arc parameters. From the characteristic study, dc arc models are derived. The dc arc models consist of both the dc high impedance component and high frequency noise component. The derived arc models can facilitate system level simulation study. For example, this arc model will be used in Chapter 5 to study the impact of dc arc fault to a dc microgrid.
Figure 2.9: Gaussian distribution fittings.

(a) Probability density function and normal fitting.

(b) Gaussian distribution fitting of different arc current levels.

(c) Comparison of arc current and before arcing current.
Chapter 3: DC Arc Fault Signatures

Proper signature selection is important for successful detection of the dc arc. Signatures should be able to represent the fault characteristics, as well as to differentiate faults from normal operating conditions (e.g. load changes) and ambient noise. Arc fault signatures from time domain and time-frequency domain are presented in this chapter.

3.1 Time Domain Based Current Variation Analysis

The physical processes of the dc arc are both chaotic and dynamic. The arc current and arc impedance waveforms are consistently changing, influenced by the evaporation and combustion process of the electrode material and the magnetic field generated by the arc current itself [37]. The chaotic characteristics of the dc arc current are reflected by the pulsed pattern of the current waveform: the current amplitude changes dramatically in a short period. Researchers have been looking into the chaotic characteristics of dc arc with comparatively complex computational procedures for fault detection purposes [19]. In this section, a simple yet effective method, realizable with low-cost detectors, is proposed utilizing the chaotic characteristic of the dc arc.
First, a proper time window $T_{sw}$ is selected. The maximum and minimum current amplitude, $I_{\text{max}}$ and $I_{\text{min}}$, within each $T_{sw}$ is identified. The current difference is then computed by:

$$I_{\text{dif}} = |I_{\text{max}} - I_{\text{min}}|. \quad (3.1)$$

The time window length selected could influence the $I_{\text{dif}}$ waveform pattern. For example, Fig. 3.1 shows the $I_{\text{dif}}$ waveform obtained with different time window lengths: 1 ms, 5 ms, 25 ms, and 125 ms. These current variance waveforms are calculated from the arc current trace shown in Fig. 2.3 ($V_{dc} = 80$ V and $I_{\text{load}} = 12.5$ A).

It can be seen that with $T_{sw} = 5$ ms and $T_{sw} = 25$ ms, there is a significant difference between the no-arcing stage and stable arcing stage. With $T_{sw} = 1$ ms, the difference between the arcing and no-arcing condition is relatively subtle, which means that 1 ms is too short to include enough current randomness in one single time window. It can also be seen that with $T_{sw} = 125$ ms the difference between arcing and no-arcing is still noticeable but is not improved compared with $T_{sw} = 5$ ms and $T_{sw} = 25$ ms. In addition, it will take 125 ms to obtain the $I_{\text{dif}}$ value for one time window, which implies a much slower detection process. Therefore, a $T_{sw}$ value between 5 ms and 25 ms is considered appropriate since it is long enough to represent current randomness appropriately with fast detection time guaranteed.

Several trials are needed before obtaining an appropriate $T_{sw}$ value. In this study, $T_{sw}$ starts from 1 ms which involves 200 data points, and is increased by a factor of five each time until the time window is too long for a fast detection. In this way, a range within which the $I_{\text{dif}}$ value shows a significant change after arc happens can be obtained. Different $T_{sw}$ values among the range have been used throughout the study, i.e., $T_{sw} = 10$ ms is used in Chapter 3 for wavelet analysis, while in Chapter
Figure 3.1: $I_{df}$ waveform with different time window length.
4, $T_{sw} = 25$ ms is used in the detection algorithm. It is important to notice that the choice of $T_{sw}$ is not unique as long as it is in the proper range.

From $I_{\text{dif}}$ waveform with $T_{sw} = 5$ ms and $T_{sw} = 25$ ms, three different patterns can be seen corresponding to three different arcing stages. Before the arc happens, a background noise of around 0.4 A is observed from $I_{\text{dif}}$. This background noise is caused by the ripple of the dc voltage generated by the rectifier and is not related to the arc characteristics. When the arc starts, a large $I_{\text{dif}}$ is produced by the current drop, which could be a signature of a dc arc but would require proper discrimination from the normal current change caused by load transients and switching operations [14]. During the arc developing stage, when the electrode is moving, $I_{\text{dif}}$ is low and smooth. When the electrode stopped moving, the current variation pattern shows that the self-sustained arc has high $I_{\text{dif}}$ values. The amplitude of the current variation can reach 1 A. One possible explanation of this phenomenon could be the motion of cathode spots [37]. The cathode spots show higher mobility when the arc is continuously burning. These repeating yet unique large $I_{\text{dif}}$ pulses can be used to indicate the occurrence of an arc fault. Therefore, $I_{\text{dif}}$ is chosen as one signature of dc arc fault.

### 3.2 Background on Time-Frequency Analysis

In this section, different frequency domain and time-frequency domain techniques are discussed. The advantages of Discrete Wavelet Transform (DWT) and Wavelet Packet Decomposition (WPD) for arc fault detection purpose will be presented. The Matlab m.file code used to generate the waveforms in this section is included as Appendix A.
3.2.1 Limitations of Fourier Analysis

Consider a uniformly sampled signal $x[n]$ with $n = 0, 1, ..., N - 1$, then its $N$ point Discrete Fourier Transform (DFT) is given by:

$$
\hat{x}[k] = \sum_{n=0}^{N-1} x[n] e^{-j\frac{2\pi}{N}kn} \text{ for } k = 0, 1, ..., N - 1 \tag{3.2}
$$

It gives an approximation to the Fourier series coefficients, $\hat{x}[k]$, of basis elements $e^{j2\pi \frac{k}{N}t}$ at equally spaced frequencies. Thus, the DFT gives a good representation of the frequency components of a signal. For example, consider the signal shown in Fig. 3.2a, this waveform is composed of a sinusoid:

$$
x_r[n] = 0.7 \sin(2\pi 100nT_s), \ n = 0, 1, ..., 2000 \tag{3.3}
$$

with a frequency of 100 Hz and a noise of 1000 Hz frequency as follows:

$$
x_w[n] = \begin{cases} 
0 & \text{if } n < 701 \text{ or } n > 1301 \\
0.1 \sin(2\pi 1000nT_s) & \text{otherwise}
\end{cases}, \tag{3.4}
$$

i.e. $x[n] = x_r[n] + x_w[n], T_s = 100 \mu s$.

Analyzing the DFT of this signal shown in Fig. 3.2b, we can see the two frequencies, 100 and 1000 Hz. However, the DFT does not give any information on when these frequencies appeared in time. If we consider the noise as an indication of a fault in a system, it is clear from Fig. 3.2a that the fault appears at $t = 0.7$ s. However, if only the DFT of this signal is analyzed, it is not possible to know at what time the fault occurred. This is a drawback of using DFT for fault detection.

In addition, there are $N^2$ operations needed to compute an $N$ point DFT (note: Fast Fourier Transform (FFT) uses approximately $\frac{N^2}{2} \log_2 N$ computations) which can be very computationally intensive. Lastly, if the frequencies of interests are in the low frequency range, it is necessary to store a larger amount of points, $N$, to view this
frequency in $\hat{x}[k]$, which increases the number of computations and detection time. Therefore, DFT can obtain excellent frequency components of the signal $x[n]$ but has poor time resolution.

### 3.2.2 Short Time Fourier Transform

It is therefore important to consider a joint time-frequency analysis of a signal to detect changes in both frequency and time domain. A different basis function is desired which can obtain good time and frequency resolution. The Short Time Fourier Transform (STFT) provides a first step towards this goal:

$$X(\tau, \omega) = \int_{-\infty}^{\infty} x(t)w(t - \tau)e^{-j\omega t}dt$$

(3.5)

where the basis function in this case is $b(t) = w(t - \tau)e^{j\omega t}$ and $w(t - \tau)$ is a “window” (e.g. Hamming, Kaiser, Hann, etc.) with the role of localizing the signal at a certain time $\tau$. Therefore, this basis function $b(t)$ gives a good description of the signal $x(t)$ in
both time and frequency domains. The traditional procedure to compute the STFT is:

1. Split the signal \( x[n] \) into blocks of equal length;

2. Overlap the blocks by a certain percentage;

3. Multiply each block by a window function \( w[m] \);

4. Calculate the DFT of each block.

As an example, the STFT of the signal in Fig. 3.2a is shown in Fig. 3.3a.

We can see that the noise/fault, \( x_w[n] \), appears well represented in frequency at around \( t = 0.7 \) s. However, one drawback of STFT is that as we increase the time resolution, i.e. the number of blocks, the frequency resolution decreases as shown in Fig. 3.3b and vice versa in Fig. 3.3c. Ideally we would like to have the temporal width, \( \Delta_t \), and the spectral width, \( \Delta_f \), of the basis function as small as possible. However, these must satisfy the “uncertainty principle” [40]:

\[
\Delta_t \Delta_f \geq \frac{1}{4\pi}, \quad \text{where}
\]

\[
\Delta_t = \sqrt{\frac{1}{E} \int_{-\infty}^{\infty} t |b(t)|^2 dt} \quad (3.7)
\]

\[
\Delta_f = \sqrt{\frac{1}{E} \int_{-\infty}^{\infty} f |B(2\pi f)|^2 df} \quad (3.8)
\]

where \( B(2\pi f) = \int_{-\infty}^{\infty} b(t) e^{-j2\pi ft} dt \) and \( E = \int_{-\infty}^{\infty} |b(t)|^2 dt = \int_{-\infty}^{\infty} |B(2\pi f)|^2 df \). Equation (3.6) implies that in order to satisfy this inequality, there is always a trade-off between time and frequency resolution as we see in Fig. 3.3.
3.2.3 Wavelet Analysis

One way to improve the drawbacks of STFT is to consider a family of basis functions with different temporal and spectral widths, in contrary to fixed widths. The reason for this is that at lower frequencies, it is desired to have a longer time window whereas at higher frequencies a smaller time window is sufficient. To accomplish this,
we can consider the Continuous Wavelet Transform (CWT) of a signal \( x(t) \) as follows:

\[
X_{\text{cwt}}(a, \tau) = \int_{-\infty}^{\infty} x(t) \psi_{a,\tau}^*(t) dt
\]  
(3.9)

where the basis functions satisfy:

\[
\psi_{a,t} = \frac{1}{\sqrt{|a|}} \psi \left( \frac{t - \tau}{a} \right), \quad a, \tau \in \mathbb{R}
\]  
(3.10)

and \( \psi(t) \) is known as the “mother wavelet.” The term \( a \) scales the wavelet and \( \tau \) shifts it in time. In addition \( ||\psi_{a,\tau}|| = 1 \) \( \forall a, \tau \in \mathbb{R} \). These shifts in scales and time achieve the desired variable windows. Fig. 3.4 shows a few examples of mother wavelet functions.

The selection of wavelet is decided by the characteristics of the signal and the nature of applications [38]. In other words, the chosen mother wavelet should match the shape of the features in the signal. It has been concluded in [39] that db4 and coiflet were equally suitable in detecting power system transients. Another factor considered in selecting the mother wavelet in this study is the number of coefficients. Different wavelets have different number of coefficients and a higher number of coefficients means higher computation load in real applications. Therefore, a mother wavelet with less coefficients is desired in the hardware implementation.

An interesting point to take into account is that the CWT function \( X_{\text{cwt}}(a, \tau) \) is now dependent on scales (can be mapped to frequency) and time. Using the example signal in Fig. 3.2a, the CWT result is shown in Fig. 3.5. The large yellow area represents the 100 Hz main signal, while the small light blue area represents the 1000 Hz noise. The y-axis \( \text{Scales} \) is a nonlinear function of frequency. This explains why the main signal is much wider in the y-axis compared to that in Fig. 3.3. The 1000 Hz noise is also clearly visible.
Hz noise signal has clear edges in both time and scales which means that the noise is well detected in both time and frequency.

In order to implement the wavelet transform, we must consider its discrete version, namely, the Discrete Wavelet Transform (DWT). DWT is a multi-resolution analysis which states that any signal in the space of square integral functions, i.e. $x(t) \in L_2$ or $\int_{-\infty}^{\infty} |x(t)|^2 dt < \infty$, can be written as a linear combination of a countable orthonormal
basis:

\[ x(t) = \sum_{k=-\infty}^{\infty} \sum_{n=-\infty}^{\infty} d_{k,n} \psi_{k,n}(t), \quad (3.11) \]

where \( \psi_{k,n}(t) \in \mathcal{L}_2 \) and \( k, n \in \mathbb{Z} \). The index \( k \) represents stretches and \( n \) represents shifts of the mother wavelet \( \psi \). The coefficients, \( d_{k,n} \), describe the signal of interest in the \( k^{th} \) level with respect to the wavelet used. Due to the orthonormality of the basis, the coefficients can be obtained as:

\[ d_{k,n} = \langle x(t), \psi_{k,n} \rangle = \int_{-\infty}^{\infty} x(t) \psi_{k,n}^*(t) dt \quad (3.12) \]

A different way to compute the coefficients \( d_{k,n} \) is necessary for its implementation of a discrete signal \( x[n] \). Consider another basis function \( \phi(t) \) (scaling function) used
to prove (3.11) [40]. This scaling function is also stretched and shifted as follows:

\[
\phi_{k,n}(t) = 2^{-k} \phi(2^{-k}t - n)
\]  

(3.13)

This function can be used to create spaces \(V_k = \text{span} \{ \phi_{k,n} \, \forall n \in \mathbb{Z} \} \) where \(V_k \subset V_{k-1} \) for all \(k \in \mathbb{Z} \). It is also possible to find an orthogonal complement \(W_k \) such that \(V_{k-1} = V_k \oplus W_k \), where \(W_k = \text{span} \{ \psi_{k,n} \, \forall n \in \mathbb{Z} \} \). These spaces are shown in Fig. 3.6. Note that since \(V_k \subset V_{k-1} \) and \(W_k \subset V_{k-1} \), then the basis functions for both \(V_k \) and \(W_k \) can be written as a linear combination of the basis elements of \(V_{k-1} \). For example for \(k = 1 \):

\[
\phi_{1,0}(t) = \sum_{n=-\infty}^{\infty} \tilde{h}[n] \phi_{0,n} = \sum_{n=-\infty}^{\infty} \tilde{h}[n] \phi(t - n)
\]

(3.14)

\[
\psi_{1,0}(t) = \sum_{n=-\infty}^{\infty} \tilde{g}[n] \phi_{0,n} = \sum_{n=-\infty}^{\infty} \tilde{g}[n] \phi(t - n)
\]

(3.15)

for some coefficients \(\tilde{h}[n]\) and \(\tilde{g}[n]\) which represent low and high pass filters respectively [40]. These filters become fundamental in finding the representation of a signal at any particular level, for example:

\[
x(t) \approx \sum_n c_0[n] \phi_{0,n}(t) \triangleq x_0(t), \quad \text{where } c_0[n] = \langle x(t), \phi_{0,n}(t) \rangle
\]

(3.16)
This signal can be further decomposed as:

\[ x_0(t) = \sum_{n \in V_1} c_1[n] \phi_{1,n}(t) + \sum_{n \in W_1} d_1[n] \psi_{1,n}(t) \]  

(3.17)

where the coefficients can be computed using the filtering and downsampling by 2:

\[ c_1[n] = \langle x_0(t), \phi_{1,n}(t) \rangle = \sum_m c_0[m] \tilde{h}[m - 2n] \]  

(3.18)

\[ d_1[n] = \langle x_0(t), \psi_{1,n}(t) \rangle = \sum_m c_0[m] \tilde{g}[m - 2n] \]  

(3.19)

Define the decomposition low pass and high pass filters as \( h[n] = \tilde{h}[-n] \) and \( g[n] = \tilde{g}[-n] \), then we can consider the DWT and in general a Wavelet Packet Decomposition (WPD) as shown in Fig. 3.7.

![Wavelet Packet Decomposition and Spectrum](image)

Figure 3.7: Two level wavelet packet decomposition and spectrum.
By passing the signal \( x(t) \) through these filters a type of filterbank analysis is formed, which gives the representation of the signal in different frequency ranges \([41, 42]\). Using the same signal in Fig. 3.2a, the DWT coefficients of interests are computed as shown in Fig. 3.8. It can be seen that by using \( d_3 \), it is possible to detect the noise/fault.

### 3.3 Time-Frequency Analysis of DC Arc

Two types of series dc arc current will serve as models for the time-frequency analysis presented: a waveform containing a noise generated by a 20 kHz nearby power electronics converter and another is a current waveform without intentionally added noise. To induce the 20 kHz switching noise, a boost converter is connected in parallel with the arc generator branch, as shown in Fig. 1(b). The current was measured at the main dc bus so it contains both arc current and boost converter input current. In this case, the current ripple of the boost converter was set at around 0.5 A peak to peak. The current on the main dc bus was tuned to be 30 A with around 25 A arc current in it. In order to analyze the frequency characteristics of the current, only the ac components of the current were recorded through a 1.5 kHz - 45 kHz band pass filter. The waveforms are shown in Fig. 3.9 (20 kHz noise) and Fig. 3.10 along with a spectrogram for the highlighted section of the signal.

From the spectrogram representation of these signals in the designated section, it is possible to see how during the arc, an amplitude increase in all frequencies occurred due to the randomness and variation of arc current. This is the main reason why WPD can be used to detect this increase in energy in the dc arc current. Moreover, the 20 kHz switching frequency noise can be easily separated and recognized from the
(a) Three level DWT tree (only the red squares need to be computed).

(b) Raw coefficients $d_3$ and $c_3$.

Figure 3.8: DWT of signal $x[n]$ in Fig. 3.2a.

frequency spectrogram to reduce its influence to dc arc fault detection. The strong energy from 40 kHz harmonic noise can also be easily identified.
The WPD procedure begins by dividing the current $x(t)$ into time windows $T_{sw} = 10$ ms for a sampling frequency $f_s = 200$ kHz, i.e.

$$x_i(t) = \begin{cases} x(t) & \text{for } (i-1)T_{sw} \leq t < iT_{sw} \\ 0 & \text{otherwise} \end{cases}$$

(3.20)

where $i \in \mathbb{N}$. The sampled signal within each time window is then passed through a WPD (level 2) using Daubechies or Coiflet wavelets. The highest frequency component achievable is half the sampling frequency, and at each level of WPD, the frequency band is divided into two, as shown in Fig. 3.7. In total four frequency bands can be achieved with a two level WPD: [0 25] kHz, [25 50] kHz, [50 75] kHz, and [75 100] kHz.
The RMS value at each terminal node \( j \in \{0, 1, ..., 3\} \) for the \( i^{th} \) window is calculated as follows:

\[
ed_{j,i} = \left( \frac{1}{N} \sum_{n=1}^{N} c_{j,n}^2 \right)^{\frac{1}{2}}.
\]  
(3.21)

For example, \( e_{1,1} \) corresponds to the RMS value of the signal \( x_1(t) \) at the frequency range [25 50] kHz in the 1st time window, i.e. \( t_1 \in [0 10) \) ms. Fig. 3.11 shows the RMS calculation result of the current before and after arcing in the frequency band [25 50] kHz for a 6 A load current and 75 V input voltage. The frequency band [25 50] kHz is selected as the arc signature to study because it is the first frequency band without dc components. There are 500 time windows within 5 s for \( T_{sw} = 10 \) ms. From Fig. 3.11, it can be seen that after the arc occurs, the RMS value boosts obviously which makes it an appropriate signature for dc arc detection.
Figure 3.11: Time-frequency analysis for $V_{in} = 75$ V, $I = 6$ A.

Figure 3.12: Time-frequency analysis for $V_{in} = 300$ V, $I = 25$ A.
However, a different scenario is observed when the circuit is operating under 25 A. Fig. 3.12 shows the RMS calculation result of the arc current and normal current under 25 A load current and 300 V source voltage. Different from low power arc, there is no obvious change of RMS value before and after arc happens. To overcome this problem, the RMS value of frequency band [25, 50] kHz is normalized by the lowest frequency band [0, 25] kHz which includes the dc component. Both the RMS values for frequency band [0, 25] kHz and [25, 50] kHz will be computed and then the normalized RMS value can be achieved by dividing the RMS value of frequency band [25, 50] kHz with the RMS value of frequency band [0, 25] kHz.

The normalized result is shown in Fig. 3.13. The upper plotting of Fig. 3.13 is the RMS value, same as the one in Fig. 3.12. With the added contour line, it can be seen that there is a 6% increase in the RMS value after arcing. The bottom plotting shows the normalized RMS waveform. After normalization, the peak value increased 15%. Thus the performance of RMS as signature can be significantly improved by normalization. For this reason, the normalized RMS value is applied as arc signature for the detection algorithm.

The effectiveness of this signature may be limited in applications with broad spectrum of ambient noise and ambient noise with changing amplitude, which is a common challenge for many detection techniques. Additional strategies are required to differentiate ambient noise with broad spectrum/changing amplitude from a dc arc fault. One possible way is to conduct a noise testing program by testing the noise sources under all possible operational conditions. Taking the aircraft application as an example, noise testing should be conducted with and without the engine running, and with and without other pieces of equipment running. The ambient noise for different
applications may be different. Therefore, the noise testing should be conducted for each different application. This can be a time-consuming process but is necessary for accurate arc fault detection, especially for applications that are known to have ambient noise with broad spectrum/changing amplitude. The recorded noise can then be compared with the arcing noise, to identify possible frequency bands for the arc fault detector to avoid the influence from the ambient noise. Some other features or signatures may be found based on the differentiation of the ambient noise and the arc noise.

3.4 Summary

This chapter presents two signatures for dc arc fault: one is from time domain analysis $I_{dif}$, the other is from DWT (time-frequency domain) $RMS_{norm}$. Various
techniques for frequency domain analysis are discussed to show the advantages of time-frequency domain analysis. The time-frequency domain signature requires more computation than the time domain signature, but is more effective for fault detection purposes. The two signatures will be applied in the detection algorithm in Chapter 4.
Chapter 4: Detection Algorithm and Experimental Verification

4.1 Detection Algorithm

Based on the two arc signatures discussed in the previous chapter, a detection algorithm is proposed and a floating point DSP board TMS320F28335 from Texas Instruments is used for the implementation of the algorithm. It has a clock frequency of up to 150 MHz and is recently gaining popularity in power electronics applications. The flow chart of the DSP interrupt and main function is shown in Figs. 4.1-4.2. The DSP code is provided in Appendix B.

As can be seen from Fig. 4.1, whenever a new data comes, $I_{\text{max}}$ and $I_{\text{min}}$ are updated at each timer cycle and $I_{\text{dif}}$ is obtained by implementing $I_{\text{dif}} = I_{\text{max}} - I_{\text{min}}$ at the $n^{th}$ cycle. The actual value of $n$ depends on the time window length and sampling frequency. For example, $n = 5000$ corresponds to 25 ms when the sampling frequency is 200 kHz. A longer time window will make the RMS vs. Time waveform smoother and can enhance detection accuracy while an over long time window leads to longer response time. Also, when the number of data points is too much, the actual implementation has to be optimized to make sure the calculation load is reasonable for the available microprocessor.
The wavelet coefficients are essentially computed by passing a signal through low pass and high pass filters, along with down-sampling by 2, as discussed in Section 3.2.3. The filters make sure that the information of the original signal is not lost from the down-sampling and the original signal can be perfectly reconstructed from the coefficients by implementing the inverse DWT [40]. The filters depend on the wavelet being used and are the same throughout the whole decomposition of all

Figure 4.1: Flow chart of DSP implementation of the proposed detection algorithm: Interrupt.
levels. Therefore, by implementing convolution and down-sampling, it is possible to realize the detection algorithm on a microprocessor in time domain.

As can be seen from the flow chart of the interrupt function in Fig. 4.1, the filtering process for the 1st level DWT to obtain Coefl1 is conducted every two timer periods for which two new data points are ready at this time. Whenever two new coefficients from the 1st level DWT are obtained, the 2nd level DWT coefficients
(Coefl2 and Coefh2) are then computed. This theoretically derived down-sampling by 2 approach automatically reduces the computation load by half than if the filtering process was done every timer period instead. This is an extra advantage of using DWT for the dc arc fault detection.

A summary of the computation flow shown in Fig. 4.1 is given here. During each timer period (the \( j^{th} \) timer period, \( j \in \{1, \ldots, 5000\} \)), \( I_{\text{max}} \) and \( I_{\text{min}} \) are updated. At every other timer period (the \( 2j^{th} \) timer period, \( j \in \{1, \ldots, 2500\} \)), the 1\(^{st}\) level DWT coefficients are computed. At every fourth timer period (the \( 4j^{th} \) timer period, \( j \in \{1, \ldots, 1250\} \)), the 2\(^{nd}\) level DWT coefficients are computed, followed by the update of \( \text{Coefl2\_sum} \) and \( \text{Coefh2\_sum} \). \( \text{Coefl2\_sum} \) and \( \text{Coefh2\_sum} \) are the square summations of all coefficients available so far from the frequency bands of [0 25] kHz and [25 50] kHz, respectively, divided by 1250. The value 1250 is the total number of the 2\(^{nd}\) level coefficients in one time window \( T_{sw} \) for each frequency band. At the last timer period of every \( T_{sw} \), i.e. the 5000\(^{th}\) timer period, \( I_{\text{diff}} \) is computed and \( \text{Coefl2\_sum} \) and \( \text{Coefh2\_sum} \) values are final. After that, \( \text{Flag} \) is set to 1, and the program goes to the main function.

The final decision is made in the main function. The major computation conducted in the main function is the ”square root” of \( \text{Coefl2\_sum} \) and \( \text{Coefh2\_sum} \), which is the sum of squares of \( \text{Coefl2} \) and \( \text{Coefh2} \), normalized by the number of original data points, with which \( RMS_{\text{norm}} \) can be computed. Only when both \( I_{\text{diff}} \) and \( RMS_{\text{norm}} \) exceed the corresponding threshold value \( I_{\text{th}} \) and \( R_{\text{th}} \) will \( k \) increase by 1, which indicates one arcing event.

In general there are two ways to set the threshold value. The first one, which is also the one applied in this study, is to make a look up table based on experimental
data of test conditions interested. With the 100 data sets, the $I_{dif}$ and $RMS_{norm}$ before and after arc at each dc voltage level and load current level are calculated. It is found out that the $I_{dif}$ and $RMS_{norm}$ after arcing are generally around 1.3 times that before arcing occurs. Therefore the threshold values are set as 1.2 to 1.4 times the average value before arcing. This method requires experimental data from the actual application where the detector will be installed.

The other way to set the threshold value is to record background noise and update the threshold value in a real time manner. This method eliminates the need to conduct lots of experiments beforehand to form the look up table. Instead, the background signal without arcing fault will be recorded and updated by the detector and the new incoming data is compared with the recorded background data to determine an arcing fault. It is noteworthy that the threshold value depends on the current level and source voltage level, therefore it should be updated with the change of current level. In this way, if the background signal without arcing can be monitored and the threshold value can be calculated in real time based on the current signal without arcing, it will reduce significant efforts in changing threshold value manually. However, strategies are needed to differentiate an arcing event from the dynamics in load current and varying ambient noise. It is important to make sure that the detector does not mistaken an arc fault as load current dynamics or ambient noise, and that it does not simply update the threshold values rather than detecting the arc event.

The parameter $k_0$ is a selected value that represents the number of windows required for detection. The actual value can be tuned depending on applications. Alert
will be given after \( k_0 \) successive arcing events are detected. Since normal operations such as load change, ambient noise will also cause a high spike in the \( I_{diff} \) and \( RMS_{norm} \) waveforms, \( k_0 \) could be set at higher than 1 to reduce nuisance tripping.

It can be seen that most of the computation is allocated into the interrupt and only the final detection decision is made in the main function. The computation load for each timer interrupt is not the same because of the fact that DWT coefficients are calculated with every two data points. The heaviest computation happens at the last timer interrupt of each time window \( T_{sw} = 25 \text{ ms} \). The computation includes: \( Coefl1, Coefl2, Coefh2, Coefl2_{sum}, Coefh2_{sum}, \) and \( I_{diff} \). Since the low and high pass filter of db4 wavelet are 8 orders, the low and high pass filters \( h[n] \) and \( g[n] \) have 8 coefficients each. Thus, \( Coefl1, Coefl2 \) and \( Coefh2 \) takes 8 multiplications and 7 additions each. \( Coefl2_{sum} \) and \( Coefh2_{sum} \) needs 2 multiplications and 1 addition each, \( I_{diff} \) takes 1 addition. In total, the timer period has 28 multiplications and 24 additions. These computations can be finished within one timer period. For the main function, only 2 square roots, 1 division, 2 comparisons are operated, as shown in Fig. 4.2, which in total takes 80 clock cycles according to the benchmarks of C28x floating point unit fast RTS library. With the 150 MHz clock frequency, the computation time of the main function at the end of each \( T_{sw} = 25 \text{ ms} \) is less than 1 \( \mu \text{s} \), which is negligible. Therefore, the detection time is mainly depending on the time window length.

At the worst case when the arc fault happens at the beginning of some time window, the detection time can be represented as: \( T_{detect} = k_0 T_{sw} \). At applications where detection time is critical, the time window length can be reduced to as low as 5 ms based on previous discussions with Fig. 3.1.
The UL 1699B requirement is used in the following as a reference to justify the
detection time, although this dissertation is not dedicated for PV applications. The
fault clearance time requirement of UL1699B is \( T_{\text{clear}} \leq \frac{750 (\text{Joules})}{V_{\text{arc}}I_{\text{arc}}} \). From Fig.
2.8, the highest \( V_{\text{arc}}I_{\text{arc}} \) in this study occurs at 0.12 in gap length and 25 A load
current. Therefore \( T_{\text{clear}} \) is required to be less than 0.9 s, which is much larger than
the detection time achieved with the proposed detection algorithm. In other words,
the detection time can meet the UL1699B requirement with significant margins for
the circuit breaker to clear the fault within \( T_{\text{clear}} \).

4.2 Experimental Verification

Experiments were conducted to verify the detection algorithm. The experimental
setup is the same as shown in Fig. 2.2. The load current/arc current was measured
using a TCP 300A sensor, at 5A/V scale. During the experiments, the dc source
voltage was adjusted at 125 V and the load current was set at around 10 A by
adjusting the resistive load banks. Besides the arcing fault condition, where the
detection algorithm is designed to alert, load change conditions were also simulated
by switching the load bank resistors manually with dc source voltage applied, to test
whether it affects the detection.

4.2.1 Experimental Results with \( k_o = 1 \)

Fig. 4.3 shows the arcing experiment results. The arc is initiated at \( t_{11} \) where a
sudden drop of load current can be observed and the detection gives the arcing alert
at time \( t_{12} \). The length between \( t_{11} \) and \( t_{12} \) is about 25 ms, which means that the
software is able to give alert within the 1\(^{st}\) time window after arc is initiated.
Fig. 4.4 shows the experiment results of a small load change. The load resistance was changed at time $t_{13}$ where a sudden drop of load current can be seen. This load change never tripped the software.

Another load change test was conducted with one more resistor switched in with dc source voltage on. In this way, the load changed more than the earlier load change test. The test results are shown in Fig. 4.5. At time $t_{14}$, one resistor is switched in and the software is not tripped. At time $t_{15}$, another resistor is switched in and at time $t_{16}$, the software is tripped. The time length between $t_{15}$ and $t_{16}$ is around 25 ms. This set of experiment shows that with $k_0 = 1$, the software is immune from a small load change, but when the load change is larger, nuisance tripping will happen. To prevent nuisance tripping, a higher value of $k_0$ is necessary.

Figure 4.3: Arc event test with $k_0 = 1$
4.2.2 Experimental Results with $k_0 = 4$

While the transient of normal operations such as load changes will induce normalized RMS and $I_{dif}$ value as high as to be enough to both exceed the threshold
values in one time window. After the transient passed, the normalized RMS and $I_{\text{diff}}$ value are expected to go back to normal again. Therefore, by increasing the value of $k_0$, which means multiple consecutive time windows have to observe normalized RMS and $I_{\text{diff}}$ value to be larger than threshold values for the detection algorithm to trip the alarm, false tripping can be eliminated or reduced. The performance of the proposed detection algorithm is then investigated by experiments with $k_0$ value larger than 1. In this case, $k_0 = 4$ is chosen in an arbitrary way so that each round of computation can finish in about 0.1 s.

The arcing experiment results are shown in Fig. 4.6. At time $t_{21}$, the arc is initiated where a sudden dip of load current due to the high impedance of arc fault can be observed. The detection algorithm gives the arcing alert at time $t_{22}$. There is about 100 ms time length between $t_{21}$ and $t_{22}$, which shows that the software is able to give an alert in the 4th time window after the arc initiation. Fig. 4.7 shows the load change experiment results. The load resistance was changed at time $t_{23}$ where a sudden drop of load current can also be seen. This load change never tripped the detection software which can be seen from the always zero DSP detection signal. This set of experiments verifies that with $k_0 > 1$, the detection algorithm is able to detect arcing successfully while preventing nuisance trips from load change operation.

The selection of $k_0$ value is a trade-off between the detection time requirement and the robustness against false trip. High power applications usually involve higher current where the series arc fault current would be high. Thus the arc power is in general expected to be higher than that in low power circuits. In this case, a smaller $k_0$ value is recommended to ensure a fast detection, at the cost of a higher false trip rate. While in low power applications which are more vulnerable to environment
noise and the detection time requirement is less stringent, a higher $k_0$ value should be used to prevent frequent false trip.

Figure 4.6: Arc event test with $k_0 = 4$

Figure 4.7: Large step load change test with $k_0 = 4$
4.2.3 Verification of Detection during Stable Arcing

In all the above tests, the detection algorithm responds as soon as the arcing starts, when the electrodes are still moving and the arcing is not totally stabilized yet. To further verify the detection effectiveness with a stabilized arc fault, a third set of experiments is conducted. This time, the detection algorithm is disabled in the beginning when the electrode is still moving, until the electrode stops and the arcing becomes stabilized. This experiment simulates a possible practical situation when the detector is reset manually while an arcing fault is still on. The test results are shown in Fig. 4.8. The arcing current in this test is around 7 A.

![Detection during stable arcing](image)

Figure 4.8: Detection during stable arcing

The arcing event starts at time $t_{31}$. After that, the electrode is still moving and the detection algorithm is controlled off. After time $t_{32}$, the electrode has stopped.
which can be seen from the constant arc current. Then the detection algorithm is enabled manually. The green detection disabling signal from DSP goes from high potential to low potential, as shown in Fig. 4.8. At time $t_{33}$ the detection algorithm is able to give a fault alert, shown by the yellow DSP detection signal, which goes from low to high potential at $t_{33}$. The time length between $t_{32}$ and $t_{33}$ is less than 50 ms. This result shows that the detection algorithm is effective not only when the arc fault just starts but also when the arcing is burning stably.

4.2.4 Detection Accuracy Analysis with Arc Current Data

In this subsection, the detection accuracy of the proposed algorithm is studied with the 100 data sets of arc current. The detection accuracy is shown in Table 4.1. For each voltage and current combination there are five data sets tested corresponding to the five gap lengths. It can be seen that with 15 A or lower load current levels, the detection accuracy can reach 100 %.

However, detection failures tend to happen at 25 A with dc source voltage at 240 V and 300 V. It is found out that the measured arc current becomes very stable at high current level, which makes the time-frequency and time domain signatures less effective. A possible cause could be the current probe used for the arc tests in this study, which is a Tektronix TCP 300. This current probe has a typical 1 % accuracy and 3 % accuracy guaranteed. It measures both ac and dc components of the dc arc current. For higher current levels, it is possible that the high dc component can lead to a low signal to noise ratio. The detection accuracy under 25 A is expected to be improved if more suitable current probes were to be used.
Table 4.1: Detection accuracy

<table>
<thead>
<tr>
<th>Voltage</th>
<th>3 A</th>
<th>6 A</th>
<th>15 A</th>
<th>25 A</th>
</tr>
</thead>
<tbody>
<tr>
<td>75 V</td>
<td>100%</td>
<td>100%</td>
<td>100%</td>
<td>100%</td>
</tr>
<tr>
<td>120 V</td>
<td>100%</td>
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<td>100%</td>
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<td>100%</td>
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<td>240 V</td>
<td>100%</td>
<td>100%</td>
<td>100%</td>
<td>60%</td>
</tr>
<tr>
<td>300 V</td>
<td>100%</td>
<td>100%</td>
<td>100%</td>
<td>40%</td>
</tr>
</tbody>
</table>

4.2.5 Detection Efficiency under Higher Source Voltage

The proposed detection signatures and algorithms are based on arc current data acquired with dc source voltage up to 300 V. The effectiveness of the proposed detection algorithm under higher source voltage is verified and analyzed in this subsection.

A Magna TSA800-30 power supply rated at 800 Vdc and 30 A is used. Tektronix MSO4054B oscilloscope is used to monitor arc current ($I_{arc}$), arc voltage ($V_{arc}$) and dc bus voltage ($V_{dc}$). The sampling frequency is 250 kHz. In order to achieve sufficient length of data for both arcing and no-arcing status, the arc data and no-arcing data are recorded separately with 4 s data length for each. Figs. 4.9-4.10 show the test results in the order of $V_{dc} = 400$ V and 600 V, respectively.

Using the proposed detection algorithm, both signatures $I_{dif}$ and $RMS_{norm}$ are calculated and analyzed. Figs. 4.11-4.12 show the $I_{dif}$ and $RMS_{norm}$ waveforms for each dc bus voltage level. The time window length is $T_{sw} = 25$ ms. From Figs. 4.11-4.12, the amplitude of arc signatures shows an obvious difference between the no-arcing case and stable arcing, which will give an efficient detection. The red dotted
line shows the potential threshold value. The above tests and analyses show that the detection algorithm will still work even at dc bus voltage as high as 600 V.

Figure 4.9: Waveforms with Vdc = 400 V.
Figure 4.10: Waveforms with Vdc = 600 V.
4.3 Summary

In this chapter, a detection algorithm is developed and implemented on a DSP microprocessor board. $k_0$ is introduced in the algorithm as a way to set the detection
robustness level. A smaller $k_0$ value leads to faster detection speed but is more prone to have false trip. A larger $k_0$ value takes longer detection time but is more robust against environmental noise or normal operation conditions. The effectiveness of the detection algorithm is verified through different sets of experiments.
Chapter 5: DC Arc Fault in DC Microgrids

DC based networks are being extensively applied as dc microgrids or dc distribution systems. DC microgrids usually include distributed generators or renewable energy resources such as PV power plants, energy storages like batteries, and loads. Considering that a large portion of the these components operate with dc power in nature, dc microgrids provides better efficiency and reliability with less conversion stage compared to their ac counterparts. DC distribution systems are even more widely adopted in applications including data centers, MEA, all electric ships, EV, and telecom power supplies [9],[44]-[11]. DC distribution systems provide the same advantages as dc microgrids including less conversion stages, higher efficiency, and less volume. The terms dc microgrids and dc distribution systems are sometimes interchangeable, although dc microgrids are more used to describe systems integrating renewable energy resources and can be locally controlled.

While dc systems offer many advantages, challenges still remain. One major challenge is the system protection. DC system protection is different from ac system due to its intrinsic natures. The fault current level in dc microgrids are usually limited by the power electronics converters, especially under islanding mode. Moreover, modern dc systems with “plug and play” features have very flexible system structures
which can cause difficulties in relay setting coordinations. Fault detection and protection coordination have already been studied extensively in order to solve the above challenges [45]-[47]. Differential current method was proved to be effective to detect high impedance fault compared to conventional overcurrent protection, although overcurrent, overvoltage, and short circuit protections are still required. However, one particular fault has been overlooked by previous studies on dc system protection: series dc arc fault.

The series dc arc fault can happen at arbitrary locations of any dc systems with a high voltage dc bus [35],[48]-[49]. A comprehensive investigation of dc arc fault in a more complicated system like dc microgrids or distribution systems still needs to be investigated. There are several issues associated with dc arc fault in a dc system that need to be addressed. A dc arc generates high frequency noise which can propagate along dc lines/cables. This traveling signal may cause false tripping on unfaulted sections. Another issue is caused by the operation of a dc microgrid. Advanced control strategies are being developed to control the current and power flow for operation optimization. The interaction between control strategies and arc faults may provide insights to the arc fault protection. A third issue is to be able to integrate the dc arc fault protection into the existing protection system very easily with the least cost.

Therefore, the focus of this chapter is to provide a study on dc arc fault protection in dc systems taking into account the aforementioned challenges and issues. This chapter will begin by presenting a generalized dc system with multiple sources and resistive loads. A dc arc simulation model is presented comprising dc impedance along with high frequency arc noise to facilitate a frequency domain detection study.
Then the impact of dc arc faults at various locations of a ring type dc microgrid is investigated. Two different droop control strategies are selected to explore the interactions between the microgrid control and dc arc faults. Based on the above study, a dc arc protection strategy is proposed.

5.1 DC Microgrids and DC Arc Faults

In this section, the structure and control of a generic dc microgrid is presented, as well as a method of modeling dc arc fault that can facilitate both analytical and simulation case studies in the following sections.

According to the applications, there are many kinds of dc microgrids and distribution systems with different system structure, components, and ratings. Although there is a lack of standards for dc applications, most dc distribution systems operate at several hundreds of volts and the current ratings vary largely depending on the load. In this chapter, a generalized ring type dc microgrid is adopted to investigate the dc arc fault analysis and protection strategy. The network scheme is shown in Fig. 5.1, consisting of four buck converter sources and three resistive loads. The system parameters are listed in Table 5.1.

Table 5.1: Simulation parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC bus reference voltage</td>
<td>$V_{\text{ref}}$</td>
<td>380 V</td>
</tr>
<tr>
<td>Load resistance</td>
<td>$R_{\text{load}}$</td>
<td>192 Ω</td>
</tr>
<tr>
<td>Nominal current of source 1, 4</td>
<td>$I_{\text{rated},1}$</td>
<td>4 A</td>
</tr>
<tr>
<td>Nominal current of source 2, 3</td>
<td>$I_{\text{rated},2}$</td>
<td>2 A</td>
</tr>
<tr>
<td>Line impedance</td>
<td>$Z_1, Z_4, Z_5$</td>
<td>0.5 Ω, 50 uH</td>
</tr>
<tr>
<td>Line impedance</td>
<td>$Z_2, Z_3, Z_6, Z_7$</td>
<td>1 Ω, 100 uH</td>
</tr>
</tbody>
</table>
In order to study the interaction between a microgrid controller and dc arc faults, two different controllers are applied for comparison: conventional voltage droop controller (CVD) and adaptive voltage droop controller (AVD). There are many other control strategies available, but the CVD and AVD are chosen because they represent distinguished controller features which will be discussed in details below [50]-[52]. The controller diagram for CVD is shown in Fig. 5.2.
The output voltage can be represented by the following equation:

\[ V_{dc} = V_{ref} - GI_{dc} \quad (5.1) \]

where \( I_{dc} \) is the converter output current, \( V_{dc} \) is the converter output voltage, \( V_{ref} \) is the output voltage reference value which is usually the system voltage rating, and \( G \) is the droop constant which is normally a positive value. As can be seen from (5.1) and Fig. 5.3, the output voltage is always less than the system rating. If all four converter sources are controlled with this strategy, the average value of all four converter output voltages is less than the system rating.
The selection of droop gain $G$ is constrained by the trade off between the desired voltage deviation and current deviation. A higher gain causes a larger voltage deviation from the reference value while a lower gain causes a larger current deviation to achieve the steady state voltage.

The droop gain of each source converter with CVD control is proportional to its current rating, to realize proportional current sharing. However, the line impedance on the dc bus causes a current sharing error in CVD. Therefore, current regulation is introduced in AVD to guarantee that the current sharing is accurately proportional to the current rating of each converter. Moreover, while the voltage reference of CVD is always lower than the rated value due to the droop gain. The AVD controller is able to correct this bias and make sure the average voltage value of all the nodes on the dc bus is equal to the rated voltage level [50].

The controller diagram for AVD is shown in Fig. 5.4. The main difference of AVD comes from the term $\bar{v}_i$ which is the locally averaged dc bus voltage, and $\Delta r$ which is the output of the current regulator. The equations for these two terms are shown below [50].

$$\bar{v}_i(t) = \int_0^t \sum_{j \in N_i} a_{ij}(\bar{v}_j(\tau) - \bar{v}_i(\tau))d\tau + v_i(t); \quad (5.2)$$

$$\Delta i = \sum_{j \in N_i} b_{ij}(i_{pu,j}^{pu} - i_{pu,i}^{pu}); \quad \Delta r = k_p \Delta i + k_i \int \Delta i \quad (5.3)$$

where $N_i$ is the set of all neighbors of converter $i$, $a_{ij}$ and $b_{ij}$ are from the Adjacency matrix, and $i_{pu,i}^{pu}$ is the per unit current value of converter $i$, equals to $\frac{I_{dc,i}}{I_{rated,i}}$.

With AVD control, each converter communicates with a few converters (neighbors) to receive per unit current value and averaged voltage value. With extra communication requirements compared to CVD, AVD control is able to boost the grid voltages.
and guarantee the average voltage of the four converter sources is at rated value, as well as to achieve accurate current sharing.

Figure 5.4: Adaptve droop controller (AVD).

In the simulation in the rest of this chapter, the dc arc fault is represented as a 10 Ω resistor in parallel with a controlled current source generating Gaussian distribution noise, as shown in Fig. 5.5. The noise variance is approximated with 0.02 A based on the preliminary results of Gaussian distribution fitting. A 10 Ω resistor is chosen to approximate an arc fault of 0.06 inch length at 4 A based on (2.3). With a known arc current $I_{arc}$ and gap length $L_{gap}$, arc voltage $V_{arc}$ can be calculated. Arc resistance $R_{arc}$ can then be calculated, which is dividing $V_{arc}$ by $I_{arc}$. Therefore, even though (2.3) does not include an arc resistance term directly, $R_{arc}$ can be calculated as follows:

$$R_{arc} = \frac{20.19 + 526.2L}{I_{arc} + 1.888L}$$

(5.4)

It is important to note that the actual arcing current will not be 4 A exactly, depending on the load current before the arc occurs, as well as the arc fault location. Therefore, the arc resistance $R_{arc}$ of a 0.06 inch arc fault in the studied microgrid may not be 10 Ω exactly.
5.2 Analysis of DC Microgrids

In order to analyze the impact of the faults, it is necessary to first study the system operation under normal conditions. Both conventional droop controller and adaptive droop controller are considered.

5.2.1 Conventional Droop Controlled DC Microgrid

Consider a dc microgrid in Fig. 5.1 that has $N = 7$ nodes with $m = 4$ sources and $n = 3$ loads. A set of $N$ equations about the node current can be derived as follows from the Kirchhoff’s circuit laws (KCL):

$$I_{dc,i} = I_{bus,i} - I_{bus,i-1}, \quad i = 1, \ldots, N$$  \hspace{1cm} (5.5)

where $I_{dc,i}$ is the unit $i$ current which can be either the output current of a source converter or a load current, $I_{bus,i}$ is the current on the bus segment connecting unit $i + 1$ and $i$. 

Figure 5.5: DC arc model for Matlab/Simulink simulation.
Another set of $N$ equations about the bus current from the Ohm’s law can be obtained as follows:

\[ I_{bus,i} = \frac{V_{bus,i+1} - V_{bus,i}}{Z_i}, \quad i = 1, \ldots, N \]  

(5.6)

where $V_{bus,i}$ is the voltage at the coupling point of unit $i$ to the dc bus.

A set of $n$ equations about the load voltage from the Ohm’s law can be obtained as follows:

\[ V_{bus,j} = R_{load,j}I_{dc,j}, \quad j = m + 1, \ldots, N \]  

(5.7)

A set of $m$ equations about the source voltage can be obtained from the CVD controller.

\[ V_{dc,k} = V_{rated} - G_kI_{dc,k}, \quad k = 1, \ldots, m \]  

(5.8)

Assuming the line impedance of each feeder connecting the converter or load to the dc bus is negligible, the converter output voltage and the load input voltage are the same as the dc bus voltage at the coupling point:

\[ V_{bus,i} = V_{dc,i}, \quad i = 1, \ldots, N \]  

(5.9)

Here we are assuming that the droop controller design is appropriate and the output voltage reference for each source can be accurately tracked. The values of $V_{rated}$, $Z_i$, $R_{load,k}$, and $G_l$ are known, leaving the unknown parameters being $V_{dc,i}$, $V_{bus,i}$, $I_{dc,i}$, and $I_{bus,i}$. These $4N$ unknown parameters can be solved with the equation groups (5.5)-(5.9), i.e. (5.10).
\[
\begin{align*}
I_{dc,i} &= I_{bus,i} - I_{bus,i-1}, \quad i = 1, \ldots, N \\
I_{bus,i} &= \frac{V_{bus,i+1} - V_{bus,i}}{Z_i}, \quad i = 1, \ldots, N \\
V_{bus,j} &= R_{load,j}I_{dc,j}, \quad j = m + 1, \ldots, N \\
V_{dc,k} &= V_{rated} - G_kI_{dc,k}, \quad k = 1, \ldots, m \\
V_{bus,i} &= V_{dc,i}, \quad i = 1, \ldots, N
\end{align*}
\]

(5.10)

The impact of a dc arc fault to the system operating points can be analyzed by inserting \( R_{arc} \) into the equations based on the fault location. It is important to notice that we are only considering the steady state arc in this analysis. The transient of arc initiation is very short and can be neglected.

### 5.2.2 Adaptive Droop Controlled DC Microgrid

For adaptive droop controlled dc microgrid, the equation groups obtained from the KCL and Ohm’s law still apply. However, due to the correction terms \( \Delta i \) and \( \Delta r \), the \( m \) equations from (5.8) cannot be used here to calculate the steady state operation point. Assuming the current sharing controller is very effective and accurate in achieving the same ratio between the actual current and the current rating in each source, the following equation can be obtained:

\[
I_{dc,l} = a_l I_{dc,l+1}, \quad l = 1, \ldots, m - 1
\]

(5.11)

where \( a_i \) is the ratio between two source current ratings and it is a known value. For a system with \( m \) sources, \( m - 1 \) equations can be derived.

Another equation can be derived from the voltage control which guarantees that the average value of all source voltage is the same as the voltage rating, as shown below:

\[
mV_{rated} = \sum_{k=1}^{m} V_{dc,k}
\]

(5.12)
Combining (5.5)-(5.7) and (5.9)-(5.12) to give (5.13) provides 4N equations, which can be solved to obtain the system operation points $V_{dc,i}, V_{bus,i}, I_{dc,i},$ and $I_{bus,i}$ for an AVD controlled dc microgrid.

\[
\begin{align*}
I_{dc,i} &= I_{bus,i} - I_{bus,i-1}, \quad i = 1, \ldots, N \\
I_{bus,i} &= \frac{V_{bus,i}-V_{bus,i-1}}{Z_i}, \quad i = 1, \ldots, N \\
V_{bus,j} &= R_{load,j}I_{dc,j}, \quad j = m + 1, \ldots, N \\
V_{bus,i} &= V_{dc,i}, \quad i = 1, \ldots, N \\
I_{dc,l} &= a_l I_{dc,l+1}, \quad l = 1, \ldots, m - 1 \\
mV_{rated} &= \sum_{k=1}^{m} V_{dc,k}
\end{align*}
\]  

(5.13)

The analytical analysis procedure presented in this section has been verified through simulations with satisfactory accuracy. It is used in the following section to investigate the impact of a dc arc fault to a dc microgrid.

5.3 The Impact of DC Arc Fault at Different Locations

For the dc microgrid protection system design, the general way to decide relay settings are through the following steps:

**Step 1** Determine possible fault locations;

**Step 2** Calculate the fault levels at different locations with each fault type;

**Step 3** Decide the fault clearing time requirement based on the device ratings and use this information to set the triggering threshold;

**Step 4** Coordinate protection devices at different locations.

The above steps are commonly adopted to set relays based on overcurrent protection, current-time protection, differential method, and time derivative of current. The
same method can be adopted for the dc arc fault protection study. In this chapter, different possible dc arc fault locations will be considered. Fault responses at each location will be analyzed, based on which the protection scheme will be developed.

In general, the possible dc arc fault locations can be summarized into five categories: input side of a source converter, source converter output close to the converter side, source converter output close to the dc bus side, one segment of the dc bus, and in series with a load.

5.3.1 Input Stage of a Source Converter

As indicated by fault location 1 in Fig. 5.1, this fault occurs at the input side of a source converter. Due to the high impedance of the dc arc, there can be a significant voltage drop across the fault, which reduces the virtual input voltage of the buck converter. However, the output voltage reference \(V_{dc,1,ref}\) generated by the droop controller remains the same and the feedback control of the converter will adjust the duty ratio to achieve the output voltage reference, as shown in Fig. 5.6. Values of the parameters in (5.5)-(5.12) remain the same.

5.3.2 Source Converter Output – Close to Converter

As indicated by fault location 2 in Fig. 5.1, the measurement point for the voltage controller is the same as bus voltage, hence \(V_{bus} = V_{dc}\) even after the arc fault starts. Since the equation groups are exactly the same as before the arc fault occurs, the system operation points maintain the same, as can be seen from Fig. 5.7.

There is no dc value or step change in all parameters. An AVD controlled system has a similar pattern. Therefore, it is not possible to detect this fault based on dc values of the measured voltage and current only. However it can also be seen from
Fig. 5.7 that high frequency noise appears at source 1 output voltage and current, as well as the load current from the adjacent load feeder, i.e. $I_{dc7}$. This high frequency noise presents the potential for efficient dc arc fault detection using frequency domain signatures.

### 5.3.3 Source Converter Output – Close to Bus

When a fault is close to the coupling point to the dc bus, as indicated by fault location 3 in Fig. 5.1, the voltage measurement for the voltage feedback control measures the converter output voltage without the voltage drop from the arc fault.

The following equation should be used in the equation groups: $V_{dc,1} = V_{bus,1} - R_{arc}I_{dc,1}$. The calculation results before and after an arc fault are shown in Table 5.2.
Figure 5.7: Fault close to converter output with CVD control

Table 5.2: Calculated source output current change with CVD control

<table>
<thead>
<tr>
<th></th>
<th>Actual Current (A)</th>
<th>Per Unit Value</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Before arc</td>
<td>After arc</td>
</tr>
<tr>
<td>Idc1</td>
<td>1.85</td>
<td>0.22</td>
</tr>
<tr>
<td>Idc2</td>
<td>0.63</td>
<td>1.42</td>
</tr>
<tr>
<td>Idc3</td>
<td>0.67</td>
<td>1.01</td>
</tr>
<tr>
<td>Idc4</td>
<td>2.74</td>
<td>3.23</td>
</tr>
</tbody>
</table>

Since $V_{dc,1}$ is still controlled to be around 380 V, the coupling point bus voltage is considerably lower than the converter output voltage due to the voltage drop across
the arc fault. Therefore the bus current $I_{\text{bus,1}}$ will increase due to the voltage difference across the bus section 1. A larger amount of current is then drawn from the other three converters and the output voltage of the faulted converter dropped to almost zero. Simulation results shown in Fig. 5.8 also verify the calculation results.

Even with AVD control, there is still a trade off: if $I_{dc,1}$ is too high, the voltage drop across the arc will increase, but then with a lower $V_{\text{bus,1}}$, the current drawn from converter 1 will be decreased. The result is that the current sharing for converter 1 cannot function anymore, which can be seen from the simulation results shown in Fig. 5.9. It can also be seen that while $I_{dc,1}$ drops to almost zero, the other three converters share the extra load for converter 1. Moreover, the per unit values of $I_{dc,2}$, $I_{dc,3}$, and $I_{dc,4}$ are still equal to each other, which shows that the current sharing control for the unfaulted sections can still function.
5.3.4 DC Bus

The dc resistance of an arc fault in this location is equivalent to increasing the line impedance from $Z_j$ to $Z_j + R_{arc}$. The operating points of the system after dc arcing can then be calculated. The calculated results are shown in Table 5.3.

Figs. 5.10-5.11 show the system response when arcing occurs on the dc bus in series with the impedance $Z_7$. Due to the unbalance of the bus impedance across the dc microgrid, the current sharing error increases significantly. The arc fault causes much impact to the neighboring nodes. Due to the increased impedance on line $Z_7$, the current drawn from source 1 reduces, and therefore weakens the dc arc fault. Moreover, due to the voltage droop gain, $V_{dc,1}$ increases with the reduced current. Hence the controllers do not worsen the arc fault when it occurs on the dc bus.

From Fig. 5.11 we can see that the current sharing control with AVD is not functioning well. By adjusting the parameters of the current sharing PI controllers in Fig. 5.4, it is possible to restore current sharing function with the cost of larger current.

Figure 5.9: Output current of the converter sources with fault close to bus with AVD control
Figure 5.10: Arc at bus with CVD control

Table 5.3: Calculated source output current change with CVD control

<table>
<thead>
<tr>
<th></th>
<th>Actual Current (A)</th>
<th>Per Unit Value</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>No arc</td>
<td>Arc at bus</td>
</tr>
<tr>
<td>Idc1</td>
<td>1.85</td>
<td>0.70</td>
</tr>
<tr>
<td>Idc2</td>
<td>0.63</td>
<td>0.37</td>
</tr>
<tr>
<td>Idc3</td>
<td>0.67</td>
<td>0.79</td>
</tr>
<tr>
<td>Idc4</td>
<td>2.74</td>
<td>3.99</td>
</tr>
</tbody>
</table>

ripples and longer stabilization time during transients and faults. This phenomenon arises an interesting prospect of the relationship between the microgrid controller
design and fault protection. On one hand, a robust microgrid controller should be able to cope with a wide range of operating conditions without compromising the current sharing capability. On the other hand, the unbalanced source currents in Fig. 5.11 could be promising dc arc fault indicators for detection purposes.

![Diagram of voltage and current sources with AVD control](image)

Figure 5.11: Arc at bus with AVD control

### 5.3.5 Load

Fig. 5.12 shows simulation results when a dc arc fault is introduced in series with load 7. Only results with the AVD controller are shown here. Both controllers are able to function well during arc faults with only the faulted load current dropping.
upon arcing. This fault location has the least impact to the other parts of the system. However, it still can be seen that the high frequency arc noise propagates to the other two unfaulted loads.

Figure 5.12: Fault at load with AVD control

5.4 DC Arc Fault Detection and Localization in DC Micro-grids

The response patterns under different fault locations are summarized in Tables 5.4-5.5. The impact of distributed line parameters is studied first. Based on the system response of dc arc faults, the detection challenges and the proposed detection and microgrid protection are then discussed.

5.4.1 Analysis of Line Attenuation Effects

In previous simulations, lumped line parameters were used to model the line impedance with one resistor and one inductor connected in series. In this subsection,
Table 5.4: DC arc fault at different locations

<table>
<thead>
<tr>
<th>Fault location</th>
<th>Analytical analysis equation group</th>
<th>AVD current sharing</th>
</tr>
</thead>
<tbody>
<tr>
<td>Source 1 input</td>
<td>No change</td>
<td>Function well</td>
</tr>
<tr>
<td>Source 1 output: close to converter</td>
<td>No change</td>
<td>Function well</td>
</tr>
<tr>
<td>Source 1 output: close to bus</td>
<td>$V_{dc,1} = V_{bus,1} - R_{arc}I_{dc,1}$</td>
<td>Relatively accurate current sharing for 3 unfaulted converters</td>
</tr>
<tr>
<td>DC bus 1</td>
<td>$I_{bus,1} = \frac{V_{bus,2} - V_{bus,1}}{Z_7}$</td>
<td>Current sharing cannot function</td>
</tr>
<tr>
<td>Load 7</td>
<td>$I_{dc,7} = \frac{V_{dc,7} - I_{dc,7} R_{arc}}{R_{load,7}}$</td>
<td>Function well</td>
</tr>
</tbody>
</table>

Table 5.5: Summary of fault responses of dc arc fault at different locations

<table>
<thead>
<tr>
<th>Fault location</th>
<th>System operation point</th>
<th>High frequency (HF) noise</th>
</tr>
</thead>
<tbody>
<tr>
<td>Source 1 input</td>
<td>No change</td>
<td>No HF noise</td>
</tr>
<tr>
<td>Source 1 output: close to converter</td>
<td>No change</td>
<td>HF noise on $V_{dc,1}, I_{dc,1}, I_{dc,2}, I_{dc,7}$</td>
</tr>
<tr>
<td>Source 1 output: close to bus</td>
<td>Change</td>
<td>HF noise on $I_{dc,1}, I_{dc,2}$, $I_{dc,5}, I_{dc,6}, I_{dc,7}$</td>
</tr>
<tr>
<td>DC bus 1</td>
<td>Change</td>
<td>HF noise on $I_{dc,5}, I_{dc,6}, I_{dc,7}$</td>
</tr>
<tr>
<td>Load 7</td>
<td>Only local load current changes</td>
<td>HF noise on $I_{dc,5}, I_{dc,6}, I_{dc,7}$</td>
</tr>
</tbody>
</table>

The impact of the distributed line parameters to high frequency noise is examined in Matlab through the following steps:

**Step 1** Real arc current data $I_{arc}$ is loaded into Matlab workspace and is then fed into variable $var$;
Step 2 The dc buses are modeled with either multiple pi sections or a distributed parameter line model;

Step 3 Set the dc bus length and pi section number;

Step 4 Compare the arc current waveforms at the sending and receiving ends of the transmission line.

The simulation model is shown in Fig. 5.13 where the top circuit uses pi sections and the bottom circuit uses a distributed parameter model. The sending end signal $I_{arc}$ only contains ac component filtered with a 1.5 kHz - 45 kHz bandpass filter. The receiving end signal is $I_{pi}$ for the pi section model and $I_{dist}$ for the distributed model. The maximum frequency range represented by the pi section line model can be approximated by the following equation [53]:

$$f_{max} = \frac{Nv}{8l_{tot}}$$  \hspace{1cm} (5.14)

where $N$ is the number of pi sections, $v$ is the propagation speed $v = \frac{1}{\sqrt{lc}}$ with $l$ in H/km and $c$ in F/km, and $l_{tot}$ is line length in the unit of km. The cases with $l = 2$ km and $l = 10$ km are studied. Eight pi sections are used for 2 km long length in order to achieve $f_{max} = 125$ kHz.

NYM3 * 2.5mm$^2$ cables as shown in Fig. 5.14 are used in distribution systems [54]. The distributed parameters of this type of cable have been studied before in [54]. Since the frequency component of interest is around 150 kHz, the line parameters under 150 kHz are estimated based on [54] and are summarized in Table 5.6.

Simulation results with both 2 km and 10 km line lengths under 15 A and 25 A arc currents are shown in Figs. 5.15-5.16. It can be seen that when cable length is
Table 5.6: Approximate distributed line parameters

<table>
<thead>
<tr>
<th>Parameters</th>
<th>values under 150 kHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>C</td>
<td>80 pF/m</td>
</tr>
<tr>
<td>R</td>
<td>0.02 Ω/m</td>
</tr>
<tr>
<td>L</td>
<td>0.19 uH/m</td>
</tr>
</tbody>
</table>

At 2 km, there is no obvious signal attenuation with both the pi and distributed line models. This shows that the lumped parameter model used in previous simulations is sufficient to represent the circuit characteristics. There is not much difference between the pi and distributed line models since a large number of pi sections are used. Both 15 A and 25 A cases share the same pattern. Attenuation is higher when the line length is increased to 10 km.
Figure 5.14: \( NYM3 \times 2.5\text{mm}^2 \) cable [54]

(a) Simulation results with 2 km line length. (b) Simulation results with 10 km line length.

Figure 5.15: Simulation results with 15 A, 240 V arc current.

5.4.2 Challenges of DC Arc Fault Detection in Microgrids

Generally, arc fault detection is achieved through time-domain and/or frequency domain change in fault current. Time domain information has the advantages of
simple calculation and easy implementation, but is subject to false trip under normal operational changes. Frequency domain or time-frequency domain detection usually has better efficiency but requires more sophisticated hardware installation. The combination of both time domain and time-frequency domain information was proposed in the previous chapter to improve the overall detection performance [48]. However, in the context of a dc microgrid rather than a single loop circuit, the efficiency of previous detection techniques are limited by two factors: microgrid control strategies and high frequency noise propagation. These factors should be taken into account when planning the protection system of a dc microgrid.

For example, when a dc arc fault occurs close to the output side of a source converter, the local output current is controlled to be the same as prior to the arc,
which makes it difficult to detect the arc fault based on dc values of the system parameter. In this case, the high frequency noise can be used. However, the high frequency arc noise will travel to the neighboring load, as can be seen from Fig. 5.7. This could easily cause a mis-trigger from the neighboring unfaulted load while leaving the fault in the voltage source unattended.

By examining Table 5.5 closely, it can be seen that, even though different fault locations can cause similar responses in certain parameters, it is possible to distinguish different faults by considering all responses including system operating points and the presence of high frequency noise in source or load currents. This observation provides opportunity for a comprehensive dc arc fault protection scheme as presented in the following section.

5.4.3 Proposed Solutions

Based on the fault responses analysis from the previous sections and Table 5.5, a fault detection and localization method is proposed. The proposed protection strategy utilizes one local detector at each feeder and one master detector, as shown in Fig. 5.17. The existing voltage and current measurement unit for converter control can be used by the local detectors. The detailed functional flowcharts for the local detectors and master detector are shown in Figs. 5.18-5.20.

Local detector has two main functions: monitor feeder voltage and current, and conduct local detection algorithm calculation including the average value step change and high frequency noise DWT coefficients. The detailed calculation procedures of DWT have been discussed in Chapter 4 and can also be found in [48]. Local detectors also compare calculated values with a threshold and then send arc event indicators.
(flags) to the master detector. Arc event indicators show if the local unit is experiencing abnormal high frequency noise or step change, but local detectors cannot decide if it is a local fault or it is influenced by a fault at nearby locations. Master detector provides final decision on the fault location by considering fault indicators from all local detectors.

The proposed arc fault detection and localization strategy provides general guidelines and framework of planning comprehensive dc arc fault protection in a microgrid.
It can be easily integrated with existing system protection functions, i.e., digital relays, programmable solid state power controllers (SSPCs), solid state circuit breakers (SSCBs). SSCBs utilize semiconductor devices as the disconnecter which has a 5-15 $\mu s$ switching time under up to 25 A. It has a much faster switching speed compared to conventional electromechanical contactors which have a typical trip time of 15 - 110 ms [55]. When adopting the above mentioned advanced protection devices, dc arc fault detection and protection can be easily implemented.
5.5 Summary

A dc arc model is utilized to study arc fault impact to a dc microgrid. The system response of dc arc faults at different locations are studied in detail. It is found that
at certain locations of the microgrid, dc arc faults can either cause current sharing problems or get higher fault current due to controllers. Challenges of detecting and localizing dc arc faults in a microgrid caused by microgrid controllers and propagation of high frequency noise from arc current are then discussed. Extrapolating these analyses, an arc fault detection and localization strategy is proposed which provides a method to coordinate arc fault detection at various locations.
Chapter 6: Contributions and Future Work

6.1 Summary and Conclusions

The major motivations and goals of this work are to develop simple yet effective detection and protection methods for dc arc faults in dc electrical systems. The main contributions of this work include:

- The physical characteristics of the dc arc are studied under the voltage, current, and gap lengths encountered in common modern dc applications. The V-I model of the dc arc is developed for a circuit with resistive loading and relatively low current amplitude, taking into account the influence of gap length. High frequency arc noise is also modeled with Gaussian amplitude distribution and is found that the noise level is related to the dc current level. The proposed arc modeling method can be used to facilitate system level simulation study.

- DC arc current is analyzed in both time and time-frequency domain. A time domain signature $I_{dif}$ with very simple computation procedure is proposed to differentiate the arc fault from the normal operational condition. The impact of narrowband power electronics switching noise is studied by connecting a boost converter in parallel with the load branch. It is found that the narrowband
switching noise and its harmonics present noises that can be easily isolated and avoided for detection purposes. Wavelet packet decomposition is adopted as a time-frequency analysis tool to identify the change caused by arcing in both time and frequency domain.

- A detection algorithm is proposed based on the time and time-frequency domain signatures. The algorithm is implemented with a DSP microcontroller board where most of the computation is allocated to the interrupt function. All the computation in the interrupt function can be finished within one timer period. The computation load is minimized and can be as low as 1 $\mu$s, which ensures fast fault detection. The effectiveness of the proposed algorithm is verified through multiple sets of experiments.

- The impact of dc arc faults to a dc microgrid with passive loads is evaluated. The fault responses of arcing at different locations are examined from the aspects of system operation points and high frequency noise propagation. It is found that the combination of the system operation points and high frequency noise propagation provides useful indication to the fault location, which a comprehensive protection scheme is developed. This protection scheme prevents mistriggering caused by high frequency noise traveling within the microgrid.

This research directly increases the reliability and stability of dc networks. It fills the gap between traditional electrical system protection and dc arc fault protection. Moreover, the method of dc arc modeling enables researchers, utilities and manufacturers to evaluate the system response under dc arc faults for more complicated systems.
6.2 Future Work

- The arc models developed in this work were from circuits with resistive loads. In the future, they can be examined for applications involving reactive loads, i.e., resistive loads with inductive or capacitive loads.

- More arc data should be obtained to establish more accurate high frequency noise models. Gaussian amplitude distribution has been adopted in this dissertation to model high frequency arc noise. It has been identified through preliminary fitting that the noise level can be related to the dc current level. A solid quantitative expression can be derived in the future by acquiring more arc data under smaller current steps, e.g. 2 A steps.

- The Gaussian distribution study was only conducted with the amplitude of the arc noise in this work. It is also of interest to study Gaussian frequency distribution of the arc noise in the future.

- The proposed detection and protection strategy should be realized in a digital relay or SSPC. Implementation can be conducted by creating real arc faults in a hardware test bed with multiple sources and loads. The time for extinguishing the arc should be considered as well.

- The dc microgrid considered in this study involves resistive loads only. Other load types, especially constant power loads, should be considered. The interactions between microgrid controllers and other load types should be studied.
Bibliography


[34] V. Terzija, M. Popov, V. Stanojevic, and Z. Radojevic, ”EMTP simulation and spectral domain features of a long arc in free air”, in Proc. 18th Int. Conf. Elec. Distrib., 2005, pp. 1-4.


[53] Available online: www.mathworks.com


Appendix A: Matlab m.file to Compare Different Time-Frequency Analysis Techniques

clc;clear all;close all;

%%% Miscellaneous
lw = 1;
fs = 22;

%%% Create the signal
Ts = .1e-3;
t = 0:Ts:0.2;
y1 = 0.7.*sin(2*pi*100*t);
y2 = 0.1.*sin(2*pi*1000*t);
n1 = find(t == 0.07);
n2 = find(t == 0.13);
y2(1:n1) = zeros(1,n1);
y2(n2:end) = zeros(1,length(y2)-n2+1);
ytotal = y1+y2;

%%% Compute the fft of this signal
amp = fft(ytotal);
abs_amp = abs(amp)./(length(y2)/2);

%%% Plot the figures
figure(1);
plot(t,ytotal,’b’,’LineWidth’,lw);
xlabel(’time (s)’,’FontSize’,fs);
ylabel(’amplitude’,’FontSize’,fs);
xlim([0 0.2]);ylim([-1 1]);
set(gca,’FontSize’,fs-4);
saveas(gca,’time_example.jpg’);
freqvals = 0:length(abs_amp)-1;
freqvals = freqvals./length(abs_amp);
freqvals = freqvals.*(1/Ts);

figure(2);
plot(freqvals,abs_amp,'LineWidth',lw);
xlabel('Freq (Hz)','FontSize',fs);
ylabel('amplitude','FontSize',fs);
xlim([0 3000]);set(gca,'FontSize',fs-4);
text(150,0.5,'ightarrow main signal','FontSize',fs-2);
text(1050,0.025,'ightarrow noise','FontSize',fs-2);
saveas(gca,'dft_example.jpg');

%% STFT Test
%N = round((length(ytotal))/12)
N = 128; % 30 time bins
figure(3);
spectrogram(ytotal,N,[],10000,1/Ts);
view(90,-90);
colormap('default')
set(gca,'FontSize',fs-2);
ylabel('time (s)','FontSize',fs);
xlabel('normalized freq. (x\pi)','FontSize',fs);
saveas(gca,'normal.jpg');

N = 256; % 14 time bins
figure(4);
spectrogram(ytotal,N,[],10000,1/Ts);
view(90,-90);
colormap('default')
set(gca,'FontSize',fs-2);
ylabel('time (s)','FontSize',fs);
xlabel('normalized freq. (x\pi)','FontSize',fs);
saveas(gca,'long.jpg');

N = 32; % 124 time bins
figure(5);
spectrogram(ytotal,N,[],10000,1/Ts);
view(90,-90);
colormap('default')
set(gca,'FontSize',fs-2);
ylabel('time (s)','FontSize',fs);
xlabel('normalized freq. (x\pi)','FontSize',fs);
saveas(gca,'short.jpg');

%% Wavelet transform
wavname = 'coif5';
figure(7);
cwt(ytotal,0.01:0.05:150,wavname,'plot');
view(0,-90);
colormap('default');
set(gca,'FontSize',fs-2);
title('');
saveas(gca,'cwtfunc.jpg');

%% Plot the wavenames
[psi x] = wavefun('mexh',12);
figure(8);
plot(x,psi,'LineWidth',lw); grid on;
%title('Mexican hat wavelet function','FontSize',fs);
set(gca,'FontSize',fs-2);
saveas(gca,'mexhat.jpg');

%% DWT
[Lo_D,Hi_D,Lo_R,Hi_R] = wfilters('coif5');
c1coef = downsample(conv(ytotal,Lo_D,'valid'),2);
d1coef = downsample(conv(ytotal,Hi_D,'valid'),2);
c2coef = downsample(conv(c1coef,Lo_D,'valid'),2);
d2coef = downsample(conv(c1coef,Hi_D,'valid'),2);
c3coef = downsample(conv(c2coef,Lo_D,'valid'),2);
d3coef = downsample(conv(c2coef,Hi_D,'valid'),2);

d1rec = conv(upsample(d1coef,2),Hi_R);
d2rec = conv(upsample(d2coef,2),Hi_R);
d2rec = conv(upsample(d2rec,2),Lo_R);
d3rec = conv(upsample(d3coef,2),Hi_R);
d3rec = conv(upsample(d3rec,2),Lo_R);

d2rec = conv(upsample(d2rec,2),Lo_R);

d2rec = conv(upsample(d2rec,2),Lo_R);

d3rec = conv(upsample(d3rec,2),Lo_R);

d3rec = conv(upsample(d3rec,2),Lo_R);

d3rec = conv(upsample(d3rec,2),Lo_R);

d3rec = conv(upsample(d3rec,2),Lo_R);

d3rec = conv(upsample(d3rec,2),Lo_R);

d3rec = conv(upsample(d3rec,2),Lo_R);

figure(10);
set(gcf,'PaperUnits','centimeters');
set(gcf,'PaperPosition',[0 0 20 21]); % [left bottom
    width height]
subplot(4,1,1);
plot(d1coef,'b');hold on;
ylabel('$d_1$','interpreter','latex','FontSize',fs);
title('[2.5, 5] kHz','interpreter','latex','FontSize',fs)
set(gca,'FontSize',fs-4);

subplot(4,1,2);
plot(d2coef);hold on;
ylabel('$d_2$','interpreter','latex','FontSize',fs);
title('[1.25, 2.5] kHz','interpreter','latex','FontSize',fs)
set(gca,'FontSize',fs-4);

subplot(4,1,3);
plot(d3coef);hold on;

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ylabel('$d_3$','interpreter','latex','FontSize',fs);
title('[$.625, 1.25]$ kHz','interpreter','latex','FontSize',fs)
set(gca,'FontSize',fs-4);

subplot(4,1,4);
plot(c3coef);hold on;
ylabel('$c_3$','interpreter','latex','FontSize',fs);
title('[$0, .625]$ kHz','interpreter','latex','FontSize',fs)
set(gca,'FontSize',fs-4);
saveas(gca,'dwtsignal.jpg');

figure(11);
subplot(2,1,1);
plot(d3coef);hold on;
ylabel('$d_3$','interpreter','latex','FontSize',fs);
title('[$.625, 1.25]$ kHz','interpreter','latex','FontSize',fs)
set(gca,'FontSize',fs-4);

subplot(2,1,2);
plot(c3coef);hold on;
ylabel('$c_3$','interpreter','latex','FontSize',fs);
title('[$0, .625]$ kHz','interpreter','latex','FontSize',fs)
set(gca,'FontSize',fs-4);
saveas(gca,'dwtsignal2.jpg');
Appendix B: DSP Code for Detection Algorithm

B.1 Main Code

// DC Arc Detection using Time Domain Current Difference and Wavelet Decomposition

#include "DSP28x_Project.h"
#include <math.h>
#include "My_structs_def.h"
#include "My_filters_def.h"

#define ADC_CKPS 0x1 // ADC module clock = HSPCLK/2
    ADC_CKPS = 25.0MHz/(1*2) = 12.5MHz
#define FREQPRD 748 // 374 = 200 kHz in Up-Down Mode
#define CLIMIT 5000 // Number of data points in one time window
#define MINLIM 65535
#define FILTLENGTH 8 // Length of the wavelet filters
#define RMSTH 2 // Threshold value of RMS
#define IDIFTH 200 // Threshold value of Idif

// Prototype statements for functions found within this file.
Interrupt void adc_isr(void);
void init_adc_params(void);
void init_pwm_params(void);

// Global variables used in this example:
Uint16 LoopCount;
Uint16 ConversionCount;
Uint16 Voltage1[10];

Uint16 Icurr = 0;
Uint16 i = 0;
main()
{
    // This example function is found in the DSP2833x_SysCtrl.c file.
    InitSysCtrl();

    // Setting up Regular GPIO
    EALLOW;
    GpioCtrlRegs.GPAMUX1.bit.GPIO7 = 0; // All GPIO
    GpioCtrlRegs.GPAMUX1.bit.GPIO16 = 0; // All GPIO
    GpioCtrlRegs.GPAMUX2.bit.GPIO7 = 0; // All GPIO
    GpioCtrlRegs.GPAMUX2.bit.GPIO16 = 0; // All GPIO
    EDIS;

    // Now set the pin GPIO7 to High using GPADAT
    GpioDataRegs.GPADAT.bit.GPIO7 = 1;
    GpioDataRegs.GPADAT.bit.GPIO16 = 0;

    // Sets up the PWM1 GPIO pins
    InitEPwm1Gpio();

    EALLOW;
    #if (CPU_FRQ_150MHZ) // Default - 150 MHz SYSCLKOUT
    #define ADC_MODCLK 0x3 // HSPCLK = SYSCLKOUT/2 *ADC_MODCLK2 =
                          150/(2*3) = 25.0 MHz
    #endif
    #if (CPU_FRQ_100MHZ)
    #define ADC_MODCLK 0x2 // HSPCLK = SYSCLKOUT/2 *ADC_MODCLK2 =
                          100/(2*2) = 25.0 MHz
    #endif
    EDIS;

    // Step 3. Clear all interrupts and initialize PIE vector table:
    // Disable CPU interrupts
    DINT;

    // This function is found in the DSP2833x_PieCtrl.c file.
    InitPieCtrl();

    // Disable CPU interrupts and clear all CPU interrupt flags:
    IER = 0x0000;
    IFR = 0x0000;

    // Initialize the PIE vector table with pointers to the shell
    Interrupt
InitPieVectTable();

// Interrupts that are used in this example are re-mapped to
EALLOW;
PieVectTable.ADCINT = &adc_isr;
EDIS;

// Step 4. Initialize all the Device Peripherals:
// This function is found in DSP2833x_InitPeripherals.c
// InitPeripherals(); // Not required for this case
InitAdc(); // Power up the adc and calibration
functions

// Enable ADCINT in PIE
PieCtrlRegs.PIEIER1.bit.INTx6 = 1;
IER |= M_INT1; // Enable CPU Interrupt 1
EINT; // Enable Global interrupt INTM
ERTM; // Enable Global realtime interrupt DBGM

// Initialize variables
for(i=0;i<FILTLENGTH;i++){
Drms.Ihold[i] = 0;
Drms.coefl1[i] = 0;
}
Drms.index = 0;
Drms.flag = 0;
Drms.counter = 0;

// Initialize variables
LoopCount = 0;
ConversionCount = 0;
Iavg.T_sum = 0;
Iavg.counter = 0;
Iavg.Cavg = 0;

Idif.Imax = 0;
Idif.Imin = MINLIM;
Idif.Idiff = 0;
Drms.indexl2 = 0;
Drms.T_sum_coefl2 = 0;
Drms.T_sum_coefh2 = 0;
Drms.Rmscoefl2 = 0;
Drms.Rmscoefh2 = 0;
Drms.Rms_normalized = 0;

Drms.coefl2E = 0;
Drms.coefh2E = 0;
Drms.counterE = 0;
Det.dflag = 0;
Det.test = 0;
Det.counter = 0;
Det.Idif_th = 200;
Det.Rms_th = 1;
Det.start_counter = 0;
Det.start_flag = 0;
Det.det_start_flag = 0;

// Initialize the adc and the pwm parameters
init_adc_params();
init_pwm_params();

// In the main function, final calculation of the signatures is
// performed here
while(1){
  if(Det.dflag == 1){
    Det.dflag = 0;
    Drms.Rmscoefl2 = sqrt(Drms.coefl2E); // Compute the rms in
each band
    Drms.Rmscoefh2 = sqrt(Drms.coefh2E); // Compute the rms in
each band
    Drms.Rms_normalized = Drms.Rmscoefh2/Drms.Rmscoefl2; // Normalized
    RMS value, (50˜100k)/(0˜50k)
    
    // If the current difference and energy is higher than threshold
    values
    if ((Idif.Idiff > Det.Idif_th)&&(Drms.Rms_normalized > Det.Rms_th)){
      Det.start_flag = 1;
      if (Det.det_start_flag == 1){
        Det.counter += 1;
      }
    }
    else{
      Det.counter = 0; // Reset the counter if not over
      threshold
    }
  }
  else{
    Det.counter = 0; // Reset the counter if not over
    threshold
  }
  
  // This part is to disable the detection signal to verify the
detection during stable arcing as presented in Fig. 4.8
  if (Det.start_flag == 1){
    Det.start_counter += 1;
    if (Det.start_counter >= 30){
      Det.det_start_flag = 1;
      GpioDataRegs.GPADAT.bit.GPIO7 = 0;
    }
  }
}
// If arc was detected consecutively in multiple windows
if (Det.counter >= 1) {  // Here k0 = 1, it can also
    Det.counter = 0;
    GpioDataRegs.GPADAT.bit.GPIO16 = 1;  // To signal fault
}
}  // End main

/******** Interrupt Functions ********/
interrupt void adc_isr(void){
    Icurr = AdcRegs.ADCRESULT0 >> 4;

    // Create FIFO Register
    for (i=7; i>=1; i--){
        Drms.Ihold[i] = Drms.Ihold[i-1];
    }
    Drms.Ihold[0] = Icurr;
    Drms.counter += 1;

    // For downsampling by two
    if (Drms.counter >= 2){
        Drms.counter = 0;
        Drms.flag = 1;  // Signal to begin the coefficient
                        // computation
    }
    else{
        Drms.flag = 0;
    }

    // Get the first level
    if (Drms.flag == 1){
        Drms.flag = 0;  // Reset the flag everytime we get
                        // two inputs
        // Compute the first level of DWT

        // Store into a FIFO Register
        for (i=7; i>=1; i--){
            Drms.coefl1[i] = Drms.coefl1[i-1];
        }
    }
}
Drms.coefl1[0] = Drms.Yout1;
Drms.counterl2 += 1;  // Make a counter for downsampling

if(Drms.counterl2 >= 2){
    Drms.counterl2 = 0;
    Drms.flagl2 = 1;  // Signal to begin the coefficient computation
}

// Level 2 low and high pass coefficient computation
if(Drms.flagl2 == 1){
    Drms.flagl2 = 0;  // Reset the flag everytime we get two inputs from level 1

    // Now compute the second level of DWT


    Drms.T_sum_coefl2 += (Drms.coefl2*Drms.coefl2)*(0.0008);
    Drms.T_sum_coefh2 += (Drms.coefh2*Drms.coefh2)*(0.0008);
    Drms.counterE += 1;
}

// For Average Computation
Iavg.T_sum += (Uint32)Icurr;

// For Idif Computation
if (Icurr > Idif.Imax){
    Idif.Imax = Icurr;
    Idif.Imin = Idif.Imin;
}
else if (Icurr < Idif.Imin){
    Idif.Imax = Idif.Imax;
    Idif.Imin = Icurr;
}
else{
    Idif.Imax = Idif.Imax;
    Idif.Imin = Idif.Imin;
}

if(Iavg.counter >= (CLIMIT-1)){
    Iavg.Cavg = ((float32)Iavg.T_sum)*(.0002);
    Idif.Idiff = Idif.Imax - Idif.Imin;
    Drms.coefl2E = Drms.T_sum_coefl2;
    Drms.coefh2E = Drms.T_sum_coefh2;
    Det.dflag = 1;
    Drms.counterE = 0;
    Drms.T_sum_coefl2 = 0;
    Drms.T_sum_coefh2 = 0;
    Idif.Imax = 0;
    Idif.Imin = MINLIM;
    Iavg.T_sum = 0;
    Iavg.counter = 0;
}
else{
    Iavg.counter ++;
}

// Reinitialize for next ADC sequence
AdcRegs.ADCTRL2.bit.RST_SEQ1 = 1; // Reset SEQ1
AdcRegs.ADCST.bit.INT_SEQ1_CLR = 1; // Clear INT SEQ1 bit
PieCtrlRegs.PIEACK.all = PIEACK_GROUP1; // Acknowledge interrupt to PIE

return;
}

/** Regular Functions **/
void init_adc_params(void){
    // Configure ADC
    AdcRegs.ADCTRL3.bit.ADCCLKFS = ADC_CKFS;
    AdcRegs.ADCMAXCONV.all = 0x0000; // Setup 2 conv’s on SEQ1
    AdcRegs.ADCCHSELSEQ1.bit.CONV00 = 0x0; // Setup ADCINA3 as 1st SEQ1 conv.
    AdcRegs.ADCTRL2.bit.EPWM_SOCA_SEQ1 = 1;// Enable SOCA from ePWM to start SEQ1
    AdcRegs.ADCTRL2.bit.INT_ENA_SEQ1 = 1; // Enable SEQ1 interrupt (every EOS)
}

114
void init_pwm_params(void)
{
  // Assumes ePWM1 clock is already enabled in InitSysCtrl();
  EPwm1Regs.ETSEL.bit.SOCASEL = 4; // Select SOC from from
  // CMPA on upcount
  EPwm1Regs.EPS.bit.SOCAPRD = 1; // Generate pulse on 1st
  // event
  EPwm1Regs.TBPRD = FREQPRD; // Set timer period
  EPwm1Regs.CMPA.half.CMPA = 1;
  EPwm1Regs.TBPHS.half.TBPHS = 0x0000; // Phase is 0
  EPwm1Regs.TBCTR = 0x0000; // Clear counter
  // Setup For PWM Output (not needed)
  EPwm1Regs.TBCTL.bit.CTRMODE = TB_COUNT_UP; // Count up
  EPwm1Regs.TBCTL.bit.PHSEN = TB_DISABLE; // Disable phase
  EPwm1Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1; // Clock ratio to
  SYCLKOUT
  EPwm1Regs.TBCTL.bit.CLKDIV = TB_DIV1;
  EPwm1Regs.CMPCCTL.bit.SHDWAMODE = CC_SHADOW; // Load registers
  // every ZERO
  EPwm1Regs.CMPCCTL.bit.SHDWAMODE = CC_SHADOW;
  EPwm1Regs.CMPCCTL.bit.LOADAMODE = CC_CTR_ZERO;
  EPwm1Regs.CMPCCTL.bit.LOADBMODE = CC_CTR_ZERO;
  // Set actions
  EPwm1Regs.AQCTLA.bit.CAU = AQ_TOGGLE; // Set PWM1A on
  // Zero
  // // // Active Low PWMs - Setup Deadband
  EPwm1Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE;
  EPwm1Regs.DBCTL.bit.POLSEL = DB_ACTV_LO;
  EPwm1Regs.DBCTL.bit.IN_MODE = DBA_ALL;
}

B.2 Filter Coefficients

// Coiflet 5 Coefficients
//float32 Lo_P[30] =
//{-0.000000095176573,-0.0000000167442886,0.0000002063761851,
// 0.0000003734655175,-0.0000021315026810,-0.0000041340432273,
// 0.0000140541149702,0.000302259581813,-0.000638131343045,
// -0.001662863702013,0.002433373212658,0.006764185448053,
// -0.009164231162482,-0.019761778942573,0.032683574267112,
// 0.041289208750182,-0.105574208703339,-0.062035963962904,}
// 0.437991626171837, 0.774289603652956, 0.421566206690851,
// -0.052043163176244, -0.091920010559696, 0.028168028970936,
// 0.023408156785839, -0.01013117519850, -0.004159358781386,
// 0.002178236358109, 0.00035858968796, -0.000212080839804;
//
// float32 Hi_P[30] =
// {0.000212080839804, 0.00035858968796, -0.002178236358109,
// -0.004159358781386, 0.01013117519850, 0.023408156785839,
// -0.028168028970936, -0.091920010559696, 0.052043163176244,
// 0.421566206690851, -0.774289603652956, 0.437991626171837,
// 0.062035963962904, -0.10574208703339, -0.041289208750182,
// 0.032683574267112, 0.0197617789422573, -0.009164231162482,
// -0.006764185448053, 0.002433373212658, 0.00166286370213,
// -0.000638131343045, -0.000302259581813, 0.000140541149702,
// 0.000041340432273, -0.000021315026810, -0.00003734655175,
// 0.000002063761851, 0.000000167442886, -0.00000095176573};

// Db 4 Coefficients
float32 Lo_P[8] = {-0.010597401784997, 0.032883011666983,
0.030841381835987, -0.187034811718881,
-0.027983769416984, 0.630880767929590,
0.714846570552542, 0.230377813308855};

float32 Hi_P[8] = {-0.230377813308855, 0.714846570552542,
-0.630880767929590, -0.027983769416984,
0.187034811718881, 0.030841381835987,
-0.032883011666983, -0.010597401784997};