Full-wave Electromagnetic Modeling of Electronic Device Parasitics for Terahertz Applications

Dissertation

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The unique spectroscopic utility and high spatial resolution of terahertz (THz) waves offer a new and vastly unexplored paradigm for novel sensing, imaging, and communication applications, varying from deep-space spectroscopy to security screening, from biomedical imaging to remote non-destructive inspection, and from material characterization to multi-gigabit wireless indoor and outdoor communication networks. To date, the THz frequency range, lying between microwave and infrared bands, has been the last underexploited part of the electromagnetic (EM) spectrum due to technical and economical limitations of classical electronics- and optics-based system implementations. However, thanks to recent advancements in nano-fabrication and epitaxial growth techniques, sources and sensors with cutoff frequencies reaching the submillimeter-wave (sub-mmW) band are now realizable. Such remarkable improvement in electronic device speeds has been achieved mainly through aggressive scaling of critical device features, such as the junction area for Schottky barrier diodes (SBDs), and the gate length in high electron mobility transistors (HEMTs). Such aggressively-scaled and refined device topologies can significantly enhance the intrinsic device capabilities, however, the overall device performance is still limited by the parasitic couplings associated with device interconnect metallization. Consequently, geometry- and material-dependent parasitic couplings,
induced by EM field interactions within the device structure, exacerbate the performance and diminish the gains achieved by the improved intrinsic device behavior. In particular, as the operation frequency approaches the THz barrier, device dimensions become comparable to signal wavelength.

The main objective of this dissertation is to develop accurate lumped- and distributed-element equivalent circuits, and full-wave EM simulation-based iterative parameter extraction algorithms, to accurately model the extrinsic parasitics of electronic devices at THz frequencies. First, we demonstrate and characterize the EM coupling effects that restrict the THz detection and mixing performance of zero-bias surface-channel sub-mmW SBDs. This is achieved by a distributed equivalent circuit model to account for the wave propagation phenomena along the device air bridge in the 10 GHz - 1.1 THz band. The major power dissipation mechanisms of THz Schottky barrier diodes, including semiconducting substrate losses, leaky passivation dielectric losses, conductive metallization losses, and losses due to increased series resistance of epitaxial and buffer layers are incorporated into the proposed equivalent circuit model. Based on this new “parasitic-aware” circuit model, we present a novel multi-step systematic parameter extraction algorithm. The accuracy of the developed extraction procedure is validated through comparisons with the experimental data reported in the literature. More importantly, the shortcomings of conventional lumped-element circuits for THz diode modeling and the broadband accuracy achieved by the proposed distributed circuit model are illustrated through comparisons with full-wave simulated frequency response of the device in THz band. Key parasitic components that are most detrimental to the performance are identified, and a method to optimize device performance using the equivalent circuit model is demonstrated. In addition,
we demonstrate over 10 dB improvement in conversion efficiency for a diode-based single-ended passive mixer at 1 THz through optimization of diode geometry.

We next focus on three-terminal devices, and utilize full-wave EM simulation tools for characterization of extrinsic parasitics of millimeter-wave (mmW) HEMTs. Subsequently, we develop a lumped-element parasitic equivalent circuit model for HEMTs in the mmW band. Based on this lumped circuit model, we develop a new multi-step systematic model extraction algorithm to determine the components of the equivalent circuit. For the first time, an analytical procedure for measurement-based estimation of gate-to-drain mutual inductance is developed. We also show that this mutual inductance is detrimental to device operation due to the inductive feedback path it creates at mmW frequencies. The accuracy and robustness of the suggested algorithm are verified through comparisons between simulated, measured, and modeled frequency responses of the designed test standards up to 325 GHz. As such, we show that the proposed lumped parasitic equivalent circuit achieves broadband accuracy in mmW band. The adverse impacts of EM interactions on gain and noise performance are also evaluated. Major parasitic components that are most detrimental to the mmW performance are identified, and conveniently optimized via subsequent circuit analysis. As a result, design guidelines are provided for optimum device geometry to achieve the maximum speed and best noise performance. We also demonstrate via full-wave EM simulations that around 20% improvement in maximum oscillation frequency, 20% reduction in minimum noise figure, and 10% increase in associated power gain at 20 GHz are concurrently achievable through optimization of number of gate fingers, and gate finger width.
To further expand the equivalent circuit of HEMTs beyond the mmW band into THz frequencies, we present a distributed parasitic equivalent circuit model to account for the wave propagation effects along the gate width of HEMTs. This is achieved by developing a multi-step systematic parameter extraction algorithm, which accounts for the external parasitics of device metallization, that are comparable in size to operating wavelength. The accuracy of the proposed extraction procedure is again validated through full-wave (FW) simulations, measurements, and circuit model responses up to 750 GHz. This distributed HEMT model is utilized to evaluate the adverse impact of extrinsic parasitic couplings on device speed and noise performance. Key parasitic components are identified, and redesigned using the equivalent distributed circuit. As a result, design guidelines are developed for optimum device layout selection to accomplish the highest speed and noise performance. As an example, we demonstrate 10% improvement in maximum oscillation frequency, 10% reduction in minimum noise figure, and 5% increase in associated power gain at 50 GHz via optimization of device gate finger number, and unit finger width.

This dissertation demonstrates the utility of full-wave EM simulation tools as an alternative to fabrication and measurement-based equivalent circuit models. As such, the proposed approach is a convenient and cost-effective solution to the problem of device modeling in THz frequency range. Through the proposed full-wave EM simulation-based characterization and performance optimization methodology, RF engineers can determine the optimum layout for the diodes and transistors used in a variety of integrated circuit applications, including low-noise amplifiers, voltage-controlled oscillators, power amplifiers, and mixers.
Dedicated to my mother...
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Vita

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Chapter 1: Introduction

The last decade has witnessed an explosive growth in wireless multimedia services, including broadband video on demand, instant messaging, and voice over the internet. The exponentially growing demand for higher data transmission rates induced by rapid proliferation of wireless applications has prompted renewed interest toward exploitation of previously unlicensed millimeter-wave (mmW) and submillimeter-wave (sub-mmW) bands. This relatively unexplored part of the spectrum, which is also referred to as the terahertz (THz) band, lies between microwave and infrared bands, spanning roughly from 100 GHz to 10 THz [1]. The primary drivers of the rising interest in this frequency range are the availability of a huge amount of unoccupied bandwidth and the low loss transmission windows over which the atmospheric absorption is relatively small [2] - [3]. Apart from short-range high-speed wireless data transfer, the THz band also possesses much potential for a wide variety of terrestrial and space-borne applications, such as deep-space spectroscopy [4], medical imaging and diagnostics [5], pharmaceutical drug discovery and formulation [6], explosive and concealed weapon detection [7], non-destructive evaluation and quality control, and material characterization [8], to have a few. Compared to its neighboring microwave and optical bands which accommodate a plethora of applications, the THz band has
remained as the last underutilized frontier of the electromagnetic spectrum, primarily
due to the difficulties in generation and detection of RF power in the THz band.

Currently, THz systems rely on solid-state electronics- and optics-based technologies. Practical constraints of compactness and portability have been the driving force for solid-state electronics as the ultimate technology of choice for THz applications [9]. Unfortunately, as the cutoff frequencies for state-of-the-art diodes and transistors are pushed into the mmW and sub-mmW regime, a number of challenges arise in terms of the accurate modeling of these rapidly evolving technological processes. Considering the high cost of THz integrated device and nano-fabrication, it is desirable to achieve best performance in fewest number of design cycles. Achieving such design objectives is, however, dependent ultimately on the availability of reliable device models up to the operating frequency. As the minimum feature sizes of the most advanced devices is scaled down to nanometers to achieve highest speed, the impact of parasitic couplings, induced by electromagnetic (EM) interactions within the device structure, becomes comparable to intrinsic device behavior, particularly for THz frequencies. Therefore, accurate modeling of the overall device characteristics necessitates appropriate treatment of EM coupling effects. As demonstrated in this work, full-wave (FW) EM simulation tools can be utilized very conveniently to develop cost-effective solutions to the problem of device modeling at THz frequencies. Below, we review the contemporary semiconductor device technologies and the associated modeling techniques for THz applications.
1.1 Modeling of Semiconductor Devices for Terahertz Applications: Motivation, Challenges, and Objectives

Starting with the early research effort on remote sensing and radio astronomy in the second half of the 20th century, a wide range of two-terminal and three-terminal semiconductor device structures have been proposed, demonstrated, and utilized in THz applications. In what follows, we discuss the evolution, operating principles, and the current state of various solid-state diode and transistor structures, and the related modeling approaches developed in this dissertation.

1.1.1 Schottky Barrier and Heterostructure Backward Diodes

Since their invention in 1980s, surface-channel planar Schottky barrier diodes (SBDs) have been one of the most critical components for direct-detection and heterodyne THz transceivers [10] - [11]. The intrinsic nonlinearity of SBD current-voltage characteristic has been widely employed for frequency multiplication, and mixing, and for applications in imaging, chemical and biological spectroscopy, and communications [12]. With the aid of SBD-based frequency multipliers, the baseband signal can be upconverted to higher harmonic frequencies in THz band, where the optical sources are limited by cryogenic cooling requirements [13] - [14]. In addition, the received waveform around a THz range carrier can be downconverted by SBD-based mixers to a lower frequency band, where the baseband amplifiers are readily accessible for further processing [15].

The performance of SBD-based direct-detection sub-mmW receivers gradually degrades as the operating frequency is extended into THz band. This unavoidable drop
in performance holds true for all electronic components due to a variety of fundamental and practical limitations. Such detrimental effects can arise both from intrinsic device behavior (related to carrier lifetime and charge transport inside the device junction), and extrinsic factors comprising geometry-dependent parasitic coupling mechanisms within the diode structure and the surrounding environment. Therefore, it is essential to develop a more comprehensive understanding of device operation that takes intrinsic nonlinear aspects and electromagnetic (EM) interactions into consideration. Such EM couplings impact the high-frequency experimental performance of the device to fall far behind of theoretical expectations [16]. Accordingly, there is a continuous demand for accurate device models that can closely predict the device performance in the THz band.

GaAs has long been the most preferred material in SBD-based THz transceiver modules since it offers a powerful combination of remarkably high mobility and fairly large bandgap. Hence, a high Schottky barrier height ($\Phi_{B-GaAs} \simeq 0.85$ eV) that suppresses the reverse leakage current can be realized. GaAs-based SBDs have been demonstrated to achieve outstanding performance as THz mixers and frequency multipliers [17] - [18]. The major drawback limiting the performance of these devices, however, is that positive turn-on voltage of GaAs SBDs necessitates implementation of a DC biasing circuitry. The device needs to be operated at the optimum bias point so that maximum conversion efficiency can be attained. The differential junction resistance of such devices around zero-bias is on the order of teraohms. Such an excessively large junction resistance makes it practically impossible to deliver the downconverted RF signal to the following baseband amplifier block in the receiver chain. Applying forward bias to device decreases the differential junction resistance to
an acceptable level, but the biasing circuitry brings additional noise and reduces the receiver sensitivity [19]. Shot noise and flicker noise, which are linearly proportional to the applied bias current, further degrade the noise performance of the receiver. A promising alternative is provided by InGaAs/InP material system, which has lower effective Schottky barrier height ($\Phi_{B-\text{In}_{0.53}\text{Ga}_{0.47}\text{As}} \approx 0.25$ eV) compared to GaAs, and thereby enables realization of thermal noise-limited detectors without externally applied bias [20]. Zero-bias detection capability of InGaAs-based SBDs eliminates need for an extra biasing circuitry and the accompanying noise. This fundamentally improves noise performance and simplifies the architecture of direct detection THz receivers. Moreover, GaAs SBD-based mixers require relatively high local oscillator (LO) power to drive the device with large enough current level so that it is completely switched on and off to sample the RF signal at the LO frequency. Given the significant cost of generating high LO power from compact, portable and room-temperature solid-state sources at submillimeter-wavelengths [21], it is imperative to resort to techniques that alleviate LO power requirement and reduce the LO frequency by using subharmonically pumped mixers. Because the antiparallel-connected SBD-based subharmonic mixers necessitate a fairly complicated bias architecture, the low Schottky barrier height of InGaAs SBD-based mixers can reduce the required LO power in the absence of an external bias, relative to those based on GaAs [22]. In comparison with GaAs, the higher electron mobility of InGaAs also leads to reduced ohmic contact resistance, and lower mixer noise temperature at THz frequencies.

Zero-bias sub-mmW SBDs offer high responsivity and high cut-off frequency which are the two most important figures-of-merit for THz detection. The cut-off frequency sets the fundamental limit where the responsivity of the intrinsic device
drops by 3 dB [23]. Here, voltage responsivity refers to the amount of DC voltage created across the terminals of the nonlinear device per incident radiation power, and it is the foremost performance metric in direct detection THz receivers. Realization of high responsivity detector without externally applied bias-voltage requires strong nonlinearity in current-voltage ($I-V$) characteristic at zero bias. The degree of this nonlinearity near zero bias is quantified by the curvature coefficient $\gamma = \frac{(\partial^2 I/\partial V^2)/(\partial I/\partial V)|_{V=0}}{\partial I/\partial V|_{V=0}}$. As a measure of the second order nonlinearity normalized to the operating differential conductance level $(\partial I/\partial V|_{V=0})$, curvature coefficient determines the responsivity that can be anticipated from a square-law power detector [24]. The major shortcoming of regular zero-bias SBDs is that their strongly temperature dependent exponential current-voltage characteristic places a theoretical limit on the maximum achievable curvature $\gamma \leq kT/q = 38.5$ V$^{-1}$ at room temperature $T = 300$ K [25]. A promising alternative to circumvent such inherent performance limitations of SBDs is provided by zero-bias antimonide-based heterostructure backward diodes (Sb-HBDs) [26]. Curvature of these quantum mechanical tunneling-based devices, having pronounced nonlinearity near zero bias, exceeds the theoretical limits of thermionic emission-based SBDs. High curvature, high sensitivity, modest temperature dependence, and high cut-off frequency offered by HBDs make them a competitive substitute for SBDs in exceptionally low-noise THz detector and mixer design.

One of the primary objectives of this dissertation is to characterize electromagnetic coupling effects that restrict the THz detection and mixing performance of zero-bias surface-channel planar sub-mmW SBDs and HBDs. Conventional equivalent-circuit
approaches toward diode modeling have been centered around lumped-element approximations with the underlying assumption that the device is electrically-short even at mmW frequencies [27]. However, as the operating wavelength becomes comparable to physical dimensions of the device at sub-mmW frequencies, compact lumped-element perspectives become increasingly less accurate. In order to circumvent the shortcomings of such lumped-element equivalent circuits at high frequencies, we propose a distributed equivalent circuit model that can accurately reproduce the frequency response of electromagnetic interactions over a broader bandwidth covering the THz range. Based on this “parasitic-aware” distributed circuit model, we also present a novel multi-step systematic parameter extraction algorithm. The accuracy of the developed extraction methodology is established through extensive comparisons with the measured data reported in the literature.

1.1.2 Millimeter-Wave InP and GaAs HEMTs

Limitations due to atmospheric propagation in the THz band impose severe constraints on the potential solid-state technologies to meet fairly tight link budget specifications. In the course of propagation, electromagnetic waves suffer from spreading of energy and atmospheric weather conditions. The effect of energy spreading, which is also known as free space attenuation or path loss, is quantified by Friis transmission formula [28], according to which the received power is inversely proportional to the square of operating frequency and propagation distance. For a 10 m wireless communication link at 300 GHz, the free space attenuation amounts to 102 dB [29], which must be overcome by the underlying transceiver gain. Such extraordinarily large attenuation in THz band necessitates development of transmitters with very large
output powers and receivers with extremely low noise temperatures. Several different types of Schottky barrier diodes (SBDs) have been utilized in terahertz heterodyne receivers, serving as mixers and detectors for frequency multiplication [30], and envelope demodulation [31]. These two-terminal semiconductor devices are mounted individually into high-precision micromachined waveguide blocks, and cascaded in order to create functional units for THz transmitter and receiver realization. However, such communication systems are usually bulky, costly to manufacture, and time-consuming to assemble by hand. They also suffer from low repeatability and integration density, which obstruct their high-volume production. Besides, so as to integrate sophisticated signal-processing algorithms into RF front-ends through switching and amplification action, it is compulsory to use active semiconductor devices that can provide gain at the frequency of application [32]. The capability of deep submicron gate-length high electron mobility transistors (HEMTs) to deliver high output power at microwave and mmW frequencies coupled with very low-noise operation makes them ideally suited for applications such as satellite communications, radio astronomy, remote sensing, electronic warfare, and base stations [33]. An exceptionally high-gain and low-noise performance at millimeter-wavelengths have already been demonstrated by HEMTs based on InP and GaAs material systems [34] - [39].

Successful realization of HEMT-based integrated circuits relies solely on the availability of accurate device models beyond the frequency of interest [40] - [41]. As such, compact transistor models with wideband accuracy is a critical tool for reducing the number of design iterations in state-of-the-art microwave monolithic integrated circuit (MMIC) design. Significant discrepancies may arise between simulated and measured performance of integrated circuits unless accurate models of their constituent devices
are available. As the operation frequency is pushed into and beyond the mmW band, the device experiences a gradual degradation in its performance. This unavoidable drop in performance arises both from intrinsic device limitations, and extrinsic factors comprising parasitic resistance, capacitance, and inductance of interconnect metallization [42]. Therefore, careful selection of device size and layout becomes important, particularly when the operating frequency creeps closer to cutoff or maximum oscillation frequency of the device. Typically, the circuit models provided by integrated device manufacturers are not certified to account for the parasitic effects at high frequencies. Post-layout simulations for parasitic element extraction are also inadequate since they do not take into consideration the frequency dependent variation of extrinsic elements, particularly the access resistances [43]. Additionally, with the continuous downsizing of minimum transistor gate length to deep submicron range, the extrinsic parasitic elements start to play a more restrictive role in the overall gain and noise performance of the device. In this respect, new high-fidelity small-signal equivalent circuits to concurrently model the intrinsic and extrinsic device behavior becomes crucial for the design of high-performance RF front-end circuitry.

Although the high-frequency small-signal behavior of three-terminal devices can be completely described via the general two-port scattering ([S]), impedance ([Z]), or admittance ([Y]) matrices, the equivalent circuit models offer the following advantages:

i ) They allow for a deeper understanding of the device physics and analysis of microwave performance since the elements can be clearly associated with the physical structure of the device. The dependence of RF performance on device
topology can be estimated very conveniently, because the equivalent circuit model links device physical structure to its operation.

ii ) The variation of equivalent circuit parameters as a function of material processing techniques can be employed for characterization and comparison of different fabrication technologies [44] - [45].

iii ) The small-signal equivalent circuits extracted at multiple bias points are valuable for bottom-up construction of large-signal equivalent circuit models [46]. Hence, the accuracy of the large signal model is dependent ultimately on the accuracy of small-signal equivalent circuit, which should reliably account for the electrical and physical properties of the device.

iv ) The knowledge of small-signal equivalent circuit elements is indispensable for extraction of noise performance-related quantities [47].

v ) A physically representative equivalent circuit model enables extrapolation of RF performance at frequencies beyond the capability of available electronic measurement and characterization hardware.

The elements of small-signal equivalent circuits can be broadly divided into non-linear intrinsic components, and linear extrinsic parasitics [48]. The equivalent circuit extraction starts with the estimation of bias-independent extrinsic elements, which is followed by deembedding the contributions of parasitic elements from the measured data. Thereafter, the bias dependent intrinsic elements can be extracted as a function of the externally applied bias voltage. Extrinsic equivalent circuit is bias independent, and fundamentally depends on the physical geometry of the device including
interconnects, electrode structures, and probing pads. Thus, accurate determination of extrinsic parasitic components is imperative, since any erroneous calculation of extrinsic components will give rise to misinterpretation of intrinsic elements. Incomplete or exaggerated elimination of parasitic couplings is also likely to introduce errors into subsequently extracted intrinsic components. This error propagation among the steps of extraction methodology will eventually result in either an overestimation or an underestimation of the performance of the device under study. Therefore, accurate extraction of extrinsic equivalent circuit components is indispensable in terms of overall accuracy of the final small-signal equivalent circuit.

Over the last decade, small-signal equivalent circuit extraction techniques for RF transistor modeling have mainly relied on measurement-based characterization of fabricated devices [49] - [50]. A particular drawback of measurement-based modeling is that it is restricted to a limited number of modeled devices supplied by the manufacturer. This is because a separate device layout needs to be fabricated and characterized each time a geometric dimension is varied. This places considerable restrictions on RF circuit designer while choosing the correct device size and geometry to meet the required performance specifications. Besides, measurement-based transistor modeling becomes increasingly more challenging at mmW frequencies because of the uncertainties introduced by inaccurate deembedding of calibration structures and the detrimental crosstalk between the probes [51] - [52]. The $S$-parameter measurements are used to extract equivalent circuit components. However, there are usually more unknowns than the number of equations provided by such experimental data. In order to solve this ill-conditioned problem, optimization algorithms are often utilized, particularly for the extraction of extrinsic parasitics. Conventional extraction methods
to model extrinsics rely on measurement of a pinched-off cold-HEMT for estimation of capacitive elements, and measurement of a cold-HEMT with forward-biased gate terminal for retrieval of the remaining resistive and inductive components [53] - [55]. Thereafter, experimental data from each measurement is processed by using a numerical optimization tool. The major shortcoming of such optimization-driven methods is that their performance is very susceptible to starting parameter values. They are also very likely to converge to inaccurate local minima with physically meaningless values for the circuit elements. The foregoing observations concerning the limitations of such extrinsic device characterization call for a new modeling technique that can ensure modeling accuracy and design flexibility concurrently. Such a technique would also enable the RF circuit designer to choose different device sizes and geometries for achieving optimum performance without worrying about the potential modeling inaccuracy.

In light of the above shortcomings, another goal of this dissertation is to characterize the EM coupling effects that restrict the speed and noise performance of mmW HEMTs. A conventional lumped-element extrinsic equivalent circuit is adopted to capture the response of parasitic couplings in the low-microwave and mmW frequency range. For the first time, a new gate-to-drain mutual inductance component is incorporated into traditional parasitic network to model the magnetic flux linkage between the gate and drain electrodes. Based on this parasitic circuit model, we develop a novel multi-step parameter extraction algorithm, and validate its accuracy via comparisons between simulated, measured, and modeled frequency responses of the designed test structures up to 325 GHz.
1.1.3 Submillimeter-Wave GaN HEMTs

The aggressive scaling of transistor channel length down to submicron regime in HEMT technology has dramatically improved the RF performance of these devices beyond the limits that were previously considered unreachable. With the aid of recent advances in HEMT fabrication technologies, devices with record cutoff frequency characteristics coinciding with the sub-mmW frequency range are now realizable [56] - [60]. Even though the performance of state-of-the-art transistors is based on relatively conventional semiconductor heterostructures (GaAs/AlGaAs, and InGaAs/InP), such devices can achieve gain in the hundreds of gigahertz range. Nonetheless, they still suffer from low power density and early breakdown due to limitations pertaining to intrinsic material properties [61] - [62]. On the other hand, high data-rate mobile communications across long distances requires implementation of portable systems that can transmit large power using carrier frequency in the hundred gigahertz range to be able to find available bandwidth. Although shrinking the gate length is helpful in improving speed of the device, its power handling capability is degraded as the breakdown voltage gradually drops with the successive introduction of new technology nodes. In order to address this tradeoff between output power capacity and switching speed, extensive research has been undertaken to develop wide bandgap nitride-based semiconductors due to their inherently high breakdown voltage [63] - [65]. Nitride-based heterostructures are unique contenders for future cutting-edge all-electronic integrated systems due to their excellent material properties with regard to power, linearity, efficiency, speed, and robustness [66]. Especially, the gallium-nitride (GaN)-based HEMTs have drawn substantial interest because of
their various fundamental advantages over the existing technologies, including outstanding heat transfer characteristic, wider bandgap energy, operation at elevated temperatures, and exceptional high frequency performance [67] - [69].

Although initially targeted for high-power applications, AlGaN/GaN HEMTs have enjoyed phenomenal success in high-speed microwave and millimeter-wave circuit applications over the last ten years [70] - [72]. With the aid of latest developments in GaN HEMT technologies, including high-quality material growth, lithographic processing techniques, and device epitaxial structures; these devices can achieve high output-power and low-noise performance at millimeter-wavelengths, comparable those of conventional AlGaAs/GaAs HEMTs [73]. Further reduction of critical device dimensions, such as gate-length and drain-to-source spacing, has recently led to the realization of devices with current-gain ($f_T$) and power-gain ($f_{MAX}$) cutoff frequencies in excess of 160 GHz [74].

Reducing the gate length is one of the most effective methods to speed up HEMTs. However, lateral scaling of gate length beyond 50 nm is challenging in AlGaN/GaN material system due to the problems of gate leakage deterioration, current collapse with high RF input drive on the gate, and emergence of short-channel effects, which refer to the degradation of drain current modulation by the externally applied voltage to the gate terminal [75] - [77]. Furthermore, despite the technological maturity of AlGaN/GaN HEMTs due to their having been explored for more than a decade, there appeared growing evidence that the lattice-mismatch and piezoelectric polarization contributions restrict the reliability of these devices. The need to raise the bandwidth of GaN HEMT-based monolithic integrated circuits to better suit mmW frequency applications, required integration of thinner top barriers
into HEMT structure to maintain a favorable channel aspect ratio so as to suppress short-channel effects and enable higher cutoff frequencies simultaneously. Since the two-dimensional electron gas (2DEG) at the AlGaN/GaN hetero-interface suffers from surface depletion effects for very thin top barrier thickness [78], relatively newer ternary compound InAlN was considered for replacement of AlGaN barrier in order to enhance the current-drive capability and frequency performance of AlGaN/GaN HEMTs. It was shown through theoretical calculations that several times improvement in polarization-induced charge and resulting drain current can be accomplished by substitution of InAlN barrier into HEMT structure [79]. The feasibility of ultra-thin barrier lattice-matched InAlN/GaN HEMTs with spontaneous polarization was verified through scaling of barrier thickness down to below 10 nm, and accomplishment of cutoff frequencies above 200 GHz with 55 nm gate length [80]. Larger polarization discontinuity between InAlN top barrier and GaN channel allows InAlN/GaN HEMTs to exhibit several times larger polarization-induced sheet electron densities in 2DEG channel, and thus much increased drain current than traditional AlGaN/GaN-based structures. Therefore, InAlN/GaN-based HEMTs exhibit record power handling capabilities.

In order to push the RF performance of these devices even further, less than 50 nm gate length was needed with a barrier layer thickness of below 5 nm so that the structural aspect ratio of gate-length to gate-to-channel separation can be maintained for appropriate handling of short-channel effects like threshold-voltage shift, soft pinch-off, high subthreshold current, and increased output conductance [81]. However, excessive thinning of the top barrier severely compromised channel sheet carrier density and brought about a serious increase in the gate leakage current [82].
The reduction of gate leakage current by more than two orders of magnitude was manageable through the application of oxygen plasma treatment to InAlN surface, which was shown to be effective also in mitigation of the RF transconductance ($g_m$) collapse [83]. As a remedy to the short-channel impairments induced by extremely thin barrier, an InGaN back barrier was incorporated into InAlN/AlN heterostructure [84]. The back barrier structure provided a high degree of immunity against the onset of short-channel effects, by preventing the degradation related to drain-induced barrier lowering (DIBL), and significantly increasing the output resistance. The collective use of oxygen plasma treatment with InGaN back barrier guaranteed greater carrier confinement and modulation efficiency of the gate, which helped to improve the range of attainable cutoff frequencies to above 300 GHz, coinciding with the submillimeter-wave frequency band [85]. Nonetheless, such ultra-scaled devices with sub-50 nm gate length suffered from high contact resistance and high on-resistance because of the alloyed ohmic contacts and large drain-to-source spacing. This prevented them from ultimately reaching even higher cutoff frequencies.

To concurrently reduce the sheet access and contact resistances while keeping short-channel effects close to minimum, a low-damage gate-recess technology [86] was employed together with a short drain-to-source distance, and recessed source/drain ohmic contacts [87]. Additionally, replacement of high resistance alloyed ohmic contacts with lower resistance molecular beam epitaxy (MBE) regrown contacts was confirmed as a viable solution to extend the cutoff frequencies of these devices further into sub-mmW band [88]. Another important factor degrading the performance of these devices was the gate-to-source and gate-to-drain parasitic capacitances associated with the dielectric passivation of surface states in the access region, which was
introduced for elimination of DC-to-RF dispersion and current collapse. A number of techniques, including deposition of ultra-thin low-\textit{k} passivation dielectric, selective removal of passivation layer around the gate, and finally dielectric free passivation through plasma treatment [89] were shown to be effective in mitigating the impact of passivation layer-related capacitances, and further improving the cutoff frequency of these devices. During the last decade, and particularly the last few years, the switching speed of GaN HEMTs has been almost tripled. Such an impressive performance advancement has been accomplished through novel device scaling technologies such as manufacturable 20 nm self-aligned gate process [90], low-resistance heavily doped \textit{n}+\textit{-GaN}/2DEG ohmic contact regrown by MBE, a vertically scaled double-heterojunction HEMT epitaxial structure [91], and a lateral metal/2DEG Schottky contact. As a consequence of proportional downscaling of intrinsic and parasitic delays, the current state-of-the-art devices can achieve an ultra-high unity current-gain cutoff frequency ($f_T$) exceeding 450 GHz, with a simultaneous maximum oscillation frequency ($f_{MAX}$) of more than 440 GHz, while maintaining superior breakdown voltages [92]. This unprecedented combination of high-speed, high-breakdown, and low-noise performance offered by deeply-scaled GaN HEMTs are expected to provide unique opportunities in the design of submillimeter-wave transceiver building blocks, including power amplifiers with low harmonic distortion, LNAs with high dynamic range, oscillators with low phase noise, and mixers with high linearity.

In light of the above-mentioned physical limitations imposed by the device operation, further lateral shrinking of gate length to below 20 nm and vertical thinning of barrier thickness to less than a few nm are very challenging tasks. Therefore,
realization of power amplification beyond 1 THz barrier is contingent upon the development of innovative device paradigms. One recently proposed solution involves excitation of plasma waves in HEMTs in conjunction with current injection from the gate structure exhibiting negative differential conductance provided by an integrated resonant tunneling diode (RTD) [93]. Nonetheless, such new device topologies are still in their early stages of investigation, and reliable fabrication of them remains as an active research area.

Once an integrated device with a cutoff frequency extending into sub-mmW range has been realized, an immediate task is to utilize that device in the design of a MMIC operating in THz band. The foremost challenge here is that the appropriate operation of an extremely high-frequency MMIC is dependent ultimately on how closely the RF characteristics of that device are captured by the underlying equivalent circuit model. Unfortunately, as the technological processes evolve, a number of serious problems arise especially in the accuracy of existing device models. Since the technology being used to fabricate THz MMICs is prohibitively expensive, achievement of the desired circuit functionality in the fewest possible number of design iterations is a necessity. Unsatisfactory circuit performance or total failure are very likely scenarios that might be encountered unless utmost attention is paid to the proper characterization of the individual device.

As the operating frequency of the most recent MMICs is pushed continuously toward sub-mmW band [94] - [95], the device undergoes severe impairments in its performance. This inevitable degradation in performance originates from both intrinsic device behavior (related to the transit delay of charge carriers crossing the gate-modulated region), and extrinsic factors including the delay time associated
with the charging of parasitic capacitances and resistances of access metallization [96].

With the continued shrinking of minimum gate length to deep deca-nanometer dimensions, the intrinsic device channel capacitances are reduced proportionally, but the extrinsic parasitic components do not comply exactly with the linear downscaling rules. Therefore, the effect of geometry- and material-dependent parasitic couplings, caused by electromagnetic interactions within the device structure and surrounding environment, becomes increasingly more comparable with intrinsic device characteristics, as the more advanced transistor technologies with steadily decreasing feature size are developed [97] - [98]. In fact, reduction of parasitic coupling effects is indispensable for exploitation of full intrinsic device potential and further enhancement of extrinsic speed and noise performance in sub-mmW frequency band. Accordingly, utmost care must be exercised in selection of device size and layout particularly when the frequency of application approaches unity current-gain or power-gain cutoff frequencies of the device [99]. In this regard, availability of small-signal equivalent circuits that take into consideration the intrinsic and extrinsic device characteristics simultaneously becomes critical for reliable design of sub-mmW RF transceivers.

In traditional equivalent circuit extraction attempts for HEMT parasitic modeling, the power dissipation and electric/magnetic energy storage inside the device structure are represented by lumped resistive and capacitive/inductive elements [100] - [101]. The assumption underneath such lumped-element equivalent circuit approximations is that the device is electrically short even in the mmW frequency range. However, as the working frequency is moved into sub-mmW band, the physical dimensions of the device become comparable to the operating wavelength. As it is well-known from waveguide analysis, with HEMTs operating at frequencies beyond several hundreds of
gigahertz, the gate width to effective wavelength ratio becomes larger than 10% and the validity of those commonly-used lumped-element models becomes progressively more questionable. Instead, the device starts to exhibit distributed effects along the gate width direction [102]. Accordingly, the gate and drain electrodes start exhibiting transmission line characteristics terminated at the end with an open boundary condition. The distributed behavior is more easily noticeable in low-noise and high-gain amplifiers which typically require wide transistors to attain high current-drive and large transconductance.

The final goal of this dissertation is to characterize distributed field coupling effects that limit the performance of sub-mmW HEMTs in THz band. In order to capture the wave propagation effects along the device electrodes at THz frequencies, a distributed parasitic equivalent circuit model is proposed. The distributed nature of gate-to-drain inter-electrode coupling capacitance and mutual inductance are taken into consideration by interpreting gate and drain electrodes as a coupled three-line structure. Compared to lumped-element formulation, the suggested distributed equivalent circuit network can accurately reconstruct the frequency response of EM interactions over a much wider bandwidth, covering the THz range. In addition, we develop a novel multi-step systematic distributed parameter extraction procedure. The accuracy of the developed distributed-parameter extraction methodology is established through comparisons with simulations, measurements, and equivalent circuit models for the studied test structures up to 750 GHz.
1.2 Contributions and Organization of the Dissertation

As noted above, successful realization of radio-frequency integrated circuits (RFICs) in the fewest possible number of design cycles is contingent upon the availability of device models with high accuracy at the operating frequency. As the operating frequency is pushed continuously upward into sub-mmW band, the device experiences an inevitable drop in its performance due to intrinsic and extrinsic factors which include parasitic resistance, capacitance, and inductance of interconnect metallization. The impact of these material- and geometry-dependent parasitic couplings due to EM field interactions becomes comparable to that of intrinsic device in sub-mmW band. Accordingly, availability of small-signal equivalent circuits that take into account the intrinsic and extrinsic device behavior simultaneously becomes critical for design of high-performance RF front-end circuitry. The primary objective of this dissertation is to characterize the parasitic EM field coupling effects that restrain the speed and noise performance of sub-mmW zero-bias Schottky barrier diodes (SBDs) and high electron mobility transistors (HEMTs). Specifically, the key contributions of this dissertation are:

- Introduction of lumped- and distributed-element parasitic equivalent circuit models for sub-mmW SBDs and HEMTs in THz band.

- Development of novel multi-step systematic lumped and distributed model extraction procedures.

- Introduction of the gate-to-drain mutual inductance in lumped-element parasitic equivalent circuit of mmW HEMTs.
• Simulation-based and experimental verification of the accuracy and robustness of the suggested methodologies up to 750 GHz.

• Evaluation of the impact of parasitic couplings on detection/mixing performance of SBDs and speed/noise performance/power gain of HEMTs.

• Improvement of the conversion efficiency of a diode-based mixer via antenna-to-device conjugate impedance matching and device geometry optimization.

• Enhancement of speed, noise performance, and power gain of mmW and sub-mmW HEMTs through optimization of device layout.

The obtained results are critical for gaining physical insight into the geometry- and material-dependent electrically- and magnetically-driven power dissipation mechanisms of SBDs and HEMTs. Employment of full-wave simulation tools instead of fabrication and measurement of test structures is a cost-effective solution to the problem of device modeling in the sub-mmW frequency range. Finally, the proposed full-wave EM simulation-based characterization and performance optimization strategy will allow RF engineers to choose the optimum layout for diodes and transistors deployed in a wide range of transceiver building blocks, comprising low-noise amplifiers, voltage-controlled oscillators, power amplifiers, and mixers.

The remainder of the dissertation is organized as follows:

Chapter 2 starts with presenting the Schottky barrier diodes (SBDs) which represent one of the most successful room-temperature nonlinear devices used as mixers, detectors, and frequency multipliers in THz monolithic integrated circuits. The advantages of zero-bias detection capability in terms of receiver noise performance are discussed. The structure and constituent materials of zero-bias surface-channel planar
InGaAs-based SBDs are introduced. Physical phenomena underlying the electrical and magnetic parasitic coupling mechanisms within the diode structure and surrounding environment are summarized. Following this, a distributed parasitic equivalent circuit model, intended to achieve broadband device modeling accuracy from mmW to THz frequencies, is proposed. Based on this new distributed equivalent circuit model, a novel systematic parameter extraction algorithm is developed. The accuracy of the presented extraction routine is verified through extensive comparisons with the measured data reported in the literature. The drawbacks of traditional lumped-element approaches toward SBD modeling and the wideband accuracy provided by the suggested distributed model are exemplified through comparisons with full-wave simulated frequency response of the device. The adverse impact of EM interactions on diode detection and mixing performance is evaluated. The key parasitic components that are most critical to the performance are optimized with the objective of improving the device responsivity and noise equivalent power (NEP).

Chapter 3 proceeds with the full-wave EM simulation-based analysis and modeling of high electron mobility transistors (HEMTs), which are the most promising candidates for next generation microwave and mmW circuits in scientific, commercial, and military applications. A detailed description of the structure and geometry of a mmW HEMT with two gate fingers is provided. Physical phenomena giving rise to the electrical and magnetic coupling mechanisms within the transistor structure and the surrounding environment are summarized. Subsequently, a lumped-element parasitic equivalent circuit, to achieve broadband modeling accuracy at mmW frequencies, is proposed. Based on the new extrinsic equivalent circuit model, a novel multi-step
systematic parameter extraction algorithm is developed to extract circuit parameters using full-wave simulations. An analytical method is also proposed to extract the gate-to-drain mutual inductance, which creates an inductive feedback path from output to input at millimeter-wavelengths. The accuracy of the presented parameter extraction routine is verified through exhaustive comparisons between simulated, measured, and modeled frequency responses of the proposed test structures up to 325 GHz. The adverse effect of EM field couplings on transistor microwave performance is also evaluated. The main parasitic components are identified, and readily optimized through subsequent circuit analysis. Design guidelines are offered for optimum device layout selection to attain the utmost speed and noise performance.

Chapter 4 is devoted to the characterization of wave propagation effects along the device electrodes of sub-mmW HEMTs at THz frequencies. A distributed parasitic equivalent circuit, aimed at achieving broadband modeling accuracy in THz band, is proposed. The major geometry- and material- dependent electrically- and magnetically-induced power dissipation mechanisms of HEMTs are taken into consideration by the proposed distributed circuit model. Based on the new distributed parasitic circuit model, a novel multi-step systematic distributed parameter extraction algorithm is formulated. The accuracy of the suggested extraction procedure is validated through extensive comparisons between full-wave (FW) simulated, measured, and modeled frequency responses of the designed test standards up to 750 GHz. The impact of EM interactions on transistor speed and noise performance is evaluated. The key parasitic elements that are significantly detrimental to the microwave performance are determined, and conveniently optimized through subsequent
circuit analysis. Design guidelines are provided for optimum device layout selection to achieve the highest attainable speed and noise performance.

Finally, Chapter 5 provides a summary of major contributions, and discusses possible future research topics to extend current THz device modeling efforts.
Chapter 2: Distributed Circuit Models
for Submillimeter-Wave Schottky Diode Parasitics

Schottky barrier diodes (SBDs) have been a workhorse for all-electronic generation and detection of signals, effectively extending solid-state microwave technology into the mmW and sub-mmW bands. Applications in imaging, remote sensing, chemical and biological spectroscopy, communications, and radio astronomy [103] often rely on Schottky diodes either in monolithically fabricated form or mechanical whisker contact implementation. The moderately nonlinear current-voltage characteristic of these devices coupled with the low internal parasitics allow them to operate at extremely high frequencies, into the THz band. As such, the performance of optical sources in THz band, which typically require cryogenic cooling, can be replaced by electronic frequency multipliers that can upconvert the baseband signal to much higher harmonic frequencies.

As the material system, GaAs has long been the preferred choice in SBD-based heterodyne receiver implementations since it provides superior combination of high mobility and fairly large Schottky barrier height, that restrains the reverse leakage current [104]. However, the major weakness limiting the use of these devices as THz detectors is the positive turn-on voltage requirement, and thus the use of a DC biasing scheme to guarantee operation at the optimum bias point, where the conversion
Figure 2.1: Three-dimensional schematics illustrating the structure of a zero-bias surface-channel planar Schottky barrier diode (SBD). (a) Top view. (b) Side view.

efficiency is maximized. The differential junction resistance of these devices around zero-bias is in the range of teraohms, making it practically impossible to transfer the downconverted RF signal to the subsequent amplifier stage in the receiver chain. Differential junction resistance can be reduced by applying forward bias to the device, but this remedy comes at the expense of additional noise introduced by the biasing circuitry. A promising alternative is offered by InGaAs/InP material system, which has lower Schottky barrier height compared to GaAs, thereby permitting realization of thermal noise-limited detectors without externally applied bias [105]. Zero-bias operation of InGaAs-based SBDs significantly improves noise performance and simplifies the system architecture for direct detection THz receivers.

As the operating frequency is extended into THz band, all electronic devices experience a performance deterioration. This inevitable drop in performance originates
Figure 2.2: Layout of Schottky diode with coplanar ground-signal-ground (GSG) probing pads. Dimensions defining the geometry are $w_1 = 1.9$, $w_2 = 2.1$, $w_3 = 10$, $d_1 = 15$, $d_2 = 30$, $s_1 = 2.9$, and $s_2 = 8$. All dimensions are in $\mu$m.

from both intrinsic device behavior, as well as extrinsic factors including parasitic resistance, capacitance, and inductance of access metallization. To maximize performance, Schottky contact areas continue to be scaled down to sub-$\mu$m$^2$ range. With such downscaling, the effect of geometry- and material-dependent parasitic couplings, induced by electromagnetic interactions within the device structure, becomes progressively more comparable to intrinsic device behavior. Consequently, it is essential to develop a more comprehensive understanding of device operation that takes intrinsic nonlinear aspects and extrinsic coupling effects into consideration.
The foremost objective of this chapter is to characterize EM field behavior within the diode topology, as depicted in Fig. 2.1, that impacts THz detection and mixing performance of zero-bias surface-channel planar sub-mmW SBDs. Traditionally, equivalent circuit extraction for SBD parasitics has focused on lumped-element approximations [106]. This approach ignores signal propagation effects due to the distributed nature of device interconnect metallization as the operating frequency reaches the THz band. To account for such wave propagation characteristics, we propose a distributed equivalent circuit model to accurately reproduce the frequency response of the device over a much broader bandwidth covering the THz range. The elements of the proposed distributed circuit model are determined through a novel systematic multi-step parameter extraction algorithm. We demonstrate the validity and performance of the proposed methodology through comparisons with the measured data reported in the literature. The frequency response of new distributed and conventional lumped circuit models are compared using the full-wave EM simulations to clearly illustrate the drawbacks of lumped-element approach for SBD modeling at THz frequencies. Subsequently, the impact of EM couplings on THz detection and mixing performance of such diodes is evaluated. The effect of antenna-to-diode impedance mismatch on the responsivity of a THz sensor is also investigated. Design guidelines are provided for optimum device layout for highest responsivity and the lowest noise equivalent power (NEP).

2.1 Full-Wave Modeling of Diode Parasitics

Here, we present a detailed description of the diode geometry investigated in this chapter. The three-dimensional diode structure depicted in Fig. 2.1 is created and
simulated by using Ansoft High Frequency Structure Simulator (HFSS v15) [107]. Full-wave electromagnetic simulation results are then processed in Agilent Advanced Design System (ADS) [108] to extract distributed equivalent circuit parameters for this diode layout.

2.1.1 Zero-Bias Schottky Barrier Diode Structure

The InGaAs-based zero-bias surface-channel planar Schottky diode structure considered in our study is described in [109]. In such surface-channel planar diode topologies, the air bridge technology offers a mechanically stable connection between anode and cathode pads, while suppressing stray capacitances and eliminating the need for fragile non-planar whisker contacts [110] - [111]. The whiskerless device geometry is more robust against high vibration spaceborne applications, and can be easily
incorporated into planar monolithic integrated circuitry. Shown in Fig. 2.3 is a cross-
sectional view of SBD [112], that depicts the layers of constituent materials used in
device fabrication. Starting from the semi-insulating InP substrate, the diode layers
consist of a heavily doped buffer layer for ohmic contact, and lightly doped junction
epitaxial layer for Schottky contact formation. The $n^+$ InGaAs buffer layer is 1 $\mu$m
thick with a doping concentration of $N_{D}^{+} = 1.5 \times 10^{19}$ cm$^{-3}$. The active $n$- InGaAs
junction epitaxial layer has a doping concentration of $N_D = 2 \times 10^{17}$ cm$^{-3}$, with
0.08 $\mu$m thickness. For device passivation, a 0.1 $\mu$m thick SiO$_2$ layer is deposited
on n- InGaAs surface. Finally, the evaporated ohmic contact and interconnecting
metallization are assumed to be gold with 1 $\mu$m thickness.

As seen in Fig. 2.3, the lumped and distributed element representation of various
geometry-dependent parasitic coupling mechanisms can be inferred directly from the
device topology. Power dissipation within the diode structure and the surrounding
environment is modeled by the series resistance $R_S$, which is responsible for lower
conversion efficiency and higher noise temperature in THz mixers [113]. The series
resistance $R_S$ is comprised of all the resistances between the boundary of depletion
region in the junction epitaxial layer, and cathode ohmic-contact metallization. It in-
cludes the contributions of undepleted junction epitaxial layer resistance $R_{EPI}$, buffer
layer spreading resistance $R_{SPREADING}$, and cathode pad ohmic-contact resistance
$R_{CONTACT}$. The ohmic contact is assumed to be lossless in our study, in accordance
with the observation that ohmic contact resistance has no discernible impact on diode
series resistance both at DC and submillimeter-wavelengths [114]. In the course of
diode operation, RF current flows downward from the anode electrode through the
active epitaxial layer, spreads into the buffer layer, and gets collected at the cathode
terminal. Opposition to the current flow in the buffer layer is modeled as spreading resistance $R_{\text{SPREADING}}$, and spreading inductance $L_{\text{SPREADING}}$ [115], which are associated with power dissipation and magnetic energy storage, respectively. As the frequency increases, the nonuniform current flow in the buffer layer becomes constrained to within a few microns of the outer surface because of the skin and proximity effects. This increases the spreading impedance and severely impacts the figure-of-merit cut-off frequency of sub-mmW SBDs [116]. Electrical coupling between anode and cathode pads is modeled as distributed feedthrough capacitance $C_{\text{PP}}$, which is composed of series-connected infinitesimal capacitance components $\Delta C_{\text{PP}}$. Fringing field lines between air bridge and cathode ohmic-contact mesa are modeled as air bridge-to-pad capacitance $C_{\text{BP}}$, which consist of oxide capacitances $C_{\text{OX1}}$, $C_{\text{OX2}}$, and inter-electrode capacitance $C_{\text{EE}}$. Oxide capacitances $C_{\text{OX1}}$ and $C_{\text{OX2}}$ originate from the field coupling between air bridge and conductive epitaxial InGaAs layer through intervening SiO$_2$ passivation dielectric [117]. In addition, the dielectric leakage loss caused by finite conductivity of the semiconductor InP substrate and SiO$_2$ passivation layer is represented as distributed pad-to-pad conductance $G_{\text{PP}}$, and lumped air bridge-to-pad conductance $G_{\text{BP}} = G_{\text{OX1}} + G_{\text{OX2}}$. Distributed pad-to-pad conductance $G_{\text{PP}}$ is denoted by series-connected infinitesimal conductance terms $\Delta G_{\text{PP}}$. In order to account for dielectric loss in full-wave EM simulations, an effective complex-valued dielectric constant $\varepsilon_{re} = \varepsilon_r - j\sigma_d/\omega\varepsilon_0 = \varepsilon_r(1 - j\tan\delta)$ is specified, where $\varepsilon_r$ is relative permittivity, $\sigma_d = \omega\varepsilon_0\varepsilon_r\tan\delta$ is conductivity, and $\tan\delta$ is loss tangent of the dielectric [118]. By definition, loss tangent is the ratio of conduction current to the displacement current in a lossy dielectric, where the conduction current is interpreted as undesirable leakage reducing the quality factor of passive components.
in microwave monolithic integrated circuits (MMICs) [119]. Typically, air bridges of millimeter-wave (mmW) SBDs are treated as a series-connected lumped resistance $R_B$ and inductance $L_B$ pair, as shown in Fig. 2.4(b). They signify the conductive metallization loss and the magnetic flux linkage, respectively. However, as the frequency of operation approaches the THz regime, air bridge-to-semiconducting substrate capacitance $C_B$ in Fig. 2.3 starts to exhibit distributed behavior. As such, the air bridge must be modeled as a short-section of high-impedance transmission line. Here, we model the air bridge as an elevated coplanar waveguide (ECPW) [120], where the signal trace is suspended above the potentially-lossy substrate to combat the dispersion and substrate leakage at high frequencies. As shown in Fig. 2.3, the distributed model of air bridge is described in terms of per unit length (p.u.l.) resistance $R'_B$, inductance $L'_B$, and capacitance $C'_B$ parameters.

### 2.1.2 Full-Wave Electromagnetic Simulation Setup

The primary motivation behind the work presented here is to first identify the EM field coupling effects that limit detection and mixing performance of submillimeter-wave SBDs in THz frequency range. Then, a distributed equivalent circuit model is developed to quantify the adverse effects of parasitic elements on diode performance. Finally, physical dimensions of the diode can be varied to match the optimized parasitic element values with those obtained from full-wave simulation results. Accordingly, equivalent circuit should be regarded not only as a way of gaining insight into the device operation, but also as a practical way of improving the device performance, since circuit simulation involves several orders of magnitude less computational complexity than time-consuming full-wave EM simulation. Quasi-electrostatic simulation
Table 2.1: List of material parameters used as input to full-wave surface-channel SBD simulation.

<table>
<thead>
<tr>
<th>Material</th>
<th>Dielectric Constant $\epsilon_r$</th>
<th>Conductivity $\sigma$ (S/m)</th>
<th>Loss Tangent $\tan \delta$</th>
</tr>
</thead>
<tbody>
<tr>
<td>InP Substrate</td>
<td>12.5</td>
<td>--</td>
<td>0.006</td>
</tr>
<tr>
<td>Epitaxial InGaAs $N_D = 2 \times 10^{17}$</td>
<td>13.88</td>
<td>$2.07 \times 10^4$</td>
<td>--</td>
</tr>
<tr>
<td>Buffer InGaAs $N_D^+ = 1.5 \times 10^{19}$</td>
<td>13.88</td>
<td>$3.78 \times 10^5$</td>
<td>--</td>
</tr>
<tr>
<td>Passivation SiO$_2$</td>
<td>3.9</td>
<td>--</td>
<td>0.05</td>
</tr>
</tbody>
</table>

tools are computationally less demanding, but they assume that the simulated structure is electrically small compared to operating wavelength, and thus the EM fields can be treated as being frequency independent [121]. Due to its neglect of frequency-dependent EM field distribution inside the target volume, a quasi-static solver would not adequately serve our goal of capturing the variation of parasitic couplings, particularly the skin and proximity effects, as a function of frequency. The commercial full-wave electromagnetic solver of HFSS can account for the variation of EM fields as a function of frequency, and its theory is based on the finite element method [122] - [126]. It is worthwhile to mention that the proposed device structures can also be full-wave simulated by using alternative methods such as finite-difference time-domain method (FDTD) [127] - [129], and a similar study can be undertaken.
In order to examine the sources of high frequency losses in surface-channel planar SBDs, three-dimensional full-wave EM simulations are performed by placing the device into a coplanar waveguide (CPW) environment, as depicted in Fig. 2.2. The material properties for cathode ohmic-contact mesa, junction epitaxial layer, semi-insulating substrate, and passivation dielectric are listed in Table 2.1 [130] - [131]. Conductivity of the doped semiconductor material is calculated as \( \sigma = qN_D\mu_n \), where \( q \) is electron charge in C, \( N_D \) is doping density in cm\(^{-3}\), and \( \mu_n \) is electron mobility in cm\(^2\)/V·sec.

### 2.1.3 Distributed Equivalent Circuit Model for Surface-Channel Schottky Diodes

Conventional equivalent-circuit models for SBDs have been based on lumped element approximations, with the underlying assumption that the device is electrically short, even at mmW frequencies. Shown in Fig. 2.4(a) is the complete lumped-element equivalent circuit model of SBD [132], that includes intrinsic nonlinear elements as well as extrinsic linear EM coupling effects. Bias-dependent nonlinear elements are denoted by depletion layer differential junction resistance \( R_J = 1/(\partial I/\partial V)|_{V=0} \) and junction capacitance \( C_J = \partial Q_J/\partial V|_{V=0} \). Connected in series with these intrinsic nonlinear elements are series resistance \( R_S = R_{SPREADING} + R_{EPI} \) and inductance \( L_S = L_{SPREADING} \). The series resistance \( R_S \) is composed of undepleted junction epitaxial layer resistance \( R_{EPI} \), and cathode ohmic-contact mesa spreading resistance \( R_{SPREADING} \). As seen, the air bridge-to-pad capacitance \( C_{BP} = C_{OX1} + C_{OX2} + C_{EE} \) is in parallel with the preceding four components, and is likely to shunt out nonlinear junction at high frequencies. In series with these elements, there is also an air bridge inductance \( L_B \), connecting anode pad to the nonlinear
Figure 2.4: Equivalent circuit models of SBD for different frequency bands. (a) Conventional lumped-element model for microwave frequency range of up to a few tens of gigahertz. (b) Lumped-element model for mmW region that accounts for conductor and substrate losses. (c) Distributed model for submillimeter-wavelengths.
junction. This air bridge inductance $L_B$ presents a high impedance to the RF current flow as the frequency increases, and tends to open-circuit the nonlinear junction. Finally, the pad-to-pad feedthrough capacitance $C_{PP}$ is in shunt with all of aforementioned parasitic elements, and it further lowers the effective series transfer impedance $-1/Y_{12}(\omega)$ of the device at high frequencies. Anode and cathode pad extensions are approximated as lumped-element low-pass $\pi$-networks, consisting of pad capacitance $C_{PAL}$, and pad inductance $L_{PAL}$. Simplification of pad extensions as a lumped-element low-pass $\pi$-network is justifiable as long as physical length of the pad is less than one tenth of guided wavelength $\lambda_{EFF}$ at the highest anticipated frequency of operation [133].

The main drawback of lumped-element equivalent circuit shown in Fig. 2.4(a) is the omission of losses due to metallization with finite conductivity, and semiconductor substrate with finite resistivity. Detection and mixing performance of SBDs is limited by losses in cathode ohmic-contact mesa in microwave frequency range of up to several tens of gigahertz. As the working frequency is raised into the millimeter-wave band, depth of current penetration (skin depth) into conductor becomes smaller than the thickness of signal trace, and conductor losses increase proportionally. In addition, the ohmic losses in the semiconducting substrate also increase as the leaky dielectric becomes more conductive at higher frequencies [134]. In an effort to capture these losses at millimeter-wavelengths, commonly adopted lumped-element equivalent circuit in Fig. 2.4(a) is complemented by additional resistances and conductances to obtain the equivalent circuit shown in Fig. 2.4(b). Conductive metallization losses of air bridge, anode, and cathode pads are symbolized by $R_B$, $R_{PAL}$, and $R_{PCL}$, respectively. Ohmic losses pertaining to the electrically-induced conduction current in
the substrate are modeled by shunt anode and cathode pad conductances of $G_{\text{PAL}}$, and $G_{\text{PCL}}$. Pad-to-pad and air bridge-to-pad leakage current through semiconducting substrate and passivation dielectric are modeled by the feedforward conductance terms $G_{\text{PP}}$, and $G_{\text{BP}} = G_{\text{OX1}} + G_{\text{OX2}}$.

Once the physical lengths of the device exceed one tenth of the effective wavelength $\lambda_{\text{EFF}}$, the air bridge, semi-insulating substrate, and connecting pads need to be modeled as distributed components for precise estimation of attenuation and propagation delay. To overcome the limitations of the lumped-element approach at THz frequencies, we propose a new distributed equivalent circuit of SBD, shown in Fig. 2.4(c).
The low-pass π-network representation of contacting pads are replaced by transmission line counterparts in this distributed model. The electrical energy storage and power dissipation at the anode/cathode pad-to-air bridge transitions are described as shunt fringing capacitances (\(C_{PA}\) and \(C_{PC}\)) and conductances (\(G_{PA}\) and \(G_{PC}\)). We note that lumped-element representation of air bridge as a series-connected resistance \(R_B\) and inductance \(L_B\) in Fig. 2.4(b) neglects air bridge-to-ground capacitance \(C_B\) in Fig. 2.3, which has a distributed nature at submillimeter-wavelengths. To address this distributed aspect of air bridge, it is modeled as an elevated coplanar waveguide (ECPW) with characteristic impedance of \(Z_{0B}\) and propagation constant of \(\gamma_B\). In the lumped element equivalent circuit of Fig. 2.4(b), displacement and conduction currents through the semi-insulating substrate are modeled by parallel-connected pad-to-pad conductance \(G_{PP}\) and capacitance \(C_{PP}\). In order to take the wave propagation phenomena into account, a distributed equivalent circuit [135] in Fig. 2.5(b) is considered. In this distributed substrate network, substrate-to-ground infinitesimal capacitance-conductance terms of \((\Delta C_{SUB}, \Delta G_{SUB})\) are included to accurately capture the attenuation and propagation characteristics of the substrate. The distributed substrate model is integrated into the proposed sub-mmW SBD equivalent circuit of Fig. 2.4(c) as a transmission line with characteristic impedance of \(Z_{0SUB}\) and propagation constant of \(\gamma_{SUB}\).

The distributed equivalent circuit analysis of the SBD is carried out using the standard π-network topology shown in Fig. 2.6. This π-network configuration is based on admittance matrix representation of a reciprocal two-port network, with
the series branch replaced by effective series transfer impedance

\[ Z_{\text{SERIES}}(\omega) = \frac{-1}{Y_{12}(\omega)} = R_{12}(\omega) + jX_{12}(\omega), \quad (2.1) \]

where \( R_{12}(\omega) \) and \( X_{12}(\omega) = \omega L_{12}(\omega) \) are effective series transfer resistance and reactance, respectively. Distributed characteristic of SBD at THz frequencies is directly recognized as a drop in effective series transfer resistance \( R_{12}(\omega) \), which can become even negative depending on the frequency range of interest [136]. This nonmonotonic variation of \( R_{12}(\omega) \) as a function of frequency can not be reproduced by the lumped-element equivalent circuit depicted in Fig. 2.4(b).

2.1.4 Model Extraction Using a Series of Test Structures

The characterization methodology developed in this chapter generates the frequency-dependent parasitic elements of SBD by partitioning the entire equivalent circuit into multiple subcircuits in four steps. In each step, an increasingly more complicated layout of the diode structure is simulated. Direct parameter extraction and highly effective optimization tools are employed concurrently for the subsequent analysis. A lumped parameter extraction procedure for mmW region was presented.
Figure 2.7: Cross-sectional views of full-wave simulation scenarios for distributed SBD equivalent circuit model extraction. The material assignments of each step are indicated by the labels placed next to each figure. (a) Step I: SBD without air bridge. (b) Step II: Short-circuited SBD. (c) Step III: Open-circuited SBD.
in a recent study [106]. To maintain the modeling accuracy in THz band, here we develop a distributed parameter extraction scheme, incorporating conductive metallization and semiconducting substrate losses. Figure 2.7 shows the cross-sectional descriptions of SBD test structures for each simulation scenario, strategically chosen to expedite the extraction process. The corresponding distributed equivalent circuit models for each simulation step are depicted in Fig. 2.8. In the first step, only the contact pads of the diode, without the air bridge, are simulated to identify the extent of electrical coupling through semiconducting substrate. In the second step, the air bridge is introduced, while epitaxial and buffer layers of the diode are replaced by perfect electric conductors. The purpose of this short-circuited SBD scenario is to extract the distributed behavior of the air bridge as the frequency increases into the sub-mmW range. In the third step, the air bridge is kept in place, however the metal via at the tip of the air bridge is removed to open-circuit the nonlinear junction. The objective of this layout is to extract the capacitance across and the leakage through the passivation dielectric. In the fourth and final step, the overall diode structure is simulated without any modification to inspect the behavior of spreading resistance and reactance of cathode ohmic-contact mesa as a function of frequency. The corresponding cross-sectional view of SBD with lossy cathode ohmic-contact mesa is shown in Fig. 2.3. In the first three steps, the junction epitaxial and buffer layers are replaced by perfect electric conductors to isolate the parasitic coupling of these layers. The anode pad is modeled as a tapered transmission line, while cathode pad is treated as a traditional CPW section. Anode and cathode contact pad extensions are simulated individually and deembedded from the above cases via successive application of $Y$- and $Z$-matrix transformations [137]. The characteristic impedance
Figure 2.8: Distributed equivalent circuit models of Schottky diode for different steps of parasitic extraction. (a) Step I: SBD without air bridge. (b) Step II: Short-circuited SBD. (c) Step III: Open-circuited SBD. (d) Step IV: SBD with lossy cathode ohmic-contact mesa.
$Z_C(\omega)$ and propagation constant $\gamma(\omega) = \alpha(\omega) + j\beta(\omega)$ of the pads are calculated by substituting the full-wave simulated $S$-parameters into [138]

$$Z_C(\omega) = Z_0 \left( \frac{(1 + S_{11} + S_{21})(1 + S_{11} - S_{21})}{(1 - S_{11} - S_{21})(1 - S_{11} + S_{21})} \right)^{1/2} \tag{2.2}$$

$$\gamma(\omega) = \frac{2}{l} \tanh^{-1} \left( \frac{(1 + S_{11} - S_{21})(1 - S_{11} - S_{21})}{(1 - S_{11} + S_{21})(1 + S_{11} + S_{21})} \right)^{1/2}, \tag{2.3}$$

where $Z_0 = 50\, \Omega$ is the reference impedance. Subsequently, the per-unit-length (p.u.l.) quantities $R'$, $L'$, $C'$, and $G'$ of the lossy transmission line are derived by invoking the classical equations

$$R' + j\omega L' = Z_C\gamma \tag{2.4}$$
$$G' + j\omega C' = \frac{\gamma}{Z_C}. \tag{2.5}$$

The effective dielectric constant $\epsilon_{\text{EFF}}(\omega)$, that describes the dispersion (frequency-dependent) characteristic of the transmission medium, is related to the phase constant $\beta(\omega)$ by

$$\epsilon_{\text{EFF}}(\omega) = \left( \frac{\beta}{\omega \sqrt{\mu_0 \epsilon_0}} \right)^2. \tag{2.6}$$

Substrate-related parasitic capacitances and conductances are extracted from the SBD simulation without the air bridge in Step I, with the equivalent circuit depicted in Fig. 2.8(a). After deembedding the contact pads, the low-frequency $Y$-matrix representation of the equivalent circuit in Fig. 2.5(a) can be evaluated to estimate the lumped pad parasitics using the following relations

$$C_{\text{PP}} = -\frac{\text{Im}\{Y_{12}\}}{\omega}, \quad G_{\text{PP}} = -\frac{\text{Re}\{Y_{12}\}}{\omega} \tag{2.7}$$
$$C_{\text{PAL}} = \frac{\text{Im}\{Y_{11} + Y_{12}\}}{\omega}, \quad G_{\text{PAL}} = \text{Re}\{Y_{11} + Y_{12}\} \tag{2.8}$$
$$C_{\text{PCL}} = \frac{\text{Im}\{Y_{22} + Y_{12}\}}{\omega}, \quad G_{\text{PCL}} = \text{Re}\{Y_{22} + Y_{12}\}. \tag{2.9}$$
At THz frequencies, $S$-matrix representation of the pad-related parasitic elements shown in Fig. 2.5(b) can be inserted into (2.2) and (2.3) to compute the characteristic impedance $Z_{\text{SUB}}(\omega)$ and propagation constant $\gamma_{\text{SUB}}(\omega)$ of the distributed substrate network, which can be written as

$$Z_{\text{SUB}}(\omega) = ((G_{\text{PP}} + j\omega C_{\text{PP}}) (G_{\text{SUB}} + j\omega C_{\text{SUB}}))^{-1/2}$$

(2.10)

$$\gamma_{\text{SUB}}(\omega)l_{\text{SUB}} = \sqrt{\frac{G_{\text{SUB}} + j\omega C_{\text{SUB}}}{G_{\text{PP}} + j\omega C_{\text{PP}}}}.$$  

(2.11)

Next, the transmission line parameters of distributed air bridge are extracted from the short-circuited SBD simulation in Step II, with the equivalent circuit shown in Fig. 2.8(b). Initially, pad related parasitics obtained in Step I are factored out from the short-circuited SBD simulation using

$$[Y_{\text{AIR BRIDGE}}] = [Y_{\text{SHORT}}] - [Y_{\text{PADS}}],$$

(2.12)

where $[Y_{\text{PADS}}]$ is admittance matrix representation of distributed substrate network of Fig. 2.5(b), and $[Y_{\text{AIR BRIDGE}}]$ is the $Y$-matrix description of air bridge-related parasitic couplings. Thereafter, we convert $[Y_{\text{AIR BRIDGE}}]$ to $[S_{\text{AIR BRIDGE}}]$, and the resulting $S$-parameters are used to compute characteristic impedance $Z_{\text{BP}}(\omega)$ and propagation constant $\gamma_{\text{B}}(\omega)$ of the air bridge using (2.2) and (2.3). The passivation layer conductance $G_{\text{BP}}$ and the capacitance $C_{\text{BP}}$ are calculated from the open-circuited SBD simulation in Step III, which results in the equivalent circuit shown in Fig. 2.8(c). To this end, we must correct the results of the open-circuited SBD simulation to account for the influence of pad parasitics. This is done by subtracting $[Y_{\text{PADS}}]$ from $[Y_{\text{OPEN}}]$, yielding $[Y_{\text{A}}] = [Y_{\text{OPEN}}] - [Y_{\text{PADS}}]$. Subsequently, the auxiliary admittance matrix $[Y_{\text{A}}]$ is converted into transmission ($ABCD$)-matrix $[T_{\text{A}}]$, which is premultiplied by the inverse of the transmission-matrix representation.
\[ [T_{\text{AIR BRIDGE}}] \text{ of air bridge to arrive at the passivation layer transmission matrix} \]

\[ [T_{\text{PASSIVATION}}] = [T_{\text{AIR BRIDGE}}]^{-1} [T_A]. \quad (2.13) \]

Doing so, passivation dielectric conductance and capacitance can be calculated as

\[ G_{BP} = \text{Re} \left\{ \frac{1}{T_{12}^{\text{PASSIVATION}}} \right\}, \quad (2.14) \]
\[ C_{BP} = \text{Im} \left\{ \frac{1}{T_{12}^{\text{PASSIVATION}}} \right\} / \omega. \quad (2.15) \]

The remaining series resistance \( R_S = R_{\text{SPREADING}} + R_{\text{EPI}} \) and inductance \( L_S = L_{\text{SPREADING}} \) of junction epitaxial layer and cathode ohmic-contact mesa are extracted from lossy SBD simulation in Step IV, whose equivalent circuit is shown in Fig. 2.8(d).

First, the effect of pad parasitics is removed from lossy SBD simulation data by subtracting \( [Y_{\text{PADS}}] \) from \( [Y_{\text{LOSSY}}] \), resulting in \( [Y^B] = [Y_{\text{LOSSY}}] - [Y_{\text{PADS}}] \). Deembedding of the pad parasitics is followed by transforming the intermediate admittance matrix \( [Y^B] \) into the transmission matrix \( [T^B] \). Similarly to the open-circuited SBD case, the intermediate transmission matrix \( [T^B] \) is premultiplied by \( [T_{\text{AIR BRIDGE}}]^{-1} \) to obtain a new transmission matrix \( [T^C] = [T_{\text{AIR BRIDGE}}]^{-1} [T^B]. \) Afterwards, this auxiliary transmission matrix \( [T^C] \) is converted back into admittance matrix \( [Y^C] \), and admittance matrix representation \( [Y_{\text{MESA}}] \) of series resistance and inductance is evaluated using

\[ [Y_{\text{MESA}}] = [Y^C] - [Y_{\text{PASSIVATION}}]. \quad (2.16) \]

Using (2.16), the series resistance \( R_S \) and inductance \( L_S \) of junction epitaxial layer and cathode ohmic-contact mesa can be expressed as

\[ R_S = \text{Re} \left\{ \frac{-1}{Y_{12}^{\text{MESA}}} \right\}, \quad (2.17) \]
\[ L_S = \text{Im} \left\{ \frac{-1}{Y_{12}^{\text{MESA}}} \right\} / \omega. \quad (2.18) \]
Figure 2.9: Pad-related capacitance and conductance terms. (a) $C_{PAL}$, $C_{PP}$, and $C_{PCL}$. (b) $G_{PAL}$, $G_{PP}$, and $G_{PCL}$.

The initial guesses obtained from equations (2.2)-(2.18) serve as high quality starting values for further numerical optimization through least squares error fitting procedure. With the aid of these analytical expressions, numerical optimization avoids convergence toward inaccurate local minimums. The accuracy of the proposed distributed-element extraction routine is evaluated by calculating the normalized error metric between the full-wave simulated and modeled $S$-parameters of the device [139]. The average percentage error is less than 10% for the simulation scenarios listed in Fig. 2.7.

2.1.5 Verification of the Proposed Distributed Circuit Model via Full-Wave EM Simulation

To verify the accuracy of the proposed distributed sub-mmW SBD model in the 10-1100 GHz band, we consider a representative diode structure, with the dimensions given in Fig. 2.2. Components of the lumped model of Fig. 2.4(b) and the distributed
model of Fig. 2.4(c) are extracted concurrently, to clearly demonstrate the limitations of lumped-element approach for THz frequency operation. Shown in Figs. 2.9(a) and 2.9(b) are the parasitic capacitance and conductance terms associated with contact pad-to-air bridge transition and pad-to-pad fringing field lines. For the device shown in Fig. 2.2, the extracted pad-to-pad capacitance is $C_{PP} \simeq 0.16 \, \text{fF}$. When the signal trace width and signal-to-ground spacing of CPW, represented by the parameters $w_3$ and $s_2$ in Fig. 2.2, are set to 30 µm and 21 µm respectively, the estimated pad-to-pad capacitance rises to $C_{PP} \simeq 1.3 \, \text{fF}$, which is closer to the measured value of $C_{PP} \simeq 3 \, \text{fF}$ in [140] for a diode having a similar geometry. The discrepancy is due to wider contact pads and much shorter pad-to-pad separation of the measured device. The extracted values of the substrate conductances are in close agreement with complex-valued permittivity relation of $G(\omega)/C(\omega) = \sigma_d/\epsilon_0\epsilon_r = \omega \tan \delta$ [141].

The transmission line parameters of contact pads and air bridge, obtained from the short-circuited SBD simulation of Step II, are shown in Figs. 2.10(a) and 2.10(b). As noted before, we considered the air bridge as a short section of high impedance elevated coplanar waveguide (ECPW). Suspending the signal trace of CPW above the substrate by surface micromachining reduces per unit length shunt capacitance remarkably, which results in realization of coplanar waveguides with very high characteristic impedance. The extracted characteristic impedance of the air bridge is $Z_{0B} \simeq 145\, \Omega$. In contrast, a conventional CPW on InP substrate with the same dimensions would result in $\sim 85\, \Omega$ characteristic impedance. Effective dielectric constant of the cathode contact pad is estimated to be $\epsilon_{C,\text{EFF}} \simeq 6.2$, and that of air bridge is extracted as $\epsilon_{B,\text{EFF}} \simeq 1.9$, which is much less than that of cathode contact pad due to lower per-unit-length shunt capacitance of elevated air bridge above the substrate.
Such lower effective permittivity leads to higher phase velocity \( v_p = c/\sqrt{\epsilon_{\text{EFF}}} \), and lower propagation delay, which are very critical features in terms of accomplishing high-speed intra-chip communication. Attenuation constants of air bridge and cathode contact pad are also shown in Fig. 2.10(b). The extracted attenuation constant of cathode contact pad at 1 THz is \( \alpha_C \simeq 12.9 \text{ dB/mm} \), which is comparable to the experimental value of \( \alpha_C \simeq 14.3 \text{ dB/mm} \) reported in [142]. Note that the attenuation of the air bridge is significantly lower than that of cathode contact pad, even though the air bridge is expected to have larger conductor loss due to narrower signal trace. The reason can be more easily explained by noting that the propagation constant expression for a transmission medium with low-loss substrate is given as

\[
\gamma(\omega) = \alpha(\omega) + j \beta(\omega) = j \omega \sqrt{L'C'} \left( 1 - j \frac{R'}{2\omega L'} \right).
\]  \hspace{1cm} (2.19)

According to (2.19), a transmission line with lower per unit length capacitance also has less attenuation. This is why CPW with an elevated signal trace offers transmission with lower insertion loss relative to conventional CPW, thus is the preferred method for realizing the Schottky contact. The capacitance and conductance of passivation SiO\(_2\) layer, calculated from open-circuited SBD simulation in Step III, are shown in Figs. 2.11(a) and 2.11(b) for the 750-1100 GHz band. The extracted air bridge-to-pad capacitance is \( C_{BP} \simeq 1.7 \text{ fF} \) with SiO\(_2\) passivation dielectric, and \( C_{BP} \simeq 0.85 \text{ fF} \) without passivation dielectric. The estimated value of \( C_{BP} \simeq 0.85 \text{ fF} \) in the absence of passivation is within the experimental \( C_{BP} \) range of 0.7-3 fF specified in [143]. It is lower than the measured value of \( C_{BP} \simeq 1.6 \text{ fF} \) in [144] for a diode having a similar geometry, but wider and thicker air bridge metal, as well as larger overlapping area between air bridge and the underlying conductive epitaxial layer.
Figure 2.10: Air bridge and cathode contact-pad characteristic impedance and attenuation constant. (a) $Z_{0B}$, and $Z_{0C}$. (b) $\alpha_B$, and $\alpha_C$.

To validate the accuracy of the proposed distributed model, the contact pad- and passivation layer-related parasitic components retrieved in the first three steps of parasitic extraction algorithm are substituted into open-circuited SBD equivalent circuit of Fig. 2.8(c). Shown in Figs. 2.12(a) and 2.12(b) are the comparison of simulated and modeled $S$-parameters for open-circuited SBD simulation in Step III of the extraction process. As observed from reflection coefficient plot of Fig. 2.12(a), semi-insulating InP substrate and low-loss passivation SiO$_2$ layer offer almost ideal open-circuit at lower end of the simulated frequency band. As the frequency increases, pad-to-pad capacitance $C_{PP}$ and air bridge-to-pad capacitance $C_{BP}$ provide a current flow path with lower reactance between anode and cathode electrodes. More importantly, the inductance of the contact pads and the air bridge creates a series-resonance with air bridge-to-pad capacitance $C_{BP}$ in sub-mmW band. Beyond this series-resonance, the impedance looking into each port turns from being capacitive into inductive. This
Figure 2.11: Air bridge-to-contact pad capacitance and conductance in the presence and absence of passivation dielectric. (a) $C_{BP}$. (b) $G_{BP}$.

example clearly illustrates how dramatically the parasitic couplings can alter the frequency response from mmW to sub-mmW bands. As clearly demonstrated in Fig. 2.12(a), the frequency response of the device is much more accurately reproduced by the proposed distributed model over a much wider bandwidth, while the lumped-model is unable to capture propagation delay and the corresponding phase shift across the terminals of the device in the sub-mmW region. As seen, the frequency response of the lumped-element equivalent circuit starts to deviate from full-wave simulations beyond $\sim 250$ GHz, where the electrical length of the device is $\sim \lambda_{EFF}/10$. The same observation also holds true for the transmission coefficient $S_{21}^{OPEN}$, as depicted in Fig. 2.12(b). As seen, $S_{21}^{OPEN}$ increases from zero transmission at low frequency toward full transmission in sub-mmW regime. The continuously increasing transmission coefficient $S_{21}^{OPEN}$ is clearly a result of the air bridge-to-pad capacitance $C_{BP}$, which provides an RF current flow path with steadily decreasing capacitive reactance as the operation frequency increases into the sub-mmW band.
The series resistance and inductance of the junction epitaxy and cathode ohmic-contact mesa are calculated from lossy SBD simulation in Step IV, using the equivalent circuit shown in Fig. 2.8(d). The series resistance \( R_s = R_{SPREADING} + R_{EPI} \) plotted in Fig. 2.13 exhibits dramatic increase as a function of frequency due to current crowding in heavily doped buffer layer of the device. Here, current crowding refers to the constriction of high-frequency electric current within the outer boundary of the conductor, and it is a direct consequence of two magnetically-induced power dissipation mechanisms (skin and proximity effects [145]). Considering the skin effect, the time-varying magnetic field created by the current flow in a conductor induces eddy currents in the conductor itself, which in turn causes current redistribution with more emphasis on the conductor surface. This nonuniform current flow increases the effective resistance of the conductive wire above the value that would apply for a uniform flow across the wire cross section at low frequency [146]. In addition to the skin effect, the time-varying magnetic field produced by the neighboring current-carrying conductor further aggravates the nonuniform current distribution of the primary conductor, which is described as a proximity effect. In the case of surface-channel planar SBD configuration, spreading resistance of the buffer layer is subject to contributions from both skin effect-eddy currents as well as proximity effect-eddy currents. The proximity effect has a significant impact since the time-varying magnetic field of the air bridge current penetrates into the buffer layer to further push the current flow toward the surface. Therefore, the eddy currents due to skin and proximity effects superimpose to increase the spreading resistance of the device very sharply in sub-mmW band.
To verify the correlation of extracted spreading resistance using experimental low-frequency data from literature, we simulated the diode structure at the lower end of mmW region, ranging from 10 to 60 GHz. Skin depth of the buffer layer was found to be $\delta = (\pi f \mu_0 \sigma)^{-1/2} = 3.3 \mu m$ at 60 GHz, which is still larger than the thickness of buffer layer. This means that the current flow through the cathode ohmic-contact mesa is roughly uniform across its cross-section in this frequency range, and the retrieved spreading resistance values can be safely extrapolated to DC. Thus, the estimated DC series resistance is $R_S = R_{\text{SPREADING}} + R_{\text{EPI}} \simeq 4.9 \Omega$, which is in reasonable agreement with the measured value of 5.5 $\Omega$ reported in [109]. Adding specific ohmic contact resistance, and resistance of interconnect metallization to the extracted $R_S$ is supposed to give a closer match between full-wave simulation and measurement.

One of the key figures-of-merit for evaluating the high frequency performance of SBDs is the intrinsic cut-off frequency $f_C = (2\pi R_S C_J)^{-1}$, which is a direct indication of the conversion loss that can be anticipated from an SBD-based mixer design [147]. Cut-off frequency has traditionally been calculated by substituting the series resistance $R_S$ value obtained from DC current-voltage ($I-V$) or low-frequency $S$-parameter measurements. According to this convention, the reported cut-off frequency of the device being studied in this chapter is 3.9 THz [109]. In view of the rapidly increasing series resistance depicted in Fig. 2.13, calculation of cut-off frequency based on DC series resistance gives rise to an overly optimistic performance prediction. For instance, substituting the series resistance extracted from full-wave simulation yields cut-off frequency of less than 1 THz, which is far below the value predicted by using DC series resistance $R_S$. This example clearly demonstrates that
Figure 2.12: Comparison of simulated and modeled $S$-parameters for open-circuited SBD simulation in Step III of parasitic extraction. (a) Reflection coefficient $S_{11}^{\text{OPEN}}$. (b) Transmission coefficient $S_{21}^{\text{OPEN}}$.

neglecting the high-frequency losses leads to an overestimation of device performance for sub-mmW operation.

Concerning the series inductance $L_S = L_{\text{SPREADING}}$ of cathode ohmic-contact mesa shown in Fig. 2.13, the extracted frequency dependent variation is observed to be the opposite of that exhibited by the series resistance. The total inductance of a conductive line consists of external and internal inductances. The external inductance arises from the magnetic energy storage outside the conductor, and it is approximately frequency independent. The internal inductance is related to the magnetic energy stored inside the conductor due to the penetration of magnetic flux into the conductor itself. The degree of magnetic field penetration into the conductor is quantified by the skin depth, which is inversely proportional with the square root of the operating
frequency. Thus, the attenuation of magnetic flux penetration into the conductor with increasing frequency due to eddy currents results in lower internal inductance, and thereby lower total inductance [148]. In addition to the skin effect-eddy currents, proximity effect-eddy currents induced by the magnetic field interaction with the neighboring conductor produce their own magnetic flux that opposes the incident original flux, in accordance with the Lenz’s law. This negative mutual magnetic flux coupling weakens the magnetic field of the primary conductor, and further lowers the overall magnetic energy storage and the corresponding inductance [149] - [152]. Contrary to the decreasing spreading inductance with frequency, the spreading reactance $X_S = \omega L_S$ increases steadily, and becomes an open-circuit to the nonlinear junction as the operating frequency reaches the sub-mmW region.
To further illustrate the accuracy of the proposed distributed model, the entire set of parasitic coupling effects retrieved throughout the four steps of parasitic extraction algorithm are used to construct the lossy SBD equivalent circuit of Fig. 2.8(d). Plotted in Figs. 2.14(a) and 2.14(b) are comparisons of full-wave simulated and equivalent circuit $S$-parameters for lossy SBD simulation in Step IV of the parameter extraction process. Similarly to the case of open-circuited SBD simulation, the proposed distributed model achieves the desired broadband accuracy, while the lumped model fails to account for propagation delay and the corresponding phase shift across the terminals of the device in sub-mmW band. The sharply varying impedance profile as a function of frequency can be better monitored by looking at effective series transfer impedance $Z_{\text{SERIES}}^{\text{LOSSY}}(\omega)$ of the device, as shown in Fig. 2.15.
For a device with electrically small dimensions, traditional lumped-element equivalent circuit approximation of Fig. 2.4(b) is clearly justifiable, and one would observe constantly increasing effective series transfer resistance $R_{12}(\omega)$ and reactance $X_{12}(\omega)$ with respect to frequency. Nevertheless, as the device dimensions become comparable to the effective wavelength, the rate of increase in $X_{12}(\omega)$ and $R_{12}(\omega)$ gradually drops, and the slope eventually becomes negative for electrically large devices. This non-monotonic variation of effective series transfer impedance with respect to frequency is a direct implication of the distributed characteristic of the device, and it is very clearly illustrated by the impedance behavior plotted in Fig. 2.15. Even though the effective series transfer resistance $R_{12}(\omega)$ becomes negative in THz range, the real part of the input impedance looking into anode and cathode terminals is still positive across the whole frequency band due to passive nature of the parasitic couplings.

### 2.2 Optimization of SBD Layout for Improved Terahertz Detection

A critical goal of developing the presented equivalent circuit is to improve device performance through a formal design optimization. For this purpose, the intrinsic small-signal equivalent circuit elements are assumed to be available. The distributed extrinsic parasitic couplings extracted by using the full-wave EM simulation-based method are then incorporated into the overall circuit model to predict performance in the mmW and sub-mmW band. The device considered here is a zero-bias heterojunction backward diode (HBD) [153], which offers superior low-noise detection performance compared to conventional SBDs. Following the extraction of intrinsic and extrinsic subcircuits, the complete set of linear and nonlinear components are assembled together in the comprehensive distributed diode equivalent circuit model.
Figure 2.15: Effective series transfer impedance $Z_{\text{LOSSY SERIES}}(\omega) = R_{12}(\omega) + jX_{12}(\omega)$ of lossy SBD in Step IV of parasitic extraction.

shown in Fig. 2.4(c) to assess the electrical performance of the diode as a detector of THz radiation using a suitable antenna structure to capture the incident THz energy.

The two most important figures of merit (FoMs) for evaluating the RF performance of diodes are the responsivity ($\beta_V$) and the noise equivalent power (NEP). Voltage responsivity ($\beta_V$) is the amount DC voltage generated across the terminals of the device per unit incident radiation power, and it is the primary measure of performance in direct detection THz receivers. Noise equivalent power (NEP) characterizes the minimum detectable RF power the device can reliably detect under a unit signal-to-noise ratio (SNR=1). When the detector is operated without external bias, thermal noise dominates the bias current-dependent shot noise and flicker noise. As such, the optimum thermal-noise limited NEP can be analytically calculated from
NEP = \sqrt{\frac{4kT}{R_d} / \beta_{V,OPT}} [154]. For responsivity calculation, two different scenarios are usually considered. These are matched and unmatched responsivities, where the unmatched responsivity (\beta_V) is subject to impedance mismatch between standard 50\Omega RF source and diode input impedance. For this scenario, only a fraction of incident RF power is delivered to the nonlinear junction and the remainder is reflected back to the source. In the second case, the unmatched responsivity is compensated for the detrimental effect of reflected power to extract matched, or optimum, responsivity (\beta_{V,OPT}). Achieving matched responsivity (\beta_{V,OPT}) requires the utilization of an ideal lossless matching network between 50\Omega RF source and complex-valued input impedance of the detector. A more practical solution that also supports compact monolithic integration is to tailor the design of THz antenna such that its input
Figure 2.17: Matched and unmatched responsivity and noise equivalent power (NEP) in the presence and absence of passivation dielectric. (a) Responsivity. (b) NEP.

impedance is conjugately matched to that of the detecting device [155]. Such an impedance-matched THz detector configuration is illustrated in Fig. 2.16 [16].

The three key parasitic components, that are detrimental to the diode performance are the air bridge inductance $L_B$, the air bridge-to-pad capacitance $C_{BP}$, and the pad-to-pad capacitance $C_{PP}$. As seen in distributed equivalent circuit model of Fig. 2.4(c), the air bridge-to-pad capacitance $C_{BP}$ is connected directly in parallel with the series-connected nonlinear junction and the spreading impedance. Thus, this capacitance introduces a short-circuit path that bypasses the nonlinear intrinsic device. To evaluate this impact of $C_{BP}$ on detection performance, matched and unmatched responsivity and NEP of the diode are computed in the presence and absence of passivation SiO$_2$ dielectric, as depicted in Figs. 2.17(a) and 2.17(b). The selected HBD exhibits unmatched responsivity of $\beta_V \approx 1.9 \text{kV/W}$ and matched responsivity of $\beta_{V,OPT} \approx 4.2 \text{kV/W}$ at 1 THz. As seen, almost 2 times improvement in THz responsivity is realizable through antenna-to-detector conjugate impedance
matching. The calculated matched responsivity is also in line with the measured optical responsivity reported in [156]. Measured optical responsivity is still lower than this theoretically calculated value, because of the additional losses involved in quasi-optical measurement setup. The effects of reflections from hemispherical lens, polarization mismatches, imprecise beam collimation by objective lens, misalignment of parabolic mirrors, and imperfect antenna-to-detector conjugate impedance matching are ignored in the above calculation [157].

As seen in Fig. 2.17(a), elimination of passivation dielectric mitigates the effect of air bridge-to-pad capacitance $C_{BP}$, and thereby enables another $\sim 1.5$ times enhancement in the calculated responsivity of HBD at 1 THz. Since a complete removal of passivation layer is not recommended due to electrical reproducibility concerns, reducing its thickness and raising the air bridge above the passivation layer might still be helpful in terms of reducing $C_{BP}$ to an acceptable level. In summary, close to 10 dB improvement in conversion efficiency of an HBD-based single-ended passive mixer design at 1 THz is realizable through conjugate impedance matching and suppression of $C_{BP}$. The noise equivalent power (NEP) is plotted in Fig. 2.17(b), where the minimum projected NEP at 1 THz in the presence of passivation dielectric is $\sim 5.8$ pW/Hz$^{1/2}$. This value is again comparable to the range of experimental values specified in [158]. The calculated optimum NEP is still somewhat lower because our analysis assumes perfect conjugate impedance matching, and the selected HBD yields higher curvature and responsivity compared to zero-bias SBDs. It should, however, be emphasized that accurate measurement of optimum NEP at
submillimeter-wavelengths is a challenging task, since precisely estimating the portion of incoming RF power that is delivered to the terminals of the detecting device is prone to experimental errors [159].

A critical dimension of sub-mmW diode geometry that can be very easily adjusted to optimize the signal reception performance is the length of air bridge. Fine-tuning the length of air bridge has two competing results in terms of the air bridge inductance $L_B$ and the pad-to-pad capacitance $C_{PP}$ parasitics. The air bridge inductance $L_B$ is directly proportional to the length of air bridge, while pad-to-pad capacitance $C_{PP}$ is inversely proportional. As the length of air bridge increases, increasing air bridge reactance ($\omega L_B$) becomes an open-circuit across the nonlinear junction in sub-mmW band. Likewise, the decreasing capacitive reactance ($1/\omega C_{PP}$) tends to

Figure 2.18: Matched responsivity and NEP without passivation dielectric as a function of air bridge length.
short-circuit the nonlinear junction, albeit to a lesser extent. The converse statement applies when the length of air bridge decreases. Accordingly, the impact of air bridge length on diode detection performance is not quite obvious, and is better optimized through a numerical procedure to make a conclusive decision. Shown in Fig. 2.18 are matched responsivity and NEP of the HBD as a function of air bridge length. In case of a very short air bridge length, the pad-to-pad capacitance $C_{PP}$ exhibits a remarkable increase, and effectively short-circuits the nonlinear junction in sub-mmW region. In case of a very long air bridge length, the air bridge inductance $L_B$ increases proportionately, and effectively open-circuits the nonlinear junction in THz band. These two opposite trends give rise to the concave-shaped responsivity curve plotted in Fig. 2.18. Through careful optimization of air bridge length, the matched responsivity of the detector can be further improved by more than $\sim$1.5 times, which translates into a $\sim$4 dB improvement in conversion efficiency of an HBD-based single-ended passive mixer design. Depending on the frequency range of operation, a different air bridge length needs to be chosen for maximum responsivity. For this example, an air bridge length of 20 µm would be a reasonable choice for broadband operation in the WR1.0 waveguide band.

2.3 Conclusion

We proposed a new distributed equivalent circuit model for sub-mmW SBDs that can accurately capture the parasitic effects of EM interactions within the device structure. Additionally, we have developed a novel model extraction methodology based on simulations of 4 successive device layouts. Direct analytic extraction and numerical optimization methods have been employed in cooperation for the subsequent
analysis. The accuracy of the recommended extraction procedure was demonstrated through extensive comparisons with the experimental results provided in the literature. The proposed distributed model and the previously-studied lumped-element circuit model have been analyzed concurrently to clearly demonstrate the shortcomings of lumped-element approach toward SBD modeling at sub-mmW frequencies. The distributed model has been verified to achieve the desired broadband accuracy, while the lumped model has failed to account for propagation delay and the corresponding phase shift across the terminals of the device in the THz band. The device has been observed to exhibit distributed effects once its physical length has reached one tenth of the effective wavelength $\lambda_{\text{EFF}}$. We have also illustrated that the cut-off frequency calculations ignoring high-frequency losses result in very optimistic prediction of device performance in sub-mmW band. In order to evaluate the adverse effects of electromagnetic couplings on detection and mixing performance, intrinsic nonlinear junction resistance and capacitance of an HBD have been incorporated into the the extracted distributed parasitic equivalent circuit model, allowing a complete circuit analysis. The three key parasitic components are the air bridge inductance $L_{\text{B}}$, air bridge-to-pad capacitance $C_{\text{BP}}$, and pad-to-pad capacitance $C_{\text{PP}}$, which are the most detrimental to device performance. We demonstrated through a full-wave EM simulation-based study that the conversion efficiency of an HBD-based single-ended passive mixer design at 1 THz can be improved by more than $\sim 10$ dB via conjugate impedance matching and optimization of air bridge-to-pad capacitance. Fine-tuning the length of air bridge has also been shown to provide another degree of freedom that can potentially bring further performance enhancement. The calculated optimum responsivity and NEP values have been observed to be in reasonable agreement
with the measured data in the literature. Finally, utilization of full-wave EM simulation tools instead of fabrication and measurement of test structures provides a cost-effective solution to the challenges of diode modeling in the sub-mmW frequency range.
Chapter 3: Methodology for Lumped-Element Parasitic Equivalent Circuit Extraction of HEMTs

Availability of accurate device models is of utmost importance in realizing radio-frequency (RF) integrated circuits with fewest number of fabrication iterations [160]. For instance, simple and accurate circuit models for complex topologies is critical for the design of state-of-the-art wideband microwave monolithic integrated circuits (MMICs). Although equivalent circuit modeling has been a workhorse in RFIC and MMIC design, these conventional models can not replicate the underlying physics and the consequent performance degradation in the millimeter-wave (mmW) band. The aforementioned performance drop is due to both intrinsic device behavior, and extrinsic factors comprising parasitics of interconnect metallizations [161]. Perhaps more importantly, the impact of material- and geometry-dependent parasitic couplings due to electromagnetic (EM) interactions within the device structure and the surrounding environment becomes comparable to that of intrinsic device behavior at millimeter-wavelengths. In this respect, high-fidelity small-signal equivalent circuits which account for the intrinsic and extrinsic device physics are necessary for effective design of high-performance mmW and sub-mmW integrated circuits.

In accordance with the underlying semiconductor and electromagnetic behavior, components of the small-signal equivalent circuits can be grouped into nonlinear
intrinsic elements and linear extrinsic parasitic couplings [162]. Equivalent circuit extraction algorithms begin with estimation of bias-independent extrinsic elements. Subsequently, bias dependent intrinsic components are determined as a function of the externally applied bias voltage. It is clear that an accurate extraction of extrinsic parasitic elements is of utmost importance, since any error in the calculation of extrinsic components results in inaccurate determination of intrinsic elements.

Over the past decade, small-signal equivalent circuits of RF transistors have been primarily studied using measurement-based characterization of fabricated devices [163] - [165]. However, this time-consuming and expensive procedure can only be applied to a limited number of device models, typically supplied by the manufacturer. This is due to the need for fabrication and characterization of a separate device when a geometric dimension within the device topology is varied. Another

Figure 3.1: Three-dimensional schematic illustrating the structure of a millimeter-wave high electron mobility transistor (HEMT): (a) Top view, (b) Side view.
Figure 3.2: Layout of an on-wafer two-finger HEMT with coplanar ground-signal-ground (GSG) probing pads, and the corresponding circuit representation. Dimensions defining the geometry are $w_1 = 20$, $w_2 = 4$, $w_3 = 2$, $d_1 = 10$, $d_2 = 28$, $d_3 = 9$, $s_1 = 14$, $s_2 = 2$, and $s_3 = 2$. All dimensions are in $\mu$m.

issue related to the equivalent circuit extraction using measured $S$-parameters relates to the ill-conditioning of the problem since there are more unknowns in the circuit model than the number of equations provided by the experimental data [166]. In order to circumvent this issue, numerical optimization algorithms must be employed particularly for extrinsic equivalent circuit extraction. A major shortcoming of such optimization-driven methods is that their performance is very susceptible to starting parameter values. They are also very likely to converge to inaccurate local minima with physically-meaningless values for the elements of the equivalent circuit. In light of the aforementioned shortcomings, a new modeling technique which can concurrently ensure modeling accuracy and design flexibility is needed. Here, we develop such a procedure based on full-wave computational models of three-terminal devices.
Commercial full-wave electromagnetic simulators have recently been used for the analysis of extrinsic parasitic couplings for lumped-element equivalent circuit extraction [167]. Nonetheless, the authors still used numerical optimization for extraction of parasitic components based on simulation data, which did not provide enough number of equations for precise determination of the extrinsic circuit components. Consequently, a fully analytic parasitic extraction procedure that guarantees physically representative set of parasitic component values is still lacking.
The primary purpose of this chapter is to characterize the EM coupling effects that impact the performance of mmW HEMTs. Shown in Fig. 3.1 is the three-dimensional topology of a millimeter-wave HEMT considered in this chapter [168]. A conventional lumped-element extrinsic equivalent circuit network is employed to predict the behavior of parasitic couplings in the low-microwave and mmW frequency range. Although we start with the conventional circuit model, a new gate-to-drain mutual inductance $L_{MGD}$ is introduced into the traditional parasitic network to model the magnetic flux linkage between gate and drain electrodes. Based on this improved circuit, we present a novel systematic multi-step parameter extraction procedure to determine the components of the equivalent circuit. The accuracy and robustness of the new methodology are validated through comprehensive comparisons between simulated, measured, and modeled frequency responses of the suggested test structures up to 325 GHz.

Using this new equivalent circuit, the impact of EM interactions on microwave performance of HEMTs is also evaluated. Subsequently, the device layout is optimized with the objective of enhancing RF performance, and design guidelines are provided for device topology to achieve the optimum operation (highest cutoff frequency) and the lowest noise level.

### 3.1 New Extrinsic Equivalent Circuit for HEMTs

Here, we briefly describe the HEMT geometry and the associated electromagnetic mechanisms that impact device parasitics. A three-dimensional HEMT structure illustrated in Figs. 3.1 and 3.2 was developed and analyzed by using Ansoft High
Figure 3.4: Lumped-element small-signal equivalent circuit model of HEMT describing extrinsic parasitic coupling phenomena.

Frequency Structure Simulator (HFSS v15) [107]. Subsequently, the full-wave electromagnetic simulation results are used in Agilent Advanced Design System (ADS) [108] to extract the external lumped-element parasitic equivalent circuit components of the HEMT, as shown in Fig. 3.4.

### 3.1.1 Device Structure and Geometry

The cross-sectional view of the HEMT topology shown in Fig. 3.3 illustrates the layers of constituent materials employed in device fabrication, as well as the lumped-element representation of various geometry- and material-dependent parasitic coupling mechanisms. In this simple equivalent circuit, the electrical coupling between gate, drain, and source contacting pads is modeled as pad-to-pad capacitances of
$C_{\text{PGS}}, C_{\text{PGD}}, \text{and} C_{\text{PDS}}$. Power dissipation within the three-terminal structure and surrounding environment is modeled as series-connected gate, drain, and source electrode resistances of $R_{\text{EG}}, R_{\text{ED}}, \text{and} R_{\text{ES}}$, respectively. These access resistances become increasingly more detrimental for microwave-frequency gain and noise performance as transistor channel length is scaled down to deep submicrometer regime [169]. Due to the skin and proximity effects, the nonuniform current flow through electrode metallization will gradually be constrained more to the outer surface, as the frequency is swept from low-microwave to millimeter-wave (mmW) region. This, in turn, increases the resistance of the device electrodes, and causes a serious degradation in the unity current-gain and power-gain cutoff frequencies of mmW HEMTs. Energy storage in the magnetic field around current-carrying gate, drain, and source electrodes is modeled as electrode inductances of $L_{\text{EG}}, L_{\text{ED}}, \text{and} L_{\text{ES}}$. These inductances tend to pose high impedance against the RF current flow at millimeter-wavelengths. In addition, the fringing electric fields among gate, drain, and source electrodes are represented as inter-electrode capacitances of $C_{\text{EGS}}, C_{\text{EGD}}, \text{and} C_{\text{EDS}}$, and the dielectric leakage loss arising from the finite conductivity of the semiconductor substrate is modeled as pad-to-pad conductances of $G_{\text{PGS}}, G_{\text{PGD}}, \text{and} G_{\text{PDS}}$. Similarly, the conduction current among gate, drain, and source electrodes due to the lossy substrate is modeled as inter-electrode conductances of $G_{\text{EGS}}, G_{\text{EGD}}, \text{and} G_{\text{EDS}}$.

Furthermore, in order to account for the effect of shunt dielectric leakage loss in full-wave EM simulations, an effective complex-valued relative permittivity $\epsilon_{\text{re}} = \epsilon_i - j\sigma_d/\omega\epsilon_0 = \epsilon_i(1-j\tan \delta)$ was used, where $\epsilon_i$ is dielectric constant, $\sigma_d = \omega\epsilon_0\epsilon_i\tan \delta$ is conductivity, and $\tan \delta$ is loss tangent of the substrate. Perhaps most importantly, we introduce, for the first time, a gate-to-drain mutual inductance of $L_{\text{MGD}}$ to model the
magnetic flux linkage between gate and drain electrodes due to their close proximity. In the mmW band, magnetic field coupling between gate and drain electrodes creates feedback path from the output back to the input port. This feedback path, in addition to that created by the gate-to-drain coupling capacitance $C_{EGD}$, may give rise to instability of the device and impact the high frequency performance [170].

3.1.2 Lumped-Element Equivalent Circuit Model of HEMT External Parasitics

The complete small-signal lumped-element equivalent circuit model of HEMT proposed here is shown in Fig. 3.4. This improved model includes both extrinsic linear parasitic coupling effects as well as intrinsic nonlinear subcircuit as a general nonreciprocal two-port network. Details of the bias-dependent intrinsic two-port network will be discussed later in detail. As seen in Fig. 3.4, inter-electrode capacitance-conductance pairs $(C_{EGS}, G_{EGS})$, $(C_{EGD}, G_{EGD})$, and $(C_{EDS}, G_{EDS})$ are connected in parallel with the nonlinear intrinsic device. At extremely high frequencies, these capacitive elements are likely to shunt out the intrinsic transconductance $G_{M}^{INT}$ which provides the gain mechanism of the device. In series with the parallel combination of intrinsic device and inter-electrode capacitance-conductance pairs, there are also resistance-inductance pairs of gate, drain, and source electrodes, which are denoted as $(R_{EG}, L_{EG})$, $(R_{ED}, L_{ED})$, and $(R_{ES}, L_{ES})$, respectively. These inductances present a high impedance to the incoming and outgoing RF current flow as the frequency increases, and tend to open-circuit the intrinsic device. In addition to these device electrode-related parasitic interactions, the pad-to-pad feedforward capacitance-conductance pairs $(C_{PGS}, G_{PGS})$, $(C_{PGD}, G_{PGD})$, and $(C_{PDS}, G_{PDS})$ are in parallel with all of the above-mentioned parasitic components. They also create an
alternative low-impedance RF current flow paths between device terminals. Finally, the gate-to-drain mutual inductance of $L_{MGD}$ is also incorporated into the proposed lumped-element parasitic equivalent circuit, for the first time, to capture the magnetic field coupling and the consequent inductive crosstalk between gate and drain electrodes at high frequencies.

### 3.1.3 Extraction of the External Parasitic Circuit Elements Using Representative Test Structures

As seen in Fig. 3.4, the extrinsic parasitic circuit of the HEMT involves 19 elements. As noted before, these circuit elements are often determined by fitting the measured response of the device to the expected circuit behavior. Although this procedure can also be applied using simulation data, instead of measurements, the large number of circuit elements that need to be concurrently determined makes the problem rather sensitive and unreliable. Here, we develop a multi-step algorithm for determining the frequency-dependent parasitic components of the HEMT by strategically dividing the extrinsic equivalent circuit into a number of subcircuits which can be easily fit to experimental or simulation data. Starting with a significantly simplified layout where the gate and drain electrodes are completely removed from the original device topology, as shown in Fig. 3.5(a), we propose a 6-step process to isolate and identify each parasitic in the extrinsic circuit. Figure 3.5 illustrates the 6 proposed layouts of the algorithm. The corresponding lumped-element equivalent circuit models for each of the test layouts are also given in Fig. 3.6.

In the first step, only the contact pads of the HEMT without device electrodes are simulated (or measured) to quantify the degree of electric field coupling and the dielectric leakage through the semiconducting substrate. The pad layout and the
Figure 3.5: Layouts of the on-wafer test standards designed for HEMT lumped-element parasitic equivalent circuit extraction. (a) PADS. (b) THRU1. (c) THRU2. (d) SHORT1. (e) SHORT2. (f) OPEN.
Figure 3.6: The proposed lumped-element extrinsic equivalent circuit representations of HEMT for different steps of parasitic extraction. (a) PADS. (b) THRU1. (c) THRU2. (d) SHORT1. (e) SHORT2. (f) OPEN.

associated equivalent circuit are shown in Figs. 3.5(a) and 3.6(a). As seen, only 6 parasitic elements are needed to capture the response of the layout in Step I.
In the second step, drain pad and electrode are removed, while the gate electrodes are connected to the CPW center conductor on the drain side. The layout of the THRU1 standard, and the corresponding equivalent circuit are given in Figs. 3.5(b) and 3.6(b), respectively. As seen, this symmetric double-gate structure introduces the gate electrode resistance $R_{\text{EG}}$ and inductance $L_{\text{EG}}$. In addition, the inter-electrode capacitance-conductance pair of $(C_{\text{EGS}}, G_{\text{EGS}})$ is included to account for the electric field coupling and the dielectric leakage loss between gate and source electrodes.

In the third step, the gate pad and electrodes are removed, while the drain electrode is connected to the CPW centerline at the gate side (THRU2 standard), as shown in Figs. 3.5(c) and 3.6(c). The basic aim of using this symmetric double drain configuration is to capture the behavior of drain electrode resistance $R_{\text{ED}}$ and inductance $L_{\text{ED}}$ as a function of frequency.

In the fourth step, the drain electrode is removed, while the gate electrodes are short-circuited to the source electrodes which are connected to CPW ground. The layout of this standard (SHORT1), and the corresponding equivalent circuit are illustrated in Figs. 3.5(d) and 3.6(d), respectively. The objective of this step is to isolate the source electrode resistance $R_{\text{ES}}$ and inductance $L_{\text{ES}}$ that impact the RF performance severely, since the corresponding impedance behaves as a series feedback degeneration impedance.

In the fifth step, the drain electrode is introduced again, while the gate electrodes stay short-circuited to the source electrodes (SHORT2 standard), as shown in Figs. 3.5(e) and 3.6(e). The main goal of the fifth step is to capture the effect of gate-to-drain mutual inductance $L_{\text{MGD}}$ and the associated inductive feedback on the impedance characteristic of the device.
Finally, in the sixth step, the overall structure of the HEMT is simulated (or measured) without any modification to identify the fringing inter-electrode capacitances and conductances. The layout of this OPEN standard, and the related equivalent circuit are given in Figs. 3.5(f) and 3.6(f). We note here that the OPEN standard corresponds to a pinched-off cold HEMT ($V_{GS} < V_P$, and $V_{DS} = 0$ V) in conventional HEMT characterization, which suppresses channel conductivity and pushes the device into a passive condition for the determination of extrinsic parasitic network elements [171] - [172].

3.1.4 Theoretical Analysis of Extrinsic Parameter Extraction Algorithm

With the above-mentioned strategic choices for 6 standard layouts, we next proceed to construct the HEMT equivalent circuit using EM simulations (or measured S-parameters). In Step I, the pad-to-pad capacitances and conductances are determined from the simulation of pad layout of Fig. 3.5(a). We apply a simple linear regression fit using the low-frequency Y-matrix representation of the equivalent circuit shown in Fig. 3.6(a) to calculate the lumped parasitics using the following matrix relation for the 2-port π-network:

$$
[Y_{PADS}] = \begin{bmatrix}
(G_{PGS} + j\omega C_{PGS}) + (G_{PGD} + j\omega C_{PGD}) & -(G_{PGD} + j\omega C_{PGD}) \\
-(G_{PGD} + j\omega C_{PGD}) & (G_{PDS} + j\omega C_{PDS}) + (G_{PGD} + j\omega C_{PGD})
\end{bmatrix}.
$$

In Step II, the gate resistance $R_{EG}$ and gate inductance $L_{EG}$ are obtained from the simulation of THRU1, with the equivalent circuit provided in Fig. 3.6(b). Initially, the pad-related parasitics extracted in Step I are deembedded the from full-wave

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simulation results of THRU1 standard using

\[
[Y^{\text{GATE}}] = [Y^{\text{THRU1}}] - \begin{bmatrix}
\frac{(G_{\text{PGS}} + j\omega C_{\text{PGS}})}{+(G_{\text{PGD}} + j\omega C_{\text{PGD}})} & \frac{-(G_{\text{PGD}} + j\omega C_{\text{PGD}})}{+(G_{\text{PGD}} + j\omega C_{\text{PGD}})} \\
-\frac{(G_{\text{PGD}} + j\omega C_{\text{PGD}})}{+(G_{\text{PGD}} + j\omega C_{\text{PGD}})} & \frac{(G_{\text{PGS}} + j\omega C_{\text{PGS}})}{+(G_{\text{PGD}} + j\omega C_{\text{PGD}})}
\end{bmatrix}, \tag{3.2}
\]

where

\[
[Y^{\text{GATE}}] = \begin{bmatrix}
\frac{(G_{\text{EGS}} + j\omega C_{\text{EGS}})/2}{+(R_{\text{EG}} + j\omega L_{\text{EG}})^{-1}} & \frac{-(R_{\text{EG}} + j\omega L_{\text{EG}})^{-1}}{+(R_{\text{EG}} + j\omega L_{\text{EG}})^{-1}} \\
-\frac{(R_{\text{EG}} + j\omega L_{\text{EG}})^{-1}}{+(R_{\text{EG}} + j\omega L_{\text{EG}})^{-1}} & \frac{(G_{\text{EGS}} + j\omega C_{\text{EGS}})/2}{+(R_{\text{EG}} + j\omega L_{\text{EG}})^{-1}}
\end{bmatrix} \tag{3.3}
\]

is the admittance matrix representation of the gate electrode-related parasitic couplings. Subsequently, least squares error fit to the elements of \([Y^{\text{GATE}}]\) can be applied to identify the associated gate-electrode parameters. It is essential to recognize that the lower diagonal entry of the second term on the right hand side of (3.2) is different from that of \([Y^{\text{PADS}}]\) expressed in (3.1). This is because the HEMT layout is not symmetric. The gate and drain pads have different geometries, and hence slightly different capacitive coupling with the source pad which is connected CPW ground.

In Step III, the resistance \(R_{\text{ED}}\) and inductance \(L_{\text{ED}}\) of the drain electrode are computed from the simulation of THRU2 standard based on the equivalent circuit seen in Fig. 3.6(c). Similarly to Step II, the simulation data of THRU2 test structure is first rearranged to cancel the influence of pad parasitics and obtain auxiliary admittance matrix \([Y^{\text{DRAIN}}]\), which accounts for the admittance matrix representation of drain electrode-related parasitics. Then, a linear curve fitting is applied to the elements of \([Y^{\text{DRAIN}}]\) to determine the drain electrode-related parasitic quantities.

In Step IV, source electrode resistance \(R_{\text{ES}}\) and inductance \(L_{\text{ES}}\) are found from the simulation of SHORT1 standard using the equivalent circuit in Fig. 3.6(d). To
do so, simulation results of SHORT1 standard is first corrected for the effects of pad parasitics and gate-to-source inter-electrode capacitance-conductance pair of \((C_{EGS}, G_{EGS})\) by calculating

\[
[Y_{SOURCE}] = [Y_{SHORT1}] - [Y_{PADS}]
\]
\begin{equation}
\begin{bmatrix}
(G_{EGS} + j\omega C_{EGS})/2 & 0 \\
0 & 0 \\
\end{bmatrix}.
\end{equation}

Following this, the source resistance \(R_{ES}\) and inductance \(L_{ES}\) can be computed using

\[
R_{ES} = \text{Re} \left\{ \frac{1}{Y_{SOURCE}^{11}} \right\} - R_{EG},
\]
\[
L_{ES} = \text{Im} \left\{ \frac{1}{Y_{SOURCE}^{11}} \right\} / \omega - L_{EG}.
\]

In Step V, the gate-to-drain mutual inductance \(L_{MGD}\) is computed using the simulation of SHORT2 standard, as shown in Fig. 3.6(e). Initially, the effects of pad-related parasitics, and inter-electrode capacitance-conductance pairs of \((C_{EGS}, G_{EGS})\) and \((C_{EDS}, G_{EDS})\) are deembedded from the simulation data of SHORT2 layout using

\[
[Y_{MUTUAL}] = [Y_{SHORT2}] - [Y_{PADS}]
\]
\begin{equation}
\begin{bmatrix}
(G_{EGS} + j\omega C_{EGS})/2 & 0 \\
0 & (G_{EDS} + j\omega C_{EDS}) \\
\end{bmatrix}.
\end{equation}

Afterwards, we transform the auxiliary admittance matrix \([Y_{MUTUAL}]\) into an impedance matrix \([Z_{MUTUAL}]\)

\[
[Z_{MUTUAL}] =  \begin{bmatrix}
\frac{(R_{EG} + R_{ES}) + j\omega(L_{EG} + L_{ES})}{(R_{EG} + R_{ED} + R_{ES}) + j\omega(L_{EG} + L_{ED}) + j\omega(L_{ES} - 2L_{MGD}) + (G_{EGD} + j\omega C_{EGD})^{-1}}
\end{bmatrix}
\]

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By incorporating the above system of equations into a least squares error fitting routine, one can easily extract the gate-to-drain mutual inductance of $L_{MGD}$.

In the 6th and final step, the inter-electrode capacitance-conductance pairs of $(C_{EGS}, G_{EGS})$, $(C_{EGD}, G_{EGD})$, and $(C_{EDS}, G_{EDS})$ are estimated from the simulation of the OPEN standard in Fig. 3.5(f). To do so, the influence of parallel-connected pad-parasitics and series-connected device electrode parasitics are first factored out from the simulation data of the OPEN standard through the relation

$$Y_{ELCTR} = \left( \left( Y^{OPEN} \right) - \left[ Y^{PADS} \right] \right)^{-1} - \left[ Z^{SERIES} \right]^{-1}, \quad (3.9)$$

where

$$Z^{SERIES} = \begin{bmatrix}
\frac{(R_{EG} + R_{ES})}{+j\omega(L_{EG} + L_{ES})} & \frac{R_{ES}}{+j\omega(L_{ES} - L_{MGD})} \\
\frac{R_{ES}}{+j\omega(L_{ES} - L_{MGD})} & \frac{(R_{ED} + R_{ES})}{+j\omega(L_{ED} + L_{ES})}
\end{bmatrix}, \quad (3.10)$$

is the impedance matrix representation of electrode-related resistances and inductances, and

$$Y_{ELCTR} = \begin{bmatrix}
\frac{(G_{EGS} + j\omega C_{EGS})}{+(G_{EGD} + j\omega C_{EGD})} & \frac{-(G_{EGD} + j\omega C_{EGD})}{-(G_{EGD} + j\omega C_{EGD})} \\
\frac{-(G_{EGD} + j\omega C_{EGD})}{+(G_{EGD} + j\omega C_{EGD})} & \frac{(G_{EDS} + j\omega C_{EDS})}{+(G_{EGD} + j\omega C_{EGD})}
\end{bmatrix}, \quad (3.11)$$

is the admittance matrix description of inter-electrode capacitances and conductances. Subsequently, a linear regression fit to the elements of $Y_{ELCTR}$ can be utilized to identify the inter-electrode capacitances and conductances. The estimations of the circuit parameters obtained from (3.1)-(3.11) provide excellent starting values for further numerical optimization through least squares error fitting algorithm. To assess the accuracy of the proposed extraction process, the normalized error metric is computed between the full-wave simulated and modeled $S$-parameters.
Figure 3.7: Micrographs of the fabricated on-wafer HEMT test structures. (a) PADS. (b) THRU1. (c) THRU2. (d) SHORT1. (e) SHORT2. (f) OPEN.

of the device [173]. For the test patterns described in Fig. 3.5, the average percentage error is less than 10%.

3.2 Experimental Verification of the Proposed Equivalent Circuit Model

To validate the accuracy of the lumped-element HEMT parasitic equivalent circuit extraction procedure developed above, here we use full-wave simulations of the HEMT topology shown in Fig. 3.2 over the frequency range of 10-325 GHz. All six proposed test standards were fabricated on a 3-inch GaAs wafer by depositing a single-layer of
Au. Figure 3.7 shows the die photographs of the fabricated HEMT test structures. The interconnect metallization was fabricated via Au evaporation, and had a thickness of 0.3 µm. The loss tangent of the substrate was set to \( \tan \delta = 0.006 \) in EM simulations [142], which is in accordance with the low-loss characteristic of GaAs material system. The \( S \)-parameters of the fabricated test patterns were also measured using a non-contact probe setup [174] over 90-325 GHz band. The predicted and measured \( S \)-parameters were compared to highlight the degree of agreement between the frequency responses obtained from full-wave EM simulations and the experimental data.

The gate, drain, and source inter-pad capacitances and conductances \( (C_{PGS}, G_{PGS}) \), \( (C_{PGD}, G_{PGD}) \), and \( (C_{PDS}, G_{PDS}) \) are shown in Figs. 3.8(a) and 3.8(b), respectively. In accordance with the physical layout of the test structure, the feedthrough capacitance of \( C_{PGD} \) between gate and drain pads is calculated to be at least 10x smaller than the remaining pad capacitances. As such, \( C_{PGD} \) is often omitted from
Figure 3.9: Device electrode-related resistance and inductance terms. (a) $R_{EG}$, $R_{ED}$, and $R_{ES}$. (b) $L_{EG}$, $L_{ED}$, $L_{ES}$, and $L_{MGD}$.

similar extrinsic equivalent circuits reported previously in the literature [175] - [176]. In addition, the linearly increasing behavior of the substrate conductances with frequency is in close correlation with the complex-valued dielectric constant relation of $G(\omega)/C(\omega) = \sigma_d/\epsilon_0\epsilon_r = \omega \tan \delta$ [177]. The gate, drain, and source electrode resistances and inductances ($R_{EG}$, $L_{EG}$), ($R_{ED}$, $L_{ED}$), and ($R_{ES}$, $L_{ES}$), calculated in Steps II, III, and IV, respectively, are plotted in Figs. 3.9(a) and 3.9(b). Compared to almost constant interconnect resistances published previously in the literature [178], the extracted values increase rapidly as the operation frequency varies from low-microwave to millimeter-wave band. This dramatic rise in device metallization resistance with increasing frequency is due to the current crowding phenomenon, as described in [179], corresponding to the concentration of current flow to the outer surface of conductor at high frequencies. On the other hand, the gate, drain, and source electrode inductances were not observed to exhibit noticeable change as a function of frequency.
The gate-to-drain mutual inductance of $L_{\text{MGD}}$ (computed using simulation of SHORT2 standard) is also given in Fig. 3.9(b). To the best of authors' knowledge, this is the first time analytical extraction of the gate-to-drain mutual inductance of HEMT transistors has been carried out using experimental data. The limited number of investigations that can be found in the literature are based solely on numerical optimization [180]. This subject has not received substantial attention to date due to the relatively lower frequencies of interest ($< 60 \text{ GHz}$) for lumped-element extrinsic equivalent circuits. In this frequency range, the amount of drain-to-gate feedback introduced by this mutual magnetic flux coupling is marginal or totally inconsequential to the device performance. In addition, the impedance associated with the mutual inductance is relatively small at low-microwave frequencies which renders extraction of this component extremely sensitive due to unavoidable measurement uncertainty [181]. However, as the operating frequency moves well into the millimeter-wave regime, the impact of mutual inductive gate-to-drain coupling becomes more pronounced, which necessitates its accurate characterization. This can be done very conveniently using the analytical extraction method developed in Section 3.1.4.

The calculated values of inter-electrode capacitances and conductances of $(C_{\text{EGS}}, G_{\text{EGS}})$, $(C_{\text{EGD}}, G_{\text{EGD}})$, and $(C_{\text{EDS}}, G_{\text{EDS}})$ are given in Figs. 3.10(a) and 3.10(b). One important difference between the lumped-element parasitic equivalent circuit proposed here and those presented in earlier research studies addressing the same subject is that the previously reported equivalent circuits do not differentiate between the
Figure 3.10: Inter-electrode capacitance and conductance terms. (a) $C_{EGS}$, $C_{EGD}$, and $C_{EDS}$. (b) $G_{EGS}$, $G_{EGD}$, and $G_{EDS}$.

inter-pad and inter-electrode capacitances [182]. Instead, the entire capacitive coupling between any two device terminals is represented as a single pad-to-pad capacitance. With the aid of this simplifying assumption, it becomes more straightforward to extract the resulting parasitic quantities, but only at the expense of degraded modeling accuracy for the mmW frequencies. In order to maintain the modeling accuracy well into the millimeter-wave frequency band, inter-pad and inter-electrode coupling capacitances need to be treated independently, as is done in this work.

In order to verify the accuracy of the presented HEMT parasitic equivalent circuit model, the contact pad- and device electrode-related parasitic elements determined in the first four steps of parasitic extraction algorithm are substituted into the equivalent circuits of THRU1 and SHORT1 standards given in Figs. 3.6(b) and 3.6(d), respectively. Figures 3.11(a) and 3.11(b) depict a comparison between the predicted, measured, and modeled $S$-parameters for THRU1 and SHORT1 test fixtures of Steps II and IV of the proposed procedure. The $S$-parameters obtained from full-wave EM
Figure 3.11: Comparison of simulated, measured, and modeled $S$-parameters for THRU1 and SHORT1 test standards. (a) Transmission coefficient $S_{21}^{\text{THRU1}}$. (b) Reflection coefficient $S_{11}^{\text{SHORT1}}$.

Simulation exhibit excellent agreement with the measured data over an extremely wide bandwidth. Perhaps more importantly, the simulated $S$-parameters of the proposed equivalent circuits given in Figs. 3.6(b) and 3.6(d) can very accurately reproduce the frequency response of the parasitic couplings over the entire millimeter-wave band.

To further establish the validity of our new methodology, the complete the set of parasitic coupling effects are estimated by executing the six steps of the suggested parasitic extraction algorithm. Following this, the extracted element values are substituted into the equivalent circuits of SHORT2 and OPEN test structures sketched in Figs. 3.6(e) and 3.6(f). As recognized from Figs. 3.12(a) and 3.12(b), the simulated, measured, and modeled $S$-parameters for the two test standards in Steps V and VI of parameter extraction are again in excellent agreement.
Figure 3.12: Comparison of predicted, measured, and modeled $S$-parameters for SHORT2 and OPEN test patterns. (a) Reflection coefficient $S_{22}^{\text{SHORT2}}$. (b) Transmission coefficient $S_{21}^{\text{OPEN}}$.

The representative comparisons given in Figs. 3.11(a)-3.11(b) and 3.12(a)-3.12(b) demonstrate the accuracy of the full-wave EM simulations in predicting the measured $S$-parameters over an extremely broad bandwidth. More importantly, the $S$-parameters obtained from the equivalent circuit simulation can very accurately track the behavior of EM interactions over the entire mmW band. As seen in Fig. 3.12(b), transmission coefficient $S_{21}^{\text{OPEN}}$ of the OPEN standard increases from virtual open-circuit at low frequencies toward full-transmission in the millimeter-wave region. This steadily-decreasing insertion loss is explained by the fact that the gate-to-drain inter-electrode capacitance $C_{\text{EGD}}$ provides an RF current flow path with continuously decreasing capacitive reactance. This example clearly illustrates the dramatic frequency-dependence of parasitic couplings over the microwave to millimeter-wave

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Figure 3.13: Comparison of simulated and modeled transmission coefficient $S_{21}^{\text{OPEN}}$ for OPEN test structure in the presence and absence of gate-to-drain mutual inductance component $L_{MGD}$. (a) $S_{21}^{\text{OPEN}}$ on polar plot. (b) Logarithmic magnitude of $S_{21}^{\text{OPEN}}$.

regime. It is also worth emphasizing that the transition from capacitive RF current transport at low frequency to inductive current transport at millimeter-wave frequencies is captured accurately with the aid of gate-to-drain mutual inductance of $L_{MGD}$. This effect is clearly demonstrated in Figs. 3.13(a) and 3.13(b), where the inclusion of $L_{MGD}$ in the equivalent circuit improves its validity region well beyond 100 GHz. Therefore, it is necessary to incorporate gate-to-drain mutual magnetic flux linkage as a separate circuit element into the parasitic equivalent circuit of HEMT to maintain the modeling accuracy at millimeter-wavelengths. This new addition of the gate-to-drain mutual inductance is a key contribution that distinguishes our work from previously reported studies on HEMT lumped-element extrinsic equivalent circuit extraction.
3.3 Impact of Parasitic Couplings on High Frequency Performance of HEMTs

The next step in HEMT characterization is to evaluate the impact of parasitic couplings on the high frequency performance of HEMTs. Toward this end, intrinsic small-signal equivalent circuit parameters of a device from the literature is brought together with the extrinsic parasitic couplings extracted by using the full-wave simulation-based methodology described in this chapter. Following the creation of complete small-signal equivalent circuit shown in Fig. 3.4, the extent of the degradation in gain and noise performance imposed by each parasitic component can be conveniently identified from circuit analysis.

Intrinsic nonlinear circuit of HEMT consists of the bias voltage-dependent components shown in Fig. 3.14 [183]. The intrinsic nonlinear elements are associated with the active device operation, and their extraction is based on processing of measured device data. The intrinsic small-signal equivalent circuit consists of device

![Intrinsic small-signal equivalent circuit of HEMT, including the associated noise sources.](image-url)
transconductance $G_{M}^{\text{INT}}$, and its time delay $\tau$, gate-to-source and gate-to-drain channel capacitances of $C_{GS}^{\text{INT}}$ and $C_{GD}^{\text{INT}}$, gate-to-source and gate-to-drain channel charging resistances of $R_{GS}^{\text{INT}}$ and $R_{GD}^{\text{INT}}$, and output capacitance and conductance of $C_{DS}^{\text{INT}}$, and $G_{DS}^{\text{INT}}$. The transconductance $G_{M}^{\text{INT}}$ is a measure of the capability of the device to amplify by transforming the incremental changes in the input voltage into changes in the output current. It constitutes the intrinsic gain mechanism of the device. The intrinsic device can be perceived as a voltage-controlled current source characterized by the transconductance term $G_{M}^{\text{INT}}$. The transconductance value is linearly scalable with the total gate periphery of the device. The device transconductance can not respond to the changes in the externally applied gate-to-source voltage instantaneously. In order to account for the delay inherent in this process, the transconductance delay parameter $\tau$ is integrated into the intrinsic small-signal equivalent circuit. The voltage-dependent distribution of the space charge beneath the gate Schottky contact is modeled as gate-to-source and gate-to-drain depletion capacitances of $C_{GS}^{\text{INT}}$ and $C_{GD}^{\text{INT}}$. These channel capacitances are directly proportional to the total gate width of the device. It requires finite amount of time for the capacitive effects of $C_{GS}^{\text{INT}}$ and $C_{GD}^{\text{INT}}$ to set up. The delay associated with the setup of charge-storage effects is characterized by the time constants $R_{GS}^{\text{INT}}C_{GS}^{\text{INT}}$, and $R_{GD}^{\text{INT}}C_{GD}^{\text{INT}}$. This is the physical origin of the gate-to-source and gate-to-drain channel charging resistance parameters of $R_{GS}^{\text{INT}}$ and $R_{GD}^{\text{INT}}$. These Schottky barrier resistances scale inversely with the total gate width of the device. The output capacitance-conductance pair ($C_{DS}^{\text{INT}}$, $G_{DS}^{\text{INT}}$) quantifies how effectively the amplified output signal can be extracted from the device. This is because output impedance of the device connects in parallel with the load of the amplifier designed by using that device. It is an important design
objective to minimize the output admittance to maximize the voltage gain attainable from the device. The output admittance is linear as a function of the total gate periphery of the device.

The device considered here for high frequency performance analysis is an AlGaN / GaN HEMT fabricated on a high-resistivity silicon substrate [184]. It has two-fingers, with 90nm gate-length, and total gate width of $W_G = 2 \times 50\mu$m. Because very little information is provided about the geometric shape of the device, the remaining lateral and longitudinal dimensions are adjusted accordingly for the subsequent parasitic equivalent circuit extraction, and performance analysis.

The two most important figures of merit (FoMs) for evaluating RF performance of HEMTs are unity current-gain cutoff frequency $f_T$ and unity power-gain cutoff frequency $f_{\text{MAX}}$. They are routinely employed as performance metrics for comparing the speed of devices based on various fabrication technologies. The transition frequency $f_T$ of a two-port device is defined as the frequency where the magnitude of common-source short-circuit current gain $|H_{21}|^2$ rolls off to unity. It is a generally accepted measure of current gain-bandwidth product of the device. The second most frequently quoted performance metric is $f_{\text{MAX}}$. It is the frequency where the magnitude of unilateral power gain $G_U$ falls to unity. The $f_{\text{MAX}}$ is also referred to as maximum oscillation frequency, where steady-state oscillation condition can be sustained assuming the presence of lossless feedback elements. The $f_T$ is more representative of the intrinsic speed of the device, while $f_{\text{MAX}}$ depends strongly on parasitic couplings associated with the device layout [185]. Therefore, the $f_{\text{MAX}}$ is regarded as a more relevant parameter for describing the true potential of a transistor as a transconductance amplifier, in most RF circuit applications. The ratio $f_{\text{MAX}}/f_T$ is
viewed as a measure of the optimality of device layout which indicates how successfully the effect of extrinsic elements on device performance is mitigated. The $f_T$ and $f_{\text{MAX}}$ values are almost exclusively obtained from measurement by extrapolating $|H_{21}|^2$ and $G_U$ curves with a slope of $-20\text{dB/decade}$, and identifying the frequency axis intercept point. This is because the cutoff frequencies of the most recent high-speed devices are significantly larger than the range of frequencies where the current electronic instrumentation is capable of taking measurement. In order to assess the influence of EM couplings on high frequency performance of the selected device, the measurement-based intrinsic equivalent circuit components specified in [184] are first used to calculate $[Y^{\text{INT}}]$, which is the admittance matrix representation of the intrinsic device. Next, the admittance matrix formulation of the extrinsic device can be obtained by performing the following matrix operation:

$$[Y^{\text{EXT}}] = 
\left(
\left([Y^{\text{INT}}] + [Y^{\text{ELCTR}}]\right)^{-1} + [Z^{\text{SERIES}}]\right)^{-1}
+ [Y^{\text{PADS}}],
$$

(3.12)

where $[Y^{\text{PADS}}]$, $[Z^{\text{SERIES}}]$, and $[Y^{\text{ELCTR}}]$ are admittance and impedance matrix descriptions of parasitic subcircuits, defined in equations (3.1), (3.10), and (3.11), respectively. Thereafter, $Y$- to $H$-matrix conversion of $[Y^{\text{EXT}}] \rightarrow [H^{\text{EXT}}]$ is carried out, and the resulting short circuit current gain of intrinsic ($|H_{21}^{\text{INT}}|^2$) and extrinsic device ($|H_{21}^{\text{EXT}}|^2$) are plotted in Fig. 3.15. In addition, admittance matrices of intrinsic ($[Y^{\text{INT}}]$) and extrinsic devices ($[Y^{\text{EXT}}]$) are plugged into Mason’s unilateral power gain definition, and the corresponding power gain curves are also shown in Fig. 3.15. Unilateral power gain is the maximum power gain attainable from the device when the source and load terminations are simultaneously conjugate-matched, and the device is unilateralized through a lossless reciprocal feedback network [186].
Figure 3.15: Current gain $|H_{21}|^2$, and unilateral power gain $G_U$ of intrinsic and extrinsic devices.

The calculated unity current-gain and power-gain cutoff frequencies of the intrinsic device are $f_{T}^{\text{INT}} = 134$ GHz, and $f_{\text{MAX}}^{\text{INT}} = 641$ GHz. For the extrinsic device, the cutoff frequencies are estimated as $f_{T}^{\text{EXT}} = 108$ GHz, and $f_{\text{MAX}}^{\text{EXT}} = 192$ GHz. The computed extrinsic cutoff frequencies are in reasonable correlation with the measured values of $f_{T}^{\text{EXT}} = 100$ GHz, and $f_{\text{MAX}}^{\text{EXT}} = 206$ GHz reported in [184], considering the fact that only a few dimensions of the overall device geometry are specified. The foregoing comment concerning the higher sensitivity of $f_{\text{MAX}}^{\text{EXT}}$ to the parasitic couplings compared to that of $f_{T}^{\text{EXT}}$ is also confirmed by the calculated intrinsic and extrinsic cutoff frequency values. The amount of degradation in $f_{T}^{\text{EXT}}$ brought about by the parasitic couplings can be more easily explained by looking at the following
approximate expression for $f_{T}^{EXT}$

$$\frac{1}{2\pi f_{T}^{EXT}} \approx \left( \frac{C_{GS}^{EXT} + C_{GD}^{EXT}}{G_{M}^{INT}} \right) + C_{GD}^{EXT} \left( R_{S}^{EXT} + R_{D}^{EXT} \right)$$

$$+ \left( C_{GS}^{EXT} + C_{GD}^{EXT} \right) \left( R_{S}^{EXT} + R_{D}^{EXT} \right) \frac{G_{DS}^{EXT}}{G_{INT}^{M}},$$

where $C_{GS}^{EXT} = C_{GS}^{INT} + C_{PGS} + C_{EGS}$, and $C_{GD}^{EXT} = C_{GD}^{INT} + C_{PGD} + C_{EGD}$ are extrinsic gate-to-source and gate-to-drain capacitances [187]. For the device under study, the contributions of second and third terms to the summation in Eq. (3.13) are less than 15%, and 5%, respectively. Unlike $R_{S}^{EXT}$ and $R_{D}^{EXT}$, the gate resistance $R_{EG}$ has no influence on $f_{T}^{EXT}$, since the device is assumed to be driven by an ideal current source in $f_{T}$ calculation. Accordingly, in order to minimize the impact of EM field couplings on $f_{T}^{EXT}$, it is necessary to minimize the ratio of $(C_{GS}^{EXT} + C_{GD}^{EXT}) / (C_{GS}^{INT} + C_{GD}^{INT})$.

This ratio can be thought of as a measure of the contribution of parasitic gate-to-source and gate-to-drain capacitive couplings to the intrinsic device capacitances. One way to achieve this device design objective is to increase the unit finger width $W_{F}$ of the device, since $(C_{GS}^{INT}, C_{GD}^{INT})$ and $(C_{EGS}, C_{EGD})$ scale linearly with the unit finger width, while $C_{PGS}$ stays roughly constant, and $C_{PGD}$ gets smaller. Nevertheless, the gate resistance $R_{EG}$ also scales linearly with the finger width, and the increasing $R_{EG}$ affects $f_{MAX}^{EXT}$ negatively as it will be discussed next.

The impact of parasitic couplings on $f_{MAX}^{EXT}$ is much more severe than that on $f_{T}^{EXT}$, as illustrated in Fig. 3.15. This is because $f_{T}$ measures the capability of the device to amplify RF current applied to the input. Thus, parasitic resistances play a secondary role in determination of $f_{T}^{EXT}$, as also indicated by Eq. (3.13). On the contrary, $f_{MAX}$ quantifies how much power gain is obtainable from an amplifier at the frequency of application. The $f_{MAX}^{EXT}$ value is therefore subject to ohmic losses related to resistive parasitic elements in the extrinsic equivalent circuit. In high-frequency
circuits, power gain is considered as the true measure of amplifier performance, rather than current gain or voltage gain. A power gain of larger than or less than unity is what qualifies a two-port device as being active or passive. Consequently, the \( f_{\text{MAX}} \) is more meaningful figure of merit for deciding the high frequency performance of a device. The dependence of \( f_{\text{MAX}}^{\text{EXT}} \) on parasitic couplings can be better understood by inspecting the following approximate definition for \( f_{\text{MAX}}^{\text{EXT}} \)

\[
f_{\text{MAX}}^{\text{EXT}} \approx \frac{f_T^{\text{EXT}}}{2\sqrt{R_G^{\text{EXT}} + R_S^{\text{EXT}} + R_{\text{INT}}^{\text{EXT}} (G_{DS}^{\text{EXT}} + 2\pi f_T^{\text{EXT}} C_{GD}^{\text{EXT}})}}
\]

where \( R_G^{\text{EXT}} = R_{EG} \), and \( G_{DS}^{\text{EXT}} = G_{\text{INT}}^{\text{DS}} + G_{PDS} + G_{EDS} \) are extrinsic gate resistance and output conductance [188]. It is immediately apparent from Eq. (3.14) that a significant fraction of the decrease in \( f_{\text{MAX}}^{\text{EXT}} \) originates from the access resistances of \( R_G^{\text{EXT}} \) and \( R_S^{\text{EXT}} \), which are dependent directly on the device topology, i.e., the number of gate fingers \( N_{GF} \) and unit finger width \( W_F \). The value of gate resistance \( R_G^{\text{EXT}} \) is of fundamental importance here. Unless \( R_G^{\text{EXT}} \) is small, the value of \( f_{\text{MAX}}^{\text{EXT}} \) can be significantly less than \( f_T^{\text{EXT}} \). This will limit the practical usefulness of the device for RF circuit applications. Increasing the unit finger width continuously for \( f_T^{\text{EXT}} \) enhancement will lead to a diminishing return in terms of the improvement in \( f_{\text{MAX}}^{\text{EXT}} \). This is because the ratio of \( (C_{GS}^{\text{EXT}} + C_{GD}^{\text{EXT}}) / (C_{GS}^{\text{INT}} + C_{GD}^{\text{INT}}) \) will converge to unity for sufficiently large unit finger width, and \( f_T^{\text{EXT}} \) will stabilize around a constant value. On the other hand, the \( R_G^{\text{EXT}} \) and \( C_{GD}^{\text{EXT}} \) will keep rising with increasing finger width, and they will eventually cause significant deterioration in \( f_{\text{MAX}}^{\text{EXT}} \).

One of the major challenges encountered while designing wireless communication receivers is to be able to find active devices with very low noise contribution. This is because the signal being amplified by the receiver is distorted by the random potential fluctuations generated by the device. The problem becomes more serious while
dealing with low amplitude signals due to power constraints as in the case of personal mobile communications. In the receiver of such low-power systems, noise determines the limit for the smallest amplitude signal for which the information content can still be recovered. The sensitivity of the whole receiver chain is dependent on the noise performance of front-end low noise amplifier, which is decided by noise behavior of devices being deployed in the design of that LNA. Since the primary function of the LNA is to lower the overall noise figure of the entire RF front-end circuitry, noise optimization is one of the major concerns in the LNA design. Therefore, the fundamental objective of microelectronics industry is realization of devices with highest possible cutoff frequency, as well as lowest level of noise. It is well known that the devices with higher cutoff frequencies have superior noise performance due to reduced thermal noise contribution of channel resistance. Although heterojunction bipolar transistors (HBTs) have achieved very good high frequency performance to date, their noise level is relatively larger than that of field effect transistors. Hence, the best high frequency noise performance has been demonstrated by unipolar devices, mostly HEMTs [189] - [190]. These devices have long been utilized as the primary front-end receiver component in the fields necessitating exceptionally low noise temperature, such as remote sensing, radio astronomy, and space communications [191]. From a circuit designer’s viewpoint, it is crucial to be capable of predicting the noise contribution of various components that constitute the circuit. In doing so, the inevitable loss of signal-to-noise ratio can be minimized as the received signal is processed to extract information content. With the aid of a variety of technological process innovations, the performance of integrated HEMT devices has been improved at a very fast pace, and they became very attractive for multigigahertz MMIC design. In light
of this rapid progress, the noise performance of intrinsic device has been enhanced substantially with technology scaling, while the noise contribution of extrinsic resistive components started to play progressively more significant role in determination of overall noise performance [192] - [193]. Indeed, overall noise behavior of high-speed nanoscale HEMTs has already started to be dominated by the thermal noise contribution of surrounding parasitic elements, especially at millimeter-wavelengths. As a result, it is of critical significance to investigate the effect of parasitic couplings on the high-frequency noise performance of deep-submicron HEMTs. Better understanding of device parasitic effects will allow for more accurate prediction of noise performance of HEMT-based RF circuits, so that number of design cycles can be reduced, and successful operation can be accomplished in the first design iteration.

Among the various figures of merit available to describe the noise characteristics of HEMT technologies, noise figure is the most commonly used one. Noise figure refers to the extent of degradation in the signal-to-noise ratio caused by the components in an RF receiver chain. One drawback associated with the definition of noise figure is that it is a function of the impedance matching at the input of the device. Therefore, minimum noise figure $NF_{\text{MIN}}$ is generally preferred as the primary performance metric for comparing noise performance of different device technologies. Minimum noise figure stands for the noise added by the transistor to the amplified signal, which reaches an absolute minimum when the source impedance is set to $Z_{S,\text{OPT}}$. The $Z_{S,\text{OPT}}$ is the impedance associated with the optimum source reflection coefficient of $\Gamma_{S,\text{OPT}}$. Closely related to the minimum noise figure is another key performance criterion, which is the associated power gain $G_{\text{ASSOC}}$. The associated power gain refers to the available gain when the device is driven by a source whose admittance is
set to the optimum source admittance $Y_{S-OPT}$, which yields the minimum noise figure. It can be calculated as

$$G_{ASSOC} = \frac{\text{Re}\{Y_{S-OPT}\}}{\text{Re}\left\{y_{22} - \frac{Y_{21}Y_{12}}{Y_{S-OPT} + Y_{11}}\right\}\left|\frac{Y_{21}}{Y_{S-OPT} + Y_{11}}\right|^2},$$

(3.15)

where $Y_{11}, Y_{12}, Y_{21},$ and $Y_{22}$ are the admittance parameters of the device under study [194].

For the noise performance analysis of the selected device, two-temperature noise model proposed by Pospieszalski is implemented [195]. This empirical noise model is described by a noise equivalent circuit of HEMT shown in Fig. 3.14, which takes gate leakage current also into consideration. It is broadly accepted as an easy-to-use FET noise model. It employs two frequency-independent equivalent temperatures for intrinsic channel charging resistance $R_{INT}^{INT}$ and drain conductance $G_{INT}^{INT}$ to predict...
the noise characteristics of a HEMT. This two-parameter noise model considers a gate noise voltage source \( v_{\text{NGS}} \) at the input, and a drain noise current source \( i_{\text{NDS}} \) at the output. They are experimentally verified to be statistically uncorrelated [196] - [197]. The spectral densities of these noise sources are assumed to be proportional to noise coefficients, also known as equivalent noise temperatures of \( T_G \) and \( T_D \). These two noise sources are defined in terms of their mean quadratic values of 
\[
\overline{v_{\text{NGS}}^2} = 4kT_G R_{\text{GS}} \Delta f \quad \text{and} \quad \overline{i_{\text{NDS}}^2} = 4kT_D G_{\text{DS}} \Delta f,
\]

where \( k \) is the Boltzmann constant, and \( \Delta f \) is frequency bandwidth. With the aid of this practical thermal noise model, the entire complexity of the physical noise behavior of a FET is summarized by these two noise parameters of \( T_G \) and \( T_D \). The noise generated by the gate leakage current is treated as a shot-noise with mean square value of 
\[
\overline{i_{\text{NGS}}^2} = 2qI_{\text{GS}} \Delta f,
\]

where \( q \) is the electron charge. Finally, the noise created by the gate-to-drain channel charging resistance of \( R_{\text{GD}} \) is modeled as a thermal noise with mean quadratic value of 
\[
\overline{v_{\text{NGD}}^2} = 4kT_\text{AMB} R_{\text{GD}} \Delta f,
\]

where \( T_\text{AMB} \) is the ambient temperature of the device. The measured DC gate leakage current density is specified as 10 nA/mm in [184]. The previously published studies on the subject predict gate leakage noise to be effective at low-microwave frequency range, while it is expected to have negligible contribution to \( NF_{\text{MIN}} \) at sufficiently high frequencies [198] - [199]. The equivalent gate temperature \( T_G \) is, within measurement errors, equal to ambient device temperature \( T_\text{AMB} \), which is set to the standard temperature of \( T_0 = 290 \text{ K} \), in our study. The equivalent drain temperature \( T_D \) is assumed to be 5000 K, which is compatible with the possible range of \( T_D \) values reported in [200]. Thermal noise contribution of the external access resistances in the parasitic equivalent circuit is also taken into account. The aim is to ascertain the relative importance of extrinsic elements in the determination of overall
noise performance of a highly scaled HEMT. Plotted in Fig. 3.16 are the calculated minimum noise figure $N_{F\text{MIN}}$, and the associated power gain $G_{\text{ASSOC}}$ of intrinsic and extrinsic devices as a function of operating frequency.

It is clearly realized from Fig. 3.16 that the overall noise performance is overwhelmed by the parasitic elements surrounding the device, as the operating frequency enters into millimeter-wave range. The rapidly rising noise figure of the extrinsic device as a function of frequency is also accompanied by a sharp drop in the associated power gain. Hence, the performance of a very low-noise, high-speed, and high-gain intrinsic device is totally limited by the EM field coupling effects external to the device. The overall performance is dictated by the quality of these extrinsic elements connecting the device to the outside world. The apparent limitation of noise performance by the extrinsic parasitic couplings is indeed very similar to the one that is observed for $f_{\text{EXT MAX}}$ in Fig. 3.15. This evident similarity points to the existence of a strong relationship between $f_{\text{EXT MAX}}$ and $N_{F\text{MIN}}$. This is in contrast to the previous investigations on the subject that interpret the noise figure as being correlated more closely with unity current-gain cutoff frequency $f_{\text{T EXT}}$ [201]. In order to gain insight into the impact of extrinsic device elements on high-frequency noise performance, the following approximate expression for minimum noise figure $N_{F\text{MIN}}$ is utilized [202] - [204]

$$N_{F\text{MIN}} \approx 1 + \frac{f_{\text{EXT MAX}}}{f_{\text{EXT MAX}}} \sqrt{\frac{G_{\text{EXT DS}}^2 T_D}{G_{\text{INT M}}^2 T_0}} \cdot \sqrt{1 + \left(2 \frac{f_{\text{EXT MAX}}}{f_C}\right)^2 G_{\text{INT M}}^2 (R_{\text{INT G}}^\text{EXT} + R_{\text{EXT S}}^\text{EXT} + R_{\text{GS}}^\text{INT})},$$

(3.16)

where $f_C = G_M/2\pi C_{\text{GS}}^\text{INT}$ is the intrinsic cutoff frequency [205]. It is apparent from the preceding formulation that the extrinsic parameters limiting high-frequency power
gain characteristics of deeply-scaled HEMTs are also responsible for larger $NF_{MIN}$ and lower noise performance. Consequently, $f_{MAX}^{EXT}$ is one of the most appropriate criteria to compare microwave performance of transistors, for applications involving high-gain and low-noise. Any technological effort directed toward improving $f_{MAX}^{EXT}$ will also be useful in terms of lowering $NF_{MIN}$. As pointed out by Eq. (3.16), special attention must be paid to reduce the resistance of gate electrode metallization by using mushroom gates or multi-finger gate structures. Once the contribution of access resistances is minimized, further improvement of $f_{MAX}^{EXT}$, and thus $NF_{MIN}$, is contingent on suppression of gate-to-drain feedback capacitance $C_{EGD}^{EXT}$ and output conductance $G_{DS}^{EXT}$. Increasing output conductance with continuously shrinking channel length is of major concern in high-speed device design. Similarly to the case of $f_{MAX}^{EXT}$, increasing unit finger width of the device for $f_{T}^{EXT}$ improvement will have an adverse effect on noise performance because of the proportional increase in the extrinsic elements of $R_{G}^{EXT}$ and $C_{GD}^{EXT}$. Having investigated the influence of parasitic couplings on speed and noise characteristics of nanoscale HEMTs, full-wave EM simulation-based device geometry optimization will now be illustrated.

In order to evaluate the effect of gate length scaling on noise performance, the suggested characterization methodology is also applied to an AlN/GaN/AlGaN HEMT with 45 nm gate length. Plotted in Fig. 3.17 is comparison of extrinsic and intrinsic minimum noise figure $NF_{MIN}$ for HEMTs with 45 nm [206] and 90 nm [184] gate length. The aggressive shrinking of minimum gate length to deep submicron range increases device transconductance, and reduces intrinsic capacitances proportionally. Accordingly, the speed and noise performance of intrinsic device improve significantly as a consequence of gate length scaling. However, the rate of decrease in parasitic
element values is much slower than linear due to the tradeoffs involved in device geometry [207], and the limitations imposed by the material systems and litographic processes [208]. Hence, the impact of gate length scaling on extrinsic device performance is not as much pronounced as that on intrinsic device performance, as also illustrated in Fig. 3.17. More concentrated research effort is required to reduce the parasitic components, including access resistances and gate fringing capacitances, for further maximization of device performance.

### 3.4 Optimum Device Periphery Selection

The final step in extrinsic equivalent circuit characterization is to acquire design optimization capability. In a multifinger transistor structure, the layout of the device
is controlled mainly by the gate length, number of gate fingers $N_{GF}$, and unit finger width $W_F$. The total gate periphery $W_G$ can be calculated as $W_G = N_{GF} \times W_F$. In RF circuit design, the minimum channel length device is preferred almost exclusively because of its higher speed and larger current drive capability. Hence, the RF circuit designer has two parameters to optimize the device characteristics, which are $N_{GF}$ and $W_F$. Besides, as the transistor channel length shrinks down to deep submicrometer range, layout optimization for minimization of parasitic effects and improvement of speed and noise performance becomes even more critical. The primary figures of merit for assessing the speed and noise performance of a device are unity current-gain and power-gain cutoff frequencies of $f_T$, and $f_{MAX}$, minimum noise figure $NF_{MIN}$, and associated power gain $G_{ASSOC}$, as discussed in the previous section. It is well known that the elements of admittance matrix $[Y^{INT}]$ for the intrinsic small-signal equivalent circuit scale linearly with the total gate periphery $W_G$ of the device [209]. Intrinsic gate-to-source and gate-to-drain capacitances of $C^{INT}_{GS}$ and $C^{INT}_{GD}$, output capacitance and conductance of $C^{INT}_{DS}$ and $G^{INT}_{DS}$, and device transconductance of $G^{INT}_M$ are linearly proportional to the unit finger width $W_F$, and the number of gate fingers $N_{GF}$. On the other hand, gate-to-source and gate-to-drain channel charging resistances of $R^{INT}_{GS}$ and $R^{INT}_{GD}$ are inversely proportional to the unit finger width $W_F$, and the number of gate fingers $N_{GF}$ [210]. Since a different scaling rule applies to each parasitic element with respect to finger number and unit gate width, different extrinsic elements impact the performance in different directions as the size of the device is varied. Therefore, it is essential to investigate foregoing figures of merit as a function of device size in order to decide the optimum finger number and unit finger width based on the above performance metrics. The ultimate purpose of this section is to provide a qualitative
understanding of optimum device layout selection in order to help RF integrated circuit designers create superior receiver front-end circuits.

In the course of device periphery optimization, as the device size is varied, the appropriately scaled version of intrinsic equivalent circuit elements are assembled together with the extrinsic parasitic components for the analysis of microwave gain and noise behavior. For the optimization of speed of the device, the current-gain and power-gain cutoff frequencies of $f_T$ and $f_{\text{MAX}}$ are studied as a function of the changing device size. Plotted in Figs. 3.18(a) and 3.19(a) is unity current gain cutoff frequency $f_{T}^{\text{EXT}}$ of extrinsic device with respect to the width per finger $W_F$ and gate finger number $N_{GF}$. As seen in Fig. 3.18(a), the $f_{T}^{\text{EXT}}$ is approximately independent of the number of gate fingers $N_{GF}$ as long as the width per finger $W_F$ is kept constant. This behavior of $f_{T}^{\text{EXT}}$ as a function of finger number $N_{GF}$ is indeed consistent with the expression in Eq. (3.13). The numerator and the denominator of the first term $\left(C_{GS}^{\text{EXT}} + C_{GD}^{\text{EXT}}\right)/G_{M}^{\text{INT}}$ in the summation scale linearly with the
Figure 3.19: Contour plot of extrinsic unity current-gain and power-gain cutoff frequencies as a function of unit finger width $W_F$, and number of gate fingers $N_{GF}$. (a) $f_{T}^{EXT}$. (b) $f_{MAX}^{EXT}$.

finger number, and hence the ratio stays constant. A similar observation also holds true for the second and third terms in Eq. (3.13). It is further recognized that the value of $f_{T}^{EXT}$ is increasing as a function of unit finger width with a decreasing slope, and eventually approaching a steady-state value. The initial steep rise of $f_{T}^{EXT}$ as a function of increasing width per finger is because of the sharp drop of the first term in Eq. (3.13) for relatively small unit finger width. The intrinsic transconductance $G_{INT}^M$ scales linearly with the finger width, while the rate of increase for the total extrinsic capacitance of $(C_{GS}^{EXT} + C_{GD}^{EXT})$ looking into gate terminal is less than linear. This is due to nearly constant offset parasitic gate-to-source inter-pad capacitance of $C_{PGS}$. However, as the finger width is increased continuously, the contribution of $C_{PGS}$ to $C_{GS}^{EXT}$ becomes progressively more negligible, and the $f_{T}^{EXT}$ stabilizes around
a fixed value. This concave shape of $f_{T}^{\text{EXT}}$ curve as a function of finger width $W_F$ with initially positive and eventually zero slope is in agreement with simulation- and measurement-based results published previously in the literature [211] - [212].

The dependence of $f_{MAX}^{\text{EXT}}$ on the unit finger width $W_F$ and the number of gate fingers $N_{GF}$ is presented in Fig. 3.18(b) and 3.19(b). It is observed that the $f_{MAX}^{\text{EXT}}$ is decreasing with respect to increasing width per finger. It is already explained that the $f_T^{\text{EXT}}$ increases with a decreasing slope, and finally converges to a fixed value, as the unit finger width is raised incessantly. However, the extrinsic elements of $R_G^{\text{EXT}}$ and $C_{GD}^{\text{EXT}}$ exhibit a linear increase as a function of unit finger width, and they lead to an inevitable degradation in $f_{MAX}^{\text{EXT}}$ for relatively large values of finger width, as suggested by Eq. (3.14). Another issue with reduction of width per finger for $f_{MAX}^{\text{EXT}}$ optimization arises when the finger width gets disproportionately small. For a device with an unnecessarily short finger width, the offset pad-to-pad parasitic capacitance of $C_{PGS}$ dominates the intrinsic gate-to-source and gate-to-drain capacitances of $C_{GS}^{\text{INT}}$ and $C_{GD}^{\text{INT}}$. Hence, the $f_T^{\text{EXT}}$ drops severely for unreasonably small values of unit finger width, as exemplified in Fig. 3.18(a). This inevitable drop in $f_T^{\text{EXT}}$ will eventually result in deterioration in $f_{MAX}^{\text{EXT}}$, as also implied by Eq. (3.14). As a result, the value of finger width for optimum $f_{MAX}^{\text{EXT}}$ should be selected carefully to manage the tradeoff between short finger width to minimize the gate resistance $R_G^{\text{EXT}}$, and sufficiently large one needed to suppress the adverse effect of offset gate-to-source inter-pad capacitance $C_{PGS}$. This behavior of $f_{MAX}^{\text{EXT}}$ as a function of unit finger width is in close correlation with simulation- and measurement-based studies conducted previously on the subject [213] - [214]. As it is also noticed from Fig. 3.18(b), the $f_{MAX}^{\text{EXT}}$ can be improved by around 20% by choosing a device with two gate fingers and 12.5$\mu$m finger width.

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Figure 3.20: Minimum noise figure and associated power gain of extrinsic device at 20 GHz as a function of unit finger width $W_F$, and number of gate fingers $N_{GF}$. (a) $NF_{MIN}$. (b) $G_{ASSOC}$.

In order to optimize the noise performance, the minimum noise figure $NF_{MIN}$ is investigated as a function of gate finger number $N_{GF}$ and gate width per finger $W_F$. Shown in Figs. 3.20(a) and 3.21(a) is the behavior of extrinsic $NF_{MIN}$ as the number of gate fingers $N_{GF}$ and unit finger width $W_F$ are varied. As realized from Fig. 3.20(a), the value of $NF_{MIN}$ is increasing as the unit finger width is raised. The $NF_{MIN}$ increases as a function of unit finger width because the extrinsic gate resistance $R_{g}^{EXT}$ and gate-to-drain feedback capacitance $C_{GD}^{EXT}$ scale linearly with respect to width per finger. These two extrinsic elements result in a deterioration in $f_{MAX}^{EXT}$, and a corresponding increase in $NF_{MIN}$, as also implied by Eq. (3.16). This characteristic is indeed predictable if the $NF_{MIN}$ expression in Eq. (3.16) and the variation of $f_{MAX}^{EXT}$ in Fig. 3.18(b) are taken together into consideration. The intrinsic and extrinsic device parameters limiting high-frequency power gain performance and thus $f_{MAX}^{EXT}$ of the device are in fact the same as those which lower the noise performance. Therefore,
Figure 3.21: Contour plot of minimum noise figure and associated power gain of extrinsic device at 20 GHz as a function of unit finger width $W_F$, and number of gate fingers $N_{GF}$.

(a) $NF_{MIN}$. (b) $G_{ASSOC}$.

the $f_{MAX}^{EXT}$ is recommended as the most comprehensive criterion for comparing the RF performance of transistors, for both high-frequency and low-noise applications [215].

It is notable from Figs. 3.18(b) and 3.20(a) that the dependence of extrinsic $NF_{MIN}$ on width per finger is roughly the inverse of that exhibited by $f_{MAX}^{EXT}$, providing a simulation-based proof for the qualitative accuracy of the expression in Eq. (3.16). It is important to highlight that selecting an unnecessarily short finger width for improving noise performance is also problematic because the offset gate-to-source parasitic inter-pad capacitance $C_{PGS}$ will become very large in comparison to intrinsic inter-electrode capacitances of $C_{INT}^{GS}$ and $C_{INT}^{GD}$. This relative increase in $C_{PGS}$ compared to intrinsic device capacitances will lead to an inevitable drop in $f_{MAX}^{EXT}$, and a corresponding increase in $NF_{MIN}$. Similarly to the case of $f_{MAX}^{EXT}$, the value of unit finger width
for minimum $NF_{MIN}$ should be chosen cautiously to optimize the tradeoff between small width per finger to reduce the gate resistance $R_G^{EXT}$, and adequately large one required to restrain the adverse influence of offset parasitic pad-to-pad capacitance of $C_{PGS}$. This convex shape of $NF_{MIN}$ curve with respect to width per gate finger $W_F$ with progressively increasing slope is in close agreement with simulation-based studies reported previously in the literature [216] - [217]. As it is also recognized from Fig. 3.20(a), the $NF_{MIN}$ can be reduced by roughly 20% by selecting a device with two gate fingers and 12.5$\mu$m finger width. Dependence of the second most important noise performance measure $G_{ASSOC}$ on device geometry is closely related to that of $NF_{MIN}$. Plotted in Figs. 3.20(b) and 3.21(b) is the variation of extrinsic associated power gain $G_{ASSOC}$ as the gate finger number $N_{GF}$ and width per gate finger $W_F$ are varied. The behavior of $G_{ASSOC}$ as a function of number of gate fingers and unit finger width is approximately the inverse of that exhibited by $NF_{MIN}$. Therefore, the foregoing explanations for the $NF_{MIN}$ characteristics with respect to device layout hold true for $G_{ASSOC}$ as well. Similarly to the cases of $f_{MAX}^{EXT}$ and $NF_{MIN}$, the value of $G_{ASSOC}$ can be enhanced by around 10% by choosing a device with two gate fingers and 12.5$\mu$m gate finger width. In summary, the minimum noise figure and largest associated power gain are obtained from the device having the highest value of $f_{MAX}$. This justifies the use of $f_{MAX}$ as the foremost performance metric for comparing the speed and noise properties of various device technologies.

3.5 Conclusion

We have proposed a lumped-element parasitic equivalent circuit model for submicron gate-length HEMTs that can accurately reconstruct the frequency response
of EM couplings in the mmW frequency band. Additionally, we have developed a novel multi-step systematic parasitic model extraction algorithm based on successive partitioning of the whole HEMT parasitic equivalent circuit into multiple subcircuits. An analytical procedure has been offered for the first time to extract the gate-to-drain mutual inductance $L_{MGD}$, which introduces an increasingly detrimental inductive feedback path from drain to gate at high frequencies. The accuracy and robustness of the suggested extraction methodology have been established through comparisons between simulated, measured, and modeled frequency responses of the proposed test standards up to 325 GHz. The presented lumped-element parasitic equivalent circuit has been demonstrated to achieve the desired broadband accuracy over the low-microwave and millimeter-wave frequency range. The obtained results are useful in terms of gaining insight into the geometry- and material-dependent electrically- and magnetically-driven power dissipation mechanisms of HEMTs. So as to assess the adverse impact of EM interactions on gain and noise performance, intrinsic nonlinear small-signal equivalent circuit of a HEMT has been incorporated into the extracted lumped-element parasitic equivalent circuit model for the following circuit analysis. It has been concluded from layout optimization that the most reliable performance metric for comparing the gain and noise characteristics of various device technologies is extrinsic maximum oscillation frequency $f_{\text{EXT}}^{\text{MAX}}$. As a matter of fact, the $f_{\text{EXT}}^{\text{MAX}}$ is dependent on both intrinsic nonlinear and extrinsic linear parasitic elements, and thus it can be improved through optimization of device topology. The tradeoff between $f_{\text{EXT}}^{\text{P}}$ and extrinsic gate resistance $R_{G}^{\text{EXT}}$ results in existence of an optimum layout for achieving maximum $f_{\text{MAX}}^{\text{EXT}}$ and minimum $NF_{\text{MIN}}$. It has been demonstrated through a full-wave EM simulation-based parametric study that 20%
improvement in $f_{\text{MAX}}^\text{EXT}$, 20% reduction in $NF_{\text{MIN}}$, and 10% increase in $G_{\text{ASSOC}}$ at 20 GHz are realizable via optimization of device gate finger number, and unit finger width. Finally, utilization of full-wave EM simulation tools instead of fabrication and measurement of test structures is a cost-effective solution to the problem of transistor modeling in the mmW frequency range.
Chapter 4: Distributed Modeling of Submillimeter-Wave 
HEMT Parasitics

Owing to the continuous advancements in transistor manufacturing and epitaxial growth techniques, high electron mobility transistors (HEMTs) with record cutoff frequency characteristics falling into the submillimeter-wave (sub-mmW) frequency range are now realizable [218]. As the operating frequency of the most recent MMICs is pushed continuously toward sub-mmW band, the device undergoes severe impairments in its performance. This inevitable degradation in performance originates from both intrinsic device behavior, and extrinsic parasitic factors associated with device access metallization. With the continued shrinking of minimum gate length to deep deca-nanometer dimensions, the effect of geometry- and material-dependent parasitic couplings, induced by electromagnetic (EM) field interactions within the device structure, becomes progressively more comparable to intrinsic device behavior [219] - [221]. In this regard, availability of small-signal equivalent circuits that take into consideration the intrinsic and extrinsic device characteristics simultaneously becomes critical for reliable design of sub-mmW RF transceivers.

The primary objective of this chapter is to characterize EM field couplings that limit performance of sub-mmW HEMTs in terahertz (THz) band. In traditional equivalent circuit extraction attempts toward HEMT parasitic coupling modeling,
Figure 4.1: Three-dimensional schematics illustrating the structure of a submillimeter-wave high electron mobility transistor (HEMT). (a) Top view. (b) Side view.

the power dissipation and electric/magnetic energy storage inside the device structure are represented by lumped resistive and capacitive/inductive elements [222]. Nevertheless, as the working frequency is moved into sub-mmW band, the physical dimensions of the device become the same order of magnitude as the operating wavelength, and hence the device starts to exhibit distributed effects along the gate width direction [223].

A large volume of literature is available on the analysis of distributed parasitic coupling effects on microwave performance of field effect transistors (FETs). There mainly exist two complementary analysis methods. The first one is known as global modeling which couples Maxwell’s equations with the Boltzmann charge transport relations. It is a kind of numerical time-domain field-theoretical solution [224] - [225]. The other one is fully distributed model which considers the gate and drain electrode...
transmission lines as coupled through passive EM field interactions and infinitesimal sections of the intrinsic active device, designated by a two port admittance matrix [226]. An exact analytic and numerical solution of fully distributed model was derived in Lee’s paper [227] and dissertation [228]. Lee presented a distributed circuit analysis of power FETs that takes into account the lateral source parasitic impedance in addition to the lateral drain and gate parasitic impedances. Approximate equivalent circuits were developed by Lee for FETs having short gate width with two common types of boundary conditions. It was shown that when the gate and drain terminals are located on opposite sides of a short gate-width FET, the lateral source parasitic impedance can be represented by an equivalent circuit with a negative impedance in series with the source terminal. The practical consequences on parameter extraction for device modeling were also discussed in Lee’s work. The availability of an exact analytic solution for the distributed FET was predicted to assist the synthesis of traveling wave FETs.

Compared to global modeling approach, fully distributed model requires less computation time and memory, but coupled differential equations still need to be solved. This renders implementation of fully distributed model inconvenient for circuit simulation tools. Therefore, a simplified version, which is known as semi-distributed (sliced) model, was proposed. It divides the FET device into a finite number of electrically-short active transmission line sections [229]. In essence, the sliced HEMT model can be viewed as a discretized approximation of the fully distributed model, and it can be embedded into computer-aided-design (CAD) routines of circuit simulators very conveniently.
Over the last few decades, distributed parasitic equivalent circuit extraction efforts toward FET modeling have been focused primarily on optimization of equivalent circuit parameters to fit the experimental data [230]. The major weakness of distributed parameter extraction from a single $S$-parameter measurement is that there exist more unknowns than the number of equations offered by the measured data. Numerical optimization tools are employed very frequently to solve such under-determined system of equations. The main drawback of these pure optimization-based techniques is that their performance is dependent heavily on the quality of starting parameter values. The likelihood of convergence toward inaccurate local minimums with physically unfeasible circuit element values is also moderately high. Therefore, there is an ongoing
demand for a multi-step distributed parasitic model extraction approach with well-conditioned optimization of at most several components in each step. Such a multi-step characterization procedure can substantially reduce computational complexity of the optimization algorithm, and guarantee extraction of a physically representative set of parasitic element values.

Commercial full-wave electromagnetic simulators have also been utilized recently for analysis of wave propagation effects and development of empirical approaches toward distributed modeling of FETs [231]. In these former treatments of the subject, the extrinsic distributed network is described in terms of a multi-port $S$-matrix obtained from full-wave EM simulation of the actual device geometry. Although the frequency response of distributed parasitic couplings can be completely described by using scattering parameters, such mathematical representations do not provide a clearly visible relation between the device geometry and the resulting frequency characteristics. On the contrary, the elements of equivalent circuit models can be directly associated with the physical structure of the device. Consequently, modeling of wave propagation phenomena through a distributed equivalent circuit network is crucial in terms of having a deeper understanding of the relation between device geometry and the related parasitic coupling effects. Furthermore, the knowledge of distributed equivalent circuit model is prerequisite for analysis and prediction of noise performance-related parameters.

In order to account for the wave propagation effects along the device electrodes at THz frequencies, a distributed parasitic equivalent circuit model is adopted in this study. The distributed nature of gate-to-drain inter-electrode coupling capacitance
Figure 4.3: Parasitic equivalent circuit models of HEMT for different frequency bands. (a) Lumped-element model for millimeter-wave region. (b) Distributed model for submillimeter-wavelengths.
and mutual inductance are taken into account by interpreting gate and drain electrodes as a coupled three-line structure. Based on this distributed parasitic circuit model, we implement a novel systematic multi-step distributed parameter extraction procedure. The accuracy of the developed distributed-parameter extraction methodology is established through extensive comparisons between simulated, measured, and modeled frequency responses of the suggested test structures up to 750 GHz. The frequency responses of distributed and lumped models are also compared concurrently against the full-wave simulated response to reveal the shortcomings of lumped-element perspective toward HEMT modeling at terahertz frequencies. Following this, the adverse effect of EM field couplings on microwave performance of sub-mmW HEMTs is evaluated. Since the operation of the active device as an amplifier is also subject to intrinsically distributed wave propagation phenomena, a semi-distributed (sliced) HEMT model is considered for the subsequent performance analysis. Thereafter, the device layout is optimized with the purpose of improving RF performance. Design guidelines are provided for optimum device periphery selection to achieve the highest speed and the lowest noise level obtainable from the extrinsic device.

4.1 Parasitic Equivalent Circuit Modeling by Full-Wave EM Simulation

This section provides a detailed description of the HEMT geometry and the associated electromagnetic field coupling mechanisms investigated in this chapter. Three-dimensional HEMT configuration depicted in Fig. 4.1 is constructed and simulated by using Ansoft High Frequency Structure Simulator (HFSS) [107]. Thereafter, full-wave electromagnetic simulation results are analyzed in Agilent Advanced Design System (ADS) [108] to extract HEMT distributed parasitic equivalent circuit components.
Figure 4.4: Equivalent circuit models of device substrate for different frequency bands. (a) Lumped-element model for millimeter-wave region. (b) Distributed model for submillimeter wavelengths.

4.1.1 Distributed Parasitic Equivalent Circuit Model

As the operating wavelength becomes comparable to the physical dimensions, particularly the gate finger width, of the device at sub-mmW frequencies, compact lumped-element parasitic equivalent circuit approximations of HEMT become progressively more inaccurate. Gate and drain electrodes, semi-insulating substrate, and interconnecting pads need to be modeled as distributed components once their physical lengths exceed one tenth of the guided wavelength $\lambda_{\text{EFF}}$. To circumvent the
limitations of lumped-element approach toward device modeling at terahertz frequencies, we propose the distributed parasitic equivalent circuit model of HEMT shown in Fig. 4.3(b). In lumped-element equivalent circuit of Fig. 4.3(a), device contactings pads are modeled as inter-pad capacitance-conductance pairs of \((C_{\text{PGSL}}, G_{\text{PGSL}})\), and \((C_{\text{PDSL}}, G_{\text{PDSL}})\). Besides, resistance and inductance of the device pads and electrodes are represented together as resistance-inductance pairs of \((R_{\text{EG}}, L_{\text{EG}})\), and \((R_{\text{ED}}, L_{\text{ED}})\). In the proposed distributed equivalent circuit model, the device pads and electrodes are treated independently of each other. Lumped-element approximations of contacting pads are replaced by tapered transmission line counterparts. Electrical energy storage and power dissipation at the intersection of device pads and electrodes are described as shunt fringing capacitance-conductance pairs of \((C_{\text{PGSD}}, G_{\text{PGSD}})\) and \((C_{\text{PDSD}}, G_{\text{PDSD}})\) between signal trace and ground conductor of coplanar waveguide. Lumped-element representation of gate-electrode as a series-connected resistance-inductance pair of \((R_{\text{EG}}, L_{\text{EG}})\), and parallel-connected gate-to-source inter-electrode capacitance-conductance pair of \((C_{\text{EGS}}, G_{\text{EGS}})\) neglects the distributed nature of these elements at submillimeter-wavelengths. To address this distributed aspect of gate-electrode, it is modeled as a regular coplanar waveguide section with characteristic impedance of \(Z_{\text{0EG}}\), and propagation constant of \(\gamma_{\text{EG}}\). A similar interpretation also holds true for the drain electrode, which is again modeled as a regular coplanar waveguide section with characteristic impedance of \(Z_{\text{0ED}}\), and propagation constant of \(\gamma_{\text{ED}}\). The gate-to-drain coupling capacitance-conductance pair of \((C_{\text{EGD}}, G_{\text{EGD}})\) and mutual inductance of \(L_{\text{MGD}}\) also exhibit distributed characteristic as the operating frequency enters into submillimeter-wave regime. Consequently, the gate, drain, and source electrodes need to be modeled collectively as a coupled three-line [232], as
indicated in distributed parasitic equivalent circuit model of Fig. 4.3(b). The final part of the HEMT structure whose modeling requires further attention is the substrate. In lumped-element equivalent circuit of Fig. 4.4(a), displacement and conduction current flow through the substrate are modeled by parallel-connected inter-pad capacitance-conductance pair of \((C_{PGD}, G_{PGD})\). This lumped-element approximation of substrate in Fig. 4.4(a) becomes less accurate in terms of accounting for the attenuation and propagation delay through the substrate at sub-mmW frequencies. In order to take wave propagation effects through the substrate into account, a distributed substrate network \([233]\) is considered in Fig. 4.4(b). In this distributed equivalent circuit, lumped inter-pad capacitance-conductance pair of \((C_{PGD}, G_{PGD})\) is replaced by series-connected infinitesimal \((\Delta C_{PGD}, \Delta G_{PGD})\) pairs. In lumped-element substrate model of Fig. 4.4(a), the inter-pad capacitance \(C_{PGD}\) will pose a constantly decreasing capacitive reactance to the RF current flow through the substrate. This means that the RF current flowing through the substrate must experience a steadily decreasing attenuation with increasing frequency. This interpretation neglects the adverse impact of substrate-to-ground leakage on the attenuation of RF current flow through the substrate at terahertz frequencies. Substrate-to-ground infinitesimal capacitance-conductance terms of \((\Delta C_{SUB}, \Delta G_{SUB})\) are introduced in Fig. 4.4(b) to accurately capture the attenuation and propagation characteristics through the substrate. The distributed substrate network is incorporated into the proposed sub-mmW HEMT equivalent circuit of Fig. 4.3(b) as a transmission line with characteristic impedance of \(Z_{0PGD}\) and propagation constant of \(\gamma_{PGD}\).

The coupled three-line model presented here applies to passive reciprocal symmetric devices. Lee’s work \([227] - [228]\) provides a more general analytical derivation
that considers the transistor as an asymmetric non-reciprocal device providing gain.

An eight-terminal model for FETs with short gate-width was also provided by Roblin [234] to account for the effect of substrate contact. The presented eight-terminal model could be easily reduced to six-terminal model as well. The position of source impedance termination is another factor influencing the EM coupling mechanisms within the device structure, and thus needs further discussion. Transistors do not always have their source terminal grounded, and it can be floating. When grounding is targeted, air bridges are often employed to propagate the grounding, and force the source contacts to stay at the same potential. However, such grounding may not be perfect and provide an inductance leading to a balanced to unbalanced line transition. Besides, transistor modeling studies expect the device geometry to be symmetric. Any asymmetry in the device layout is likely to introduce imbalance among the measured waveforms. Special attention must be paid to independently ground the common device terminals on both sides, especially at high frequencies. In the absence of a well-defined ground return path, a ground loop might be created by the device layout [235]. In such a case, the device is operated in the common mode instead of the intended differential mode, and the proposed equivalent circuit models are no longer applicable. Consequently, ground propagation is an important and complex issue that might be the focus of future research directions.

Distributed extrinsic equivalent circuit analysis of HEMT utilizes the standard $\pi$-network configuration depicted in Fig. 4.5. This $\pi$-network topology is based on admittance matrix representation of a reciprocal two-port network, with the series
branch replaced by effective transfer impedance

\[ Z_{\text{SERIES}}(\omega) = -\frac{1}{Y_{21}(\omega)} = R_{21}(\omega) + jX_{21}(\omega), \quad (4.1) \]

where \( R_{21}(\omega) \) and \( X_{21}(\omega) = \omega L_{21}(\omega) \) are effective series transfer resistance and reactance, respectively. Distributed characteristic of HEMT gate and drain electrodes at terahertz frequencies is directly recognized as a drop in effective series transfer resistance \( R_{21}(\omega) \), which can become even negative depending on the operating frequency [236]. This nonmonotonic behavior of \( R_{21}(\omega) \) as a function of frequency can not be anticipated by the traditional lumped-element equivalent circuit presented in Fig. 4.3(a).

### 4.1.2 Parasitic Extraction by Representative Test Structures

The characterization procedure formulated in this chapter produces the frequency-dependent extrinsic components of HEMT by partitioning the whole parasitic equivalent circuit into multiple subcircuits in six steps. In each step, a progressively more complicated variation of the HEMT geometry is simulated, and also measured. Direct analytical parameter extraction technique is employed in cooperation with numerical optimization tools for the subsequent investigation. Sketched in Fig. 4.6 are
Figure 4.6: Layouts of the on-wafer test structures designed for HEMT distributed-element extrinsic equivalent circuit extraction. (a) PADS. (b) THRU1. (c) THRU2. (d) SHORT1. (e) SHORT2. (f) OPEN.
Figure 4.7: The proposed distributed extrinsic equivalent circuit descriptions of HEMT for different steps of parasitic extraction. (a) PADS. (b) THRU1. (c) THRU2. (d) SHORT1. (e) SHORT2. (f) OPEN.
the layouts of the proposed representative test standards for each simulation and measurement scenario, devised for iterative parasitic extraction. The corresponding distributed parasitic equivalent circuit models for these test fixtures are reported in Fig. 4.7. Gate and drain contact-pad extensions are modeled as tapered transmission lines. They are simulated individually and deembedded from the aforementioned scenarios through successive application of $Z$- and $Y$-matrix conversions. The characteristic impedance $Z_C(\omega)$ and propagation constant $\gamma(\omega) = \alpha(\omega) + j\beta(\omega)$ of the device electrodes are computed by inserting the full-wave simulated and measured $S$-parameters into [138]

$$Z_C(\omega) = Z_0 \left( \frac{(1 + S_{11} + S_{21})(1 + S_{11} - S_{21})}{(1 - S_{11} - S_{21})(1 - S_{11} + S_{21})} \right)^{1/2}$$  \hspace{1cm} (4.2)

$$\gamma(\omega) = \frac{2}{l} \tanh^{-1} \left( \frac{(1 + S_{11} - S_{21})(1 - S_{11} - S_{21})}{(1 - S_{11} + S_{21})(1 + S_{11} + S_{21})} \right)^{1/2}$$,  \hspace{1cm} (4.3)

where $Z_0 = 50\,\Omega$ is the reference impedance. Inter-pad capacitance-conductance pairs are estimated from the simulation of pads standard in step I, with the layout given in Fig. 4.6(a). After deembedding the contact pads, linear regression fit to the low-frequency $Y$-matrix representation of the equivalent circuit in Fig. 4.4(a) can be resorted to estimate the lumped pad parasitics according to the following relations

$$C_{PGD} = -\text{Im}\{Y_{12}\}/\omega, \hspace{1cm} G_{PGD} = -\text{Re}\{Y_{12}\} \hspace{1cm} (4.4)$$

$$C_{PGSL} = \text{Im}\{Y_{11} + Y_{12}\}/\omega, \hspace{1cm} G_{PGSL} = \text{Re}\{Y_{11} + Y_{12}\} \hspace{1cm} (4.5)$$

$$C_{PDSL} = \text{Im}\{Y_{22} + Y_{12}\}/\omega, \hspace{1cm} G_{PDSL} = \text{Re}\{Y_{22} + Y_{12}\}. \hspace{1cm} (4.6)$$

At terahertz frequencies, $S$-matrix representation of the pad-related parasitic components in Fig. 4.4(b) can be substituted into Eqs. (4.2)-(4.3) to compute the characteristic impedance $Z_{0PGD}(\omega)$ and propagation constant $\gamma_{PGD}(\omega)$ of the distributed
substrate network, which can be expressed as

\[
Z_{0PGD}(\omega) = \left( (G_{PGD} + j\omega C_{PGD}) (G_{SUB} + j\omega C_{SUB}) \right)^{-1/2}
\] (4.7)

\[
\gamma_{PGD}(\omega) l_{PGD} = \sqrt{\frac{G_{SUB} + j\omega C_{SUB}}{G_{PGD} + j\omega C_{PGD}}}
\] (4.8)

The transmission line parameters of distributed gate electrodes are extracted from the simulation of thru1 standard in step II, with the equivalent circuit provided in Fig. 4.7(b). Initially, the contact pads-related parasitics obtained from the first step are deembedded from the full-wave simulation results of thru1 standard using

\[
\left[ Y^{PADS} \right] = \left[ Y^{THRU1} \right] - \left[ Y^{PADS} \right],
\] (4.9)

where \( Y^{PADS} \) is admittance matrix description of distributed substrate network in Fig. 4.4(b), and \( Y^{GATE} \) is the \( Y \)-matrix representation of gate electrode-related parasitic couplings. Thereafter, \( Y \)-to \( S \)-matrix transformation of \( Y^{GATE} \rightarrow S^{GATE} \) is performed, and the resulting \( S \)-parameters are plugged into Eqs. (4.2)-(4.3) to compute characteristic impedance \( Z_{0EG}(\omega) \) and propagation constant \( \gamma_{EG}(\omega) \) of the gate electrodes. The transmission line parameters of distributed drain electrode are retrieved from the simulation of thru2 standard in step III, with the equivalent circuit seen in Fig. 4.7(c). Similarly to the case of thru1 standard, simulation data of thru2 standard is first rearranged to cancel the influence of pad parasitics and obtain auxiliary admittance matrix \( Y^{DRAIN} \), which stands for the admittance matrix representation of drain electrode-related parasitic couplings. Subsequently, \( Y \)-to \( S \)-matrix conversion of \( Y^{DRAIN} \rightarrow S^{DRAIN} \) is carried out, and the resulting \( S \)-parameters are entered into Eqs. (4.2)-(4.3) to straightforwardly determine the characteristic impedance \( Z_{0ED}(\omega) \) and propagation constant \( \gamma_{ED}(\omega) \) of the drain electrode. Source electrode resistance \( R_{ES} \) and inductance \( L_{ES} \) are identified from the
simulation of short1 standard in step IV, with the equivalent circuit presented in Fig. 4.7(d). To accomplish this goal, simulation results of short1 standard is first corrected for the effects of pad parasitics by subtracting \([Y^{PADS}]\) from \([Y^{SHORT1}]\), yielding \([Y^A] = [Y^{SHORT1}] - [Y^{PADS}]\). Following this, the auxiliary admittance matrix \([Y^A]\) is converted into transmission (ABCD)-matrix of \([T^A]\), which is pre-multiplied by the inverse of transmission matrix representation \([T^{GATE}]\) of the gate electrodes to acquire source electrode transmission matrix of

\[
[T^{SOURCE}] = [T^{GATE}]^{-1} [T^A].
\] (4.10)

Source electrode resistance \(R_{ES}\) and inductance \(L_{ES}\) can eventually be calculated as

\[
R_{ES} = \text{Re} \left\{ \frac{1}{T_{21}^{SOURCE}} \right\},
\] (4.11)

\[
L_{ES} = \text{Im} \left\{ \frac{1}{T_{21}^{SOURCE}} \right\} / \omega .
\] (4.12)

Gate-to-drain mutual inductance of \(L_{MGD}\) is derived from the simulation of short2 standard in step V, with the equivalent circuit shown in Fig. 4.7(e). To start with, the effects of pad-related parasitics are deembedded from the simulation data of short2 standard by calculating \([Y^{MUTUAL}] = [Y^{SHORT2}] - [Y^{PADS}]\). Removal of the pad-related parasitics is succeeded by the transformation of auxiliary admittance matrix \([Y^{MUTUAL}]\) into impedance matrix \([Z^{MUTUAL}]\). By incorporating the elements of \([Z^{MUTUAL}]\) into a numerical optimization routine, one can easily extract gate-to-drain mutual inductance of \(L_{MGD}\). Finally, inter-electrode capacitance-conductance pairs of \((C_{EGSD}, G_{EGSD})\), \((C_{EGD}, G_{EGD})\), and \((C_{EDSD}, G_{EDSD})\) are estimated from the simulation of open standard in step VI, with the equivalent circuit depicted in Fig. 4.7(f). For this purpose, the influence of parallel-connected pad-parasitics are first subtracted from the simulation data of open standard by applying \([Y^{ELECTR}] = \)
Figure 4.8: Micrographs of the fabricated on-wafer HEMT test structures in a two-port ground-signal-ground (GSG) configuration. (a) PADS. (b) THRU1. (c) THRU2. (d) SHORT1. (e) SHORT2. (f) OPEN.

\[ [Y^{\text{OPEN}}] - [Y^{\text{PADS}}] \]. Then, a numerical optimization tool can be utilized to obtain the values of inter-electrode capacitances and conductances. The initial parameter estimations acquired from equations (4.4)-(4.12) serve as high-quality starting values for further numerical optimization through least squares error fitting procedure. The accuracy of the proposed distributed-element parasitic extraction routine is evaluated by calculating the normalized error metric [173] between the full-wave simulated and modeled S-parameters of the device. The average percentage error is less than 10% for the test structures described in Fig. 4.6.
4.2 Experimental Verification

To validate the accuracy of the proposed distributed-element HEMT extrinsic equivalent circuit extraction routine, the device structure and the respective test standards, with the dimensions given in Fig. 4.2, are first created and full-wave simulated over the frequency range of 10-750 GHz. Afterwards, the suggested test structures are fabricated by depositing single-layer metal on a semi-insulating GaAs substrate. Shown in Fig. 4.8 are the die photographs of the fabricated HEMT test standards. The evaporated interconnecting metallization is chosen to be gold with thickness of 0.2 µm. The loss tangent of the substrate is set to 0.009 in EM simulations [142], which is in accordance with the low-loss feature of GaAs material system. $S$-parameter measurements of the fabricated test patterns are taken by using non-contact probe setup [174] over the mmW and sub-mmW frequency range of 90-650 GHz. Thereafter, a selection of simulated and measured $S$-parameters are compared to decide the degree of agreement between the frequency responses acquired from full-wave EM simulations and experimental data.

The gate, drain, and source inter-pad capacitance-conductance pairs of $(C_{PGSL}, G_{PGSL})$, $(C_{PGD}, G_{PGD})$, and $(C_{PDSL}, G_{PDSL})$ are shown in Figs. 4.9(a) and 4.9(b). Regarding the substrate conductances, the linearly increasing behavior with frequency is in close agreement with complex-valued dielectric constant relation of $G(\omega)/C(\omega) = \omega \tan \delta$ [237]. The characteristic impedance and attenuation constant of gate and drain electrodes are plotted in Figs. 4.10(a) and 4.10(b). In contrast to the case of constant-valued device access metallization resistances reported previously in the literature [238], the extracted values of device electrode resistance and the consequent attenuation constant increase rapidly as the working frequency is raised from mmW to
sub-mmW band. This dramatic rise in interconnect metallization resistance originates from the current crowding phenomena, which is defined as the constriction of high-frequency current flow to the outer boundary of the conductor. Concerning the source electrode resistance and inductance, the retrieved values based on full-wave simulation of short1 test structure are given in Figs. 4.11(a) and 4.11(b). The extracted value of gate-to-drain mutual inductance $L_{MGD}$ based on full-wave simulation of short2 standard is displayed in Fig. 4.11(b). Regarding the gate-to-drain inter-electrode capacitance $C_{EGD}$, the obtained value based on full-wave simulation of open test pattern is $\sim 5.7$ fF.

In order to verify the accuracy of the proposed distributed HEMT parasitic equivalent circuit model, the contact pad- and device electrode-related parasitic elements estimated in the first four steps of parasitic extraction algorithm are substituted into the equivalent circuits of thru2 and short1 test fixtures sketched in Figs. 4.7(c) and 4.7(d). Graphed in Figs. 4.12(a) and 4.12(b) is comparison of predicted, measured,
Figure 4.10: Characteristic impedance and attenuation constant of gate and drain electrodes. (a) $Z_{0EG}$, and $Z_{0ED}$. (b) $\alpha_{EG}$, and $\alpha_{ED}$.

Figure 4.11: Device electrode-related resistance and inductance terms. (a) $R_{ES}$. (b) $L_{ES}$, and $L_{MGD}$.

and modeled $S$-parameters for thru2 and short1 test patterns in steps III and IV of parameter extraction. The $S$-parameters obtained from full-wave EM simulation
Figure 4.12: Comparison of simulated, measured, and modeled $S$-parameters for thru2 and short1 test standards. (a) Transmission coefficient $S_{21}^{\text{THRU2}}$. (b) Reflection coefficient $S_{11}^{\text{SHORT1}}$.

exhibit close agreement with the measured data over a very wide frequency bandwidth. Besides, the simulated $S$-parameters based on the extracted parameters of the proposed distributed equivalent circuits in Figs. 4.7(c) and 4.7(d) can accurately reconstruct the frequency response of EM field couplings over the mmW and sub-mmW band. However, the traditional lumped-element model is incapable of capturing the attenuation, propagation delay, and the corresponding phase shift across the terminals of the device in sub-mmW region. Frequency response of lumped-element equivalent circuit starts to diverge from the full-wave simulated behavior at $\sim 250$ GHz, where the electrical length of the device is $\sim \lambda_{\text{EFF}}/10$. The sharply varying impedance profile with respect to frequency can be better monitored by looking at effective series transfer impedance $Z_{\text{SERIES}}^{\text{THRU2}}(\omega)$ of thru2 standard, shown in Fig. 4.13.
For a device with dimensions much smaller than the guided wavelength $\lambda_{\text{EFF}}$, conventional lumped-element equivalent circuit approximation of Fig. 4.3(a) would be valid, and one would observe steadily increasing effective series transfer resistance $R_{21}(\omega)$ and reactance $X_{21}(\omega)$ as a function of frequency. However, as the device dimensions become comparable to a fraction of the effective wavelength at high frequencies, the rate of increase in $X_{21}(\omega)$ and $R_{21}(\omega)$ gradually drops, and the slope eventually becomes negative for electrically large devices. This nonmonotonic variation of effective series transfer impedance as a function of frequency is direct consequence of the distributed behavior of the device under study, and it is very clearly exemplified by the impedance behavior plotted in Fig. 4.13.
Figure 4.14: Comparison of predicted, measured, and modeled $S$-parameters for short2 and open test patterns. (a) Reflection coefficient $S_{22}^{\text{SHORT2}}$. (b) Transmission coefficient $S_{21}^{\text{OPEN}}$.

To further establish the accuracy of the developed distributed-element parasitic model extraction routine, the whole set of EM field coupling effects identified throughout the six steps of parasitic extraction algorithm are assembled together in the equivalent circuits of short2 and open test patterns indicated in Figs. 4.7(e) and 4.7(f). Plotted in Figs. 4.14(a) and 4.14(b) is comparison of simulated, measured, and modeled $S$-parameters for short2 and open test structures in steps V and VI of parasitic extraction. As demonstrated by Figs. 4.14(a) and 4.14(b), full-wave EM simulation can closely predict the measured $S$-parameters over a very wide bandwidth. Similarly to the case of thru2 and short1 standards, the proposed distributed model can accurately track the frequency response of EM field interactions over the investigated frequency range, while the lumped-element model fails to account for attenuation,
propagation delay, and the consequent phase shift across the device terminals in sub-mmW band. The continuously increasing transmission coefficient $S_{21}^{\text{OPEN}}$, plotted in Fig. 4.14(b), is explained by the fact that the distributed gate-to-drain inter-electrode capacitance $C_{\text{EGD}}$ provides an RF current flow path with steadily decreasing capacitive reactance. It is also important to point out that the transition from capacitive RF current transport at low frequency to inductive current transport at sub-mmW frequencies is captured properly with the aid of gate-to-drain mutual inductance of $L_{\text{MGD}}$. As the frequency rises, a progressively more significant disagreement emerges between full-wave simulated and modeled $S$-parameters in the absence of this inductive feedback component, as clearly illustrated in Figs. 4.15(a) and 4.15(b). Consequently, it is indispensable to include gate-to-drain mutual magnetic flux linkage as a separate circuit element into the distributed parasitic equivalent circuit of HEMT to maintain the modeling accuracy at terahertz frequencies.

4.3 Impact of Parasitic Couplings on RF Performance of HEMTs

The next step in HEMT characterization is to assess the impact of parasitic couplings on RF performance of HEMTs. For this purpose, intrinsic small-signal equivalent circuit elements of a demonstrated device from the literature is incorporated into the extrinsic parasitic couplings retrieved by utilizing the full-wave EM simulation-based approach elaborated in this chapter. Subsequent to the creation of complete small-signal equivalent circuit of the device, the degree of degradation in gain and noise performance caused by each parasitic element can be conveniently determined from circuit analysis.
Figure 4.15: Comparison of simulated and modeled transmission coefficient $S_{21}^{\text{OPEN}}$ for open test structure in the presence and absence of gate-to-drain mutual inductance component $L_{MGD}$. (a) $S_{21}^{\text{OPEN}}$ on polar plot. (b) Logarithmic magnitude of $S_{21}^{\text{OPEN}}$.

Intrinsic nonlinear subcircuit of HEMT per unit gate width is composed of the applied bias voltage-dependent elements depicted in Fig. 4.16 [239]. The intrinsic nonlinear components are related to the active device operation, and they are thought of as being independent of the operating frequency. Following the measurement-based characterization of nonlinear intrinsic device, the extracted intrinsic component values are integrated into the per unit gate width extrinsic small-signal equivalent circuit model of HEMT, sketched in Fig. 4.17. In this incremental extrinsic equivalent circuit network, the parasitic elements are extracted by employing the full-wave EM simulation-based methodology described in this chapter. Thereafter, the per unit gate width extrinsic equivalent circuit in Fig. 4.17 is multiplied by $W_G/N$ ($W_G$ is the total gate width of the device), and $N$ such stages are cascaded to obtain the overall
semi-distributed (sliced) model of HEMT [240], depicted in Fig. 4.19. Each stage is modeled as an intrinsic HEMT with gate width of $W_G/N$, and the consecutive stages are connected through lossy coupled transmission line elements to obtain a discretized approximation of the distributed behavior. In this sliced HEMT model, the electrically-short gate and drain electrode transmission line sections are approximated by the low-pass $\pi$-networks shown in Fig. 4.18. The unit finger width $W_F$ in Fig. 4.18 stands for the width of single gate finger of the device. The number of cascaded stages $N$ in semi-distributed HEMT model should be chosen such that the electrical length of each cell is substantially less than a fraction of effective wavelength at the maximum expected frequency of application. The gate and drain feed regions are treated independently as tapered transmission lines in order to account for the inevitable differences in the field distribution. As the number of slices $N$
Figure 4.17: Extrinsic small-signal equivalent circuit of HEMT per unit gate width, including parasitic components.

As the gate length is increased, the semi-distributed model converges to a fully-distributed one (complete sliced model) [241], which provides greater accuracy but only at the expense of additional computational complexity due to the necessity of solving coupled differential equations for model extraction. The accuracy of the sliced model can be easily improved to the desired level simply by increasing the number of cascaded elementary HEMT stages, and it can be embedded into computer-aided-design (CAD) routines.
of circuit simulators very conveniently. After the creation of semi-distributed HEMT model in Fig. 4.19, the impact of extrinsic parasitic couplings on speed and noise performance of the device is investigated through straightforward circuit simulation.

The device considered here for high frequency performance analysis is an AlN / GaN / AlGaN HEMT fabricated on a high-thermal conductivity silicon carbide substrate [92]. It has two-fingers, with 20 nm gate-length, and total gate width of \( W_G = 2 \times 37.5 \mu m \). Since very little information is released about the overall geometric shape of the device, the remaining lateral and longitudinal dimensions are chosen accordingly for the subsequent analysis of distributed parasitic coupling effects. So as to analyze the effect of EM field interactions on microwave performance of the selected device, the measurement-based nonlinear intrinsic equivalent circuit parameters specified in [92] are integrated into the \( N=10 \)-stage semi-distributed HEMT equivalent circuit of Fig. 4.19. Then, a circuit simulator is utilized to obtain the
short-circuit current gain ($|H_{21}|^2$), and Mason’s unilateral power gain ($G_U$) curves of intrinsic and extrinsic devices, plotted in Fig. 4.20.
Figure 4.19: Semi-distributed (sliced) model of HEMT, including intrinsic nonlinear and extrinsic linear parasitic elements. Transmission line sections are used to represent the low-pass π-network equivalent of electrically-short transmission line elements described in Fig. 4.18.
The computed unity current-gain and power-gain cutoff frequencies of the intrinsic device are $f_{\text{INT}}^{\text{T}} = 475$ GHz, and $f_{\text{INT}}^{\text{MAX}} = 3220$ GHz. For the extrinsic device, the cutoff frequencies are estimated as $f_{\text{EXT}}^{\text{T}} = 398$ GHz, and $f_{\text{MAX}}^{\text{EXT}} = 387$ GHz. The calculated extrinsic cutoff frequencies are in reasonable correlation with the measured values of $f_{\text{T}}^{\text{EXT}} = 454$ GHz, and $f_{\text{MAX}}^{\text{EXT}} = 444$ GHz reported in [92], considering the fact that only a few dimensions of the overall device geometry are specified. In order to reveal the necessity of distributed-element perspective toward sub-mmW HEMT modeling at terahertz frequencies, the extrinsic cutoff frequencies of semi-distributed HEMT equivalent circuit in Fig. 4.19 are calculated as a function of the number of cascaded stages $N$, and the resulting values are shown in Fig. 4.21. As it is seen in Fig. 4.21, the extrinsic transition frequency $f_{\text{T}}^{\text{EXT}}$ is almost independent of
the number of cascaded stages \( N \), while the extrinsic maximum oscillation frequency \( f_{\text{EXT}}^{\text{MAX}} \) depends strongly on the number of stages in the semi-distributed HEMT equivalent circuit network. The negligible effect of distributed gate resistance on \( f_{\text{EXT}}^{\text{MAX}} \) is explained by the fact that the device is driven by an ideal current source in \( f_{\text{EXT}}^{\text{MAX}} \) simulation configuration. For the case of \( f_{\text{EXT}}^{\text{MAX}} \), the calculated values initially exhibit a steep rise for small number of cascaded stages \( N \), and then converge to a steady-state value for relatively large number of stages. The lumped-element HEMT parasitic equivalent circuit of Fig. 4.3(a) with a single stage (\( N=1 \)) yields a very pessimistic performance prediction because the incoming RF signal is assumed to be attenuated by the entire gate resistance \( R_{\text{EG}} \), before it gets amplified by the intrinsic transconductance \( G_{\text{M}}^{\text{INT}} \). However, in actual case, as the incoming RF signal propagates along the gate width, the attenuation by gate resistance \( R_{\text{EG}} \), and amplification by intrinsic transconductance \( G_{\text{M}}^{\text{INT}} \) take place incrementally as suggested by the semi-distributed equivalent circuit of HEMT in Fig. 4.19. That is why the \( f_{\text{EXT}}^{\text{MAX}} \) in Fig. 4.21 is observed to increase with a decreasing slope as a function of the number of cascaded stages \( N \). The necessary number of cascaded stages \( N \) for accurate modeling of wave propagation effects is dependent on the gate width of the device and the frequency of operation. The gate and drain electrode transmission line sections interconnecting two consecutive stages in semi-distributed HEMT equivalent circuit of Fig. 4.19 need to be electrically much shorter than the operating wavelength. It is noteworthy to emphasize that, as the number of cascaded stages \( N \) is raised continuously, the semi-distributed HEMT model approaches the fully distributed model [242], and \( f_{\text{EXT}}^{\text{MAX}} \) stabilizes around a steady-state value. This concave shape of \( f_{\text{EXT}}^{\text{MAX}} \) curve as a
Figure 4.21: Extrinsic unity current-gain \( f_{\text{EXT}}^{T} \), and power-gain \( f_{\text{MAX}}^{\text{EXT}} \) cutoff frequencies as a function of the number of cascaded stages \( N \).

The extent of deterioration in \( f_{\text{EXT}}^{T} \) caused by the parasitic couplings can be more conveniently explained by inspecting the following expression of \( f_{\text{EXT}}^{T} \) for lumped-element equivalent circuit approximation of HEMT in Fig. 4.3(a)

\[
\frac{1}{2\pi f_{\text{EXT}}^{T}} \approx \left( \frac{C_{\text{GS}}^{\text{EXT}} + C_{\text{GD}}^{\text{EXT}}}{G_{\text{M}}^{\text{INT}}} \right) + C_{\text{GD}}^{\text{EXT}} \left( R_{S}^{\text{EXT}} + R_{D}^{\text{EXT}} \right) \\
+ \left( C_{\text{GS}}^{\text{EXT}} + C_{\text{GD}}^{\text{EXT}} \right) \left( R_{S}^{\text{EXT}} + R_{D}^{\text{EXT}} \right) \frac{G_{\text{DS}}^{\text{EXT}}}{G_{\text{M}}^{\text{INT}}},
\]

where \( C_{\text{GS}}^{\text{EXT}} = C_{\text{GS}}^{\text{INT}} + C_{\text{PGS}} + C_{\text{EGS}} \), and \( C_{\text{GD}}^{\text{EXT}} = C_{\text{GD}}^{\text{INT}} + C_{\text{PGD}} + C_{\text{EGD}} \) are extrinsic gate-to-source and gate-to-drain capacitances [244]. For the device under study, the contributions of second and third terms to the summation in Eq. (4.13) are less than 10%, and 5%, respectively. Unlike \( R_{S}^{\text{EXT}} \) and \( R_{D}^{\text{EXT}} \), the gate resistance \( R_{\text{EG}} \) has no impact on \( f_{\text{EXT}}^{T} \), because the device is assumed to be excited by
an ideal current source in $f_{T}^{\text{EXT}}$ calculation. Consequently, so as to minimize the influence of EM field interactions on $f_{T}^{\text{EXT}}$, it is imperative to minimize the ratio of

$\frac{(C_{GS}^{\text{EXT}} + C_{GD}^{\text{EXT}})}{(C_{GS}^{\text{INT}} + C_{GD}^{\text{INT}})}$, which can be conceived as a useful metric for quantifying the contribution of extrinsic gate-to-source and gate-to-drain capacitive couplings to the intrinsic device capacitances.

The effect of parasitic couplings on $f_{\text{MAX}}^{\text{EXT}}$ is much more pronounced than that on $f_{T}^{\text{EXT}}$, as exemplified in Fig. 4.20. This is because $f_{T}$ quantifies the capability of the device to amplify RF current driving the input gate terminal. Hence, parasitic interconnect resistances play a secondary role in determination of $f_{T}^{\text{EXT}}$, as also implied by Eq. (4.13). In contrast, $f_{\text{MAX}}$ measures how much power gain is obtainable from an amplifier at the frequency of operation. The $f_{\text{MAX}}^{\text{EXT}}$ value is therefore impacted by the ohmic losses associated with the resistive access elements in the parasitic equivalent circuit. Accordingly, the $f_{\text{MAX}}$ is more representative figure of merit for assessing the high frequency performance of a device. The dependence of $f_{\text{MAX}}^{\text{EXT}}$ on parasitic couplings can be better understood by investigating the following expression of $f_{\text{MAX}}^{\text{EXT}}$ for lumped-element equivalent circuit approximation of HEMT in Fig. 4.3(a)

$$f_{\text{MAX}}^{\text{EXT}} \approx f_{T}^{\text{EXT}} \frac{f_{T}^{\text{EXT}}}{2 \sqrt{(R_{G}^{\text{EXT}} + R_{S}^{\text{EXT}} + R_{GS}^{\text{INT}})} (C_{DS}^{\text{EXT}} + 2 \pi f_{T}^{\text{EXT}} C_{GD}^{\text{EXT}})} \tag{4.14}$$

where $R_{G}^{\text{EXT}} = R_{EG}$, and $C_{DS}^{\text{EXT}} = C_{DS}^{\text{INT}} + G_{PDSL} + G_{EDS}$ are extrinsic gate resistance and output conductance [245] - [246]. It is immediately apparent from the preceding formulation that a sizeable fraction of the reduction in $f_{\text{MAX}}^{\text{EXT}}$ arises from the interconnect resistances of $R_{G}^{\text{EXT}}$ and $R_{S}^{\text{EXT}}$, which are linked directly to the device topology, i.e., the number of gate fingers $N_{GF}$ and unit finger width $W_{F}$.

One of the primary difficulties faced by RF integrated circuit designers is to be able to access devices with very low noise contribution. This is because the signal being
amplified by the wireless communication receiver is at the same time distorted by the random fluctuations generated by the device itself. The sensitivity and dynamic range of the entire receiver architecture is predetermined by the noise performance of frontend low noise amplifier, which is dependent on the noise characteristic of the devices being deployed in the implementation of that LNA. The design of an LNA requires careful balancing of many tradeoffs between the stringent requirements of high gain to suppress the noise contribution of the mixer, low noise to enhance receiver sensitivity, wide bandwidth to accommodate multiple wireless standards simultaneously, proper input and output impedance matching to minimize return loss, low power dissipation to increase battery life, stability to prevent occurrence of oscillations, linearity to achieve high dynamic range, and compact size to occupy less of the expensive chip
area. Since the foremost function of LNA is to keep the overall noise figure of the whole RF front-end circuitry within acceptable levels, noise optimization is one of the major priorities in LNA design. From a circuit designer’s perspective, it is critical to be capable of forecasting the noise contribution of various components that make up the circuit, so that necessary measures can be taken to alleviate the unavoidable loss of signal-to-noise ratio as the received signal is processed to recover information content.

With the assistance of substantial technological advancements, the performance of integrated HEMT devices has been enhanced at a very fast pace, and they became well suited for multigigahertz MMIC design. In consideration of this rapid progress, the noise performance of intrinsic device has been enhanced substantially with aggressive technology scaling, while the noise contribution of extrinsic resistive elements started to play increasingly more significant role in determination of overall noise performance [247] - [248]. Indeed, overall noise characteristic of high-speed nanoscale HEMTs has already started to be decided by the thermal noise contribution of surrounding parasitic elements, particularly at submillimeter-wavelengths. As a consequence, it is of crucial significance to examine the impact of extrinsic parasitic couplings on the high-frequency noise performance of deeply scaled HEMTs.

In order to analyze the noise performance of the selected device, two-temperature noise model developed by Pospieszalski is adopted [195]. This empirical noise model proposed by Pospieszalski is explained with the aid of a noise equivalent circuit of HEMT per unit gate width [249], delineated in Fig. 4.16, which takes gate leakage current also into account. This two-parameter noise model incorporates two noise sources into the conventional intrinsic small-signal equivalent circuit of HEMT, which are gate noise voltage source \(v_{\text{NGS}}\) at the input, and drain noise current source \(i_{\text{NDS}}\)
at the output. The power spectral densities of these noise sources are suggested as being directly proportional to noise coefficients, also known as equivalent noise temperatures, of $T_G$ and $T_D$. These two noise sources are specified in terms of their mean square values of $\overline{v_{NGS}^2} = 4kT_G(G_{GS}^{\text{INT}r}/\Delta z)\Delta f$ and $\overline{i_{NDS}^2} = 4kT_D(G_{DS}^{\text{INT}r}/\Delta z)\Delta f$, where $k$ is the Boltzmann constant, and $\Delta f$ is frequency bandwidth. The noise created by the gate leakage current is regarded as a shot-noise with mean quadratic value of $\overline{i_{NGS}^2} = 2qI_{GS}\Delta f$, where $q$ is the electron charge. Finally, the noise generated by the gate-to-drain channel charging resistance of $R_{GD}^{\text{INT}r}$ is treated as a thermal noise with mean square value of $\overline{v_{NGD}^2} = 4kT_{\text{AMB}}(R_{GD}^{\text{INT}r}/\Delta z)\Delta f$, where $T_{\text{AMB}}$ is the ambient temperature of the device. The DC gate leakage current density is assumed to be 10 nA/mm in [184]. The equivalent gate temperature $T_G$ is, within measurement errors, identified to be equal to ambient temperature $T_{\text{AMB}}$ of the measurement setup, which is set to the standard temperature of $T_0 = 290$ K, in our analysis. The equivalent drain temperature $T_D$ is assumed to be 5000 K, which is in alignment with the acceptable range of $T_D$ values reported in [250]. Thermal noise contribution of the extrinsic interconnect resistances in the semi-distributed equivalent circuit of Fig. 4.19 is also taken into consideration, so as to reveal the relative significance of parasitic elements in the determination of overall noise performance of a highly scaled sub-mmW HEMT. Plotted in Fig. 4.22 are the computed minimum noise figure $NF_{\text{MIN}}$, and the associated power gain $G_{\text{ASSOC}}$ of intrinsic and extrinsic device, which are acquired from the circuit simulation of semi-distributed HEMT equivalent circuit in Fig. 4.19.

It is readily apparent from Fig. 4.22 that the overall noise performance is dominated by the extrinsic parasitic components surrounding the device, as the operating
frequency moves into millimeter-wave range. The sharply increasing noise figure of
the extrinsic device with respect to frequency is also accompanied by a rapid de-
crease in the associated power gain. Accordingly, the performance of a very low-noise,
high-speed, and high-gain intrinsic device is completely restricted by the EM field in-
teractions external to the device, and the overall performance is decided by the quality
of these parasitic components interfacing the device to the outside world. The obvious
limitation of noise performance by the parasitic EM field coupling effects is actually
analogous to the one that is observed for $f_{\text{EXT}}^{\text{MAX}}$ in Fig. 4.20. This evident similarity
in terms of the impact of extrinsic elements on overall speed and noise performance
indicates existence of a close relationship between $f_{\text{EXT}}^{\text{MAX}}$ and $NF_{\text{MIN}}$. So as to gain
insight into the effect of parasitic components on microwave noise performance, the
following expression of $NF_{\text{MIN}}$ for lumped-element equivalent circuit approximation
of HEMT in Fig. 4.3(a) is utilized [202] - [204]

$$NF_{\text{MIN}} \approx 1 + \frac{f}{f_{\text{EXT}}^{\text{MAX}}} \sqrt{\frac{G_{\text{DS}}^{\text{EXT}}}{G_{\text{INT}}^{\text{M}}}} \frac{T_D}{T_0} \cdot \sqrt{1 + \left(\frac{2 f_{\text{EXT}}^{\text{MAX}}}{f_C}\right)^2 G_{\text{M}}^{\text{INT}} \left(R_{G}^{\text{EXT}} + R_{S}^{\text{EXT}} + R_{GS}^{\text{INT}}\right)},$$

(4.15)

where $f_C = G_M/2\pi C_{GS}^{\text{INT}}$ is the intrinsic cutoff frequency [251]. It is clearly realizable from Eq. (4.15) that the parasitic parameters restricting high-frequency power
gain characteristics of nanometer gate-length HEMTs are also effective in increase
of $NF_{\text{MIN}}$ and degradation of microwave noise performance of these devices. Hence,$f_{\text{EXT}}^{\text{MAX}}$ is one of the most representative criteria to compare RF performance of trans-
sistors, for applications necessitating high-gain and low-noise. Having examined the
impact of EM field couplings on speed and noise characteristics of nanoscale HEMTs,
full-wave EM simulation-based device topology optimization will now be exemplified.

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4.4 Layout Optimization for RF Performance Enhancement

The final step in HEMT distributed parasitic equivalent circuit characterization is to acquire the capability of device design optimization. In a multi-finger transistor configuration, the RF circuit designer is given two degrees of freedom to optimize the device performance, which are the number of gate fingers $N_{GF}$ and unit finger width $W_F$. The total gate width $W_G$ can be computed as $W_G = N_{GF} \times W_F$. As the transistor channel length is scaled down to sub-100 nm range, layout optimization for minimization of EM field coupling effects and advancement of speed and noise performance becomes even more essential. The fundamental figures of merit for evaluating the speed and noise performance of a device are unity current-gain and power-gain cutoff frequencies of $f_T$, and $f_{MAX}$, minimum noise figure $NF_{MIN}$, and associated power gain $G_{ASSOC}$, as explained in the previous section. It is well known that the elements of admittance matrix $[Y^{INT}]$ for the intrinsic small-signal equivalent circuit are linearly proportional to the total gate width $W_G$ of the device [252]. Since a different scaling rule holds true for each extrinsic component as a function of finger number and unit finger width, different parasitic components affect the various aspects of the performance in distinct directions as the device size is changed. Hence, it is imperative to investigate foregoing performance metrics with respect to the device size so as to identify the optimum finger number and unit finger width based on either one or several of the above four figures of merit. The eventual goal of this section is to provide a qualitative explanation of optimum device layout selection so as to assist RF integrated circuit designers in creating high-performance receiver front-end circuits.
Figure 4.23: Extrinsic unity current-gain and power-gain cutoff frequencies as a function of unit finger width $W_F$, and number of gate fingers $N_{GF}$. (a) $f_T^{EXT}$. (b) $f_{MAX}^{EXT}$.

Figure 4.24: Contour plot of extrinsic unity current-gain and power-gain cutoff frequencies as a function of unit finger width $W_F$, and number of gate fingers $N_{GF}$. (a) $f_T^{EXT}$. (b) $f_{MAX}^{EXT}$.
During the device size optimization, as the number of gate fingers or unit finger width is adjusted, the proportionately scaled version of intrinsic small-signal equivalent circuit elements are brought together with the parasitic components for the following analysis of RF gain and noise behavior by employing straightforward circuit simulation. For device speed optimization, the current-gain and power-gain cutoff frequencies of $f_T$ and $f_{\text{MAX}}$ are investigated with respect to the varying device periphery. Plotted in Figs. 4.23(a) and 4.24(a) is unity current gain cutoff frequency $f_{\text{T}}^{\text{EXT}}$ of extrinsic device as a function of the gate finger number $N_{\text{GF}}$ and width per finger $W_F$. As seen in Fig. 4.23(a), the $f_{\text{T}}^{\text{EXT}}$ is roughly independent of the number of gate fingers $N_{\text{GF}}$ as long as the width per finger $W_F$ is kept unchanged. This characteristic of $f_{\text{T}}^{\text{EXT}}$ as a function of finger number $N_{\text{GF}}$ is actually in agreement with the expression in Eq. (4.13). The numerator and the denominator of the first term $(C_{\text{gs}}^{\text{EXT}} + C_{\text{gd}}^{\text{EXT}}) / G_M^{\text{INT}}$ in the summation scale proportionally with the finger number, and therefore the ratio stays constant. A similar interpretation also applies to the second and third terms in Eq. (4.13). The value of $f_{\text{T}}^{\text{EXT}}$ is observed to be increasing as a function of unit finger width with a decreasing slope, and finally converging to a fixed value. The initial steep climb of $f_{\text{T}}^{\text{EXT}}$ as a function of increasing width per finger is due to the severe drop of the first term in Eq. (4.13) for excessively small unit finger width. The intrinsic transconductance $G_M^{\text{INT}}$ varies linearly with the finger width, while the rate of increase for the total parasitic capacitance of $(C_{\text{gs}}^{\text{EXT}} + C_{\text{gd}}^{\text{EXT}})$ looking into gate terminal is less than linear due to virtually constant offset extrinsic inter-pad capacitance of $C_{\text{PGSL}}$. Nevertheless, as the finger width is raised incessantly, the contribution of $C_{\text{PGSL}}$ to $C_{\text{gs}}^{\text{EXT}}$ becomes increasingly more unimportant, and the $f_{\text{T}}^{\text{EXT}}$ stabilizes around a steady-state value. This concave shape of $f_{\text{T}}^{\text{EXT}}$
curve with respect to finger width $W_F$ with initially positive and finally zero slope is consistent with simulation- and measurement-based studies conducted previously on the subject [211] - [212].

The variation of $f_{\text{EXT MAX}}$ with respect to the unit finger width $W_F$ and the number of gate fingers $N_{GF}$ is presented in Figs. 4.23(b) and 4.24(b). It is recognized that the $f_{\text{EXT MAX}}$ is decreasing as a function of increasing width per finger. It is already clarified that the $f_{I T}$ increases with a downward slope, and eventually approaches a fixed value, as the unit finger width is raised continuously. On the other hand, the extrinsic elements of $R_{\text{EXT G}}$ and $C_{\text{EXT GD}}$ scale linearly as a function of unit finger width, and they result in an unavoidable deterioration in $f_{\text{EXT MAX}}$ for rather large values of finger width, as implied by Eq. (4.14). Another problem with decrease of width per finger for $f_{\text{EXT MAX}}$ optimization emerges when the finger width gets unreasonably small. For a device with disproportionately short finger width, the offset inter-pad parasitic capacitance of $C_{\text{PGSL}}$ overwhelms the intrinsic gate-to-source and gate-to-drain capacitances of $C_{\text{INT GS}}$ and $C_{\text{INT GD}}$. Therefore, the $f_{I T}$ drops dramatically for unnecessarily small values of unit finger width, as illustrated in Fig. 4.23(a). This inevitable drop in $f_{I T}$ leads ultimately to degradation in $f_{\text{EXT MAX}}$, as also indicated by Eq. (4.14). As a consequence, the value of finger width for optimum $f_{\text{EXT MAX}}$ should be chosen cautiously to address the tradeoff between short finger width to reduce the gate resistance $R_{\text{G EXT}}$, and adequately large one required to restrain the adverse influence of offset gate-to-source inter-pad capacitance $C_{\text{PGSL}}$. This characteristic of $f_{\text{EXT MAX}}$ with respect to the unit finger width is in close agreement with simulation- and measurement-based results reported previously in the literature [213] - [214].
Figure 4.25: Minimum noise figure and associated power gain of extrinsic device at 50 GHz as a function of unit finger width $W_F$, and number of gate fingers $N_{GF}$. (a) $NF_{MIN}$. (b) $G_{ASSOC}$.

It is also realized from Fig. 4.23(b), the $f_{MAX}^{EXT}$ can be enhanced by around 10% by choosing a device with two gate fingers and 25$\mu$m finger width.

So as to optimize the noise performance of the selected HEMT with respect to device periphery, the minimum noise figure $NF_{MIN}$ is examined as a function of gate finger number $N_{GF}$ and gate width per finger $W_F$. Shown in Figs. 4.25(a) and 4.26(a) is the variation of extrinsic $NF_{MIN}$ as the number of gate fingers $N_{GF}$ and unit finger width $W_F$ are adjusted. As recognized from Fig. 4.25(a), the value of $NF_{MIN}$ goes up as the unit finger width is raised. The $NF_{MIN}$ increases with respect to unit finger width since the extrinsic gate resistance $R_{G}^{EXT}$ and gate-to-drain feedback capacitance $C_{GD}^{EXT}$ scale proportionately as a function of width per finger. These two extrinsic components lead to a degradation in $f_{MAX}^{EXT}$ and a corresponding increase in $NF_{MIN}$, as also implied by Eq. (4.15). This behavior is in fact foreseeable if the $NF_{MIN}$ expression in Eq. (4.15) and the variation of $f_{MAX}^{EXT}$ in Fig. 4.23(b) are
Figure 4.26: Contour plot of minimum noise figure and associated power gain of extrinsic device at 50 GHz as a function of unit finger width $W_F$, and number of gate fingers $N_{GF}$.
(a) $NF_{MIN}$.  (b) $G_{ASSOC}$.

inspected together. The intrinsic and extrinsic device parameters restricting high-frequency power gain performance and hence $f_{MAX}^{EXT}$ of the device are indeed the same as those which undermine the noise performance and obstruct the development of low-noise microwave integrated circuits. Accordingly, the $f_{MAX}^{EXT}$ is proposed as the most representative indicator for comparing the RF performance of transistors, for both high-frequency and low-noise applications [253] - [254]. It is noticeable from Figs. 4.23(b) and 4.25(a) that the variation of extrinsic $NF_{MIN}$ with respect to width per finger is approximately the inverse of that exhibited by $f_{MAX}^{EXT}$, supplying a simulation-based support for the qualitative accuracy of the expression in Eq. (4.15). The convex shape of $NF_{MIN}$ curve as a function of width per gate finger $W_F$ with gradually rising slope is in close correlation with simulation-based results reported previously in the
literature [216] - [217]. As it is also realized from Fig. 4.25(a), the $NF_{\text{MIN}}$ can be decreased by roughly 10% by choosing a device with two gate fingers and 25$\mu$m finger width. Variation of the second most critical noise performance metric $G_{\text{ASSOC}}$ as a function of device topology is closely related to that of $NF_{\text{MIN}}$. Plotted in Figs. 4.25(b) and 4.26(b) is the dependence of extrinsic associated power gain on the gate finger number $N_{\text{GF}}$ and width per gate finger $W_{F}$. The characteristic of $G_{\text{ASSOC}}$ as a function of number of gate fingers and unit finger width is roughly the inverse of that exhibited by $NF_{\text{MIN}}$. Hence, the foregoing discussion for the $NF_{\text{MIN}}$ behavior with respect to device layout applies to $G_{\text{ASSOC}}$ as well. Similarly to the cases of $f_{\text{MAX}}^{\text{EXT}}$ and $NF_{\text{MIN}}$, the value of $G_{\text{ASSOC}}$ can be improved by around 5% by selecting a device with two gate fingers and 25$\mu$m gate finger width. In conclusion, the minimum noise figure and highest associated power gain are acquired from the device having the largest value of $f_{\text{MAX}}$, justifying the utilization of $f_{\text{MAX}}$ as the foremost performance measure for comparing the speed and noise characteristics of various device technologies.

4.5 Conclusion

We have proposed a distributed-element parasitic equivalent circuit model for ultra-short gate-length HEMTs, that can accurately reconstruct the frequency response of EM field couplings in THz band. Additionally, we have developed a novel systematic multi-step distributed parasitic model extraction algorithm. The accuracy of the recommended extraction methodology has been established through extensive comparisons between simulated, measured, and modeled frequency responses of the suggested test structures up to 750 GHz. It has been confirmed that it is necessary
to incorporate gate-to-drain mutual inductance \( L_{MGD} \) as a separate distributed element in order to capture the increasingly detrimental effect of inductive feedback path from output-to-input at THz frequencies. The proposed distributed model and the previously studied lumped model have been extracted simultaneously to clearly demonstrate the drawbacks of lumped-element perspective toward HEMT modeling at submillimeter-wavelengths. The distributed model has been verified to achieve the desired broadband accuracy, while the lumped model has failed to account for attenuation, propagation delay, and the resultant phase shift across the terminals of the device in terahertz band. The device has been recognized to exhibit distributed effects once its physical length has exceeded one tenth of the effective wavelength \( \lambda_{EFF} \). The obtained results supply useful insight into the major geometry- and material-dependent electrically- and magnetically-driven power dissipation mechanisms of HEMTs. Following the study of EM field coupling phenomena, intrinsic nonlinear small-signal equivalent circuit of a HEMT has first been incorporated into the extracted distributed parasitic components to create the overall semi-distributed HEMT model. Subsequently, the adverse impact of EM field interactions on speed and noise performance has been evaluated through straightforward circuit analysis. It has been shown through a full-wave EM simulation-based parametric study that 10% increase in \( f_{MAX}^{EXT} \), 10% decrease in \( NF_{MIN} \), and 5% increase in \( G_{ASSOC} \) at 50 GHz are achievable via optimization of device gate finger number, and unit finger width. Finally, use of full-wave EM simulation tools instead of fabrication and measurement of test standards is a cost-effective solution to the challenges of device characterization in the sub-mmW frequency range.
Chapter 5: Conclusions and Future Work

Over the past decade, with the aid of intense research and development efforts in academia and industry, impressive advances have been accomplished in the field of terahertz science and technology. As the new opportunities arise in a wide range of application areas including imaging, sensing, communications, security, and surveillance, the field continues its evolution by exploiting and transforming the device concepts from the neighboring microwave and infrared bands. Various impediments to the progress in semiconductor device technology have been overcome, but a considerable range of challenges remain especially at the level of device characterization and subsequent circuit integration. This dissertation was meant to bring a new perspective to deal with the challenges of device modeling at THz frequencies. It was intended to come up with a novel characterization technique that will allow integrated circuit designers to perform optimization not only at the system level but also at the component level without getting concerned about the possible inaccuracies of device models supplied by the manufacturers.

Specifically, the new contributions can be summarized as follows:

- Proposal of lumped- and distributed-element parasitic equivalent circuit models for sub-mmW SBDs and HEMTs in THz band.
- Implementation of novel systematic multi-step lumped and distributed model extraction algorithms.

- Formulation of an analytical procedure to extract gate-to-drain mutual inductance in lumped-element parasitic equivalent circuit of mmW HEMTs.

- Simulation-based and experimental validation of the accuracy and robustness of the suggested characterization techniques up to 750 GHz.

- Verification of the broadband accuracy provided by the proposed lumped- and distributed-element extrinsic equivalent circuits.

- Assessment of the effect of parasitic couplings on detection/mixing performance of SBDs and speed/noise performance/power gain of HEMTs.

- Enhancement of the conversion efficiency of a diode-based mixer through antenna-to-device conjugate impedance matching and device geometry optimization.

- Improvement of speed, noise performance, and power gain of mmW and sub-mmW HEMTs via optimization of device layout.

To summarize, Chapter 2 presented a distributed equivalent circuit model for sub-mmW SBDs that can accurately reproduce the frequency response of EM field interactions in THz band. Additionally, a novel systematic multi-step distributed model extraction methodology was developed. The validity of the recommended extraction procedure was justified through extensive comparisons with the experimental results provided in the literature. The proposed distributed model and the previously studied lumped model were extracted concurrently to clearly demonstrate the shortcomings of lumped-element approach toward SBD modeling at submillimeter wavelengths.
The distributed model was verified to achieve the desired broadband accuracy, while the lumped model failed to account for propagation delay and the corresponding phase shift across the terminals of the device in terahertz band. The obtained results provide useful insight into the major electrically- and magnetically-driven power dissipation mechanisms of SBDs, including ohmic metallization losses, losses caused by finite substrate conductivity, leaky passivation dielectric losses, and losses due to dramatically increasing series resistance of epitaxial and buffer layers. The adverse effect of EM field couplings on diode detection and mixing performance was analyzed. The major parasitic components that are most detrimental to the microwave performance were identified, and readily optimized through subsequent circuit analysis. It was demonstrated through a full-wave EM simulation-based parameteric study that conversion efficiency of an HBD-based single-ended passive mixer design at 1 THz can be improved by more than $\sim 10$ dB via antenna-to-device conjugate impedance matching and reduction of air bridge-to-pad capacitance. Fine-tuning the length of air bridge was proven to provide another degree of freedom that can potentially bring further performance enhancement. The calculated optimum responsivity and NEP values were observed to be in reasonable agreement with the measured data in the literature.

Chapter 3 presented a lumped-element parasitic equivalent circuit model for sub-micron gate-length HEMTs that can accurately reconstruct the frequency response of EM field couplings in the mmW frequency band. Following this, a novel systematic multi-step parasitic model extraction algorithm was developed. An analytical procedure was offered for the first time to extract the gate-to-drain mutual inductance $L_{MGD}$, which introduces an increasingly detrimental inductive feedback path.
from drain to gate at high frequencies. The accuracy and robustness of the suggested extraction methodology were established through extensive comparisons between simulated, measured, and modeled frequency responses of the proposed test standards up to 325 GHz. The presented lumped-element parasitic equivalent circuit was demonstrated to achieve the desired broadband accuracy over the low-microwave and millimeter-wave frequency range. The obtained results are useful in terms of gaining insight into the geometry- and material-dependent electrically- and magnetically-driven power dissipation mechanisms of HEMTs. The adverse impact of EM field couplings on HEMT gain and noise performance was investigated. The key parasitic components that are most harmful to the microwave performance were determined, and conveniently optimized through subsequent circuit analysis. Design guidelines were offered for optimum device layout selection to attain the utmost speed and noise performance. It was demonstrated through a full-wave EM simulation based parametric study that 20% improvement in $f_{\text{EXT MAX}}$, 20% reduction in $NF_{\text{MIN}}$, and 10% increase in $G_{\text{ASSOC}}$ at 20 GHz are realizable via optimization of device gate finger number, and unit finger width.

Chapter 4 presented a distributed-element parasitic equivalent circuit model for ultra-short gate-length HEMTs that can accurately reproduce the frequency response of EM field couplings in THz band. Additionally, a novel systematic multi-step distributed parasitic model extraction algorithm was developed. The validity of the recommended extraction methodology was established through extensive comparisons between simulated, measured, and modeled frequency responses of the suggested test structures up to 750 GHz. The proposed distributed model and the previously studied lumped model were extracted simultaneously to clearly demonstrate the drawbacks of
lumped-element perspective toward HEMT modeling at submillimeter-wavelengths. The distributed model was verified to achieve the desired broadband accuracy, while the lumped model failed to account for attenuation, propagation delay, and the resultant phase shift across the terminals of the device in terahertz band. Following the study of EM field coupling phenomena, the adverse effect of EM field interactions on HEMT gain and noise performance was evaluated. A semi-distributed HEMT model was utilized to account for the wave propagation phenomena along the active device electrodes during normal transistor operation as an amplifier. The key parasitic components that are considerably detrimental to the microwave performance were identified, and readily optimized through subsequent circuit analysis. Design guidelines were provided for optimum device layout selection to achieve the highest attainable speed and noise performance. It was shown through a full-wave EM simulation based parametric study that 10% increase in $f_{\text{EXT}}^\text{MAX}$, 10% decrease in $NF_{\text{MIN}}$, and 5% increase in $G_{\text{ASSOC}}$ at 50 GHz are achievable via optimization of device gate finger number, and unit finger width.

This dissertation clearly demonstrates that utilization of full-wave EM simulation tools instead of fabrication and measurement of test standards is a convenient and cost-effective solution to the challenges of device modeling at THz frequencies. Finally, the suggested full-wave EM simulation-based characterization and performance optimization methodology will enable RF engineers to select the optimum layout for diodes and transistors used in a variety of circuit applications including low-noise amplifiers, voltage-controlled oscillators, power amplifiers, and mixers. The device modeling concepts introduced in this dissertation can be used as a starting point for exploring several future research topics including the following:
• The frequency-dependent table-based equivalent circuit elements can be replaced with ideal frequency independent ones through integration of transformer-coupled networks into the suggested circuit models. In this way, the proposed equivalent circuits can be made fully compatible with transient analysis in commonly used circuit simulators.

• The parasitic-aware small signal equivalent circuits extracted by using the formulated characterization methodology can be used for more accurate bottom-up construction of large-signal equivalent circuit models.

• The knowledge of parasitic elements provided by the presented modeling technique can be employed for more reliable extraction of fitting parameters in empirical noise models.

• A solid state device simulator can be used for intrinsic device characterization. The resulting nonlinear intrinsic elements can be combined with the linear parasitic components obtained from full-wave EM simulation. In this way, the overall performance of the device can be predicted and also optimized without having to fabricate and measure a separate device each time a critical parameter is varied.

• The proposed characterization and performance optimization guidelines can be applied to antiparallel-connected SBDs being deployed in subharmonic mixer implementations.

• The offered modeling strategy can be extended to characterize the parasitic couplings of heterojunction bipolar transistors (HBTs), which together with
HEMTs represent the most frequently used solid-state devices in THz integrated circuit modules.
Bibliography


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