Advanced Channel Engineering in III-Nitride HEMTs for High Frequency Performance

DISSERTATION

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By

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Abstract

In this thesis, we have investigated and overcome the major limiting factors of intrinsic and parasitic parameters in III-Nitride high electron mobility transistors for high frequency performance with a combined study of simulations and experimental work.

The high frequency RF performance of these transistors is severely degraded when short-channel effects, and parasitic resistances are present. To investigate short-channel effects, first, we have developed a simulation model for Ga-polar and N-polar HEMT structures, and found the main reasons for these degradations are drain-induced barrier-lowering and space-charge-limited current injection. To mitigate this, a strong electrostatic back-barrier structure from N-polar orientation is suggested. Secondly, the effect of quantum displacement in GaN HEMTs were investigated using both simulation and experimental measurements. It was discovered that the quantum displacement in a highly scaled device can give more than 2x change in the gate-source capacitance between two different orientations. Therefore it is imperative that the device design for such highly scaled devices consider quantum displacement effects in order to avoid short-channel effects.

Another limiting factor from extrinsic elements is the parasitic resistances, especially from contact resistance. To achieve low-resistance non-alloyed Ohmic contacts, we developed two new process technologies that included an inserted graphene layer between
metal and AlGaN, and a graded n+ AlGaN Ohmic layer. Both approaches utilized the current path where no barrier exists. In this work, we set the record low contact resistance of 0.049 Ω·mm for Ga-polar technology using the graded AlGaN scheme.

The most crucial factor for improving high frequency performance for III-Nitride HEMTs is the saturation of the effective electron velocity. We have modeled the velocity saturation in GaN channel based on LO phonon emission, and explain the phenomena of rapidly decreasing behavior transconductance. This model was also applied to 2-D device simulation where it was possible to obtain the DC and RF characteristics matching to the experimental results.

To overcome the fast reduction in $g_m$ and $f_T$, we have introduced a polarization graded channel in AlGaN/GaN HEMT and graded AlGaN HFET to tailor the charge profile, and demonstrated a flat $g_m$ profile for the first time in field-effect-transistor structure. The high frequency performance of this engineered channel was measured from a highly scaled graded AlGaN HFET with advanced process technology including contact layer regrowth and e-beam lithography. Although the flat $g_m$ improved the linearity of $f_T$ and $f_{max}$, they do not stay flat due to an increasing capacitance profile in a regular 2 × 50 µm device. With further scaling of the device width, we obtained an increasing $g_m$ profile which can compensate the increment of capacitance, and finally we demonstrated flat $f_T$ and $f_{max}$ profile which has been unseen in any field-effect-transistors.

All these results shown in this thesis can contribute to further improvements in high frequency and high power performance of III-Nitride HEMTs for the future RF application beyond mm-Wave frequency.
Dedicated to Chanhee
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**Fields of Study**

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Table of Contents

Abstract ........................................................................................................................................... ii

Dedication ........................................................................................................................................ iv

Acknowledgments ............................................................................................................................ v

Vita ................................................................................................................................................... viii

Table of Contents ........................................................................................................................... xv

List of Tables .................................................................................................................................... xix

List of Figures ................................................................................................................................... xx

Chapter 1 Introduction ...................................................................................................................... 1

1.1 Why III-Nitride RF transistors .................................................................................................. 3

1.2 Motivation: High frequency operation of III-Nitride HEMTs for mm-Wave PAs and the limiting factors. .................................................................................................................. 6

1.3 Main limiting factors in scaled III-Nitride HEMTs ................................................................. 9

1.3.1. Short-channel-effects ......................................................................................................... 9

1.3.2. Parasitic resistances, $R_S$ and $R_D$ ................................................................................ 11

1.3.3. Underperforming Saturation Electron Velocity, $v_{sat,n}$ ................................................. 13

1.3.4. Transconductance ($g_{m}$) reduction .................................................................................. 14
1.4 Overview of the dissertation ................................................................. 16

Chapter 2 Short-Channel-Effects: Charge Confinement and Quantum Displacement.... 18

2.1 GaN-based HEMT structure with Polarization Engineering.......................... 20

2.2 Simulation of Short-Channel Effects in N- and Ga-polar AlGaN/GaN HEMTs .... 23

2.2.1 Device Structures for Simulation ................................................................... 23

2.2.2 Physical Models in Simulation ..................................................................... 25

2.2.3 Simulation Results and Analysis .................................................................. 27

2.3 Quantum Capacitance in N-polar GaN/AlGaN/GaN Heterostructures............. 35

2.3.1 Growth, Fabrications and Measurements .................................................... 36

2.3.2 Analysis and Comparison with Ga-polar AlGaN/GaN HEMT .................... 40

Chapter 3 Low-Resistance Non-alloyed Ohmic Contacts ........................................ 46

3.1 Ohmic Contact Formation between Metal and AlGaN/GaN Heterostructure via
Graphene Insertion ......................................................................................... 49

3.1.1 Growth/Synthesis of Materials and Fabrications ......................................... 49

3.1.2 Measurements and Analysis .................................................................... 52

3.2 Recess-Free Non-alloyed Ohmic Contacts on Graded AlGaN HFETs .......... 58

3.2.1 Growth and Fabrication ........................................................................... 59

3.2.2 Measurements and Analysis .................................................................... 63

3.3 Summary ..................................................................................................... 68
Chapter 4 Optical Phonon Emission and Its effects on The Effective Electron Velocity in GaN Channel ................................................................. 70

4.1 Hot-Phonon Induced Electron Velocity Saturation ................................. 72

4.2 Other Physical Models ........................................................................... 77

4.2.1 Charge Modulation: Polarization and Surface Charge ....................... 77

4.2.2 Semi-insulating GaN Buffer .............................................................. 78

4.3 Validation of New Model and Discussion ............................................. 83

4.3.1 Simulations and Results ................................................................. 83

4.4 Summary ......................................................................................... 91

Chapter 5 Polarization-Graded Channel HFETs with High Linearity of $g_m$ and $f_T$ .... 93

5.1 Flat Transconductance in AlGaN/GaN HEMTs using Polarization-Induced Channel Engineering ................................................................. 95

5.1.1 Structure Design, Growth and Fabrications ...................................... 97

5.1.2 Characterizations and Discussion ...................................................... 101

5.2 Highly Scaled Polarization-Graded AlGaN FETs .................................. 103

5.2.1 1st generation: GaN/graded AlGaN(0→45%)/GaN .......................... 104

5.2.2 2nd generation: Graded AlGaN (0→50%)/GaN ............................ 106

5.3 Summary ......................................................................................... 115
Chapter 6 Conclusions and future work ................................................................. 116

6.1 Conclusions ........................................................................................................ 116

6.1.2 Non-alloyed Ohmic contact ........................................................................ 119

6.1.3 Low electron velocity in GaN channel device ........................................... 120

6.1.4 Flat $g_m$ and $f_T$ ..................................................................................... 121

6.2 Future works ..................................................................................................... 122

6.2.1 Optimization of device scaling and process technology ......................... 123

6.2.2 New channel material for higher frequency operation ............................. 123

6.2.3 Expansion of the simulation modeling ....................................................... 124

Appendix A Derivation of Small-Signal Circuit Parameters ............................. 126

Appendix B Simulation Codes ............................................................................ 130

B.1 ATLAS code for AlN/InAlN/AlN/GaN HEMT [185] in 4.3.1 ......................... 130

B.2 C-code library of the optical-phonon mediated velocity saturation model .... 137

Appendix C Process Traveler for the 2nd gen. Graded AlGaN HFETs ............ 139

Bibliography .......................................................................................................... 145
List of Tables

Table 1.1 Properties of III-nitride materials compared to other semiconductors ............. 4
Table 1.2 Names and units of the parameters consisting Eq. (1.2) – (1.4).......................... 8
Table 2.1 Important parameter values, models and solving method for simulation........ 26
List of Figures

Figure 1.1 Summary of the applications of III-nitride semiconductors ......................... 2

Figure 1.2: Output power range of RF power amplifiers with different semiconductor materials with commercial/reported output powers of a single GaN-based PA in a form of a discrete device [39-43] or a MMIC [44-48] .................................................................................................................. 5

Figure 1.3 (a) A schematic of a highly scaled III-N HEMT with a heavily doped (regrown) Ohmic regions, SiNx/dielectric passivation, and T-gate, (b) the corresponding small-signal circuit diagram of (a) .................................................................................................................. 7

Figure 1.4: $f_T \cdot L_g$ product vs. aspect ratio ($L_g/d$) plot of GaN-based HEMT reported in the literature [54-80]. Short-channel effects due to Drain-induced barrier-lowering (DIBL) were found from both single-heterojunction and double-heterojunction structures .......... 10

Figure 1.5: The historical progress in the improvement of high frequency response of GaN-based HEMTs [54-80]. It shows a significant boost from 2009-2010 when the n+(In)GaN Ohmic regrowth was invented .................................................................................................................. 12

Figure 1.6: $f_T$ vs. $L_g$ plot of GaN-based HEMT reported in the literature [54-80]. The solid lines show the ideal peak $f_T$ value for highly scaled sub-micron gate length with $v_{e,peak}$ of $2.7 \times 10^7$ [52] and $1.38 \times 10^7$ cm/s [53] .................................................................................................................. 13

Figure 1.7: A comparison of measured and simulated transfer characteristics of a highly scaled InAlN/GaN HEMT structure reported in [79] .................................................................................................................. 15

Figure 2.1 Polarization in wurtzite crystalline GaN .......................................................... 20
Figure 2.2 Strain-Engineered Polarization in the over-layer or cap-layer ..................... 21
Figure 2.3 Polarization-induced 2DEG formation in (a) Ga-polar and (b) N-polar AlGaN/GaN HEMT structures ................................................................................................................................. 21
Figure 2.4 Structure Schematics and Energy Band Diagrams (a) Ga-SHEMT  (b) Performance Improved Ga-DHEMT (c) N-HEMT .................................................. 24
Figure 2.5 Various Electron velocity vs. Electric field profile. Monte Carlo data was obtained from Silvaco MOCASIM simulation................................................................. 26
Figure 2.6 Current-voltage characteristics of each device (a) Ga-SHEMT  (b) Performance Improved Ga-DHEMT (c) N-HEMT ................................................................. 28
Figure 2.7 Conduction energy band profiles along the channel of each HEMTs with different drain bias which are corresponding to the solid line in Figure 2.6 ............ 30
Figure 2.8 1-D and 2-D Conduction band profiles in the intrinsic channel layer ($V_{GS} = -3 V =V_p– 1 V$, and $V_{DS} = 0$ and 10 V) ............................................................................................................................ 32
Figure 2.9 Threshold Voltage shift of Ga-DHEMT and N-HEMT ................................. 34
Figure 2.10 The 2DEG formation and quantum displacement in (a) Ga-polar and (b) N-polar AlGaN/GaN heterostructures .................................................................................. 36
Figure 2.11 (a) Epitaxial structure and (b) energy band diagram of an N-polar AlGaN/GaN heterostructure ................................................................................................. 37
Figure 2.12 Fabrication process of Schottky diode for a thickness-series .................. 39
Figure 2.13 Measured physical cap thickness vs. electrical cap thickness which includes 5nm of Al2O3 layer ($\epsilon_r=9$) [125]......................................................................................... 40
Figure 2.14 (a) First and second sub-band wave-functions in the quantum well, and (b) equivalent circuit diagram of the given N-polar AlGaN/GaN heterostructure.................. 42

Figure 2.15 The quantum displacement \( \Delta d \) of each sub-band from the hetero-interface toward the Schottky barrier.................................................................................................................. 43

Figure 2.16 The total capacitance as functions of the cap thickness which includes 5nm of Al2O3 layer................................................................................................................................. 44

Figure 3.1(a) Measured XRD \( \omega-2\theta \) scan and corresponding fit from as-grown AlGaN/GaN structure and AFM image of surface morphology. (b) Raman spectrum from transferred CVD graphene on AlGaN/GaN substrate with D, 2D, and G bands indicated. .............................................................................................................................................. 50

Figure 3.2 Schematic diagram showing the structure of the Cr/Graphene/AlGaN/GaN structure. In the case of the reference device, the graphene layer is removed.............. 52

Figure 3.3 Current-voltage characteristics of Cr/AlGaN/GaN and Cr/Graphene/AlGaN/GaN................................................................................................................................. 53

Figure 3.4 Current-voltage characteristics as a function of temperature (77 to 300 K, \( 2\times10^{-6} \) Torr) of: (a) Cr/AlGaN/GaN (inset: Schottky diode turn-on at 250 K) and (b) Cr/Graphene/AlGaN/GaN ........................................................................................................................................ 54

Figure 3.5 Schematic energy band diagrams of: (a) Cr/AlGaN/GaN Schottky diode under zero-bias (top) and forward-bias (bottom) conditions, and (b) Cr/Graphene/AlGaN/GaN junction (proposed). .................................................................................................................... 56
Figure 3.6 Energy band diagram, epitaxial structure, charge diagram of channel region (a-c) and Ohmic regions (d-f), respectively. (g) SEM image of the regrown source and drain Ohmic with metal contacts.

Figure 3.7 Schematics of (a) TLM A structure on graded AlGaN HFETs, (b) TLM B control structure for the resistance de-embedment.

Figure 3.8 Measurement results of TLM sets shown in Figure 3.7 (a) and (b) (inset: intercept of RT at zero spacing).

Figure 3.9 Schematics of (a) epitaxial structure for non-alloyed Ohmic when L=0, and (b) its current conducting path where the carrier density, $n_e > 10^{19}$ cm$^{-3}$.

Figure 3.10 The resistor network of the Ohmic contact with the parallel interface resistors connected from 3DES to each sub-band of 2DEG in the channel region.

Figure 4.1 (a,b) Sketch of electron distribution in Brillouin zone of GaN for two different values of drift velocity. (c,d) LO-phonon assisted scattering for the same two values of drift velocity. (e) LO phonon absorption and (f) stimulated emission for the same two values of drift velocity.

Figure 4.2 The electron saturation velocity vs. sheet charge density in the channel of GaN HEMTs.

Figure 4.3 The translated electron saturation velocity vs. volume charge density in the channel of GaN HEMTs for TCAD simulations.

Figure 4.4 Commonly detected trap levels, $E_t$, in high-quality GaN [177-183].

Figure 4.5 Test structure for the simulation of buffer leakage in S.I. GaN.
Figure 4.6 (a) Energy band diagram of an AlGaN/GaN HEMT for S.I. GaN buffer test structure (b) the buffer leakage I-V with various trap densities ............................................. 81
Figure 4.7 (a) Energy band diagram of an AlGaN/GaN HEMT for testing S.I. GaN buffer (b) the buffer leakage I-V with various UID GaN channel thickness........................................ 82
Figure 4.8 Schematic of the transistor structure for simulations with structural parameters ............................................................................................................................................. 83
Figure 4.9 The simulated results of (a) $I_D-V_D$ characteristics, (b) the transfer curves, (c) Frequency-gain characteristics compared with the measured results from[184]............. 85
Figure 4.10 The simulated results of (a) $I_D-V_D$ characteristics, (b) the transfer curves, (c) Frequency-gain characteristics compared with the measured results from [79]................. 88
Figure 4.11 The simulated results of (a) $I_D-V_D$ characteristics, (b) the transfer curves, (c) Freq-gain characteristics compared with the measured results from [185]................. 90
Figure 5.1 A schematic of charge distribution of a graded channel in AlGaN/GaN HEMT ............................................................................................................................................. 96
Figure 5.2 Epitaxial structure of the (a) graded channel HEMT and (b) conventional HEMT ............................................................................................................................................. 98
Figure 5.3 (a) Energy band diagram of the graded channel HEMT (b) Simulated electron density profiles and the conduction band profiles in quantum well (c) Two sub-bands occupied and the profile of the wave-functions (d) Measured C-V profiles of graded channel HEMT ............................................................................................................................................. 99
Figure 5.4 DC I-V characteristics of (a) the graded channel HEMT and (b) the conventional HEMT after gate recess ............................................................................................................................................. 102
Figure 5.5 (a) gm vs. Vgs and (b) gmi vs. Vgc for the graded channel HEMT and the conventional HEMT at Vds = 10V .......................................................... 102

Figure 5.6 (a) Schematic of the epitaxial structure and (b) energy band diagram of the Gen.1 vertically scaled graded AlGaN HFET. ................................................................. 105

Figure 5.7 (a), (b) Annealing temperature optimization for the alloyed Ohmic contacts 105

Figure 5.8 (a), (b) Annealing temperature optimization for the alloyed Ohmic contacts 106

Figure 5.9 (a) Schematic of a highly-scaled graded AlGaN HFET, (b) the measured charge profile from C-V measurement compared with a simulated charge profile ....... 107

Figure 5.10 DC characteristics of (a) $I_{DS}$-$V_{DS}$ and (b) $g_m$-$V_{GS}$ (inset: $I_{DS}$-$V_{GS}$) of a graded AlGaN HFET with $L_g$ of 250 nm and $W_g$ of $2 \times 50$ µm ................................................................. 109

Figure 5.11 The extrinsic RF performance of a graded AlGaN HFET with $L_g$ of 250 nm and $W_g$ of $2 \times 50$ µm ........................................................................................................ 111

Figure 5.12 Bias-dependent ($f_T$ and $f_{max}$) of a graded AlGaN HFET with $L_g = 250$ nm and $W_g = 2 \times 50$ µm ......................................................................................... 112

Figure 5.13 (a) DC transfer characteristics and (b) bias-dependent $f_T$ and $f_{max}$ of a graded AlGaN HFET with $L_g = 450$ nm $W_g = 2 \times 20$ µm at $V_{DS} = 6$ V ......................................................... 114

Figure A.1 Small-signal equivalent circuit of a HEMT structure ........................................ 126
Chapter 1

Introduction

The group-III nitride semiconductor material system includes aluminum-nitride (AlN), gallium-nitride (GaN), indium-nitride (InN), and their ternary and quaternary alloys with direct bandgaps ranging from 0.7 eV (InN) [1] to 6.2 eV (AlN)[2] which make it attractive for a wide range of applications. The breakthrough results of efficient Mg-doping activation by thermal annealing [3], and polarization-induced 2 dimensional electron gas (2DEG) in AlGaN/GaN heterostructure [4] provided highly efficient electronic and opto-electronic applications after the first HVPE GaN growth of GaN in 1969 [5]. These breakthroughs fueled the research on the III-nitride material resulting in the first demonstrations of multi-quantum-well (MQW) light-emitting-diodes (LEDs) [6], AlGaN/GaN high-electron-mobility-transistors (HEMTs) [7], and GaN-based laser diodes [8].

Over the years, there has been considerable maturity in epitaxial growth technology, including growth of GaN on Si [9] for a cheaper manufacturing cost. A substantial amount of processing technology also has been developed for both electronic and opto-electronic devices such as SiNx passivation [10], field-plate [11, 12], back-barrier structures [13] for
transistor applications, and omni-directional reflector [14], surface roughening [15], vertical thin-film structure [16] for LED applications. These technological breakthroughs were made only within two decades from their first demonstrations, and GaN-based devices are now gradually replacing other devices based on other materials such as GaAs and Si due to their higher efficiency.

GaN-based products such as blue/green LEDs & laser diodes [17-20], 600 V power transistors & diodes [21, 22], S- and X-bands RF high-power amplifiers [17, 23-25] have been already commercialized and are available in the market in 2013. GaN-based ultraviolet (UV) [26] and hybrid white LEDs [25] are also commercially available. In addition to light emitters and transistors, exciting research is being carried out in the area of novel
devices such as GaN quantum cascade lasers (QCLs) [27], biochemical and heat/pressure sensors [28, 29], and polarization-induced tunnel junctions [30-32].

In Figure 1.1, the major GaN-based commercialized applications and their revenue in 2012 are depicted with some of the future III-N based applications. Although LEDs and laser diodes hold more than 90% of the total $10 billion USD market of GaN industry [33], the power switching/RF power electronics are expected to grow up to $1.75 billion USD by 2021 with an explosive compound average annual growth rate (CAAGR) of 63.78% [34].

1.1 Why III-Nitride RF transistors

III-nitride semiconductor materials have several advantages over other material systems (Si, GaAs, SiC, SiGe, InP) due to the material properties listed in Table 1.1. These advantages include high breakdown field due to wide bandgap ($E_g$), high saturation velocity ($v_{Sat}$) and electron mobility ($\mu_n$), the ability to induce large charge density due to polarization engineering, high temperature operation, and high thermal conductivity ($\kappa$).

The combined figure of merit (CFoM) [35] indicates the high frequency, high power performance of the device during operation, hence including effects such as thermal conductivity. The CFoM is given by

$$CFoM = \frac{\kappa \cdot \varepsilon_r \cdot \varepsilon_0 \cdot \mu_n \cdot v_{Sat} E_{Cr}^2}{\left(\kappa \cdot \varepsilon_r \cdot \varepsilon_0 \cdot \mu_n \cdot v_{Sat} E_{Cr}^2\right)_{Silicon}}$$

(1.1)
The CFoM of III-nitride material family clearly shows their potential capability in RF performance compared to other semiconductor material systems. The CFoM is a comprehensive figure of merit compared to the application-specific figure of merits such as the high frequency performance Johnson [36] and high power performance Baliga [37] figures of merit.

After the first demonstration of an AlGaN/GaN-based RF device [38], GaN-based RF HEMTs have shown unprecedented RF performance with output power densities of 41.4 W/mm at 4 GHz [39], 30.6 W/mm at 8 GHz [40], 13.7 W/mm at 30 GHz [41], 10.5 W/mm at 40 GHz [42], and 2.1 W/mm at 80.5 GHz [43] in a form of a discrete device, and 200 W for C-band [44], 45W for X-band [45], 10 W for Ku-band [46], 15 W for K-band [25], 7 W for Ka-band [47], and 1.7 W for W-band [48] in a form of a monolithic microwave integrated circuit. Among all kinds of solid-state power-amplifier (SSPA) families, III-N HEMT-based PAs have the highest output power, and the widest application spectra range.

### Table 1.1 Properties of III-nitride materials compared to other semiconductors

<table>
<thead>
<tr>
<th>Material</th>
<th>$E_g$ (eV)</th>
<th>$\varepsilon_r$</th>
<th>$E_{Cr}$ (MV/cm)</th>
<th>$v_{Sat}$ (10^7 cm/s)</th>
<th>$\mu_n$ (cm^2/V·s)</th>
<th>$\kappa$ (W/cm·K)</th>
<th>CFoM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>1.12</td>
<td>11.7</td>
<td>0.3</td>
<td>1</td>
<td>1350</td>
<td>1.3</td>
<td>1</td>
</tr>
<tr>
<td>SiGe</td>
<td>0.7-1.1</td>
<td>11.7-16</td>
<td>0.1-0.3</td>
<td>-</td>
<td>3000</td>
<td>0.6-1.3</td>
<td>-</td>
</tr>
<tr>
<td>GaAs</td>
<td>1.42</td>
<td>12.9</td>
<td>0.4</td>
<td>0.72</td>
<td>8500</td>
<td>0.5</td>
<td>3.4</td>
</tr>
<tr>
<td>InP</td>
<td>1.35</td>
<td>13.5</td>
<td>0.5</td>
<td>0.67</td>
<td>5400</td>
<td>0.68</td>
<td>4.5</td>
</tr>
<tr>
<td>4H-SiC</td>
<td>3.26</td>
<td>9.7</td>
<td>3</td>
<td>0.8</td>
<td>700</td>
<td>3.7</td>
<td>97.9</td>
</tr>
<tr>
<td>GaN</td>
<td>3.39</td>
<td>8.9</td>
<td>3.3</td>
<td>1.4</td>
<td>2000</td>
<td>2.9</td>
<td>425</td>
</tr>
<tr>
<td>AlN</td>
<td>6.2</td>
<td>8.5</td>
<td>11.7</td>
<td>1.6</td>
<td>300</td>
<td>2.85</td>
<td>861</td>
</tr>
<tr>
<td>InN</td>
<td>0.7</td>
<td>15.3</td>
<td>-</td>
<td>2.5</td>
<td>3200</td>
<td>1.76</td>
<td>-</td>
</tr>
</tbody>
</table>

Table 1.1 Properties of III-nitride materials compared to other semiconductors
Figure 1.2: Output power range of RF power amplifiers with different semiconductor materials with commercial/reported output powers of a single GaN-based PA in a form of a discrete device [39-43] or a MMIC [44-48].

The reported power values for GaN-based transistors are nearly one order of magnitude higher than Si-based LDMOS and GaAs-based RF PAs. This has led to a reduction in the size of PAs by 30-50% compared to the conventional Si-based and GaAs-based PAs. The effect of the use of III-N HEMT-based PAs is maximized when loaded as a payload onto unmanned aerial vehicles (UAVs) or satellites. The size reduction associated with reduced cooling requirements can enable light-weight design of transceiver units, and improve cost and lifespan of UAVs and satellites activities.
1.2 Motivation: High frequency operation of III-Nitride HEMTs for mm-Wave PAs and the limiting factors.

Currently available microwave bands for wireless communications and military applications are almost saturated and high-power high-efficient RF PAs are required to satisfy a continuously increasing demand for a wider bandwidth. As mentioned in the previous section, III-nitride semiconductor-based PAs are very promising for the purpose.

Although the available output power from III-Nitride HEMT-based PAs is higher than the other semiconductor PAs’ output power, multi-stage MMICs, bulky splitters & combiners, and tuners, are still required to achieve the required output power for higher frequency bands such as W-band (75 to 110 GHz) or G-band (110 to 300 GHz). This is because of insufficient gain and output power from a single MMIC chipset. The need for multi stage amplifiers leads to a larger footprint of module, reduced efficiency, increased complexity of design, and consequently higher costs. This necessitates a single stage III-Nitride HEMT with sufficient output power and high frequency gain.

In Figure 1.3, a schematic of a highly scaled III-N HEMT is shown with the consisting small-signal circuit-elements for the given structure. With these circuit elements, the required transistor specification of the desired high-frequency gain and the output power can be determined from the unity current gain frequency, $f_T$ [49], the maximum oscillation frequency, $f_{max}$ [50], and the maximum AC output power, $P_{out}^{AC}$ which are given by
Figure 1.3 (a) A schematic of a highly scaled III-N HEMT with a heavily doped (regrown) Ohmic regions, SiNx/dielectric passivation, and T-gate, (b) the corresponding small-signal circuit diagram of (a)

\[
f_{T,\text{Extrinsic}} = \frac{g_m}{2\pi \cdot (C_{gs} + C_{gd}) \left\{ 1 + (R_s + R_D) \cdot g_{ds} + \frac{g_m}{C_{gs} + C_{gd}} \cdot C_{gd} \cdot (R_S + R_D) \right\}}
\]

\[
f_{T,\text{Intrinsic}} = \frac{1}{\left\{ 1 + (R_s + R_D) \cdot g_{ds} + 2\pi \cdot f_{T,\text{Intrinsic}} \cdot C_{gd} \cdot (R_S + R_D) \right\}}
\]

\[
f_{\max} = \frac{g_m}{2\pi \cdot (C_{gs} + C_{gd}) \cdot \sqrt{4 \cdot (R_g + R_S + R_t) \cdot g_{ds} + 8\pi \cdot f_T \cdot C_{gd} \cdot (2R_g + R_S + R_t) }}
\]

\[
f_{\max} = \frac{1}{2} \cdot \frac{1}{\sqrt{R_g + R_S + R_t} \cdot g_{ds} + 2\pi \cdot f_T \cdot C_{gd} \cdot (2R_g + R_S + R_t) }}
\]

\[
P_{\text{out}}^{\text{AC}} = \frac{I_{\text{Swing}} \cdot V_{\text{Swing}}}{8} = \frac{I_{\text{max}} (V_{\text{Br}} - V_{\text{Knee}})}{8}
\]

\[
f_T \text{ and } f_{\max} \text{ are also known for the unity gain (0dB) value of the small-signal short-circuited current gain } |h_{21}|^2 \text{ and Mason’s unilateral power gain, } U, \text{ respectively.}
\]
<table>
<thead>
<tr>
<th>Term</th>
<th>Name</th>
<th>Unit</th>
<th>Term</th>
<th>Name</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_{g}$</td>
<td>Gate inductance</td>
<td>[H]</td>
<td>$R_{i}$</td>
<td>Charging resistance</td>
<td>[Ω]</td>
</tr>
<tr>
<td>$L_s$</td>
<td>Source inductance</td>
<td>[H]</td>
<td>$g_{ds}$</td>
<td>Output conductance</td>
<td>[1/Ω]</td>
</tr>
<tr>
<td>$L_d$</td>
<td>Drain inductance</td>
<td>[H]</td>
<td>$R_{gd}$</td>
<td>Gate-drain leakage resistance</td>
<td>[Ω]</td>
</tr>
<tr>
<td>$R_c$</td>
<td>Metal-Semicon. Resistance</td>
<td>[Ω]</td>
<td>$C_{gs,p}$</td>
<td>Gate-source pad capacitance</td>
<td>[F]</td>
</tr>
<tr>
<td>$R_{sh,Lat}$</td>
<td>Lateral resistance of n' GaN</td>
<td>[Ω]</td>
<td>$C_{gd,p}$</td>
<td>Gate-drain pad capacitance</td>
<td>[F]</td>
</tr>
<tr>
<td>$R_{sh,Ver}$</td>
<td>Vertical resistance of n' GaN</td>
<td>[Ω]</td>
<td>$C_{ds,p}$</td>
<td>Drain-source pad capacitance</td>
<td>[F]</td>
</tr>
<tr>
<td>$R_{3D-2D}$</td>
<td>3D-2D interface resistance</td>
<td>[Ω]</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_{S,acc.}$</td>
<td>Source access resistance</td>
<td>[Ω]</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_{D,acc.}$</td>
<td>Drain access resistance</td>
<td>[Ω]</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{\text{max}}$</td>
<td>Drain saturation current</td>
<td>[A]</td>
<td>$g_m$</td>
<td>Intrinsic transconductance</td>
<td>[S]</td>
</tr>
<tr>
<td>$V_{\text{Knee}}$</td>
<td>Knee voltage</td>
<td>[V]</td>
<td>$V_{\text{Br}}$</td>
<td>Breakdown voltage</td>
<td>[V]</td>
</tr>
</tbody>
</table>

Table 1.2 Names and units of the parameters consisting Eq. (1.2) – (1.4)

It must be note that $f_{\text{max}}$ should be at least the same or larger than $f_T$ to have the small-signal gain beyond $f_T$ and up to $f_{\text{max}}$ [50]. More detailed derivation of the small-signal circuit elements from measured scattering parameters are described in Appendix A.

For many military applications such as Radars, and satellite communications, a small-signal gain of 10-15 dB or higher should be guaranteed. Since $|h_{21}|^2$ and $U$ are decaying with a rough slope of -20 dB/decade, the required $f_T$ and $f_{\text{max}}$ should be at least 3-5 times faster than the operating frequency, $f_{\text{op}}$ to obtain a minimum gain required, which means the transistor should have $f_T$ and $f_{\text{max}}$ beyond 300 GHz ~ 1 THz for covering upper mm-Wave frequency of W- and G-bands. Then, the specification for the desired output power can be obtained from Eq (1.4). $V_{\text{Knee}}$ is determined from $I_{\text{max}}/R_{\text{on}}$, and $V_{\text{Br}}$ typically follows the $V_{\text{Br}} \cdot L_{gd}$ product of 100 V·µm [51] where $R_{\text{on}}$ (the sum of all series resistance to the channel) and $L_{gd}$ are the on-resistance and the gate-drain spacing of the given transistor. $R_{\text{on}}$ and $I_{\text{max}}$ are the key parameters for optimization of the output power of the amplifier.
The transconductance, \( g_m \), is often estimated as \( v_{Sat} C_{gs}/L_G \) where \( v_{Sat} \) is the saturation velocity in the channel of the transistor; i.e. a higher \( g_m(v_{Sat}) \) gives a higher \( I_{max} \). For an ideal transistor of which all parasitic elements are eliminated, \( f_{T,Intrinsic} \) can be written in a more physical expression of

\[
f_{T,Intrinsic} = \frac{v_{Sat}}{2\pi \cdot L_G}
\]  

The theoretical peak electron velocity of GaN is reported to be \( 2.7 \times 10^7 \) cm/s [52]. Based on this first-order estimate desired high-frequency gain should require \( L_G \) of 40 nm to 150 nm for frequency of 300 GHz to 1 THz.

However, the emission of optical-phonon affects in a GaN-based HEMT, and the realistic saturation velocity is limited to be only \( 1.4 \times 10^7 \) cm/s which prevents GaN-based HEMTs from achieving \( f_T \) and \( f_{max} \) higher than 500 GHz [53]. Moreover, there are limitations other than the peak velocity which are discussed in the following section. This thesis explores these limitations and seeks alternative solutions of each limitation to provide methods for realization of high frequency III-nitride HEMTs.

1.3 Main limiting factors in scaled III-Nitride HEMTs

1.3.1. Short-channel-effects

In order to achieve higher \( f_T \) and \( f_{max} \), the scaling of the device dimension, especially \( L_G \), is necessary while maintaining an aspect ratio, \( L_G/d \) (\( d \): the gate-to-channel distance),
Figure 1.4: $f_T L_g$ product vs. aspect ratio ($L_g / d$) plot of GaN-based HEMT reported in the literature [54-80]. Short-channel effects due to Drain-induced barrier-lowering (DIBL) were found from both single-heterojunction and double-heterojunction structures.

...for preventing short-channel-effects which significantly degrade the high frequency gain by increasing the output-conductance, $g_{ds}$. In GaAs and InP-based HEMT technology, a typical aspect ratio of 2.5-5 is regarded as an optimum aspect ratio [81-84]. However, it was found that a larger aspect ratio of 15 at least is required for GaN-based HEMTs to minimize Short-channel effects [85, 86].

For a conventional AlGaN/GaN HEMT structure which consists of 20-30 nm of AlGaN and 1-2 nm AlN as the barrier, and GaN channel and GaN buffer, gate-recess process has been widely used to reduce the gate length below 100 nm while minimizing Short-channel effects. Due to the chemical inertness of (Al)GaN, it is required to implement a dry etching process for the gate-recess process which may cause reliability issues from a degradation of Schottky gate contact on the etched surface [58, 87].
Recently, lattice-matched InAlN/GaN HEMTs [62, 66-68, 79, 80], which have a higher aspect ratio while avoiding the dry-etching process, have shown their greatly improved high-frequency performance compared to conventional AlGaN/GaN HEMTs. However, these devices also suffer from high $g_{ds}$, therefore requiring a back-barrier structure to have a better charge confinement.

In double-heterojunction FET structure such as AlN/GaN/AlGaN and N-polar GaN/Al(Ga)N HEMTs, DIBL induced short-channel effects are greatly mitigated and it can be suppressed down till $L_g/d$ of 10 compared to $L_g/d$ of 15 for single-heterojunction FETs (Figure 1.4). Although there have been significant technological improvements for higher frequency operation, it is still necessary to investigate further the geometry for a scaled device to have better charge control and to mitigate short-channel effects even at high drain bias conditions.

1.3.2. Parasitic resistances, $R_S$ and $R_D$

The high frequency performance depends greatly on parasitic elements, especially, the resistances such the source and drain resistances, $R_S$ and $R_D$, which include the source and drain access resistance, $R_{S,Access}$ and $R_{D,Access}$, and the contact resistance, $R_C$. Although the charging delay from the gate-source capacitance, $C_{gs}$, dominates the total time delay for a long channel device, its effect reduces as the dimensions of gate footprint decrease. Therefore, the existence of these parasitic resistances plays an important role in a highly scaled HEMT [54, 76].
Figure 1.5: The historical progress in the improvement of high frequency response of GaN-based HEMTs [54-80]. It shows a significant boost from 2009-2010 when the n+ (In)GaN Ohmic regrowth was invented.

A drain access resistance ($R_D$) is inevitable in large signal amplifier transistors in order to drop voltage between the gate and the drain [88]. However, $R_S (= R_C + R_{S,\text{Access}})$ can be minimized to obtaining the highest transconductance close to its intrinsic value of $g_{m, \text{intrinsic}} = g_m/(1-R_S\cdot g_m)$ [89].

Although typical Ti/Al-based alloyed Ohmic contact formation could yield as low as 0.20 $\Omega\cdot$mm of the contact resistance [54] there are issues associated with reproducibility and reliability, especially for thin cap structures ($t_{\text{Barrier}} < 10$ nm) [90]. Si$^+$ implantation [91-93] and n$^+$ (In)GaN regrowth using molecular-beam epitaxy [79, 94, 95] have been proposed and used as non-alloyed low-resistance Ohmic contacts resulting in a substantial improvement of $f_T$. (Figure 1.5) However, this increases the complexity in fabrications as
well as the thermal budget. Thus, a new technology which does not involve such complicated regrowth process, but with a low resistance Ohmic contact is required.

1.3.3. Underperforming Saturation Electron Velocity, $v_{sat,n}$

Electron-phonon coupling is very strong in the III-Nitride materials, with optical phonon emission times being an order of magnitude lower than GaAs or Si. In the case of GaN-based HEMTs, this limits the mean-free-path ($\lambda_{OP}$) of hot electrons to be approximately 3.5 nm which is far shorter than than any other material systems [53]. As a result, GaN-based HEMTs do not display a (near) ballistic transport effects as seen in Si-MOSFETs and other III-V semiconductor HEMTs [96, 97] when gate lengths and parasitic effects are reduced.

![Figure 1.6: $f_T$ vs. $L_g$ plot of GaN-based HEMT reported in the literature [54-80]. The solid lines show the ideal peak $f_T$ value for highly scaled sub-micron gate length with $v_{e,peak}$ of $2.7 \times 10^7$ [52] and $1.38 \times 10^7$ cm/s [53].](image)
The peak measured electron velocity of GaN-based HEMTs is found to be only $1.38 \times 10^7$ cm/s [53] which is considerably lower than the theoretical value of $2.7 \times 10^7$ cm/s expected due to the phonon emission related saturation. This sets a fundamental limitation of the achievable $f_T$ and $f_{max}$ of GaN-based HEMTs.

To solve this intrinsic electron velocity issue of GaN channel, there exist two possible approaches.

1) Use of vertical transistor structures such as heterojunction bipolar transistors (HBTs), tunneling hot-electron transistors (THETs) or tunnel-emitter transistors (HETs) [98] to have a near ballistic behavior by shrinking the intrinsic electron travel path (base & base-to-collector barrier) close to $\lambda_{OP}$.

2) Substitution of GaN-channel with different channel materials with lower electron effective mass which results in a higher effective electron velocity such as high composition In(Ga)N [99, 100].

1.3.4. Transconductance ($g_m$) reduction

In the previous section, the velocity degradation resulting from optical phonon mediated electron back-scattering was explained. The amount of the velocity degradation increases with an increase in the 2DEG density in the GaN channel which is responsible for a rapid reduction in $g_m (= \partial I_{ds} / \partial V_{gs})$ after reaching a maximum value (Figure 1.6).
Figure 1.7: A comparison of measured and simulated transfer characteristics of a highly scaled InAlN/GaN HEMT structure reported in [79].

Since $g_m$ determines the current gain of the transistor, the reduction in $g_m$ directly affects high-frequency gain, $f_T$, and $f_{max}$, and may limit the $I_{max}$ when the $f_T$ and $f_{max}$ at higher current density do not satisfy the bandwidth requirements for power amplification. This has been a common problem of other field-effect-transistors in Si-MOSFETs and III-As or III-P based HEMTs. In the case of AlGaN/GaN HEMTs used for power amplification, this limits the output power, $P_{out}$ as well as the efficiency. Thus, a solution to solve this issue could enable improvements in the efficiency and linearity of RF power applications.
1.4 Overview of the dissertation

The main goal of this dissertation is to investigate the main limiting factors which limit III-N based HEMTs to obtain a higher frequency performance beyond $f_T$ & $f_{\text{max}} > 500$ GHz, and provide viable solutions for them. For this, I have developed precise device simulation modeling for III-N HEMT technology. A thorough analysis of device characterization using DC and RF measurements together with the developed simulation model was performed. New methods were introduced to reduce the parasitic resistance in the III-nitride system. Finally, less complex and more reliable advanced fabrication process technologies were developed for highly scaled III-N HEMTs.

The order of following chapters is organized to show the methodology for improving high-frequency operation by the minimization (ideally elimination) of the extrinsic RF circuit elements and the improvement of the intrinsic elements in Eq. (1.2-3).

In chapter 2, a brief introduction of polarization of wurtzite III-Nitride material system is presented. The charge confinement and the channel control of highly scaled HEMTs, which are responsible for short-channel effects with high $g_{\text{ds}}$, are investigated and compared for two different polarity of Ga- and N-polar oriented AlGaN/GaN structures using experiments and simulations. Initial work on the 2-dimensional technology computer-aided design (TCAD) and 1-dimensional self-consistent Poisson-Schrödinger calculation simulation modeling is explained.

In chapter 3, the effect from parasitic resistances on the RF performance and existing technologies for Ohmic contact formation are discussed. Two novel methods to obtain a low-resistance non-alloy Ohmic contacts are introduced. The first method is to insert a
monolayer graphene sheet between metal (Cr) and AlGaN interface in which a percolation-related transport promotes current conduction and graphene forms a virtually n-doped semiconductor. The second method is the use of grading of (Al)GaN layer with and without doping on AlGaN/GaN HFETs. This method prevents the formation of abrupt heterojunction barriers between the doped and undoped layers, and could lead to a new method for achieving low-resistance ohmic contacts without the use of regrowth or ohmic recess.

In chapter 4, systematic modeling of electron charge transport in III-N HEMTs is presented. First, the model for the hot phonon emission versus 2DEG density, which represent the LO phonon-electron interaction in GaN-based HEMT is calculated from first principles. Then, TCAD simulation results using this model are compared with the reported results which matched the simulation prediction.

In chapter 5, FET structures using a thin AlGaN composite channel with polarization grading are studied to solve the dropping $g_m$ problem. The insertion of graded AlGaN channel in a HEMT structure shows the scalability of the transistor device while maintaining a constant $g_m$. Then, the $f_T$ or velocity improvement in higher current density is demonstrated in a highly-scaled polarization graded AlGaN HFET with sub-micron gate and Ohmic regrowth technologies.
Chapter 2

Short-Channel-Effects:

Charge Confinement and Quantum Displacement

Channel length scaling is an essential step towards achieving high frequency operation for all transistor applications. Considerable efforts to scale vertical dimensions in III-Nitride HEMTs are also necessary to improve the high-frequency performance. Other material technologies have shown that devices show short-channel effects as the gate length is reduced. Scaled HEMT devices with short-channel effects lead to output conductance which degrades the transfer characteristics as well as high-frequency response. Therefore, the performance enhancement from device scaling is reduced even though the gate length can be shrunk down to 25 nm [101], and short-channel effects simply degrade $f_T$ and $f_{max}$ by increasing the output conductance $g_{ds}$ in Eq (1.2-3).

Various non-idealities are introduced due to device scaling, and short-channel effects are introduced due to poor charge confinement and low aspect ratio. Efforts to mitigate these effects included the use of a double heterojunction structure [69, 102], insulation of the buffer layer with p-type dopant [103] for better charge confinement, gate recessing technology [104] and ultra-thin (In)AlN cap layer [80, 95].
Even though several analytical models have been adopted in Ga-polar single-heterojunction HEMTs to analyze DC characteristics, there are few 2D simulations of highly scaled GaN devices [103, 105, 106]. Also, at the time this work was done, no analytical or simulation models had been developed for Ga-polar double-heterojunction HEMTS and N-polar HEMTs.

In addition, the effect of quantum displacement (also referred to quantum mechanical capacitance) has not be quantitatively established, although this effect was shown to play an important role [107]. Quantum displacement can enhance or weaken the gate-channel capacitance over the geometric capacitance as the device is vertically scaled for higher aspect ratio. This effect becomes significant at highly scaled dimensions where the wavefunction displacement is of the same order of magnitude as the physical gate-channel spacing.

In this chapter we discuss short-channel effects in GaN-based HEMTs using 2D device drift-diffusion based simulation [108] to investigate the operation of highly scaled III-Nitride HEMTs grown in both Ga-polar and N-polar directions [109]. Then, we discuss the negative quantum displacement in a N-polar AlGaN/GaN HEMT using direct comparison of physical and electrical measurements of the GaN cap thickness [110].
2.1 GaN-based HEMT structure with Polarization Engineering

One of the most unique properties in III-N material system is polarization effects \([111]\) within the wurtzite crystal structure along \(c\)-axis of the growth direction. The lack of inversion symmetry of the crystal structure leads to a strong electric dipole in each unit cell in \(c\)-axis direction (Figure 2.1 (a)). The net polarization in the material is compensated (Figure 2.1 (b)) and a net sheet charge is left on the top and bottom surface of the layer (Figure 2.1 (c)). In addition, a strain-induced piezoelectric effect can be used to engineer
Figure 2.2 Strain-Engineered Polarization in the over-layer or cap-layer

Figure 2.3 Polarization-induced 2DEG formation in (a) Ga-polar and (b) N-polar AlGaN/GaN HEMT structures
the total polarization in the material (Figure 2.2). The magnitude of polarization effects in III-N material is significantly larger than other III-V semiconductors [112].

The strong polarization field in single-layered III-N material is generally screened by counter ions in atmosphere (Figure 2.1 (d)). However, when it is terminated with another III-nitride material to form a heterojunction, the net polarization combined with the conduction band offset induces a very high sheet charge density, $n_s$, of $2\text{–}6 \times 10^{13}$ cm$^{-2}$ in the form of a 2-dimensional electron-gas (2DEG). These charges are provided by surface donors, and therefore polarization enables the formation of mobile carrier population without intentional impurity doping. The high charge density ($> 1 \times 10^{13}$ cm$^{-2}$) would not be possible in a traditional MODFET structure with impurity doping.

The most common III-nitride HEMT is the Ga-polar HEMT structure consisting of a GaN channel layer capped with a wider bandgap layer. For a simple AlGaN/GaN HEMT structure, the positive polarization charge at the bottom of GaN is canceled out with screening charges at the GaN/substrate surface, and there are donor-like surface states created on top of the AlGaN. Following the charge conservation law, the sum of the net-polarization at the AlGaN/GaN hetero-interface and the top of AlGaN induce electron charges into the 2DEG. A simple N-polar AlGaN/GaN HEMT structure is shown in Figure 2.3 (b). In this case, the net polarization induces charges a 2DEG at the upper GaN/AlGaN interface of the inverted HEMT structure.

The difference in the orientation or polarity can be considered similar to the one between a conventional cap-layer delta doping (Ga-polar) and inverted III-V HEMT technologies.
2.2 Simulation of Short-Channel Effects in N- and Ga-polar AlGaN/GaN HEMTs

In this study, we investigate Short-channel effects in GaN HEMTs with self-consistent device simulations providing a perspective of the variation in energy-bands. To emphasize Short-channel effects in different HEMT structures, only electrostatic barrier, but no S.I. buffer layer, was introduced in the structure.

2.2.1 Device Structures for Simulation

Simulations for the comparison of short-channel effects in three different AlGaN/GaN HEMT structures were carried out using the two-dimensional (2-D) device simulator Silvaco ATLAS. To analyze and to compare short-channel effects of both Ga- and N-HEMTs, we chose three different AlGaN/GaN HEMTs epitaxial structures.

The first structure is a Ga-polar AlGaN/GaN HEMT with a cap composition of 30% and thickness of 30 nm on top of 1 μm of GaN buffer layer (Ga-SHEMT, Figure 2. 4. (a)). AlGaN back-barriers were found to improve the short channel performance in previous work [13]. We have therefore included a double heterostructure HEMT consisting of 30 nm of 30% AlGaN cap layer on top of 30 nm GaN channel layer and 1 μm of 4% AlGaN backbarrier layer as the buffer layer to improve the charge confinement (Ga-DHEMT, Figure 2.4 (b)). Finally, we simulated a N-polar HEMT consisting of 30 nm GaN channel layer on top, 30 nm of 30% AlGaN layer in the middle as a barrier layer, and 1 μm thick GaN buffer layer on the bottom (N-HMET, Figure 2.4 (c)).
Figure 2.4 Structure Schematics and Energy Band Diagrams (a) Ga-SHEMT (b) Performance Improved Ga-DHEMT (c) N-HEMT
The gate-source and the gate-drain spacing were fixed at 0.1 μm and 0.5 μm, respectively. We simulated 50 nm gate length devices for each epitaxial structure, and the cap layer was recessed under the gate by 20 nm leading to a nominal gate to channel distance of 10 nm. We used the metal work-function of Ni (5.2 eV) for the gate Schottky contact. The material parameters of Al$_x$Ga$_{1-x}$N semiconductor were also introduced into the simulation.

### 2.2.2 Physical Models in Simulation

The composition dependent material structure, spontaneous polarization, and piezoelectric polarization parameters were included in the simulation to introduce the correct polarization charges at the hetero-interface [112-114]. Figure 2.4 (a) – (c) show the calculated energy band diagrams (black) and charge distributions (blue) below the gate region (solid) and the access region (dashed-dot) in the growth (c-axis) direction. The charge densities of the two-dimensional electron gas (2DEG) in the gate region (in the access region) for Ga-SHEMT, Ga-DHEMT, and N-HEMT were obtained as 1.11x10$^{13}$ (1.45x10$^{13}$) cm$^{-3}$, 0.89x10$^{13}$ (1.24x10$^{13}$) cm$^{-3}$, and 0.74x10$^{13}$ (1.07x10$^{13}$) cm$^{-3}$, respectively. The pinch-off voltage ($V_P$) of each device with the recessed gate is obtained -3 V, -2 V, and -2 V, respectively.

Palacios et al. [115] pointed out the discrepancy of the velocity-field relationship between Monte Carlo calculation and measured data. We used the experimentally measured velocity field curves from [115] and applied the Farahmand Modified Caughey-Thomas expression for group-III nitride material system [116, 117] in this work. Figure
2.5 depicts this new curve with Monte Carlo velocity-field curves, and the extrapolated curve from [115]. Both N- and Ga-polar HEMT simulations used this curve for the electron transport.

<table>
<thead>
<tr>
<th>Gate work-function</th>
<th>5.2 eV</th>
</tr>
</thead>
<tbody>
<tr>
<td>Surface Pinning</td>
<td>1.6 eV (for 30% AlGaN)</td>
</tr>
<tr>
<td>(on S &amp; D access regions)</td>
<td>0.9 eV (for GaN)</td>
</tr>
<tr>
<td>Doping density</td>
<td>$1 \times 10^{20} \text{ cm}^{-3}$</td>
</tr>
<tr>
<td>in Ohmic region</td>
<td></td>
</tr>
<tr>
<td>Simulation Models</td>
<td>SRH, FLDMOB, SPONTANEOUS, FMCT, and GANSAT</td>
</tr>
<tr>
<td>Solving Method</td>
<td>GUMMEL, NEWTON, AUTONR</td>
</tr>
</tbody>
</table>

Table 2.1 Important parameter values, models and solving method for simulation

Figure 2.5 Various Electron velocity vs. Electric field profile. Monte Carlo data was obtained from Silvaco MOCASIM simulation.
In this present study, effect of gate leakage current and charge quantization effects have not been taken into account. However, gate leakage current in an actual field effect device can strongly affect the modulation and pinch-off characteristics. A thin AlGaN layer and SiN insulator are added into an actual N-polar HEMT structure to minimize gate leakage current due to a low Schottky barrier height between gate metal and GaN in previous works [118, 119]. Introduction of high-k dielectric would be essential to mitigate the gate leakage in N-polar HEMTs while minimizing degradation due to short-channel effects.

2.2.3 Simulation Results and Analysis

DC current-voltage (I-V) characteristics of each HEMT are simulated for the gate biases ($V_{GS}$) from 0 V to $V_P$ -1 V, and for the drain biases from 0 to 10 V which are depicted in Fig. 3 (a) – (c). In Figure 2.6, the solid line of each figure shows the I-V for their $V_P$.

Short-channel effects are apparent not only from the large threshold voltage shifts but also from the high output conductance in both highly scaled Ga-polar HEMTs. However, N-HEMT maintains a low output-conductance and minimizes the threshold voltage shift in the same scaling condition with two Ga-polar HEMTs. To show drain-induced barrier lowering more explicitly in a highly scaled device, we investigated the conduction band profiles. First, the one-dimensional (1-D) conduction energy profiles in the channel of each device at pinch-off are shown in Figure 2.7 (a)-(c). The profiles were calculated at a gate bias of $V_P$ (corresponding to the solid (blue) line in Figure 2.6 (a)-(c)) with the drain bias varied between 0 to 8 V.
Figure 2.6 Current-voltage characteristics of each device (a) Ga-SHEMT (b) Performance Improved Ga-DHEMT (c) N-HEMT
Due to the poor aspect ratio, the gate channel control is lowered so that the drain bias affects the entire potential barrier in the channel of all three devices. The potential barrier between source and drain in both Ga-polar HEMTs is lowered as the drain bias increases. The poor channel control in Ga-polar HEMTs directly deteriorates the channel confinement and the output-conductance. Moreover, for Ga-DHEMT (Figure 2.7 (b)), the potential barrier at its $V_p$ is immediately lowered below the quasi Fermi level as the drain bias starts to be applied so that current can flow through the channel without any obstruction. This potential barrier lowering results in the threshold voltage shift and drain-induced barrier lowering (DIBL) in the channel. However, N-HEMT still holds its potential barrier under a high drain bias since the gate bias directly controls the potential barrier. Thus, the N-HEMT is expected to maintain good pinch-off performance and a very low output-conductance unlike the other two Ga-polar HEMTs.

Space charge injection also contributes to current flow under hard pinch-off conditions in Ga-HEMTs. A dashed-dot line in Figure 2.6 (b) shows I-V curve of Ga-DHEMT at $V_{GS} = -3$ V and Figure 2.8 (a)-(b) is the corresponding 2-D conduction band profile in the intrinsic channel layer. The applied gate bias maintains the potential barrier higher than the quasi Fermi level to prevent the current flowing through the channel at high drain bias (inset of Figure 2.8 (c)). The device, which is initially pinched off when the drain bias is low, turns on as the drain bias is increased beyond 7 V. Two vertically cut 1-D conduction band profiles show that the applied drain bias in Ga-DHEMT lowers not only the potential barrier height in the channel, but also the band-engineered back barrier in Figure 2.8 (c).
Figure 2.7 Conduction energy band profiles along the channel of each HEMTs with different drain bias which are corresponding to the solid line in Figure 2.6.
As the drain bias increases, electrons injected from source start to accumulate on the source-side gate edge of GaN/Al$_{0.04}$Ga$_{0.96}$N interface. The accumulated electrons create a field opposing the back-barrier inside the channel layer. This field compensates the back-barrier structure as the drain bias increases and forms a parasitic channel at GaN/Al$_{0.04}$Ga$_{0.96}$N interface. With the onset of the formation of this parasitic channel, current starts to flow through the channel formed at bottom GaN/Al$_{0.04}$Ga$_{0.96}$N interface rather than the actual channel at the top Al$_{0.3}$Ga$_{0.7}$N/GaN interface.

The gate of N-HEMT directly controls the field in the channel layer unlike in the case of Ga-HEMTs. Since the 2DEG channel in N-HEMT is firmly confined due to the depletion and an abrupt junction at the heterointerface, the drain field only affects the 2DEG channel. Furthermore, since the conduction band offset at GaN/Al$_{0.3}$Ga$_{0.7}$N interface creates the back-barrier structure of N-HEMT, electrostatics cannot lower the barrier structure and electrons need much higher energy to enter the Al$_{0.3}$Ga$_{0.7}$N back-barrier layer in N-HEMT. N-HEMT shows better DIBL suppression compared to Ga-polar HEMTs with the same aspect ratio, and thickness of channel layer. These advantages make N-face orientation suitable for scaled transistors. In our simulation study (not shown here,) N-HEMT starts to show output conductance when the gate length shrinks down below 25 nm.
Figure 2.8 1-D and 2-D Conduction band profiles in the intrinsic channel layer ($V_{GS} = -3$ V = $V_p$ = 1 V, and $V_{DS} = 0$ and 10 V)
The conventional definition of drain-induced barrier lowering (defined as $\Delta V_{th}/\Delta V_{DS}$) is still useful to characterize the threshold voltage shift in HEMT. In Figure 2.9 (a), Ga-DHETM shows not only a large threshold voltage shift, but also a significant degradation in the subthreshold slope unlike in N-HEMT case. Figure 2.9 (b) shows the conventional DIBL as a function of the drain bias. An integration of Figure 2.9 (b) gives the total threshold voltage shift at a certain drain bias caused by DIBL. The space-charge-limited injection through the entire channel layer mainly contributes to short-channel effects in Ga-polar HEMTs at a high drain bias ($V_{DS} > 2.5$ V) so that a large threshold voltage shift is shown in Figure 2.9 (b) for Ga-DHETM. However, N-HEMT suppresses DIBL well as expected from the I-V characteristics and the analysis of energy band diagram.

This non-linear threshold voltage shift in Ga-polar HEMTs deteriorates device pinch-off and increases output-conductance of the highly scaled Ga-polar devices significantly. According to the model here, N-polar HEMTs have low output conductance and good pinch-off control as required for RF operation. We note here that real N-polar HEMTs were found to have higher output conductance even at long gate lengths [75, 119]. Our simulations only take into account electrostatics in an idealized device. Real devices may demonstrate short channel effects due to other non-idealities such as gate leakage current, traps, and impact ionization which are not taken into account in this present study.
Figure 2.9 Threshold Voltage shift of Ga-DHEMT and N-HEMT
2.3 Quantum Capacitance in N-polar GaN/AlGaN/GaN Heterostructures

The key difference between Ga-polar and N-polar HEMT is the charge distribution in 2DEG. The inverted HEMT structure of N-polarity makes the electron wave-function spread toward the gate metal, and reduces the gate-channel distance by forming the 2-dimensional electron gas (2DEG) between the gate metal and GaN/AlGaN hetero-interface. This is opposite to normal HEMT (or MOSFET) structures where the wave-function extension toward the substrate increases the effective gate-channel distance [120] and thereby reduces the capacitance. The quantum mechanical capacitance in the inverted HEMT structure therefore enhances the gate-channel capacitance over the geometric capacitance. This effect becomes significant at highly scaled dimensions where the wavefunction displacement is of the same order of magnitude as the physical gate-channel spacing, which in the case of a normal FET is the oxide or barrier layer.

Due to the finite width of the electron wave-function along the direction of confinement, a two-dimensional electron gas (2DEG) manifests itself as a capacitor in series with the geometrical capacitance, with capacitance \( C_Q = \frac{m^*e^2}{\pi \hbar^2} \), where \( m^* \) is the electron mass transverse to the quantum well [121]. This is the quantum capacitance of a 2DEG and is related to the 2D density of states in the material.

In a typical Ga-polar AlGaN/GaN HEMT (Figure 2.10 (a)), the gate-channel capacitance \( C_G = 1/(1/C_{\text{geometric}} + 1/C_Q) \) can be simply written as \( C_G = \varepsilon/(d_{\text{physical}} + \Delta d) \) where \( \Delta d \) is the quantum displacement of 2DEG and is known to be \( \sim 2 \text{ nm} \) for single subband occupancy in a Ga-polar AlGaN/GaN HEMT [122]. However, 2DEG in N-polar structure...
Figure 2.10 The 2DEG formation and quantum displacement in (a) Ga-polar and (b) N-polar AlGaN/GaN heterostructures

is pushed toward the gate (Figure 2.10 (b)), the gate capacitance becomes \( C_G = \varepsilon / (d_{\text{physical}} - \Delta d) \), thus leading to an increased gate-channel capacitance compared to a Ga-polar structure with the same physical thickness.

In this section, we discuss the negative quantum displacement in an N-polar AlGaN/GaN HEMT with the comparison of physical and electrical measurements of the GaN cap thickness. When the cap thickness \( d \) is similar to \( \Delta d \) which is the case for highly scaled devices, \( \Delta d \) starts to play a significant and interesting role, and the negative \( \Delta d \) of N-polar HEMTs becomes very critical and advantageous to device performance. This is the first experimental report of this effect in an inverted field effect device.

2.3.1 Growth, Fabrications and Measurements

An N-polar AlGaN/GaN HEMT structure was grown on 4H-SiC substrate using plasma-assisted molecular-beam-epitaxy for the measurements of the negative quantum
Figure 2.11 (a) Epitaxial structure and (b) energy band diagram of an N-polar AlGaN/GaN heterostructure
displacement. The two-step GaN buffer layer was grown on 45 nm of AlN nucleation layer to minimize buffer leakage, dislocation density and impurity incorporation [123].

To keep the valence band edge far away from the Fermi level to avoid charge trapping by the donor-like trap found near the valence band edge [75, 124], the barrier layer grown on GaN buffer consists of 10 nm of Si-doped (N_D = 2×10^{18} cm^{-3}) GaN layer and 31.5 nm of linearly graded n-doped (N_D = 4×10^{18} cm^{-3}) AlGaN layer in which the Al-composition was graded from 5% (bottom) to 34% (top). Then, 30 nm of GaN channel layer was grown on top of the structure (Figure 2.11).

To measure capacitance-voltage characteristics, circular metal-oxide-semiconductor capacitors of 90 μm radius were fabricated on the epi-structure. Ti/Al/Ni/Au alloyed ohmic contacts were formed by rapid-thermal-annealing and the contact resistance was found to be 0.4~0.5 ohm-mm by TLM method. The GaN channel layer was etched down using low-power Cl_2-based inductively-coupled-plasma reactive-ion-etching for different durations. 5 nm of Al_2O_3 thickness (measured independently using ellipsometry) was deposited using atomic-layer-deposition to suppress the gate leakage from thin GaN cap layer. Finally, Ni was evaporated to form Schottky contacts on the etched surface (Figure 2.12).

For samples with different etch durations, capacitance–voltage (C-V) measurements (using Agilent B1500 parameter analyzer), and physical thickness measurements (using Zeiss Ultra 55 Plus FE-SEM) were taken to find the quantum displacement, Δd. From the zero-bias capacitance of C-V measurements, the electrical cap thickness was calculated as 

\[ d_{cap,electrical} = \varepsilon / C_{C-V} \]

for each etch duration (each physical thickness). Then, the calculated cap thickness is depicted in Figure 2.13 as a function of the physical thickness.
Figure 2.12 Fabrication process of Schottky diode for a thickness-series

The physical cap thickness as a function of the etch duration can be written as,

\[ d_{\text{cap, physical}}(t) = d_0 - \kappa \cdot t + d_{\text{ALD}} \]  

(2.1)

where \( t \), \( d_0 \), \( \kappa \), and \( d_{\text{ALD}} \) are the etch duration, initial cap thickness, etch rate and deposited ALD oxide thickness, respectively. Similarly, the calculated cap thickness is

\[ d_{\text{cap, electrical}}(t) = d_0 - \kappa \cdot t + \Delta d + d_{\text{ALD}} \]  

(2.2)
From Eq. (2.1) and the measured initial cap thickness, $d_{\text{physical}}(t=0)$, the etch rate $\kappa$ was found to be 0.9 Å/sec by linear fitting of the measured physical thickness (Standard deviation = 0.3%).

Since both two equations share the same components except for the quantum capacitance, the averaged $\Delta d$ value of ~-4 nm for N-polar AlGaN/GaN HEMT structure was found from Figure 2.13. This experimentally confirms that the electron wave-function spread in the inverted HEMT determines the gate to channel spacing, effectively making it smaller than the physical GaN cap thickness.

2.3.2 Analysis and Comparison with Ga-polar AlGaN/GaN HEMT

To understand the physics of the quantum spread $\Delta d$, 1-dimensional self-consistent Schrödinger-Poisson simulations [126] were done. At zero bias, two wave-functions

Figure 2.13 Measured physical cap thickness vs. electrical cap thickness which includes 5nm of Al2O3 layer ($\varepsilon_r=9$) [125]
corresponding to the first and second sub-bands of the structure (Fig. 1) were calculated and are shown in Figure 2.15 (a). The first sub-band at \( T = 300 \, ^\circ\text{K} \), \( E_0 \), was found to be 142 meV below the Fermi level with \( \Delta d \) of -1nm. For the GaN cap thickness of 30 nm, the second sub-band, \( E_1 \), (35meV above the Fermi level) shows \( \Delta d \) of -3.5 nm that agrees well with the measured \( \Delta d \) (~ 4 nm). Since \( E_1 \) is in proximity to the Fermi level can be easily occupied at room temperature [127, 128], it can be assumed that the second sub-band is occupied. Next, we carried out simulation of the C-V curve, including quantum mechanical effects. The equivalent circuit model of the gate capacitor of the given structure with two parallel capacitors associated with the occupied sub-bands is depicted in Figure 2.15 (b). We consider the case where the barrier layer consists of 5nm of \( \text{Al}_2\text{O}_3 \) and etched GaN channel layer has initial thickness 30 nm. With the variation of the GaN thickness with the etching as in the actual experiments, \( \Delta d \) of the wave-function was estimated for the first and second sub-bands.
Figure 2.14 (a) First and second sub-band wave-functions in the quantum well, and (b) equivalent circuit diagram of the given N-polar AlGaN/GaN heterostructure.
The quantum displacement $\Delta d$ of each sub-band from the hetero-interface toward the Schottky barrier is shown in Figure 2.15. The critical GaN cap thickness of 2DEG formation, $d_{cr}$, was found to be 6 nm, i.e. 11 nm with 5 nm of Al$_2$O$_3$. After the GaN layer becomes thicker than $d_{cr}$, the sheet charge density increases and the first and second sub-bands begin to be filled up in the order. Unlike $|\Delta d|$ of the first sub-band that is ~ 1 nm even for a thick GaN layer, the value for the second sub-band increases from 2.5 nm to 3.5 nm after the onset of the charge accumulation with the increasing GaN thickness. This increasing $|\Delta d|$ of the occupied second sub-band also explains the increasing C-V profile in N-polar oriented HEMT structures [129, 130].

The simulated C-V curve with two sub-bands occupancy matches well with the measured value for the range of cap thickness investigated here, as shown in Figure 2.16. For comparison, capacitance for a Ga-polar AlGaN/GaN HEMT structure with 5 nm Al$_2$O$_3$...
Figure 2.16 The total capacitance as functions of the cap thickness which includes 5nm of Al2O3 layer varying thicknesses of 34% AlGaN cap layer corresponding to GaN cap thickness of N-polar structure are also shown. As expected from the negative $\Delta d$ in the N-polar oriented HEMT structure, there is a significant increase in the gate-channel capacitance, $\Delta C_{\text{N-polar HEMT}}$ when compared to the geometric capacitance. The summation of $\Delta C_{\text{N-polar HEMT}}$ and $\Delta C_{\text{Ga-polar HEMT}}$ shows the effective difference of $C_g$ between Ga-polar oriented and N-polar oriented HEMT structures for the same physical barrier thickness. With the difference in $\Delta d$ between Ga- and N-polar HEMT structures, which is approximately 5~6 nm, the N-polar AlGaN/GaN HEMT structure can obtain additional gate capacitance value against to Ga-polar HEMT structures for the same cap thickness. In Figure 2.16, the additional capacitance value is about 15~20 % over the cap thickness of 15~35 nm. However, for mm-wave and higher frequencies, the cap thickness will be reduced further and the effects of this enhancement will be more pronounced. For example, for a physical cap thickness
of 6 nm, there is more than 2X enhancement in the gate-source capacitance between N-polar and Ga-polar structures, and consequently a higher device transconductance. We expect that this will lead to direct reduction in the parasitic delays such as the delay related to the gate-drain capacitance $C_{gd}$. 
Chapter 3

Low-Resistance Non-alloyed Ohmic Contacts

The source and drain parasitic resistance, $R_{S/D}$ are consist of the contact resistance $R_C$ and the access resistance $R_{S,\text{access}}/R_{D,\text{access}}$. For high frequency transistors, $R_C$ and $R_{S,\text{access}}$ should be minimized since the parasitic resistances of $R_S$ and $R_D$ can significantly increase the total time delay, $\tau_{\text{Total}}$. The effect of $R_S$ and $R_D$ in the total time delay can be obtained as,

$$
\tau_{\text{Total}} = \frac{1}{2\pi f_{T,\text{Ext.}}} \left[ \frac{C_{gs} + C_{gd}}{g_m} \cdot \left[ 1 + (R_S + R_D) \cdot g_{ds} + \frac{g_m \cdot C_{gd}}{C_{gs} + C_{gd}} \cdot (R_S + R_D) \right] \right] \tag{3.1}
$$

or

$$
\tau_{\text{Total}} = \tau_{\text{Int.}} + \tau_{\text{Int.}} \cdot \left( R_S + R_D \right) \cdot g_{ds} + C_{gd} \cdot (R_S + R_D) \tag{3.2}
$$

where $\tau_{\text{Int.}}$ is the intrinsic delay given by $(C_{gs}+C_{gd})/g_m$. The second and third terms in Eq. (3.2) are referred the parasitic delays in field-effect-transistor, and are responsible for the resistor divider effect and Miller effect, respectively [49]. The normalized parasitic delay components with respect to the intrinsic delay can be written as,
\[ \tau_{\text{parasitic}} = \tau_{\text{int}} \left( R_S + R_D \right) \cdot g_{ds} + \frac{C_{gd} \cdot (R_S + R_D)}{\tau_{\text{int}}} \tag{3.3} \]

In Eq. (3.3), the output conductance, \( g_{ds} \) generally increases with the drain bias and saturates, although it can become significantly high when short-channel effects occurs. The gate-to-drain capacitance, \( C_{gd} \) is relatively independent of the gate length, but is determined by the extension of the depletion region at the drain-side gate-edge and \( C_{gd} \) decreases as the drain bias increases due to the extended depletion region.

The very first Ohmic contact on AlGaN/GaN HEMT was a refractory metal stacks of Ti/Au or Ti/W, which yielded a very high contact resistance of 28 \( \Omega \cdot \text{mm} \). The high contact resistance was responsible not only for low \( f_T \) and \( f_{\text{max}} \), but also for the low maximum current density [131]. Ti/Al-based alloyed metal stacks were found to form a low resistance Ohmic contact to 2DEG [132], and this method could reduce \( R_C \) close to 0.2 \( \Omega \cdot \text{mm} \) which are more than two orders of magnitude lower value than the first Ti/Au contact.

However, the lowest value of \( R_C \) from the alloyed Ohmic contact is still much larger than the one for other III-V or Si-based RF transistor application [133]. It is also much larger than the total access resistance in an ultra-scaled device with \( L_{DS} \) below 0.5 \( \mu \text{m} \) where the total access resistance is only 0.1-0.15 \( \Omega \cdot \text{mm} \) (for sheet resistivity \( R_{sh} \) of GaN HEMTs in the range between 200 to 300 \( \Omega/\square \)). Moreover, for different epitaxial stacks, Ohmic contacts to AlGaN/GaN heterostructures require highly tailored recipes of multi-layer metallization (typically Ti/Al/Ni/Au) and annealing at high temperatures (typically above 800 \( ^\circ \text{C} \)) [134, 135] due to the large barrier height associated with the
metal/AlGaN/GaN interface. Such Ohmic contacts formed by metal spiking into the GaN layer have uncontrolled, poorly understood morphologies [134, 135], and they are known to reduce device reliability [136]. This also limits the minimum feature sizes that can be achieved in devices due to a high thermal expansion coefficient of Al, which in turn limits their high-frequency performance. Therefore, the alloyed Ohmic contact formation and the relatively high RC are major limiting factors for further improvements in high-frequency performance of GaN-based HEMTs.

Various alternative methods have been used to form low-resistance smooth Ohmic contacts including Si-containing recessed alloyed Ohmic contacts [54], and non-alloyed Ohmic contacts with Si\(^+\) ion-implantation [92, 93] or n\(^+\) (In)GaN Ohmic regrowth using molecular-beam epitaxy (MBE) contacts [137, 138]. Among those new technologies, the lowest and the most reproducible RC was obtained from MBE regrowth of n\(^+\) (In)GaN. However the associate fabrication steps are complex, and the method requires a regrowth process which is inherently complex and expensive for production.

In this chapter, we introduced two new methods to achieve a low-resistance non-alloyed Ohmic contact using an insertion of graphene and successive polarization grading schemes. Both of these methods can provide a route to achieving non-alloyed Ohmic contact to GaN.
3.1 Ohmic Contact Formation between Metal and AlGaN/GaN Heterostructure via Graphene Insertion

The isolation of single-layer graphene [139, 140] has led to the demonstration of several exciting properties of this 2-D crystal of carbon, such as ballistic conduction by massless Dirac fermions [141, 142] quantum Hall effect [141-143], and size-dependent band gap [144]. Developments in the synthesis of high-quality, large-scale graphene by epitaxial growth [145] and chemical vapor deposition (CVD) [146], has expanded the choice of substrates for the fabrication of graphene-based devices [139]. Moreover, CVD graphene is now being incorporated into other devices [147] as well as GaN optical devices [148, 149]. In this work, we show that insertion of single-layer CVD graphene between Cr and AlGaN/GaN layers offers a simple way to create Ohmic contacts to AlGaN/GaN heterostructures without the need for high-temperature annealing or other additional processing steps.

3.1.1 Growth/Synthesis of Materials and Fabrications

In this study, 31 nm Al0.28Ga0.72N/GaN heterostructures were grown epitaxially on Fe-doped, semi-insulating GaN buffer layers on sapphire substrates (Lumilog, Vallauris, France) at ~770 °C using plasma-assisted molecular beam epitaxy (MBE; Veeco Gen 930, Plainview, NY) under Ga-rich conditions[150]. The as-grown material was characterized using x-ray diffraction (XRD; BEDE D1, Durham, UK) ω-2θ scans (Figure 3.1 (a)), and
Figure 3.1(a) Measured XRD $\omega$-2$\theta$ scan and corresponding fit from as-grown AlGaN/GaN structure and AFM image of surface morphology. (b) Raman spectrum from transferred CVD graphene on AlGaN/GaN substrate with D, 2D, and G bands indicated.
the thicknesses and composition of the layers were determined using routine dynamical XRD simulation. Atomic force microscopy (AFM; Veeco DI 3100, Plainview, NY) measurements reveal a smooth surface, with expected step-flow growth. The root mean square (RMS) roughness was estimated to be less than 0.5 nm over a surface area of 5 μm x 5 μm (Figure 3.1 (a)).

Single-layer graphene was grown by CVD on high-purity polycrystalline Cu foils (Alfa Aesar, Ward Hill, MA) of 25 μm thickness using a process described elsewhere [151]. Cleaned Cu foil pieces (1×1 cm²) were placed inside the CVD chamber consisting of a controlled-atmosphere quartz-tube furnace (Lindberg/Blue M, Asheville, NC), CH₄+H₂ CVD was performed at 1000 °C. The polymethyl methacrylate (PMMA) method [146] was used to transfer the CVD graphene from the Cu foil onto the as-grown AlGaN/GaN substrate. The transferred graphene was characterized by Raman spectroscopy (InVia Raman Microscope, Renishaw, Gloucestershire, UK) using a 514 nm wavelength, 1 mW laser. Figure 3.1 (b) shows representative Raman spectrum from the transferred graphene, with the signature D-band, G-band, and 2D-band peaks at 1350 cm⁻¹, 1580 cm⁻¹, and 2700 cm⁻¹, respectively. The approximate 2D:G peak height ratio of 2:1 is indicative of single-layer graphene. The lower intensity D-band peak in the spectrum indicates presence of a small amount of defects in the graphene.

Metal/Graphene/AlGaN/GaN diodes (Figure 3.2), and reference metal/AlGaN/GaN Schottky diodes without the graphene, were fabricated. In both types of diodes, an electron-beam evaporated Cr/Au/Ni metal stack (referred to as Cr) was used
Figure 3.2 Schematic diagram showing the structure of the Cr/Graphene/AlGaN/GaN structure. In the case of the reference device, the graphene layer is removed for contacts. In the case of the Cr/AlGaN/GaN Schottky diodes, the graphene layer was removed by O₂ plasma reactive ion etching (RIE) before metal evaporation. In both types of diodes, Ohmic contact to the 2DEG at the AlGaN/GaN interface was formed at the edge of the samples using pressed indium metal.

3.1.2 Measurements and Analysis

Current density-voltage (I-V) characteristics of Cr/Graphene/AlGaN/GaN and reference Cr/AlGaN/GaN diodes were measured using a semiconductor parameter analyzer (Agilent B1500 A, Santa Clara, CA) (Figure 3.3). The reference Cr/AlGaN/GaN diode shows Schottky behavior, with several orders of magnitude rectification, which is to be expected [150]. In contrast, linear Ohmic-like behavior is observed in the Cr/Graphene/AlGaN/GaN diode, with an extracted resistivity of ~2 mΩ.cm⁻². While the
specific resistance of 2 mΩ·cm² is higher than the state-of-the-art, there are no other published reports showing a metal stack by itself making Ohmic contact to a 2DEG through a thick AlGaN barrier.

To confirm that the measured $I$-$V$ characteristics are not related to room-temperature thermionic emission or trap-assisted hopping transport, $I$-$V$ characteristics of both Cr/AlGaN/GaN and Cr/Graphene/AlGaN/GaN diodes were measured at low temperatures (77 K to 300 K range) in vacuum ($\sim 2 \times 10^{-6}$ Torr) (Figure 3.4 (a), (b)). The Cr/AlGaN/GaN diode is found to be rectifying at all temperatures (Figure 3.4 (a)), with several orders of magnitude change in current density, which is consistent with the thermionic nature of carrier transport. The Cr/Graphene/AlGaN/GaN diode $I$-$V$ characteristics (Figure 3.4 (b)) are Ohmic at all temperatures, with higher current density at lower temperatures due to
Figure 3.4 Current-voltage characteristics as a function of temperature (77 to 300 K, 2×10^{-6} Torr) of: (a) Cr/AlGaN/GaN (inset: Schottky diode turn-on at 250 K) and (b) Cr/Graphene/AlGaN/GaN.
reduced series resistances and higher electron mobilities. In particular, no thermally-activated transport mechanisms were evident from these measurements, eliminating thermionic emission or trap-assisted hopping transport as possible reasons for the observed Ohmic behavior.

Chromium, with work function $\Phi_{Cr}=4.28$ eV was chosen as the metal in contact with graphene because it pins the work function of graphene to the value $\Phi_{Cr/Graphene}=4.28$ eV [152]. Cr in contact with bare AlGaN ($\chi_{AlGaN} = 3.48$ eV from an assumption of a linear variation) results in a Schottky barrier $\Phi_B \sim 0.8$ eV, and based on the effective work function, would be expected to be the same in the case of Cr/Graphene/AlGaN. While $I-V$ characteristics of Graphene/AlGaN have not been reported, they have been reported for graphene/GaN, and show Schottky behavior with a $\Phi_B \sim 0.74$ eV [153]. Thus, it is likely that graphene alone would also provide Schottky contact at the AlGaN surface. Thus, while Cr, or graphene, alone result in Schottky contacts, Cr/Graphene combination provides an Ohmic contact with AlGaN/GaN.

In order to analyze these results, first consider the Cr/AlGaN/GaN junction. In forward bias, the flow of electrons from the 2DEG to the metal takes place with a threshold of $\sim 0.3$ V (Figure 3.3). For metal/AlGaN/GaN junctions in general it is observed that the onset of current from the 2DEG to the metal takes place when there is no opposing field in the AlGaN. We attribute this to percolation transport of carriers from the GaN layer into Al-lean (GaN-like) regions in the random AlGaN alloy layer, which has been observed in GaN/AlGaN/GaN heterostructures previously [154], as well as in InGaN-based LEDs [155]. In metal/AlGaN/GaN contacts in general, this results in conduction between the
Figure 3.5 Schematic energy band diagrams of: (a) Cr/AlGaN/GaN Schottky diode under zero-bias (top) and forward-bias (bottom) conditions, and (b) Cr/Graphene/AlGaN/GaN junction (proposed).
2DEG and gate under flat band conditions for the AlGaN layer, when there is no electrostatic barrier to allow percolation-based transport for carriers in AlGaN. Thus, for Cr/AlGaN with $\Phi_B$~0.8 eV, and a conduction band offset of 0.45 eV, the measured ~0.3 V turn-on voltage for the Cr/AlGaN/GaN Schottky junction is reasonable. The “effective” energy band diagram for this situation is shown in Figure 3.5 (a), where the top and the bottom diagrams depict zero-bias and forward-bias conditions, respectively. The more widely studied Ni/AlGaN/GaN Schottky show the same behavior, as the gate turn-on is usually at a gate bias of $+0.8 \sim 1$ V [156], when the field in the AlGaN reaches flat band. In reverse bias, the metal/semiconductor barrier between metal and GaN prevents electron transport, although the relatively weak temperature dependence (~10-fold increase in current density over a temperature difference of 223 K; Figure 3.4 (a)) can be attributed to the low effective barrier height ($\Phi_B$~0.2 eV) for transport from Cr to the GaN ($\chi_{AlGaN} = 4.1$ eV). In the case of Ni/AlGaN Schottky diodes [156], as expected the reverse bias leakage depends on the barrier height of the Ni/GaN junction (0.81 eV), rather than that of the Ni/AlGaN junction (1.5-1.6 eV). Thus, while the electrostatic barrier height for the heterostructure is set by the AlGaN alloy, there is a lower (percolation) barrier to transport in either direction.

In the case of Cr/Graphene/AlGaN/GaN, the $I$-$V$ characteristics are symmetric, and there is no threshold for conduction (Figure 3.4 (b)). The absence of a threshold voltage for current in forward- and reverse-bias conditions indicates zero-field in the AlGaN, in contrast to the Cr/AlGaN/GaN case. The energy band diagram is, therefore, expected to be symmetric (Figure 3.5 (b)), with the Cr/graphene providing the same energy line-up
relative to the AlGaN as the underlying GaN layer. The effective conduction band for percolation (Figure 3.5 (b)), therefore, presents no barrier to transport in forward or reverse bias. This model is consistent with previous work, where Cr is shown to interact with graphene strongly, relative to other metals such as Au and Fe [157], and open a band gap in Cr/Graphene making it behave like a semiconductor [158]. It is suggested that the Cr/Graphene combination here behaves akin to doped n-GaN. While further work is needed to validate this hypothesis, an important conclusion of this model is that thinner AlGaN layers are likely to lead to significantly lower contact resistance because the probability of percolation through the AlGaN is likely to increase. Optimization of graphene quality, metal-stack parameters, and the epitaxial AlGaN/GaN structure could lead to further reduction in the specific resistances, with important implications for making contact in future group III nitride devices.

3.2 Recess-Free Non-alloyed Ohmic Contacts on Graded AlGaN HFETs

As mentioned earlier in this chapter, MBE-based Ohmic contact regrowth has been used to reduce the total parasitic resistance leading to excellent high-frequency performance in III-Nitride transistors [55, 80, 88, 94, 95, 159, 160]. Recently, it was shown [79, 95] that GaN-HFETs can also approach the theoretical quantum limit [161, 162] of 3D-2D interface resistance between regrown GaN and the 2DEG. In the case of AlGaN/GaN HEMTs, the abrupt AlGaN/GaN heterojunction conduction band offset
prevents vertical contact, and it is necessary to etch away the top AlGaN layer to provide lateral access to the 2DEG. While this approach is successful, the recess and regrowth processes used are inherently more complex than alloyed Ohmic contact formation [163] and require a larger thermal budget.

In this work, we show an approach that could enable non-alloyed Ohmic contacts without regrowth or Ohmic recess. We investigate a device design that uses an upward graded AlGaN heterojunction channel to increase the number of sub-bands, and a reverse graded n+ AlGaN layer to eliminate abrupt conduction band offsets. The design is based on a polarization graded channel transistor [164, 165]. We show that such an approach can enable a very low interface resistance to the 2DEG of 25 mΩ·mm which is close to the calculated quantum limit of $R_{\text{interface}} |_{\text{Quantum limit}} = 20$ mΩ·mm. The total resistance (including metal-semiconductor resistance) was found to be 49 mΩ·mm, which represents the lowest recorded contact resistance for a Ga-polar III-Nitride HEMT structure.

3.2.1 Growth and Fabrication

A graded composition HFET structure was grown on Si-face SiC by plasma-assisted molecular-beam epitaxy in Ga-rich N$_2$-limited growth regime starting with 70 nm of AlN nucleation layer followed by two-step GaN buffer (500nm) to reduce dislocation density and achieve smooth surface [123]. Graded AlGaN was formed by varying the Al flux logarithmically during the growth at a constant Ga flux and growth temperature of 700 °C. The epitaxial structure was confirmed by X-ray diffraction ($\omega-2\theta$ scans) to be a linearly graded AlGaN layer with the composition varying from 0 % (bottom) to 50 % (top) over
Figure 3.6 Energy band diagram, epitaxial structure, charge diagram of channel region (a-c) and Ohmic regions (d-f), respectively. (g) SEM image of the regrown source and drain Ohmic with metal contacts.
15 nm. The energy band diagram of the graded HFET (Figure 3.6 (a)) shows that the polarization gradient induces a 2DEG in the lower 3-4 nm of the graded AlGaN layer (Figure 3.6 (b)-(c)). For the Ohmic regrowth, a SiO₂ mask was deposited using plasma-enhanced chemical-vapor deposition, and the windows for the Ohmic region were defined by fluorine-based reactive-ion-etching (RIE) followed by buffered-oxide-etchant (BOE) wet-etching. Heavily doped contact layers 55 nm reverse graded n⁺ AlGaN (50 → 0 %)/20 nm n⁺ GaN were grown over the regrowth windows at 700 °C. Heavy silicon doping was used to compensate negative polarization in the reverse graded AlGaN layers. Migration-enhanced epitaxy [166] (using N shutter pulsing) was used to provide higher mobility to Al atoms, and to increase Si incorporation for a target doping density of 1.8 × 10²⁰ cm⁻³ in the regrown layers. As a result (Figure 3.6 (d)-(f)), the conduction band is below the Fermi level throughout the Ohmic region, and a continuous 3D electron slab (3DES) is formed from the contact metal to 2DEG under the Ohmic region with no barrier between the channel and the regrown graded AlGaN contact layers. This vertical access to the channel layer is in contrast to previously used approaches for recessed/regrown contacts [95, 159, 160], where a lateral contact was made to the channel.

The polycrystalline (Al)GaN formed on the SiO₂ regrowth mask and the mask were etched using diluted KOH (~ 15% wt.), and BOE, respectively. For the fabrication of test structures with the channel (Figure 3.7 (a)), Ti/Au Ohmic stack was first deposited using e-beam evaporation, and the mesa was isolated using Cl₂-based RIE. Test structures entirely on the regrown region were also defined (Figure 3.7 (b)) to estimate various components of the resistances measured in Figure 3.7 (a).
Figure 3.7 Schematics of (a) TLM A structure on graded AlGaN HFETs, (b) TLM B control structure for the resistance de-embedment
3.2.2 Measurements and Analysis

The total contact resistance, $R_{C,\text{Total}}$, consists of the contact resistance between metal-semiconductors, $R_{\text{Metal}} = R_1$, the vertical resistance from the top of the upper GaN to 2DEG, $R_2$, the sheet resistivity of the regrown region for the estimation of Ohmic extension resistance of $L_2$, $R_{\text{sh,Regrown}} = R_3$, and the 3D-to-2D interface resistance $R_{\text{Interface}} = R_4$. In a self-aligned process, the access region of $L_2$ can be eliminated, and only the components $R_1$, $R_2$, and $R_4$ would exist. Therefore, the achievable contact resistance is the sum of $R_1$, $R_2$, and $R_4$.

In TLM structure A (Figure 3.7 (a)), the channel length $L_1$ was varied from 0.7 μm to 16 μm (Ohmic extension, $L_2 = 0.5$, TLM width, $W=100$ μm). From a linear fit of the measured total resistance, the total contact resistance, $R_{C,\text{Total}}$, was estimated to be $73 \pm 18$ mΩ·mm and the channel resistivity, $R_{\text{sh,Channel}|\text{TLM}}$ was found to be $986 \pm 4$ Ω/□, in agreement with Halls measurement ($R_{\text{sh,Channel}|\text{Hall}} = 985$ Ω/□, $n_S|_{\text{Hall}} = 9.2 \times 10^{12}$ cm$^{-2}$, $\mu_e|_{\text{Hall}} = 690$ cm$^2$/V·s).

To de-embed $R_1$ and $R_3$, another TLM set (TLM structure B) fabricated on the regrown Ohmic slab (Figure 3.7 (b)) in the same die was measured where the separation between the two metal contacts $L_3$ was varied from 2 to 25 μm ($W = 100$ μm). The TLM measurement results gave the contact resistance, $R_1$, the specific contact resistance, $\rho_C$, and the sheet resistivity of 3DES in the Ohmic region, $R_{\text{sh,Regrown}|\text{TLM}}$ as $20 \pm 1$ mΩ·mm, $8.28 \times 10^{-8}$ Ω·cm$^2$, and $48 \pm 0.07$ Ω/□, respectively. The results are consistent with the Hall measurement results ($R_{\text{sh,Regrown}|\text{Hall}} = 48$ Ω/□, $n_S|_{\text{Hall}} = 1.16 \times 10^{15}$ cm$^{-2}$, $\mu_e,\text{Regrown}|_{\text{Hall}} = 113$ cm$^2$/V·s). The results quoted here were fairly uniform across the wafer, and measured
contact resistance and the sheet resistivity across 16 dies on the wafer were found to be 83 ± 10 mΩ·mm ($R_{C,\text{Total}}$) and $1000 \pm 15 \ \Omega/\square$ ($R_{\text{sh,Channel}}$) for TLM A, and $20 \pm 5 \ m\Omega\cdot mm$ ($R_{\text{Metal}}$) and $48 \pm 2 \ \Omega/\square$ ($R_{\text{sh,Regrown}}$) for TLM B, shown in Figure 3.7 (a) and (b), respectively.

After subtracting measured $R_1$, and $R_3 \times L_2$, the value of 29 mΩ·mm was extracted for $R_2 + R_4$. Although the fraction of the resistance from the vertical conducting path, $R_2$, in the Ohmic region is much smaller than other components, it is still necessary to be excluded to obtain more accurate interface resistance, especially when $L_2$ becomes zero. Since there is no structure for a direct measurement of the vertical resistance, we assumed that vertical sheet resistivity is the same as lateral sheet resistivity measured from TLM B. Based on this assumption, the 3D-2D contact resistance, $R_4$ was extracted to be 25 mΩ·mm, and the total intrinsic contact resistance ($R_1 + R_2 + R_4$) was estimated to be 49 mΩ·mm.
The quantum limit for minimum resistance between a highly conductive contact region and a 2DEG can be estimated from the quantum conductance limit of the various sub-bands of the 2DEG [161, 162]. For a channel consisting of $N$ sub-bands with the total electron density of $n_{S,total} = \sum n_{S,i}$ ($n_{S,i}$: the charge density of $i^{th}$ sub-band, $E_i$), the conductance of each band is itself the sum of contributions from various “wires” that make up the 2DEG, and the total conductance of 2DEG can be calculated to be $G = \sum \sigma_i(n_{S,i})$ where $\sigma_i$ is the conductance of $i^{th}$ sub-band. From this equation, it is clear that increasing the channel 2DEG density, and the number of sub-bands improves the contact resistance. To provide low-resistance non-alloyed contact to the 2DEG, it is therefore necessary to eliminate
abrupt conduction band barriers between the contact and the channel and to increase the 2DEG density or number of sub-bands.

To estimate the theoretical interface resistance for the structure in this work, the 2-D charge distribution of the structure shown in Figure 3.9 was calculated using self-consistent Schrodinger-Poisson simulations [108]. Simulation indicates that in the Ohmic region, there is no conduction barrier between the top and bottom of the AlGaN and a 3D electron slab is formed, while in the channel region a 2DEG with two occupied sub-bands is formed at equilibrium. The charge density was calculated as $6.8 \times 10^{12}$ and $2.4 \times 10^{12}$ cm$^{-2}$ for the first two sub-bands. At the edge of Ohmic region, the 3DES makes contact with the 2DEG in the channel. Since the graded structure in the channel region induces a 2DEG with two sub-bands, we can model the interfacial resistance as two parallel resistors associated with these sub-bands as shown in Figure 3.10. From [161, 162] The quantum conductance for a 2DEG with $N$ sub-bands is

$$
\frac{1}{R_{\text{interface}}} = \frac{q^2}{\pi^2 \hbar^2} \sum_{i=1}^{N} \sqrt{2m_{e,i}(E_F - E_i)} \left[ \frac{1}{\Omega \cdot \text{mm}} \right]
$$

Assuming equal effective mass for each sub-band ($m_{e,1} = m_{e,2} = 0.2 \cdot m_0$), the minimum interface resistance was estimated to be 20 m$\Omega \cdot$ mm, compared to the experimental value of 25 m$\Omega \cdot$ mm. The calculated quantum resistance for a 2DEG with one sub-band and the same density would be 27 m$\Omega \cdot$ mm, showing that increasing the number of sub-bands in the channel is a promising way of reducing contact resistance.
Figure 3.10 The resistor network of the Ohmic contact with the parallel interface resistors connected from 3DES to each sub-band of 2DEG in the channel region.

The values of the intrinsic $R_{C,\text{total}}$ of 49 mΩ·mm and $R_{\text{Interface}}$ of 25 mΩ·mm are the lowest values reported for Ga-polar GaN HEMTs. With further increase in electron density or engineering to increase the number of sub-bands, it is possible that even lower interfacial contact resistance could be achieved, with important implications for high-frequency transistors. In addition, since electron velocity of a sub-band decreases \[53\] with increasing electron density, increasing the number of sub-bands could also play an important role in increasing effective velocity.

A very promising aspect of this demonstration is the use of polarization and band gap engineering to remove abrupt conduction band offsets while still obtaining relatively high mobility and charge. This could enable ultra-low resistance Ohmic contacts without the use of either a recess or a regrowth step, along the same lines as was achieved previously for inverted N-polar GaN HEMTs \[167\]. Such a process would involve growth of the entire structure, including the Ohmic graded layers, and removal of the Ohmic layers in the
channel region. This could greatly simplify the design and fabrication process for highly scaled III-nitride devices.

3.3 Summary

In closing, two new approach to form non-alloyed Ohmic contact to 2DEG in AlGaN HFETs have been demonstrated. The first one which utilizes the insertion of single-layer graphene between Cr metal layer and AlGaN/GaN semiconductor heterostructure provides an Ohmic contact with a specific resistance of ~2 mΩ·cm². It is proposed that the Cr/Graphene combination behaves akin to a doped n-type semiconductor leading to a symmetric energy line-up, and that percolation of Al-lean (GaN-like) regions promotes carrier transport through the AlGaN layer, leading to the Ohmic behavior. This method of making Ohmic contacts in GaN-based HEMTs could provide a superior alternative to high-temperature annealed or regrown contacts. The results reported here could have important implications for the fabrication and design of GaN-based electronic and optoelectronic devices of the future. The second method, non-alloyed Ohmic contacts with reverse graded n+ AlGaN fabricated on a polarization-graded AlGaN HFET structure, uses the successive grading from the channel layer to the heavily doped Ohmic layer to prevents the formation of barrier between two graded layers eliminating the need for recess etching for lateral access to the 2DEG. This results in very low total intrinsic contact resistance of 49 mΩ·mm and 3D-2D interface resistance of 25 mΩ·mm. An increment in 2DEG density or the number of sub-bands can lead further improvement in the total contact resistance. The
process described here could enable ultra-low resistance non-alloyed Ohmic contacts to wide gap materials without recess and regrowth.
Chapter 4

Optical Phonon Emission and Its effects on

The Effective Electron Velocity in GaN Channel

Extrinsic performance of a high frequency device consists of the intrinsic device performance as well as the parasitics. Although the parasitic elements and non-ideality factors cannot be eliminated in a practical transistor, intrinsic device performance is often used to benchmark the RF performance of the material, and to evaluate the compatibility of the device for an existing or new application.

The intrinsic $f_T$ can be estimated to first order simply as $g_m/(2\pi \cdot C_{gs})$ for an ideal transistor which does not have any parasitic elements and non-ideality factors in its small-signal circuit. Since the ideal transconductance is given as $v_e \cdot C_{gs}/L_G$, the ideal $f_T$ can be re-written as $f_{T,int} = v_e/(2\pi \cdot L_G)$. Although those parasitic elements and non-ideality factors cannot be eliminated in a practical transistor, it is often used to benchmark the RF performance of the material, and to evaluate the compatibility of the device for a new or existing application. Thus, the material parameter $v_e$ has been of great interest when evaluating the applicability of different materials for high frequency transistors.
In many theoretical calculations based on Monte Carlo simulation [52, 117, 168-170], the peak electron velocity and the saturation electron velocity of GaN channel were found to be \( \sim 2.5 - 3 \times 10^7 \) cm/s and \( 1 - 1.9 \times 10^7 \) cm/s, respectively. However, from the total time delay analysis in recent ultra-scaled GaN HEMT results [76-78, 95], the average electron velocity, \( v_{\text{ave}} \), of the devices was found to be in the range from \( 1.1 \times 10^7 \) to \( 1.5 \times 10^7 \) cm/s. In such devices, the parasitic charging delay \( = C_{gd}(R_s + R_d) \) is found to be only less than \( 5 \sim 10 \% \) of the total time delay. This substantial discrepancy between the experimental measurements and theoretical calculations of electron velocity values is still being investigated by researchers.

Various explanations for this discrepancy has been suggested, such as hot-phonon population [98, 171-173], drain-field associated the effective gate length extension [174], and strong interface scattering due to the large transverse electric-field [175]. However, none of above models could provide an accurate prediction of DC or RF characteristics of GaN-based HEMTs.

In this chapter, we introduce a new carrier transport model based on the strong interaction between optical-phonon and electron carriers in 2DEG of GaN HEMT. This model is then implemented in 2-dimensional TCAD simulations. The close agreement between experiments and simulations suggest that the model presented here captures most of the physics in GaN-based HEMT devices under operation.
4.1 Hot-Phonon Induced Electron Velocity Saturation

In a previous study, Fang et al [53] suggested a model based on optical-phonon emission to explain the saturation of electron velocity in GaN-based HEMTs. Although the assumed electron backscattering in [53] explains general trends rather well, there are several simplifications whose validity is questionable. First of all, it assumes that the LO phonon scattering is infinitely strong, and is thus capable of maintaining the difference between quasi-Fermi levels of backward and forward propagating electrons precisely equal. Second, it assumes that the two quasi-Fermi levels change abruptly at $k_x=0$. Thirdly, it also assumes that the electron temperature is at equilibrium with the lattice. However, the position of Fermi level and electron temperature are interrelated, and the electron temperature can be much higher than the lattice temperature when the device is operation. Therefore, the assumptions made in [53] can be voided when the current is driven in the device. In addition, its calculation of the average electron velocity is based on 2-D sheet charge density. It prevents this model to be utilized in 2-D or 3-D device simulators to predict device performance or to optimize device structure.

Khurgin et al [176] introduced a new velocity saturation model which still owes to LO phonons related electron backscattering for the saturation of electron velocity. However, the new model characterizes the electron distribution in the band with a shifted Fermi-Dirac distribution as shown in Figure 4.1. Furthermore, the 3-D nature of the solution acquisition can greatly reduce the use of resources for testing the fully range performance of the structure using simulations.
Figure 4.1 (a,b) Sketch of electron distribution in Brillouin zone of GaN for two different values of drift velocity. (c,d) LO-phonon assisted scattering for the same two values of drift velocity. (e) LO phonon absorption and (f) stimulated emission for the same two values of drift velocity.
The calculated solutions prove that the saturation velocity is indeed a rather strong function of carrier concentration. The calculated $v_{Sat} - n_S$ curve shown in Figure 4.2 is fitted to an expression written in Eq. (4.1) where $n_{S,0}$ is $1.8 \times 10^{13}$ cm$^{-2}$.

$$v_{Sat}(n_S) = \frac{10^7}{0.38 + \left(\frac{n_S}{n_{S,0}}\right)^{0.45}}$$

(4.1)

The 2-D TCAD simulation used for this study [108] utilizes finite-element-method to obtain self-consistent solutions over the given 2-D structures in which the solutions include energy band structure, carrier distribution, electric field, carrier mobility and velocity. Thus, the carrier density in the structure including the channel is acquired in a 3-D volume density for the given unit area rather than 2-D sheet charge density which can be obtained from a vertical integration along the growth direction of the structure.

The saturation velocity for the 3-D carrier density is obtained separately. The 3-D carrier density dependent saturation velocity curve, $v_{Sat} - n_v$, is depicted in Figure 4.3, and its fitted equation is obtained as

$$v_{Sat}(n_S) = \frac{10^7}{0.38 + \left(\frac{n_v}{n_{v,0}}\right)^{0.5}}$$

(4.2)

where $n_{v,0} = 6 \times 10^{18}$ cm$^{-3}$. 

74
Figure 4.2 The electron saturation velocity vs. sheet charge density in the channel of GaN HEMTs

Figure 4.3 The translated electron saturation velocity vs. volume charge density in the channel of GaN HEMTs for TCAD simulations
The field dependent electron velocity for different carrier density is calculated using the standard high-field mobility equation as

\[
v(n_y, E) = \frac{\mu_0 \cdot E}{1 + \left( \frac{\mu_0 \cdot E}{v_{Sat}} \right)^\beta} \]

(4.3)

where \(\mu_0\) is the low-field mobility, \(E\) is applied field in the region, and \(\beta\) is a constant for different material (e.g. \(\beta_{GaAs} = 1, \beta_{Si} = 2\)). We used \(\mu_0\) of the measured Hall mobility in different HEMT structures examined, and \(\beta\) of 2 for GaN for the simulation conducted in this study.
4.2 Other Physical Models

4.2.1 Charge Modulation: Polarization and Surface Charge

As described in Chapter 2, III-Nitride HEMTs utilize the polarization charges to induce 2DEG in the channel, which arises due to the sum of the net polarization at each interface with the donor- or acceptor-like surface states.

The polarization in wurtzite III-Nitride materials is consisting of two components, the spontaneous polarization, $P_{SP}$, and the strain-induced piezoelectric polarization, $P_{PZ}$. Thus the total polarization in a certain layer is given by

$$ P_{Total} = P_{SP} + P_{PZ} $$(4.4)

where $P_{SP}$ is a fixed material parameter. The calculated $P_{SP}$ for AlN, GaN and InN can be found in [112], and the $P_{SP}$ of ternary or quaternary material of Al$_x$In$_y$Ga$_{(1-x-y)}$N can be found by linear interpolation between AlN, InN and GaN.

The $P_{PZ}$ of a pseudomorphically grown layer on the substrate is given by

$$ P_{PZ} = 2 \cdot \frac{a_L - a_S}{a_S} \left( e_{31} - e_{33} \cdot \frac{c_{31}}{c_{33}} \right) $$$(4.5)

Where $a_L$ and $a_S$ are the lattice constants of the strained layer and the substrate, respectively, and $e_{31}/e_{33}$ and $c_{31}/c_{33}$ are piezoelectric constants and elastic constants of the strained layer which also can be found by a linear interpolation for the ternary or quaternary material [112].

The surface states on those of unpassivated structures have generally been found to be influenced by growth conditions and the equipment itself. There is also a wide scatter in
the reported values of surface pinning unlike passivated structures. Moreover, this difference in surface states also affect the Schottky barrier height of the gate metal. Hence for a given experimental data, we adjust the surface pinning and the Schottky barrier height to obtain the reported 2DEG density and the pinch-off voltage, $V_{th}$, in the given structure. It should be noted that these adjustments do not undermine the physical solution obtained from simulation in the section 4.3.1.

4.2.2 Semi-insulating GaN Buffer

Although there are several different structures to improve the charge confinement in the channel using a back-barrier as described in chapter 2, in most of GaN HEMT structures for the practical RF applications, the structure simply consists with the barrier layer, few hundred nanometers of GaN channel layer and semi-insulating (S.I.) GaN buffer layer on the substrate. Due to the unintentionally n-type doping during GaN buffer growth, C or Fe doping is typically used for achieve S.I. GaN buffer to prevent buffer leakage. However, it is also strongly related to the growth conditions in different systems, and it has been found that the C or Fe doping used for semi-insulation stimulate more incorporation of the unintentional n-doping in the S.I. GaN layer. Since the structures examined in this study are using such S.I. GaN layer, it is necessary to set the S.I. model for the study.
Various energy levels of the trap states, $E_t$, in GaN are created by the material defects such as threading-dislocation, stacking-fault, Ga or N vacancies, antisites as well as impurity incorporation of carbon, oxygen and hydrogen during the growth [177-180]. For S.I. GaN grown using Fe- and C-doping by metal-organic chemical-vapor-deposition (MOCVD) or without doping (MBE), the major deep level traps were found at $E_C - E_t$ of 1.1 eV (Fe-doping), and 3.28 eV for C-doped (C-doping). For the S.I. GaN grown by molecular beam epitaxy (MBE), $E_C - E_t$ of 3.28 eV (background C-related) was found in both MOCVD and MBE grown S.I. GaN, minor traps located with the major traps at the levels depicted in Figure 4.4 were also observed, and these minor trap states can also compensate unintentional n-doping in S.I. GaN layer.
For the rest of the study, since the trap density for each $E_C - E_t$ is hard to estimate for different GaN buffer grown with different equipment, we have used a deep level traps located at $E_C - 3.28$ eV which are the carbon-related trap level ($E_C - 3.28$ eV [181-183]) commonly found in both MOCVD and MBE grown S.I. GaN buffer.

To find a reasonable trap density which prevent the significant buffer leakage of UID GaN while avoiding the degradation in electron transport due to traps, a pinched-FET structure in Figure 4.5 is simulated. The structure consists of 28 nm of Al$_{0.3}$Ga$_{0.7}$N and 1.5 nm of AlN for the barrier layer, UID GaN channel layer with thickness ranging between 0 to 300 nm, and 1 µm of S.I GaN buffer layer with UID doping, $N_{UID}$, and trap densities $N_t$.

In order to investigate the buffer breakdown, the channel region is trench-etched with 100 nm of the etch depth ($t_{etch}$), and the length of trenched well, $L_{Etch}$, is set to be 1 µm centered at 2 µm of $L_{SD}$. The doping density of $n^{++}$ GaN is set to be $1 \times 10^{21}$ cm$^{-3}$ and an ideal contact is set to avoid the effect of the contacts to the current level.
Figure 4.6 (a) Energy band diagram of an AlGaN/GaN HEMT for S.I. GaN buffer test structure (b) the buffer leakage I-V with various trap densities

The first simulations of the S.I. GaN buffer test structure is carried out by using \( N_{UID} \) of 0 and \( 1 \times 10^{15} \) cm\(^{-3} \), and various \( N_t \) with the range from \( 1 \times 10^{15} \) to \( 1 \times 10^{17} \) cm\(^{-3} \). In Figure 4.6 (a) and (b), it can be seen that the conduction band of S.I. GaN is pulled up more steeply by more acceptor-like trap states, and the buffer become more insulating as \( N_t \) increases. And, it is also clear from the figures that the GaN buffer with no \( N_{UID} \) and \( N_t \) has exactly the same result with the one with \( N_{UID} = N_t \). This means the trap density compensate the unintentional n-doping in S.I. layer, and the rest of trap states from \( N_t - N_{UID} \) makes the GaN buffer semi-insulating from hot-electron injection into the buffer.

Since the remaining \( N_t \) after compensation \( N_{UID} \) will degrade the current conduction when the trapping effect is activated in the simulation, we added UID GaN spacer as a channel layer between S.I GaN buffer and the barrier layers for the simulations. The thickness of UID GaN channel with UID doping density of \( 1 \times 10^{16} \) cm\(^{-3} \) varies from 0 nm
Figure 4.7 (a) Energy band diagram of an AlGaN/GaN HEMT for testing S.I. GaN buffer (b) the buffer leakage I-V with various UID GaN channel thickness to 300 nm while N_t and N_{UID} in S.I. GaN buffer is fixed to be $1 \times 10^{15}$ cm$^{-3}$ and $5 \times 10^{16}$ cm$^{-3}$, respectively.

The ionized UID donors in the GaN spacer push the conduction band down in channel layer as the thickness of spacer increases. Although the N_{UID} in the additional GaN spacer can lead more buffer leakage current compared to a buffer with no GaN spacer, a typical UID density $1 \times 10^{16}$ cm$^{-3}$ does not greatly deteriorate the S.I. behavior. For the simulation in following section 4.3, we used the UID doping in the channel layer of $1 - 2 \times 10^{16}$ cm$^{-3}$, and N_t – N_{UID} in the S.I. layer with the range between $1 \times 10^{15}$ cm$^{-3}$ and $1 \times 10^{17}$ cm$^{-3}$. 

82
4.3 Validation of New Model and Discussion

4.3.1 Simulations and Results

To validate the newly introduced carrier transport model for 2-D simulation in this study, we have chosen three GaN HEMT structures recently published which are unpassivated AlGaN/GaN HEMT [184], InAlN/GaN HEMT with dielectric-free-passivation [79], and InAlN/GaN HEMT with AlN cap and SiN passivation [185]. We chose all three HEMT structures grown on SiC substrate which minimizes the thermal effect, thereby we could run the simulation with the lattice temperature at the room temperature (300 °K).

Figure 4.8 Schematic of the transistor structure for simulations with structural parameters
Ni Schottky contacts were used as the gate metal in all these three transistors, and the gate-to-source and the gate-to-drain spacing are equal. Figure 4.8 shows the representative schematic of the transistor structure with the different structural dimensions marked in the figure.

The lengths of the contact region, regrown region, and the metal contact are set to be the same as \( L_C = L_{\text{Regrown}} = L_{\text{Metal}} = 0.2 \ \mu m \), and the length of the Ohmic access region, \( L_{\text{Acc}} \), is set to be zero for all three device structures. Since the simulator assumes all conductor with zero resistance, Lumped resistances are added in series to source/drain Ohmic contact and the gate contact, and a high doping density of \( 1 \times 10^{21} \ \text{cm}^{-3} \) is set for the contact layer and the regrown layer for \( R_C \) and \( R_g \).

The first transistor device used for the model validation is a standard AlGaN/AlN/GaN HEMT structure on SiC substrate which consist 21 nm of AlGaN barrier layer, 1nm of AlN interlayer and GaN buffer [184, 186]. To satisfy the 2DEG density measured from Hall measurement, the surface pinning on the access region is set to be \( E_C - 2.6 \ \text{eV} \) which results in the 2DEG density of \( 7.5 \times 10^{12} \ \text{cm}^{-2} \). To match the threshold voltage, \( V_{\text{th}} \), the Schottky barrier height, \( \Phi_B \), between the Ni gate and AlGaN barrier and is set to be 2.8 eV. The UID GaN channel layer was set to be 200 nm with \( 1 \times 10^{16} \ \text{cm}^{-3} \) of \( N_{\text{UID}} \), and \( N_i \) of 1 \( \mu \text{m} \) S.I. GaN is set to be \( 3.5 \times 10^{15} \ \text{cm}^{-3} \). The gate and the alloyed Ohmic contacts were defined with 5 nm and 10 nm of the recess depth, respectively. The source-to-drain distance, \( L_{SD} \), the gate length, \( L_G \), and the head length, \( L_{\text{Head}} \), were 1.1 \( \mu \text{m} \), 60 nm, and 550 nm, respectively, and the heights of gate stem, \( t_{\text{Stem}} \), and the gate head, \( t_{\text{Head}} \), were set to be 200
Figure 4.9 The simulated results of (a) $I_D-V_D$ characteristics, (b) the transfer curves, (c) Frequency-gain characteristics compared with the measured results from [184]
nm and 360 nm respectively. The gate resistance, $R_g$, and contact resistance, $R_c$, are added in series to each contact, and to be 0.15 $\Omega \cdot$mm and 0.23 $\Omega \cdot$mm, respectively, as described in [184, 186].

For the high-field electron transport calculation in the simulation, the reported low-field electron mobility of 2200 cm$^2$/V$\cdot$s was used along with the new velocity saturation model developed in this study. And, the DC $I_D-V_D$, transfer characteristics, and the small-signal gain versus frequency plots are depicted with the reported data in Figure 4.9 (a), (b), and (c), respectively.

From the comparison with the measured data, both measured and simulation results consent in their $V_{th}$ of -2.8 V. The maximum transconductance, $g_{m,peak}$, was found to be 416 mS/mm at $V_g = -1.9$ V for $V_{DS} = 5$ V from simulation which is closely matching to the measured values of $g_{m,peak} = 410$ mS/mm at $V_g = -1.9$ V. The maximum drain current at $V_{GS} = 0$ V, $I_{D,max}|V_{gs}=0V$, the simulated result shows a bit higher value ($I_{D,max} = 995$ mA/mm) compared to the measured value ($I_{D,max} = 950$ mA/mm). The $f_T$ and $f_{max}$ of the simulated results were found to be 90 GHz and 250 GHz, and the overall small-signal gain from the simulation showed ~ 3dB higher values compared to the reported value.

The second device simulated is the lattice matched InAlN/AlN/GaN HEMT on SiC consisting of 7.5-nm InAlN barrier, 1.5-nm AlN interlayer, 200-nm UID GaN channel ($N_{UID} = 1 \times 10^{16}$ cm$^{-3}$), and a 1.6-μm Fe-doped S.I. GaN buffer ($N_t = 1 \times 10^{17}$ cm$^{-3}$) from top to bottom [79]. The $t_{Regrown}$ of 40 nm as the regrown $n^+$ GaN layer was inserted between the Ohmic contact and the $n^+$ GaN contact layer, and the doping density in both $n^+$ GaN layers was set to be $1 \times 10^{21}$ cm$^{-3}$. A rectangular Ni Schottky gate with a cross-sectional
The charge density for matching $I_{D,max}|V_{gs}=0V$ is lower than the reported $n_S$ of $1.92 \times 10^{13}$ cm$^{-2}$ measured from Hall, and can be explained with plasma charging damage [187] or “Antenna” effect [188, 189]. The plasma-induced oxygen ions or electrons during the blanket dielectric-free-passivation process tend to be deflected toward the highly conductive material which is the regrown GaN walls of the source and drain Ohmic contact for this case. This will induce more surface states near the regrown n$^+$ GaN or the entire active region, and possibly degrade the electron mobility which could be responsible for the unclear origin of the additional resistance in this device [79].

The saturation velocity model with the reported low-field electron mobility of 1240 cm$^2$/V·s resulted in closely matched DC $I_D-V_D$, transfer characteristics, and the small-signal gain versus frequency plots shown with the reported data in Figure 4.10 (a), (b), (c), respectively. The $V_{th}$ and $I_{D,max}|V_{gs}=0V$ are -3.85 V and 1.53 A/mm for the simulated results, and -3.85 V and 1.57 A/mm for the reported values, respectively. The maximum transconductance, $g_{m,peak}$, was found to be 583 mS/mm at $V_g = -3.1$ V for $V_{DS} = 3$ V from simulation which is lower than the measured values of $g_{m,peak} = 650$ mS/mm at $V_g = -2.9$ V. The simulated $f_T$ and $f_{max}$ of were found to be 370 GHz and 24 GHz while the reported $f_T$ and $f_{max}$ were 370 GHz and 30 GHz at the given bias of $V_{gs} = -2.9$ V and $V_{ds} = 2.75$ V. The difference between the simulated and the reported small-signal gain was
Figure 4.10 The simulated results of (a) $I_D$-$V_D$ characteristics, (b) the transfer curves, (c) frequency-gain characteristics compared with the measured results from [79]
only 1 – 2 dB in overall frequency range.

The last HEMT device compared for the validation is an AlN (1.5 nm)/In$_{0.13}$Al$_{0.87}$N (3.5 nm)/AlN (1 nm)/GaN (2 µm) structure [185]. Since it was passivated with 70 nm of SiNx layer unlike former two transistor structures, the surface pinning was not set, but the pre-determined $\Delta E_C$ between SiNx and AlN induced the $n_S$ of $2.1 \times 10^{13}$ cm$^{-2}$ in the channel (the pre-process Hall measured $n_S$ : $2.1 \times 10^{13}$ cm$^{-2}$). To have similar buffer characteristics and $V_{th}$, $N_{UID}$ of $2 \times 10^{16}$ cm$^{-3}$ in 200 nm GaN channel layer and $N_t$ of $3 \times 10^{15}$ cm$^{-3}$ in 1.8 µm S.I. GaN buffer layer were set, and $\Phi_B$ was set to be of 4.5 eV. The centered gate with $L_G = L_{Head} = 200$ nm was defined within $L_{SD}$ of 0.5 µm. The $R_c$ of 0.3 Ω·mm and $R_g$ of 0.66 Ω·mm were included, and the low-field electron mobility of 1320 cm$^2$/V·s was used for field-dependent mobility calculation.

The simulated results of $I_D-V_D$, $I_D-V_G$, and the small-signal gain characteristics are compared with the measured data in Figure 4.11 (a), (b), and (c), respectively. The DC $I_D-V_D$ and $I_D-V_G$ are matching well to the experimentally measured value, and the slightly lower off-state current in simulation is due to the simplified trap states for the S.I. buffer which is uniformly distributed at the same energy level in simulation. The $f_T$ and $f_{max}$ for the simulated/measured were 100/80 GHz and 143/135 GHz, respectively, and the difference in the small-signal gain was found to be only 1 – 2 dB in overall frequency range.

The adjustment of $\Phi_B$, $N_{UID}$ in GaN channel, and $N_t$ in S.I. GaN buffer are the only empirical parameters used in this simulation study. However, the $N_{UID}$ and $N_t$ values are chosen from the reported values and are not arbitrary. The Schottky barrier height $\Phi_B$ for
Figure 4.11 The simulated results of (a) $I_D$-$V_D$ characteristics, (b) the transfer curves, (c) Freq-gain characteristics compared with the measured results from [185]
all three structures were commonly found to be $1.5 \pm 0.1$ eV higher than the ideal Schottky barrier height between Ni and the barrier material of AlGaN, InAlN and AlN. This common increment in $\Phi_B$ can be related to the distributed surface donor states [58] which are induced during O$_2$ plasma treatment before the gate metallization. In addition, these empirical values of $N_t$, $E_{\text{pinning}}$, $\Phi_B$ can be obtained from the pinched-FET measurements, 1-D Schrodinger-Poisson simulation with the measured epitaxial structure and $n_s$, and capacitance-voltage analysis on a representative wafer, respectively.

4.4 Summary

In this work, we introduced a new model for the electron saturation velocity in GaN channel HEMTs. Due to strong electron-phonon interaction and long LO phonon lifetime in GaN, the electron velocity is clamped by the stimulated LO phonon emission. Moreover, it was found the clamping of the saturation velocity is strongly dependent to electron carrier density in GaN channel.

Based on the new model, 2-D TCAD simulations were performed for three high performing GaN-based HEMT and compared with the experimentally measured results as the model validation. The new saturation velocity model led to an excellent agreement in the results between simulation and experimentally measurement of the devices. This clearly shows that the key ingredient in predicting the HEMT performance is the accurate saturation velocity.

Thus, the work presented here could be used for minimizing the use of resources for the optimization of the transistor structure from the experimental studies, and can also be
used to provide the close-fit benchmark for the upcoming high-frequency mm-Wave applications.
Chapter 5

Polarization-Graded Channel HFETs

with High Linearity of $g_m$ and $f_T$

The magnitude and linearity of gain in a transistor are highly dependent on the transconductance profile of a transistor. A non-linear gain in the transistor operation can severely influence on the output large signal linearity for RF power amplification [190]. Thus, it limits the full-range utilization of the output current gain of the transistor and reduces efficiency.

A rapid dropping behavior in $g_m$ profile has been observed from the most of FET structures which utilize a triangular quantum well as its conducting channel such as Si-MOSFET, (In)GaAs HEMTs where $g_m$ sharply raises to its peak value after the device turns on and rapidly decrease as the drain current (or the gate bias) increases. GaN-based HEMT structures also have been found to have such behavior.

For FETs with other material system rather than Nitride-based HEMT, there have been proposed various explanations such as the effect of interface roughness in Si/SiO$_2$ [191], an inefficient charge modulation due to the transferred hot electron between the delta-doped layer in the barrier and the channel [192, 193].
However, none of above applies to GaN HEMTs since Nitride-based HEMT exploit the induced polarization effects for the charge population in 2DEG, and the AlN interlayer normally used in-between the barrier and GaN channel pushes the wave-function away from the AlN/GaN interface which already has high quality with the electron mobility higher than 2200 cm$^2$/V·s. For other possible causes of the dropping $g_m$ in Nitride-based HEMT were suggested such as self-heating, and non-linear source (or drain) resistance. However, the use of different substrates having different thermal conductivities does not scale down the phenomena, and the same behavior was found to exist in an ultra-highly scaled device structure [95] where $R_{S/D}$ was found only $\sim 0.2$ Ω·mm.

In the previous chapter, we derived the effective saturation electron velocity based on strong interaction between LO phonons and electrons with respect to the 2DEG density, and attributed the lower peak or saturation electron velocity to optical-phonon emission in GaN HEMT. Furthermore, it was found that the saturation velocity decreases as the 2DEG density increases while other scattering mechanisms dominate for lower 2DEG density ($n_s < 2 \times 10^{12}$).

In triangular quantum well, the centroid of the charge distribution of the 2DEG has a nominal variation with respect to the 2DEG density. For an example, the peak volume charge density is found to be $4 \times 10^{18}$ and $1 \times 10^{20}$ cm$^{-3}$ for the 2DEG density of $2 \times 10^{12}$ and $2 \times 10^{13}$ cm$^{-2}$ in an AlN/GaN HEMT structure which is responsible for the decreasing $g_m$ profile after it reaches its peak value. In other word, the rapidly dropping behavior of $g_m$ can be mitigated if we can engineer the charge distribution so as to spread it over a
certain distance which had already been demonstrated in GaAs MESFET with a gradient doping [194-196], and in polarization-graded AlGaN HFET [165].

In this chapter, first, we introduce an AlGaN/GaN HEMT structure with an inserted graded AlGaN channel, and show the vertical scalability of such structure while maintaining a constant $g_m$ profile. Secondly, we show RF performance of a highly scaled polarization-graded AlGaN HFET in which the linearity of $g_m$ and $f_T$ have been greatly improved with the modified charge distribution as well as an Ohmic regrowth technology which minimizes the parasitic resistance.

5.1 Flat Transconductance in AlGaN/GaN HEMTs using Polarization-Induced Channel Engineering

Conventional HEMT structures have been scaled down successfully to gate-channel distance of few nanometers [2], but, their $g_m-V_{gs}$ profile is found to be non-linear, with a steep decrease in the $g_m$ profile as the output current is increased. It was shown in [1], [3] that a three-dimensional electron slab can substitute a two-dimensional sheet charge formed to screen the net positive charge at the heterojunction in AlGaN/GaN HEMTs, leading to a MESFET-like structure without impurity doping. Polarization-graded (PolFET) devices can be used to engineer the $g_m-V_{gs}$ curve in a similar way to metal-semiconductor FETs (MESFETs) [4-6], but with improved gate leakage, breakdown and mobility characteristics compared to MESFETs [1]. However, vertical scaling down of these structures is limited.
In this work, we describe a hybrid approach for HEMTs where the charge profile consists of a 2-dimensional as well as a 3-dimensional electron gas by inserting a polarization-graded layer into a HEMT structure, and show that such an approach leads to a highly constant or flat transconductance profile over the input voltage range. The 2-D electron gas formed by the abrupt spontaneous and piezoelectric polarization sheet charges at the hetero-interface is similar to that in a conventional HEMT, while the 3-D component arises from polarization grading of the channel layer from GaN to low composition AlGaN layer (Figure 5.1), such that the polarization-induced charge is smeared over the graded region. The integrated 3DEG sheet carrier density in this hybrid HEMT structure is still given by the total spontaneous and piezoelectric polarization sheet charge densities across the Al\textsubscript{x}Ga\textsubscript{1-x}N/GaN hetero-interface. This graded channel HEMT combines the advantages of HEMTs and MESFETs by offering high $g_m$ and tailored $g_m-V_{gs}$ profile simultaneously.
In addition to achieving high linearity and high gain, gate leakage and channel breakdown are also improved by high Al-composition AlGaN barrier layer and a graded AlGaN channel layer. Finally, the effective velocity in AlGaN/GaN 2DEGs has been found to be lower than the reported bulk or 3D values. Tuning of dimensionality could therefore provide another approach to improving velocity characteristics in AlGaN HEMT channels, and ultimately achieving higher frequency performance.

5.1.1 Structure Design, Growth and Fabrications

For comparison, we designed two samples, a conventional HEMT and a graded channel HEMT in this study (Figure 5.2). The samples were grown on Si-face 4H-SiC substrate by plasma-assisted molecular-beam-epitaxy (PAMBE). To reduce buffer leakage, dislocation density and impurity incorporation, a 45 nm of AlN nucleation layer was first grown in N-rich regime (Al/N ~ 0.6), followed by two-step GaN buffer of 550nm8,9. For both structures, the AlGaN cap layer consists of three layers, 15 nm of Si-doped (N_D = 5×10^{18} cm^{-3}) Al_{0.25}Ga_{0.75}N, 5 nm of UID Al_{0.25}Ga_{0.75}N and 3 nm of Al_{0.9}Ga_{0.1}N from top to bottom. The high composition Al_{0.9}Ga_{0.1}N layer mainly supplies mobile charges into the channel and 15 nm of Si-doped Al_{0.25}Ga_{0.75}N layer helps to introduce additional charges in the access region. The entire Al_{0.25}Ga_{0.75}N layer was grown to form a low Ohmic contact resistance with a typically alloyed Ti/Al/Ni/Au metal stack. For the graded channel HEMT structure, an additional 5nm of a linearly graded layer from GaN (bottom) to Al_{0.15}Ga_{0.85}N (top) was inserted into the abrupt junction between Al_{0.9}Ga_{0.1}N and GaN buffer layer of the conventional HEMT structure. Al-composition of each layer was confirmed by HRXRD
Figure 5.2 Epitaxial structure of the (a) graded channel HEMT and (b) conventional HEMT measurements.

We calculated the energy band diagram using a self-consistent one-dimensional Schrödinger-Poisson solver (BandEng). The calculated band diagram of the graded channel HEMT structure at zero-bias and the carrier concentration profile in the channel are depicted and compared with the one for the conventional HEMT structure in Figure 5.3 (a)-(b). The gate region is recessed by 12 nm, and 3.0 eV of Schottky barrier height was determined by comparison of capacitance-voltage (C-V) measurements (Figure 5.3 (d)) and theoretical C-V curves from Schrödinger-Poisson simulations. As reported earlier, a higher Schottky barrier height was estimated in the gate recessed region due to a change in the surface donor density after the gate recess etch. The increasing C-V profile of the graded channel HEMT indicates 5–6 nm of channel thickness which matches well with the full-width half maximum (FWHM) of the calculated charge profile. In comparison to a deep quantum well in the conventional HEMT structure, the graded AlGaN layer forms a
Figure 5.3 (a) Energy band diagram of the graded channel HEMT (b) Simulated electron density profiles and the conduction band profiles in quantum well (c) Two sub-bands occupied and the profile of the wave-functions (d) Measured C-V profiles of graded channel HEMT
shallower but wider quantum-well in which two sub-bands are occupied (E₀ = -0.0559 eV, E₁ = -0.0086 eV).

Two wave-functions in the sub-bands spread out the sheet charge density of 1.1×10¹³ cm⁻² (after gate recess) over the wide quantum-well of the graded channel HEMT with a volume charge density of (1 – 1.5)×10¹⁹ cm⁻³ (Figure 5.3 (c)). The width of this quasi-3D charge profile is 3~4 times wider than FWHM of Gaussian-like charge profile of the conventional HEMT (which is theoretically assumed 1.5~2 nm wide).

The fabrication of transistors started with the formation of Ohmic contacts. Ti/Al/Ni/Au alloyed source and drain contacts were evaporated and annealed at 850 °C. Then, mesa isolation and gate recess were done using chlorine-based inductively-coupled-plasma reactive-ion etching. A Ni/Au/Ni metal stack was evaporated to form the gate Schottky contact for gate after the gate recess step. The device dimensions of both HEMTs are W = 150 µm (2×75 µm), L_g = 1.5 µm, L_gS = 1 µm, and L_gd = 1.5 µm.

Hall and TLM measurements results agreed well with each other and the measured charge density, mobility, sheet resistance and contact resistance were 1.4×10¹³ cm⁻² (before gate recess), 524 cm²/Vs, 872 Ω/□, and 0.74 Ω·mm, respectively for the graded channel HEMT, and 1.5×10¹³ cm⁻² (before gate recess), 635 cm²/Vs, 536 Ω/□, and 0.64 Ω·mm, respectively for the conventional HEMT. Compared to a typical mobility in a conventional AlGaN/GaN HEMT (> 1000 cm²/Vs), the conventional HEMT has relatively low mobility due to the use of Al₀.₉Ga₀.₁N cap. However, the low mobility is not expected to affect the shape of the g_m profile in the saturated region. We expect that the mobility in both structures could be improved through the substitution of Al₀.₉Ga₀.₁N layer with AlN for the cap layer.
5.1.2 Characterizations and Discussion

DC I-V plots for the graded channel HEMT and the convention HEMT are shown in Figure 5.4 (a)-(b). In the graded channel HEMT, the pinch-off voltage \( V_{p, \text{Graded channel}} = -3.2 \) V is slightly more negative than the conventional HEMT case \( V_{p, \text{Conventional}} = -2.6 \) V because the graded channel HEMT has a thicker and deeper channel than the conventional HEMT. Although the charge densities for both HEMTs were approximately the same from C-V measurement in Figure 5.3(c), the maximum drain current \( I_{d, \text{max}} \) for the graded channel HEMT (~970 mA/mm) was observed higher than the one for the conventional HEMT (~720 mA/mm).

The measured \( g_m \) variation with the gate bias, \( V_{gs} \), at 10 V of drain voltage, \( V_{ds} \), is shown in Figure 5.5 (a). The graded channel HEMT shows a flat \( g_m \) profile for wide input range (an average \( g_m \approx 159 \) mS/mm over \( V_{gs} = -2.2 \sim 3.5 \) V with a total gate voltage range = - 3.2 \sim 3.5 \) V which is about 85\% of total input bias range). The peak transconductance, \( g_{m, \text{peak}} \), was measured to be 168 mS/mm which is comparable to the \( g_{m, \text{peak}} \) of the convention HEMT, 159 mS/mm, and higher than the one reported for MESFET(-like) devices\(^1\).

The source resistance \( (R_S = R_{S, \text{contact}} + R_{S, \text{Access}}) \) was measured to be fairly high, 3 Ω-mm for the graded channel HEMT and 4.8 Ω-mm for the conventional HEMT, due to the long gate-to-source distance with low mobility and gate-recess. Since a high source-resistance underestimates \( g_m \) and extends the input voltage range, the intrinsic transconductance \( (g_{mi} = g_m / (1-R_s \cdot g_m)) \) and the gate-to-channel bias \( (V_{gc} = V_{gs} - R_S \cdot I_{DS}) \) were extracted as depicted in Figure 5.5 (b). The peak intrinsic transconductance, \( g_{mi, \text{peak}} \), for the graded channel
Figure 5.4 DC I-V characteristics of (a) the graded channel HEMT and (b) the conventional HEMT after gate recess.

Figure 5.5 (a) gm vs. V\textsubscript{gs} and (b) g\textsubscript{mi} vs. V\textsubscript{gc} for the graded channel HEMT and the conventional HEMT at V\textsubscript{ds} = 10V.
HEMT and the conventional HEMT were found to be 318 mS/mm and 674 mS/mm, respectively.

The $g_{mi}-V_{gc}$ of the graded channel HEMT maintains a consistent value of 300 mS/mm with a high averaged value (95% of $g_{mi,peak}$) over $V_{gc} = -1.7 \sim 0.5V$ (55% of total gate bias range) unlike the $g_{m}-V_{gs}$ profile of the conventional which is drops rapidly after reaching $g_{m,peak}$. This clearly shows that 5 ~ 6 nm of the distributed charge profile in the graded channel HEMT is effective to tailor a flat $g_m$ profile while maintaining a high $g_m$ value.

The flat transconductance profile will improve the overall linearity and gain curves of large signal microwave amplifiers based on these graded channel devices. In addition to the obvious impact this graded channel design has on linearity, there may be other significant advantages from the nano-scale control of electron density in the channel. It has been reported that the electron velocity in low electron density GaN layers is significantly higher than in high electron density channels. The structure described will enable channel density in the channel to be varied with great precision while maintaining channel thickness dimensions that are suitable for high frequency scaled devices.

5.2 Highly Scaled Polarization-Graded AlGaN FETs

Although the AlGaN/GaN HEMT with an inserted polarization-graded channel in previous section showed possible vertical scalability with a flat $g_m$ profile, it was found that the high parasitic resistances from the contact resistance and low mobility were limiting the high frequency performance. Especially, with a single Al-cell configuration in our MBE system for the growth, it was found that there is a significant mobility degradation
due to growth interruption at the high composition AlGaN/graded AlGaN interface used to increase Al-cell temperature. To overcome this issue, we designed vertically highly scaled polarization-graded AlGaN FET structure explained below.

5.2.1 1st generation: GaN/graded AlGaN(0→45%)/GaN

The first generation polarization-graded AlGaN HFET structure was grown on 4H SiC substrate using PA-MBE. The buffer layer consists of a 45 nm of AlN nucleation layer grown in N-rich regime (Al/N ~ 0.6), followed by a 550 nm thick two-step GaN buffer. On top of the GaN buffer layer, an AlGaN layer with AlN mole fraction graded from 0% (bottom) to 45% (top) over 10 nm was grown and capped with 5 nm of UID GaN cap layer to reduce the gate leakage current. The epitaxial structure and its band structure is shown in Figure 5.6. In the structure, the electrons are confined in bottom 3 nm of graded layer where the composition is varying from 0% to 15% as in the AlGaN/GaN HEMT with an inserted graded channel.

Using the standard Ohmic stack of Ti/Al/Ni/Au (20/120/30/50 nm) for Ga-polar AlGaN/GaN HEMT, an annealing temperature optimization of the alloyed Ohmic contact was conducted and it was found the best Ohmic contact was obtained to be 20 sec annealing at 840°C in N2-ambient. (Figure 5.7)

After the alloyed Ohmic formation, the devices were isolated using Cl2-based ICP-RIE dry etching. Then, from the TLM and Hall measurements, the measured charge density,
Figure 5.6 (a) Schematic of the epitaxial structure and (b) energy band diagram of the Gen.1 vertically scaled graded AlGaN HFET.

Figure 5.7 (a), (b) Annealing temperature optimization for the alloyed Ohmic contacts

mobility, sheet resistivity and contact resistance were found to be $5.5 \times 10^{12}$ cm$^2$, 930 cm$^2$/V·s, 1.3 KΩ/□, and 0.9 Ω·mm, respectively.

For the transistors, optical gates with the gate length $L_G$ of 0.7 µm were defined using a projection lithography with GCA 6100 stepper, and Ni/Au/Ni (20/200/30 nm) of Schottky contact was formed by e-beam evaporation. One of the representative DC current-voltage and the transfer characteristics is shown in Figure 5.8 (a)-(b).
Figure 5.8 (a), (b) Annealing temperature optimization for the alloyed Ohmic contacts

The maximum saturated drain current was found to be only 0.4 A/mm at $V_{gs} = 2$ V and a very high on resistance, $R_{on}$, of $10 \, \Omega \cdot \text{mm}$ was measured. The low saturated drain current is due to the low 2DEG density due to depletion from the 5 nm of GaN cap layer that has been used to prevent the gate leakage current. Moreover, a flat transconductance profile expected from the graded AlGaN channel AlGaN/GaN HEMT was not found in this structure. This is possibly due to the narrow channel depth of 3 nm which is similar to the charge profile in a conventional AlGaN/GaN HEMT which is not enough to tailor the charge profile in the channel.

5.2.2 2nd generation: Graded AlGaN (0→50%)/GaN

As a simple solution to the issues of the low 2DEG density and narrow channel depth in the 1st generation device discussed in section 5.2.1, the 5 nm GaN cap layer was removed. Thickness of the graded AlGaN layer was changed to 15 nm with a linear grading
Figure 5.9 (a) Schematic of a highly-scaled graded AlGaN HFET, (b) the measured charge profile from C-V measurement compared with a simulated charge profile
from AlN mole fraction of 0% (bottom) to 50% (top), to have the charge confined in the bottom 5 nm of the graded region, where the AlN mole fraction changes from 0% to 15%, similar to the AlGaN/GaN HEMT with an inserted graded channel described in section 5.1.

To address the issue of high contact resistance, $R_C$, we used selective MBE regrowth of n$^+$ GaN/reverse-graded (50→0%) n$^+$ AlGaN layers on the Ohmic region as described earlier in section 3.2. From the TLM measurements on the specific die where the DC and RF measurement were performed, the total Ohmic contact resistance, $R_{C,\text{Total}}$, was estimated to be 0.075 Ω·mm, and the sheet resistivity, $R_{\text{sh}}$, was found to be 957 Ω/□ which are in agreement with Halls measurement ($R_{\text{sh,Channel}|\text{Hall}} = 985 \text{ Ω/□}, n_S|\text{Hall} = 9.2 \times 10^{12} \text{ cm}^{-2}, \mu_e|\text{Hall} = 690 \text{ cm}^2/\text{V·s}$).

A T-shaped gate profile using ZEP/PMGI/ZEP process was defined using Vistec® EBPG-5000 e-beam writer. Schottky contact for the gates with a metal stack of Ni (20 nm)/Al(200nm)/Ni(30 nm) was deposited using e-beam evaporator for these highly scaled transistors. A gate length, $L_g$, of 250 nm, the gate head length, $L_{\text{Head}}$, of 500 nm, the stem height, $t_{\text{Stem}}$, of 80, and the head height, $t_{\text{Head}}$, of 250 nm were measured using SEM. This gate is located at the center of the active region with the regrown wall-to-wall distance, $L_{\text{DS}}$, of 920 nm.

The DC characteristics of the fabricated gate-recessed graded AlGaN HFET were measured using Agilent B1500 parameter analyzer, and is shown in Figure 5.10. The recessed gate maintains a good channel control which results in the good pinch-off characteristics with $I_{\text{on}}/I_{\text{off}} > 1 \times 10^3$. From two-terminal gate-drain I-V, the breakdown
Figure 5.10 DC characteristics of (a) $I_{DS}-V_{DS}$ and (b) $g_m-V_{GS}$ (inset: $I_{DS}-V_{GS}$) of a graded AlGaN HFET with $L_g$ of 250 nm and $W_g$ of $2 \times 50$ µm.
voltage, $V_{Br}$, defined at 1 mA/mm of the reverse gate current was estimated to be $\sim 16$ V in spite of the triangle shaped graded AlGaN barrier and a short gate-to-drain spacing. Although the $V_{Br}$ and the vertical scaling using a recess-etch technology for this transistor structure is limited by the gate leakage current, it could be improved using a better Schottky metal such as Pt, or O$_2$ plasma treatment as available elsewhere [54, 197]. The maximum drain current density at $V_{GS} = 1$ V was found to be 1.44 A/mm The ultralow contact resistance along with the highly scaled source-to-drain spacing yielded a low $R_{on}$ resistance of 1 $\Omega \cdot$mm in Figure 5.10 (a).

From the transfer characteristics shown in Figure 5.10 (b), it was found that there is only slight threshold voltage shift with different drain bias, and $V_{Th}$ was found to be at $V_{gs} \sim -3$ V. The transconductance profiles at different $V_{DS}$ reaches its peak value at $V_{GS} = -2$ V, and gets flatter as the $V_{DS}$ increases. We could find a flat transconductance profile for the applied $V_{DS}$ beyond 5 V, and the $g_m$ value in the plateau stayed in the range of 370 $\pm$ 10 mS/mm. This is $\sim 2.5x$ higher value compared to the extrinsic $g_m$ value found in the AlGaN/GaN with an inserted graded AlGaN channel in section 5.1, and is also higher than the intrinsic $g_m$ value of our previous work which could be achieved from the minimized source resistance.

The small signal RF performance of this transistor was measured using Agilent E8361 programmable network analyzer (PNA) at room temperature. The PNA was calibrated using short-open-load-through (SOLT) off-wafer impedance standards before the device measurements. On-wafer s-parameter measurements for different $V_{DS}$ and $V_{GS}$ were measured in the frequency range from 100MHz to 67 GHz, the drain bias range from 1
to 6 V, and the gate bias range from -2.5 to 0 V.

The highest $f_{T,\text{extrinsic}}$ and $f_{\text{max,extrinsic}}$ of this device was found at $V_{GS} = -1.8$ V and $V_{DS} = 6$ V as shown in Figure 5.11. Typically, the parasitic capacitance from the coplanar waveguide structure of the contact pads lowers the intrinsic $f_T$ and $f_{\text{max}}$ by 10-20%. Thus, it is expected to have $f_T$ and $f_{\text{max}}$ within the range of 60-66 GHz, and 100-110 GHz, respectively, after de-embedding the pad capacitances. A short stem height ($t_{\text{Stem}} = 80$ nm) possibly induces a high parasitic capacitance which is responsible for the low $f_T$ and $f_{\text{max}}$ for the relatively short $L_g$ of 250 nm.

In Figure 5.12, bias-dependent $f_T$ and $f_{\text{max}}$ curves are depicted as a function of the applied gate bias, $V_{GS}$. Since $f_{\text{max}}$ is directly proportional to $f_T$ and $f_{T-VGS}$ generally follows the trend of the transconductance profile, the improvement in the linearity of the $g_m$ with
Figure 5.12 Bias-dependent (a) $f_T$ and (b) $f_{\text{max}}$ of a graded AlGaN HFET with $L_g = 250$ nm and $W_g = 2 \times 50$ µm
increasing drain bias is found to manifest as improved linearity in measured $f_T$ and $f_{max}$ respect to the applied gate bias.

Due to an increasing capacitance profile of the given structure while the $g_m$ profile that stayed flat, $f_T$ given by $f_T \sim g_m / (2\pi \cdot C_{gs})$, and the $f_{max}$ decrease consequently as the gate bias is increases. Thus, an increasing $g_m$ profile to overcome the increasing capacitance is required to have flat $f_T$ and $f_{max}$ profiles.

A transistor with a longer gate length ($L_g = 450$ nm) but with a narrower device width ($2 \times 20$ $\mu$m) showed an increasing $g_m$ profile as shown in Figure 5.13 (a) in which the poor pinch-off was not due to short-channel effect, but a disconnected gate finger near the edge of the isolated MESA. In this device, we could find the plateau of $f_T$ and $f_{max}$, which are staying flat at $32 \pm 2$ GHz and $66 \pm 5$ GHz for the gate bias ranging from -2.3 to 0 V and the drain current range between 0.17 and 1 A/mm. Although there are reports about the improved $g_m$ and $f_T$ linearity, this is the first demonstration of having flat $f_T$ and $f_{max}$ over the wide input bias and output current ranges.

Consider the other expression for $f_T$ given by, $f_T (V_{gs}) \sim \nu_e(V_{gs})/(2\pi \cdot L_g)$, the results shown in Figure 5.13 (b) implies that the device is not suffering from the degradation of the electron velocity by LO phonon scattering or dynamic source resistance which are responsible for the dropping $g_m$ and $f_T$. In other word, the electron velocity stays constant throughout the available output current range, and this can lead a significant improvement of the high frequency RF power performance of HEMT devices for the future mm-Wave applications.
Figure 5.13 (a) DC transfer characteristics and (b) bias-dependent $f_T$ and $f_{\text{max}}$ of a graded AlGaN HFET with $L_g = 450$ nm $W_g = 2 \times 20$ µm at $V_{DS} = 6$ V
5.3 Summary

In this chapter, we have demonstrated flat $g_m$ profiles in both highly scaled AlGaN/GaN HEMT and graded AlGaN HFET using polarization-engineered channel design. High gain and high linearity are simultaneously achieved by distributing charges across 5 nm wide channel depth in both transistor structure with an appropriate grading scheme. Flat $f_T$ and $f_{max}$ over wide input voltage ($V_{gs}$) and output current range ($I_D$) were achieved with a careful ensemble of advanced process technologies including the geometrical device scaling, the regrown source/drain Ohmic contact, and low-damage gate recess.

These results demonstrate the potential of FETs with a graded channel in achieving both high speed and high power RF performance simultaneously without degrading in efficiency. In addition, these results encourage the exploration of multi-wavefunction, or 3D electron gas channels for future III-Nitride transistors.
Chapter 6
Conclusions and future work

6.1 Conclusions

In this dissertation, critical factors for the RF performance of III-Nitride HEMTs were investigated, and mainly dealt with engineering the channel layer of III-Nitride HEMT structure for high frequency performance.

To mitigate short-channel effects, the buffer layer and the aspect ratio play the most important role in GaN-based HEMT. Thus, the carrier confinement and the effect of the quantum displacement in GaN channel were studied through simulation modeling as well as the experimental measurements for Ga-polar and N-polar AlGaN/GaN HEMT structures. In this study, we found advantages with the N-polar oriented structure such as more rigorous electron confinement in the 2DEG due to the electrostatic back-barrier, and a negative quantum displacement. This emphasized the importance of a back-barrier and higher aspect ratio rather than making a competition between Ga-polar and N-polar orientations.

Non-alloyed Ohmic contacts are required for the aggressive device scaling as well as for the long-term reliability. We have suggested two new ways to form a non-alloyed
Ohmic contact to 2DEG using the insertion of graphene between metal and AlGaN barrier layer, and a polarization grading scheme. Both methods exploit the current conduction path where no barrier exists from the metal contact to the channel. Especially, for the polarization graded AlGaN Ohmic layer, we have achieved the record low contact resistance to the best of our knowledge from this work. This also simplify the fabrication process by growing the entire structure including the graded Ohmic layer together.

The saturation of electron velocity in GaN channel was investigated based on the effect of LO phonon emission with respect to the electron carrier density in the channel. Detailed physics behind the $g_m$ reduction was described and modeled for 2-D device simulation. Based on simulation with the newly developed velocity saturation model, three different HEMT structures were examined, and their results validated the model used here. This new simulation model could enable the investigation of local electron velocity in a HEMT structure to find the point where the high speed transport is limited.

Polarization graded AlGaN channel in AlGaN/GaN HEMT and graded AlGaN HFET were investigated, and an unprecedented flat transconductance profile could be achieved using this channel. To obtain the high frequency performance of this channel, the formerly mentioned graded n+ AlGaN Ohmic layer with submicron gates were exploited. The combination of these advanced process technologies along with the epitaxial design for the device scaling resulted in flat $f_T$ and $f_{max}$ profiles which have never been seen before.
6.1.1 Short-channel effects

The following two issues are responsible for the short-channel effects in GaN-based HEMT. First one is poor electron confinement from the most commonly used single heterojunction configuration of the GaN-channel HEMT structure. The other is a poor modulation efficiency of the gate from a low aspect ratio of \( L_g/d \). Short-channel effects caused by these two result in a large threshold voltage shift, soft pinch-off, and high output conductance which are limiting the high frequency performance of \( f_T \) and \( f_{max} \).

In this dissertation, we investigated about short-channel effects in GaN-based HEMTs using 2 dimensional device simulation. Three different device structures of conventional single heterojunction AlGaN/GaN, double-heterojunction AlGaN/GaN/AlGaN, and N-polar GaN/AlGaN/GaN were examined for this study. It was found that the drain-induced barrier-lowering and the space-charge-limited current injection into the buffer are responsible for short-channel effect.

Among all three devices, the N-polar HEMT which has the highest electrostatic back-barrier height showed the best suppression of short-channel effects from the simulation. Although imperfect electrostatic barrier due to the composition fluctuation of the AlGaN back-barrier in a practical N-polar GaN/AlGaN/GaN HEMT could lead short-channel effects, we have shown the importance of a back-barrier structure for suppression of short-channel effect with an improved charge confinement.

Secondly, the effect of the quantum displacement in 2DEG was discussed. With the existence of polarization in Nitride material, the HEMT structure can be chosen to be a conventional structure or an inverted structure. In two different HEMT structure, the
extension of wavefunction in 2DEG known as a quantum displacement ($\Delta d$) can change the actual gate-to-channel distance and plays an important role when the device is deeply scaled down.

From simulation and experimental measurement, the quantum displacement in N-polar GaN HEMT was found to be in a range between –1 to -3.5 nm while Ga-polar GaN HEMT has ~2 nm of $\Delta d$. Since the minimum aspect ratio ($L_g/d$) required to minimize short-channel effect is suggested to be 10 for a structure with a back-barrier and 15 for a convention structure for GaN-based HEMT. When the physical thickness of the barrier layer become thinner than 6 nm, there will exist more than 2X difference in the gate-source capacitance between N-polar and Ga-polar structures.

### 6.1.2 Non-alloyed Ohmic contact

Non-alloyed Ohmic contact are important not only for the improvement of high frequency RF performance, but also for the long-term reliability of GaN-based HEMT technology. Selective regrown Ohmic layer using molecular-beam epitaxy is now widely used to for a low-resistance non-alloyed Ohmic contacts. However, unlike N-polar GaN HEMT, a direct growth of n$^+$ GaN on top of Ga-polar GaN HEMT structures have considerably high resistance due to the wide-bandgap barrier layer on top, and consequently it needs extra fabrication process steps for the barrier layer removal.

To minimize the complex preparation and fabrication process, we suggested two new methods in this work to form non-alloyed Ohmic contacts to 2DEG in AlGaN HFET structures. The First method was to use a graphene layer insertion between metal and
AlGaN. It was found the inserted graphene layer becomes n-doped by changing the work-function of graphene to that of the contact metal used. The changed work-function of n-doped graphene brought the conduction band down at the graphene/AlGaN interface, and the percolation-based electron transport through GaN-like region in AlGaN layer was attributed to the Ohmic behavior.

Secondly, we designed a graded AlGaN layer structure which has a continuous 3DES. The structure consists of a graded UID AlGaN layer (0 → 50%) and a reversely-graded n⁺ AlGaN layer (50 → 0%) from bottom to top. From this structure, we prove there is no barrier formed in between upper and lower graded AlGaN layer which led the record low contact resistance of 0.049 Ω·mm for Ga-polar HFET structure with no recess-etching which is commonly used for Ga-polar HEMT technology.

**6.1.3 Low electron velocity in GaN channel device**

Although the electron velocity in GaN channel is expected from theoretical calculations to be $2 \times 2.7 \times 10^7$ cm/s, the measured value has been found to be only $1 \times 1.5 \times 10^7$ cm/s for most of practical GaN HEMT devices. Since effective electron velocity is the key ingredient in intrinsic high frequency performance in GaN HEMTs there has been a great deal of interest in finding the exact electron velocity in the device experimentally.

In this work, we have investigated the recently reported model for the optical-phonon mediated electron velocity saturation in GaN HEMTS by amending the several assumptions used in the previously reported models, and derived a new velocity saturation
model which has also been incorporated in a 2-D device simulation to benchmark the DC and RF performance of HEMT devices.

As the validation of our new model, three different GaN-based HEMTs were examined, and it was found the results from both simulations and experimental measurements match each other. From this study, we confirmed the major limiting factor of the low effective electron velocity in GaN channel device is due to a strong interaction between LO phonon and electron carrier in the channel. Moreover, it is also found that the LO phonon-induced velocity saturation is dependent to the electron carrier density, and this dependence causes the rapid reduction in the transconductance profile of GaN HEMT. The new simulation model can be used for the optimization of the HEMT structure to maximize its capability to achieve the best RF performance.

6.1.4 Flat \( g_m \) and \( f_T \)

The transconductance given as \( g_m = dI_D/dV_G \), directly determines the output current gain respect to the input bias. And, it also directly affects the \( f_T \) and \( f_{\text{max}} \) which are the most important figures of merit for the high frequency and high power operation of HEMT devices. The output linearity is closely related to the output gain with respect to the output power. Flat \( f_T \) and \( f_{\text{max}} \) are required to have consistent output gain over a wide output power range for the linear amplification. This implies that a consistent electron velocity which is not dependent to the electron carrier density is needed.

Since \( f_T \) generally follows the trend of \( g_m \) profile, we focused on having a flat transconductance profile to achieve high linearity in \( f_T \) and \( f_{\text{max}} \) profile over a wide input
bias range. Our approach is similar to the graded doping in GaAs MESFET structure, but the electron charges were induced by the polarization gradient. From an AlGaN/GaN HEMT structure with 5 nm of a graded AlGaN as the channel layer, we demonstrated a flat $g_m$ profile for the first time in field-effect-transistors.

To measure the RF performance of the graded AlGaN channel, we carefully redesigned a graded AlGaN HFET structure in which the electron charges are distributed in bottom 5 nm of the graded AlGaN layer similar to the previous structure. Highly scaled transistors were fabricated, and the flat $g_m$ profile also could be achieved with 2.5x improved value compared to our previous work. For the RF response, the linearity of $f_T$ and $f_{\text{max}}$ were found to be greatly improved. However, the $f_T$ and $f_{\text{max}}$ values were not found to be constant for the given input bias range. This is due to an increasing capacitance profile from the structure since the $f_T$ is given by $f_T \sim g_m/(2\pi C_{gs})$. An increasing $g_m$ profile was found in a device with shorter device width of 2 × 20 µm, this increasing $g_m$ compensates the increment in the capacitance, and resulted in flat $f_T$ and $f_{\text{max}}$ profiles which have never seen in any other field-effect-transistor structure including Si and other III-V devices.

6.2 Future works

We have invented and reinvented the entire process technologies used in this work to demonstrate new device concept which can offer a better RF performance. However, the large-signal RF power performance still needs to be investigated for the devices developed in this dissertation. Device passivation is required to prevent the RF dispersion during the large signal device operation. The simulation modeling to investigate the device
performance was only done for GaN-based HEMTs in this work. There is plenty of room for further investigations of HEMT device structures based on the III-Nitride material system which can lead further improvement in RF performance.

6.2.1 Optimization of device scaling and process technology

For the project of highly scaled HFET fabrication, every dimension of the transistor was scaled down including the gate length, the barrier thickness, the source-to-drain spacing, and the device width. To maximize the RF performance within this scaled dimension, it is required to have a minimal source-to-gate spacing to reduce the parasitic resistances and a taller stem height of the gate to minimize parasitic capacitances in a tight box. And, the dimension of the gate head also important to have higher $f_{max}$.

Every dimension of the transistor including the device width should be scaled to achieve a higher frequency performance, but the output power level decreases as a result. To gain back the required power in a discrete transistor, multi-finger of distributed-$\pi$ geometry is required. Unlike two-finger T-layout used for this project, the distributed $\pi$ layout has very complicated communication from each source/gate/drain to others. Thus, a careful design of the structure is required to achieve a true high speed and high power HEMT device.

6.2.2 New channel material for higher frequency operation

We have shown the major factor limiting the effective electron velocity in GaN channel is a strong interaction between LO phonon and the carrier electrons, also found to be the
reason for the dropping $g_m$ profile. Although we have suggested a graded AlGaN channel to mitigate the dropping behavior of the transconductance, the effective electron velocity in such channel has not been investigated. Moreover, we only investigated the device performance of the graded channel having the channel depth of 3 nm and 5 nm. Thus, the future work of this polarization graded channel could be to explore the measurement of the effective electron velocity in various depth of the channel.

Another approach to increasing the high frequency capability of III-Nitride material-based HEMTS is the use of In containing channel material such as InGaN or InN. At this point in time, the highest record with InGaN channel was obtained from In$_{0.05}$Ga$_{0.95}$N channel layer. Higher In content channel would be interesting to investigate for velocity performance. Although it is hard to grow a thin InN layer directly onto GaN substrate due to a large lattice mismatch, a high composition InGaN (In content of 25 ~ 35%) can be grown on GaN template. An extensive growth study is required to have high quality with low back-ground doping density for HEMT operation. Moreover, this growth study may enable high quality InGaN buffer layer on which InN layer can be utilized as the channel layer.

### 6.2.3 Expansion of the simulation modeling

The simulation modeling work in this project only include the models for the velocity saturation, polarization effect, the surface pinning and the semi-insulating GaN buffer, and the rest of the models such as gate leakage current, surface/buffer trap related dispersion, and thermal effects on the carrier transport were neglected for simplification. Although the
model developed here could predict the device performance reasonably well, these neglected models of thermal-effect, trapping effect, and the gate leakage needs to be included to have a more accurate prediction of the RF power performance. Especially, the breakdown model is critical for high power, and needs an immediate investigation.

Once these models are included for GaN-based HEMTs, the simulation model could be expanded for other channel material such as graded AlGaN channel, and the relatively unexplored In(Ga)N channel.
Appendix A

Derivation of Small-Signal Circuit Parameters

Figure A.1 Small-signal equivalent circuit of a HEMT structure

Using DUT, open, and short measurement structures [198], the capacitance and inductance from CPW pads can be de-embedded, then the impedance matrix for the active region can be obtained from measured scattering parameters as,

\[
Z_A = Z[y_{DUT} - y_{open}] - Z[y_{short} - y_{open}] \tag{A.1}
\]

where the impedance (Z) and admittance (Y) matrices of each structure can be converted from the measured scattering matrix (S) from following conversion rules.
The access resistances of $R_s$ and $R_d$ can be measured using the gate current injection method [199] and the gate resistance $R_g$ can be extracted from the zero-biased $Z$-parameters at low frequency range [200]. These parasitic resistances for the device shown in Figure 1.3 also can be obtained from simple calculations written in Eq. (A.6)-(A.9)
\[ R_s = R_C + R_{Sh,Ver} + R_{Sh,Lat} + R_{3D-2D} + R_{s,acc}. \]  
(A.6)

\[ R_d = R_C + R_{Sh,Ver} + R_{Sh,Lat} + R_{3D-2D} + R_{d,acc}. \]  
(A.7)

\[ R_{g,DC} = \frac{W_g}{A} \]  
(A.8)

\[ R_{g,RF} = \frac{R_{g,DC}}{3} \]  
(A.9)

The reduction of the RF gate resistance in Eq. (A.9) is due to the distributed charges along the gate when the transistor is under biased condition [201].

The intrinsic impedance matrix can be extracted by subtraction of these resistances as

\[
Z_{\text{intrinsic}} = \begin{bmatrix}
Z_{A,11} - R_g - R_s & Z_{A,12} - R_s \\
Z_{A,21} - R_s & Z_{A,22} - R_d - R_s
\end{bmatrix}
\]  
(A.10)

Then, the remaining circuit elements of the intrinsic parameters can be derived by [49] as

\[ C_{gs} = \sqrt{\frac{\text{Re}(Y_{11} + Y_{12})}{\omega^2 R_i (1 - R_i \text{Re}(Y_{11} + Y_{12}))}} \approx \frac{\text{Im}(Y_{11} + Y_{12})}{\omega} \text{ for a very small } R_i \]  
(A.11)

\[ C_{gd} = \frac{\text{Im}(-Y_{12})}{\omega} \]  
(A.12)
\[ C_{ds} = \frac{\text{Im}(Y_{12} + Y_{22})}{\omega} \]  
(A.13)

\[ R_f = \sqrt{\frac{1}{\omega C_{g_t}} \text{Im}(Y_{11} + Y_{12}) - \left( \frac{1}{\omega C_{gs}} \right)^2} \approx \text{Re} \left( \frac{1}{Y_{11} + Y_{12}} \right) \]  
(A.14)

\[ R_{gd} = \text{Re} \left( \frac{1}{Y_{12}} \right) \]  
(A.15)

\[ g_o = \text{Re}(Y_{12}) + \text{Re}(Y_{22}) \]  
(A.16)

\[ g_m = g_{m0} e^{-j\omega \tau} = (Y_{21} - Y_{12}) \left( 1 + \omega^2 R_f^2 C_{gs}^2 \right) \left( 1 + j\omega \tau_{gm} \right) \]  
(A.17)

\[ g_{m0} = \left| (Y_{21} - Y_{12}) \left( 1 + \omega^2 R_f^2 C_{gs}^2 \right) \left( 1 + j\omega \tau_{gm} \right) \right| \]  
(A.18)

\[ \tau = \frac{1}{\omega} \text{arg} \left[ (Y_{21} - Y_{12}) \left( 1 + \omega^2 R_f^2 C_{gs}^2 \right) \left( 1 + j\omega \tau_{gm} \right) \right] \]  
(A.17)
Appendix B

Simulation Codes

B.1 ATLAS code for AlN/InAlN/AlN/GaN HEMT [185] in 4.3.1

go atlas
#simflags="-P 4"

### The coded date is Sep-29-2013
### The code is written by Pil Sung Park
### Simulation of GaN HEMT structure with 3D optical-phonon-emission model
Set LABEL=JJAP_52_08JN16_ver4

### This simulation is for the DC IV-Characteristics

## Declare Parameters##
Set VgStart=0
Set VgEnd=-5
Set Vd1=8
#Set Vd2=3
Set VgRF=-1.8
Set VdRF=10
Set pol=1
### The lateral spacing of Lgs,Lg,Lgd are 0.5 um, 0.5um, and 0.5um, respectively
## Gate Length
Set Lg=0.2
## Head Length
Set Lhead=0.34
## Recess Length
#Set LRecess=0
## source-drain distance
Set Lsd=0.5
## gate-source distance
Set Lgs=$Lsd/2-$Lg/2
## gate-drain distance
Set Lgd=$Lsd/2-$Lg/2

130
## Contact Length
Set Lc=0.5

# Set Ls1=-$Lg/2-$LRecess
Set Ls0=-$Lg/2
Set Ls1=-$Lhead/2
Set Ls2=-$Lg/2-$Lgs
Set Ls3=$Ls2-$Lc
# Set Ld1=$Lg/2+$LRecess
Set Ld0=$Lg/2
Set Ld1=$Lhead/2
Set Ld2=$Lg/2+$Lgd
Set Ld3=$Ld2+$Lc
## x-dir mesh size
Set Lm1=5e^{-3}
Set Lm2=1e^{-2}
Set Lm3=5e^{-2}
Set Lm4=1e^{-1}

### The sample consisted of 1 um GaN buffer layer followed by a 30 nm Al(0.3)Ga(0.7)N layer
Set tAir=1

## Recess depth
# Set tRecess=20e^{-3}
## Metal thickness
Set tOhmic=0.16
Set tSiN=0.07
Set tGstem=0.2
Set tHead=0.385
Set tGate=tGstem+tHead
## Barrier#1 thickness
Set tBar1=15e^{-4}
## Barrier#2 thickness
Set tBar2=35e^{-4}
## Barrier#3 thickness
Set tBar3=1e^{-3}
## Channel thickness
set tCh=1e^{-2}
## Buffer#1 thickness
set tB1=19e^{-2}
## Buffer#2 thickness
set tB2=1.8
##
set t1=tBar1+tBar2
set t2=tBar1+tBar2+tBar3
set t3=t1+tCh
set t4=t3+tB1
set t5=t4+tB2
## Mesh size
set Tm1=5e-4
set Tm2=$t1/5
set Tm3=1e-2
set Tm4=4e-2
set Tm5=1e-1

# 1 Mesh

mesh
## Set x-dir meshes
x.m l=$Ls3 s=$Lm4
x.m l=$Ls2 s=$Lm1
x.m l=$Ls2+0.035 s=$Lm2
x.m l=$(Ls1+$Ls2)/2 s=$Lm2
x.m l=$Ls1 s=$Lm1
x.m l=$(Ls1+$Ls0)/2 s=$Lm2
x.m l=$Ls0/2 s=$Lm1
x.m l=0 s=$Lm2
x.m l=$Ld0/2 s=$Lm1
x.m l=$(Ld1+$Ld0)/2 s=$Lm2
x.m l=$Ld1 s=$Lm1
x.m l=$(Ld1+$Ld2)/2 s=$Lm2
x.m l=$Ld2-0.07 s=$Lm1
x.m l=$Ld2-0.035 s=$Lm2
x.m l=$Ld2 s=$Lm1
x.m l=$Ld3 s=$Lm4
## Set y-dir meshes
y.m l=$tAir s=$Tm5
y.m l=-0.655 s=0.035
y.m l=-0.23 s=0.035
y.m l=$tGstem s=$Tm4
y.m l=$tOhmic s=$Tm4
y.m l=0 s=$Tm2
y.m l=$tBar1 s=$Tm1
y.m l=$t3 s=$Tm1
y.m l=$t4 s=$Tm4
y.m l=$t5 s=$Tm5

## Reduce the number of meshes
#eliminate columns x.min=$Ls3 x.max=$Ld3 y.min=0.5 y.max=$t5
#eliminate columns x.min=$Ls3 x.max=$Ld3 y.min=$tAir y.max=-0.5

### 2 Structure
#
region num=1 material=Air x.min=$Ls3 x.max=$Ld3
  y.min=-$tAir y.max=0
region num=2 material=SiN x.min=$Ls3 x.max=$Ld3
    y.min=-0.23 y.max=0
region num=3 material=Air x.min=$Ls2+0.07 x.max=$Ld2-0.07
    y.min=-$tAir y.max=0
region num=4 material=SiN x.min=$Ls1 x.max=$Ld1 y.min=-0.655
    y.max=0
region num=5 material=AlGaN x.min=$Ls3 x.max=$Ld3
    y.min=0 y.max=$tBar1 donor=1e16 polarization polar.scale=$pol calc.strain x.comp=1
region num=6 material=InAlN x.min=$Ls3 x.max=$Ld3
    y.min=$tBar1 y.max=$t1 donor=1e16 polarization polar.scale=$pol calc.strain x.comp=0.866
region num=7 material=AlGaN x.min=$Ls3 x.max=$Ld3
    y.min=$t1 y.max=$t2 donor=1e16 polarization polar.scale=$pol calc.strain x.comp=1
region num=8 material=GaN x.min=$Ls3 x.max=$Ld3
    y.min=$t2 y.max=$t4 donor=2e16 polarization polar.scale=$pol
region num=9 material=GaN x.min=$Ls3 x.max=$Ld3
    y.min=$t4 y.max=$t5 insulator polarization polar.scale=$pol substrate
region num=10 material=GaN x.min=$Ls3 x.max=$Ld3
    y.min=0 y.max=$t3 donor=1e21
region num=11 material=GaN x.min=$Ld2 x.max=$Ld3
    y.min=0 y.max=$t3 donor=1e21
region num=12 material=Gold x.min=$Ls3 x.max=$Ls2 y.min=-$tOhmic y.max=0
region num=13 material=Gold x.min=$Ls0 x.max=$Ld0 y.min=-$tGate y.max=0.0
region num=14 material=Gold x.min=$Ld2 x.max=$Ld3 y.min=-$tOhmic y.max=0
#
## Electrodes
#
# Source
elec num=1 name=source x.min=$Ls3 x.max=$Ls2 y.min=-$tOhmic
    y.max=0
#
# Gate
elec num=2 name=gate x.min=$Ls0 x.max=$Ld0 y.min=-$tGate
    y.max=0.0
#
# Drain
elec num=3 name=drain x.min=$Ld2 x.max=$Ld3 y.min=-$tOhmic
    y.max=0
#
## 3 Material
material kp.set2 pol.set3
#material material=AlGaN affinity=3.44 eg300=3.967 psp=-0.0446
alattice=3.1659 c13=104.5 c33=395.4 e31=-0.523 e33=0.949
taun0=1e-9 taup0=1e-9 copt=1.1e-8 augment=1.0e-34 augp=1.0e-34 mup=1
material material=AlN affinity=1.9 eg300=6.2 psp=-0.081
alattice=3.112 c13=108 c33=373 e31=-0.6 e33=1.46 taun0=1e-9

taup0=1e-9 copt=1.1e-8 augment=1.0e-34 augp=1.0e-34 mup=1 vsatp=1
F.TOFIMUN=OP_gan2.lib
material material=GaN affinity=4.1 eg300=3.4 psp=-0.029
alattice=3.189 c13=103 c33=405 e31=-0.49 e33=0.73
taun0=1e-9 taup0=1e-9 copt=1.1e-8 augment=1.0e-34 augp=1.0e-34 mup=1
vsatp=1 F.TOFIMUN=OP_gan2.lib

# contact name=gate workfunc=6.7 resistance=660
contact name=source resistance=300
contact name=drain resistance=300
#
# inttrap s.i acceptor e.level=4.1 density=5e13 degen=4
# sign=2.84e-15 signp=2.84e-14 x.min=$Ls2 x.max=$Ls0 y.min=0 y.max=0
# inttrap s.i acceptor e.level=4.1 density=5e13 degen=4
# sign=2.84e-15 signp=2.84e-14 x.min=$Ld0 x.max=$Ld2 y.min=0 y.max=0
# trap acceptor e.level=3.28 density=3e15 degen=4 sign=2.84e-15
# signp=2.84e-14 x.min=$Ls3 x.max=$Ld3 y.min=$t4 y.max=$t5

models srh fldmob fermi spontaneous print
#
# 4 Solution
method newton carr=2 itlim=50 trap maxtrap=20 print

output con.band val.band charge polar.charge flowlines e.velocity
ex.velocity ey.velocity e.mobility e.temp
#
solve init
save outf="$LABEL"_Lg($Lg).str master
#
# master structures as a function of the gate bias
### DC I-V characteristics
solve vgate=0
save outf="$LABEL"_Lg($Lg)_Vg(0).str master
solve vgate=-1
save outf="$LABEL"_Lg($Lg)_Vg(-1).str master
solve vgate=-2
save outf="$LABEL"_Lg($Lg)_Vg(-2).str master
solve vgate=-3
save outf="$LABEL"_Lg($Lg)_Vg(-3).str master
solve vgate=-4
134
save outf=$"LABEL"_Lg($Lg)_Vg(-4).str master

load inf=$"LABEL"_Lg($Lg)_Vg(0).str master
log out=$"LABEL"_IV_Vg(0)_Lg($Lg).log master
solve name=drain vdrain=0 vstep=0.1 vfinal=2
save outf=$"LABEL"_Vg(0)_Vd(2)_Lg($Lg).str master
solve name=drain vdrain=2.1 vstep=0.1 vfinal=4
save outf=$"LABEL"_Vg(0)_Vd(4)_Lg($Lg).str master
solve name=drain vdrain=4.1 vstep=0.1 vfinal=6
save outf=$"LABEL"_Vg(0)_Vd(6)_Lg($Lg).str master
solve name=drain vdrain=6.1 vstep=0.1 vfinal=8
save outf=$"LABEL"_Vg(0)_Vd(8)_Lg($Lg).str master
#solve name=drain vdrain=8.1 vstep=0.1 vfinal=10
#save outf=$"LABEL"_Vg(0)_Vd(10)_Lg($Lg).str master
log off

load inf=$"LABEL"_Lg($Lg)_Vg(-1).str master
log out=$"LABEL"_IV_Vg(-1)_Lg($Lg).log master
solve name=drain vdrain=0 vstep=0.1 vfinal=2
save outf=$"LABEL"_Vg(-1)_Vd(2)_Lg($Lg).str master
solve name=drain vdrain=2.1 vstep=0.1 vfinal=4
save outf=$"LABEL"_Vg(-1)_Vd(4)_Lg($Lg).str master
solve name=drain vdrain=4.1 vstep=0.1 vfinal=6
save outf=$"LABEL"_Vg(-1)_Vd(6)_Lg($Lg).str master
solve name=drain vdrain=6.1 vstep=0.1 vfinal=8
save outf=$"LABEL"_Vg(-1)_Vd(8)_Lg($Lg).str master
#solve name=drain vdrain=8.1 vstep=0.1 vfinal=10
#save outf=$"LABEL"_Vg(-1)_Vd(10)_Lg($Lg).str master
log off

load inf=$"LABEL"_Lg($Lg)_Vg(-2).str master
log out=$"LABEL"_IV_Vg(-2)_Lg($Lg).log master
solve name=drain vdrain=0 vstep=0.1 vfinal=2
save outf=$"LABEL"_Vg(-2)_Vd(2)_Lg($Lg).str master
solve name=drain vdrain=2.1 vstep=0.1 vfinal=4
save outf=$"LABEL"_Vg(-2)_Vd(4)_Lg($Lg).str master
solve name=drain vdrain=4.1 vstep=0.1 vfinal=6
save outf=$"LABEL"_Vg(-2)_Vd(6)_Lg($Lg).str master
solve name=drain vdrain=6.1 vstep=0.1 vfinal=8
save outf=$"LABEL"_Vg(-2)_Vd(8)_Lg($Lg).str master
#solve name=drain vdrain=8.1 vstep=0.1 vfinal=10
#save outf=$"LABEL"_Vg(-2)_Vd(10)_Lg($Lg).str master
log off

load inf=$"LABEL"_Lg($Lg)_Vg(-3).str master
log out=$"LABEL"_IV_Vg(-3)_Lg($Lg).log master
solve name=drain vdrain=0 vstep=0.1 vfinal=2
save outf=$"LABEL"_Vg(-3)_Vd(2)_Lg($Lg).str master
solve name=drain vdrain=2.1 vstep=0.1 vfinal=4
save outf=$"LABEL"_Vg(-3)_Vd(4)_Lg($Lg).str master
solve name=drain vdrain=4.1 vstep=0.1 vfinal=6
save outf=$"LABEL"_Vg(-3)_Vd(6)_Lg($Lg).str master
solve name=drain vdrain=6.1 vstep=0.1 vfinal=8
save outf=$"LABEL"_Vg(-3)_Vd(8)_Lg($Lg).str master
#solve name=drain vdrain=8.1 vstep=0.1 vfinal=10
#save outf=$"LABEL"_Vg(-3)_Vd(10)_Lg($Lg).str master
log off

load inf=$"LABEL"_Lg($Lg)_Vg(-4).str master
log outf=$"LABEL"_IV_Vg(-4)_Lg($Lg).log master
solve name=drain vdrain=0 vstep=0.1 vfinal=2
save outf=$"LABEL"_Vg(-4)_Vd(2)_Lg($Lg).str master
solve name=drain vdrain=2.1 vstep=0.1 vfinal=4
save outf=$"LABEL"_Vg(-4)_Vd(4)_Lg($Lg).str master
solve name=drain vdrain=4.1 vstep=0.1 vfinal=6
save outf=$"LABEL"_Vg(-4)_Vd(6)_Lg($Lg).str master
solve name=drain vdrain=6.1 vstep=0.1 vfinal=8
save outf=$"LABEL"_Vg(-4)_Vd(8)_Lg($Lg).str master
#solve name=drain vdrain=8.1 vstep=0.1 vfinal=10
#save outf=$"LABEL"_Vg(-4)_Vd(10)_Lg($Lg).str master
log off

load inf=$"LABEL"_Lg($Lg)_Vg(0).str master
solve vdrain=$Vd1
log outf=$"LABEL"_IdVg_Vd($Vd1)_Lg($Lg).log master
solve name=gate vgate=$VgStart vstep=-0.1 vfinal=$VgEnd
log off

### RF small-signal characteristics
load inf=$"LABEL"_Lg($Lg)_Vg(0).str master
solve name=gate vgate=-0.1 vstep=-0.1 vfinal=$VgRF
log outf=$"LABEL"_IV_Vg($VgRF)_Vd($VdRF)_Lg($Lg).log master
width=50
solve name=drain vdrain=0 vstep=0.1 vfinal=$VdRF
save outf=$"LABEL"_Vg($VgRF)_Vd($VdRF)_Lg($Lg).str master
log off

load inf=$"LABEL"_Vg($VgRF)_Vd($VdRF)_Lg($Lg).str master
log outf=$"LABEL"_Vg($VgRF)_Vd($VdRF)_ac.log master gains
s.params inport=gate outport=drain width=50

solve ac freq=10 fstep=10 mult.f nfstep=7
solve ac freq=1e9 fstep=1e9 nfstep=8
solve ac freq=1e10 fstep=5e9 nfstep=18
solve ac freq=1e11 fstep=1e11 nfstep=9
log off

136
B.2 C-code library of the optical-phonon mediated velocity saturation model

```c
#include <stdio.h>
#include <stdlib.h>
#include <math.h>
#include <ctype.h>
#include <malloc.h>
#include <string.h>
#include <template.h>

/*
 * Optical Phonon Limited field & charge density dependent mobility model
 * based on General field dependent mobility model for electrons.
 * Total Field Mobility (parallel and perpendicular field components)
 * Statement: MATERIAL/MOBILITY
 * Parameter: F.TOFIMUN
 * Arguments:
 * Eperp [in] - perpendicular electric field (V/cm)
 * Na [in] - acceptor concentration (/cm^3)
 * Nd [in] - donor concentration (/cm^3)
 * nconc [in] - electron concentration (/cm^3)
 * Epar [in] - parallel electric field (V/cm)
 * TL [in] - lattice temperature (K)
 * xcomp [in] - x-species fraction (0-1)
 * ycomp [in] - y-species fraction (0-1)
 * 
 * *mun [return] - hole mobility (cm^2/Vs)
 * *dmundep [return] - derivative of *mun wrt Eperp
 * *dmundepar [return] - derivative of *mun wrt Epar
 * *dmundl [return] - derivative of *mun wrt TL
 * *dmundn [return] - derivative of *mun wrt nconc
 */

int tofimun(double Eperp,double Na,double Nd,double nconc,double Eparl,double TL,double xcomp,double ycomp,double *mun,double *dmundep,double *dmundepar,double *dmundl,double *dmundn) {
```
double n0 = 6e19;
double vsat, mu0;
double beta, a, b, c, d, da, db, dc, dd;

vsat = 1.0e7/(0.38+sqrt(nconc/n0));
mu0=1320;
/* mu0=3000/(1+3/(1+3*sqrt(nconc/n0))); */

if(Eparl == 0)
{
    *mun=mu0;
    *dmundepar = 0.0;
}
else
{
    beta = 2;
    a = mu0*Eparl/vsat;
    b = pow(a,beta);
    c = 1.0 / (1.0 + b);
    d = pow(c,1.0/beta);
    *mun=mu0*d;

da = mu0/vsat;
    db = beta*b/a*da;
    dc = -1.0*pow(1.0+b,-2.0)*db;
    dd = d/(beta*c)*dc;
    *dmundepar = mu0*dd;

    *dmundep=0.0;
    *dmundl =0.0;
    *dmundn = 0.0;
}
return(0);  /* 0 - ok */
Appendix C

Process Traveler for the 2nd gen. Graded AlGaN HFETs

Alignment Marker

- Std Solvent cleaning : ACE/IPA/DI + US for 5’ each
- SiO₂ sacrificial layer (CVD02): 0.9 Torr, N₂O/SiH₄He = 100/300 sccm, 22W for 55” for 20 nm SiO₂
- Std Solvent cleaning : ACE/IPA/DI + US for 5’ each
- Dehydration bake at 150°C for 5’ followed by 5’ cool down
- Drip HMDS 30” wait, Spin HMDS @ 4000 rpm for 40”, 1’ wait
- Spin SPR 950 @ 3500 rpm for 40”
- Soft bake @ 95C for 1’
- 5.4” exposure
- 2’ PEB @ 105C for 2’ cool down
- 2’ Development in MF24A
- Inspection under microscope
- O₂ Descum (Asher): power 90%, O₂ = 25 sccm, duration : 2’ (before running 10’ chamber cleaning with the boat)
- 20” HF Dip 10:1 followed by 1’ DI rinse
- 5’ Cl₂/BCl₃/Ar dry etching : 5mTorr, RIE/ICP = 30 W / 0 W, Cl₂/BCl₃/Ar = 50/5/5 sccm
- Std Solvent cleaning : ACE/IPA/DI + US for 5’ each
- Inspection

**Ohmic Regrowth**

- Removal of SiO₂ sacrificial layer: 1’ HF Dip 10:1 followed by 1’ DI rinse
- Std Solvent cleaning : ACE/IPA/DI + US for 5’ each
- SiO₂ regrowth mask (CVD02): 0.9 Torr, N₂O/SiH₄He = 100/300 sccm, 22W for 22’55” for 500 nm SiO₂
- Std Solvent cleaning : ACE/IPA/DI + US for 5’ each
- Dehydration bake at 150C for 5’ followed by 5’ cool down
- Drip HMDS 30” wait, Spin HMDS @ 4000 rpm for 40”, 1’ wait
- Spin SPR 950 @ 3500 rpm for 40”
- Soft bake @ 95C for 3’
- Spin SPR 950 @ 3500 rpm for 40” (dynamic dispense)
- Soft bake @ 95C for 3’
- 5.4” exposure
- 2’ PEB @ 105C for 2’ cool down
- 2’ Development in MF24A
- Inspection under microscope
- O₂ Descum (Asher): power 90%, O₂ = 25 sccm, duration : 2’ (before running 10’ chamber cleaning with the boat)
- 5’ CF₄/Ar/O₂ dry etching: 5mTorr, RIE/ICP = 120W/120W, CF₄/Ar/O₂ = 20/5/2 sccm
- Std Solvent cleaning : ACE/IPA/DI + US for 5’ each
- Prolonged O₂ Descum (Asher): power 90%, O₂ = 25 sccm, duration : 10’ (before running 10’ chamber cleaning with the boat)
- 3’ BOE(10:1) : DI = 1 : 15 (etch rate after 1 hour stirring: 50 nm/min)
- Inspection (Dektak profilometer, SEM, AFM)
- Std Solvent cleaning : ACE/IPA/DI + US for 5’ each prior to regrowth.
- Regrowth of downward graded n+ (Al)GaN (extensive buffer bake and Ga polishing prior to the growth)
- Inspection (SEM, AFM)
- Poly-(Al)GaN etching: 5’ at 75°C in diluted KOH(~15% wt; KOH 45%:DI = 1:3.5)
- Removal of SiO2 regrowth mask: 5’ in HF 49%

Ohmic Contact

- Std Solvent cleaning : ACE/IPA/DI + US for 5’ each
- Dehydration bake at 150°C for 5’ followed by 5’ cool down
- Spin SPR 950 @ 3500 rpm for 40’
- Soft bake @ 95°C for 1’
- 5.4” exposure
- 2’ PEB @ 105°C for 2’ cool down
- 2’ Development in MF24A
- Inspection under microscope
- O2 Descum (Asher): power 90%, O2 = 25 sccm, duration : 2’ (before running 10’ chamber cleaning with the boat)
- Native oxide removal: HCl:DI=1:3 for 1’ followed by 1’ DI rinse and N2 dry
- Contact Metal Evaporation (EVP03) - Ti/Au/Ni = 20/100/20 nm, rate : 0.3/0.5→1.0/0.3 A/s
- Lift off in heated (85°C) Remover PG for 1 hour with pipette and ultrasonication
- Std Solvent cleaning: ACE/IPA/DI + US for 5’ each
MESA isolation

- Std Solvent cleaning : ACE/IPA/DI + US for 5’ each
- Dehydration bake at 150C for 5’ followed by 5’ cool down
- SPR950 spin @ 3500 rpm for 40”, SB @ 95C for 1’
- Exposure : t=5.4’, f/o=6
- PEB @ 105C for 2’
- Development in MF24A for 2’
- Inspection
- O2 Descum (Asher): power 90%, O2 = 25 sccm, duration : 1’ (before running 10’ chamber cleaning with the boat)
- Device isolation : BCl3/Cl2/Ar=5/50/0 sccm, 5 mTorr, DC=40V (5W), ICP=40W for 4’
  (before running 10’ Ar chamber cleaning and 5’ chamber seasoning were done)
- Std Solvent cleaning : ACE/IPA/DI + US for 5’ each
- Inspection (Optical microscope, Dektak profilometer)

Gate/Source/Drain CPW contact pads

- Std Solvent cleaning : ACE/IPA/DI + US for 5’ each
- Dehydration bake at 150C for 5’ followed by 5’ cool down
- Spin OCG825 @ 6krpm (6krpm/sec accel.) for 40”
- Soft-bake @ 95C for 3’ followed by 3’ cool down
- Drip SPR950, wait 30”, then spin @ 3.5krpm (4krpm/sec accel.) for 60”
- Soft-bake @ 95C for 1’ followed by 1’ cool down
- 5.4” exposure with f/o -12
- Post-exposure-bake @ 105C for 2’
- Develop in MF24A for 50"

- Inspection

- O2 Descum (Asher): power 90%, O2 = 25 sccm, duration : 2’ (before running 10’ chamber cleaning with the boat)

- Pad Metal Evaporation (EVP03) - Ti/Au/Ni = 30/200/30 nm, rate : 0.3/0.5→1.0/0.3 A/s

- Lift off in heated (85C) Remover PG for 2 hour with pipette (no ultrasonication)

- Solvent cleaning: 5’ each ACE/IPA/DI with stirrer (no ultrasonication)

**E-beam gate**

- Solvent cleaning: 5’ each ACE/IPA/DI with stirrer (no ultrasonication)

- Dehydration bake at 150C for 5’ followed by 5’ cool down

- Spin diluted ZEP520A (ZEP:Anisole = 1:1) @ 6krpm (6krpm/sec accel.) for 60"

- Soft-bake @ 200°C for 2’ followed by 2’ cool down

- Spin PMGI-9 @ 4 krpm (6krpm/sec accel.) for 60"

- Soft-bake @ 190’C for 5’ followed by 5’ cool down

- Spin ZEP520A @ 3 krpm (6krpm/sec accel.) for 60"

- Soft-bake @ 200°C for 2’ followed by 2’ cool down

- Al sputtering: 3 mTorr, 150 W, 6˚ 25” (50 nm)

- E-beam writing: 100 KeV/300 µm aperture/ 100 pA

- Development: MF-CD26 for 1’ followed by 1’ DI rinse
  
  → MIBK:MEK=1:1 for 1’30” followed by 30’ IPA rinse

  → MF-CD26 for 30” followed by 1’ DI rinse

  → ZED N50 for 1’30” followed by 30’ IPA rinse

143
- O2 Descum (Asher): power 90%, O2 = 25 sccm, duration : 1’ (before running 10’ chamber cleaning with the boat)

- Gate Metal Evaporation (EVP03) - Ti/Au/Ni = 20/200/30 nm, rate : 0.3/0.5→1.0/0.3 A/s

- Overnight lift off in Remover PG

- Gentle pipetting (no ultrasonication)

- Solvent cleaning: 3’ each ACE/IPA/DI with stirrer (no ultrasonication)

- Inspection
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150


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157


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