Catalyst-free III-nitride Nanowires by Plasma-assisted Molecular Beam Epitaxy: Growth, Characterization, and Applications

DISSERTATION

Presented in Partial Fulfillment of the Requirements for the Degree Doctor of Philosophy in the Graduate School of The Ohio State University

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2013

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Abstract

In the past twenty years, III-nitride devices have had an enormous impact on semiconductor-based technologies. This impact is seen in both optoelectronic and electronic devices. The aim of this dissertation is to take advantage of III-nitride nanowires grown by plasma-assisted molecular beam epitaxy to form heterostructures that are difficult or impossible to achieve in traditional, thin films. To do this, it is first necessary to establish the growth phase diagrams that correlate the characteristics of GaN nanowires to MBE growth conditions. By using the information in these growth maps we can control growth kinetics and the resulting nanowire structures by making strategic, timely changes to growth conditions. Using this control electronic and optoelectronic III-nitride nanowire devices are created. First, coaxially-oriented AlN/GaN nanowire resonant tunneling diodes are formed on Si substrates. Second, polarization-induced nanowire light emitting diodes (PINLEDs) are fabricated that exhibit electroluminescence at wavelengths from the deep UV into the visible. Because these PINLEDs utilize polarization doping, they can be formed with and without the use of dopants. Device and structural characterization are provided, including a detailed investigation of the mixed material polarity in these nanowires. Finally, the dissertation closes with a discussion of recent work and future ideas for optimizing the PINLED design.
Dedication

This work is dedicated to my lovely wife, Jess.
Acknowledgments

This work would have been impossible without the help of my friends and colleagues at OSU. I'd like to begin by mentioning all of those people "in the trenches" with me over the years. When I first arrived at OSU, Jing Yang and I were the only Myers Group members. We learned so much together, and through that time she has been a constant friend and ally. Thomas Kent provided all of the optical work in this dissertation. We got the PINLED project off the ground together. ATMG Sarwar provided the more onerous nanowire device modeling, and has helped me answer many device related questions. Patrick Phillips put in many hours on the TEM to provide the beautiful images that make the rest of us look good. All of the STEM images in this text are due to Patrick's hard work. I consider them all great friends, and I so happy I got to know them.

Of course, the family of MBE growers at OSU deserve to receive thanks. My fellow nitride MBE growers Digbijoy Nath, Sriram Krishnamoorthy, Fatih Aykol, Masihhur Laskar, and Alessandro Giussani (in addition to the Myers Group growers: Jing, Thomas and Sarwar) have all been great people to work with. I must also thank the As/P MBE growers: Andrew Carlin, Tyler Grassman, Javier Grandal, Krishna Swaminathan, and Chris Ratcliff. They were often the first people I would ask about MBE-related issues, and as a consequence I have learned a good deal of what I know about MBE and vacuum systems from them.
Obviously, I cannot discuss MBE work without mentioning Mark Brenner. Without Mark's patience and guidance, all of the work we have done on the MBE system would have been tremendously more difficult, and not nearly as much fun.

All of the other staff members in various roles on campus should be acknowledged. Cameron Begg from CEOFF (and now CEMAS) taught me how to use the SEMs and assisted all of my SEM work throughout my time at OSU. Camelia Selcu performed the individual nanowire measurements in Chapter 3 and the C-AFM in Chapter 5. Jim Jones taught me how to use all of the equipment in the Dreese cleanroom, and Denis Pelekhov taught me XRD. I am grateful for all of their help.

The professors in the MSE and ECE departments at OSU deserve thanks. I was lucky to learn from many wonderful professors, and I would like to specifically mention Suliman Dregia, Mike Mills, Pete Anderson, Yunzhi Wang, JC Zhao, Len Brillson, and Steve Ringel. Siddharth Rajan was not only an effective instructor, but his feedback on my research has been invaluable from just about the first day I arrived at OSU. Finally, I’d like to thank my advisor, Roberto Myers. I have learned more about science and research from him than anyone else, for which I will always be grateful. I am happy to have been a part of the Myers group in the early days of what will certainly be Roberto’s long and illustrious career.
Finally, I need to thank my family. Each of the adults in my family has helped me get to this point in their own way. My mother read to me every night as a child, and stressed the importance of a good education. My father instilled in me a love of ideas (especially crazy ones). My Uncle Armand and I loved to do math and logic puzzles together, which I believed honed my critical thinking skills from an early age. My grandparents, Noni, Nono, and Pepe, helped out in whatever way they could (e.g. help with school projects, driving me to school in the morning, picking me up from band practice at night, etc). Without their collective effort, I never would have been able to pursue my goals in education and get to this point. I love you all.
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Chapter 1

Introduction

1.1 Background on III-nitrides

Since the foundational work on blue light-emitting diodes and lasers by Shuji Nakamura in the early 1990's[1-5], the Group III-nitride family of semiconductors (GaN, AlN, and InN) has shown its importance in a number of applications. Due to their wide range of direct band gaps (GaN=3.4 eV, AlN=6.2 eV, and InN=0.7 eV), the III-nitrides are obviously attractive for use in optoelectronic devices. While III-N-based blue LEDs and lasers have already had an enormous impact on the solid-state lighting industry, the largest impact of the nitrides will likely come in the future employment of white light LEDs for general lighting purposes. The U.S. Department of Energy has set a goal that by the year 2025 white light LEDs will account for roughly 60% of the nation’s general lighting usage. This transition from less efficient light sources to LEDs could save up to 217 TW-h of energy, a savings that will match the predicted combined output of all renewable sources of energy in the same time frame[6].

Based on their use in optoelectronic devices alone, the III-nitrides are an amazingly important material. In addition to this, the nitrides are also increasingly important in electronic applications. High breakdown fields and good transport properties make the nitrides useful in a range of applications that
are unavailable to Si-based technology [7]. This includes uses in high-temperature and high power applications, such as power switching. A wide array of nitride electronic devices is currently commercially available. Combining the impact of nitrides used in optoelectronic and electronic devices, it is clear that the nitrides will be an important family of semiconductors for years to come.

Given the remarkable advances in nitride research and development, an essential question is whether there is more work to be done in this area. While this is true nitride-based devices are commercially available and perform well, there is still a great deal of university-level research dedicated to making progress with the nitrides, by either improving on current III-nitride based technologies or by expanding what devices are possible to fabricate using the nitrides. The work discussed in this dissertation attempts to make progress in the nitrides in a very specific way - by pushing the boundaries of what is possible in III-nitride devices through the use of nanowires in place of traditional thin films. Nanowires have many advantages, and some disadvantages, compared to thin films, which will be discussed in the following section.

1.2 Benefits of Nanowires Compared to Thin Films

III-nitride nanowires can be formed several ways, such as chemical vapor deposition (CVD) [8] and metalorganic chemical vapor deposition (MOCVD)[9, 10], but nanowires grown by plasma-assisted molecular beam epitaxy (PAMBE) are the sole focus of this dissertation. Since first grown by PAMBE in 1997[11],
catalyst-free III-nitride nanowires have garnered a great deal of attention. This attention is well-deserved since these nanowires have a number of attractive characteristics.

First, catalyst-free III-N nanowires grow on a variety of substrates, including Si(111)[12], Si(001) [13], sapphire[11], and amorphous films[14]. A variety of characterization techniques, most commonly photoluminescence (PL) and transmission electron microscopy (TEM), demonstrate that each NW grows fully relaxed and free of extended defects[15, 16]. The fact that high quality nanowires can be formed on a range of substrates is a huge advantage over thin films. To date, commercially available nitride devices are still grown heteroepitaxially on either sapphire or SiC substrates because nitride substrates are not widely available. This heteroepitaxial growth causes the formation of a high density of extended dislocations in nitride devices, reducing device performance. Though there is currently effort underway to fabricate large area nitride substrates to address just this problem, these materials are still prohibitively expensive. Therefore, catalyst-free nanowires might be one way to achieve III-nitride material with high material quality. Furthermore, catalyst-free III-N nanowires are commonly formed on Si substrates. Si substrates are attractive because they are available in very large sizes (wafers up to 12” in diameter), have extremely high material quality, are cost-effective, and allow for integration with currently existing Si technologies.
A second benefit of catalyst-free III-N nanowires is that they grow along the wurtzite (i.e. the crystal structure of the III-N) c-axis (<0001>). Figure 1.1 shows a scanning electron microscopy image of GaN nanowires grown on Si(111) by PAMBE.

![SEM image of catalyst-free GaN nanowires grown on Si(111) by PAMBE](image)

Figure 1.1: SEM image of catalyst-free GaN nanowires grown on Si(111) by PAMBE

The nanowires form perpendicular to the substrate. The c-axis points along the length of the nanowire, and the sidewalls consist of m-plane surfaces ({$\{10\text{-}10\}$}). This orientation opens up new possibilities that are not available to thin films. For example, it has been proposed that core-shell nanowire solar cells can increase performance by absorbing photons along the length of a nanowire while collecting them along the sidewalls (i.e. laterally) of the nanowire[9]. This advantage over thin films is true for all nanowires. However, one advantage
specific to the nitrides is that the sidewalls are a non-polar surface. Most III-N devices are formed on the wurtzite c-plane, which leads to the distortion of energy bands due to polarization charge. In certain situations it would be beneficial to form a device on a non-polar plane to avoid band bending, and nanowires offer the opportunity to do this. That being said, non-polar and semi-polar III-N substrates are becoming increasingly available over time, though they are still quite expensive. Both non-polar core-shell structures and the effects of polarization in the nitrides will be discussed in greater detail later on in this document.

Nanowire sidewalls provide an extra benefit compared to thin films in the form of enhanced strain accommodation. Because the exposed nanowire sidewalls are free surfaces, the material in the nanowire is allowed to relax in the lateral direction. Thus, if there is any strain in a nanowire, for example due to a heterostructure formed between two lattice mismatched materials, that strain is relieved more effectively compared to a thin film by the presence of the free surface. This enhanced strain accommodation has been predicted theoretically [17, 18] and shown experimentally as well [19]. Furthermore, theoretical work has also predicted that the smaller the nanowire radius, the more strain accommodation can be expected [18]. The plot in Figure 1.2 shows the predicted dependence of strain accommodation on nanowire radius. In this plot, the predicted critical thickness for a lattice mismatched layer of material deposited onto a nanowire is shown as a function of the nanowire’s radius. The contour
lines correspond to different amounts of lattice mismatch. For any given degree of lattice mismatch, the area above the contour corresponds to combinations of nanowire radius and layer thickness that will lead to plastic relaxation of strain and the incorporation of extended defects. Below the contour lines the combination of radius and layer thickness will not lead to the formation of strain-related defects. This means that there are a large number of nitride heterostructures that can be formed using nanowires, which cannot be formed in thin films without sacrificing material quality. This is perhaps the most important advantage to using nanowires in III-N devices.

Figure 1.2: Figure demonstrating the relationship between lattice-mismatch, critical thickness, and nanowire radius [18].

When adding the many advantages of nanowires over thin films to the already amazing characteristics of the III-nitrides, it is clear that III-N nanowires
are potentially useful in a wide range of applications. This dissertation focuses on exploiting the characteristics of both nanowires and III-N to push the boundaries of what has previously been achieved in the nitrides.

1.3 Overview of the Thesis

In Chapter 2, the growth of III-nitride nanowires by PAMBE is described in detail. Because these nanowires form without catalysts, MBE growth conditions must be used to tailor nanowire characteristics such as areal density, radius, and length. Growth maps are created by forming GaN nanowires under different MBE growth conditions. A two-step growth technique is provided that makes use of the growth maps to tailor growth kinetics. By manipulating growth kinetics it is possible to control nanowire density over arbitrarily long deposition times and adjust the ratio of vertical to lateral growth. To prove the effectiveness of the two-step process, vertical and coaxial AlN/GaN nanowire superlattices were formed.

With the basics of nanowire growth established in Chapter 2, coaxially oriented AlN/GaN nanowire resonant tunneling diodes (RTDs) are presented in Chapter 3. The m-plane nanowire sidewalls provide a non-polar surface for the RTD active region. These devices are measured in two ways. Ensembles of nanowires are measured by first creating a thin layer of insulating layer between the nanowires and on top of the Si substrate, then depositing a thick metal layer on top of all of the nanowires. The thick metal layer contacts the nanowire
sidewalls, and a separate contact is made to the substrate. Current-voltage (I-V) measurements of these nanowire ensembles taken at cryogenic temperatures show negative differential resistance. Individual nanowire I-Vs taken using SEM equipment with nano-probes show negative differential resistance at room temperature. The individual nanowire measurements show exceptionally high peak current densities in excess of $10^5$ A/cm$^2$.

In Chapter 4, graded AlGaN nanowires are used to form polarization-induced nanowire light emitting diodes (PINLEDs). Background information on polarization in the III-nitrides is provided. The design and motivation for PINLEDs is then covered. Nanowire structural and chemical characterization shows that the target nanowire heterostructure (graded from GaN to AlN, then back to GaN) is achieved. Device characterization shows that PINLEDs exhibit rectification and emit light when a current is driven through the device. By changing the composition of the QW in the center of the nanowire, electroluminescence (EL) can be tuned over a wide range of frequencies from the deep ultraviolet (UV) into the visible. Variable temperature electrical measurements show that PINLEDs doped with impurities still work to cryogenic temperatures, showing that impurities are not activated by thermal energy, but rather by polarization-induced charge. Furthermore, dopant-free PINLEDs are fabricated that also exhibit rectification and EL. These dopant-free devices show that it is possible to form both p-type and n-type graded AlGaN material through polarization-induced charge alone.
In Chapter 5, the material polarity of PINLED devices is investigated and it was found that catalyst-free nanowires grow with a mixture of material polarities. Scanning transmission electron microscopy (STEM) of individual as-grown nanowires shows that they exhibit an N-face polarity. However, after etching the as-grown sample for long periods in KOH, it is found that roughly 10% of nanowires remain on the substrate after the etch. STEM imaging of these nanowires show that they are Ga-face, proving that the majority of nanowires grow with N-face polarity while a small number grow Ga-face. Conductive atomic force microscopy (C-AFM) is used to electrically characterize nanowire material polarity. Because polarization-induced charge is determined by material polarity, nanowires with opposite polarities are also p-n junctions with opposite polarities, and thus can be electrically measured using C-AFM. Finally, by fabricating devices from nanowires with a mixture of orientations, EL is observed regardless of the polarity of the applied bias. This ambipolar EL is more intense under conditions in which the majority N-face nanowires are biased.

Because PINLEDs were originally designed for Ga-face polarity, their design must be modified to accommodate N-face polarity. Preliminary work to address this issue is provided in Chapter 6. First, to optimize growth on p-Si substrates, PINLEDs with different graded base lengths are compared. As expected, the nanowires with the shortest base length exhibit the best electrical characteristics. Devices are also formed on films of molybdenum as an alternative to p-Si. The PINLEDs grown on p-Si show superior electrical
characteristics to those formed on Mo. Ideas for further optimization of PINLED designs, including grading to lower compositions of Al, using polarization-matched InAlN QWs, and employing patterned nanowire growth instead of catalyst-free nanowire growth, are put forth.

Finally, Chapter 7 summarizes the findings of this dissertation and offers some broad conclusions about the work.
Chapter 2
Nanowire Growth

This chapter is a modified version of a previous publication by the author[20]. I would like to give special thanks to Patrick Phillips for all of the STEM work included in this chapter.

For reasons discussed in the previous chapter, catalyst-free III-nitride nanowires are promising for use in electronic and optoelectronic devices. However, because these nanowires form through a bottom up approach, a central challenge to the formation of III-nitride nanowires by PAMBE, as well as other nanostructures assembled in a bottom up approach, is to control assembly well enough to reproducibly achieve nanostructures with a desired shape, size and density. In this chapter, we provide techniques that can be used to control the bottom-up formation of GaN nanowires and AlN/GaN heterostructures. We provide growth maps that relate GaN nanowire formation to PAMBE growth conditions. By using the different conditions in these growth maps, nanowire density, radius, and height can be controlled. Furthermore, growth conditions can be altered during deposition to actively alter growth kinetics and nanowire formation. We first show that it is possible to nucleate nanowires to a target density at low temperatures, then increase temperature so that the further
nucleation of nanowires stops and the existing nanowires continue to grow, thus controlling nanowire density. This two-step method also allows for GaN nanowires to grow purely in the vertical direction, which is not possible for nanowires formed under normal conditions. If instead nanowires are nucleated and the temperature is reduced, lateral formation is preferred, again tailoring the way in which nanowires form. Finally, this chapter will close with a description of both vertical and coaxial nanowire AlN/GaN heterostructures. However, before the specifics of the nanowire growth studies we have performed are covered, a brief discussion of the basics of PAMBE and GaN nanowire growth are provided.

2.1 Basics of GaN Growth by PAMBE

This section covers some of the basics of GaN growth by PAMBE. This includes a description of the primary components of an MBE system, the growth phase diagrams of homoepitaxial thin film GaN growth, and previously published work on GaN nanowire growth by PAMBE. This section is meant for less experienced readers, who do not necessarily have a background in MBE or nitrides. Therefore, it is suggested that more experienced readers familiar with such topics feel free to skip this section, and instead move directly to the experimental results contained in Section 2.2.

To understand the growth of GaN by PAMBE, one must first understand what parameters can be changed during the PAMBE growth process that might
affect the resulting material. To this end, a very simplified diagram of an MBE chamber is displayed in Figure 2.1.

![Diagram of MBE Chamber](image)

Figure 2.1: A schematic diagram of the most essential parts of a nitride MBE chamber.

There are a huge number of components on an MBE chamber, but the system can be broken down into some very basic elements and functions. First, MBE is a process used to form material with a great deal of control over thickness, composition, and purity. To ensure that materials form with a low concentration of impurities, the volume inside the chamber must be kept at very low pressures. Otherwise the atoms present in the chamber, for example unwanted Oxygen
atoms, incorporate into the material as it grows. Low pressures like this are referred to as ultra-high vacuum, or UHV. UHV conditions are maintained in an MBE chamber using a series of sophisticated pumps that reduce pressure in the chamber to $<10^{-9}$ Torr. Generally speaking, the lower the pressure in an MBE chamber the better, as this reduces the incorporation of impurities into samples grown in the MBE.

The source material used to form samples in the MBE chamber typically consists of a crucible of a very high purity material that is heated until it evaporates into the UHV environment. For example, a standard Ga source might consist of a crucible made of pyrolitic Boron nitride (or PBN), a ceramic that is stable to very high temperatures, filled with pure Ga. The crucible is surrounded with heating coils that are used to heat the material inside it. At low pressures the evaporated atoms are treated as straight beams of atoms and impinge on the substrate. This is how standard Ga, or other metal sources such as In or Al, cells work in an MBE chamber.

Unlike metal sources, the N source depends on the type of system in question. For PAMBE a supply of high purity $N_2$ is passed through a radio frequency plasma source. During this process some of the $N_2$ dissociates into individual N atoms, as well as electrically excited nitrogen atoms and molecules.

All of these forms of N contribute to GaN growth[21]. Through controlling the source of N and Ga impinging on the substrate, the properties of the resulting material can be modulated.
Another critical element of an MBE chamber is the substrate and the CAR that the substrate sits on during growth. A wide variety of different substrates (mostly single crystal wafers) can be loaded into an MBE chamber, including Si, sapphire, or GaN wafers. Inside the growth chamber, the substrate is placed onto what is called a CAR. The CAR serves two major functions. First, motors in the CAR continually rotate the substrate during deposition to ensure even coatings from the impinging fluxes of material. Additionally, the CAR contains heating elements that can control the substrate’s temperature. The temperature of the substrate can either raise or lower the adatom mobility of impinging material, with higher temperatures leading to higher mobilities. Along with the impinging material from the group-III and N source, substrate temperature is one of the key parameters that can be used to control the formation of materials as it is deposited.

A great deal of research has been done to optimize the growth of GaN and other III-nitride materials grown by PAMBE. One common method to optimize growth is to adjust the ratio of impinging Ga to N (or III/V ratio) and substrate temperature and determine the effect on the resulting material. By growing samples under different combinations of III/V and substrate temperature, researchers have established different regions of GaN growth, and summarized them into surface growth phase diagrams [22-24]. One such growth phase diagram is shown in Figure 2.2. Nitride thin film growers use growth maps like this to know what parameters should be used in their own growth. Obviously,
diagrams such as this are extremely helpful to Nitride MBE growers, because they can use it to target certain parameters for their own thin film growths.

![Growth phase diagram for GaN growth on GaN substrates by PAMBE from Koblmuller et al. [23].](image)

Figure 2.2: Growth phase diagram for GaN growth on GaN substrates by PAMBE from Koblmuller et al. [23].

Similar work has been carried out for catalyst-free nanowires grown by PAMBE. The first description of catalyst-free GaN nanowires by PAMBE came in a paper published in 1997 by Yoshizawa et al., who grew on sapphire substrates [11]. Soon afterwards, Sanchez-Garcia et al. reported catalyst-free nanowires grown on Si(111) substrates[12]. Since these early works, a great deal of research has been dedicated to better understanding the growth of GaN nanowires by PAMBE. Through this work, it became generally accepted that nanowires form under N-rich (i.e. III/V<1) conditions, with substrate temperatures
higher than what is generally used for GaN thin film growth (>750°C). The first growth phase diagram for GaN nanowires formed by PAMBE on bare Si(111) substrate was published by Fernandez-Garrido et al. in 2009 (shown in Figure 2.3).

They found that at too low of a temperature nanowires will not form, possibly because Ga adatom mobility is too low in this region for nanowires to nucleate. At too high of a temperature there is no growth at all since the desorption of Ga adatoms and thermal decomposition of GaN will occur faster than the formation of GaN. III/V ratio usually needs to be below 1 (i.e. N-rich conditions), but at high enough temperatures it is possible to still achieve nanowire growth with a III/V greater than 1.0. This is possible because enough Ga desorbs from the
surface so that the actual III/V conditions on the sample will be below stoichiometry even if the nominal III/V maybe be above stoichiometry. In addition to the growth map in Figure 2.3, there have been numerous other studies that look for monotonic relationships between nanowire properties and growth conditions [11, 26-28].

In the following section, nanowire growth phase diagrams formed by the author will also be presented. These growth maps differ from the studies mentioned above because they are designed to map nanowire characteristics to a wide range of growth conditions. Like the growth phase diagram shown in Figure 2.2, these growth maps seek to provide an MBE grower the ability to form nanowires with specific characteristics under certain prescribed growth conditions. This is not possible to do using monotonic growth conditions, or the growth map in Figure 2.3, which does not include any information about the resulting nanowire characteristics. It should be noted that the growth diagrams in the following section and the one in Figure 2.3 do not match one another exactly, possibly due to differences in the growth time for each sample used in the diagram or different amounts of active nitrogen used during growth.

2.2 Growth Phase Diagrams of GaN NWs on Si(111)

In this section, nanowire growth phase diagrams are presented that relate nanowire characteristics to growth conditions. These maps are important not only because they allow for a comparison between nanowires grown at different
conditions, but they also provide information about how the nucleation of nanowires changes under different growth conditions.

At the beginning of GaN nanowire growth, small islands of GaN nucleate and grow until they reach a critical size and shape[29], at which point they start to grow vertically. They then continue to grow vertically because Ga adatoms prefer to incorporate onto the c-plane nanowire tops instead of m-plane sidewalls[30, 31]. As stated in the opening chapter, nanowires can form in this way on a variety of substrates, including sapphire[11] or amorphous substrates[14]. For each substrate material, nanowires formed under the same MBE conditions will lead to nanowires with different characteristics. Because the vast majority of the samples described in this dissertation are formed on Si(111) substrates, how nanowires form on Si must be very well understood. To achieve this understanding, it is necessary to create a growth phase diagram that relates the characteristics of nanowires (e.g. height, radius, areal density) to MBE growth conditions. As stated in the previous section, there is a need to form growth maps that not only show under what conditions nanowires form, but also what the characteristics are of nanowires grown under the different conditions.

To achieve this, growth maps are formed by plotting the change in a specific nanowire parameter as a function of III/V ratio and substrate temperature. To ensure that the information in the growth maps is as accurate as possible, III/V and substrate temperature must be carefully controlled. Furthermore, if growth conditions are calibrated properly, the resulting growth maps should serve as
system independent references for other researchers that would like to grow GaN nanowires on Si(111). Therefore, a detailed list of the MBE system used to grow the samples, and the methods used to calibrate growth conditions is provided in Appendix A. It should be noted here that III/V ratio was adjusted by changing the flux of Ga and leaving the supply of active nitrogen the same from growth to growth. An alternative method could be to adjust the amount of active nitrogen while leaving the impinging Ga flux constant. This would have changed the III/V ratio while leaving the growth rate (determined by Ga flux because of N-rich conditions) constant, though growth rate will change with substrate temperature due to Ga desorption and GaN decomposition. The former approach (i.e. Ga flux changes, N is constant) is used for consistency with previously formed GaN growth phase diagrams for thin film growth[22-24]. In the initial phases of forming the growth maps, a number of samples were grown for 30 minutes with a constant III/V (III/V = 0.26) and a range of different substrate temperatures (720 to 790°C). Scanning electron microscopy (SEM) images taken of these samples in cross-section and plan view are provided in Figure 2.4. All images are obtained on an FEI Sirion scanning electron microscope operating at an accelerating voltage of 15 kV using the “in lens” secondary electron detector. The image analysis software ImageJ[32] is used to determine nanowire density, height, and radius. The areal density of nanowires is determined using image analysis of plan view SEM images. The average nanowire density is found from plan view images by first approximating the
nanowire tops as circles, measuring their area, and the calculating the radius of those circles. Cross-sectional SEM images are used to measure the average nanowire height.

Figure 2.4: SEM images of GaN nanowires in plan view (top) and cross section (bottom) grown at a constant III/V and increasing substrate temperature.

This small set of samples shows some interesting and important features. As temperature is increased, nanowire areal density drops by more than two orders of magnitude. Below GaN decomposition temperatures (750°C)[33, 34], nanowire density is consistently near 1000 µm⁻², but when substrate temperature increases and GaN starts to decompose, density sharply decreases (Figure 2.5A). This decrease also occurs in average height and radius(Figure 2.5B) although the changes in radius and height are not quite as large. This change in nanowire morphology is expected for multiple reasons. First, as temperature is
increased, the rates at which GaN decomposes and Ga adatoms desorb from the substrate also increase. This leads to a reduction in the overall growth rate of the material, which manifests itself as a reduction in nanowire height, radius, and density.

![Graph showing density, height, and radius as a function of substrate temperature with a constant III/V ratio.]

**Figure 2.5:** A) Density, B) height, and radius as a function of substrate temperature with a constant III/V ratio.

Second, completely independent from the rate of GaN growth in these conditions, the nucleation of GaN islands is also affected by the increased substrate temperatures. At higher temperatures, the necessary size for a GaN islands to be stable will increase. Thus the time it takes for nanowires to reach this critical size will also increase. Since all the samples are grown for only 30 minutes, there should be a large range in nanowire areal density based solely on the time for an average nanowire to nucleate under a certain set of conditions. If the nanowires nucleate in much less time than 30 minutes, then the nanowire
density should reach a saturation point before the deposition is completed. If however, the nanowire nucleation time is on the scale of 30 minutes or in excess of 30 minutes, the areal density at the end of deposition will be far below the expected saturation point.

To build up system independent growth maps, 22 samples were grown at various combinations of III/V and substrate temperature. Growth maps relating several nanowire characteristics to growth conditions are shown in Figure 2.6. The map relating density to growth conditions (Figure 2.6A) shows that both substrate temperature and III/V ratio impact the resulting nanowire density. At low temperatures (720 to 740 °C) and high fluxes (III/V = 0.3 to 0.6) high density nanowires are generally obtained. These high density samples approach a saturation density of approximately 1000 \( \mu \text{m}^{-2} \). As stated earlier, as GaN decomposition starts at higher substrate temperatures, density tends to drop, which can be seen in the bottom right hand corner of Figure 2.6A.

Growth maps relating average height and radius are displayed in Figure 2.6B and C. A map of equivalent two-dimensional growth rate, calculated by taking the product of average nanowire volume and areal density, is shown in Figure 2.6D. All of these maps show the same basic regions of the growth map in Figure 2.6A, namely large values in the top left hand corner (i.e. low temperature, high flux) and small values in the bottom right hand corner (i.e. high temperatures, low fluxes). This is not surprising, since at low III/V ratios and high temperatures the nucleation of nanowires must compete with the desorption of
Ga adatoms from the substrate as well as the decomposition of GaN. It should be stressed that all of the samples used in these maps were grown for 30 minutes.

Figure 2.6: A) Density, B) average radius, C) average height, and D) equivalent 2D growth rate as a function of substrate temperature and III/V.
This 30 minutes growth time is positive in one sense, because it provides a snapshot of nucleation and growth after a relatively short amount of time. However, the information is somewhat limited because under some conditions, nanowire nucleation may take longer than 30 minutes. Thus, these conditions will appear to have no material grown after 30 minutes by SEM, but a very small amount of material may nevertheless still be present (i.e. there is still some small formation of GaN material). So to investigate the characteristics of nanowires grown at temperatures much hotter than 780°C, samples grown for longer than 30 minutes need to be used. Unfortunately this cannot be avoided, as any one map cannot fully describe the characteristics of nanowires grown under all conditions.

Using the information contained in the growth maps, it is possible to control nanowire characteristics by actively changing growth conditions during deposition. For example, to obtain a high density of thick nanowires, growth conditions in the top left hand corner of the growth phase diagram (i.e. low temperature and high fluxes) should be used. Unfortunately, because nanowire nucleation and growth occur simultaneously, the density and length are not independently tunable. For example, if one would like to grow a low density of nanowires, the growth maps suggest using a high temperature and low III/V. But the density provided in the growth map will only be achieved if the nanowires are grown for 30 minutes. If grown for longer, new nanowires will continue to nucleate while the previously nucleated nanowires continue to grow. That is,
under these conditions, nanowire density is low because nucleation is not complete after 30 minutes, but by growing further at these conditions nucleation continues and density increases. Thus nanowire density and length are not usually separately tunable characteristics. Therefore, it is desirable if there is a method that could be used to separate the nucleation and growth stages of the nanowires, so that nucleation occurs until a desired density is reached, nucleation is then stopped and growth alone continues. The following section provides just such a method.

2.3 Two-step growth procedure

This problem of overlapping nucleation and growth steps can be avoided by adjusting growth conditions to favor or suppress the nucleation of GaN nanowires. During the deposition of all the samples used in the growth maps provided above, growth conditions are held constant throughout. We will call these “one-step” samples. To separate nucleation and growth, a two-step method is employed. For these “two-step” samples, deposition is initiated under conditions in which nanowires readily form, and when a desired density is reached, substrate temperature is rapidly increased, thus suppressing the nucleation of any further nanowires. While the substrate temperature is changed, the N shutter is left open so that the decomposition of what material has already formed is limited. The exact temperatures and III/V ratios to use during the nucleation and growth steps are decided upon by using the growth
maps in the previous section. In the “two-step” samples presented in this section, III/V ratio is held constant and only substrate temperature is changed.

A series of samples grown over different lengths of time show the effectiveness of the two-step method. First, a series of one-step samples are grown under the same conditions (substrate temperature = 765 °C) over increasing lengths of time (22.5 to 90 minutes). SEM images of both the one-step and two-step samples grown for a total of 90 minutes are provided in plan view and in cross-section (Figure 2.7). The areal density for these samples is shown in Figure 2.8. Until the 30 minute mark is reached, nanowire density is low and consistent with the data in the growth phase diagrams.

Figure 2.7: SEM images of one-step (A,B) and two-step (C,D) nanowires shown in plan view (A, C) and cross-section (B, D). All nanowires are grown for a total of 90 minutes.
The data clearly shows that between 30 and 45 minutes the nanowire density sharply increases, and reaches a saturation value just over 400 µm\(^2\) for longer growth times. As a comparison, two-step samples are grown using the same conditions during the nucleation step, but a higher temperature (780 °C) during the growth step. For all two-step samples in this series, a nucleation time of 22.5 minutes is used, which should provide a nanowire density of approximately 10-20 µm\(^2\). The plot of areal density in two-step samples over time (Figure 2.8) clearly shows that the sharp increase in nanowire density seen in the one-step samples does not occur. Furthermore, the equivalent 2D growth rate for these samples shows a large difference in the amount of material formed using a one-step or a two-step procedure.

Figure 2.8: A) Density and B) Equivalent 2D growth as deposition time increases in one-step and two-step samples.
The difference between one-step and two-step samples shown in Figure 2.7 and Figure 2.8 can be understood by investigating the growth phase diagrams in the previous section. At 780 °C (the temperature used during the growth step of the two-step samples) additional nanowire nucleation is suppressed due to thermal decomposition of GaN and Ga adatom desorption. This allows the existing nanowires to grow vertically, as shown in Figure 2.9, while no new nanowires nucleate. As one might expect, because the two-step samples are grown at temperatures well above the decomposition temperature of GaN, vertical growth is slightly smaller in the two-step samples compared to the one-step (see Figure 2.9). This is further shown by examining how the equivalent amount of 2D growth changes over time (Figure 2.8B). Again, because two-step samples are grown much hotter, the equivalent 2D growth is lower. Note that at this point, separate control of density and length has been achieved by only changing substrate temperature. It stands to reason that by also modifying III/V ratio during deposition one might gain additional control. This might be the case, but one must be cautious in doing so, as an increase in Ga flux could change the balance of formation and decomposition/desorption, thus allowing more nanowires to nucleate. Using the two-step technique also has a large impact on the formation of GaN nanowires in the lateral direction (see Figure 2.9). A vertical to lateral growth rate of 30:1 is usually reported for catalyst-free GaN nanowires [26, 35, 36]. Lateral formation of GaN is suppressed by the two-step
method (see Figure 2.9B), leading to nanowires with an ever increasing nanowire aspect ratio for two step samples.

![Graphs showing radius, height, and height/radius ratio over time for one-step and two-step samples.]

Figure 2.9: A) Radius and B) the ratio of height to radius as a function of deposition time for one-step and two-step samples.

The one-step samples show aspect ratios similar to what has been previously reported (see Figure 2.9C). This could provide an opportunity to create GaN nanowires with sizes and shapes not previously achieved.

The suppression of radial growth in the two-step grown samples has a number of possible explanations. First, the higher substrate temperature may affect the incorporation of adatoms on either the m-plane nanowire sidewalls or the c-plane nanowire tops. Second, at higher temperatures GaN might decompose slightly more from m-plane rather than c-plane surfaces. This could
slightly affect the balance of formation and decomposition on the sidewalls, thus suppressing lateral growth. A third possibility is that an increase in Ga adatom mobility at higher temperatures makes it easier for adatoms to reach the more favorable c-plane nanowire tops. Of these, the third possibility seems the most likely, though determination of the exact mechanism would require additional investigation. That being said, the current results clearly show the elimination of lateral GaN growth due to a change in growth kinetics using the two-step growth method, regardless of the exact mechanism by which this occurs.

Through using the two-step method, we can therefore control a number of aspects of catalyst-free nanowire formation. It allows for the grower to separate the nucleation and growth of nanowires, and therefore independently control nanowire density (set during the nucleation step) and height (controlled through the amount of deposition that occurs during the growth step). The two-step method also results in a change in growth kinetics such that nanowires cease growing both vertically and laterally, and only grow vertically. For all of these reasons, the two-step method is extremely useful in the formation of nanowire heterostructures, which will be dealt with in greater detail in Section 2.4 below.

2.4 Increased lateral growth of GaN nanowires

At this point, one might naturally ask if it is also possible to control growth kinetics such that lateral nanowire growth is preferred over vertical growth. Coaxially (also called lateral or core-shell) heterostructures are interesting for a
number of reasons. The sidewalls of III-nitride nanowires consist of m-plane surfaces, which is a non-polar surface in the wurtzite structure. This means that coaxial heterostructures can also be used to form devices that avoid polarization-induced band bending by growing on the non-polar surfaces. The advantages of non-polar growth were described in Section 1.2. With these advantages in mind, controlling lateral growth in III-nitride nanowires grown by PAMBE is desirable.

Unfortunately, controlling lateral growth is not a trivial task. As previous cited, the ratio of vertical to lateral growth in GaN nanowires is usually measured at 30:1[26, 35, 36]. This large difference between vertical and lateral growth makes sense when one considers that the nanowires form in a vertically aligned fashion without the use of catalysts. This must mean that there is a strong driving force for vertical rather than lateral formation of GaN. Luckily, the two-step growth of GaN nanowires we previous discussed have already provided a way to increase the lateral growth of the nanowires. In the two-step growth, it was said that higher temperatures increase mobility, and thus increases the vertical growth rate of nanowires. It stands to reasons that it should be possible to suppress vertical growth by lowering substrate temperature, thus reducing Ga adatom mobility and forcing incorporation on nanowire sidewalls.

To prove this concept works, a series of samples are grown in which nanowires are nucleated at a low density and grown vertically using the two-step method, followed by 30 minutes of deposition at lower temperatures on top of the previously formed nanowires cores. All samples are identical to one another,
except in the temperature used during the low temperature deposition, which ranged from 500 to 700 °C.

![SEM images](image_url)

Figure 2.10: SEM images in cross-section showing coaxial layers deposited using different substrate temperatures.

SEM images taken from these samples are shown in Figure 2.10. These images reveal a number of characteristics of these samples. First, in all three samples, there is some growth on the Si between the tall, initially nucleated nanowires, but only in the sample in which deposition occurred at 700 °C does
this material take the form of nanowires instead of a rough film. This shows that nanowires grow as low as 700 °C, even if samples were not grown at such a low temperature in the growth phase diagrams. Also, the SEM images show that for the samples with deposition occurring at 500 and 600 °C, there is a distinct “bulb” at the nanowire tops. It is unclear what causes this formation, and counter intuitive that the bulbs would be larger at 600 °C compared to 500 °C. The average length and diameter (measured near the center of the nanowires) is found from these images and shown in Figure 2.11. A plot of the ratio of nanowire length to diameter as a function of the temperature used during the coaxial deposition step is also shown in Figure 2.11, and it demonstrates that at lower temperatures lateral incorporation of adatom is favored.

Figure 2.11: A) Length, B) diameter, and C) the ratio of length to diameter as a function of substrate temperature used during the coaxial growth step.
Once it was clearly shown that substrate temperature can affect lateral growth, a series of samples was grown to address how coaxial growth changes with III/V. In these samples, low density nanowires are again grown using the two-step method and substrate temperature is reduced to boost lateral growth.

Figure 2.12: SEM images in cross-section showing coaxial layers deposited using different fluxes of Ga.

Once at these lower temperatures, the III/V ratio is changed (by increasing or decreasing the Ga flux). SEM images from these samples are shown in Figure 2.12 and plots of the resulting nanowire characteristics are displayed in Figure 2.13. At lower III/V the ratio of vertical to lateral growth drops when III/V is
reduced. Put another way, there is an increase in lateral growth compared to vertical growth at lower fluxes. However, it should be noted that based on the plots in Figure 2.11 and Figure 2.13, lateral growth rate depends more on substrate temperature than on III/V. The data contained in these two figures provides a good start, but much more work needs to be done to fully understand how growth conditions affect the lateral formation of GaN.

Figure 2.13: A) Length, B) diameter, and C) the ratio of length to diameter as a function of Ga flux used during the coaxial growth step.

2.5 Vertical and Coaxial GaN/AlN Nanowire Superlattices

Using the control of nanowire growth achieved in the previous sections of this chapter, this section will present both vertically and coaxially oriented AlN/GaN heterostructures that utilize this control. To form vertical heterostructures, low-density, long GaN nanowires are first grown using the previously described two-step method. After this, 50 periods of AlN and GaN are
deposited on top of the nanowires by pulsing the Ga and Al shutters and leaving the N source open continuously. This pulsing leads to the formation of short period vertical superlattices (SLs) along the c-axis of the nanowires. In previous attempts at growing nanowire SLs the coalescence of nanowires at higher density was detrimental to achieving reproducible SLs. Therefore, it is important that the initial plain GaN nanowires have a low density (in this case 16 µm⁻²). SEM images of the as-grown vertical heterostructures reveal that there is no coalescing between nanowires (see Figure 2.14).

![SEM image of as-grown vertical GaN/AlN nanowire superlattices.](image)

Figure 2.14: SEM image of as-grown vertical GaN/AlN nanowire superlattices.

High-resolution microscopy performed on an FEI Titan3 80-300 probe-corrected monochromated scanning/transmission electron microscope (S/TEM) operated at 300 kV is displayed in Figure 2.15. The microscope was operated in high-angle annular dark field (HAADF) mode, providing Z-contrast. As expected
from the previously discussed results regarding the two-step method, radial deposition of GaN is not observed. However, the low mobility of Al adatoms, even at substrate temperatures near 800°C, forces AlN to form both vertically and coaxially.

![STEM HAADF image of a single nanowire GaN/AlN vertical superlattice.](image)

Figure 2.15: STEM HAADF image of a single nanowire GaN/AlN vertical superlattice.

The ratio of vertical to coaxial growth for AlN is estimated at 11:1, similar to reports from one-step grown GaN/AlN nanowires[35]. Somewhat surprisingly, the layer thicknesses obtained from the HAADF images like the one in Figure 2.15 show that the average GaN vertical growth rate is $2.8 \pm 0.3$ nm/min, which is larger than the value obtained in Figure 2.8 ($2.4 \pm 0.1$ nm/min). It is unclear what is responsible for this difference in growth rates. One possible explanation is that Ga adatoms have a higher mobility on m-plane AlN sidewalls compared to GaN sidewalls.

The formation of these vertical SLs can provide some information about nanowire growth kinetics. By closely inspecting the HAADF image shown in
Figure 2.15, it is clear that the AlN SL layer thicknesses decrease as the nanowire structure grows taller.

![Graph showing vertical growth rate vs. nanowire diameter for GaN and AlN](image)

Figure 2.16: GaN and AlN vertical growth rates as a function of nanowire diameter.

Image analysis used to measure the thickness of each period of the superlattice in the vertical direction from multiple individual nanowires shows the growth rate of GaN and AlN layer as a function of the diameter (determined by the width of the GaN disk itself)(Figure 2.16). As diameter gets larger the AlN growth rate drops while the GaN growth rate does not. This is consistent with reports in the literature that show the length of nanowires to be inversely proportional to nanowire diameter plus a constant[35]. The relationship between nanowire length and diameter is described by

\[ l = C_1(1 + C_2/d) \]  

(Eq. 2.1)
where \( l \) is nanowire length, \( d \) is diameter, \( C_1 \) and \( C_2 \) are both constants. Interestingly, the \( C_2 \) constant corresponds to twice the value of the adatom diffusion length. The fact that the AlN growth rate drops as diameter is increased is consistent with the fact that Al adatoms have a lower mobility than Ga adatoms. The GaN growth rate does not change with diameter because of the larger Ga adatom mobility at high substrate temperatures. This result has a number of implications. First, it shows that vertical SLs grown under different growth conditions can be used to gain quantitative information about growth kinetics. However, any experiment that seeks to do this must ensure that the nanowires are grown with a low enough areal density to ensure that minimal interaction between adjacent nanowires in the form of shadowing the impinging beam flux and competition for adatoms. This reinforces the importance of using our two-step growth procedure to control nanowire density. Secondly, when growing AlN/GaN heterostructures, if layers with repeatable thicknesses are desired, one must take into consideration the change in vertical growth rate in each subsequent layer as diameter increases.

As a final note concerning vertical SLs, while AlN/GaN heterostructures have been previously formed by MBE[36], the nanowires here differ in that the GaN layers do not form coaxial, only vertically. This means the GaN layers are completely surrounded by AlN. This encapsulation in a material with a much larger band gap might be useful for the development of vertical nanowire photonic and electronic devices.
In much the same way that we controlled nanowire growth kinetics to create vertical SLs, the same can be done to create coaxial SLs. The growth of coaxial SLs starts in much the same way as the vertical SLs. Again, deposition starts with the nucleation of a low density, long GaN nanowires. In the case of the vertical nanowires, the initial GaN growth acted as a pedestal for the subsequent formation of the SL. In this case, the initial GaN acts as the core for the coaxially oriented SL deposited on top. With the cores formed, substrate temperature is lowered to 500 °C and a five period superlattice of AlN and GaN is deposited. As discussed in the previous section, the lower substrate temperature increases the rate of lateral GaN growth. This is again shown using an STEM imaging in HAADF mode (see Figure 2.17).

Figure 2.17: STEM HAADF image of GaN/AlN coaxial superlattice.

Both the GaN and AlN coaxially oriented layers have a thickness of 1-2nm. Atomic resolution HAADF images such as the one in Figure 2.18 display
atomically sharp GaN/AlN interface to within ± 1 monolayer. Though III-nitride core-shell structures such as the one shown here have been previously formed using catalyst assisted nanowire growth (e.g. chemical vapour deposition[8] or metalorganic chemical vapour deposition[9, 10]), we believe that our MBE grown coaxial AlN/GaN SLs are the first to be formed using a catalyst-free method.

Figure 2.18: Atomic resolution STEM image in HAADF mode of coaxially oriented AlN/GaN layers.

Like with the vertical SL sample, the two-step growth technique is essential to forming the GaN nanowire cores at the initiation of deposition. If the density of the nanowire cores is too high then adjacent nanowires will shadow the impinging flux of atoms from one another, and lead to unevenly deposited material. The lower temperatures and decreased adatom mobility should make shadowing even more detrimental than it would already be for comparable
structures grown at high temperatures. This is because adatoms with low mobility will incorporate closer to where they land on the surface and therefore cannot move about to find other potentially more preferential sites. Thus establishing a low NW density with the two-step method is necessary for achieving uniform coaxial layers.

As with the vertical SLs, we can investigate the dependence of layer thickness on the overall diameter of the nanowire when that layer was deposited. That is, you can investigate whether the diameter of the nanowire core determines the thickness of the coaxial shell deposited onto it. A plot of the thickness of coaxial GaN and AlN layers as a function of nanowire density is provided in Figure 2.19.
The data clearly shows that layer thickness, and therefore growth rate, of the coaxial layers drops as the nanowire gets wider. Unfortunately, while the same behavior in vertical SLs could be explained using previously published theories, to our knowledge there is no equivalent theory to explain how coaxial growth should depend on nanowire diameter. This is most likely due to the fact that coaxial SL structures in catalyst-free nanowires like these have not been previously reported in the literature. As stated at the close of the previous section, a great deal remains to be understood concerning the coaxial growth of catalyst-free nanowires by PAMBE.

To close this chapter, a brief review of the material covered so far is in order. Growth phase diagrams for catalyst-free GaN nanowires were developed allowing control over nanowire characteristics by initiating growth under different sets of conditions. The effects of nucleation and growth were separated using a two-step dynamic method allowing independent control of nanowire density and height. Furthermore, growth using the two-step technique leads to a suppression of radial GaN formation. With this lack of radial growth, scientists can more accurately form target structures in which only vertically oriented heterostructure layers are desired. Additionally, coaxial growth was enhanced by exploiting reduced adatom mobility at low temperatures. Vertical and coaxial AlN/GaN SLs were both formed. By carefully manipulating growth conditions, a range of growth kinetics can be achieved, allowing the formation of three-dimensional nanowire heterostructures with monolayer precision. These heterostructures
may enable a variety of nanoelectronics and nanophotonics. The following chapter provides a proof of concept device that takes advantage of a coaxially oriented heterostructure to achieve flat band conditions.
Chapter 3

Coaxial AlN/GaN Nanowire Resonant Tunneling Diodes

This chapter is a modified version of a previous publication by the author [37]. I would like to thank to Patrick Phillips (STEM imaging), Thomas Kent (low temperature ensemble measurements), A.T.M.G Sarwar (device modeling), and Camelia Selcu (individual nanowire electrical measurements) for their contributions to this chapter.

The previous chapter focused on controlling the formation of III-nitride nanowires and nanowire-based heterostructures. This chapter covers proof-of-concept work we have done to show that coaxially-oriented AlN/GaN heterostructures formed using the methods established in the previous chapter can be used to create single nanowire electronic devices. The specific device dealt with in this chapter is the resonant tunneling diode (RTD). Background on RTDs, and why how these devices might benefit from a core-shell heterostructure geometry is covered in the following section.
3.1 Motivation for non-polar, AlN/GaN Resonant Tunneling Diodes

RTDs are electronic devices whose key characteristic is negative differential resistance (NDR) caused by an increase and decrease of tunneling current. An RTD usually consists of a double barrier structure of wide band gap material with a quantum well (QW) between the barriers and n-type material outside of the barriers on either side. A schematic of the target nanowire RTD design is shown in Figure 3.1. At low applied voltages conduction band electrons do not have the correct energy to resonantly tunnel through the double barrier structure. As the voltage is increased, electrons will at some point have the correct energy to resonantly tunnel through the double barrier structure, and the device will pass some current. If the increase in voltage continues, electrons will no longer have the proper energy to resonantly tunnel through the barriers and the current reduces with increasing voltage. Therefore, the current initially increases with increase voltage, but after a certain point decreases. This decrease in current as voltage increases is commonly referred to as NDR because $\frac{dI}{dV}$ is less than zero in this section of the device’s I-V.

Because of their high-speed capabilities and non-linear I-V characteristics (i.e. NDR), RTDs have many potential applications, including THz devices[38-40] and multi-valued logic circuits[41]. Recent work has shown that it is possible to fabricate RTDs that operate at fundamental frequencies above 1 THz at room temperature[42, 43]. To date the majority of research has focused on III-V RTDs such as GaAs/AlGaAs[44, 45] and InAs/AlSb[46]. III-nitride-based RTDs are
also attractive because of the large conduction band offset (2.1 eV)[47] between AlN and GaN, high electron mobilities, and good thermal stability, all of which could enhance RTD performance.

NDR in double-barrier AlGaN/GaN RTDs have previously been reported[48-51]. The NDR in these structures disappears after repeated scans and is not present scanning backwards (i.e. from V > 0 to V = 0). One possible explanation of this behavior is that the current in these devices is not due solely to tunneling, but rather a combination of tunneling through and charging of trap states[49, 50]. Nitride RTDs using a non-polar orientation and AlGaN barriers with a low composition of Al have also been grown[52]. These non-polar devices show more reproducible NDR than polar devices. The reports of NDR in III-nitride devices are still somewhat controversial. Sakr et al. have proposed that the non-reproducible NDR seen in previously formed AlGaN/GaN RTDs is not due to resonant tunneling at all, and instead can be explained using the charging and discharging of trap states[53]. Their argument is based, in part, on the fact that these previous examples of NDR have been stronger at room temperature than at low temperatures. This is the opposite from what would normally be expected for a device that utilized tunneling, which leads them to argue that the observed NDR in the III-nitrides is not due to tunneling.

Our work focuses on GaN/AlN RTDs formed in a similar fashion to the coaxially oriented AlN/GaN superlattices described in the previous chapter. The target AlN/GaN double barrier structure is shown in Figure 3.1. The band
diagram for this structure (Figure 3.1) is modeled using a one-dimensional, self-consistent Schrödinger-Poisson solver[54]. In this band diagram it is assumed that the Fermi level is pinned 0.55eV below the conduction band at the sidewall surface, which previous experimental work has shown is caused by the presence of oxygen on the m-plane sidewalls of GaN nanowires [55]. This pinning causes some portion of the outermost section of the nanowires to be depleted, depending on the concentration of dopants in the nanowires, as shown in Figure 3.1.

![Figure 3.1: Schematic of AlN/GaN coaxially oriented nanowire resonant tunneling diode, including the band diagram in the lateral direction.](image)

Given its coaxial orientation, the heterostructure is formed on the nonpolar (m-plane) nanowire sidewalls, leading to flat band conditions (i.e. no band bending due to polarization charge). This non-polar design provides several
advantages over the more common, polar (c-plane oriented) AlGaN/GaN RTDs that have been reported. A one-dimensional non-equilibrium Green’s function based model is developed, using the commercial software ATLAS, to simulate RTDs with polar surfaces, non-polar surfaces, and different barrier heights (AlGaN %Al). The results of this modeling are found in Figure 3.2. In Figure 3.2A the transmittance as a function of electron energy shows that electrons will tunnel through the double barrier structure at lower energies in an RTD with a non-polar orientation compared to a polar orientation.

![Simulation results](image)

**Figure 3.2:** A) Simulated transmittance as a function of electron energy for the proposed AlN/GaN nanowire RTD. B) Peak-to-valley current ratio as a function of %Al in the AlGaN barrier.

In Figure 3.2B, simulations show that as the amount of Al used in the AlGaN double barriers increases, the expected peak-to-valley current ratio (PVCR) also increases. PVCR is a common device parameter used to determine the quality of an RTD.
Unfortunately, the small critical thickness of AlN on GaN makes it difficult, though not impossible, to form a planar AlN/GaN double barrier RTD without incorporating a large number of strain related defect. Strain accommodation in nanowires is therefore useful in this application, in that they allow for high quality nitride RTDs with AlN barriers. Of course, the other benefits of using III-nitride nanowires grown by PAMBE (e.g. integration with Si, high material quality) still hold true for this specific device. With these benefits in mind, Songmuang et al. used III-nitride nanowires grown by PAMBE to form vertically aligned AlN/GaN nanowire RTDs[56]. In this work, researchers were able to achieve reproducible NDR using a similar double-barrier heterostructure to our target structure, with the biggest difference being the vertical, and hence polar, orientation. In addition to the previously mentioned benefits of non-polar orientations, the coaxial structure we have proposed should have the added benefit of leading to larger current densities (normalized by the nanowire’s cross-sectional area). Because the device active region is a cylindrical shell in the coaxial case, current density should scale with nanowire height (i.e. the taller the nanowire, the larger the area of the active region). In a vertical orientation the active region’s size is simply the cross-sectional area of the device and therefore does not scale with height. Thus coaxial RTDs should exhibit higher current densities than both planar RTDs or vertically aligned nanowire RTDs.
3.2 Growth and Structural Characterization

The previously described two-step growth method was used to grow Si doped (nominally $1 \times 10^{19}$ cm$^{-3}$) n-GaN NWs at low densities (1-10 µm$^{-2}$) on n-Si(111) substrates (see Section 2.3 for more details). Like with the coaxially-oriented SLs in Section 2.5, the GaN nanowires deposited in the initial stages of growth serve as n-GaN cores for the subsequent deposition of the lateral heterostructure. Once the cores are established, substrate temperature is reduced to 500°C to promote coaxial formation of GaN. At this low temperature a double barrier structure consisting of 1.5nm of i-AlN/2.5nm i-GaN/1.5 nm i-AlN/15 nm n-GaN ($1 \times 10^{19}$ cm$^{-3}$ Si) is deposited.

![Figure 3.3: A) Cross-section and B) plan view SEM images of the as-grown RTD structures.](image)

We investigated the structural characteristics of the nanowires using electron microscopy. SEM images of the sample in cross-section and plan view
are provided in Figure 3.3. As seen in Section 2.4, the thick material between nanowires and the large bulb of material on top of the nanowires forms due to lower adatom mobility achieved at a decreased substrate temperature.

Individual nanowire heterostructures are analyzed using high resolution STEM, using the same equipment described in Section 2.5. HAADF images are provided in Figure 3.4 and Figure 3.5. The images in Figure 3.4A and Figure 3.4B are of individual nanowires with the same device active region, but different outermost shell thicknesses (thinner in A).

![Figure 3.4: STEM HAADF images of two nanowire RTDs with outer shells of different thicknesses (A is thinner).](image)

The thinner shell reduces the size of the bulb on top of the nanowire, which seems on the face of it advantageous, even though no study has been performed to determine what effects this faceted material has on device operation. This might lead one to think that a thinner shell is preferred. However, because of the
pinning of the Fermi level on the nanowire sidewalls, a thicker shell might be needed to insure that the outermost shell is not fully depleted. Atomic resolution images (Figure 3.5) of a single nanowire’s active region shows close agreement with the target design, though the outermost shell is somewhat thinner than intended. This could be due to the change in coaxial growth rate as a function of diameter shown in Figure 2.19.

![Atomic resolution STEM image of the nanowire RTD’s coaxial heterostructure.](image)

Figure 3.5: Atomic resolution STEM image of the nanowire RTD’s coaxial heterostructure.

Many images like those in Figure 3.4 and Figure 3.5 show the nanowires to be free of dislocations or stacking faults. Additionally, it is clear that the bulb of material on the nanowire tops contains alternating layers of AlN and GaN. Even at low substrate temperatures, vertical growth is still preferred to lateral growth, meaning that the layers of AlN and GaN are thicker (roughly 10x thicker) on the nanowire top than on its sidewalls. This is beneficial, as the presence of a ~12
nm thick section of AlN at the nanowire top should prevent current from passing through the top directly into the nanowire core.

3.3 Electrical Characterization

The nanowires RTDs are characterized electrically in two ways: as an ensemble or individually. The ensemble case is considered first.

A schematic of the processed ensemble device’s design is provided in Figure 3.6A. To process an ensemble of low density nanowires into a single device, careful attention must be given to preventing conduction through the material between the nanowires. To do this, a thin layer of HSQ (Hydrogen silsesquioxane) is spun onto the surface, and then cured at 350°C for 30 minutes. The cured HSQ forms an insulating layer that prevents shorting of the contacts directly to the Si substrate. With this insulating layer, we can then deposit a thick metal contact (20 nm Ti/50 nm Au) directly onto the nanowires. This metal layer covers everything, but conduction should only occur through the nanowire sidewalls because of the HSQ and the thick layers of AlN in the nanowire tops that were previously described. A small area of nanowires is scratched from the surface of the sample, leaving bare n-Si behind. A small piece of In is annealed onto the bare Si and acts as the secondary contact. I-V measurements are taken by applying a bias to the contact on top of the nanowires and grounding the Si substrate through the In contact.
Electrical measurements of ensembles of nanowires were performed at both room temperature (Figure 3.6B) and 11 K (Figure 3.6C). In both cases, we measured I-Vs by sweeping only over small increments of voltage (1-2 V) at a time. This is done so that if any evidence of NDR is present the scan can be repeated immediately.

![Figure 3.6: A) Schematic showing how ensembles of NW RTDs are contacted. B) Room temperature and C) low temperature current-voltage relationships for an ensemble measurement of nanowire RTDs.](image)

We did not observe NDR when measuring these devices at room temperature. When measured at 11K, clear NDR appeared in the first two scans of a device (Figure 3.6), but was not present in subsequent scans. PVCRs of 1.6 and 1.9 were found for this device. Recall that Sakr et al. has argued that the presence of NDR at room temperature but not at low temperature indicates that
most of the NDR seen in the nitrides is not due to tunneling at all. Here, we saw NDR at cryogenic temperatures but not at room temperature, from which we can conclude that these devices work through a resonant tunneling mechanism and not through the charging and discharging of trap states. The fact that the NDR is not present in ensemble measurements at room temperature but is present at cryogenic temperatures is consistent with a tunneling mechanism leading to NDR. However, the fact that scans show hysteresis does leave open the possibility that traps have some effect on the electrical characteristics of the device, perhaps playing some role in the disappearance of NDR upon repeated scans. Further work in this area is needed to decisively state the role of traps, if any, in these devices. It should also be noted that the NDR in these ensemble measurements occurs at a higher voltage than what simulations would predict (see Figure 3.7). This could be due to a large series resistance in the device, or a thin layer of insulating material coating the nanowires acting as a barrier after the application of HSQ. Improvements in processing could potentially bring down the voltages at which NDR occurs in future devices.

To further support these ensemble measurements, single nanowire electrical measurements are performed at room temperature using a FEI Helios Nanolab 600 Dual Beam Focused Ion Beam/Scanning Electron Microscope equipped with Kleindiek nanomanipulators. These nanomanipulators are capable of making contact to both a single nanowire and the Si substrate, and can therefore be used to take I-Vs of individual nanowires still attached to their
substrate. A schematic representation of the measurement is provided in Figure 3.7A, along with an SEM image of the measurement included in Figure 3.7B. Not only can this measurement scheme tell us the electronic characteristics of individual nanowires, but it also allows for accurate calculations of current density, since the radius of the contacted nanowire can be directly measured in the SEM. Room temperature J-V measurements for both a single contacted nanowire and two simultaneously contacted nanowires can be seen in Figure 3.7C. These J-Vs show clear NDR occurring in both the single and double nanowire measurements. Unfortunately, it is difficult to maintain contact to the same nanowire for a prolonged amount of time using the nanomanipulators, making it difficult to repeatedly scan the same nanowires. That being said, what limited repeated measurements that were performed show that NDR disappears after the initial scan of the nanowires and is not present in backwards scans. The J-V for the single nanowire shows a PVCR of 2.4 and a peak resonant tunneling current density of $5 \times 10^5 \text{A/cm}^2$. This is an exceptionally high current density, and is roughly five times higher than what has been previously reported for AlN/GaN RTDs[51]. Though this current density is not quite as high as some astoundingly high current densities that have recently been reported (current densities greater than $10^6 \text{A/cm}^2$ [57]), it is comparable to what has previously been shown in other III-V RTDs[58, 59].

The experimental data in Figure 3.7C is modeled using a simple circuit consisting of three components in series: the simple RTD model described in
Section 3.1, a Schottky diode between the top n-GaN region and nanoprobe tip, and a generalized series resistance. The model RTD’s active region consists of 1.25 nm of AlN and 2-nm of GaN. These values are within 1 or 2 monolayers of the thicknesses revealed by STEM in Figure 3.4. The ratio of nanowire sidewall area to nanowire top area (roughly a factor of 18) is used to scale down the current density, thus taking into account the effect of nanowire geometry on the model.

Figure 3.7: A) Schematic showing how individual nanowire RTDs are contacted. B) SEM image of a nano-probe contacting a single nanowire RTD. C) Room temperature current-voltage relationships for a single nanowire measurement. Simulated I-Vs are included for comparison.

The Schottky diode between the nanowire top and the nanomanipulator tip is modeled according to the electron affinity of GaN and the work function of the tungsten probe (4.5eV). Series resistance, the only fit parameter, is adjusted to achieve the best fit, which corresponds to a series resistance of 4µΩ-cm². Given
the simple nature of this model and that only one fit parameter is used, the modeled and experimental J-Vs are exceptionally close.

These results show that it is possible to fabricate a coaxial (m-plane) nanowire AlN/GaN RTD grown on Si(111) substrates by PAMBE. The STEM results prove that the methods described in Chapter 2 can be used to grow nanowires within target layer thicknesses for use in coaxially-oriented electronic devices. The lack of NDR at room temperature and the presence of NDR at cryogenic temperatures in ensemble I-V measurements provides evidence that these nanowire RTDs work though tunneling and not charging and discharging trap states. This shows that high quality nanowire heterostructures could be particularly useful in the formation of nitride RTDs. Furthermore, the extremely high current density found in single nanowire measurements (5×10^5 A/cm²) supports our general idea that a core-shell geometry might lead to increased currents due to active region area scaling with nanowire length. These nanowires also offer a path forward towards the integration of III-nitride RTDs onto Si substrates and technologies.

But on a larger level, the work in this chapter demonstrates that it is possible to create devices using nanowires that cannot be formed in a planar geometry. The combination of non-polar orientation, an active region that scales with nanowire length while the nanowire has a small footprint, and the integration onto Si substrates together make this result challenging to replicate in a planar device. That being said, one must always keep in mind that using a nanowire
geometry comes with many challenges that are not faced when a planar device is used, particularly difficulties related to the reproducible processing of nanowire devices. For each different nanowire-based device, the potential advantages of using the nanowire geometry must be weighed against potential disadvantages. The next chapter will again focus on another device that would be extremely difficult to form in a thin film form, but is possible to form using nanowires.
Chapter 4
Graded AlGaN polarization-induced nanowire LEDs

This chapter is a modified version of two previous publications by the author [60, 61]. I would like to thank Patrick Phillips (STEM imaging) and Thomas Kent (EL) for their contributions to this chapter.

This chapter focuses on our research into polarization-induced doping in AlGaN nanowires. Because polarization-doping might not be familiar to some readers, a brief explanation of the basics of polarization is provided. With these basics covered, we argue that III-nitride nanowires are particularly well suited for applications involving polarization-doping. The design, growth, and device characterization of polarization-induced nanowire light-emitting diodes is then described.

4.1 Polarization in III-nitrides

Polarization-related effects are seen in all materials with a non-centrosymmetric crystal structure. Non-centrosymmetric crystal structures, for example the zincblende and wurtzite structures, are commonly found in compound semiconductors. Therefore, polarization-effects are present in many semiconductors. However, polarization-related effects took on a new level of
importance in the early 1990’s with the work of Shuji Nakamura on GaN based blue LEDs and lasers[1, 5]. It was quickly realized that polarization-effects in nitrides play a large role in device performance. For example, polarization charge at interfaces can lead to shifting of emission in the active region of an LED or can lead to the formation of a two-dimensional electron gas in a high electron mobility transistor (HEMT). The relative importance of polarization in nitrides is larger compared to other common semiconductors because polarization itself is stronger in the nitrides.

One major difference between the nitrides, which have a wurtzite structure, and other III-V semiconductors, which have a zincblende structure, is that the nitrides exhibit both spontaneous and piezoelectric polarization while the zincblende semiconductors only exhibit the latter. A material exhibits piezoelectric polarization if an applied strain in the material leads to some separation of charge (i.e. a dipole, or just polarization) in the crystal. A material exhibits spontaneous polarization if the separation of charge is intrinsic to the material itself. That is, no applied strain or field is needed to create a charge dipole in materials that exhibit spontaneous polarization, the dipole already exists. This then is one reason why polarization is more important in the nitrides than in other semiconductors, because in the nitrides some charge separation is always present in the crystal, while in other semiconductors the state of the crystal determines whether there is any separation in charges.
One might ask how spontaneous polarization occurs in the nitrides. As previously stated, the wurtzite structure is non-centrosymmetric, which means it lacks inversion symmetry. In addition to this, the lattice parameters of wurtzite structures commonly deviate from their ideal ratio (i.e. $c/a = (8/3)^{1/2}$). The deviation provides a small displacement between the cation and anion positions in the material. The displacement between cation and anion, along with the lack of inversion symmetry, and the strongly ionic character of the nitride bonds leads to a small dipole created within the unit cell of material. The more ionic the bonding, the stronger these dipoles and spontaneous polarization will be. Also, the dipoles are aligned the [0001] direction of the wurtzite structure such that the [0001] direction points towards the negative end of the dipole and the [000-1] points to the positive. We will see later that the distinction between materials that grows along the [0001] (called Ga-face) and material that grows along the [000-1] (called N-face) has a large effect on polarization-induced charge. The magnitude of the spontaneous polarization in a variety of materials is shown in Figure 4.1. Notice that ZnO, another semiconductor that has the wurtzite crystal structure, also exhibits spontaneous polarization.
In the bulk, this spontaneous polarization does not usually manifest because the charge in adjacent dipoles in neighboring unit cells cancel out with one another. This makes sense, since there should be no net charge in a bulk slab of semiconductor material. But at a surface of interface, the change in spontaneous polarization density ($P_{sp}$) on either side of the interface leads to some net charge. One way of considering this is that at a surface, there are no longer any adjacent dipoles in neighboring unit cells to cancel out the charge at that surface. Bound charge density is determined by the following equation:

$$\rho_R(z) = \nabla \cdot P(z)$$  \hspace{1cm} (Eq. 4.1)
where \( P(z) \) is the polarization density along the growth direction of the material, \( z \).

Figure 4.2: Polarization-induced charge in free-standing GaN. A) A schematic of a free-standing slab of GaN with surfaces labeled. B) Polarization density along the slab. C) Polarization-induced and compensating charge due to changes in polarization density.

As an example of this, Figure 4.2 shows the positive and negative bound polarization charge in either end of a free-standing slab of GaN material. The unbalanced surface charge causes an electric field in the semiconductor, dictated by Poisson’s equation

\[
\nabla \cdot E = \rho / \epsilon \quad \text{(Eq. 4.2)}
\]

where \( E \) is the electric field, \( \rho \) is charge density, and \( \epsilon \) is the permittivity of the material. The electric field in this slab leads to an unsustainably large voltage across the slab that must be removed. Therefore, the bound polarization charge
at the surfaces of the GaN material must be screened by some other charges ($\rho_s$). The possible sources of charge that might provide this screening, including surface states or valence band electrons, are described elsewhere[63].

A similar case occurs for a heterojunction made between two materials that have different spontaneous polarization densities. For example, AlGaN and GaN have different magnitudes of spontaneous polarization, and therefore there will be some bound polarization charge at an interface between the two. This is shown in Figure 4.3. Two points should be made about this figure before it is discussed further. First, it should be noted that in Figure 4.3 only the bound charge at the AlGaN/GaN interface and the AlGaN surface is accounted for. Of course there will be some charge on the free surface of GaN on the opposite side of the material, but this is assumed to be screened for the same reasons described above, and is therefore neglected. Second, strain in the AlGaN layer will lead to some addition contribution to the spontaneous polarization due to piezoelectric polarization. Because these two sources of polarization will add charge with the same sign for AlGaN strained to GaN, the spontaneous polarization is the focus here. This is in fact the case for the majority of this dissertation, as the strain-accommodation in nanowires reduces the piezoelectric polarization effects. However, it should be noted that polarization induced charge from spontaneous and piezoelectric polarization will not always necessarily have the same sign, and in some cases can cancel one another out.
Figure 4.3: Polarization-induced charge in an AlGaN/GaN heterostructure. A) A schematic of AlGaN on top of GaN. B) Polarization density along the length of the heterostructure. C) Polarization-induced and compensating charge due to changes in polarization density.

With these clarifications aside, we can now discuss Figure 4.3 in greater detail. At the AlGaN/GaN interface there will be some net positive bound charge, assuming the material is Ga-face. This charge is due to the step function in polarization density that occurs at the interface. The bound positive charge pulls down the bands at this interface, which will be an attractive position for electrons to accumulate in. Electrons then diffuse to this interface from either donor like surface states on the AlGaN, or from donor states already in the material. Note
that this process is very similar to modulation doping, first established using AlGaAs/GaAs heterostructures in the late 1970’s [64]. Regardless of where they originate, electrons at the interface will be confined so that they can move freely in the plane perpendicular to the growth direction, but cannot move parallel to the growth direction. In other words, a two-dimensional electron gas \((n_s)\) forms at the heterojunction interface. Because the electrons have screened the bound positive polarization charge, local charge neutrality is maintained at the interface and the minimum energy state of the system is achieved. Heterostructures of AlGaN on GaN are commonly used to form HEMTs[65]. As mentioned earlier, if the material is grown N-face instead of Ga-face the bound polarization charge at the interface will have the opposite sign and will not be compensated by electrons, but instead by holes.

Next, consider what would occur if the heterostructure is not abrupt, but instead the composition of the material is linearly changed from GaN to AlN. In this case, the change in polarization density, like the change in composition, will also change linearly. Because the bound polarization charge is determined by the gradient of polarization density, a constant amount of bound polarization charge will be present throughout the entire graded section of the material. This is illustrated in Figure 4.4. It is assumed that this material is initially GaN, but as it is grown along the [0001] the composition of Al is steadily increased. One way of thinking about this is that there is a small increase in the dipole magnitude in each unit cell of the materials as more Al is increase. Essentially, this takes all of
the change that occurred at the abrupt interface shown in Figure 4.2 and smears it out along the length of the entire graded section. Again, if the bound polarization charge is positive, electrons will move to screen the bound charge, leaving a three-dimensional electron slab, or in other words, n-type material. Jena et al. first showed this could be used to form n-type material in Ga-face material graded from GaN to AlGaN[66].

![Diagram](image)

**Figure 4.4:** Polarization-induced charge in graded AlGaN. A) A schematic of AlGaN on top of GaN. B) Polarization density along the length of the heterostructure. C) Polarization-induced and compensating charge due to changes in polarization density.
In this case, surface donor states were used to provide the electrons. Similarly, Simon et al. formed p-type material by grading N-face material from GaN to AlGaN[67]. However, in this latter case, Mg dopant atoms were used to provide the holes necessary to screen the bound negative polarization charge, not surface states. A later publication showed that it is possible to form p-type material without the use of Mg dopants[68]. Unfortunately, it seems that there is no consensus currently as to whether Mg is indeed necessary to form p-type material in this way. This technique of compositionally grading III-nitride layers to form conducting layers is called polarization-induced doping or simply polarization doping. Utilizing this technique in AlGaN nanowires will be the focus of the remainder of this text.

There are two major benefits to polarization-induced doping. First, generally speaking, impurity activation energies increase with band gap, making it difficult to thermally ionize dopants in wide band gap semiconductors. This trend is shown in Figure 4.5. For example, the very large activation energies of Mg in AlN or AlGaN with a high % of Al make it difficult to form highly conductive p-type material. Luckily, polarization-induced doping can be used to activate dopants so that large thermal activation energies are not a problem. We previously mentioned that the source of free carriers that screen bound polarization charge can come from multiple sources, including surface states or impurities. Therefore, if a graded heterostructure like the one in Figure 4.4 is doped with the proper impurities, the bound polarization charge will activate the
impurities, not thermal energy. This was shown in Simon et al. [67]. In this work, low temperature Hall measurements of Mg doped graded AlGaN layers showed that hole concentrations do not freeze out at low temperatures.

Figure 4.5: Impurity activation energies as a function of band gap for some common semiconductor[69, 70].

This is not possible if the Mg atoms were thermally activated, so they therefore must be activated by the presence of polarization-induced charge. Therefore, polarization-induced activation of dopants is one possible solution to the high thermal activation energies in wide band gap semiconductors.
Polarization-doping also provides the opportunity to achieve highly conductive material while maintaining high mobilities. When dopants are used to control conductivity, there is always a tradeoff between high carrier concentrations and mobility. Activated impurity sites do supply free carriers, but they also act as scattering sites for those carriers, thus reducing mobility. Electrical conductivity (\(\sigma\)) is given by,

\[
\sigma = q(n\mu_n + p\mu_p)
\]

(Eq. 4.3)

where \(q\) is the charge of an electron, \(n(p)\) is the electron(hole) concentration, and \(\mu_n(\mu_p)\) is the electron (hole) mobility. So by adding impurities \(n\) or \(p\) will increase, but \(\mu_n\) or \(\mu_p\) will decrease. Polarization-induced doping can reduce ionized impurity scattering, by avoiding the need for impurities altogether. This means that charge concentration can be controlled without a decrease in mobility, leading to overall higher conductivity. This was experimentally shown by Jena et al.[66]. They found that it is possible to achieve polarization-doped n-type AlGaN with higher concentrations than Si-doped GaN. Surprisingly, the conductivity was higher not only because of larger carrier concentrations in the AlGaN, but also higher mobilities in the AlGaN. This could be quite useful in devices that require not only highly conductive 3D material, but also high mobilities. That being said, in some devices it might be beneficial to achieve the highest possible carrier concentrations by reinforcing the polarization-induced charge by adding the appropriate impurity atoms.
4.2 Motivation for nanowire-based polarization doped devices

The previous section covered how polarization-induced doping works, and what advantages it has over impurity doping. In the current section, some of the difficulties of employing polarization-induced doping are covered, and nanowires are presented as possible solutions to these difficulties. The main difficulty comes in the lattice mismatch between different members of the III-nitrides. As stated before, the bound polarization charge in a layer is determined by the gradient of the polarization density. In AlGaN, that specific amount of charge is given by the following expression

\[
\rho_p(x) \approx 5 \times 10^{13} \times \frac{(x_2 - x_1)}{d}
\]  
(Eq. 4.4)

where \(x_1\) and \(x_2\) are the composition of Al at either end of the graded layer, and \(d\) is the thickness of the graded layer (in centimeters)[67]. From this expression, it is clear that the greatest amount of polarization-induced charge is achieved by grading over large ranges in composition over small lengths. However, the lattice mismatch between the different binary members of the nitrides (for example, GaN and AlN) sets limitations on the compositional range that can be graded over.

As testimony to this limitation imposed by strain, there have been many publications in which researchers used polarization induced doping in graded AlGaN layers[66-68, 71-73], but they collectively have only graded over
compositional ranges as large as 30% (i.e. either grading from GaN to Al$_{0.3}$Ga$_{0.7}$N or from AlN to Al$_{0.7}$Ga$_{0.3}$N). If layers where graded over a larger range of composition but over the same thickness of materials, they would most likely relax. That is, strain energy builds up in the graded layer as composition is changed and the layer gets thicker. At a certain critical thickness, defects form in the material to relieve the strain energy it contains [74]. The value of the critical thickness decreases as the compositional range increases.

In order to show the range of possibilities for polarization-doping in graded AlGaN, Figure 4.6 displays $\rho_n$ for different combinations of layer thickness and compositional range using Eq. 4.4. Note that this does not include the amount of charge due to piezoelectric polarization.

Figure 4.6: Polarization-induced due to spontaneous polarization in AlGaN layers graded different lengths and compositional ranges. [75]
Values for the critical thickness of AlGaN grown on GaN were approximated from plots found in Lee et al.[75], and included as the dashed line in Figure 4.6. Additionally, the approximate critical thickness of graded AlGaN layers on GaN is plotted as a dotted line. The critical thickness for a graded layer that terminates at a given composition is found by multiplying the critical thickness of an abrupt layer of the same composition by a factor of 2. This should only be taken as a very rough estimate of the critical thickness of the graded layer, meant only to show that in general graded layers should have a larger critical thickness.

Because lattice mismatched materials that have relaxed are too defective for use in a device, any graded layer grown with a range of composition and thickness over the dotted line are not useful. This sets a limit on the kind of layers that can be formed using polarization-doping. Any way of overcoming this limitation would need some method of grading any compositional range over a target thickness without worrying about strain-related defects.

Nanowires are ideally suited for just such a solution due to strain accommodation. As described in section 1.2, nanowires benefit from increased strain accommodation compared to thin films. The dislocation-free AlN/GaN heterostructures described in Section 2.5 exhibited the benefits of this strain accommodation. The following section describes the design of a nanowire structure that takes advantage of polarization-induced doping to create light emitting diodes. These devices will be the primary focus of the remainder of this dissertation.
4.3 Polarization-induced Nanowire Light Emitting Diodes (PINLEDs)

As previously stated, the large energies required to activate dopants in wide band gap semiconductors is a serious impediment to using those materials in certain applications. Ultraviolet(UV) light emitting diodes is one such application that is limited by this problem. AlGaN is generally assumed to be the most likely candidate for high efficiency UV LEDs and lasers, but the difficulty in creating highly conductive, high % Al AlGaN has held back progress in this area[76]. This makes UV LEDs an ideal candidate with which to implement polarization-induced doping. We propose the use of polarization-induced nanowire light emitting diodes (PINLEDs) that emit in the UV that could possibly alleviate the problem of poor p-type doping in high %Al AlGaN.

The basic PINLED design is shown in Figure 4.7. In the base of the nanowires, Al\textsubscript{x}Ga\textsubscript{1-x}N is graded from x=0 to x=1 along the c-axis, resulting in an n-type conducting region(assuming Ga-face orientation). At the center of the nanowires, an active region of a single GaN (or AlGaN) quantum disk with an AlN cladding on either side of the well is grown. Finally, in the top of the nanowires, Al\textsubscript{x}Ga\textsubscript{1-x}N is graded from x=1 to x=0, resulting in a p-type conducting region(again, assuming Ga-face). Anderson’s Law is used to determine the band offset between n-GaN and n-Si, using published electron affinities for both[77]. This method predicts a conduction band offset of 0.5-0.75eV at the n-Si/n-GaN interface. However, in the case of Ga-face nanowires, bound polarization charge
at this n-GaN/Si interface reduces this barrier, which should allow for conduction through the Si substrate into the nanowire base.

Figure 4.7: Schematic of original design for polarization-induced nanowire light emitting diodes (PINLEDs).

The three-dimensional self-consistent strain and Poisson solver, nextnano3[78], is used for modeling the PINLED structure. The strain state of the nanowires is modeled (see Figure 4.8A), so that contributions from piezoelectric polarization can be considered. The contribution from spontaneous polarization due to change in composition is also considered. The predicted carrier densities and band diagram from this model are displayed in Figure 4.8B and Figure 4.8C, respectively. This model is admittedly simple, as it does not include surface pinning of the nanowires [55]) or the formation of coaxial AlN and its effect on the
strain state of the nanowire. Therefore it is only meant to provide a rough idea of the values it provides (i.e. carrier density, strain state, etc.).

Figure 4.8: The modeled A) strain, B) carrier concentration, and C) band diagram for an individual PINLED.

There are several advantageous aspects of this design. In the base and top graded sections of the nanowire, the gradual change in band gap between GaN and AlN (2.8 eV) is seen in only one band (valence band for the base, conduction band for the top). This creates barriers on either side of the device.
active region that prevent free carriers from overshooting the QW. The barrier in the conduction band of the nanowire top is especially important, as it should help prevent electrons from overshooting the QW. Furthermore, the center of the nanowire consists solely of AlN. Given the extremely large band gap of AlN (6.2 eV), the device can accommodate AlGaN QWs with very high concentrations of Al without sacrificing much in the way of confinement. This should make it possible to push PINLED emission into the deep UV. Finally, as with almost all of the nanowires described in this dissertation, PINLEDs are grown on Si substrates. The possibility of fabricating deep UV LEDs on Si substrates that avoid the problem of p-type doping in AlGaN make this device design particularly interesting. The benefit in growing on Si wafers comes not only from the lower cost of Si wafers compared to sapphire, but also the possibility of scaling up production by using large, 12” Si substrates. For all of these reasons, the devices described here could offer a possible alternative to the current technology in III-nitride based UV LEDs.

4.4 Growth of Graded Nanowires

To realize this structure, we employ the two-step growth method described in Chapter 2. Nanowires are first nucleated at 720°C, then the substrate temperature is ramped to 780°C, after which no new wires should nucleate, and existing nanowires continue to grow. Previously, the two-step method was used, in part, to suppress the nucleation of nanowires and maintain low densities at
long growth times. But in the current case, a low density of nanowires is not desirable, so the nucleation step is executed under conditions in which nanowires nucleate and reach saturation quickly (roughly 2 to 3 minutes). The nanowire density is chosen to be \( \sim 400 \, \mu m^{-3} \), resulting in an array of densely packed nanowires (see SEM image in Figure 4.9). The importance then to using the two-step growth with these devices is not to control density but rather to ensure that GaN forms exclusively in the vertical direction, while AlN continues to grow both vertically and coaxially. The result is a graded AlGaN core encased radially in an AlN shell. While its formation is unintentional, this coaxial layer of AlN is beneficial to the PINLED structure, as it seems to passivate the sidewall surfaces of the nanowires and make devices fabricated from these nanowires less susceptible to changes in their surroundings.

Figure 4.9: SEM images of an as-grown PINLED sample in A) plan view and B) cross-section.
This passivation becomes apparent when two PINLED samples grown using either one-step or two-step conditions are electrically measured while the surrounding air is pumped away. In this measurement, a constant current is sourced in the device, and the voltage necessary to achieve that current is recorded. The measurement begins under atmosphere, and then the air surrounding the nanowires is pumped away, leaving the devices under vacuum. The responses of the one-step and two-step devices are quite different when the air is pumped away (see Figure 4.10).

Figure 4.10: The voltage needed to supply a constant current of 120 mA over time while the air around the device is pumped away. A) PINLEDs grown using one-step procedure. B) PINLEDs grown using two-step procedure.

For the one-step sample, the voltage drops dramatically and EL emission disappears when the pumping starts. When the chamber that holds the sample is vented both the voltage and EL slowly return to their normal levels. From this experiment we can clearly see that the device’s performance depends greatly on
its surroundings. The samples grown using the two-step method show much
different results. Like what occurred for the one-step sample, voltage drops
when pumping starts. Both the voltage and EL change much less drastically
than what occurred for the one-step sample (Figure 4.10B). Thus devices made
from two-step samples are less sensitive to changes in their environment. We
believe that this difference is due to the lack of radial GaN formation at the higher
temperatures of the two step growth. Having covered the impact of using two
step growth conditions to form PINLEDs, let us now turn our attention to another
important aspect of their growth: how to control alloy composition along the
length of the nanowires.

Compositional grading can be accomplished in one of two ways. In the
first generation of PINLEDs, graded AlGaN sections were formed by changing
the effusion cell temperatures of both the Al and Ga cells (increasing Al cell
temperature and decreasing the Ga cell temperature). Because the flux of
material from an effusion cell is exponentially related to the cell’s temperature it is
necessary to logarithmically increase cell temperature to linearly increase flux
(vice versa to decrease the flux). While this does work in creating graded AlGaN
sections, there are two major drawbacks to using this method. First, the change
in cell temperature in graded sections leaves the two cells with drastically
different temperatures than what they started with. This means the flux they
provide will also be drastically different. If the same cell needs to be used in
subsequent stages of the growth, then the grower will need to wait for the cell
temperatures to stabilize, during which time impurities can adsorb to the nanowires. This growth stop can be detrimental to device performance.

An additional difficulty with using this method is that it does not allow a great deal of freedom in the length of nanowire that is graded. Recall, that if a section is to be graded from GaN to AlN, using this method the Ga cell temperature is lowered while the Al cell temperature is increased. To grade over a shorter distance, it is necessary to cool or heat the cell more rapidly. However, at some point there is a limit to how quickly a cell can be cooled. That is, once all power to the cell has been cut off, the cell will cool in “free fall” and there is nothing the grower can do to make this cooling occur faster. This then sets some minimum value on the length of graded sections.

To avoid these problems, an alternative method is to pulse the shutters for the Ga and Al cells such that the effective flux over a given time is lower than it would be if the cell's shutter simply remained open. The composition of the nanowires is then controlled by changing the duty cycles of the Ga and Al shutters. The pulses each occur within the amount of time it takes to grow a single monolayer of material, so as to gradually change the composition. There is no limit to how quickly the duty cycle can be changed, so there is no lower limit to length of the graded sections. Additionally, previous results have demonstrated that the shutter pulsing method leads to increased EL. Unfortunately, there are some drawbacks to this method. First, while the shutters of an MBE system are designed to be pulsed many thousands of times, at some
point actuating the shutters enough will cause mechanical failure of the shutters. Second, the shutters take some small amount of time to actuate. As long as the time for the formation of one monolayer of material is much longer than this actuation time (usually fractions of a second), then there is no problem. For the growth rates used in this work, this is not an issue. However, if the growth rates were increased, this would decrease the time needed to form a single monolayer and the time it takes to actuate the shutters come into play. That is, the use of shutter pulsing could set a limit on the maximum growth limit that can be employed. Therefore, each of these techniques (cell temperature ramping and shutter pulsing) has its own drawbacks that must be considered.

4.5 Structural Characterization

A variety of techniques are used to characterize PINLED samples once they are grown. For initial samples, X-ray diffraction (XRD) was used to verify that the nanowires include both GaN and AlGaN (Figure 4.11). To do this, the Si (111) peak is used to align the diffractometer. ω-2θ scans over the range of angles that would include both the GaN and AlN (0002) peak was performed. If the nanowires consisted of only GaN, then only one peak should occur in this scan. However, if the material composition is graded, then there should be a broad shoulder on the main GaN peak extending to the position one would expect to find the AlN (0002) peak. Just such a scan is shown in Figure 4.11.
XRD scans such as this were the first proof that PINLED samples were successfully graded over the compositional range from GaN to AlN.

![XRD scan of PINLED sample](image)

Figure 4.11: XRD of an as-grown PINLED sample.

However, this is a bulk measurement, and can only determine what compositions are present in the material, not how composition changes along the length of the nanowires.

STEM is used to determine how composition changes along the length of the individual nanowires (Figure 4.12A). In HAADF mode, the image intensity is related to the atomic number of the material, thus the intensity is brighter in areas high in Ga and the intensity is low in areas with a high amount of Al. A few general features of the nanowire shown in Figure 4.12A can be pointed from a simple inspection of the image.
Figure 4.12: HAADF of A) an entire individual PINLED nanowire and B) an atomic resolution image of the GaN quantum well at the center of the nanowire.

First, along the length of the nanowire the intensity gradually decreases (increasing Al content), there is then a small bright section at the nanowire center (the GaN QW), finally followed by an increase in intensity (increasing Ga content). Another feature is that the nanowire has a thick coaxial shell of AlN (darker material). This shell is thicker at the nanowire base because it grows continually during deposition. That is, at the base the coaxial shell forms over roughly the entire deposition time and closer to the top the coaxial shell forms over a shorter length of time. This leads not only to a thicker shell at the base, but also a darker intensity when looking through the center of the nanowire at its
bottom (due to the thicker AlN coverage in this section). While these general observations are important for understanding how PINLEDs form, a different technique is needed for a quantitative measurement of composition.

To support the qualitative change in intensity seen in the HAADF image, composition is measured quantitatively using energy-dispersive x-ray spectroscopy (EDXS). This technique measures the relative amounts of Ga and Al along the length of nanowire (see Figure 4.13). The trend in both Ga and Al composition shows the nanowires to be linearly graded as desired.

It should be pointed out that the average length of each graded layer slightly deviates from the target structure. This is most likely due to changes in vertical growth rates caused by the increase in nanowire diameter during deposition, consistent with AlN/GaN heterostructures previously discussed in Section 2.5.
STEM is also used to get a sense of the number of extended defects in the nanowires. When STEM is used instead of conventional TEM, the conditions for imaging dislocations are relaxed, thus allowing easier imaging of dislocations[79]. Therefore, dislocations would be apparent in images like the one displayed in Figure 4.12, if they were present. However, dislocations are not the only form of extended dislocations. Direct comparisons of catalyst-free and catalyst-assisted nanowires exhibit a large difference in stacking fault density [80]. Therefore, the density of stacking faults in PINLEDs is expected to be quite low or non-existent, given the fact that they are catalyst-free nanowires. To determine the density of stacking faults, we used atomic resolution STEM imaging in HAADF mode. At least 19 atomic resolution STEM images from 6 different PINLED samples have been closely investigated to discern the density of stacking faults in PINLED samples. Of these 6 samples, only one of them showed the presence of stacking faults. An example of stacking faults in a PINLED structure is shown in Figure 4.14. In the one nanowire that contained stacking faults, the density of stacking faults is 2.6E-6 cm⁻¹, which is comparable to the density of stacking faults found in catalyst-assisted nanowires grown by MOCVD [81].

It is unclear what caused the stacking faults in only one PINLED sample. Homogeneous GaN nanowires grown by PAMBE are usually reported to be free of stacking faults in the literature, and for the most part our results are consistent with this finding. Because the PINLED sample that showed stacking faults is not
in any sense an unusual sample, it is unclear why it would exhibit stacking faults while others do not.

Figure 4.14: STEM image in HAADF mode taken showing the presence of stacking faults in some PINLED structures [82].

Furthermore, given that only one sample has exhibited stacking faults, it is not possible to establish any trends in what might be driving the formation of stacking faults in PINLEDs. Any future STEM work on PINLEDs should be closely analyzed to see if stacking faults are present, so that a better understanding of their formation in PINLEDs can be reached.

In this section, experimental evidence was provided that shows that the target PINLED structures can be achieved by PAMBE. However, the question still remains to be answered, whether or not the nanowire structures that have been grown exhibit the device characteristics we desire. This will be the subject of the following two sections.
4.6 Device Characterization of Dopant-reinforced PINLEDs

Once the nanowire samples are grown, they are fabricated in simple two terminal devices. Standard photolithography and e-beam evaporation of metal is used to define small circles of thin metal on the nanowire tops. A second contact is made directly to the Si substrate by first scratching off the nanowires on its surface, then annealing a small piece of In onto the Si. More details on the processing steps and contact design are provided in Appendix B. Once the nanowires are processed, a voltage is applied to the nanowire tops and the Si substrate is grounded. In this way, device characteristics of PINLED samples can be determined.

This section and the next focus on the device characteristics of these samples. All of the devices discussed in the current section are doped with Si and Mg during growth to reinforce the polarization-induced doping, and the devices in the following section are dopant-free. Because the nanowires are assumed to be Ga-polar, the bottom section is assumed to be n-type from polarization-induced doping, and is therefore doped with Si (vice versa for the top section). It is difficult to determine the exact amount of Si and Mg in the nanowires, but it can be approximated using the growth rate of the nanowires, the known concentration of dopants in thin film calibration samples measured by secondary ion mass spectroscopy, and the growth rates of these thin films. Working from these known values in thin films, the Si impurity concentration in
the nanowires is believed to be in the range of $1 \times 10^{19}$ cm$^{-3}$, while the Mg impurity doping is thought to be in the range of $1 \times 10^{18}$ to $1 \times 10^{20}$ cm$^{-3}$. Secondary ion mass spectroscopy measurements were performed on a PINLED sample (shown in Figure 4.15).

![Figure 4.15: Secondary ion mass spectroscopy measurements of an ensemble of PINLED. A) Group-III somatic fraction of Ga and Al as a function of depth (top of nanowire corresponds to 0 nm). B) Concentrations of Mg, Si, and O as a function of depth (top of nanowire corresponds to 0 nm). The values provided here are not accurate given the presence of the Si substrate and the unusual nanowire geometry.]

While the results of this measurement do show the presence of both Mg and Si, the company that performed the measurements could not guarantee the concentrations of these atoms given the unusual geometry of the nanowires and the presence of the Si substrate.

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Electrical characterization of a sample PINLED device is shown in Figure 4.16. As expected, the device shows rectification. Under forward bias, electrons and holes recombine in the device active region, leading to EL (Figure 4.17). In Figure 4.17A, EL under different currents is displayed for a PINLED device with an active region consisting of a single GaN QW. The emission energy strongly blue shifts from 2.4 eV at low bias to 3.29 eV as current is increased (Figure 4.17B).

Figure 4.16: A) Linear and semi-log I-Vs for a PINLED device with a single GaN quantum well.

This large blue shift is common in III-nitride LEDs and it is due to the bound polarization charge at the interfaces between the AlN cladding layers and the GaN QW. The bound charge leads to band bending in the quantum well, which separates electrons and holes. This band bending can be seen in Figure 4.8C. Though the space between electrons and holes is increased because of the band
bending, the lowest electron and hole energy levels in the quantum well are now closer to one another.

![Figure 4.17](image)

Figure 4.17: A) Electroluminescence spectra for different current densities. (Inset – picture of a turned-on PINLED device). B) A contour plot of EL intensity as a function current density showing the large blue shift in emission energy with increased current.

This is referred to as the quantum confined Stark effect. Under small current injection, the PINLED EL is strikingly similar to photoluminescence results from similar previously published results[83]. Under high current injection, carriers screen the bound polarization charge and emission blue shifts until the bands in the QW are flat and emission energy equals that of the band gap (Figure 4.17).

As stated earlier, because the center of the PINLED structure consists of AlN, it is possible to employ AlGaN QWs with a wide range of compositions to achieve EL at a wide range of wavelengths. In the initial samples grown, we
attempted to achieve deep UV emission using a sample that contained a 7-nm thick Al$_{0.8}$Ga$_{0.2}$N active region. The EL for this device is shown in Figure 4.18.

![Figure 4.18](image)

**Figure 4.18:** A) EL spectra at taken at room temperature with different current densities. B) Quantum well and overshoot emission as a function of current.

At room temperature and for small currents there is a weak peak at 5eV (250nm) close to what one would expect for Al$_{0.8}$Ga$_{0.2}$N and a second peak near 4eV (300nm). In this case the 5eV peak is assumed to be emission from the quantum well, whereas the 4eV peak is believed to be caused by carrier overshoot of the quantum well. This view is supported by the relationship between the EL intensity of each peaks and current (Figure 4.18B). As current is increased a greater proportion of electrons will overshoot the quantum well. This is in part due to the increased voltage used to achieve higher currents providing more energy to electrons, thus making it easier for them to escape the QW or overshoot it altogether. The increase in the number of electrons injected into the
QW also plays a role, as the recombination of carriers is likely limited by the number of holes in the active region. Any increase in the number of electrons beyond the number of holes will increase overshoot. Thus even though the peaks at 250nm and 300nm start off at roughly the same value for small currents, the peak at 300nm increases much more rapidly as current is increased.

To better understand what range of wavelengths is accessible for PINLEDs, a series of samples was grown that included a progressively larger percentage of Al in an AlGaN QW. The composition of each QW was controlled by pulsing Ga and Al shutters during the QW step. The normalized emission from a selection of these devices is shown in Figure 4.19.

![Figure 4.19: Normalized EL intensity from PINLED samples grown with a variety of active regions.](image)

With a GaN quantum well, emission is centered at 365 nm, as expected. Progressively larger amounts of Al were then incorporated into the quantum well, shifting the EL emission deeper into the UV. The data shows emission as low as
282 nm. In addition to emission from AlGaN, an InGaN quantum well was also inserted into the active region of a PINLED, providing green emission at 563 nm. Even though this is an impressively large range of emission, it should be possible to cover an even broader range by using higher percentages of Al and In in the AlGaN and InGaN quantum wells.

Figure 4.20: Peak EL wavelength as a function of A) the ratio of Al and Ga on and off times used during shutter pulsing in device active regions and B) the expected % of Al in the active region due to shutter pulsing.

While it is already possible to achieve emission over a wide range of wavelengths, EL from the devices in this study seem to suggest that there is a limit to how far into the UV emission can be pushed using the current active region design. Figure 4.20 shows the main emission wavelength for each device in this series, as a function of the ratio of Al to Ga shutter on and off times in the
QW taken (Figure 4.20A), as well as the expected composition of AlGaN in the QW due to this duty cycle (Figure 4.20B).

The emission shifts to shorter wavelengths as the amount of Al is increased. However, the wavelength starts to converge near 280 nm for large amounts of Al in the active region. There are multiple possible explanations of this data. This saturation at a specific wavelength could be due to radiative recombination from a defect site dominating the emission from the AlGaN QW emission. Or perhaps this could also be due to a memory effect from pulsing the shutters during growth. At this point the cause for this trend in emission remains unclear.

Until now, the discussion of device characterization has focused on EL results. This is obviously extremely important given that the devices are LEDs. However, the devices are also designed to function using polarization-induced doping reinforced with impurity dopants. So to confirm that impurities in the nanowires are activated by the presence of bound polarization, we measured PINLED device characteristics room temperature to 15 K. Normal J-V and EL behavior both persist to temperatures as low as 15 K (Figure 4.21).
Figure 4.21: A) EL intensity and current density at 10V as a function of temperature. B) Current density as a function of temperature compared to expected impurity dopant freeze-out if thermally activated.

Upon cooling, EL intensity drops by roughly 80% (Figure 4.21A) and current density at a given voltage drops by roughly 20% (Figure 4.21A). If Mg impurities in the structure were thermally activated, holes in the device would freeze-out and their concentration would drop by many orders of magnitude. To demonstrate this, the current density measured at 10V is plotted as a function of temperature in Figure 4.21B alongside the expected carrier concentration freeze-out for GaN:Si, GaN:Mg, AlN:Si, and AlN:Mg (using previously published values for activation energies[69, 70]). Clearly, the carrier concentrations in impurity doped AlN and GaN should rapidly freeze-out as temperature is lowered. Meanwhile the current in the device remains relatively constant down to 15K, showing that no freeze-out occurs in the device. This insensitivity to temperature
is evidence that impurities are not thermally ionized, but are instead ionized by bound polarization charge.

However, the current in a p-n junction should exhibit an exponential dependence on temperature as described by the ideal diode equation, independently from whatever changes may occur to the carrier concentrations. Our data does not show such dependence. This is possible if carriers tunnel into the active region of the device and recombine, thus providing a current that is largely insensitive to changes in temperature. Figure 4.22 shows how this might occur. First, a band diagram is provided for the entire nanowire structure under a small forward bias. Under forward biasing conditions, the barriers in the depletion region that prevent carriers from making their way into the QW are smaller and thinner. This makes it relatively easier for electrons and holes to tunnel into the QW and recombine (Figure 4.22 C). Because tunneling is insensitive to temperature, this accounts for PINLED devices still working at cryogenic temperatures. Furthermore, Figure 4.21 shows that there is a drop in current and EL intensity when the sample is cooled from room temperature to 150 K. This is most likely due to thermally assisted tunneling. At higher temperatures, carriers will have slightly more energy, due to thermal energy, and can therefore move slightly higher up the barriers on either side of the QW (see Figure 4.22 B). Because the barrier is slightly thinner at its top, the fact that electrons and hole can move closer to the top of the barrier increases the probability of tunneling into the QW. When temperature is lowered from room
temperature, this possibility goes down, reducing both current density and EL intensity.

Figure 4.22: A) Band diagram of a full PINLED structure under forward bias, exhibiting the position of the electron and hole quasi Fermi levels. View of device active region to show how carriers might tunnel into the QW both B) with and C) without assistance from thermal energy.

To further investigate this, the I-Vs measured over a range of temperatures were fit using the ideal diode equation, namely

$$I = I_o (e^{\frac{v}{nkT}} - 1) \sim I_o e^{\frac{v}{nkT}}$$  \hspace{1cm} (Eq. 4.5)
where \( I \) is the current in the device, \( I_o \) is the reverse-bias saturation current, \( V \) is the voltage applied to the device, \( n \) is the ideality factor, \( k \) is Boltzmann’s constant, and \( T \) is temperature in K. Only the section under small biases (~0 to 1V) was used to fit the equation, as it is possible for sections under higher biases to be limited by series resistance. The ideality factor describes how closely to an ideal diode the device is behaving, with an ideal diode having an ideality factor equal to 1. Of course, the PINLED structure is different from a normal p-n junction in many ways, so one would expect a large deviation from expected ideality factors for an ideal diode. Somewhat surprisingly then, previous work in III-nitride p-n junctions has measured ideality factors as high as 7 or 8[84], while the PINLED ideality factor measured here is close to 4 at room temperature. Even though these ideality factors are similar to one another, it is still difficult to interpret these results given that the PINLED structure is very different from a typical p-n junction. That being said, it is still useful to look for large changes in the value of \( n \) as a function of temperature to see if any clear trends emerge from the data. To this end, the PINLED ideality factor as a function of temperature is shown in Figure 4.23. Until temperatures as low as 150 K, the ideality factor is within the previously reported range, but as temperature goes much lower than this the ideality factor increases to values as high as ~90 at 15K. This means that thermionic emission over the built-in p-n junction barrier cannot be the source of current at these low temperatures. We instead attribute this current to carriers tunneling into the device active region, as previously discussed.
4.7 Device Characterization of Dopant-free PINLEDs

Until now, all of the device characterization provided has been for devices that take advantage of Mg acceptors and Si donors to reinforce polarization-induced charges. To better understand how reliant these devices are on impurities, we compare three types of PINLEDs: impurity-free, acceptor doped (Mg), and acceptor (Mg) and donor (Si) doped. The I-V characteristics of these devices are shown in Figure 4.24.

Starting from the device that includes both acceptors and donors, if donors are removed there is a decrease in current at a specific voltage (+10 V) by a factor of 5. If both donors and acceptors are removed there is a further drop in current by a factor of 20. When directly comparing the electrical characterization of devices formed with the use of impurity dopants (both acceptors and donors)
and those that are dopant-free, there is a drop in current by roughly a factor of 100.

Figure 4.24: Current density as a function of applied bias for PINLED devices with different combinations of donors.

This shows that conductivity is greatly improved by supplemental doping of impurities to reinforce polarization-induced charge. As would be expected, p-type conductivity is more strongly improved by supplemental doping, whereas supplemental Si doping has a smaller effect. The small effect of removing Si impurities from the p-type could be due to the unintentional inclusion of donor-like impurities (e.g. Oxygen atoms) that are naturally incorporated into the material during growth. Furthermore, both the dopant-free and doped nanowires exhibit EL with similar intensity for lower current densities (Figure 4.25).
Figure 4.25: EL spectra for three devices with different combinations of doping at the same current.

The peaks seen at ~3.7 and ~4.1 eV in the sample that included acceptors and donors do not appear in the dopant-free device. This indicates that these peaks could be due to impurity-related radiative recombination.

Perhaps more important than how conductivity is increased when impurity dopants are added is the fact that dopants are not strictly necessary in order for the device to work. To our knowledge this is the first time that a p-n junction has been formed without the use of impurity atoms as dopants. This is somewhat surprising, given that the initial work on polarization-induced p-type AlGaN layers showed that graded layers must be doped with Mg atoms to achieve hole conductivity [67]. However, subsequent reports have provided evidence, as we do here, that it is possible to form III-nitride p-n junctions without the use of impurities and that Mg doping is not needed [68].
Putting this discrepancy in the literature aside, there is reason to believe that achieving p-type graded AlGaN without the use of impurity atoms might be easier to achieve in nanowire structures than in planar ones. This is because the nanowire geometry leads to a larger ratio of surface to volume compared to planar material. If we assume that holes must come from surface states (if the material is not doped with Mg), than the large m-plane sidewall surfaces of the nanowires are ideally suited for supplying this charge. The ratio of acceptor-like surface states on the nanowire sidewalls to the bulk donor states is given by the following

\[ \frac{N_A}{N_D} = \frac{\sigma_A^{surf} \times 2\pi rh}{\rho_D^{back} \times \pi r^2 h} = \frac{2\sigma_A^{surf} N_A}{\rho_D^{back} \pi r^2 h} = \frac{2\sigma_A^{surf}}{\rho_D^{back} \pi r^2} \]

where \( N_A \) is the total number of acceptor states, \( N_D \) is the number of donor states, \( \sigma_A^{surf} \) is the density of acceptor-like surface states, \( \rho_D^{back} \) is the density of donor states due to unintentional background doping, \( r \) is the nanowire radius and \( h \) is its height. If typical values for the variables on the right side of the equation are used (\( \rho_D^{back} = 10^{17} \text{ cm}^{-3} \) [85], \( \sigma_A^{surf} = 10^{12} \text{ cm}^{-2} \) [86], \( r = 20 \text{ nm} \)) then this simple calculation shows that the ratio of acceptors to donors is 10:1. This calculation also predicts that as radius increases, this ratio will decrease.

Therefore, it might be interesting in future work to grow graded nanowires with a variety of radii to determine if it is more difficult to achieve polarization-doped p-type material in the thicker nanowires, which this equation predicts.
A similar calculation can also be made for planar material. In this case, the ratio of acceptors to donors should be inversely related to the thickness of the graded layer. This would seem to suggest that p-type polarization in thin films may be more effective in thinner layers. Of course, as discussed previously in Section 4.3, grading over smaller thickness will increase the gradient in composition, thus leading to higher polarization induced charge. This effect will be difficult to separate from the purely geometric effect described above. Nevertheless, grading thin films over progressively shorter layers would be quite an interesting experiment, as it might provide some insight as to the limitations of p-type polarization doping with and without Mg impurities.

At this point, it would be beneficial to take a step back and look at the evidence for p-type polarization-doped material without dopants a bit more closely. With data in Figure 4.24 and Figure 4.25 alone, one might question whether p-type material has been achieved in these nanowires without impurity-doping. Both the electrical and optical characterization of the dopant-free device may have possible alternative explanations. In the case of the electrical characterization that shows rectification (Figure 4.24), there are other ways to achieve rectification without the formation of a p-n junction, for example, with a Schottky barrier. With respect to the observed EL, it is undeniable that electrons and holes are radiatively recombining in the QW to emit light, but holes could be present in the material without any p-type AlGaN. For example, holes could be injected into the nanowire through a reverse biased Schottky barrier between the
p-type nanowire tops and the Ni/Au contact. Unfortunately, direct measurements of carrier type and concentrations in a nanowire are difficult. After all, Hall measurements are the preferred method for measuring carrier type and concentrations in a material, but such measurements require thin film geometry and cannot be carried out in nanowires. This is because an ensemble of individual nanowires does not allow for the lateral conduction necessary to perform a Hall measurement.

Because of this difficulty, an alternative approach is needed to determine if polarization-induced holes are present in the dopant-free PINLEDs. To do this, we compared the electrical characteristics of two devices with the same structure, only with a different metal top contact (in one case Ti is used, and the other Ni). Figure 4.26 includes band diagrams corresponding to the nominal, Ga-face nanowire heterostructures for four different conditions. Two sets of conditions are varied to form these band diagrams. First, it is assumed that either polarization-induced p-type material is successfully formed in the nanowire tops, or that polarization-induced p-type material does not form and that the top is instead lightly n-type due to background impurities. For each of these two conditions, a band diagram is provided with either Ti or Ni used as a contact.

To show the importance of these band diagrams, we will assume for the time being that polarization-doping does provide holes without the use of impurity doping, and that the top of each Ga-face nanowire will be p-type. If the top is p-type, a Ni top contact will result in a smaller Schottky diode at the top of the
nanowire than would occur if a Ti contact is used. Because this Schottky is in series with the actual nanowire p-n junction itself, more voltage dropped on the Schottky will lead to less voltage dropped on the p-n junction.

This difference should lead to devices turning on at a lower applied bias for a smaller Schottky barrier height. Therefore if the device turns on sooner with a Ni contact, this is evidence that polarization-induced holes are present in the nanowire tops.

Let us now assume the opposite situation; that there are no polarization-induced holes in the nanowire tops. In this case, the material would be n-type, with carrier concentrations on the order of the unintentional impurities occurring during growth (here we assume this to be roughly 1E17 cm\(^{-3}\)). If the nanowire

Figure 4.26: Band diagrams for PINLED in which polarization-induced holes are present (A, B) or not present (C, D) with either Ti (A, C) or Ni (B, D) contacts on top.
tops are n-type, then the opposite argument can be made to what was discussed above. That is, the Ti contact will form a smaller Schottky diode than the Ni, so the Ga-face nanowires should turn on sooner with Ti contacts.

Here then, we have a way to gain information about the charge carriers in the nanowire tops from processing devices from the same dopant-free nanowire sample with either Ni or Ti top contacts. If the device with Ni turns on first, that is evidence that the nanowire tops are p-type, and therefore that polarization-induced hole doping is working. On the other hand, if the device with Ti turns on sooner, then it is evidence that there are no polarization-induced holes and that the material is lightly n-type. The I-Vs in Figure 4.27 are taken from a device that contains no intentional dopants in its graded sections. The results show that the device using a Ni top contact turns on sooner than the same device using a Ti contact, therefore we conclude that polarization-induced p-type material is present in the nanowire top.

However, while the electrical characteristics in Figure 4.27 do show that a smaller Schottky exists when Ni is used instead of Ti, which is consistent with the Fermi level being close to the valence band in the tops of the nanowires, this does not necessarily mean that holes are present in the tops of the nanowires. That is, the possibility exists that the Fermi level is indeed close to the valence band, but no holes are present in the material.
A situation similar to this has been previously discussed in the context of N-face high electron mobility transistors [87]. In this work, it was shown that polarization-induced charge and ionized donor states near the valence band can give rise to a situation in which the Fermi level is close to the valence band, and yet there are no holes present. A similar situation might exist in the dopant-free PINLED structures. That is, it is possible that the polarization-induced charge helps provide the proper band lineup such that the valence band and Fermi level are close to one another. This would still lead to the electrical characteristics shown in Figure 4.27, even without the presence of holes in the top layer. Of course, EL requires the recombination of electrons and holes, so holes must be present when the nanowires are forward biased. These holes might arise in the structure when the nanowires are forward biased because the Schottky on top of the nanowires will simultaneously be reverse biased. Under these conditions,
valence band electrons can tunnel through the Schottky barrier into the metal, leaving behind a hole.

In this way, both the electrical and optical data for the dopant-free devices can be explained assuming that polarization-induced charge in the graded top layer provides the proper band alignment, and holes are injected into the nanowires through the Schottky barrier on top of the nanowires. Of course, the same data can be explained if one assumes holes are present in the p-type graded AlGaN section of the device. Unfortunately, at this time it is not clear how one might experimentally determine which of these two situations is the case. That being said, it is perhaps largely irrelevant which of the two is actually occurring in the dopant-free PINLEDs, as the performance of the device in either case will be quite similar.

This chapter has focused on the design and characterization of PINLEDs. The data here shows that PINLEDs and polarization-doping in nanowires can play an important role forming UV LEDs. However, the design used to fabricate the devices in this chapter assumed that nanowires grow with a Ga-face orientation. As will be shown in the following chapter, nanowires in fact grow predominately with an N-face orientation. The consequences of this will be dealt with in the following two chapters.
This chapter is a modified version of a recently accepted publication by the author[88]. I would like to thank Patrick Phillips (STEM imaging), Thomas Kent (EL), Camelia Selcu (conductive-atomic force microscopy measurements), and A.T.M.G. Sarwar (etch studies) for their contributions to this chapter.

The previous chapter has hopefully provided a comprehensive background on PINLEDs. One important area was largely left out of the discussion, namely the importance of material polarity in PINLEDs. This topic is the focus of the current chapter. It will be shown that while the PINLED devices described until now were designed assuming a Ga-face polarity, in fact the nanowires grow with a mixture of material polarities, with a strong majority of nanowires having an N-face orientation. This mixture of polarity is characterized in several ways, including selective etches of nanowires, STEM, conductive atomic force microscopy(C-AFM), and ambipolar EL measurements. Not only do these characterization techniques offer a new view of material polarity in III-nitride nanowires by PAMBE, but they also provide new perspectives on the interaction between polarization-induced charge and impurity charge in the
nanowires. Finally, the measurements and related discussion in this chapter set the stage for the future directions in PINLED device design.

5.1 The Importance of Material Polarity in Polarization-doped Devices

As discussed in Section 4.2, there are many advantages to using III-nitride nanowires instead of thin films in the use of polarization-induced doping. However, one major difficulty comes in the form of controlling material polarity. As described in Section 4.1, material polarity (i.e. Ga-face or N-face) determines the sign of polarization induced charge. In the case of thin film growth, both N-face and Ga-face GaN templates are available, so it is relatively simple to control for material polarity by choosing the correct template. The material polarity of catalyst-free GaN nanowires is not as clear cut. Both Ga-face[89-91] and N-face polarities[92-97] have been reported. Some researchers have even found that in a single sample of catalyst-free GaN nanowires both polarities exist at the same time. Alloing et al. found that in a given sample, 90% of the nanowires were Ga-face[90], while Cherns et al. found that GaN nanowires grown on a thin film of AlN were Ga-face while the defective material that formed between the nanowires was N-face[91]. Based on what has already been published regarding GaN nanowire material polarity, it is unclear what to expect in PINLED samples, even though the original PINLED structure was designed for a Ga-face polarity. Obviously, since material polarity dictates the sign of polarization-induced charge, material polarity in PINLED samples must be well understood.
All samples in this study are grown by PAMBE on n-Si(111) substrates using the design and growth methods described in Chapter 4. To investigate the effects of material polarity and impurity doping in PINLED structures, both dopant-free and impurity doped PINLEDs were used in this study. Because the samples were assumed to be Ga-face, impurities were added to augment polarization-induced charge consistent with a Ga-face polarity. This means the impurities will compensate polarization-induced charge in the N-face nanowires, which will be discussed later on in this chapter.

A sample of dopant-free PINLEDs with a mixture of polarities formed in the same sample would result in a collection of nanowire p-n junctions like the ones shown in Figure 5.1. Both Ga-face and N-face PINLEDs will form a p-n junction, with the only difference coming in their orientation. The Ga-face nanowires will have their n-side down while the N-face nanowires have their p-side down.

The band diagram for both of these configurations is shown in (Figure 5.2). These band diagrams assume the nanowires are fully relaxed and are calculated using the software Band Eng, a one-dimensional Poisson-Schrodinger solver that accounts for the spontaneous polarization in the nanowires[54]. From these band diagrams you can clearly see that the major difference between the two orientations comes at the Si interface. For the n-down, Ga-face PINLEDs (Figure 5.2A) there is no barrier to conduction at the interface (as discussed in
the previous chapter). For the p-down, N-face nanowires (Figure 5.2B) the interface is an n-Si/p-GaN junction.

![Schematic showing resulting situation when dopant-free PINLEDs grow with a mixture of material polarity.](image)

**Figure 5.1:** Schematic showing resulting situation when dopant-free PINLEDs grow with a mixture of material polarity.

This means that the overall structure for the N-face nanowires (including the Si substrate) is n-p-n or two back-to-back diodes. The presence of the n-Si/p-GaN junction should make it very difficult to turn-on the p-n junction in the nanowire. The overall structure for the Ga-face PINLEDs is n-n-p, which means there is no barrier to turning on the nanowire junction caused by the substrate. The electrical and optical behavior of nanowires with each different polarity will be the topic covered in Sections 5.3 and 5.4, respectively. Before that can be covered, an accurate measurement of the number of Ga-face and N-face nanowires in a given sample must be established.
5.2 Characterization by Selective Etching and Electron Microscopy

The first method we used to determine nanowire material polarity was STEM imaging in Annular Bright Field (ABF) mode (Figure 5.3). All STEM images are acquired using a probe-corrected JEOL JEM-ARM 200CF operated at 200 kV. To prepare the nanowires for STEM work, a carbon grid is rubbed onto an as-grown sample and individual nanowires adhere to the carbon. Both
group-III atoms and nitrogen atoms are observed in ABF mode (see Figure 5.3), which means that the stacking sequence of the atoms with respect to growth direction can be determined. ABF mode has been used in previous publications to determine the material polarity in multiple polar materials, including III-nitride material[97]. A total of seven individual nanowires samples were measured in this way, and all seven exhibit an N-face polarity.

![Figure 5.3: STEM image in ABF mode showing stacking order of Ga and N atoms along the growth direction, thus revealing N-face polarity.](image)

This clearly demonstrates that at least the majority of nanowires on the surface of an as-grown sample are N-face. However, this does not rule out the possibility that a minority of the nanowires on a given sample are Ga-face. To determine if there are Ga-face nanowires, and their relative number with respect to N-face nanowires, one could simply perform a great deal of ABF mode atomic resolution imaging on a large number of nanowires. Unfortunately, this would be extremely time consuming.
To avoid this time consuming endeavor, we have employed the use of a selective etch that removes only N-face material to determine the relative number of Ga-face nanowires in a given sample. For this task, we chose KOH as an etchant, which has been shown previously to selectively etch N-face nanowires[95, 96]. In these previous uses, the nanowires were etched for a short amount of time (5 to 10 minutes) with different concentrations of KOH (either a saturated solution [95] or a 0.5 M concentration aqueous solution in [96]) until facets form on the top of N-face nanowires. We have chosen to etch our samples for much longer amounts of time (up to 2 hours) in an 11.7 M aqueous solution of KOH, so that the N-face nanowires will be completely removed leaving behind only Ga-face nanowires. Figure 5.4 shows what a PINLED sample looks like in cross-section before and after a long etch in KOH.

![Figure 5.4: Cross-section SEM images of PINLED samples before and after etching in KOH.](image)

To systematically track the change in density as a function of etch time, separate pieces of the same sample were etched for different amounts of time. SEM images in plan view were used to determine the number of nanowires on the
surface as the etch continues for longer amounts of time. Figure 5.5 shows that there is a steady drop in nanowire density from its initial value (350 µm$^{-2}$) until roughly the 90 minute mark. At this point the density saturates and remains constant at 30 µm$^{-2}$. The remaining nanowires after etching constitute 9% of the initial density.

![Graph showing density as a function of etch time.](image)

Figure 5.5: Density as a function of etch time.

An STEM sample is prepared by dispersing the nanowires that remain on the substrate after a long etch (90 minutes) onto a carbon grid. These post-etch nanowires are imaged using STEM in both HAADF mode (Figure 5.6) and ABF mode (Figure 5.7). STEM images taken in HAADF mode exhibit an interesting feature, namely that the thick shell of AlN has been removed by the KOH. It is unclear why this coaxially formed material alone is removed and the etch stops at the inner AlGaN portion of the nanowire that formed vertically during deposition.
Other than the removal of the AlN shell and some slight removal of material from the nanowire top, the structure is relatively unaffected by etching. Atomic resolution images taken in ABF mode (Figure 5.7) from these nanowires show that the nanowires are Ga-face. A total of six post-etch nanowires were imaged in this way, and all were found to be Ga-face. From this we can clearly see that Ga-face nanowires remain relatively intact on the substrate after long etches and N-face nanowires do not. Looking back to the results in Figure 5.5, we can assume that the as-grown sample consists of a mixed polarity of nanowires, with 9% of them having a Ga-face orientation.

Figure 5.6: STEM HAADF images of individual nanowires both before and after etching in KOH.
Figure 5.7: Atomic resolution STEM image in ABF mode taken from a nanowire remaining after a long etch in KOH. Ga and N stacking proves Ga-face polarity.

5.3 Characterization by Conductive Atomic Force Microscopy

C-AFM is used to both reinforce the results of our etch study, as well as electrically characterize the as grown Ga-face nanowires. C-AFM works by scanning a small probe over the surface of the sample. While the probe is scanned over the sample, a bias is applied to the probe’s tip and the substrate is grounded. Current is collected through the tip and used to form an image. Our aim was to apply a positive or negative bias to the C-AFM tip, which should forward bias only specific nanowires with correct orientation. That is, Ga-face nanowires have an n-down structure and should therefore turn on when a positive bias is applied to the nanowire tops.

The sample measured using this technique includes impurity dopants chosen to reinforce the polarization-induced charge in Ga-face nanowires (Si is
included in the graded bases and Mg doping is included in the top graded section). This should maintain the previously described p-n junction orientation for Ga-face nanowires, but we will see shortly the same will not necessarily be true for N-face nanowires.

Figure 5.8: Conductive atomic force microscopy imaging of as-grown PINLEDs. A) Raw current data collected with a positive bias applied to nanowire tops. B) Isocurrent map of data in A.

It should be noted that the contact between the C-AFM tip and the nanowire tops will most likely be a Schottky. While this will likely increase the applied voltages needed to make the individual nanowires to turn on, it should not prevent the selective imaging of Ga-face PINLEDs.

Figure 5.8 displays the results of a C-AFM measurement conducted with a positive voltage applied to the nanowire tops. Note that we are showing only a narrow range of current to most easily display the C-AFM data. In actuality,
certain small areas of the measurement show currents higher than 100’s of pA. So that the data in Figure 5.8A can be more easily understood, an isocurrent map formed from the same data is shown in Figure 5.8B. As these images show, only a fraction of the total nanowires conduct current during the measurement. More specifically, the density of the conducting areas in Figure 5.8B is 32 µm⁻², which corresponds quite closely to the Ga-face nanowires that remain after long etched in KOH, 30 ± 5µm⁻². The agreement between these two separate measurements of Ga-face nanowires shows that Ga-face nanowires are being selectively imaged in the C-AFM measurements in Figure 5.8.

At this point, one might suggest that the conducting pathways in the C-AFM measurements are due to areas in which nanowires have coalesced. Coalesced GaN nanowires have been widely reported[11, 26, 35, 98, 99], but to our knowledge there have not been any reports of their effect on the electrical characteristics of nanowires. That being said, it is not unreasonable to think that coalescence sites could act as leakage pathways in an ensemble of nanowires and show up in the C-AFM measurements. It is unlikely that this is the source of the C-AFM data in Figure 5.8 for a number of reasons. First, the shape of the conducting paths in Figure 5.8 more closely resemble the tops of nanowires (roughly circular features) than the boundaries between nanowires where they have coalesced, which one might expect to look like the outlines of nanowires. Furthermore, many of the conducting pathways in the C-AFM measurement have a core-shell structure, which means the center of the nanowires are more
conductive than the edge, which would not be possible if coalesced areas were responsible for conduction. Finally, from SEM image analysis we have found that the density of coalescence sites is many times larger than the density of conducting sites measured by C-AFM (see Figure 5.9). For all of these reasons, coalescence sites are not the source of conducting pathways in the C-AFM measurements.

![Bar chart showing density of nanowires](chart.png)

Figure 5.9: The possible sources of conduct paths measured by CAFM with a positive bias applied to the nanowire tops.

So far, only C-AFM measurements with a positive applied bias have been presented. Applying a bias with the opposite sign leads to a situation that is much more complicated than the first because impurities added to the material will compensate the polarization-induced N-face charge. Furthermore, the combination of charges from impurities and polarization might lead to either n-type or p-type material depending on which of these two dominates in each
section of the nanowire. Figure 5.10C shows the possible combinations of n-type and p-type material that might exist in N-face nanowire depending on whether polarization of impurity charge dominates in each section (i.e. top and bottom) of the nanowire.

Putting this complication aside, C-AFM measurements with a negative bias applied to the nanowire tops is shown in Figure 5.10. Even though the same magnitude of voltage is applied, the measured current drops drastically, from 10’s of pA under a positive bias and fractions of a pA under a negative bias. Though the current is much smaller in the negative case, the isocurrent map in Figure 5.10 does seem to display what looks like nanowire features. All four combinations shown in Figure 5.10C will be discussed as possible sources for the conducting areas under a negative bias.

Figure 5.10: C-AFM conducted with a negative bias applied to nanowire tops. A) Raw current data. B) Isocurrent map of data in A. C) The possible combinations of polarization and impurity charges for N-face nanowires.
In the first possible combination of charges (Figure 5.10A, I), Si induced charge dominates in the nanowire base and polarization-induced charge dominates in the top. This all n-type combination makes some intuitive sense, as it is widely known that Mg doping at high substrate temperatures is difficult. There are also no issues with Si doping at high temperatures, so it is not unreasonable to think that impurity charge dominates in the base. Because the samples are grown on n-Si substrates, the overall structure through wires with this combination of charge would be n-n-n, and there would be little barrier to conduction. This type of wire could lead to the conduction in Figure 5.10A.

The second possible combination (Figure 5.10C, II), assumes that impurity doping dominates the polarization-induced doping in both the nanowire base and top. This structure would be a p-n junction with the same orientation as the Ga-face nanowires measured in the Figure 5.8. If nanowires did exist in the sample with this particular combination of doping sources, they would be reverse biased when a negative tip potential is applied, and therefore cannot explain the result C-AFM measurements shown in Figure 5.10A.

The third possible combination is the case where polarization-induced charge dominates the impurity provided charge in both sections of the nanowire (Figure 5.10C, III). The overall structures for this combination would be n-p-n. As stated in Section 5.1, this structure would be difficult to turn on due to the presence of back-to-back diodes. Given that only a relatively narrow range of
voltages are possible to apply during the C-AFM measurement (± 10V), it is unlikely that these nanowires provide the current in Figure 5.10.

In the fourth combination (Figure 5.10C, IV), polarization-induced charge dominates in the base, and impurity charge dominates in the nanowire top. This is unlikely for the same reasons that the first combination discussed above was unlikely (i.e. difficulty in doping Mg at high temperatures, no difficulty in doping Si). Put another way; if Mg doping dominated in the nanowire top, then one might reasonable assume Si doping would dominate in the base (i.e. the second combination). This means that this fourth possible combination is the least likely of the four possible combinations, and there is therefore little chance that the conduction in Figure 5.10A is due to this combination.

After having described each of these combinations, it seems that the first or third are the most likely to be the source of what is measured in Figure 5.10A. But both of these explanations have their own complication. If combination I occurs in the N-face nanowires there would be very little impediment to conduction, and larger currents might be expected under a negative bias. The third combination is not likely the source for considerations listed earlier, namely that a large enough voltage cannot be applied during the C-AFM measurement to turn on these p-down PINLEDs on n-Si. For all of these reasons, it remains unclear what combination of polarization-doping and impurity charge have given rise to the conduction seen in C-AFM under a negative applied bias.
5.4 Electroluminescence and Mixed Polarity

EL measurements of dopant-free PINLEDs and intentionally doped PINLEDs show some striking results of a mixed nanowire polarity. Once again, PINLED ensemble devices were fabricated using the process in described in Appendix B. The two device measured here have the exact same structure, except for a small difference in QW composition (and of course as previously mentioned, the inclusion or exclusion of dopants). EL spectra were measured using a thermoelectrically cooled UV-VIS CCD coupled to a 0.5m spectrometer. Light from the sample was collected using a fused quartz 50mm f/2 singlet lens and subsequently focused onto the entrance slit of the spectrometer. I-Vs for both the dopant-free and intentionally doped structures are provided in Figure 5.11. These I-Vs show that the doped PINLEDs are more conductive under a positive applied bias, while the dopant-free structure is more conductive under a negative bias. This is consistent with dopants augmenting the charge in Ga-face nanowires and compensating charge in N-face nanowires. The EL results of LEDs fabricated from both intentionally doped and UID graded nanowire devices are shown in Figure 5.12 and Figure 5.13, respectively. EL was taken at a range of currents under both positive and negative bias.

The device that includes dopants exhibits strong EL under a positive applied bias (red line in Figure 5.12), which is the appropriate bias to turn on the impurity-augmented Ga-face PINLEDs. The EL peak under this applied bias corresponds to recombination in the device’s Al₁₁Ga₈₉N QW, with some shift in
the emission due to the quantum confined Stark effect (as described in Section 4.6). When the opposite bias is applied the compensated N-face PINLEDs are not nearly as conductive, making very high biases necessary for enough current to flow to carry out the EL measurement.

Figure 5.11: A) Linear and B) semi-log scale I-V characteristics for PINLEDs with and without dopants.

Under a very large negative bias (-30V) applied to the top, the EL intensity is more than 5000 times dimmer than what was seen for the same current density under the opposite bias. This quenching of the QW EL intensity is likely due to a drastic increase in non-radiative recombination from the presence of compensated impurities in the N-face nanowires. In addition to the large
change in intensity, the emission energy has also shifted to much shorter wavelengths.

Figure 5.12: EL for a PINLED device with dopants added under positive and negative bias.

The 264 nm peak could be from radiative recombination at a specific defect site or from the band gap emission in graded AlGaN. Finally, there is a very small peak near 350 nm in the spectrum taken under negative applied bias that could correspond to emission from the device QW. Obviously this peak is many times smaller than the same peak under a positive bias. This shows that QW EL is quenched in N-face nanowires, most likely because compensated dopants prevent electrons and holes from reaching the QW.
The dopant-free nanowires exhibit much different EL characteristics (see Figure 5.13) compared to the intentionally doped samples. Without impurities compensating the N-face PINLEDs, both the Ga-face and N-face nanowires show strong EL. Emission at 405 nm under a positive bias is consistent with the device’s GaN QW that is again red-shifted due to polarization charge. Under a negative bias, EL is observed at 390 nm, corresponding to emission from a slightly less red-shifted GaN QW.

**Figure 5.13:** A) EL for a PINLED device without dopants under positive and negative bias. B) Wavelength and C) EL intensity as a function of current.

The discrepancy in wavelength between the two spectra is most likely due to different current densities in the N-face and Ga-face nanowires, even though the total current reading during the measurement is the same. This difference could
come from the fact that under positive bias, the majority N-face nanowires are reversed biased and act as a large source of leakage for the Ga-face nanowires (which are forward biased). Meanwhile, under the opposite biasing condition, Ga-face nanowires (under reverse bias) supply a source of leakage for N-face nanowires (forward biased). Because there are a greater number of N-face nanowires in a sample, they act as a larger source of leakage, and therefore a smaller amount of overall current passes through the Ga-face nanowires when they are forward biased. Since higher current densities screen polarization charge and blue shift EL, this is consistent with the more red-shifted EL from the Ga-face nanowires. This is supported by the plot of wavelength vs. current density shown in Figure 5.13B, which shows that the N-face PINLEDs blue shift much more quickly as current is increased than do the Ga-face nanowires.

The most striking difference between the EL in Figure 5.12 and Figure 5.13 is the large difference in EL for the negative bias condition. Under a negative bias the intentionally doped PINLEDs exhibited much weaker EL than what is observed under positive bias. In the case of dopant-free devices, the situation is flipped, with the negative bias condition showing roughly 100 times brighter EL compared to the positive bias condition (Figure 5.13C). This shows that in the absence of compensating impurities, N-face PINLEDs do emit strong EL, even in the case where the overall structure of the device is n-p-n, as it is here. Furthermore, the fact that the EL from N-face nanowires surpasses the intensity of the Ga-face nanowires is consistent with a much larger number of N-
face nanowires in the sample, and the previously mentioned argument regarding leakage.

A number of important conclusions can be taken from the effects due to mixed polarity seen in this chapter. First, PINLED samples form with a mixture of material polarities, with 90% N-face and 10% Ga-face nanowires. Second, it is clear that PINLEDs can be successfully formed with either a Ga-face or an N-face polarity, as shown by the ambipolar EL exhibited by the dopant-free PINLED sample. Third, both the C-AFM and EL measurements show that impurities can be added to PINLED structures to either augment or compensate the polarization-induced charge in the structure. This last point is important for PINLEDs moving forward. If catalyst-free nanowire polarity cannot be controlled by either forcing 100% N-face or Ga-face growth, these results show that properly doping the structures can be used to compensate the unwanted polarity, thus making them less conductive and not as large as a source of leakage for the nanowires with the preferred polarity.

Given that the majority of nanowires are N-face, any device utilizing polarization in these nanowires should be designed specifically for N-face nanowires. As stated previously, the original PINLED design assumed a Ga-face orientation. Therefore, a new PINLED design must be established that takes advantage of the N-polar nanowire orientation. This, and other possible changes to the original PINLED design that could improve performance, are covered in the following chapter.
Chapter 6

 Modifications to Original PINLED Design

In this chapter, some possible future directions for PINLED devices will be presented. The previous chapter firmly established that the majority of nanowires in any given PINLED sample are N-face, and therefore the original design for PINLEDs must be reexamined. There are a number of possible ways in which the original design can be modified to better accommodate N-face nanowires. All of these modifications must deal with a central problem: making contact to the p-type bottom half of the nanowires. P-type GaN is notoriously difficult to make ohmic contact to given the large band gap and electron affinity of GaN. Ni is predominately used to make ohmic contact to p-GaN because of its large work function. Unfortunately, it is difficult to form Ni contacts to the bottom of nanowires without using a complicated “flip-chip” device fabrication technique in which nanowires are removed from the substrate exposing their bases. If possible, this type of processing should be avoided, as perfecting the flip-chip technique is not a trivial task, and quite time consuming.

The question then becomes, how does one make good contact to p-GaN nanowire bases without removing the nanowires from the substrate? There are two main ways to approach this question. One approach is to try and find an
appropriate substrate to grow the PINLEDs on. Because catalyst-free nanowires
grow on a wide variety of substrates, including amorphous substrates[14], there
are many options for substrates that could offer good electrical contact to the p-
GaN nanowire base. A second approach is to insert a section of n-GaN with a
tunnel junction at the base of the nanowires. The n-GaN would have good
alignment with n-Si and the tunnel junction will act as a carrier type inverter
between the n-GaN and p-GaN. Tunnel junctions have been extensively studied
in planar III-nitride devices[100-103], so there are clear paths to implementing
such devices in nanowires. While the second approach is quite promising,
investigation into this area is still in its very early stages and will not be covered
in this text. Much more work has been put into the first approach, so that will be
the main focus of this chapter. Once this is covered, some more general
modifications to the original PINLED design are covered.

6.1 Optimizing p-down PINLEDs on p-Si

The first and simplest step towards developing a new substrate for N-face
PINLEDs is to abandon n-Si substrates for p-Si. N-Si is an obviously bad choice
for p-down nanowires as the overall device that is formed is n-p-n (as discussed
in the previous chapter). With this design, when one p-n junction turns on, the
other is reversed biased and therefore restricting current from passing through
the nanowires. If p-Si is instead used, the overall devices becomes p-p-n. This
should show a great deal of improvement compared to n-Si. However, p-Si is not
a perfect substrate given that there is a large barrier in the valence band at the p-Si/p-GaN interface. A band diagram for an N-face PINLED grown on p-Si is shown in Figure 6.1. This diagram does not include an active region, as it is only meant to demonstrate the presence of the barrier at the p-Si/p-GaN interface.

Figure 6.1: Band diagram for an N-face PINLED on a p-Si substrate.

This barrier will certainly have a detrimental effect on device performance, but as was stated earlier, it is difficult to make contact to p-GaN in general. So while there may be other better possibilities available, p-Si is not unlike other materials in that its band alignment with GaN does not allow for perfect ohmic conduction to p-GaN. With those downsides in mind, it is important to reiterate all the reasons Si was chosen as a substrate in the first place. Si wafers are relatively inexpensive, they are widely available in large sizes, and are manufactured with incredibly high material quality. Perhaps even more importantly, all of the experimental work discussed in the previous chapters was done on Si wafers, and is not directly applicable to other substrates. For all of these reasons, it is
prudent to first explore p-down PINLED designs grown on p-Si before other substrates are investigated.

To determine what kind of device characteristics are possible for p-down PINLEDs grown on p-Si, a series of samples with different graded base lengths was grown. The p-down samples in this series were identical to one another, other than their different graded base lengths. The graded base lengths were varied from 25 to 200 nm. By grading over shorter base lengths, the amount of polarization-induced charge is increased in the p-type region. This should have a number of beneficial effects on performance. First, by increasing the carrier concentrations in the p-region, the overall series resistance of the device should reduce, thus also allowing for turn-on at lower voltages. Second, higher carrier concentrations will lead to a reduction in the depletion region at the p-Si interface, as well as a reduction in the depletion region at the center of the nanowire due to the p-n junction. In the case of the former, a reduced depletion width will make it easier for holes to tunnel into the p-GaN valence band from the Si valence band. In the latter, a thinner depletion region will make it easier for holes to tunnel into the device active region. Both of these effects should lead to lower turn-on voltages for shorter graded base lengths. A schematic showing what the four samples with different graded base length might look like are shown Figure 6.2.
These samples are processed using the normal procedures for PINLED devices (Appendix B). EL was measured from the device with a graded length of 100 nm (Figure 6.3). Emission from this device has a wavelength of 355 nm. This is consistent with emission from the device’s GaN multiple quantum well active region. Confinement in the thin GaN QWs (nominally 5 nm thick) leads to emission shorter than the GaN band gap. Plotting emission wavelength as a function of current shows the same red shift seen in earlier PINLED devices, as expected.
Figure 6.3: A) EL spectra as a function of current for a p-down PINLED device grown on p-Si(111) substrates. B) The change in peak wavelength and LE intensity as a function of current in the device.

In the measurements taken here, the emission wavelength has not yet reached a steady value, indicating that at higher currents more screening of polarization charge should occur and emission should continue to blue shift.

The electrical characteristics of all four samples in this series are shown in Figure 6.4. These J-Vs show that, as expected, the sample with the shortest graded base (25 nm) turns on at the lowest voltage. A separate plot of the voltage needed to obtain certain current densities (1, 50, and 100 A/cm²) as a function of base length shows that the voltage needed to obtain a specific current reduces as base length is shortened (Figure 6.5A). A plot of series resistance (determined by the differential resistance at high voltages) as a function of graded base length (Figure 6.5B) shows that series resistance is roughly constant for different base lengths.
Figure 6.4: Linear scale J-Vs for PINLED devices grown with different graded base lengths.

This implies that the resistance of the p-type layer does not dominate the series resistance. Somewhat interestingly, the trend in Figure 6.5A indicates that grading over a length less than 25 nm could further reduce turn-on voltage. At the time of writing, such a sample has not been grown. Nevertheless, the data in Figure 6.5 already shows a clear reduction in turn-on voltage, consistent with a reduction in the depletion widths within the p-type region of the device. This shows that it is possible to engineer the polarization in PINLED devices to improve device characteristics, a step which had not been previously taken until these samples were grown.
Figure 6.5: A) Voltage needed to achieve a certain current density and B) series resistance for PINLED devices grown with different base lengths.

After some optimization of p-down PINLEDs on p-Si, one might ask how these devices compare to the previous design that uses Ga-face (p-up) nanowires. Unfortunately, at the time of writing the p-down devices with different base lengths have primarily been electrically characterized, making it difficult to discuss emission from these at this time. In lieu of a comparison between p-down and p-up device designs, the performance of p-down devices is instead compared to the published characteristics of other UV LEDs. Figure 6.6 plots the average turn-on voltage for select UV LED devices from the literature[104-115] and deep UV LEDs currently available from the company SETi[116]. The results show that as traditional LEDs are pushed to shorter wavelengths, the turn-on voltage increases. So while the turn-on voltages for the PINLED described here might not compete with traditional LEDs that emit near the GaN band gap, it is
more likely that they could be comparable to traditional devices that emit in the deep UV.

![Graph showing turn-on voltage as a function of emission wavelength](image)

Figure 6.6: Turn-on voltage and as a function of emission wavelength for traditional UV LEDs published in the literature[104-115] and commercially available devices [116] compared to the turn-on of p-down PINLEDs on p-Si.

The current commercially available devices that emit near 250 nm turn-on near 6 or 7 V. If the turn-on voltage for p-down PINLEDs on p-Si can be maintained near its current value (~7.5V) as wavelength is pushed towards shorter wavelengths, then these devices might be able to compete with traditional UV LEDs. Of course, if the turn-on voltage could be reduced further this would make the PINLED devices even more competitive with other devices. An alternative to growing on p-Si substrates that might reduce turn-on, namely growing on metal substrates, is covered in the following section.
6.2 Metal Substrates as an Alternative to Si

While the results of the previous section showed improvement in device performance by engineering polarization charge, there might be other substrates that could replace p-Si and lead to even better performance. This section explores the possibility of using other substrates in place of Si. The main alternative to Si discussed here is the use of metal substrates. The use of metal substrates is only possible because catalyst-free nanowires grow on a wide variety of substrates, and it would be nearly impossible to do so using thin film-based devices. If the appropriate metal substrate were chosen, then depositing PINLEDs on top of the metal would amount to essentially growing the devices directly on top of its p-type contact. As mentioned previously, metals with large work functions are preferred for use in ohmic contacts to p-GaN. Ni is commonly used for its large work function, so it would seem to be the natural choice for use as a metal substrate. However, introducing new metals into an MBE chamber is a risky endeavor, so by introducing Ni one runs the possibility of contaminating the system which could have a large deleterious effect on other samples grown in the system, not just the samples formed on Ni. This is especially the case with Ni, as it has been previously shown that even a small concentration of Ni (<1 atomic %) can have a large deleterious effect on the characteristics of GaN[80]. The vapor pressure of Ni at growth temperatures is also larger than other metals that are already introduced into the growth chamber and considered safe, for example, Ti[117], although it is something of a judgment.
call as to how much higher Ni’s vapor pressure would need to be in order for it to be considered unsafe. With these concerns in mind, refractory metals then stand out for use as substrates. Metals such as Mo and W are commonly used in MBE components, so there is no risk of contaminating an MBE system by introducing either of these metals as a substrate. These metals also have relatively high work functions, so they might provide good contact to the p-down nanowires. Of the two, Mo was pursued for use as a substrate because it is generally and easier metal to work with than W.

Two types of Mo substrates were considered. First, Mo foil was procured from a commercial vendor, with the hopes of growing nanowires on the foil. Unfortunately, polishing these foils to achieve atomically smooth surfaces is something of a difficult process. To our knowledge, atomically smooth, polished Mo foils are not commercially available. Therefore, before growing nanowires on the foil, steps must be taken to polish the foil. The foil was electropolished using a mixture of methanol, sulfuric acid, and hydrochloric acid. Images of the foil before and after polishing are shown in Figure 6.7. AFM images of the polished substrate are shown in Figure 6.7 as well. The smoothest sample had an RMS roughness of 2.3 nm. While this roughness may be small enough to deposit nanowires on top of and use in devices, the difficulty in machining and polishing the substrates made this approach to Mo substrates prohibitively time consuming, and therefore a second approach was taken.
A more promising approach to Mo substrates is to evaporate Mo onto existing atomically smooth substrates and then grown on top of the deposited layer of Mo. Thin layers of Mo were deposited onto both Si and sapphire substrates. This provides a much simpler technique to form atomically smooth Mo substrates. However, using Mo coated Si and sapphire wafers comes with some difficulties. In initial growths on Mo coated Si, the normal substrate treatment was used when the sample was put into the chamber. For bare Si wafers, this includes a high temperature step where the substrate is taken to ~1000°C to remove the thin oxide from the surface. When the Mo coated Si wafer was taken to this high of a temperature, the Mo delaminated from the Si surface (see Figure 6.8). Nanowires still formed on the surface, even though the Mo layer was rippled and uneven.
In subsequent growths, substrate temperatures above the sample’s growth temperature were avoided. However, even heating the substrate to lower temperatures has some effect on the Mo layer. In Figure 6.9, AFM images are shown from samples of Mo coated Si taken to different temperatures in the MBE system’s bake station. As can be seen, the as-deposited Mo film has a low roughness, and would be perfect for growth, as is. However, when heated the Mo substrate roughens. This could be due to grain growth or recrystallization in the Mo layer. This roughening led to many nanowire samples that were too rough to be used in devices. To avoid this, thinner layers of Mo (10 nm thick instead of 50 nm) were used to coat the Si. Nanowire samples grown on thinner Mo were less rough and could be used in devices.

Several proof of concept PINLED samples were grown and fabricated on Mo-coated Si substrates. The EL from one such device is shown in Figure 6.10. As can be seen from this figure, the EL intensity initially increases with an
increase in current, however a maximum intensity is reached at the relatively low current of 30 mA.

![Image](image.png)

**Figure 6.9:** Mo-coated Si substrates as-deposited and after a bake of 800°C for one hour.

This is peculiar, as most previous PINLED devices show increases in EL up to much higher currents. The peak wavelength of this EL comes at roughly 410 nm. This specific device has a GaN MQW active region which should emit near 365 nm. The discrepancy between the two is possibly due to a relatively low percentage of overall current being injected into the device active region. With only a small amount of current making it into the active region there will be less screening of the polarization-induced charge in the QWs (as described in Chapter 4), meaning the emission will be red shifted compared to what would be expected under flat band conditions.
Figure 6.10: EL from a p-down PINLED device grown on a Mo-coated Si substrate.

These issues aside, to our knowledge, this device and the EL measured constitutes the first time that a nanowire-based LED has been formed on a metal substrate. This allows for the possibility of using thin metal layers deposited onto a wide range of substrates, perhaps glass, that can potentially be available in much larger areas and more cost-effectively than substrates traditionally used for III-nitride based LEDs (namely, sapphire).

Once devices have been fabricated on Mo substrates, it is natural to compare their performance to those formed directly on p-Si. The use of alternative substrates to p-Si was primarily driven by a desire to improve the electrical characteristics of p-down devices, specifically lowering turn-on voltage. To compare the electrical characteristics of the same device grown on p-Si and
Mo-coated Si, I-V’s for both devices are shown in Figure 6.11. This data shows that the turn-on voltage is lower for devices grown on p-Si (12.6 eV compared to 13.6 eV on Mo). However, the series resistance for the devices fabricated on Mo-coated Si is higher than the series resistance for the p-Si device. This increase in series resistance will push out the turn-on voltage for the devices on Mo, and could be responsible for the higher turn-on voltage in these devices.

![Graphs showing J-V characteristics](image)

Figure 6.11: Linear and semi-log scale J-Vs of p-down PINLEDs grown on p-Si substrates or on Mo coated Si substrates.

Therefore, these initial results point towards p-Si being a better substrate than Mo coated Si, but this is not conclusive. Further experiments with different thicknesses of Mo (the I-V in Figure 6.11 correspond to devices grown on 10 nm thick Mo) or perhaps Mo on different substrates (I-V’s here correspond to Mo on n-Si, Mo-coated p-Si could improve performance).
6.3 Further Optimization of PINLED Design

The previous two sections have dealt with modifications to the original PINLED design in order to take advantage of N-face nanowires. The N-face polarity of nanowires is a problem for the original PINLED design that must be addressed; however, there are a number of other modifications that can be made to further optimize PINLED operation, even if they do not specifically address the issue of N-face polarity. These secondary modifications will be the topic of this section.

One simple modification that can be made to the PINLED design is to reduce the highest Al composition of each graded layer on either side of the device active region. Currently, both the bottom section is graded from GaN to AlN, and the top is graded from AlN to GaN. This means that AlN is present on either side of the device active region. This has some benefit as the wide band gap of AlN will provide a large amount of confinement for whatever QW is included in the center of the nanowire. However, there is a drawback to having AlN on either side of the active region, which is shown schematically in Figure 6.12. During growth, a shell of AlN forms on the nanowire because of the different rates of lateral incorporation between GaN and AlN (as discussed in Chapter 2). This shell should act as a passivation layer for the nanowires and help reduce surface recombination. But this occurs primarily because the
material through the center of the nanowire (i.e. compositionally graded AlGaN) has a lower band gap than the AlN shell.

Figure 6.12: Schematic showing the benefits of grading the top and bottom sections of the nanowires to AlGaN instead of AlN.

This is true everywhere except for the material directly adjacent to the nanowire active region. In these sections, there is no change in band gap along the radius of the nanowire, which will make it more likely that carriers will move laterally towards the nanowire surface. The ensuing surface recombination will then prevent some carriers from being injected into the active region. To prevent this and increase injection efficiency, the n-type and p-type sections should be graded to some composition of AlGaN that still allows for a great deal of confinement in the QW (in the vertical direction), while also having a lower band gap than the AlN shell (in the lateral direction). The exact composition each layer
should be graded to will need to be established experimentally and in part will depend on the composition of material in the QW. By doing this, PINLED efficiency should increase.

A second change that can be made to the original PINLED design is a switch to using polarization-matched InAlN QWs in place of AlGaN. The benefits of polarization-matched devices were described by Jena et al. [118]. By using AlGaN in both the graded nanowire sections and the QW active region, there will always be some polarization induced sheet charge at the interface between the QW and the graded sections due to the change in spontaneous polarization on across the interface. This sheet charge leads to a distortion of the bands in the active region, leading to separation of electrons and holes at either side of the QW. All PINLED devices exhibit evidence of this distortion in the form of red-shifted emission under low current injection conditions. But if InAlN is used in the QW instead of AlGaN, then the possibility exists for there to be no change in polarization density on either side of the graded layer/QW interface. The correct composition of InAlN to use in the center of the nanowires depends on the composition of AlGaN that the n- and p-type sections are graded to and the strain state of the InAlN QW. A band diagram showing a PINLED design with a polarization-matched InAlN QW is shown in Figure 6.13. In this design, Al$_{0.6}$Ga$_{0.4}$N is present on either side of the InAlN. The InAlN layer is assumed to be relaxed and has a composition of In$_{0.25}$Al$_{0.75}$N. While there will be some challenges in growing InAlN within AlGaN nanowires because alloys
containing In generally need to be grown at lower temperatures, using InAlN QWs should lead to increased PINLED device performance.

Figure 6.13: Band diagram for a PINLED using a polarization-matched InAlN QW.

Finally, to improve PINLED device performance, nanowires grown on patterned substrates should be used instead of self-assembled nanowire growth. Self-assembled nanowires have many attractive attributes, and even though it is possible to control the average attributes of the nanowires by manipulating growth conditions (as described in Chapter 2), the resulting nanowire characteristics still fall within some distribution. This means that even if an ensemble of nanowires on average has the optimum characteristics for a PINLED (e.g. thickness of QW, nanowire radius, graded section lengths, etc.), some of the nanowires in the distribution will deviate from the optimal
parameters. It has been repeatedly shown that using patterned substrates can lead to much better uniformity than what is possible with catalyst-free nanowires. Some examples of nanowires grown on patterned substrates are shown in Figure 6.14[119, 120]. With this increased control, it should be possible to grow a greater portion of nanowires in a given sample that exhibit optimal characteristics, which should lead to better device performance. Of course, using patterned substrates has its downsides.

First, preparing the substrates can be quite costly, as the patterns are usually formed using electron beam lithography. Second, it will not be possible to take conditions optimized for deposition on bare Si wafers and apply them for use with patterned substrates. Therefore, some experimental effort must be spent simply determining the proper conditions for nanowire deposition. That being said, it is
the author’s belief that at some point in the switch to growing on patterned substrates will eventually happen. In the short term, it would most likely be best to work of optimizing the PINLED heterostructure design using catalyst-free nanowires, while in parallel working on better understanding growth on patterned substrates.

In this section, a number of modifications to the PINLED design have been put forth. This list is by no means comprehensive, but rather should be taken as the author’s perspective on how this project should best move forward.
Chapter 7
Conclusions

This dissertation has covered a wide range of topics, all dealing with the growth of catalyst-free nanowires grown by PAMBE. First, to gain control of nanowire formation, growth maps were created that relate specific nanowire characteristics. A two-step growth technique was established that uses the growth maps as a guide to manipulating conditions such that growth kinetics and nanowire formation can be tuned to achieve target structures. This was used to form both vertical and coaxial AlN/GaN heterostructures.

With the control of nanowire formation established, our attention turned to nanowire-based devices. Coaxially oriented AlN/GaN nanowire resonant tunneling diodes were fabricated. These devices exhibit exceptionally high peak current densities, and to my knowledge, they are the first ever coaxially-oriented III-nitride nanowire devices grown by PAMBE.

Polarization-induced nanowire light emitting diodes (PINLEDs) were also discussed. The necessary background on polarization in the III-nitrides, design of PINLEDs, their growth and characterization were all provided. These devices have already been shown to emit light into the deep UV portion of the electromagnetic spectrum, and could potentially be pushed to even shorter...
wavelengths. Additionally, we have fabricated dopant-free p-n junctions that rely solely on polarization-induced charge for the formation n-type and p-type layers. These devices show the potential power of polarization-induced doping in III-nitride nanowires.

However, many challenges still remain to improving PINLED device performance. A major first step came when it was established that PINLED nanowires grow with a mixture of material polarity. A wide range of characterization techniques (etch studies, SEM, STEM, and C-AFM) were used to show that the majority of nanowires grow with an N-face polarity, while roughly 10% of the nanowires are Ga-face. This mixture of polarities was used to show ambipolar EL from dopant-free PINLED devices.

Since most nanowires are N-face, the PINLED design must be modified to make better use of the N-face material polarity. Optimizing PINLEDs grown on p-Si substrates, as well as exploring the use of metal substrates in place of Si were discussed. Additional modifications to the PINLED structure were proposed, including the use of polarization-matched InAlN QWs, grading to lower % Al, and switching from self-assembled nanowires to nanowires grown on patterned substrates. Implementing these changes should lead to increased PINLED performance.

Having summarized the work included in this dissertation, it is now an appropriate time to take a broader (and brief) view of what it all means. In Chapter 1, it was stated that the goal of this work was to push the boundaries of
what is possible in III-nitride devices through the use of nanowires. In other words, the goal was to use III-N nanowires to form devices that could not be made using thin films. But more than simply forming nanowire devices that cannot exist in thin film form as ends in themselves, we also focused our attention on applications in which current III-N technology can be improved. The PINLED research demonstrates this well. Employing polarization-induced doping in graded nanowires could be viewed as interesting in and of itself. But it is the fact that UV LED efficiency in traditional nitride devices is still low, coupled with the exploitation of nanowire strain accommodation to produce polarization-induced doping with high material quality that makes the PINLED work particularly interesting. It is the author's sincere hope that because of this balance between novelty and utility, this work will be viewed as a success, and that future research in this area will continue with this balance in mind.
References


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Appendix A: MBE Growth Details

This appendix provides further details concerning the growth of samples by PA-MBE.

All samples in this work are grown using a Veeco 930 PAMBE system on n-type Si (111) substrates. Prior to growth, Si wafers are cleaned using a standard solvent clean (5 min. Acetone, Methanol, Isopropanol in ultrasonic). Samples are loaded into the system’s load lock, and baked at 200°C for between one and four hours. Next the wafers are baked in the system’s buffer chamber for 1 hour at 800°C. After these preparation steps are taken, the substrate is loaded into the growth chamber. Once loaded into the growth chamber, a short bake of 600°C for ten minutes is performed with the substrate facing the back of the growth chamber (i.e. an index of 180°). The native oxide is removed by heating the substrate to 1000 °C for one minute in the growth position. When the sample is at these high temperatures, a streaky 1×1 reflection high energy electron diffraction pattern out emerges from a diffuse background. The sample is then cooled from this high temperature to growth temperatures. While it is cooling, the 1×1 pattern changes to a 7×7 pattern, further indicating that the native oxide layer has been removed. Substrate temperature is monitored using an optical pyrometer that faces the growth position. All temperatures are measured before the nitrogen plasma is lit, as previous work has found that the temperature
reading by the pyrometer changes when the plasma is lit. Therefore, if multiple temperatures are used during growth, they all must be measured before lighting the plasma. To do this, the thermocouple setting is adjusted until the appropriate pyrometer reading is reached. The correct thermocouple setting for each temperature is recorded, so that the correct temperatures can be set during the growth.

Standard effusion cells are used for the Ga and Al sources. Active nitrogen is supplied by a Veeco radio frequency plasma source. Beam fluxes are measured using a nude ion gauge at the substrate position. The plasma source is operated at 350 W using a constant N\textsubscript{2} flow rate supplied by a mass flow controller. To ensure that the flow of nitrogen is the same from growth to growth, the mass flow controller setting is adjusted to reach the same chamber pressure (2E-5 Torr) before the plasma is lit. Plasma is lit by first setting the power to 50 W, and the reflected power is optimized. The power is then set to 350 W. Early work with Si substrates showed that the Si surface becomes nitridated once the N plasma is lit forming a thin layer of SiN on the surface, which makes the 7×7 pattern transition to a diffuse image. This occurs even when the nitrogen shutter is closed due to unintentional leakage of active nitrogen around the plasma shutter. To minimize this unintentional nitridation, all samples are grown with the substrate first pointed 180° from the N source during which time the plasma is lit. When this is done, the 7×7 pattern is still apparent when the sample is rotated into the growth position, even if the plasma has been lit for an extended amount
of time. However, once the sample is in the growth position, it will begin to nitridate. Therefore, growth of nanowires is started immediately once the substrate is in the growth position.

To provide an accurate measure of the III/V flux ratio, a series of samples are grown using a variety of Ga fluxes and a constant supply of active N. We have grown these samples on a number of substrates and temperatures. GaN calibration samples have previously been grown on either AlN or Si(111) substrates, with little difference found between the two. AlN has been grown on Si(111) and GaN templates. When grown on Si(111), the AlN growth results in thick layers of AlN with nanowires protruding from the top of the thin film’s surface. Therefore, GaN templates are preferred for the AlN calibration. InN calibration samples have only been formed on Si(111) substrates. For GaN and InN calibration samples, substrate temperatures below GaN (InN) decomposition and Ga (In) desorption should be used, to ensure that all of the material impinging on the substrate is incorporated into the resulting layer. Cross-sectional scanning electron microscopy (SEM) of each sample is used to determine the thickness of the layer, and hence the growth rate of the film at a given flux. From low group-III fluxes, the growth rate is linear with the impinging metal flux, denoting the metal-limited (N-rich, III/V < 1) growth regime. For high metal fluxes the growth rate is constant, denoting the N-limited (metal-rich, III/V >1) growth regime. The Ga flux at which these growth rates intersect is the stoichiometric point (III/V = 1), which is used as a reference point to convert
group III fluxes to their appropriate III/V ratios. It should be noted that from
growth to growth the N-limited growth rate changes. Values in the range of ~250.
to ~310 nm/hr. have been observed previously. After the system openings, the
N-limited rate seems to be stable until the next opening. This being said, the
change in N-limited growth rate has not proven to have a large effect on
nanowire formation. This is most likely due to the III-limited growth of the
nanowires.
Appendix B: Processing Details

This appendix details all of the steps used to process PINLED samples. This basis for these steps was originally given to me by Andrew Carlin and Krishna Swaminathan when they were PhD students in Steve Ringel’s lab in the ECE department. The original recipes were modified to fit the specific needs for my nanowire-based devices. I should note that the steps here are in no way optimized. They were only developed to get the PINLED devices to work, not to maximize performance. This means I tweaked the recipes until I found something that was reproducible and worked well enough. Future PINLED work will likely have to optimize these processing steps to increase device performance.

First, here are the steps needed to form a simple thin metal top contact for a PINLED device:

1. Dehydration bake of sample at 120°C on hot plate for 5 minutes.

2. Place sample on spinner and solvent clean with Acetone, Methanol, and Isopropanol. To do this, start the sample spinning and spray it with each of the solvents listed for approximately 10 seconds. To make sure that you don’t let the Acetone dry on the surface, starting spraying Methanol before you stop spraying the Acetone. Then when you do stop spraying Acetone, continue spraying the Methanol.
3. Spin on AZ 5214 at 5000 rpm at 6000 rpm/s for 40s.

4. Soft bake on hot plate at 100°C for 1 minute. Usually if multiple samples are being processed at once, the samples are put onto and taken off of the hotplate in a staggered fashion to save time. That is, if three samples are being processed, put samples on and take them off in increments of 20 seconds.

5. Exposure with desired pattern for 2 second.

6. Bake for 35s on hotplate at 130°C. This bake needs to be much more accurate, so only one sample at a time if put onto the hot plate.

7. Flood exposure for 19s. That is, expose the entire sample without a mask.

8. Develop using MF319 for 50 seconds and then dip in DI water for about 10 to 15 seconds.

9. Use the Dreese evaporator to deposit 10nm Ni, 20nm Au contacts. This metal layer is thick enough to make contact to the NW tops, but not so thick that it absorbs all of the light. When the sample is loaded into the chamber, place it along the outside of the plate so that there is a slight angle to the incoming flux of material. Though this has never been tested, the fear is that is the evaporated metal impinges without an angle it can get between the nanowires and form a short to the Si substrate.

10. Liftoff with Acetone in ultrasonic (a couple of minutes in ultrasonic) and dip in DI to rinse.
For some nanowire samples, a contact pad was used to make contact to the thin metal window. Those devices require three photolithography steps and two metallization steps. The first photolithography step uses hard baked PR as an insulating layer. A mask is used to leave open areas in the PR that thin metal is then deposited on top of. To hard bake the PR, put it on a hot plate with a temperature of 200°C for 20 minutes. This bake should make the PR resistant to removal in Acetone. After this, use the previously described steps and a second mask to deposit a thin metal layer on top of the windows exposed in the PR. Finally, use a third mask to deposit a thick Au contact pad that makes contact to the thin metal layer. In the past, sections of the contact pads have come off during the lift off step. To prevent this, use a thin layer of Ti before the Au to increase adhesion of the contact pad. This means the contact pad should consist of roughly 10 nm Ti, 200 nm Au. If desired, the thickness of the Au layer can be increased to reduce contact resistance.
Appendix C: Miscellaneous Nanowire Growth Results

This appendix discusses some nanowire growth results that the author feels are too preliminary to include in the main text of the thesis, but should still be included because they bring about interesting questions regarding catalyst-free nanowire growth. First, a series of two-step samples were grown with short nucleation times. These results show that small changes in nucleation time can have an enormous effect on the resulting nanowire properties, even if the amount of growth time is held constant between samples. Second, SEM images of two plain GaN nanowire samples grown on Mo coated sapphire substrates are shown. These nanowires have a much different morphology from what is usually seen when nanowires are grown on Si(111) substrates. The exact reason for this difference is not clear, but some possible explanations are provided.

C.1 Two-step samples with short nucleation times

A series of four samples were grown using the two-step growth procedure described in Chapter 2 using a variety of nucleation times. In most previous results, the nucleation step of the two-step process had a duration of 22.5 minutes, but in the samples described here, shorter nucleation times (between 3 and 15 minutes) are used. All samples were nucleated at a substrate temperature of 765 °C. The growth step is the same for all samples; 45 minutes
of deposition at an elevated substrate temperature of 780 °C. The original idea for this series of samples was to push the density of nanowires to progressively smaller values, and see if the two-step growth technique still worked at such low densities. SEM images of the samples were used to determine nanowire areal density, average height and average radius. Density as a function of nucleation time is shown in Figure C.1 below.

![Figure C.1: Areal density of GaN nanowires grown with a variety of nucleation step times using the two-step method.](image)

As expected there is a clear trend that nanowire density increases as nucleation time increases. Perhaps somewhat surprisingly, while the nanowire density is exceptionally low when a 3 min. nucleation time is used, there are still some nanowires on the surface (i.e. a non-zero nanowire density).
Average radius and height vs. nucleation time are displayed in Figure C.2. First, notice that the average radius does increase as a function of nucleation time. This might seem to contradict the results from Chapter 2, but they are in fact consistent with what was previously stated. In the initial work on two-step samples, we showed that average radius remains roughly constant as growth time is increased. This means that when the two-step method is used, radius does not increase during the growth portion of the deposition. But this does not mean that radius should not increase during the nucleation step, which is shown in Figure C.2. This means that if one wanted to control radius and the exact density of nanowire was somewhat flexible (i.e. it had to be low, but no specific value was needed), then different nucleation time lengths could be used to control average radius. This could be a useful tool for growing low density nanowires with exceptionally small radii.

Along with this useful aspect of short nucleation times comes a rather strange results regarding the average nanowire heights for longer nucleation times (Figure C.2). The sample with the shortest nucleation time has an average height of 90 nm. There is a clear trend that as nucleation time is increased, so does average height, since in this extra nucleation time the nanowires that have nucleated will continue to grow taller. However, what is quite surprising is that the sample with the longest nucleation time (15 minutes) has an average height of 183 nm. This is more than double the average height of the sample with the shortest nucleation time, even though the total difference in growth time is only
12 minutes. Growth during this 12 minutes alone cannot explain the large difference in heights because if it were responsible for the difference in height, the nanowire growth rate during this twelve minutes would need to be 7.75 nm/min. This is well above the N-limited growth rate (~5 nm/min.). Growth exceeding the N-limited growth rate would require a substantial amount of N atoms diffusing up the nanowire sidewalls and onto the nanowire tops, which is generally not believed to occur during nanowire growth. Therefore, the large difference in height cannot be attributed simply to a longer overall deposition time.

![Graphs](image)

**Figure C.2:** A) Average nanowire radius and B) height as a function of nucleation time.

A more likely possibility is that the difference in average heights might be due to some effect that is at play during the entire deposition of the nanowires. A
small effect that boosts the vertical growth of certain nanowires over the entire deposition could explain such a large difference between samples with different nucleation times. While an effect such as this is possible, it is difficult to see what might provide it. If anything, the most obvious changes that occur during nanowire vertical growth rate would seem to favor higher vertical growth rates for nanowires with shorter nucleation times. As stated in Chapter 2, nanowire height should decrease as radius increases, but Figure C.2 shows that radius is larger for longer nucleation times. This would suggest that nanowires will have a lower vertical growth rate if nucleated for longer times, due to an increase in radius.

The fact that the opposite trend is seen is perplexing, and puts us further away from understanding how longer nucleation times leads to nanowires that are so much longer than the other samples with only very slightly shorter nucleation times. We are left then to look for effects that can change vertical growth rates that have not been discussed to this point. For example, perhaps higher nanowire density increases vertical growth rate? This is unlikely, given that with more nanowires nucleated on the surface there is more competition for adatoms on the surface.

The most likely explanation is that after 3 minutes of nucleation time, very few nanowires have nucleated on the surface, and therefore the extremely small number of nanowires that are measured on the surface after growth actually nucleated sometime during the high temperature step (i.e. the growth step). At higher temperatures, nanowires are much less likely to nucleate, which means
any nanowires that do nucleate would have taken longer to do so. In the samples nucleated at longer times, the nanowires that have already formed in the nucleation step continue to grow throughout the entire high temperature step. This would make it appear that the vertical growth rate is larger for these nanowires formed with a longer nucleation steps. In an attempt to show this graphically, histograms of nanowire height for different nucleation times are shown in Figure C.3 below. Certain features of the plots in Figure C.3 should be noted. First, for the sample with a 15 minute nucleation time, there is a clear group of nanowires with heights centered near 230 nm that looks somewhat like a Gaussian distribution along with a clear tail of nanowires with shorter heights. If the explanation above is correct, the group of nanowires that formed during the initial nucleation step are found in the group centered near 230 nm. The tail of shorter nanowires is most likely due to nucleation occurring during the high temperature step of deposition. In the sample with the shortest nucleation time, there is no clear group of nanowires with similar heights, only a very wide dispersion of nanowires at the smaller nanowire height. This supports the idea that no nanowires have formed during the nucleation step of deposition in 3 minutes, and all of the nanowires found in this sample were due to limited nucleation during the high temperature step.
While these results support the hypothesis for the formation of nanowires with vastly different heights resulting from relatively small changes in deposition, further work would need to be done to more fully understand these samples. A sample should be grown that has no nucleation step, and instead only involves deposition at 780 °C for 45 minutes. If this sample showed similar results to what was seen in the sample with the shortest nucleation time, then this would further support the explanation provided. Future work in this area could be useful to more fully understand the limitations of the two-step method. However, while initial research goals pushed us to grow nanowires with low densities, more recent work has moved away from using low density nanowires. Therefore, it is not clear how much would be gained by pursuing this line of research further.
C.2 Nanowires on Mo coated Sapphire substrates

In Chapter 6, the use of Mo coated Si substrates as an alternative to bare Si\(\text{111}\) substrates was discussed. In addition to the work that was described there, we have also pursued growing nanowires on sapphire wafers coated with sapphire. Only two samples were grown on Mo coated sapphire (although a third was attempted, but failed when the sapphire wafer broke apart at high temperatures in the MBE chamber before growth was initiated). The idea behind using Mo on sapphire was to put a thin layer of conducting materials on top of a substrate that is transparent to UV light (such as sapphire). The metal layer would be used to make contact to the base of the nanowires, but also be thin enough to avoid absorbing a large portion of the UV light emitted in that direction.

The samples described in this section were grown on sapphire wafers that had a 5 nm thick layer of Mo deposited on top of them. The back side of the sapphire wafer was coated with a thick coat of Ti to aid in absorbing infrared light from the CAR heater. Each sample was grown for one hour. As with other samples, an infrared pyrometer was used to determine the temperature of the substrate. Based on previous calibrations in our group for growth on Ti backed sapphire substrates, an emissivity of 0.53 was used instead of the normal emissivity of 0.67 (calibrated for Si). Because these samples were meant only to find the appropriate conditions for nanowire growth, PINLEDs were not formed, but instead only p-GaN was deposited.
SEM images in cross-section from these samples are shown in Figure C.4. The sample grown at a higher temperature shows the clear formation of nanowires, while the sample grown at lower temperatures consists of a thin film of material. This is consistent with the broad temperature range for nanowire growth expected for nanowires formed on Si. However, the nanowires that formed on Mo coated sapphire at 700°C have a much different morphology compared to nanowires on Si. The heights of the nanowires grown on Mo coated sapphire are strikingly uniform, with very little deviation from nanowire to nanowire. The average radius is also much larger.

Figure C.4: GaN:Mg nanowires grown on Mo coated sapphire substrates at different substrate temperatures.

Comparing the nanowires grown at 700°C and the thin film grown at 650°C reveals some interesting facts about the nanowire sample. First, the average height of the nanowires (143±4 nm) is nearly twice the thickness of the thin film (78±4 nm). This is expected, since the movement of Ga adatoms to the tops of the nanowires should increase vertical growth rate. If we use the density,
average height, and average radius of the nanowire sample (as determined by SEM image analysis), we can calculate the equivalent thickness of 2D material formed in this sample, which is 65±18 nm. The large error in this number is due to a large error in the average nanowire radius (59±11 nm). Given that the difference between the nanowire equivalent thickness and the actual thickness of the thin film sample is not statistically significant, we can use this as a sign that the nanowire sample is formed at a substrate temperature below the onset of Ga desorption and GaN decomposition. This is promising, since it provides evidence that the measured temperature of 700°C is reasonably accurate. After all, Ga desorption and GaN decomposition begins at substrate temperatures not much higher than 700°C.

It is unclear that future work will be committed to forming nanowires on Mo coated sapphire. However, if it is, there are a number of future experiments to perform. First, more samples under different growth conditions must be grown. The morphology of the nanowire sample shown in Figure C.4 most likely has too large of an average radius and too low of a density to be useful in PINLED based devices, so growth conditions need to be found in which more densely packed nanowires with smaller radii form. Second, in Chapter 6, we showed that growth on Mo coated Si wafers involves many challenges, mostly in the form of nanowire misalignment due to roughening of the Mo layer. The nanowires grown on Mo coated sapphire show no such misalignment. Quite the opposite, the nanowires seem to even better aligned than nanowire grown on bare Si. It is
unclear what is causing this. One possibility is that when Mo is deposited on sapphire or Si(111) it has a preferred orientation, and during growth this Mo layer prevents the formation of amorphous materials, which would normally form in the initial stages of deposition on bare Si(111). In this way, the Mo could strengthen the epitaxial relationship between the nanowires and the underlying substrate. However, it is unclear under what conditions the Mo will help and in what conditions it will hinder the formation of well aligned nanowires. To date, nanowires have been formed on Si substrates coated with 50 nm and 10 nm of Mo, and sapphire wafers coated with 5 nm of Mo. Clearly the nanowires grown on sapphire have the best alignment. This could be due to the lower thickness of the Mo layer on sapphire, or perhaps it could be due to some difference in the way Mo coats sapphire and Si. X-ray diffraction measurements of Mo coated Si and sapphire wafers with different thicknesses of metal could be used to determine if there is any difference in how Mo coats either of the two substrates, or if there is some change in Mo formation as layers get thicker. So while it is unclear if this line of research will be pursued further, it certainly offers a wide range of interesting materials questions that could be investigated further.