Analysis and Design of Wide Tuning Range Low Phase Noise
mm-wave LC-VCOs

Dissertation

Presented in Partial Fulfillment of the Requirements for the Degree
Doctor of Philosophy in the Graduate School of The Ohio State
University

By

Qiyang Wu, B.S., M.S.

Graduate Program in Department of Electrical and Computer Engineering

The Ohio State University

2013

Dissertation Committee:

Waleed Khalil, Advisor
Steven Bibyk
Patrick Roblin
Abstract

The growing demand for higher data rate in wireless transceivers continues to consume available bandwidth and move towards multi-band/multi-channel mm-wave systems to satisfy latest specifications and be compatible with legacy standards. One of the critical components, the LC-voltage controlled oscillator (LC-VCO), is required to have low phase noise while maintaining wide tuning range to achieve low bit error rates (BERs). Due to the large parasitic capacitance and high losses in silicon based technologies, extending the tuning range and reducing phase noise is becoming very challenging. This dissertation studies and proposes novel architectures and circuit techniques to overcome the limitations of high frequency LC-VCOs.

Different LC-VCO architectures are reviewed and the performance is summarized and compared. The components in LC-VCOs are theoretically analyzed and a prototype VCO is designed. An inductance redistribution technique to equally space sub-band coarse tuning characteristics is proposed and implemented. To predict the tuning range, a detailed analysis of the frequency dependent quality factor ($Q$) of the LC-tank is performed to characterize the tank loss. The frequency dependent $Q$ is used to size the transconductance ($g_m$) of the cross-coupled pair to satisfy the VCO startup condition. The relationship between the cross-coupled pair $g_m$ and the operating frequency is further derived.
To extend the tuning range, active negative capacitance (NC) circuits are investigated and integrated to bottom-biased and top-biased cross-coupled pair CMOS LC-VCOs in order to cancel the fixed parasitic capacitance in the LC-tank. Various NC circuits with low power consumption are designed and analyzed. A figure of merit (FOM) is proposed to compare the performance of different NC circuits. A power and area efficient NC scheme is then selected for mm-wave applications.

Applying the NC circuit to a bottom-biased mm-wave LC-VCO, the tuning range is increased with minimal impact on power consumption, silicon area or phase noise. The NC structure is further modified to be tunable based on switched varactors, enabling additional expansion of the bottom-biased VCO tuning range. By manipulating the quality factor \((Q)\) of the NC tuning varactor pair, a prototype VCO achieves a maximum tuning range of 27% in a 130 nm technology, while dissipating 13 mA from a 0.9 V supply. The tuning range is the highest reported to date at Q-band, covering from 34.5 GHz to 45.4 GHz.

A method of combining the tunable NC circuit and a top-biased VCO is also proposed and verified. A switched MOS transistor NC circuit is analyzed and demonstrated to have a wide tuning range. With this technology, the VCO achieves a maximum tuning range of 26% with worst-case phase noise of \(-100.1\) dBc/Hz at 1 MHz offset.

For VCOs in SiGe BiCMOS technology, combining NMOS and BJT cross-coupled pairs to reduce the sizes of transistors and current consumption is proposed and analyzed. The tuning range is improved by adopting small MOS transistors while the reduced BJT current lowers phase noise. To verify the results, a 37.8 GHz VCO is designed and fabricated with a 30% tuning range and an average phase noise
of −103.6 dBc/Hz at 1 MHz offset. The corresponding figure of merit with tuning (FOM\textsubscript{T}) is −193.5 dBc/Hz, which is the highest reported to date in Ka-band.
To my family
Acknowledgments

First, I give thanks to my parents. They have always been supportive and understanding, even when my research has reduced the frequency of contact with them. They let me know that I can make other people live better by becoming a scientist, rather than my initial dreams of being a medical doctor. Any success that I have today could not have been possible without them.

I am grateful to my advisor Professor Waleed Khalil for being a member of his research group and for his continuing support and guidance through my research, especially his unending patience with me to let me become a dedicated student. Through him, I have not only benefited from his wisdom and valuable advice, but also from his insight, experience and his high-standards in research, teaching, presentation and publication.

I would like to express my special appreciation to Tony Quach, Aji Mattamana, Pompei (Len) Orlando, Gregory Creech and Steven Dooley from the Air Force Research Lab (AFRL) for providing valuable support in design, silicon and PCB fabrication as well as funding this work.

My colleagues, Brian Dupaix, Samantha Yoder, Sidharth Balasubramanian, Salma Elabd, Sleiman Bou-Sleiman, Jamin McCue, Luke Duncan, Matthew Casto, Shahriar Rashid, Vipul Patel, Matthew LaRue, Wagdy Gaber, Moataz Abdelfattah, deserve
special recognition for offering me ideas, helping me and co-working with projects. They have been helpful with their comments and friendship.

I would like to thank all the teachers who taught me at the Ohio State University. They guide, support and inspire me. They provided me with invaluable knowledge throughout my study. At the same time, they created an exciting classroom environment and helped me with specific questions during their office hours without asking for any returns.

There are many friends who I met at the Ohio State University. I want to express my thanks to them, although I cannot list all their names here. They helped me in my studies and my life.

Finally, I thank the members of my dissertation committee, including Prof. Steven Bibyk, Prof. Patrick Roblin and Prof. Harris Kagan, for taking the time to evaluate my work.
Vita

May 7, 1983  ........................................ Born - Huaian, JS, China

June 2005  ......................................... B.S. Optoelectronics,  
                                    A.S. Computer Science & Engineering,  
                                    Nanjing University

June 2008  ......................................... M.S. Optoelectronics,  
                                    Nanjing University

June 2011  ......................................... M.S. Electrical and Computer  
                                    Engineering,  
                                    The Ohio State University

2008-2009  ......................................... University Fellow,  
                                    The Ohio State University

2011-present  ................................. NSF/MIPR Fellow,  
                                    The Ohio State University

**Fields of Study**

Major Field: Department of Electrical and Computer Engineering
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Chapter 1: Introduction

1.1 Motivation

The ever-increasing demand for data rates in modern wireless and wireline communication systems coupled with the push towards mm-wave links, has dictated the need for wide tuning range voltage controlled oscillators (VCOs) to satisfy multi-band/multi-channel standards. Nowadays, mm-wave circuits have proliferated into many commercialized applications, including next generation WiFi (WiGig), auto short range radar (SRR), satellite commercial data and video and mm-wave cellular (LMDS). A wide frequency range is covered by these systems, requiring wide tuning range VCOs to generate the frequency references.

Traditionally, mm-wave VCOs have been implemented in III-V technologies. The primary advantage provided by these technologies is the fast device speed and less parasitic capacitance. Therefore, VCOs can operate at high frequencies with reasonable tuning range. However, they suffer from the main drawback of high manufacturing cost and limited level of integration. With the continued scaling of CMOS technology in accordance with Moore’s law, transistor $f_T$ is improving faster than that in other technologies. With lower cost, ease of integration and power-savings, CMOS VCOs
are very attractive for large-volume applications and can be built as a macro-block in a single-chip transceiver system, allowing high throughput chips with low pin counts. Unfortunately, the benefits in digital CMOS technology is not perpetuated easily in designing mm-wave VCOs. The RF components, including inductors and capacitors, suffer from their low $Q$-factors. Therefore, large transconductance ($g_m$) transistors are required to compensate for high losses incurred in the LC-tank, leading to pronounced capacitive loading effects that sharply reduce the VCO tuning range. Moreover, the process variation in CMOS technology, voltage variation and temperature variation (PVT) necessitate extra frequency margin in VCO design, further limiting the tuning range. Meanwhile, transistors with large $g_m$ generate more noise, which significantly degrade phase noise of the VCO. In mm-wave CMOS VCOs, the contribution of phase noise from transistors can be more than 50%.

This dissertation focuses on the fundamental issues in mm-VCOs: 1) the markedly large VCO fixed capacitance relative to the tank total capacitance and 2) the high $g_m$ from CMOS transistors leading to large fixed capacitance and high phase noise. This work demonstrates new high frequency wide tuning range CMOS VCOs based on novel negative capacitance (NC) circuits. BiCMOS VCOs utilizing both NMOS and BJT cross-coupled pairs to reduce transistor $g_m$ are also validated to reduce phase noise and increase the tuning range.

1.2 Organization

The rest of this thesis is organized as follows. Chapter 2 analyzes the fundamental LC-VCO structure. The circuit design considerations of RF passive components are discussed. Different tuning structures are
analyzed and compared. Specifically, the parasitic inductance in capacitive tuning is analyzed and several inductance redistribution techniques are proposed in the mm-wave LC-VCO design to avoid non-overlap or excess-overlap tuning curves.

Chapter 3 reviews previous mm-wave wide tuning range VCO designs, summarizes the VCO performance and estimates the tuning range scaling trend. Since the understanding of the tuning range issue is the first essential step to solve the problem, the limitations of current mm-wave LC-VCO are investigated and the relationship between tuning range and frequency is theoretically analyzed.

Chapter 4 proposes single-ended and differential NC circuits and optimizes these NC circuits to obtain wide bandwidth to satisfy mm-wave operations. The technology scaling of the NC circuit is also discussed. A new figure-of-merit (FOM) is defined to compare different NC circuits.

Chapter 5 addresses the tuning range issues in mm-wave CMOS LC-VCOs. The amount of tuning range extension is derived by using fixed and variable NC circuits. The NC circuits are further optimized to fit bottom-biased and top-biased VCOs so that they can be combined together without consuming extra power. Both NC VCOs are analyzed and verified.

A novel mm-wave VCO topology in BiCMOS technology is discussed in Chapter 6. Since all-NMOS and all-BJT VCOs can be implemented in BiCMOS technology, they are designed, analyzed and compared. A novel BiCMOS VCO structure is proposed using both NMOS and BJT cross-coupled pairs and compared with all-NMOS and all-BJT VCOs.

Chapter 7 is devoted to the measurement results of different VCO designs. The test setup and the precautions necessary for the high frequency characterization are
explained in this chapter. The conclusion and pointers to future research in this field to expand the tuning range is the subject of Chapter 8.
Chapter 2: Analysis and Design of mm-wave LC-VCOs

VCOs are widely used in both transmitters and receivers of communications systems to generate local oscillator (LO) frequencies and other reference clocks. In mm-wave RF applications, the LC-VCO is the dominant choice due to its robust operation and low phase noise. An LC-VCO can be viewed as two one-port systems connected to each other, as shown in Figure 2.1. A passive LC resonator can be equivalent to an inductor in parallel with a capacitor. The resistor $R_{\text{tank}}$ represents the overall losses of the inductor and capacitor. The active network generates an resistance equal to $-R_{\text{tank}}$ so that the losses can be compensated. Therefore, the circuit can steady oscillate without energy loss. The nominal frequency of oscillation is determined by the LC-tank, and can be expressed as

$$f = \frac{1}{2\pi\sqrt{LC}}. \quad (2.1)$$

In reality, the AM, FM or PM noise from different sources generates noise sidebands around the oscillating frequency $f$, as shown in Figure 2.2. The AM noise contributions are less significant compared to FM or PM noise and can be eliminated by the LC filter. However, the AM noise can be converted into PM noise, which further degrade the VCO phase noise performance. Hence, reducing the sources of these noises in a VCO design can improve the phase noise performance.
Figure 2.1: One port model of VCOs.

Figure 2.2: The power spectral density of the VCO output.
The design of a mm-wave LC-VCO includes three major steps: structure selection, LC-tank design and negative resistance design. Since differential LC-VCOs have advantage on the multi-phase clock generation, a cross-coupled pair differential LC-VCO structure is adopted in this work, as shown in Figure 2.3. The inductor and capacitors comprise the LC-tank. The negative resistance circuit consists of two transistors ($M_1$, $M_2$) and a current source. The buffers amplify the output signal to the desired output power.

Due to the importance of the LC-tank, the following part of this chapter analyzes and designs high performance inductive and capacitive components in circuit level. To reduce the VCO gain ($K_V$) and hence minimize the phase noise associated with AM-PM noise conversion, a coarse tuning structure is utilized. Since the tuning range and phase noise is mainly determined by coarse tuning structures, they are carefully studied and analyzed in a 130 nm process. The phase noise generation mechanism is also discussed.

### 2.1 Inductor Analysis and Design

Inductors are usually implemented in three ways for an LC-VCO: 1) off-chip inductors, 2) bond-wire inductors and 3) on-chip spiral inductors. In mm-wave VCO designs, given the relatively low value of inductance required, the on-chip spiral is preferred to minimize additional parasitics. Figure 2.4(a) shows a two-turn on-chip spiral inductor. Its inductance can be obtained by using a simple equation [66]

$$L = \frac{1.07\mu_0 d_{avg} n^2}{2} \left( \ln \frac{2.29}{\rho} + 0.19\rho^2 \right)$$

(2.2)

where $\mu_0$ is magnetic permeability, $d_{avg}$ is the average outer dimension, $n$ is the number of turns, and $\rho$ is the filling factor. To derive the $Q$-factor expression, two
Figure 2.3: An LC-VCO with coarse tuning ($B_0 - B_N$).
major losses of inductors in CMOS technology are considered: the metal resistance and eddy loss. The metal resistance with the skin effect can be written as

\[ R_{\text{skin}}(f) = \frac{l}{W_L \sigma \delta (1 - e^{-t/\sigma})} \]  

(2.3)

where \( W_L, l \) and \( t \) are the width, total length and thickness of the inductor winding, as shown in Figure 2.4(a), \( \sigma \) is the conductivity of the metal, and the skin depth \( \delta \) is given by \( \sqrt{1/\pi f \mu_0 \sigma} \). The eddy loss is determined by [65]

\[ R_{\text{eddy}}(f) = \frac{\sigma_{\text{sub}} (\mu_0 n f)^2 d_{\text{avg}}^3 \rho^{0.7} h^{0.1} t_{\text{ins}}^{0.55}}{4e} \]  

(2.4)

where \( t_{\text{ins}} \) is the thickness of the insulator between inductor metal and the substrate, \( h \) is the thickness of the substrate. Using a simplified circuit model in Figure 2.4(b), the inductor \( Q \) is further calculated as

\[ Q_{\text{ind}} = \frac{L/C_L(1/\omega C_L - \omega L) - (R_{\text{skin}} + R_{\text{eddy}})^2/\omega C_L}{(R_{\text{skin}} + R_{\text{eddy}})/\omega^2 C_L^2} \]  

(2.5)

where \( C_L \) is the parasitic capacitance, proportional to \( W_L \) and \( l \). From (2.5), one can see that the \( Q \)-factor of the inductor suffers from three loss mechanisms: metal resistance, eddy loss and capacitive coupling. To improve the inductor \( Q \), 1) stacking of metal layers and the copper coil are employed to reduce the metal resistance, 2) the substrate is lightly doped and with deep trench to obtain high-resistivity and thus reduce the magnetic loss (eddy loss), 3) the top layer is used in inductor designs to increase the distance between the substrate and inductor metal.

At a specific frequency, inductors with different outer dimensions have different \( L \) and \( Q_{\text{ind}} \). Table 2.1 shows some examples of the calculated \( L \) and \( Q_{\text{ind}} \) for different inductor designs in a 130 nm CMOS process with thick top metal option. As \( L \) increases, \( Q_{\text{ind}} \) increases to a maximum value, then starts to decrease. When \( Q_{\text{ind}} \) is maximum, this inductor is optimum at that frequency.
Figure 2.4: On-chip spiral inductor (a) geometry and (b) simplified circuit model.

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<td>27.1</td>
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<td>60</td>
<td>75</td>
<td>26.9</td>
</tr>
<tr>
<td>60</td>
<td>100</td>
<td>25.2</td>
</tr>
</tbody>
</table>
To verify the results, different inductors are designed and compared with the calculation. Figure 2.5 shows an example of the inductor layout. Since the required inductance is typically below hundreds of pH in mm-wave applications, the inductor can be designed to be one turn only to avoid the capacitance coupling between different turns. In addition, the inductor uses top layer metal only to reduce the parasitic capacitance. A deep trench is doped into the substrate area near the inductor to further reduce the coupling capacitance to the substrate. Meanwhile, due the high resistance of the deep trench, the eddy loss reduces. To minimize the resistive loss, the width of the inductor is designed to be 25 μm. The ground is placed around the inductor with 25 μm spacing to shield the inductor while avoiding parasitic capacitance coupling.

The same inductor is redesigned in Sonnet electromagnetic (EM) simulator. The metal conductivity and material dielectrics are extracted from the process and specified in the EM simulator. To ensure the accuracy of the simulation, the simulation area (box) is selected to be 200 μm away from the structure [91]. The extra metal from the side of the box to the inductor ports are de-embedded to obtain the property of the stand-alone inductor only. A center tap is also included in the simulation to capture accurate results, as shown in Figure 2.6. The simulated differential inductance is 107 pH and $Q$ is 26.1 at 35 GHz.

To obtain inductors with optimum $Q$-factor, different outer dimensions of the inductors are designed and simulated at various mm-wave frequencies. The inductor with best $Q_{ind}$ at each frequency is selected and plotted in Figure 2.7. Based on the given dimensions, the calculated optimal inductors are also plotted in the same figure for comparison. The calculation shows consistent results as simulation. It is worth
Figure 2.5: The layout of the inductor.

Figure 2.6: The layout of the inductor in Sonnet EM simulator.
Figure 2.7: Calculated and simulated inductance and quality factor for inductors designed with the highest $Q$ at different mm-wave frequencies.

noting that the $Q$-factor of inductors operating in mm-wave range is typically high ($>20$).

2.2 Capacitor Analysis and Design

Capacitive components in the LC-tank includes routing capacitance ($C_{rt}$), buffer capacitance ($C_{buf}$), transistor capacitance ($C_t$) and capacitance from fine and coarse tuning structures. $C_{rt}$ is determined by the length and width of the routing traces. $C_{buf}$ and $C_t$ are fixed once the gain and size of buffer and transistor are designed. For the tuning structure, a varactor, usually a high $Q$ accumulation MOS [3], can be used for the fine tuning and the switched MIM-caps or varactor structures can be utilized for the coarse tuning [87].
2.2.1 Switched MIM-cap Coarse Tuning

For switched MIM-caps coarse tuning structures, there are two implementations in the literature [1]: double switch MIM-caps (Figure 2.8(a)) and single switch MIM-caps (Figure 2.8(b)). Compared to the double switch MIM-cap structure, the single switch MIM-cap structure reduces the losses from MOS switches to half of the double switch one. Furthermore, the possibility of forward biasing source and drain junction diodes during large signal operation is not present since the DC voltage at the source and drain of the transistor switch in Figure 2.8(b) is set to the power supply voltage when the MOS switch is off. Therefore, this structure is preferred in the VCO design.

To calculate the tuning range, a model of this structure is built, as shown in Figure 2.8(c), and the single-ended capacitance is derived as

\[
C_{sw,MIM} = C_{MIM} / \left( 1 + \frac{\omega^2 R_{sw}^2 (C_{sw} + C_{MIM,p})^2}{\omega^2 R_{sw}^2 (C_{sw} + C_{MIM,p})} \right) \tag{2.6}
\]

where \(C_{MIM}\) is the capacitance of the MIM capacitor, \(C_{MIM,p}\) is the parasitic capacitance (back plate capacitance) of the MIM capacitor, and \(R_{sw} \) and \(C_{sw}\) are given by

\[
\frac{1}{R_{sw}} = \frac{2}{R_{MOS}} + \frac{1}{R_b} + \frac{\omega^2 C_{db}^2 R_s}{1 + \omega^2 C_{db}^2 R_s^2} \tag{2.7}
\]

\[
C_{sw} = C_{gd} + \frac{C_{db}}{1 + \omega^2 C_{db}^2 R_s^2} \tag{2.8}
\]

The single-ended parallel resistance is expressed by

\[
R_{sw,MIM} = R_{MIM} + \frac{R_{sw}}{1 + \omega^2 R_{sw}^2 C_{sw}^2}. \tag{2.9}
\]

When the switch is off, \(R_{sw}\) is high if choosing the bias resistor \(R_b\) to be sufficiently high. Assume \(C_{sw} \gg C_{MIM,p}\), \(C_{sw,MIM}\) can be approximated as \(C_{MIM} / / C_{sw}\). While
Figure 2.8: (a) Double switch MIM-caps coarse tuning structure. (b) Single switch MIM-caps coarse tuning structure. (c) Equivalent circuit of Figure 2.8(b).
the switch is on, $R_{MOS}$ can be represented as

$$R_{MOS, on} = \frac{L}{\mu C_{ox} W (V_{gs} - V_{th})}.$$  \hspace{1cm} (2.10)

The value of $R_{MOS, on}$ is usually below 10 $\Omega$, and $C_{sw,MIM}$ can be approximated as $C_{MIM}$. The tuning range of switched MIM-cap structure is

$$TR_{sw,MIM} = \frac{C_{MIM}}{C_{MIM} + (C_{sw} + C_{MIM,p})}.$$  \hspace{1cm} (2.11)

To increase $TR_{sw,MIM}$ of the MIM-cap structure, $C_{sw}$ should be reduced, which necessitates a decrease in the size of the MOS switch. However, with the decreasing of the switch size, $R_{MOS, on}$ increases, and the losses of switched MIM-cap structure $R_{sw,MIM}$ also increases, which degrades the $Q$-factor of the LC-tank. To illustrate this tradeoff, Figure 2.9 shows the calculated, along with the simulated capacitance and $Q$ of the switched MIM-caps with different MOS switch sizes. As expected, $Q$ increases as the switch width increases, but the tuning range decreases. Considering the $Q$-factor of the LC-tank, the width of the switch can be selected to be 200 $\mu$m for a 100 fF MIM capacitor. The corresponding tuning range is only 1.5.

### 2.2.2 Switched Varactor Coarse Tuning

MOS varactors are widely used in fine tuning of mm-wave LC-VCO [9, 14, 21, 36, 47, 53, 56, 61, 93, 96, 107]. If applying digitally-controlled voltage to the varactor, it can be used for coarse tuning. The model of a digitally-controlled varactor [89], as shown in Figure 2.2.2, is utilized to calculate the capacitance. The bias dependent $C_{vs}$ can be represented as [23]

$$C_{sw,v} = C_{vs,min} + B_N \Delta C_{vs}$$  \hspace{1cm} (2.12)
Figure 2.9: (a) The capacitance and (b) the $Q$-factor of the single switch MIM-caps and varactor. Solid and dotted Lines are calculated value, and symbols are simulated results.
where \( B_N \) is the digital tuning bit. \( C_{\text{vs,\text{min}}} \) and \( \Delta C_{\text{vs}} \) are device parameters, which are proportional to the area of the varactor. The losses of the varactor can be written as [89]

\[
R_{\text{sw-v}} = R_{\text{vs}} + R_{\text{vacc}}/R_{\text{vp}} \tag{2.13}
\]

where \( R_{\text{vacc}} \) is the resistance of the accumulation layer, \( R_{\text{vs}} \) is the effective resistance between the accumulation layer and the source/drain, and \( R_{\text{vp}} \) represents the effective resistance between \( R_{\text{vs}} \) and the edge of the depletion layer. When the varactor is off, \( R_{\text{vacc}} \) equals \( 1/K_{\text{vacc}} \). It is infinity when the varactor is on. \( R_{\text{vs}}, K_{\text{vacc}} \) and \( R_{\text{vp}} \) are proportional to the width of a minimum length varactor. To illustrate the advantage of the varactor coarse tuning structure, both capacitance and \( Q \) of the grounded source/drain varactor are calculated at 40 GHz, and results are plotted in Figure 2.9. Simulated results are plotted in the same figure to verify the above analysis. The on-state and off-state capacitance of a 0.7 \( \mu \text{m} \) width varactor is the same as that of the switched MIM-caps structure with a 65 \( \mu \text{m} \) switch. The tuning range of both structures is 2.5. However, the on-state \( Q \) of the varactor tuning structure is above 15, while it is below 10 for the switched MIM-cap structure.

From the above analysis, varactor coarse tuning structures have superior \( Q \) over switched MIM-caps, and will be adopted in the mm-wave VCO design.

2.3 Coarse Tuning Structure Implementation with Inductance Redistribution

To reduce the AM-PM noise conversion and hence lower the overall phase noise of the VCO, digital coarse-tuning is often employed to lower the VCO gain (\( K_V \)) [25,87]. In this design, a 6-bit coarse tuning structure is utilized. The structure typically
employs a binary-weighted switched-capacitor (C-DAC) array to reduce the number of capacitors and simplify the tuning control logic [88]. However, the mismatch between the coarse tuning capacitors, exacerbated by the small unit capacitor cell, may result in non-overlapping tuning curves. To reduce this error, a thermometer C-DAC that distributes the mismatch among different tuning curves is utilized for the 3 most significant bits, while a simple binary C-DAC is used for the 3 least significant bits. Figure 2.3 shows the cross-coupled LC-VCO design. To connect across such a large number of C-DAC elements, a long feed line is required. This comes at the expense of large parasitic inductance, which results in non-uniform frequency step ($f_{step}$) across the tuning range.

To reduce the variations in $f_{step}$, a pseudo-exponential capacitor bank was proposed [43]. In [62], a varactor array was utilized in parallel with the conventional switched capacitor array to achieve uniform $f_{step}$. A sizing methodology was proposed in [17], where each varactor branch in the bank is sized according to the $C_{max}$
and $C_{\text{min}}$ values required to achieve the specified $K_V$ and $f_{\text{step}}$ for each sub-band. The aforementioned solutions, while applicable in the low-GHz range, fail to operate at mm-wave frequencies. At such high frequencies, the capacitance unit step ($C_{\text{step}}$) is in the range of a few fFs, and hence the parasitic inductance of the feed line can significantly change the effective capacitance of the C-DAC, leading to non-uniform $f_{\text{step}}$.
2.3.1 Limitations in Conventional Coarse Tuning Structure

The capacitor bank is implemented as an array of MOS varactors that are digitally switched, where the varactors are switched between accumulation and depletion regions. A 6-bit C-DAC is implemented as 50% segmented, i.e. thermometer code is employed for the 3 most significant bits (MSBs), while the other 3-bits are binary coded. The binary-weighted capacitor employs unit capacitor $C_0$ or arrays of $C_0$s to

Figure 2.12: The conventional capacitor bank.
alleviate the mismatch between the binary-scaled cells and ensures monotonicity. The total number of capacitors in this structure is 28, which are connected together by an 80 \( \mu \text{m} \) trace, as shown in Figure 2.12. B0-B2 denote the binary bits, and T0-T6 denote the thermometer bits. The feed line structure is modeled using Sonnet EM simulator. Simulation shows that by switching T3-T6 bits, a higher capacitance is added to/subtracted from the tank, resulting in a frequency gap, as illustrated in Figure 2.13. Since bits T3-T6 are close to the cross-coupled pair, less routing inductance shields the tuning capacitance. Hence, these bits have higher impact on changing the effective capacitance of the tank. Conversely, bits T0-T2, which are farther away from the cross-coupled pair, have more routing inductance shielding the tuning capacitance. These bits have less impact on changing the tank capacitance. Therefore, switching T0-T2 results in an excess overlap between tuning curves, as shown in Figure 2.13. In contrast, without considering the routing parasitics, neither frequency gaps nor excess overlaps exist in the tuning curves.

To theoretically explain the problem, a simplified model of the routing structure is constructed. Since the distance between two successive capacitors is 4 \( \mu \text{m} \), which is smaller than one-twelfth of the wavelength in Ka-band, this segment is modeled by a lumped RLCG model, as shown in Figure 2.14. To demonstrate the impact of the line inductance on the effective capacitance, two segments of the line are considered and the resistive losses and the mutual coupling are neglected. The effective capacitance is given by

\[
C_{eq2}(\omega) = \frac{C_{X1} + C_{X2} - \omega^2LC_{X1}C_{X2}}{\omega^4L^2C_{X1}C_{X2} - \omega^2L(C_{X1} + 2C_{X2}) + 1}
\]

where \( C_{X1} = C_{01} + C \) and \( C_{X2} = C_{02} + C \). For \( L = 0 \) and \( C = 0 \), \( C_{eq2} \) is reduced to \( C_{01} + C_{02} \), which is the parallel equivalent of two capacitors. However, the inductance
of the feed line introduces error to the effective capacitance by adding the capacitances in a non-uniform way. The error in $C_{\text{step}}$ per digital code can be reduced by decreasing the inductance of the line. While increasing the width of the routing trace reduces its inductance, the capacitance of the line increases, limiting further decrease of the error in $C_{\text{step}}$.

### 2.3.2 Inductance Balance Structure

Figure 2.15 shows the one of the proposed VCOs with inductance redistribution. The bias, inductor and cross-coupled pair remains the same as the aforementioned conventional structure, the capacitive part and the according connection utilize wider routing line and inductance balance techniques. From resistance prospective, the top metal is employed to maintain the $Q$-factor of the tank. To guarantee the low

Figure 2.13: Frequency tuning curves of the conventional structure.
inductance for high frequency operation, the width of the routing line is increased from 15 µm to 50 µm, which further improves the tank $Q$-factor.

To balance the inductance, each varactor ($8C_0$) connected to thermometer bits (T0-T6) in conventional design is separated into two varactors ($2 \times 4C_0$). One of the varactors is arranged to be close to the cross-coupled pair and the other is away from the cross-coupled pair. Since the control lines of these two varactors are connected together, they switch on/off simultaneously. As illustrated in Figure 2.15, considering thermometer coarse tuning bit T0, the varactor on the top ($4C_0$) has less inductance ($L_{rt} - 3\Delta L_{rt}$) in the routing path, while the other varactor ($4C_0$) has more inductance ($L_{rt} + 3\Delta L_{rt}$) in the routing path. The overall equivalent inductance associated with the two varactors is the average, which is $L_{rt}$. For other coarse tuning bits, the equivalent inductance associated with varactors can similarly be calculated to be $L_{rt}$, which is the same as that of the thermometer coarse tuning bit T0. Therefore, the overall inductance is balanced, and no gaps or overlaps are shown in the tuning curves.

To verify this inductance balance structure, the VCO with the proposed tank is implemented in a 130 nm CMOS technology. Figure 2.16 shows the layout of the
Figure 2.15: Capacitive tank with the inductance redistribution technique.
inductance balanced tank. The varactors are placed close to the feed line to minimize any additional parasitics. The properties of the feed line is characterized by the Sonnet EM simulator and exported into the circuit simulator. The VCO with the proposed tank is simulated and the tuning curves at high and low frequencies are shown in Figure 2.17. Compared to the tuning curves in Figure 2.13, the spacing across tuning range from 30.5 GHz to 39.6 GHz is uniform with minimum overlap of 28% and maximum overlap of 36%.

Figure 2.16: LC-tank layout with the inductance balance technique.
2.3.3 Symmetrical Tree Structure

As shown in Figure 2.18, another proposed tree feed structure is realized with equal routing inductance between the $g_m$ devices and each capacitor in the tuning structure, resulting in minimal variation in $f_{\text{step}}$. Each branch of the tree has a unit varactor ($C_0$) controlled by the binary bits and $8C_0$ controlled by the thermometer bits. The tree structure uses a wide line to minimize its resistive losses and inductance.

Figure 2.19 shows the layout of the tree structure. The characteristics of the structure are modeled using the Sonnet EM simulator. Figure 2.20 shows the frequency tuning curves per digital word. The VCO tuning range is simulated to be uniform without any gaps from 30.8 GHz to 37.6 GHz. The $K_V$ varies by $\pm15\%$ over the
6.8 GHz tuning range from 350 MHz/V at the lowest frequency end to 480 MHz/V at the highest frequency end.

2.4 Negative resistance Design

The losses of the LC components in the VCO are compensated by the negative resistance of the cross-coupled pair, as shown in Figure 2.21. To satisfy the oscillation startup, \( g_m \) is set to be

\[
g_m = \eta \times \frac{2}{R_{\text{tank}}} \quad (2.15)
\]
Figure 2.19: LC-tank layout with the balance tree technique.

Figure 2.20: Frequency tuning curves of the VCO with the tree structure.
where $R_{tank}$ is the parallel resistive loss of the LC-tank and $\eta$ is the design margin. Ideally, the oscillation starts when $\eta > 1$. However, due to process, voltage and temperature (PVT) variations, $\eta$ is usually set to be between 2 to 3. In this VCO design, $\eta$ is set to be 2.5 to overcome process, voltage and temperature (PVT) variations.

### 2.5 VCO Buffer Design

The VCO buffer amplifies the output signal power to drive off-chip 50 $\Omega$ impedance. To reduce the capacitive loading effect of the LC-tank, the buffer is connected to the VCO core through a small coupling capacitor. Due to the gain requirement, a two-stage buffer and inductive peaking techniques are utilized. Figure 2.22 shows the schematic of the two-stage buffer.
Figure 2.22: The schematic of the VCO buffer.

The first stage of the buffer mainly functions as a voltage amplifier. The second stage uses the pre-amplified voltage, amplifies it and outputs high power. Due to the additional inductors at the output stage, the impedance is not exactly 50 Ω. A matching network is designed and connected to the second stage buffer to match 50 Ω impedance. The layout of the two stages are shown in Figure 2.23. The buffer boosts the VCO output to $-5$ dBm with power variation of 3 dBm from 30 GHz to 40 GHz.
Figure 2.23: The layout of (a) the first stage buffer (b) the second stage buffer with matching network.
2.6 VCO Phase Noise

There are two types of noises in LC-VCOs: amplitude modulation (AM) noise and phase modulation (PM) noise. AM noise is the undesired amplitude fluctuation of a signal. In an LC-VCO, AM noise only changes the amplitude of the output signal, and this amplitude variation can be suppressed by buffers or filters in the circuits. It is also rejected by the differential nature of the VCO since it is common mode noise. PM noise, which is usually called phase noise, is the frequency domain representation of phase fluctuations of a periodic signal. In time domain, phase noise can be represented as jitter, which is reflected as the time deviation between the expected occurrence of a signal edge and the time the edge actually occurs. Phase noise of LC-VCOs can be predicted by Leeson’s formula [80] after accounting for the varactor AM–PM conversion factor,

\[
L(\Delta f, K_V) = 10 \log \left\{ \frac{2FkT}{P} \left( \frac{1}{2Q} \frac{f_0}{\Delta f} \right)^2 \left( 1 + \frac{f_c}{\Delta f} \right) + \frac{1}{2} \left( \frac{K_V V_m}{2\Delta f} \right)^2 \right\}
\]

(2.16)

where \( K_V \) is the gain of the VCO, \( V_m \) is the total amplitude of low frequency noise from the bias circuit and varactor control line, \( P \) is the output power, \( Q \) is the qualify factor of the tank. To minimize the VCO phase noise, high \( Q \) tank and high output power are required. While Leeson’s formula delivers a simple and intuitive understanding of phase noise, it does not specify where the origin of the noise is from and how it correlates with the VCO phase noise.

To identify noise sources, a conventional NMOS bottom-biased cross-coupled pair LC-VCO shown in Figure 2.24(a) is carefully studied. The LC-VCO consists of three major parts: LC passive components, the tail current source and negative resistance cross-coupled pair of transistors. All these three components contribute noise, which
essentially converts into VCO phase noise. Figure 2.24(b) shows the noise sources in the half circuit of the LC-VCO. The noise of the LC passive components is attribute to their losses. These losses can be modeled as a parallel resistor $R_p$. The noise current from the LC passive components is expressed as

$$I_{n-R_p}^2 = \frac{4kT}{R_p}. \tag{2.17}$$

Half of $I_{n-R_p}^2$ is amplitude noise, the other half is phase noise. The noise of the tail current source can be represented as a shunt noise current $I_{n-b}^2$, which will be discussed in detail. The noise from the transistors can be written as

$$I_{n-M}^2 = 4kT\gamma g_m t_{sw} \frac{T}{T}. \tag{2.18}$$

where $t_{sw}$ is the switching time of the transistors, $T$ is the period of the VCO signal, $\gamma$ is $2/3$ for short-channel MOS devices in LC-VCOs [32].

Among these three noise sources, the AM noise of the tail current source can be upconverted or downconverted into the AM noise with the frequencies close to the VCO oscillating frequency. The MOS switching transistors $M_1$ and $M_2$ behave like a single balance mixer with LO frequency $f_{LO}$ equals to the fundamental frequency of the VCO and upconvert or downconvert the tail current noise (around dc and second harmonic) to the AM noise near the desired frequency. Second and higher harmonics in the LO signal are not considered because even harmonics can be completely canceled in fully differential VCOs, and the high order harmonics can be suppressed by the VCO tank. The detailed mixing process is illustrated in Figure 2.25. The mixer upconverts low frequency noise from the tail current source into two correlated AM sidebands at the center frequency of $f_{LO}$. High frequency noise at $2f_{LO}$ is also downconverted into noise at $f_{LO}$ and upconverted into noise at $3f_{LO}$. The noise at $3f_{LO}$ is
rejected by the LC tank. The total noise at $f_{LO}$ equals to the sum of low frequency upconverted noise and high frequency downconverted noise. The use of RC filters between the bias circuit and the cross-coupled pair does not prevent AM modulation. This is attributed to the fact that it only filters high frequency noise, while allowing low frequency noise to pass almost unattenuated from the current source [44]. The varactor further converts this AM noise into PM noise which degrades the VCO phase noise. Therefore, low VCO gain $K_V$ can improve the phase noise at the expense of smaller tuning range. For wide tuning range VCOs without adopting coarse tuning
(\(K_V \sim 5\) GHz/V), the tail current noise contributes up to 75\% of the overall phase noise in LC-VCOs [68, 79].

To better minimize the phase noise performance of LC-VCOs, the noise distribution for the designed 35 GHz VCO (\(K_V = 500\) MHz) is simulated at 10 kHz and 1 MHz offset, as listed in Table 2.2. At 1 MHz offset, the majority noise contribution is from the \(g_m\) transistors. However, the bias noise contributes the most for close-in offset frequency (10 kHz). Since some AM noise from the bias circuitry is up-converted to phase noise, to evaluate the amount of AM-PM conversion, the same frequency
Table 2.2: Noise Contribution of Different Noise Sources in 35 GHz LC-VCO

<table>
<thead>
<tr>
<th>Source</th>
<th>@10kHz offset w/ varactor</th>
<th>@10kHz offset w/o varactor</th>
<th>@1MHz offset w/ varactor</th>
<th>@1MHz offset w/o varactor</th>
</tr>
</thead>
<tbody>
<tr>
<td>LC tank</td>
<td>14%</td>
<td>23%</td>
<td>17%</td>
<td>19%</td>
</tr>
<tr>
<td>Bias</td>
<td>59%</td>
<td>23%</td>
<td>21%</td>
<td>12%</td>
</tr>
<tr>
<td>$g_m$ transistor</td>
<td>22%</td>
<td>36%</td>
<td>56%</td>
<td>62%</td>
</tr>
<tr>
<td>Routing</td>
<td>5%</td>
<td>8%</td>
<td>6%</td>
<td>7%</td>
</tr>
</tbody>
</table>

The oscillator is designed without varactors. The results show that the bias noise of the varactorless oscillator is significantly less at 10 kHz offset. Hence, a VCO with lower $K_V$, which reduces AM-PM conversion, shows better phase noise performance.
Chapter 3: Limitations of mm-wave LC-VCOs

3.1 Introduction to mm-wave LC-VCOs

Over the past few years, the rapid growth of wireless communications systems has led to the shift to mm-wave links. The commonly used mm-wave frequency bands ranging from 10 to 110 GHz are shown in Table 3.1. Nowadays, a lot of commercial products have been developed, such as next generation WiFi (WiGig), short range radar (SRR) for automobiles, satellite commercial data and video. Figure 3.1 shows the operating frequency range of these devices. A wide channel bandwidth and/or efficient modulations are required by the demand for high data rates.

As standards evolve and develop, systems have to satisfy multi-band/multi-channel requirement to cope with a more crowded spectrum and be compatible with a number of legacy standards for backward compatibility, resulting in a trend of wide-band system designs. Wide tuning VCOs are required to generate reference clocks for

<table>
<thead>
<tr>
<th>Band</th>
<th>K_u</th>
<th>K</th>
<th>K_a</th>
<th>Q</th>
<th>U</th>
<th>V</th>
<th>E</th>
<th>W</th>
</tr>
</thead>
<tbody>
<tr>
<td>f (GHz)</td>
<td>12–18</td>
<td>18–26.5</td>
<td>26.5–40</td>
<td>33–50</td>
<td>40–60</td>
<td>50–75</td>
<td>60–90</td>
<td>75–110</td>
</tr>
</tbody>
</table>
these systems. Furthermore, the process, voltage and temperature (PVT) variations necessitate VCOs to have extra margin on the tuning range, as shown in Figure 3.1.

Traditionally, system designers utilize multiple VCOs operating at different bands in transmitters or receivers to address this tuning range demand, leading to an increase in the cost and complexity of the systems [39]. Simplifying multiple VCOs into a single VCO becomes a trend in modern handheld equipment designs. In single wide tuning range VCO implementation, two dominant approaches are widely adopted: push-push (N-push) and magnetic coupling/tuning.

VCOs using their second/Nth harmonic as the output are named push-push/N-push VCOs. A push-push/N-push VCO has a LC-VCO operating at a low frequency (usually half of the desired frequency) and a doubler or multiple doublers [9, 96] to boost the operating frequency. Figure 3.2(a) illustrates a simplified push-push doubler. When the signal of the low frequency LC-VCO is fed to the doubler (or directly to the common mode inductor), the tuning range does not change, but the operating frequency doubles. Since running the VCO core at lower frequency has
wide tuning range and the doubler maintains the tuning range at twice of the original frequency, both wide tuning range and high operating frequency can be achieved in the push-push VCO. However, the output power of LC-VCOs using harmonics is low due to the poor efficiency of harmonic generation. To maintain the desired output amplitude, more power is required from the power supply. Furthermore, if the second harmonics is used, the phase noise decreases by at least 6 dB compared to that of the LC-VCO using fundamental component as its output.

On the other hand, magnetic coupled/tuned VCOs show wide tuning range while consuming no extra power [21,47,93]. Figure 3.2(b) and Figure 3.2(c) show simplified magnetic tuned and coupled VCO tanks, respectively. In the magnetic tuned VCO, inductors are placed in series and some inductors can be turned on/off, offering additional tuning capability. In the magnetic coupled VCO structure, the inductor in the tank is coupled to a second inductor. By altering the impedance of the second inductor, the inductance in the LC-tank also changes, providing an increase in the tuning range. However, finite resistance in the inductance tuning structure adds losses to the LC-tank, resulting in a degradation in phase noise. Further increasing the switch lowers its resistance but results in higher loading capacitance, which ultimately limits the frequency of oscillation.

To reduce phase noise, different filtering techniques can be applied to LC-VCOs to minimize contribution of noise sources [31]. Since $2\omega_0$ noise at the current source can be down-converted to noise around $\omega_0$ and further converted into phase noise, placing a capacitor in parallel with the current source in a bottom-biased VCO can short $2\omega_0$ noise to ground (Figure 3.3(a)). In Figure 3.3(b) an inductor is further added in series with the current source. The inductor is selected to be high impedance at $2\omega_0$,
which resists $2\omega_0$ noise while increases the impedance of the VCO tank to ground to avoid tank impedance degradation when a transistor is turned on. A top-biased VCO is also proved to be more immune to substrate noise and up-convert less flicker noise into phase noise since the bias transistor is moved away from cross-coupled pair and noise at low frequencies or $2\omega_0$ is not up-converted or down-converted into $\omega_0$ noise [31]. Adding filters in top-biased structure can further improve phase noise performance (Figure 3.3(c)). Reducing the active device sizes [35] or optimizing the current mirror ratio [45] is also shown to reduce phase noise.

### 3.1.1 Current Trends in mm-wave LC-VCOs

Figure 3.4(a) and Figure 3.4(b) summarize the tuning range and figure-of-merit-with-tuning (FOM_T) of recent VCOs. At low frequencies, The VCOs achieve a relatively wide tuning range. However, when the frequency shifts to 10s of GHz, most VCOs show a small tuning range (< 30%). Specifically, for CMOS VCOs, when the
frequency is above 30 GHz, the best tuning range is less than 20%. The corresponding
FOM_T is also worse than that of low frequency VCOs.

Different techniques have been utilized to achieve wide tuning range. Careful
layout of inductors, varactors and transistors in the VCO tank can achieve high
frequencies and better tuning range [7, 8, 33, 60, 98, 110]. The LC-VCO in [10] uses
top metal only to design the inductor. This top metal is 0.8 μm thick and ∼ 5 μm
above the substrate. The metal width of the inductor is also selected according
the skin depth of the current flowing in the inductor to minimize extra losses. The
spacing between different turns of this inductor is carefully chosen to reduce parasitic
capacitance. Furthermore, a patterned ground is being placed under the inductor to
reduce capacitive coupling to the lossy substrate. The varactor is carefully laid out:
Figure 3.4: (a) The tuning range and (b) the $FOM_T$ vs. frequency of mm-wave LC-VCOs.
(1) both ends of the poly gate are connected to reduce resistive loss, (2) each finger of these gates are connected by two top layer metal, (3) the contact between metal-to-poly and metal-to-diffusion is placed farther away from the active gate area to reduce parasitic capacitance. Moreover, the two transistors in this VCO are combined to reduce the interconnection loss and parasitic capacitance. The finger width is balanced between gate resistance and gate-to-substrate capacitance. The drains of different fingers are also connected by high layer metal to reduce capacitance.

The use of SiGe [12,37,64,99] or other advanced technologies [48,63,92] can also achieve wide tuning range at mm-wave frequencies. The SiGe process provides high gain and less parasitics by utilizing bipolar transistors. Other advanced technologies, such as silicon-on-insulator (SOI), also promise less parasitics [39–42]. VCOs in V-band [6,15,26,49,50,83] or W-band [54,75,77,78,84,102] are designed in the above technologies. Although the operating frequency is improved, the VCOs operating at high fundamental frequency still show limited tuning range and high power consumption.

Another VCO structure, known as push-push VCO, uses its second harmonic as the output to double the VCO fundamental frequency [2,9,16,76,94]. However, this VCO shows lower output power and higher phase noise compared to that of the LC-VCO using fundamental component. The VCOs using higher order harmonics encounters further performance degradation [11,96,97]. Combining push-push and SiGe technologies, better performance VCO can be realized with the drawback of high power consumption [5,38,69,72,82,95].

By using a variable inductor technique, which adopts bridge circuit to tune the tank inductance, a VCO achieves a 69% tuning range [93]. The coarse tuning of
this LC-VCO combines both switched MIM capacitors and a bridged inductor. The bridged inductor is superior to a regular switched inductor in parasitic resistance and capacitance. Furthermore, the switched MIM capacitors assist the bridged inductor to obtain wider tuning range by changing tank capacitance. The frequency range of this VCO is further extended using a divider to 5–20 GHz. Other VCOs with switched coupled-inductors [21, 22, 52, 70, 74, 81], tuned transconductor [20, 47, 55, 59, 107, 109] or transformer [13, 46, 57, 71, 73, 108] techniques can also cover a wide tuning range. However, all the above VCOs operate at relatively low frequencies, below 30 GHz.

3.2 Tuning Range Limits of mm-wave LC-VCOs

In the LC-tank of a VCO (Figure 2.3), there are two types of capacitance: fixed capacitance ($C_{fix}$) and variable capacitance ($C_{var}$). $C_{fix}$ includes fine tuning varactor fixed capacitance ($C_{v,fix}$), coarse tuning switch capacitance ($C_{sw}$), buffer capacitance ($C_{buf}$) and transistor capacitance ($C_t$). Fine tuning varactor variable capacitance ($C_v$) and MIM capacitor ($C_{MIM}$) are variable capacitance. At mm-wave frequency range, issues such as low $Q$-factor of the MOS varactor, higher losses incurred in the switched-capacitor elements and parasitic capacitances from the transistors and varactors, result in a sharp degradation in the resonator $Q$. To compensate for these losses, large size transistors are required to provide negative resistance to start the oscillation. Due to large gate capacitance and the capacitive coupling to the low resistivity Si substrate in CMOS processes, the transistors add large amount of parasitic capacitance ($C_t$) to the LC-tank, limiting the tuning range of the VCO significantly. Therefore, designing high frequency VCOs with wide tuning range becomes a challenging task.
To illustrate range limitations, two cross-coupled VCOs with fine and switched MIM coarse tuning have been designed in a 130 nm process at 10 GHz and 40 GHz. In the 10 GHz VCO, the capacitance distribution is extracted, as shown in Figure 3.5(a). Since the tuning range can be expressed as

\[
TR_{VCO} = 2 \cdot \frac{\sqrt{C_{fix} + C_{var}} - \sqrt{C_{fix}}}{\sqrt{C_{fix} + C_{var}} + \sqrt{C_{fix}}}
\]

(3.1)

it can be calculated to be 34% given that \(C_{fix}\) contributes 50% of the total capacitance. However, when the frequency of the LC-VCO in the same process shifts to 40 GHz, the inductance and total capacitance should be reduced by a factor of 4\times to accommodate the frequency increase. Without changing the \(g_m\) transistors, buffers or routing, the ratio of \(C_t, C_{buf}\) or \(C_{rt}\) to the total capacitance increases by four times.

In reality, at high frequencies, the overall \(Q\)-factor of the LC-tank reduces. The transistor size must increase to compensate for the additional tank losses at high frequencies, which essentially increases \(C_t\). Furthermore, \(C_{buf}\) increases due to the gain reduction at high frequencies. Consequently, \(C_{fix}\) contributes 77% of the total capacitance in this 40 GHz VCO, as shown in Figure 3.5(b), resulting in a tuning range of only 15%.

### 3.2.1 Frequency Tuning Range Analysis

To derive the relationship between the tuning range and the operating frequency, CMOS LC-VCOs in a 130 nm process with maximum tuning range are carefully studied. Since the VCO oscillating frequency is determined by the inductor and capacitors in the LC-tank, and the \(Q\)-factors of these components set the required \(g_m\) to start the oscillation and the transistor capacitance, both RF passives and transistors limit the tuning range. To better understand these limitations and derive
Figure 3.5: (a) Capacitance distribution in a 10 GHz switched MIM capacitor LC-VCO. (b) Capacitance distribution in a 40 GHz switched MIM capacitor LC-VCO.
the tuning range vs. the oscillation frequency, the inductor, capacitors, along with the $g_m$ transistors are further analyzed.

**RF passives in the LC-tank**

The frequency dependent inductance and $Q$ of the optimal inductor can be obtained from (2.2) and (2.5). Capacitive components in LC-tank includes several different capacitors. Routing capacitance ($C_{rt}$) is fixed for VCO designs with same routing trace. The parallel resistive loss ($R_{rt}$) may change as the frequency changes due to skin effect. However, since $C_{rt}$ is only a small fraction of total capacitance, $R_{rt}$ is assumed to be fixed across frequency. The buffer and the VCO core are AC coupled through a small coupling capacitor. This coupling capacitor is fixed with low loss. Hence, the effective buffer capacitance $C_{buf}$, which is the series capacitance of the coupling capacitor and the input capacitance of the buffer, can be assumed to be fixed without losses. The transistor capacitance $C_t$ will be calculated as part of the cross-coupled pair. It is assumed lossless since the loss will be accounted for in the cross-coupled pair negative resistance part (i.e. $g_m$). The remaining capacitance is attributed to the fine and coarse tuning structure, which will be analyzed separately. As mentioned earlier, the digitally-switched varactor coarse tuning structure has superior $Q$ over switched MIM-caps (Chapter 3).

By adopting a varactor coarse tuning structure, the capacitance and $Q$ of the fine and coarse tuning can be lumped together in the analysis. If varactors with different sizes are used, the on and off capacitance can be calculated from the varactor model (Chapter 3). However, to reduce the impact of mismatch across the C-DAC array, the tuning structure with minimum capacitance is designed as unit cell (LSB unit). The additional capacitance from higher order bits are arrayed in multiple of the unit...
cells, as shown in Figure 3.6. Therefore, the tuning range of the whole structure is the same as the unit cell. Off state capacitance $C_{v,\text{off}}$ and the tuning range $m$, $m = C_{v,\text{on}}/C_{v,\text{off}}$, can be used to characterize the capacitance of the tuning structure. It is worth noting that $C_{v,\text{off}}$ and $m$ remains constant in the mm-wave range.

Figure 3.6 shows equivalent circuits of the varactor array. The $Q$-factor of varactors is inversely proportional to frequency. Using $R_{v,\text{off}}$, which equals $Q_{v,\text{off}}/\omega C_{v,\text{off}}$, to represent the varactor loss, $R_{v,\text{off}}$ is found to be constant across frequency. Hence, $R_{v,\text{off}}C_{v,\text{off}}$ can be expressed as a constant $\tau_{\text{off}}$. The varactor coarse and fine tuning structure can be completely characterized for both off and on conditions using four frequency independent parameters: $C_{v,\text{off}}$, $m$, $\tau_{\text{off}}$ and $\tau_{\text{on}}$. 
The values of the inductor and capacitors in the LC-tank determine the VCO oscillating frequency, while the tank $Q$ dictates the required $g_m$ to satisfy the startup condition. Since phase noise is proportional to $Q^2$ in Lesson’s equation (2.16), and the output power is also proportional to the tank $Q$, a high $Q$ tank can significantly reduce the phase noise of the VCO. As frequency increases, the inductor $Q$ increases. However, the capacitor $Q$ decreases. The LC-tank overall $Q$ can be written as

$$\frac{1}{Q_{\text{tank}}} = \frac{1}{Q_{\text{ind}}} + \frac{1}{Q_{\text{cap}}}$$ (3.2)

where $Q_{\text{ind}}$ and $Q_{\text{cap}}$ are the quality factors of the inductor and the capacitor, respectively.

Although the $Q$-factor of capacitive components remains fairly constant with the size of capacitor, the $Q$-factor of inductors changes with inductor size and frequency. To optimize the tank overall $Q$-factor, the inductor with highest $Q$ is selected (Chapter 2) and its $Q$-factor is plotted in Figure 3.7. Therefore, the overall tank $Q$ ($Q_{\text{tank}}$) is dominated by the capacitive component, and decreases with frequency, as shown in Figure 3.7.

**Transconductance of Cross-Coupled Pair**

The negative resistance is designed according to (2.15), where $\eta$ is set to 2.5 to satisfy oscillation startup condition with sufficient margin. In a long channel process, both the bias current and the width of transistors can be controlled to increase $g_m$.

In deep submicron technologies, however, owing to the velocity saturation effects, the short channel $g_m$ at low frequencies can be represented as [85]

$$g_m = \frac{1}{2} \mu C_{ox} W E_{sat}$$ (3.3)
Figure 3.7: The quality factor of the inductor, capacitance and LC-tank in VCO changes as the frequency increases.

where $\mu$ is the channel mobility, $C_{ox}$ is the oxide capacitance, $W$ is the transistor width, and $E_{sat}$ is the carrier velocity saturation field. Equation (3.3) shows that for a short channel device, $g_m$ has a weak dependency on current and can only be increased by enlarging the device width. Doubling the current from 10 mA to 20 mA in a 80 $\mu$m/0.13 $\mu$m device slightly increases the $g_m$ from 25 mS to 27 mS, as shown in Figure 3.8. Although the magnitude of the bias current has a small impact on $g_m$, it is set relatively high to obtain maximum voltage swing and hence minimize phase noise.

It is worth noting that when shifting to mm-wave frequencies, the VCO may not oscillate if only the DC $g_m$ of transistors satisfies the oscillation startup condition. By examining $g_m$ of the cross-coupled pair, one can see that it dramatically decreases as
the frequency increases [103]. To better explain this behavior, the transconductance of the cross-coupled pair \( g_{m_{\text{x CPL}}} \) is analyzed from the small signal equivalent circuit shown in Figure 3.9(a). The single-ended input reactance of the cross-coupled pair can be written as

\[
Y_{in}(s) = \frac{1}{r_o} + 2sC_{gd} + sC_{db} + (sC_{gs} + 2sC_{gd} - g_m) \frac{1/R_g - sC_{gd}}{1/R_g + sC_{gs} + sC_{gd}} \quad (3.4)
\]

The real part, which is the frequency dependent \( g_{m_{\text{x CPL}}} \), can be derived from the above equation

\[
g_{m_{\text{x CPL}}}(f) = g_m - \frac{1}{r_o} - g_m \frac{4(f_{\text{max}}/f_T)^2r(2r + 1)^2 + (r + 1)(2r + 1)}{16r^2 f_{\text{max}}^4/f^2 f_T^2 + (r + 1)^2} \quad (3.5)
\]
Figure 3.9: (a) Small signal equivalent circuit of a cross-coupled pair. (b) Cross-coupled pair single-ended $g_m$ degradation and capacitance vs. frequency for different $f_T$ and $f_{max}$. 
where $r$ is the ratio between $C_{gd}$ and $C_{gs}$, $f$, $f_T$ and $f_{\text{max}}$ are the operating frequency, unity current gain frequency and unity power gain frequency of the transistor, respectively. $f_T$ and $f_{\text{max}}$ are given by

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}$$  \hspace{1cm} (3.6)

$$f_{\text{max}} = \frac{f_t}{2\sqrt{\frac{2}{\pi R_g C_{gd}}}}.$$  \hspace{1cm} (3.7)

The $g_m$ degradation in percentage, which is defined as $(g_m - g_{m,\text{xcpl}})/g_m$, is plotted for different transistor $f_T$ and $f_{\text{max}}$ in Figure 3.9(b). $g_m$ has a significant degradation at high frequencies. At low frequency (< 10 GHz), the $g_m$ degradation is flat with a nonzero value. This is due to the finite $r_o$ reducing the effective $g_m$. It is worth noting that $f_{\text{max}}$ has a significant impact on the high frequency $g_m$ degradation, while the $g_m$ degradation is small when $f_T$ decreases. Since $f_{\text{max}}$ is related the resistive losses in the transistors, including gate resistive loss ($R_g$), without considering these losses, $g_{m,\text{xcpl}}$ is unchanged over the entire frequency range. When the frequency increases to be comparable to $f_{\text{max}}$, $g_{m,\text{xcpl}}$ decreases significantly. To satisfy the VCO startup condition in mm-wave VCOs, $g_m$ must be increased to compensate for both high frequency transconductance reduction and the degradation in tank $Q$. From (3.3), the increase in transistor $W$, which largely increases the VCO fixed capacitance, is the only viable option to increase $g_{m,\text{xcpl}}$ at the target frequency.

The imaginary part of $Y_{in}$, implying fixed parallel capacitance from the cross-coupled pair, is extracted as

$$C_t(f) = 2C_{gd} + C_{db} + C_{gd}\frac{(2r+1)(4+16r(f_{\text{max}}/f_T)^2-(r+1)(f/f_{\text{max}})^2]}{164^2(f_{\text{max}}/f_T)^2 + (r + 1)^2(f/f_{\text{max}})^2}.$$  \hspace{1cm} (3.8)

54
$C_t$ has small dependent on frequency, as shown in Figure 3.9(b). Since $C_{gd}$ and $C_{db}$ are proportional to the width of the transistor with minimum length, $C_t$ is approximately proportional to transistor $W$.

To obtain the tuning range of the VCO with highest operating frequency of $\omega_H$, the inductor $L$ can be selected to have highest $Q_{ind}$ from Figure 2.7. Using (2.1), $\omega_H$ can be represented as

$$\omega_H = \frac{1}{\sqrt{L(C_t + C_{rt} + C_{buf} + C_{v,off})}}.$$  \hfill (3.9)

The tank parallel resistance can be derived by paralleling resistance from each lossy components,

$$R_{tank} = \omega_H L Q_{ind} / / R_{rt} / / \frac{\tau_{off}}{C_{v,off}}.$$  \hfill (3.10)

By setting the oscillation startup margin to $2\times$,

$$g_{m,\text{geq}} = \frac{4}{\omega_H L Q_{ind} / / R_{rt} / / \frac{\tau_{off}}{C_{v,off}}}.$$  \hfill (3.11)

$C_{v,off}$ can then be solved from (3.5), (3.3) and (3.8). The tuning range can then be calculated by using (3.1), where $C_{var} = (m - 1)C_{v,off}$. The tuning range of several VCOs is calculated using 130 nm CMOS process parameters, and the results are plotted in Figure 3.10. The same VCOs are designed, simulated and compared with the calculated results.

### 3.3 Phase Noise Limits of mm-wave VCOs

Due to the decrease in tank $Q$ and increase in transistor $g_m$, the phase noise degrades as frequency increases. An exact analysis of phase involves complicated mathematically derivation and usually cannot provide useful design insights. Instead, Leeson’s formula provides a basic relationship between phase noise and frequency in
VCOs. Without considering varactor AM–PM conversion effect, Leeson’s formula can be written as \[80]\]

\[
L(\Delta f) = 10 \log \left\{ \frac{2FkT}{P} \left( \frac{f_0}{2Q \Delta f} \right)^2 \left( 1 + \frac{f_c}{\Delta f} \right) \right\}
\]

(3.12)

The excess noise factor is given by \[79]\]

\[
F = 2 + \frac{8\gamma I_{bias} R_{tank}}{\pi V_{max}} + \frac{8\gamma g_{m,bias} R_{tank}}{9\alpha}
\]

(3.13)

where \(\alpha\) and \(\gamma\) are approximately 0.6 and 3 in 130 nm process, respectively, \(I_{bias}\) is the bias current of the VCO, \(g_{m,bias}\) is the bias transistor transconductance and \(V_{max}\) is the amplitude of the output swing. The operating frequency is given by (3.9) and the tank \(Q\) is

\[
Q = Q_{ind} \frac{1}{\omega_H L} \frac{1}{\omega L C_{v,off}}
\]

(3.14)
The phase noise is evaluated at 1 MHz offset and shown in Figure 3.11. The phase noise of afore-designed VCOs are also simulated and plotted in the same figure for comparison. The calculation results are consistent with the simulation. The phase noise of the VCO in the same process increases significantly when the operating frequency increases to be close to the unity gain frequency of transistors.

Figure 3.11: CMOS LC-VCO phase noise at 1 MHz offset vs. different mm-wave frequencies.
Chapter 4: Design and Analysis of Negative Capacitance Circuits

4.1 Introduction to Negative Capacitance Circuits

The idea of negative capacitance was first introduced in 1931 [100]. Linvill [58] later proposed negative impedance converters (NICs) to transform a real capacitor into an equivalent negative capacitor, as shown in Figure 4.1(a). The diagram in Figure 4.1(b) is a notional illustration of the NIC concept and structure. Ideally, the input impedance $Z_{\text{in}} = Z/(1 - A)$ is negative if $A > 1$. An earlier demonstration of an NC circuit utilizing a discrete op-amp extended microcomputer data bus speeds to tens of MHz [86]. In [30], a transimpedance amplifier (TIA) with an integrated NC circuit achieved 6 GHz of bandwidth. The efficiency of a Class-E power amplifier is proved to increase by adopting an NC circuit [90]. An NC utilized in SRAM is shown to improve its yield [67] and an NC utilized in a transformer structure is shown to improve its bandwidth [29]. However, there is little in the literature describing the bandwidth limitations of the NC circuits and address their applicability to mm-wave circuits. This chapter presents a comprehensive analysis of various wideband NC circuits. An FOM is introduced for comparison among various parameters, including large signal behavior and bandwidth limitations.
A simple single-ended NC circuit can be realized by using a single pole amplifier with a feedback capacitor $C$ [86], with the resulting transfer function expressed by

$$A = \frac{V_o}{V_i} = \frac{g_m R_o}{1 + sR_o C_o},$$

(4.1)

where $C_o$ and $R_o$ represent the amplifier total output capacitance and resistance, respectively. The NC bandwidth is determined by $A$, which is a function of $C_o$ (around the feedback capacitance $C$) and $R_o$. $R_o$ is typically in the range of few k-Ohm for high gain amplifiers, resulting in a 3-dB frequency in the hundreds of MHz. Consequently, the bandwidth of this NC topology is insufficient for mm-wave applications.

A one-stage amplifier can replace the op-amp to achieve better bandwidth [18], as shown in Figure 4.2(a). An NC circuit can also be built with a cross-coupled pair combined with an inductor [28,29], as shown in Figure 4.2(b) and Figure 4.2(c). The bandwidth of these two circuits is limited since the inductor can only operate at a certain frequency range. Furthermore, large silicon area is required to implement the inductors on chip.
4.2 Single-ended Negative Capacitance Circuits

An architecture consisting of two inverters with a feedback capacitor $C$ is shown in Figure 4.3(a) [104]. A feedback resistor, $R$, is added in the second stage to lower the output impedance to $R/(1 + A_2)$, where $-A_2$ is the voltage gain of the second stage. Meanwhile, $R$ self biases the second inverter since a capacitor $C_{bias}$ is inserted between two inverters to isolate DC biases. By using small signal equivalent circuit in Figure 4.3(b), $A_2$ can be calculated as

$$A_2 = \frac{g_{m1}(g_{m2}R - 1) + sRC(g_{m2}C_{gs} + 1)}{g_{m1}(sRC + 1) - sC}$$  (4.2)

where $g_{m1}$ and $g_{m2}$ are transconductance of the first and the second inverter, respectively.
To further illustrate the bandwidth improvement of this circuit, the input capacitance is calculated as (assume $C_{\text{bias}}$ is sufficiently large)

$$C_{\text{in}} = C(1 - A) + C_{\text{gd}}(1 + A) + C_{\text{gs}}$$  \hspace{1cm} (4.3)

where $C_{\text{gs}} = C_{\text{gs,p}} + C_{\text{gs,n}}$ and $C_{\text{gd}} = C_{\text{gd,p}} + C_{\text{gd,n}}$. Note that the bandwidth limitation can be derived from the first term, where the transfer function $A$ can be expressed in terms of the first and second inverter’s gain, $-A_1$ and $-A_2$, respectively:

$$A = A_1 A_2 g_{m1} R (g_{m2} R - 1) + s R C (s C_{gs2} + 1) \frac{(s R C + 1)(s R C_{gs2} + 1)}{(s R C + 1)(s R C_{gs2} + 1)} + g_{m2} R.$$  \hspace{1cm} (4.4)

To a first-order approximation, the 3-dB bandwidth is $1/2\pi R C$. Compared to (4.1), this 3-dB bandwidth can be up to few tens of GHz. The input capacitance plotted in Figure 4.4(a) as solid blue line shows the bandwidth of the circuit. The inset in Figure 4.4(a) shows the exploded view. This circuit is designed and simulated in a 130 nm process and the simulated result is consistent with the theoretical analysis.
Inserting a 1.5 nH inductor to the NMOS gate path (Figure 4.3(a)) can further extend the bandwidth of the NC circuit (dashed red line in Figure 4.4(a)).

The above NC circuit is scalable by changing the feedback capacitor $C$. From (4.3), the input NC has a linear relationship with $C$ when $A$ and $A_1$ are constant. Figure 4.4(b) shows this relationship at 10 GHz. At this frequency, $A$ and $A_1$ are unchanged even when the feedback $C$ changes from 100 fF to 300 fF. However, the 3-dB frequency is proportional to $g_{m2}/(2\pi C)$, and hence, when $C$ continues to increase, the bandwidth decreases.

The large signal operation of the aforementioned circuit needs to be carefully studied since the NC changes as a function of the input signal amplitude. This is attributed to the change of the input bias voltage, which reduces $g_m$ and consequently $A$ and $A_1$. To obtain the large signal response of this two-inverter NC circuit, the large signal transconductance of the first stage is derived as

$$G_{m1} = \begin{cases} g_{m1}, & V_p \leq \frac{V_{dd}}{2A_1} \\ \frac{2}{\pi} \sin^{-1} \left( \frac{V_{dd}}{2A_1V_p} \right) \cdot g_{m1}, & V_p > \frac{V_{dd}}{2A_1} \end{cases} \quad (4.5)$$

where $V_p$ is the amplitude of the input sinusoidal signal. $g_{m1}$ is given by

$$g_{m1} = \mu_n C_{ox} \frac{W_{n1}}{L} (V_{dd} - V_{th,n1} + V_{th,p1}) \quad (4.6)$$

if $g_{m1,p}$ is set to equal $g_{m1,n}$. The second stage transconductance, $G_{m2}$, can similarly be calculated. Substituting $G_{m1}$ and $G_{m2}$ in (4.4), the large signal $C_{in}$ is calculated and the result is plotted at 10 GHz, as shown in Figure 4.5(a). It is worth noting that (4.5) contains $A_1$, and thus, a recursive method is necessary to solve the equation. The simulated large signal $C_{in}$ in a 130 nm process (VDD=1.2 V, $W_{1,n}=36$ $\mu$m, $W_{2,n}=32$ $\mu$m) is also shown in Figure 4.5(a) and the results are consistent with the calculation in (4.5). The NC reduces as the amplitude of the input signal increases.
Figure 4.4: (a) Simulation results of the NC circuits. (b) The relationship between input NC and the feedback capacitor with bandwidth.
To maintain negative $C_{in}$, the input signal amplitude should be below 0.6 V. The resultant DC power consumption of this NC circuit is simulated as 1.2 mW at 10 GHz, as shown in Figure 4.5(b).

### 4.3 Differential Negative Capacitance Circuits

A differential NC structure is more attractive in circuits with differential signals. Using a differential amplifier can construct a differential NC circuit, as shown in Figure 4.6(a). However, this circuit encounters the same bandwidth problem as the single-ended amplifier NC circuit in Figure 4.1(b). Alternatively, the NMOS/PMOS cross-coupled pairs topologies in Figure 4.6(b) and 4.6(c) not only use a small capacitor $C$ to substitute $2 \times 2C$ but also can increase the bandwidth significantly. The small signal equivalent circuit of Figure 4.6(b) is shown in Figure 4.6(d). Since the input signals are differential, the capacitor at the source can be split into two capacitors. From small signal analysis, the single-ended input impedance can be written as

$$Z_{in}(s) = -\frac{s(C_{gs} + 2C_{cl}) + g_m}{(g_m - sC_{gs})s2C + 4sC_{gd}[s(C_{gs} + 2C_{cl}) + g_m]}.$$  

(4.7)

At first-order approximation, the bandwidth is determined by $g_m/2\pi(1+2C_{cl}/C_{gs})C_{gs}$.

Compared to the two-inverter NC circuit in Figure 4.3(a), the bandwidth of this circuit is superior (Figure 4.7(a)). The input negative capacitance can be calculated as

$$C_{in}(\omega) = -2C_{cl}\frac{g_m^2 - \omega^2C_{gs}(C_{gs} + 2C_{cl})}{g_m^2 + \omega^2(C_{gs} + 2C_{cl})^2} + 4C_{gd}.$$  

(4.8)

The amount of canceled capacitance $C_{NC}$ is $C_{in} - C_{cc}$, where $C_{cc}$ is transistor capacitance contribution with value of $2C_{gs} + 4C_{gd}$. When $\omega << \omega_T$, $C_{NC}$ linearly scales with the capacitor $C$ and is equal to $-2C_{cl} - 2C_{gs}$. Figure 4.7(b) shows this.
Figure 4.5: (a) Large signal input negative capacitance. (b) The power consumption at different frequency.
Figure 4.6: (a) A differential pair NC circuit. (b) A drain input cross-coupled NC circuit. (c) A source input cross-coupled NC circuit. (d) Small signal equivalent circuit of the drain input cross-coupled NC circuit.
relationship between the input capacitance and the source capacitance at 10 GHz. For this NC structure, considering the first order approximation in (4.8), the input capacitance is not related to the amplitude of the input signal unless the large input signal causes the current source to operate out of the saturation region. The NC circuit in Figure 4.6(c) has similar performance in NC. However, the input resistance is positive, while it is negative in Figure 4.6(b).

The addition of 200 pH inductors to the cross-coupling path results in an increase in the bandwidth of operation. To further illustrate the circuit operation, the topology in Figure 4.6(b) with and without inductors was simulated and the single-ended capacitance is plotted in Figure 4.7(a). A negative capacitance of 205 fF can be achieved up to a frequency of 80 GHz with a bias current of 2 mA. Without inductors, the bandwidth is only around 32 GHz. It is worth noting that bandwidth scales with advanced technology, which makes this circuit very attractive for mm-wave applications.

4.4 Technology Scaling of Negative Capacitance Circuits

If a better process is employed, the NC circuit can achieve better performance. Figure 4.8 illustrates the normalized NC values that can be obtained at 40 GHz for different device $f_T$s. Using a process with an $f_T$ of 150 GHz, an NC of $-3C_{gs}$ can be obtained. In contrast, the maximum NC in a process with an $f_T$ of 100 GHz is only $-2.2C_{gs}$. This technology scaling effect has been verified by designing the NC circuit in both 130 nm and 90 nm nodes. Figure 4.8 shows both calculated and simulated results. The simulation is consistent with the calculation.
Figure 4.7: (a) Simulation results of the cross-coupled NC circuit in Figure 4.6(b).
(b) The relationship between input NC and the source capacitor.
4.5 Performance Comparison

To compare the performance of aforementioned NC circuits, an FOM is proposed and is defined as following

\[
FOM = 20 \log \left( \frac{\text{NC}}{1 \text{pF}} \right) + 20 \log \left( \frac{\text{BW}}{1 \text{Hz}} \right) - 20 \log \left( \frac{\text{area}}{1 \mu \text{m}^2} \right) + 20 \log \left( \frac{V_p}{1 \text{mV}} \right) - 10 \log \left( \frac{P}{1 \text{mW}} \right)
\]

(4.9)

where BW is the bandwidth of NC circuit, area is the die area the circuit occupying, \( V_p \) is the maximum acceptable AC input voltage amplitude, \( P \) is the power consumption measured at the highest frequency in the bandwidth. The specification and the FOM of different NC circuits are listed in Table 4.1. It is worth noting that the 2× multiplier is applied to single-ended circuits to normalize the area and power.
consumption. From Table 4.1, the NC circuit in Figure 4.3(a) has the best FOM, and is preferred especially in single-ended applications.

<table>
<thead>
<tr>
<th>NC circuit</th>
<th>NC (pF)</th>
<th>BW (GHz)</th>
<th>Area ($\mu m^2$)</th>
<th>Max $V_p$ (mV)</th>
<th>$P$ (mW)</th>
<th>FOM (dB)</th>
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</thead>
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<tr>
<td>Figure 4.1(b) w/FB C, 4.6(a)</td>
<td>-0.2</td>
<td>0.15</td>
<td>2×8000</td>
<td>100</td>
<td>2×0.2</td>
<td>109</td>
</tr>
<tr>
<td>Figure 4.3(a)</td>
<td>-0.2</td>
<td>16</td>
<td>2×600</td>
<td>400</td>
<td>2×1.2</td>
<td>177</td>
</tr>
<tr>
<td>Figure 4.3(a) with ind</td>
<td>-0.2</td>
<td>28</td>
<td>2×11000</td>
<td>400</td>
<td>2×1.2</td>
<td>156</td>
</tr>
<tr>
<td>Figure 4.6(b), 4.6(c)</td>
<td>-0.2</td>
<td>32</td>
<td>3500</td>
<td>600</td>
<td>3</td>
<td>176</td>
</tr>
<tr>
<td>Figure 4.6(b), 4.6(c) with ind</td>
<td>-0.2</td>
<td>80</td>
<td>24000</td>
<td>600</td>
<td>3</td>
<td>167</td>
</tr>
</tbody>
</table>
Chapter 5: Tuning Range Extension in mm-wave CMOS LC-VCOs

This chapter focuses on using the aforementioned NC circuit to reduce the fixed capacitance in the LC-tank and thus extend the VCO tuning range. Tunable NC structures are analyzed and demonstrated to extend the tuning range significantly with minimal impact on phase noise, power consumption or chip area. Unlike other techniques only applicable at low frequencies, the tunable NC circuit effectively cancels the fixed capacitance in the LC-VCO tank at mm-wave frequency range and creates an extra freedom on the tank capacitance by controlling the amount of canceled capacitance to further increase the tuning range.

5.1 Tuning Range Extension with NC

When connecting an NC circuit to the VCO tank, the fixed capacitance reduces, as shown in Figure 5.1. To maintain the same oscillation frequency, more tuning capacitance (including fixed capacitance $C_{add,fix}$ and variable capacitance $C_{add,var}$) can be added to the LC-tank, which increases the tuning range. Assume the negative capacitance, $C_{NC}$, is set to a fraction of $C_{fix}$, $C_{NC} = aC_{fix}$, the tuning range is rewritten as

$$TR_{VCO} = 2 \cdot \frac{\sqrt{C_{tank}} - \sqrt{[1 - a(1 - 1/b)]C_{fix}}}{\sqrt{C_{tank}} + \sqrt{[1 - a(1 - 1/b)]C_{fix}}} \quad (5.1)$$
Figure 5.1: The NC circuit cancels fixed capacitance in the LC-VCO tank.

where $C_{tank}$ is the total capacitance in the LC-tank, and $b$ is the tuning range of added tuning structure to the tank. $b$ is given by $(C_{add,fix} + C_{add,var})/C_{add,fix}$. Figure 5.2 shows the tuning range improvement for the aforementioned 40 GHz VCO with $a = 30\%$ and $b = 2$. Due the fact that adding variable capacitance to the LC-tank to compensate for the subtracted NC also adds fixed parasitic capacitance, the increase in tuning range is limited. Further altering the fixed NC to variable NC, assume the maximum canceled capacitance is $C_{NC,max}$ and the minimum canceled capacitance is
The tuning range becomes

\[
TR_{\text{VCO}} = 2 \cdot \frac{\sqrt{C_{\text{tank}}} - \sqrt{[1 - a(2 - 1/b - 1/c)]C_{\text{fix}}}}{\sqrt{C_{\text{tank}}} + \sqrt{[1 - a(2 - 1/b - 1/c)]C_{\text{fix}}}} \quad (5.2)
\]

where \( c \) is tuning range of the \( C_{\text{NC}} \) and is given by \( C_{\text{NC, max}}/C_{\text{NC, min}} \). If the variable NC is implemented using a varactor pair, \( c \) is approximately 2. The tuning range of the aforementioned 40 GHz VCO (\( C_{\text{fix}}/C = 77\% \)) can be further increased by 25% (from 19% to 24%) compared to the VCO with the fixed NC structure, as shown in Figure 5.2. Another implementation of the variable NC is to use a MOS switch. The gate-drain/source capacitance of the switch can provide NC when it is off. When it is on, if the resistance of the switch is ignored, the NC is zero since the two terminals of the switch are shorted. Therefore, \( c \) is \( \infty \), and the tuning range can be expressed as

\[
TR_{\text{VCO}} = 2 \cdot \frac{\sqrt{C_{\text{tank}}} - \sqrt{[1 - a(2 - 1/b)]C_{\text{fix}}}}{\sqrt{C_{\text{tank}}} + \sqrt{[1 - a(2 - 1/b)]C_{\text{fix}}}}. \quad (5.3)
\]

The increase in tuning range for the same 40 GHz VCO can be up to 60% (from 19% to 30%), as shown in Figure 5.2. Hence, the increase in tuning range of the switched NC VCO is 3\times of that of the fixed NC VCO. It is worth noting that in the LC-tank, a switch cannot be directly added since it connects two differential terminals when the switch is on and hence shorts the inductor and capacitors in the LC-tank. However, it is possible to be in an NC structure. The following part will reveal detailed structures and analysis of varactor and switch NC circuits.

### 5.2 Bottom-biased LC-VCO with NC

An early demonstration of the tuning range extension with NC circuit in LC-VCO is described in [101], where two inductor-based NC circuits are utilized, occupying a
large die area and consuming additional power. In this work, since the proposed NC structure in Figure 4.6(b) lends itself to the bottom-biased VCO structure (Figure 2.3) without the addition of any auxiliary structure or extra power, the two circuits are simply combined together, as shown in Figure 5.3, where the VCO tank remains the same, while the added NC capacitor \( (C_{cl}) \) provides the target cancelation. This structure was also shown to reduce the impact of flicker noise in the cross-coupled pair [34]. Considering a high frequency \( g_m \) reduction factor of 20\%, the width of transistors \( M_{1,2} \), which determines \( C_{gs} \) and \( g_m \), is optimized to maximize the NC performance while satisfying the startup condition of the VCO. It is worth noting that no extra power consumption is incurred when adding the NC to the standalone

Figure 5.2: The tuning range extension in LC-VCO with fixed and variable NC circuits.
5.2.1 LC-VCO with Fixed NC

Within the bandwidth of operation, the input NC changes linearly with $C_{cl}$, as shown in Figure 4.4(b). However, in the proposed design, the VCO operates above the 3-dB bandwidth of the NC circuit and near the transistor $f_T$. To examine the amount of canceled parallel capacitance $C_{NC}$, which is expressed as

$$C_{NC} = C_{in} - C_{cc}$$

(5.4)
where $C_{in}$ is the capacitance of the NC structure seen from the tank and $C_{cc}$ is the fixed capacitance of the cross-coupled pair, $C_{cc} = 2C_{gs} + 4C_{gd}$, (4.8) can be rewritten as

$$\frac{C_{NC}}{C_{gs}} = -\frac{2h[1 - (f/f_T)^2(1 + 2h)]}{1 + (f/f_T)^2(1 + 2h)^2} + \frac{4C_{gd} - C_{cc}}{C_{gs}} \quad (5.5)$$

where $h$ is the normalized capacitance of $C_{cl}$, $h = C_{cl}/C_{gs}$. Figure 5.4(a) shows the ratio of $C_{NC}$ that can be obtained at 40 GHz relative to the intrinsic gate capacitance $C_{gs}$, as a function of $C_{cl}/C_{gs}$. As $C_{cl}$ increases, the absolute value of $C_{NC}$ increases to a maximum, then decreases due to bandwidth limitation. A maximum cancelation of $2C_{gs}$ is obtained when $C_{cl} = C_{gs}$.

The input parallel resistance $R_{in}$, which can be extracted from (4.7) and is shown as solid line in Figure 5.4(b), is also dependent on $C_{cl}$. When $C_{cl}$ is set to 0, the circuit displays poor negative resistance, which is attributed to infinite impedance at the source of cross-coupled pair leading to reduced $g_m$ (source degeneration). While large $C_{cl}$ results in $R_{in}$ approaching $-1/g_m$, which is the same as that of the cross-coupled pair. Since the reference VCO is designed using a tank with parallel resistance ($R_p$) of 80 Ω, the absolute value of $R_{in}$ is required to be smaller to start oscillation. In practice, $R_{in}$ is designed to be a factor of two smaller than $R_p$ to allow for startup margin. The choice of $C_{cl} = C_{gs}$, while it optimizes the NC, fails to satisfy the startup condition with $2\times$ margin, as shown in Figure 5.4(b). Increasing the $g_m$ of $M_{1,2}$ can set the negative resistance to satisfy the startup condition, but it also leads to higher fixed capacitance. Alternatively, by choosing the capacitor $C_{cl}$ to be $1.5C_{gs}$, without increasing the size of $M_{1,2}$, the VCO can start oscillation with $2\times$ margin, while $C_{NC}$ is slightly reduced by 5% from the optimum value.
Figure 5.4: Simulated negative capacitance $C_{NC}$ (a) and parallel resistance (b) seen by the tank vs. added cancelation capacitance $C_{cl}$ for different quality factor of $C_{cl}$.
Using the above NC approach, the fixed capacitance $C_{fix}$ is reduced by 25%. This leads to an upward shift in the center oscillation frequency by 10% with little impact on the tuning range, as shown in Figure 5.5. To increase the tuning range while maintaining the target center frequency, the size of fine and coarse tuning capacitors are increased. However, as a result of increasing the size of the varactors, the fixed portion of their capacitance is also increased, resulting in 20% increase in tuning range compared to the reference VCO, as illustrated in Figure 5.5.

5.2.2 LC-VCO with Varactor Based Variable NC

To further extend the tuning range, the NC capacitor $C_{cl}$ is implemented to be variable [106]. However, the loss from the tuning structure and the bias current source with finite $R_{on}$ should be considered. The overall losses are represented by the resistor
$R_{cl}$, and the amount of canceled tank capacitance $C_{NC}$ can be represented as

$$\frac{C_{NC}(f)}{C_{gs}} = \frac{2h\left[1 -(1+2h)\left(\frac{f}{f_T}\right)^2 - \frac{4h}{Q_{cl}}\left(1+\frac{h}{Q_{cl}}\frac{f}{f_T}\right)\left(\frac{f}{f_T}\right)\right]}{(1 + 2\frac{h}{Q_{cl}}\frac{f}{f_T})^2 + (1 + 2h)^2\left(\frac{f}{f_T}\right)^2} + \frac{4C_{gd} - C_{ce}}{C_{gs}}$$  \hspace{1cm} (5.6)

The impact of finite $Q_{cl}$ on $C_{NC}$ is illustrated in Figure 5.4(a). Since the NC impact reduces as $C_{cl}$ decreases, a better cancelation can be achieved by adopting a capacitor with high $Q_{cl}$. The negative input resistance $R_{in}$ can be derived as

$$R_{in}(f) = -\frac{\left[(1 + 2\frac{h}{Q_{cl}}\frac{f}{f_T})^2 + (1 + 2h)^2\left(\frac{f}{f_T}\right)^2\right]}{2\left(1 + 2\frac{h}{Q_{cl}}\frac{f}{f_T}\right) + 4Q_{cl}(1+h)\left(\frac{f}{f_T}\right) - 2\left(\frac{f}{f_T}\right)^2}R_{cl}$$  \hspace{1cm} (5.7)

As shown in Figure 5.4(b), the negative resistance is minimally impacted by $Q_{cl}$. To satisfy the oscillation startup condition with 2x margin for the VCO, $C_{cl}$ can be selected to be $1.5C_{gs}$ instead of $C_{gs}$.

To implement the variable NC structure, a digitally-switched varactor NC structure is utilized, as shown in Figure 5.6. The varactor is designed to operate in only two states: on and off. The $Q$ of the varactor is sufficiently high compared to the bias current source, as shown in Figure 5.7. Therefore, $Q_{cl}$ is dominated by the bias.
current source and can be approximated as $2\pi f (C_{cl_v} + C_{cl_b}) R_{cl_b}$. Switching the varactor from off to on, $C_{cl}$ changes from $1.5C_{gs}$ to $3.5C_{gs}$ with $Q_{cl}$ increases from 2.5 to 3.5. The NC remains nearly unchanged between the on/off states (dashed arrow in Figure 5.8), and hence the tuning range only increases by less than 1% compared NC VCOs where fixed NC is not variable.

To exploit the varactor on/off modes towards a wider tuning range, a feature of MOS varactors can be used, whereas the $Q$-factor of an off varactor is significantly higher than that of an on varactor [23], as shown in Figure 5.7. At 40 GHz, an off varactor with minimal finger length ($L = 0.24 \, \mu m$) has $Q$ of 100, while the $Q$-factor is 10 when it is switched on. Furthermore, the $Q$-factor of a MOS varactor is controllable by altering the finger length, as shown in Figure 5.7. By increasing the length of the varactor, $R_{cl_{v\_b}}$ of an on varactor can be smaller than $R_{cl_{\_b}}$, while $R_{cl_{\_v}}$
<table>
<thead>
<tr>
<th>Varactor Type</th>
<th>High Q</th>
<th>Low Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>Varactor Status</td>
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<td>On</td>
</tr>
<tr>
<td>$Q_{cl,v}$</td>
<td>90</td>
<td>10</td>
</tr>
<tr>
<td>$Q_{cl,b}$</td>
<td>2.3</td>
<td>2.3</td>
</tr>
<tr>
<td>$Q_{cl}$</td>
<td>2.5</td>
<td>3.5</td>
</tr>
<tr>
<td>$C_{NC}$</td>
<td>-1.2</td>
<td>-1.2</td>
</tr>
</tbody>
</table>

of an off varactor is several times higher than $R_{cl,b}$. In this case, when the varactor is off, the current source dominates $Q_{cl}$, while the varactor dominates $Q_{cl}$ when it is on. Table 5.1 shows an example of manipulating the varactor $Q$-factor to obtain wide tuning range. By utilizing a low $Q$ varactor, when $C_{cl}$ tunes from $1.5C_{gs}$ to $3.5C_{gs}$ (varactor off to on), $Q_{cl}$ decreases from 3.5 to 2.5, resulting in the NC changes from $-1.64C_{gs}$ to $-0.82C_{gs}$, as shown in the solid arrow in Figure 5.8. This in turn shifts the center frequency from 39 GHz to 41.5 GHz and increases the VCO tuning range.

The Bottom-biased NC LC-VCO is designed using the aforementioned approach. The layout of this design is shown in Figure 5.9. Without using inductors, the additional NC does not increase the VCO core size since the NC can be placed behind the tank structure.

### 5.3 Top-biased LC-VCO with NC

Since the bias circuit for a top-biased VCO and the cross-coupled NC circuit are different, they cannot directly combined together. Examining the function of the bias circuitry in the NC circuit, one can see that the ideal current sink only provides DC...
current. Since an inductor passes the DC signal and blocks RF signal at a specific frequency range (when tuned with the source node capacitance), it can be used to substitute for the current sink. Therefore, the NC circuit can be combined with the top-biased VCO, where the VCO tank and bias circuit remain the same, while the added NC capacitor ($C_{cl}$) along with the inductor provides tank capacitance cancelation, as shown in Figure 5.10.

The NC capacitor $C_{cl}$ can be implemented to be variable to further extend the tuning range. Since the VCO has the fine tuning structure, $C_{cl}$ is only required to switch between two states: maximum capacitance ($C_{cl, on}$) and minimum capacitance ($C_{cl, off}$). The loss of the tuning structure can be represented by parallel resistance.
Figure 5.9: The layout of the bottom-biased VCO with the NC circuit.

\[ R_{cl, on} \text{ and } R_{cl, off}. \text{ The amount of canceled tank capacitance } (C_{NC}) \text{ can be derived as} \]

\[
\frac{C_{NC}(f)}{C_{gs}} = -\left(2h - \frac{1}{2\pi^2 f^2 L C_{gs}}\right) \left[1 - \left(1 + 2h - \frac{1}{2\pi^2 f^2 L C_{gs}}\right) \left(\frac{f}{f_T}\right)^2\right]
\]

\[
= \left(1 + \frac{2h - \frac{1}{2\pi^2 f^2 L C_{gs}}}{Q_{cl}}\right)^2 \left(1 + 2h - \frac{1}{2\pi^2 f^2 L C_{gs}}\right)\left(\frac{f}{f_T}\right)^2 + \frac{2h - 1/2\pi^2 L C_{gs}}{Q_{cl}}\left(1 + \frac{h - 1/4\pi^2 L C_{gs}}{Q_{cl}}\right)\left(\frac{f}{f_T}\right)
\]

\[
+ \frac{4C_{gd} - C_{cc}}{C_{gs}}\left(\frac{f}{f_T}\right)^2 (5.8)
\]

where \( h = C_{cl}/C_{gs} \). To better understand how the variable capacitor switching on and off affects \( C_{NC} \), \( C_{NC} \) is plotted as \( C_{cl} \) or \( Q_{cl} \) varying, as shown in Figure 5.11(a). Since the maximum cancelation of \(-2.7C_{gs}\) can be obtained when \( C_{cl} = 1.5C_{gs} \) for a 1 nH inductor, the highest tuning range can be achieved if \( C_{cl, off} = 1.5C_{gs} \).
Figure 5.10: The top-biased VCO with the cross-coupled NC circuit.
Figure 5.11: Simulated negative capacitance $C_{NC}$ (a) and parallel resistance (b) seen by the tank of the top-biased VCO vs. added cancelation capacitance $C_{cl}$ for different $Q_{cl}$ and $L$. 
Another design consideration in NC VCO is the negative resistance to ensure oscillation startup. To verify this condition, the input parallel resistance $R_{in}$ is extracted as

$$R_{in}(f) = -\frac{\left[\left(1 + \frac{2h - 1/2\pi^2 f^2 LC_{gs}}{Q_{cl}} \frac{f}{f_T}\right)^2 + \left(1 + 2h - \frac{1}{2\pi^2 f^2 LC_{gs}}\right)^2 \left(\frac{f}{f_T}\right)^2\right] R_{cl}}{2 \left[1 + \frac{2h - 1/2\pi^2 f^2 LC_{gs}}{Q_{cl}} \frac{f}{f_T}\right] + 4Q_{cl} \left(1 + h - \frac{1}{4\pi^2 f^2 LC_{gs}}\right) \left(\frac{f}{f_T}\right) - 2 \left(\frac{f}{f_T}\right)^2}. \quad (5.9)$$

To show if the cross-coupled pairs with different $Q_{cl}$ and $L$ satisfy the oscillation startup condition, the input resistance $R_{in}$ is plotted in Figure 5.11(b) using the same cancelation capacitors and inductors. Although $Q_{cl}$ and $L$ have minimal impact on $R_{in}$, when $C_{cl}$ is small ($\ll C_{gs}$), the circuit displays poor negative resistance. However, $R_{in}$ can be adjusted by altering $C_{cl}$. When $C_{cl}$ is $2C_{gs}$, the structure has a negative resistance of $-40 \Omega$, which satisfy the startup condition with $2\times$ margin. Therefore, without increasing the transistor size or $C_t$, the negative resistance can satisfy the oscillation startup condition with the desired margin.

To realize the tunable NC circuit, a MOS switch can be applied to substitute for the capacitor, as shown in Figure 5.12. When the switch is off, $C_{cl,off}$ equals $(WC_{ov} + C_{db})/2$. Since the resistance of the switch is high, $Q_{cl,off}$ is dominated by the inductor loss $R_{cl,L}$. When the switch is on, $C_{cl,on}$ is $WC_{ov}/2 + WLC_{ox}/4 + C_{db}/2$. The total loss is $R_{cl,m}/R_{cl,L}$, where $R_{cl,m}$ is the on-state switch loss (differential). In 130 nm process, with $C_{cl,off}$ set to be $2C_{gs}$, $C_{cl}$ with $Q_{cl,on}$ and $Q_{cl,off}$ is shown in Figure 5.13. When switching from off to on, the NC changes from $-2.5C_{gs}$ to $-0.1C_{gs}$ with $C_{NC}$ tuning range of 25. Substitute these values into (5.2), the VCO tuning range increases by 30%.
Figure 5.12: The implementation of the variable NC circuit and its small signal equivalent in the top-biased VCO.

Figure 5.13: $C_{NC}$ range of the top-biased VCO increases as the MOS switch turning on and off.
Figure 5.14: The layout of the top-biased VCO with the NC circuit.

Figure 5.14 shows the layout of the top-biased NC LC-VCO. Compared to the bottom-biased NC LC-VCO, two more inductors are required for top-biased NC LC-VCO, which slightly increases the die area.
Chapter 6: Design of Low Phase Noise mm-wave BiCMOS LC-VCOs

6.1 All-NMOS and All-BJT VCOs

As mentioned in chapter 3, a lot of work has been done to reduce the VCO phase noise. Earlier methods such as inductive coupling [22], filtering noise [31], reducing the device sizes [35] are proved to reduce VCO phase noise at a relatively low frequency. In mm-wave frequency range, the above methods show little improvement. For example, reducing the device sizes is an effective method in lowering phase noise in general. However, it also reduces $g_m$. Due to high losses in high frequency VCOs, the oscillation may not start.

In general, LC-VCO designs utilize only one type of transistors, either all-CMOS or all-BJT. For an NMOS LC-VCO (Figure 6.1(a)), a large bias current and high negative transconductance ($g_m$) are, respectively, needed to maintain a given oscillation amplitude and to satisfy the startup condition. Since $g_m$ has a weak dependency on current in strong inversion, it can primarily be increased by enlarging the device width, $W_1$, as illustrated in Figure 6.2(a). As noted in Chapter 3, further degradation in the device $g_m$ is experienced when the VCO operates near the transistor cutoff frequency, necessitating an even larger $W_1$ (Figure 6.2(a)). Since the single-ended fixed
capacitance $C_{fix1}$ is expressed as

$$C_{fix1} = C_{gs1} + 2C_{gd1} + C_{db1}$$  \hspace{1cm} (6.1)

where $C_{gs1}$, $C_{gd1}$ and $C_{db1}$ are proportional to $W_1$, a large fixed capacitance $C_{fix1}$ is expected and hence a limited VCO tuning range [19, 93]. It can also be shown that for the same bias current (i.e. output swing), increasing $W_1$ comes at the expense of large thermal ($1/f^2$) noise. This can be illustrated by examining the excess noise factor $F$, defined as the ratio between the transistors’ switching noise and the tank resistor noise [4]

$$F|_{@1\text{MHz offset}} = 10 \log \left( 1 + \frac{N_{itransistor}}{N_{Rp}} \right).$$  \hspace{1cm} (6.2)

As depicted in Figure 6.2(b), an extra 5dB of $1/f^2$ noise is added to the VCO output when the transistor $W_1$ is increased from 20 $\mu$m to 60 $\mu$m, which is required to meet a 2× startup margin. Moreover, increasing $W_1$ leads to a higher contribution of $1/f^3$ noise from up-converted $1/f$ noise [51].

Alternatively, SiGe LC-VCOs (Figure 6.1(a)) offer higher $g_m$ (Figure 6.2(a)) with significantly lower base/collector and base/emitter capacitances, $C_{\mu 1}$ and $C_{\pi 1}$, and thus, can achieve a wider tuning range [99] than its CMOS counterpart since

$$C_{fix2} = C_{\mu 1} + C_{\pi 1}$$  \hspace{1cm} (6.3)

where $C_{\mu 1}$ and $C_{\pi 1}$ are proportional to the emitter area $A_{E1}$. However, thermal noise is further degraded in SiGe VCOs as large current is still required to maintain the output swing given the low $Q$-factor of the tank. Since thermal noise increases with bias current in bipolar transistors (BJTs), more so than in CMOS, SiGe VCOs incur a higher $1/f^2$ noise (Figure 6.2(b)). This issue can be mitigated by using embedded frequency doubling (push-push) techniques to operate the VCO core at
lower frequencies for optimum resonator $Q$, and thus reducing the bias current [72]. However, this approach requires significantly higher core output swing compared to traditional LC-VCOs, at the cost of increased current and supply voltage.

### 6.2 BiCMOS VCOs

A VCO that combines NMOS and BJT cross-coupled pairs is proposed to overcome the fundamental trade-off between excess noise and high output swing in SiGe VCOs, and hence achieving wide tuning range and low phase noise simultaneously at minimal power consumption [105]. Figure 6.3 shows a conceptual diagram of the proposed BiCMOS VCO with current redistribution.
Figure 6.2: (a) Simulated transistor $g_m$ vs. frequency and (b) excess noise figure for All-NMOS, All-BJT and BiCMOS LC-VCOs.
The idea of paralleling two cross-coupled NMOS pairs was used in [24] to optimize the phase noise and startup performance of a Class-C NMOS VCO by adding a parallel NMOS pair biased near Class-B. In contrast, the proposed work, utilizes a Class-AB BJT pair using a fraction of the total current. This minimizes the $1/f^2$ noise contribution, while ensuring sufficient $g_m$ at mm-wave frequencies, without incurring the size (capacitance) and noise penalty of an NMOS device. The remaining portion of the bias current flows through an NMOS pair operating in Class-B to maintain the target output swing. Since the majority of the $g_m$ is supplied by the BJTs, the NMOS pair is sized with small $W_2$ to minimize its capacitance and noise contribution.

Figure 6.4 shows the schematic of the proposed BiCMOS LC-VCO. A 6-bit coarse-tuned varactor array is employed to lower the VCO gain ($K_V$) and thus minimizing
the AM-PM conversion. To reduce the mismatch between different coarse tuning bits, a thermometer varactor array is utilized for the 3 most significant bits, while a binary structure is used for the 3 least significant bits. The inductance redistribution technique is utilized in the layout of the varactor array to balance the parasitic inductance of the long traces connecting across the varactor cells. This is seen as critical in ensuring a uniform overlap between the 64 tuning curves at high frequencies.

The total VCO current is preset according to the LC tank \((Q = 8)\) to obtain the desired swing. Since the role of the BJT pair is to generate sufficient \(g_m\) to start the oscillation, it utilizes only 30% of the total 7 mA bias current \((I_{b, BJT} \sim 2 \text{ mA})\). At such low current, a minimum emitter area \((A_{E2})\) BJT can be used, further reducing the tank capacitance. The NMOS pair is sized to be small \((W_2 = 12 \mu \text{m})\) since it does not contribute to the overall \(g_m\), but it should be able to switch the remaining 70% of the bias current. The bias current of the BJT and NMOS pairs is controlled by two separate NMOS tail current sources. An NMOS bias transistor is used in lieu of a BJT to improve supply headroom and power efficiency. The \(1/f\) noise up-conversion from the NMOS bias transistor is simulated to be comparable to a BJT tail bias.

To illustrate the effectiveness of the proposed approach, three VCO architectures: all-BJT, all-NMOS and proposed BiCMOS, are designed to have the same oscillation frequency, VCO gain, tank \(Q\) and total bias current. Figure 6.5 shows the layout of the proposed BiCMOS VCO. The use of NMOS or BJT tail bias structure is further analyzed through simulation. All three VCOs are simulated and their phase noise results are compared in Figure 6.6, at both 1 MHz and 10 kHz offsets. The BiCMOS structure shows a marked improvement in both \(1/f^2\) and \(1/f^3\) noise regions across a wide range of bias current. In particular, at the optimum transition point from
Figure 6.4: The proposed BiCMOS LC-VCO schematic.
current-limited to voltage-limited region \((I_b \sim 7 \text{ mA})\), the BiCMOS design shows a reduction of \(>7\) dB in PN at both 1 MHz and 10 kHz offsets compared to all-NMOS or all-BJT VCOs. The impact of using an NMOS bias transistor on the \(1/f^3\) noise is seen as minimal \((<0.5 \text{ dB})\). This can be explained by noting that the majority of the bias current is switched through the small-\(W_2\) NMOS pair, which suppresses noise up-conversion [51].
Figure 6.6: Simulated phase noise of the three VCO structures using NMOS tail bias (solid lines) and BJT tail bias (dashed lines) at (a) 1 MHz offset and (b) 10 kHz offset.
Chapter 7: Experimental Results

The aforementioned VCOs, including three conventional VCOs, bottom-biased and top-biased NC VCOs, BiCMOS VCO and reference VCOs, are designed and fabricated in a 130 nm process to verify the results. On-chip 50 Ω CML amplifiers are utilized to buffer the VCO outputs. The chips are wire-boned on printed circuit boards providing RF connection to the test equipment.

7.1 Measurement Setup

The printed circuit boards (PCBs) are designed to provide all DC and RF connections. Figure 7.1 shows an example of the designed PCB schematic. The analog VDD and digital VDD are fed through two separate DC jacks. Two different size decoupling capacitors, 10 μF and 10 nF, are placed on each power rail. The 10 μF capacitor can reduce low frequency fluctuations in power rail and the 10 nF capacitor lower high frequency supply fluctuations. The bias current is generated by a potentiometer. Six one-pole double-throw switches are utilized to toggle the coarse tuning voltages between VDD and ground. The fine tuning control voltage terminal can be directly controlled by a header pin. A 1.85 mm RF connector, supporting the frequency up to 67 GHz, is used to connect the VCO high frequency output signal.
Two layer Rogers board is employed to design the PCB. To reduce the losses and minimize the 50 Ω trace width, the dielectric material thickness is selected to be 8 mils. The 50 Ω trace is also optimized to be short to lower the losses and with ground vias surrounded to shield the signal. Figure 7.2 shows the layout of the PCB.

An Agilent N9030A PXA spectrum analyzer with internal frequency range up to 50 GHz is used to measure the VCO output frequencies. Figure 7.3(a) shows the test setup for measuring the VCO tuning curves. To reduce the impact of switched power supply noise on the VCO phase noise, the power supply is replaced by a battery voltage supply and an Agilent E5052B with an E5053A down-convertor and 11970Q harmonic mixers are used. The VCO phase noise measurement setup is illustrated in Figure 7.3(b).
7.2 VCO Tuning Range Test Results

To verify the maximum tuning range vs. frequency (Figure 3.10) for conventional mm-wave VCOs, three LC-VCOs at different frequencies are implemented. Each VCO occupies an area of 1.25 × 1.25 mm², as shown in Figure 7.4. The VCO cores occupy areas of 150 × 200 μm². Figure 7.5(a) shows the tuning range of the three VCOs measured by an Agilent PSA N9030A spectrum analyzer. The 26 GHz VCO covers a tuning range of 25% from 22.7 GHz to 29.2 GHz. The tuning range of 34 GHz and 40 GHz VCOs is from 30.5 GHz to 37.6 GHz (21%) and from 36.4 GHz
Figure 7.3: (a) The tuning curve and (b) the phase noise measurement setup for LC-VCOs.
Figure 7.4: Micrograph of the (a) 26 GHz VCO, (b) 34 GHz VCO and (c) 40 GHz VCO.
Figure 7.5: (a) Measured tuning range of the three VCOs. (b) Calculated, Simulated and Measured CMOS LC-VCO tuning range at different mm-wave frequencies.
to 43.6 GHz (18%), respectively. Figure 7.5(b) shows the comparison among the results of model calculation, simulation, and measurement. The measurement and the simulation have consistent results as the calculation, especially at the frequency range below 40 GHz. As the frequency increases, the buffer size of the VCO increases, which is not accounted for in the analysis. Hence, there is a slight deviation between calculated and measured tuning range at higher frequencies. The phase noise is also captured by the PSA. The average phase noise of 26 GHz, 34 GHz and 40 GHz VCOs is $-103.7$ dBc/Hz, $-101.6$ dBc/Hz and $-98.8$ dBc/Hz at 1 MHz offset, and the VCO cores draw 11 mA, 13.5 mA and 15 mA of current from a 0.9 V power supply, respectively.

### 7.3 Bottom-biased NC LC-VCO Test Results

The bottom-biased LC-VCO with tunable NC and a baseline VCO without the NC circuit are designed and fabricated in a 130 nm CMOS process. Figure 7.6(a) shows the chip micrograph of the tunable NC LC-VCO. The chip area of each VCO including bond pads is $1.55 \times 1.25$ mm$^2$, while each VCO core occupies $150 \times 200$ μm$^2$. The tuning curves are measured using an Agilent N9030A signal analyzer and shown in Figure 7.7. Using the NC technique, the tuning range increases by 38% from 7.9 GHz to 10.9 GHz. Figure 7.6(b) shows the phase noise of the NC VCO. When the frequency tunes from 34.5 to 45.4 GHz, the phase noise ranges from $-98$ to $-95$ dBc/Hz. While for the reference VCO, the phase noise is from $-98$ to $-96$ dBc/Hz. Both VCO cores draw 13 mA of current each using a 0.9 V power supply.
Figure 7.6: (a) Micrograph of the NC VCO. (b) Measured phase noise of the NC VCO.
Figure 7.7: Tuning curves of (a) reference VCO and (b) tunable NC VCO.
### 7.4 Top-biased NC LC-VCO Test Results

Two inductance redistributed top-biased VCOs with/without NC are fabricated in a standard eight metal 130 nm CMOS process with each VCO occupying an area of $1.25 \times 1.25 \text{ mm}^2$, as shown in Figure 7.8. The VCO cores occupy areas of $200 \times 250 \mu\text{m}^2$ and $180 \times 250 \mu\text{m}^2$, respectively. Figure 7.9 shows the tuning curves of the two VCOs measured by an Agilent E4440A spectrum analyzer with an additional down conversion mixer to extend the measurement frequency range up to 40 GHz. As expected, the NC VCO covers a wide tuning range from 30.5 GHz to 39.6 GHz with uniform $f_{\text{step}}$. Compared to the reference VCO, the tuning range of the NC VCO increases by 34% from 6.8 GHz to 9.1 GHz. The phase noise is captured using an Agilent E5052B signal source analyzer and shown in Figure 7.10. The phase noise of the reference VCO ranges from $-102.8$ to $-100.4$ dBc/Hz across the frequencies. With the tunable NC circuit, the phase noise is from $-102.7$ to $-100.1$ dBc/Hz. The VCO core draws 9 mA of current from a 1.2 V power supply.

To summarize and compare the phase noise of the four VCOs, the phase noise at 1 MHz offset across the tuning range is shown in Figure 7.11. The utilization of tunable NC circuits does not incur additional phase noise degradation. However, as the frequency increases, the phase noise increases.

### 7.5 BiCMOS LC-VCO Test Results

The proposed BiCMOS VCO is realized in a 130 nm SiGe process. Figure 7.12(a) shows the die micrograph. The VCO core occupies $150 \times 200 \mu\text{m}^2$. Figure 7.13(a) shows the tuning curves of the BiCMOS VCO measured by an Agilent E4440A PSA. The VCO covers a tuning range of 9.8 GHz ranging from 28 GHz to 37.8 GHz with a
Figure 7.8: Micrograph of (a) the reference VCO and (b) the NC VCO.
Figure 7.9: Measured tuning curves of (a) the reference VCO and (b) the NC VCO.
Figure 7.10: Measured phase noise of (a) the reference VCO at 37.58 GHz, (b) the NC VCO at 39.56 GHz.
minimal overlap between tuning curves of 30%. The measured phase noise is provided in Figure 7.12(b). The average phase noise across the tuning range is $-103.6$ dBc/Hz and $-51.5$ dBc/Hz at 1 MHz and 10 kHz offsets, respectively, as shown in Figure 7.13(b). The VCO draws 7 mA from a 1.5 V supply, corresponding to an average FOM$_T$ of $-193.5$ dBc/Hz. A reference all-BJT VCO is fabricated and its measured phase noise is shown in Figure 7.13(b) for comparison.

### 7.6 Performance Summary of LC-VCOs

To evaluate the performance of the VCO designs, a figure-of-merit-including-tuning-range (FOM$_T$) [14] is adopted:

$$
FOM_T = L \{\Delta f\} - 20 \log \left( \frac{f_0}{\Delta f} \cdot \frac{\text{TR}}{10} \right) + 10 \log \left( \frac{P}{1\text{mW}} \right)
$$

(7.1)
Figure 7.12: (a) Micrograph and (b) Measured phase noise of the proposed BiCMOS VCO.
Figure 7.13: (a) Measured tuning range of the proposed BiCMOS VCOs. (b) Measured phase noise at 1 MHz and 10 kHz offsets across the tuning range for the BiCMOS VCO and the reference all-BJT VCO.
where $L\{\Delta f\}$ is the average phase noise, $\Delta f$ is an offset frequency from the carrier frequency $f_0$, TR is the tuning range of the VCO and $P$ is the power consumption. Table 7.1 summarizes the performance of the tunable NC CMOS VCOs, the reference CMOS VCOs, the BiCMOS VCO, the reference all-BJT VCO, and other state-of-art high frequency VCOs. The BiCMOS VCO achieves the highest tuning range and best reported $\text{FOM}_T$ among VCOs with similar center frequencies.
Table 7.1: Performance Summary of Wide Tuning Range mm-wave VCOs

<table>
<thead>
<tr>
<th>Reference</th>
<th>Process</th>
<th>Freq (GHz)</th>
<th>TR (%)</th>
<th>PN (dBc/Hz) @1MHz</th>
<th>Power (mW)</th>
<th>FOM_T</th>
</tr>
</thead>
<tbody>
<tr>
<td>[10]</td>
<td>130 nm CMOS</td>
<td>59</td>
<td>10</td>
<td>-89@1M</td>
<td>9.8</td>
<td>-174.5</td>
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<tr>
<td>[14]</td>
<td>180 nm CMOS</td>
<td>38</td>
<td>20</td>
<td>-100.2@1M</td>
<td>27</td>
<td>-183.5</td>
</tr>
<tr>
<td>[19]</td>
<td>65 nm CMOS</td>
<td>58</td>
<td>4.4</td>
<td>-95@1M</td>
<td>22</td>
<td>-169.7</td>
</tr>
<tr>
<td>[27]</td>
<td>130 nm SOI</td>
<td>40</td>
<td>15</td>
<td>-110@4M</td>
<td>11</td>
<td>-183.1</td>
</tr>
<tr>
<td>[42]</td>
<td>120 nm SOI</td>
<td>44</td>
<td>9.8</td>
<td>-101@1M</td>
<td>7.5</td>
<td>-184.9</td>
</tr>
<tr>
<td>[47]</td>
<td>130 nm CMOS</td>
<td>26</td>
<td>23</td>
<td>-93@1M</td>
<td>43</td>
<td>-172.2</td>
</tr>
<tr>
<td>[72]</td>
<td>SiGe</td>
<td>52.5</td>
<td>26</td>
<td>-108@1M</td>
<td>132</td>
<td>-189.6</td>
</tr>
<tr>
<td>[93]*</td>
<td>90 nm CMOS</td>
<td>15</td>
<td>69</td>
<td>-90@1M</td>
<td>6</td>
<td>-182.5</td>
</tr>
<tr>
<td>[99]</td>
<td>SiGe</td>
<td>36</td>
<td>7</td>
<td>-105@2M</td>
<td>84</td>
<td>-167.8</td>
</tr>
<tr>
<td>BB Ref VCO</td>
<td>130 nm CMOS</td>
<td>38</td>
<td>20</td>
<td>-97.3@1M</td>
<td>12</td>
<td>-184.1</td>
</tr>
<tr>
<td>BB NC VCO</td>
<td>130 nm CMOS</td>
<td>40</td>
<td>27</td>
<td>-96.9@1M</td>
<td>12</td>
<td>-186.8</td>
</tr>
<tr>
<td>TB Ref VCO</td>
<td>130 nm CMOS</td>
<td>34.2</td>
<td>20</td>
<td>-102.3@1M</td>
<td>11</td>
<td>-188.6</td>
</tr>
<tr>
<td>TB NC VCO</td>
<td>130 nm CMOS</td>
<td>35</td>
<td>26</td>
<td>-101.9@1M</td>
<td>11</td>
<td>-190.7</td>
</tr>
<tr>
<td>All-BJT VCO</td>
<td>SiGe</td>
<td>30.2</td>
<td>25**</td>
<td>-98.2@1M</td>
<td>10</td>
<td>-185.8</td>
</tr>
<tr>
<td>BiCMOS VCO</td>
<td>SiGe</td>
<td>32.9</td>
<td>30</td>
<td>-103.6@1M</td>
<td>10</td>
<td>-193.5</td>
</tr>
</tbody>
</table>

* Bridge circuit is used to tune the tank inductance.

** Tuning range is reduced, as large current flows through the BJT pair in the all-BJT VCO, dictating a 4× increase in emitter area compared to the BiCMOS VCO ($A_{E1} = 4A_{E2}$).
Chapter 8: Conclusion

The continuing trends in the RF circuit industry suggest that communications equipments are required to support wider bandwidth while limit the transmission in specific channels. This poses interesting challenges in LC-VCO design: wide tuning range and low phase noise. This dissertation has identified and analyzed the tuning range limitation of mm-wave LC-VCOs. The relatively large fixed capacitance in high frequency VCO is the fundamental problem in LC-VCO designs. The problem is studied and an analytical expression of the tuning range is derived for the conventional LC-VCOs at different mm-wave frequencies. Three VCOs in mm-wave range have been designed and implemented in a 130 nm process to verify the tuning range limitation.

Variable NC circuits have been proposed to cancel the large fixed capacitance in the LC-tank and hence extend the tuning range. The variable NC circuits are optimized to fit both bottom-biased and top-biased LC-VCO structures with minimal impact on power consumption and phase noise. Both VCOs are designed and implemented in a 130 nm process. The VCOs achieves best tuning range and FOM_T among VCOs in CMOS technologies with similar center frequencies.

The phase noise limitation is also analyzed. Since it is mainly limited by the large CMOS transistor $g_m$ or high BJT transistor current. In BiCMOS VCO design,
a VCO combining both NMOS and BJT cross-coupled pairs is proposed to simultane-ously reduce $g_m$ of CMOS transistors and current of BJT transistors. Using this approach, not only the phase noise is reduced, the tuning range is also extended. By implementing the VCO in a 130 nm SiGe process, the performance is demonstrated to be the best reported.

All VCOs utilized 6-bit coarse-tuned varactor arrays to lower the VCO gain ($K_V$) and thus minimizing the AM-PM conversion. Thermometer varactor arrays are utilized for the 3 most significant bits, while binary structures are used for the 3 least significant bits to reduce the mismatch between different coarse tuning bits. Inductance redistribution techniques are proposed and applied to the layout of the varactor array to balance the parasitic inductance of the long traces connecting across the varactor cells, which is seen as critical in ensuring a uniform overlap between the all tuning curves at mm-wave frequencies.

Using the above techniques, the best mm-wave LC-VCO achieves a tuning range of 30% at 40 GHz, with an average FOM$_T$ of $-193.5$ dBc/Hz.

**Future work**

Since the scaling of CMOS provides high $f_{max}$ and $f_T$, one possible application is towards license-free 60 GHz radios, which has an unprecedented 7 GHz of unchannel-ized spectrum for wireless operation between 57–64 GHz. Applying techniques such as NC and inductance redistribution to a 60 GHz VCO, a wide tuning range can be achieved to satisfy the wide spectrum specifications while leaving a necessary margin for PVT variations.
Another fruitful extension to this work is to apply the NC circuits to other applications including high speed I/Os, ultra fast supply regulators, optical communication circuits and antennas with non-Foster impedance matching. The unwanted parasitic capacitance can be significantly reduced to improve the speed and the performance of the systems.
Bibliography


