Charge transport properties in semiconductor nanowires

DISSERTATION

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Abstract

Semiconductor nanowires have shown promising results for next generation integrated electronics such as field effect transistors (FET), tunable optoelectronics and quantum information technology, etc. By reducing device size, the effects of defect states can be readily occurred: such as space charge limited current and hopping transport. Also, the interface property is a significant factor in nanoelectronic device design. In order to solve these problems, a comprehensive investigation of electrical and optical properties becomes extremely important.

Here, charge transport mechanisms are investigated in Se-doped InP nanowires grown via pulsed laser deposition (PLD). Current-voltage (I-V) curves reveal that transport is limited by trapped space charge at high bias rather than Schottky diode behavior in most temperature regimes while at low bias electron mobility calculations indicate that hopping between defect states plays a dominant role. This model is further supported by careful temperature-dependent studies of the zero-bias resistance that reveal a crossover between hopping mechanisms at a temperature of ~ 158 K. Nearest neighbor hopping (NNH) dominates in the high temperature regime (T > 158 K) where resistance is found to depend on $exp(T_0/T)^{1.03}$ and Efros-Shklovskii variable range hopping (ES-VRH) dominates in the low temperature regime (T < 158 K) where resistance is found to depend on $exp(T_{ES}/T)^{0.49}$. The average separation between carriers is comparable to the
thermal deBroglie wavelength at all temperatures. As a result, this system is in the quantum regime while both NNH and ES-VRH treat electron-electron interactions classically. When applying a positive gate voltage, the crossover temperature is found to decrease from 158 K to 130 K and the exponent for low temperature regime deviates from the theoretically predicted value, $\frac{1}{2}$. These results highlight the increased importance of defect states in quasi-1D systems and the gate dependence of the crossover temperature, as well as of the related hopping parameters, suggests that applying a gate voltage can tune the strength of electron correlations in these systems.

To explore 1D structures further, superlattice nanowire pattern transfer (SNAP) has been developed where the device design is applicable for the non-local spin transport measurement. In order to obtain injection of spin information from a ferromagnetic to a semiconductor, understanding of interface characteristics is crucial. Here we developed a procedure to improve interface characteristic, thereby enhancing spin injection efficiency. Anisotropic magneto-resistance (AMR) measurements are conducted to determine the coercive fields of ferromagnetic electrodes. Doping concentration, oxide barrier thickness and other parameters can be adjusted further to obtain successful non-local spin transport.
Dedication

This document is dedicated to my family.
Acknowledgments

When I started PhD course in physics department at the Ohio State University, I was glad about the variety of research area and enthusiasm of faculty members. Then one interesting material came out to me which was semiconductor nanowire with excellent collaboration between our group and Prof. Yang’s group. I loved the whole spectrum to be able to conduct this research, nanowire growth, device fabrication and the measurement and characterization of nanowire. As a result, it makes me to achieve the scientific knowledge in nanostructure.

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1. “Comprehensive control of optical polarization anisotropy in semiconducting nanowires”

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Chapter 1: Introduction – Charge transport in semiconductors

1.1 Motivation

Nanowire and nanotube systems have been an attractive field for several decades as a candidate for the next-generation highly integrated circuits such as field effect transistors (FET) and single electron transistors structured on the scale of 10 nm [1][2]. Electrical and electroluminescence (EL) experiments with InP NWs were carried out by X. Duan et al. [3]. They demonstrated both rectifying and strong light emitting behaviors in a crossed wire p-n junction fabricated with a nanowire FET structure. High mobility and good FET behavior (optimal characteristics in nanowire systems) were observed in InAs/InP heterostructure in a single nanowire, as shown in Fig. 1.1 [4]. X. Jiang et al. in Ref. [4] demonstrated the design of a high mobility heterostructure nanowire device and created opportunities for nanoscale building blocks such as high-speed and low-power nanoelectronic circuits. Figure 1.1 shows the FET behavior of a device where high carrier mobility is enhanced in the core/shell heterostructure of a single nanowire. The increased mobility as temperature decreases denotes that the conduction band transport mechanism is dominant.
These high mobility and FET behaviors have been discussed in high quality of NWs; however, there has not been a deep investigation into charge transport in disordered NWs. In typical nanowire growth, there is high probability of the formation of defect states in nanowires, such as dislocations, interstitials and vacancies. The typical nanowire diameter is 10 ~ 100 nm and length is ~ 10 μm. And the control of growth conditions, especially impurity level, is difficult during nanowire growth because of catalyst based growth. Because most of NWs systems can be readily created with defects and disorders, it is important to explore their functionality in electronic systems. In this thesis, I focus mainly on the charge transport mechanisms of disordered InP NW systems where I try to answer the questions: What is the functionality of defect states in charge transport in NW systems? How can transport mechanisms be controlled?

Beyond charge transport properties, spin transport in a 1D system is an emerging field for next-generation spin based electronic device [5]. For the promising 1D system in spin transport measurement, I discuss new technique which has been developed within
the past decade [6][7]. This technique is a top-down NW growth method through the use of a nanowire pattern transfer instead of growing nanowires (bottom-up growth). This technique creates a high quality NWs array because of patterning from high quality bulk system, and provides easy control of doping level. Therefore it is one of the most promising systems for spin transport measurement in 1D systems.

We applied a nanowire patterning process for the fabrication of Si nanowire devices where we can conduct non-local spin transport measurements. The interface properties between a ferromagnetic (FM) material and a semiconductor (SC) are extremely important in order to achieve successful spin-injection, thus we have also developed procedures to improve the interface conditions in this study.
1.2 Metal-Semiconductor junction: Schottky diode

The typical junction between a metal and semiconductor is a Schottky junction which is a result of band bending from the alignment of the Fermi levels. Figure 1.2 shows the formation of Schottky barrier at the interface between metal and $n$-type semiconductor. By aligning the Fermi-levels, the band bending occurs at the interface and forms a barrier against electron transport. When charges move across a Schottky barrier, there are two current behaviors: thermionic emission over the barrier and quantum mechanical tunneling through the barrier [8][9].

![Diagram of Schottky barrier formation](image)

Fig. 1.2 Formation of Schottky barrier at metal-semiconductor interface. Band bending occurs from aligning the Fermi levels in metal and $n$-type semiconductor.

The thermionic emission theory assumes that electrons, which have the energy larger than barrier height, will cross the barrier. The current density from thermionic emission can be expressed as [8]:

$$J \propto J_0 \exp\left(-\frac{q\phi_b}{kT}\right) \exp\left(\frac{qV}{nkT}\right) - 1$$

(1.1)
where $\phi_b$ is Schottky barrier height and $n$ is the ideality factor. The minus term ensures that the current is zero if no voltage is applied as in thermal equilibrium where any motion of carriers is balanced by a motion of carriers in the opposite direction.

The tunneling current through Schottky barrier is obtained from the product of the carrier charge, velocity and density. The velocity is the Richardson velocity, which is the average velocity with which the carriers approach the barrier. The carrier density equals the density of available electrons, $n$, multiplied with the tunneling probability, $\Theta$, yielding [8]:

$$J_n = qv_R n\Theta$$

The tunneling probability enters as a product because the total current depends on the product of carrier flux arriving at the tunnel barrier and the probability that carriers tunnel through the barrier. The tunneling probability is obtained from:

$$\Theta = \exp \left( -\frac{4}{3} \frac{\sqrt{2qm^*}}{h} \frac{\phi_b^{3/2}}{F} \right)$$

where $F$ is electric-field and $m^*$ is an effective mass. The tunneling current therefore depends exponentially on the barrier height, $\phi_b$, to the 3/2 power. Schottky barrier height ($\phi_b$) is defined as $\phi_b = \phi_M - \chi_s$ – it is valid as long as there is no interface states at Schottky junction – where $\phi_M$ is the work function of metal and $\chi_s$ is semiconductor’s electron affinity.

In low doping cases, thermionic emission dominates in Schottky junction so the current is an exponential function of applied bias ($V$), which is verified by the linear behavior in semi-log plot of the I-V curve. Figure 1.3(a) shows the schematic band
diagram with Schottky barrier, while Fig. 1.3(b) is the semi-log plot of representative I-V by charge transport over Schottky barrier. Here $n$ is the ideality factor calculated from Eq. (1.1) which is 1.93 in this plot.

Fig. 1.3 (a) Band diagram in Schottky junction, $\phi_b = \phi_M - \chi_s$, where $\phi_M$ is the work function of metal and $\chi_s$ is semiconductor’s electron affinity. (b) Typical schottky diode behavior (In thermionic emission) in semiconductor (GaP) and Au contact (Courtesy of Chris Ratcliff in Steven Ringel’s group at The Ohio State University). The ideality factor ($n$) for usual Schottky diode current is less than 2.
1.3 Space charge limited current (SCLC)

Space charge is a term which is typically applicable when charge carriers have been emitted from some region of a solid. This cloud of emitted carriers can form a space charge region if a number of carriers are spread out (enough to redistribute carriers by the induced electric-field). This space charge usually only occurs in dielectric media (including vacuum) because in a conductive medium the charge tends to be rapidly neutralized or screened. This situation is common in the area near a metal object when it is heated to incandescence in a vacuum, such as the light bulb filaments observed by Thomas Edison. Space charge is a significant phenomenon in many vacuum and solid-state electronic devices. Here two types of space charge limited current (SCLC) are introduced: trap free SCLC behavior and trapped-SCLC behavior.

1.3.1 SCLC without traps

The SCLC behavior without traps can be derived as follows [10]. One requirement for SCLC is that one of the two contacts must be Ohmic because charge injection shouldn’t be limited on that contact. In this case the contact provides an excess amount of carriers to the channel.

The capacitance of a parallel plate capacitor is \( C = \varepsilon A/d \), where \( \varepsilon \) is the permittivity of channel material, \( A \) is the cross sectional area and \( d \) is the length of channel. The charge on the parallel plate capacitor is given as,

\[
Q = CV = \varepsilon AV / d
\]
Then, the SCLC is dominated by the drift of the injected carriers so the current density is given by \( J = qnv \), where \( n \) is carrier density and \( v \) is the velocity. The injected carriers thus control the space charge and the electric-field profile. This results in a feedback mechanism where the field drives the current, which in turn sets up the field. Now, \( J = qnv \) can be written as \( I = Q/T \), where \( T \) is the time for the charge move the length of the channel. \( T \) can be found from

\[
v = \mu F
\]

where \( \mu \) is mobility and \( F \) is electric field.

Because \( F = V/d \), where \( V \) is applied bias, \( T \) can then be derived as

\[
T = \frac{d}{v} = \frac{d}{\mu F} = \frac{d^2}{\mu V}
\]

The SCLC is then,

\[
I = \frac{Q}{T} = \frac{\varepsilon A \mu V^2}{d^3}
\]

This is called Mott-Gurney law. Finally, the current density has power law of \( V \), \( J \propto V^2 \), for trap free SCLC.

1.3.2 SCLC with traps (trapped-SCLC)

In bulk insulating or semiconducting materials, SCLC is a well-known model used to describe nonlinear and non-exponential IV characteristics [11][12]. This phenomenon usually happens in the case of low intrinsic doping and charge traps, therefore current is controlled by space charge (trapped charge) effect with low effective
carrier concentration. In nanowire systems, charge transport can be highly affected by trapped-SCLC because the carrier depletion is more frequently caused by the surface states due to high surface-to-volume ratio. The trap states, mainly on the surface of the nanowire, can easily be incorporated during growth. A. Rose demonstrated that the SCLC is an exponential function of the bias when traps are assumed to have a uniform distribution, and is a power-law when the distribution is exponential [13]. Many sources have shown the power-law dependence of the SCLC and hence the exponential distribution of trap states.

Mark and Helfrich discuss trapped-SCLC model [14]. They assumed that the free carrier concentration is much less than the trapped carrier concentration and that the traps are distributed in energy as,

$$h(E) = \frac{H_t}{E_t} \exp\left(\frac{-E}{E_t}\right)$$  \hspace{1cm} (1.2)

where $E$ is the relative energy measured from bottom of conduction band. This exponential distribution of traps is characterized by two parameters: trap concentration, $H_t$, and the characteristic constant of the distribution, $E_t$. Figure 1.4 shows the trap states distribution below the conduction band. Injected electrons are trapped in defect states, and the amount of trapped electrons depends on temperature ($T$) and applied bias ($V$).
Mark and Helfrich found the space charge, \( \rho(x) \), which fills all the traps to Fermi level and also derived the density of the free carrier \( \rho_f(x) \). By comparing \( \rho_f(x) \) to \( \rho(x) \), one can obtain the relation between the free and the total charge density

\[
\rho_f(x) = N_0 e^0_{l=0} H_{l=0} \left[ \rho(x) \right]^{l=0}
\]

where \( l = T_i / T \), \( N_0 \) is the effective density of states in the conduction band and \( H_i \) is the trap concentration. The current density limited by space charges is given by

\[
J = \mu \rho_f(x) F(x)
\]

where \( \mu \) is mobility and \( F(x) \) is electric field. The detailed algebraic calculation with Eq. (1.4) is described in Ref. [14]. As a result, the current density becomes

\[
J = N_0 q^{l+1} \mu \left( \frac{q e}{H_i (l+1)} \right)^l \left( \frac{2l+1}{l+1} \right)^{l+1} \frac{V^{l+1}}{d^{2l+1}}
\]

where \( d \) is the length of channel and \( l = T_i / T \) as in Eq. (1.3). \( J \) is a power law of applied bias \( (V) \). Therefore \( l+1 \) becomes the slope in log-log plot of \( J-V \) curves. \( T_i \) is the characteristic trap temperature which gives \( E_i = k T_i \), and determines the width of exponential trap state distribution as shown in Fig. 1.4.
Kumar et al. created log-log plots of current density vs. voltage ($J$-$V$) from Eq. (1.5) at different temperatures [15], as shown in Fig. 1.5. At high temperature trapped charges are promoted back into the conduction band so the conduction band transport is exacerbated by suppressing space charge effect. This makes $I$-$V$ curve becoming more Ohmic (Slope approaches one). Thus the slope of the plot increases as the temperature decreases. There is a crossover voltage ($V_C$) at certain point where the current is temperature independent. This point can be used to calculate the total trap concentration (defect states) which distributes exponentially below conduction band.

![Log-log plots of current density vs. voltage](image)

**Fig. 1.5** Calculated log-log plots of current density vs. voltage ($J$-$V$) for different temperatures, (1) 100 K, (2) 150 K, (3) 200 K, and (4) 300 K. Calculation is conducted with Eq. (1.2). Note that all the lines meet at crossover voltage $V_C = 30$ V [15].

1.3.3 Calculation of trap concentration in SCLC model

In Fig. 1.5, a crossover point is observed from the log-log plots of $J$-$V$. An analytical method to determine the trap concentration, $H_n$, was introduced by Kumar et al. [15][16] by rearranging Eq. (1.5) as follows:
the exponential function can be applied to a natural logarithm without altering the result, and \( J \) can be written as

\[
J = \frac{\mu qNV}{d} \exp\left\{-\frac{E_i}{k_B T} \ln\left[\frac{(2l + 1)^{-1/4}}{l + 1} \frac{(l + 1)^2}{l(2l + 1)} \frac{qH_i d^2}{\varepsilon V} \right]\right\}
\]

where \( \left[ \frac{(2l + 1)^{-1/4}}{l + 1} \frac{(l + 1)^2}{l(2l + 1)} \right] \) is equal to \( \frac{1}{2} \) within 4% error in temperature variation.

As a result, current density becomes

\[
J = \frac{\mu qNV}{d} \exp\left\{-\frac{E_i}{k_B T} \ln\left(\frac{qH_i d^2}{2\varepsilon V} \right)\right\}
\] (1.6)

This suggests that current density \( (J) \) becomes \( \mu qNV/d \) at crossover point. So, the term inside of the exponential in Eq. (1.6) should be zero, driving the natural-log term to zero. Therefore, this implies we should have

\[
\frac{qH_i d^2}{2\varepsilon V} = 1 \quad \text{at} \quad V = V_c.
\]

Finally, this can be rearranged into a simple equation for the trap state concentration,

\[
H_t = \frac{2\varepsilon V_c}{q d^2}
\] (1.7)

\( H_t \) (trap states concentration) can be determined with permittivity \( \varepsilon \), elementary charge \( q \), channel length \( d \) and \( V_c \).

The trapped-SCLC model is an important theory to explain I-V characteristics in disordered semiconductor systems, both in 1D [17][18] and 2D [19] systems. Schricker et
al. in Fig. 1.6(a) and Qiao et al. in Fig. 1.6(b) show log-log plots of I-V curves which were measured in GaAs nanowires [17] and SnCl$_2$Pc thin films [19]. Both data sets show similar behaviours as predicted theoretically in Fig. 1.5: linear slopes in log-log plot where the slope increases as temperature decreases [20],[21]. For exploring detailed exploration of the trap state distribution, Ref. [6] shows that surface trap states in CdS nanowires play a significant role in the electron conduction through the nanowire. This property is investigated by the oxygen adsorption on surface states of nanowire.

![Log-log plots of IV curves](image)

Fig. 1.6 Log-log plots of IV curves show trapped-SCLC behaviours. (a) Data was taken in GaAs NW system [17]. (b) Data in amorphous tin-phthalocyanine-dichloride (SnCl$_2$Pc) thin films [19].
1.4 Hopping transport

1.4.1 Nearest-neighbor hopping (NNH)

In highly disordered systems, hopping transport can be the dominant transport mechanism. Here, carriers are transported by phonon assisted tunneling processes between localized states. There are two types of hopping conduction: nearest-neighbor-hopping (NNH) and variable-range-hopping (VRH). In nearest-neighbor hopping (NNH) conduction, electrons with activation energy hop to the nearest neighboring empty site. In this regime, the temperature dependence of conductivity can be derived as follows.

Consider two localized states with an energy separation $W$ and the NN distance $r$, an electron can hop from one site to the other site by the absorption of a phonon with energy $W$ as shown in Fig. 1.7(a). The tunneling probability is proportional to $e^{-r/\xi}$ as illustrated with blue-curve in Fig. 1.7(b).

![Diagram of hopping transport](image)

Fig. 1.7 Diagram of hopping transport, (a) Nearest-neighbor hopping (NNH) from one site to the other site, (b) Hopping probability depending on tunneling decay.
From Ref. [22], the hopping probability can be expressed as

\[ P_{\text{hop}} = \nu_{ph} \exp \left( - \frac{2r}{\xi} - \frac{W}{k_B T} \right) \]  

(1.8)

where \( \nu_{ph} \) is the phonon frequency associated with hopping process, \( k_B \) is Boltzmann’s constant, and \( \xi \) is localization length (\( 1/\xi \) is the decay rate of the wave-function as shown in Fig. 1.7(b)).

The electrical conductivity is calculated by using the diffusion coefficient \( D_{\text{hop}} \) and the Einstein relation between the mobility \( \mu \) and \( D_{\text{hop}} \):

\[ D_{\text{hop}} = \frac{P_{\text{hop}} r^2}{6}, \quad \mu = \frac{eD_{\text{hop}}}{k_B T} \]  

(1.9)

The density of electrons participating in the conduction is \( n \approx g(E)k_B T \), where \( g(E) \) is the density of states (DOS). Using Eqs. (1.8) and (1.9), \( \sigma \) is obtained as follows:

\[ \sigma = ne\mu = e^2 D_{\text{hop}} g(E) \]  

(1.10)

Substituting for \( D_{\text{hop}} \) we find the temperature dependence of the conductivity is

\[ \sigma = \frac{1}{6} g(E) \nu_{ph} e^2 r^2 \exp \left( - \frac{2r}{\xi} - \frac{W}{k_B T} \right) \]  

(1.11)

where \( r \) is constant in the NNH regime. Eq. (1.11) can be simplified to:

\[ \sigma = \sigma_3 \exp \left( - \frac{W}{k_B T} \right) \]  

(1.12)

Here, the only temperature dependent term is \( \exp(-W/k_BT) \) in the NNH regime (high temperature). At low temperature, the electrons can prefer to move to a more energetically similar remote site so the term \( \exp(-2r/\xi) \) is not temperature independent.
any more. As a result, a different hopping mechanism is observed when both terms depend on the temperature.

1.4.2 Variable-range hopping (VRH)

Usually in amorphous semiconductors, hopping conduction occurs through unoccupied localized states near the Fermi level as low temperature behavior of the resistivity. The existence of this type of hopping conduction was first pointed out by Mott [23], who called it the variable-range-hopping (VRH). Fig. 1.8 shows why VRH behavior is more favorable than NNH at low temperature. At high temperature ($k_B T$ greater than the average variation in trap energy) phonon-assisted hopping allows access to NN hopping sites, Fig 1.7(a). At low temperature the range of energetically accessible hopping sites decreases and the electron may hop to long range hopping sites.

![Fig. 1.8](image_url)

Fig. 1.8. Schematic illustration of variable-range-hopping (VRH) behavior at low temperature regime.

In the following, there is briefly derived calculation for the VRH in terms of a simple physical consideration given by Mott [24][25]. The difference between VRH and NNH is that the hopping distance $r$ and the hopping energy $W$ are related to each other in VRH, and conductivity in VRH is determined by optimizing the competition between $e^{-2r/\xi}$ and $e^{-W/k_B T}$.
The energy difference \( W \) in Eq. (1.8) is estimated in the following way. One can consider that an electron jumps from one site to another a distance \( r \) apart. In 3D systems, the number of states situated between \( E \) and \( E + \Delta E \) within a sphere of radius \( r \) is given by

\[
\frac{4\pi}{3} r^3 g(E) \Delta E
\]

These states lie in the width of \( \Delta E \), so that the energy difference \( W \) is given by

\[
W = \frac{\Delta E}{\frac{4\pi}{3} r^3 g(E) \Delta E} = \frac{3}{4\pi r^3 g(E)} \tag{1.13}
\]

Applying Eq. (1.13) to Eq. (1.8), the most probable distance \( r \) is obtained from \( \frac{\partial P_{\text{hop}}}{\partial r} = 0 \) as follows:

\[
r = \left\{ \frac{3}{(2/\xi) (4\pi/3) g(E_F) k_B} \right\}^{1/4} T^{-1/4} \tag{1.14}
\]

Substituting Eq. (1.14) into Eq. (1.13), one can obtain

\[
P_{\text{hop}} = \nu_{ph} \exp \left( -B / T^{1/4} \right) , \quad B = 2.06 \left\{ \frac{\alpha^3}{k_B g(E_F)} \right\}^{1/4}
\]

From Eq. (1.10), conductivity is given by

\[
\sigma = \sigma_0 \exp \left( -B / T^{1/4} \right) \equiv \sigma_0 \exp \left\{ -\left( T_M / T \right)^{1/4} \right\} \tag{1.15}
\]

\[
T_M = \frac{18.1 \alpha^3}{k_B g(E_F)}
\]

The temperature dependence of VRH comes from a factor of \( \exp \left\{ -\left( T_M / T \right)^{1/4} \right\} \) in Eq. (1.15). This hopping mechanism is called Mott-VRH.

There was suggestion by Efros and Shklovskii that the long-range nature of the Coulomb interaction should lead to a dip in the DOS at the Fermi energy [25]. By
considering the net energy change in transition of the electron from filled site to empty site, the net energy in transition should be larger than zero which creates the limited DOS (dip in the DOS) at the Fermi level. DOS vanishes at $E_F$ for $T = 0$, and has the following parabolic form in the immediate vicinity of $E_F$:

$$g(E) = \alpha_{3D} E^2, \quad \alpha_{3D} = \left(\frac{3}{\pi}\right)\left(\kappa^3/e^6\right)$$

(1.16)

where $\kappa$ is the dielectric constant and $e$ is the elementary charge. Using Eq. (1.16) and by analogy with the Mott-VRH derivation, Efros and Shklovskii (ES) showed the temperature dependence of the VRH conductivity as [24]:

$$\sigma = \sigma_0 \exp\left(-\frac{T_{ES}}{T}\right)^{1/2}$$

(1.17)

As expressed in Eq. (1.12), (1.15) and (1.17), the typical hopping transport equation can be expressed as:

$$\sigma = \sigma_0 \exp\left(-\frac{T_0}{T}\right)^m$$

(1.18)

where $\sigma_0$ is the pre-exponential factor and $T_0$ is a characteristic temperature. $m = 1$ is explained by NNH whereas $1 > m > 0$ is a result of VRH. Therefore investigating the exponent $m$ from conductivity vs. temperature measurement can reveal the hopping transport mechanism.

The most acceptable method to verify ES-VRH, rather than Mott-VRH, is the $dI/dV$ vs. $V$ plots where one can observe the dip in the DOS. Many experiments have been conducted to explore Mott-VRH and ES-VRH properties in various systems. Recently, several experiments on NNH transport properties in 1D systems were
performed by Ma et al. who demonstrated hopping transport in ZnO nanowires with an exponent of $\frac{1}{2}$, corresponding to ES-VRH [26]. Ma et al. show the log-log plot of resistivity $\rho$ vs. $T^{1/2}$ showing linear behavior in Fig. 1.9(a). And $dI/dV$ vs. $V$ plot in Fig. 1.9(b) shows a dip in the DOS ($g(E)$) which represents the Coulomb gap near the Fermi level. This Coulomb gap is caused by Coulomb interaction between localized electrons.

Fig. 1.9. (a) Log-log plot of $ln(\rho)$ vs. $T^{1/2}$, (b) $dI/dV$ vs. $V$ plot revealing the Coulomb gap which denotes ES-VRH mechanism in ZnO nanowire [26].
1.5 Reference


Chapter 2: Nanowire growth and device fabrication

2.1 III-V nanowire growth

2.1.1 Nanowire growth via vapor-liquid-solid (VLS) synthesis

Vapor-liquid-solid (VLS) growth is a common mechanism to grow semiconductor nanowires. This mechanism is broadly applicable to many growth tools. Pulsed laser deposition (PLD) [1][2], molecular beam epitaxy (MBE) [3] or metal-organic chemical vapor deposition (MOCVD) [4] are three tools used to create vapor-phase semiconductor reactants via momentum and energy transfer to targets. Targets are prepared from mixed powders or precursor decompositions by a chemical vapor deposition (CVD) process. In this study, we used a PLD system for the VLS growth of InP nanowires.

In the VLS growth of semiconductor nanowires, a gold catalyst is widely used as growth seed [5]. Fig. 2.1(a) shows VLS growth mechanism for GaAs nanowires via gold catalysts. The growth procedure is as follows: i) Vapor-phase of nanowire materials are prepared by evaporation-pulsed laser deposition (PLD) in our system. ii) Absorption of the vapor-phase materials into liquid droplet creates a liquid phase of metal-semiconductor alloy. iii) The growth temperature needs to be between the eutectic temperature and melting point of source material. The specific composition and growth
temperature will be decided by the phase diagram, as seen in Fig. 2.1(b). iv) Once the liquid phase of semiconductor-metal alloy is supersaturated, the nucleation triggers the crystallization to form a solid-phase semiconductor. v) By supplying continuous vapor-phase material into the liquid droplet, it maintains the supersaturated condition and continues one dimensional growth of nanowires at the interface between liquid-phase alloy and solid-phase semiconductor.

![Fig. 2.1. (a) Schematics of GaAs nanowire growth with Au catalyst. (b) Au/GaAs phase diagram [5].](image)

The diameter of a typical VLS grown nanowire is a few tens of nanometers and is determined by the size of Au catalyst. The length of nanowires ranges up to several tens of micrometers and depends on growth time.

Semiconductor nanowires can be grown on many different materials because the nanoscale diameter of the nanowires can introduce lateral strain relaxation in the crystal structure of nanowire [6]. Therefore, dislocations are not produced and heterojunctions between materials of different lattice constants is possible. Some examples are GaAs, GaP, and InP nanowires on Si [7][8] or InP nanowires on Ge [9]. One particularly interesting aspect of semiconductor nanowire growth is the possibility of a
heterostructure which would provide an opportunity for adapting nanowire systems for nanoelectronics and optoelectronics applications. Many groups have demonstrated axially and radially heterostructured nanowires [10] in GaAs-InAs [11], InP-InAs [12] and GaAs-GaP [13] materials. Verheijen et al. show TEM images of axially heterostructured GaP-GaAs nanowire synthesized in metal-organic-vapor phase-epitaxy (MOVPE), as shown in Fig. 2.2 [14]. These heterostructured nanowires are grown using careful temperature and pressure control. The contrast lines within GaP segments, orthogonal to the axial direction of a nanowire, correspond to the twin domains with stacking faults, as shown in Fig. 2.2(b). However, GaAs segments do not show these stacking faults in Fig. 2.2(c). These stacking faults in GaP segments reflect the unstable growth conditions (temperature and pressure). The stacking faults are also observed in our nanowires, as shown in Fig. 2.8.

Fig. 2.2 (a) TEM image of a heterostructured GaP-GaAs nanowire. (b) High resolution TEM (HRTEM) image of GaP showing stacking faults. (c) HRTEM image of GaAs, No stacking faults. (d) HAADF TEM image of nanowire showing the heterostructure. Since As is a heavier element than P, the GaAs sections give a brighter contrast than the GaP parts [14].
2.1.2 Nanowire growth in PLD system

Prof Fengyuan Yang’s group at The Ohio State University has grown semiconductor nanowires in pulsed laser deposition (PLD) system. I conducted microscopic analysis and device fabrication with single nanowires and provided feedback from electrical and transmission electron microscopic (TEM) analysis in an effort to improve the quality of NWs.

To produce InP nanowires, first gold colloid (50 nm in diameter) solution (0.01% concentration, BBI International) is spun onto a substrate which is quickly rinsed with DI water and blown dry with nitrogen. InP targets containing 0.1% and 1% Se are prepared with InP polycrystalline powder by mixing In\textsubscript{2}Se\textsubscript{3} powder. Additionally, by mixing the InP with powder containing Se or Zn, either n-type or p-type InP nanowires can be grown, respectively. By differential doping on a single nanowire a p-n junction can be obtained which has applicable for nanowire LEDs and photodiode devices.

The growth temperature for InP nanowire is between 450 °C and 550 °C, and the pressure is controlled between 50 – 100 Torr using Argon as a carrier gas. A 2 Hz pulsed laser beam with a wavelength of 248 nm and pulse duration of 10 ns is focused into a 2.4\times3.9 \, \text{mm}^2 spot on the InP target to start the ablation which produces In and P vapors. The laser energy density is maintained at 1 – 2 \, \text{J/cm}^2 per pulse and the growth time is about 10 – 30 minutes. The nanowire length is directly proportional to growth time, in our system 15 – 30 minutes creates 10 – 20 \, \mu\text{m} length of nanowires. The PLD system comprises of a KrF excimer laser and a quartz tube furnace and is schematically shown in Fig 2.3.
Fig. 2.3 Schematic diagram of pulsed laser deposition (PLD) system for nanowire growth.

The major factor affecting optimum growth conditions is temperature. 470 °C ~ 520 °C is the best temperature window we have obtained. If the growth temperature is below 470 °C, nanowires deviate from cylindrical wire geometry. If the temperature goes above 520 °C, no wires are grown on the substrate. In the PLD system, it is hard to control the III-V vapor ratio as desired. The laser ablation on a new InP target causes the amount of P vapor generated to be more than that of In vapor because P is more volatile than In. This changes the III-V vapor ratio during the growth. Therefore, a relatively fresh target surface and moderate laser energy (1 – 2 J/cm² per pulse) benefit III-V nanowire growth. X. Zhao et al. reported successful GaAs nanowire growth in this PLD system [15]. Optical investigation of these InP nanowires had been carried out by Lei Fang et al. in our group [16].
2.2 TEM analysis of InP nanowires

Figure 2.4 is a scanning electron microscopy (SEM) image of InP nanowires grown in the PLD system. Most of nanowires are straight and have uniform geometry (no tapering). The typical nanowire length is 10 - 20 µm with a nanowire diameter of about 50 nm.

![SEM image of InP nanowires grown in pulsed laser deposition (PLD) system.](image)

For the characterization of nanowire quality and crystal structure, a high resolution transmission electron microscopy (HRTEM) analysis in a Tecnai F-20 was conducted in the campus electron optics facility (CEOF) at The Ohio State University. Figure 2.5 shows HRTEM images of representative an InP nanowire, (a) shows the tip of nanowire which has a gold bit on it with a nanowire diameter of 40 – 50 nm, (b) shows single crystal structure at the core of nanowire and 2 – 5 nm thickness of oxide shell. The different contrast patterns in Fig. 2.5(a) are Moire patterns created when the lattice surfaces are overlaid at an angle. Movement in these patterns (like liquid flow) is
observed while changing the angle in the TEM confirming that this contrast does not arise from defects in the nanowire.

Fig. 2.5. (a) HRTEM image of the tip of InP nanowire, (b) Single crystal structure (zinc-blende) at core of nanowire and outer oxide shell.

In a further investigation of HRTEM, Fig. 2.6(a) is a highly magnified image of Fig. 2.5(b) at the core of nanowire which shows no stacking faults. Figure 2.6(b) is a diffraction mode image taken at the same spot as Fig. 2.6(a). In Fig. 2.6(b), T is the transmitted beam spot and [112] is the zone axis. The core is found to have zinc-blende structure with growth direction along the <111> axis.

Fig. 2.6. (a) HRTEM image at the core of InP nanowire, (b) Diffraction pattern image showing zinc-blende structure with growth direction along the <111> axis.
Although bulk III-V semiconductors typically crystallize in the zinc-blende (ZB) form, stable wurtzite (WZ) phase is encountered in nanowire growth [17][18]. ZB is a cubic structure where the arrangement of atoms is the same as that of the diamond cubic structure but with alternating types of atoms at the different lattice sites. WZ crystal structure is a member of the hexagonal crystal system and consists of two tetrahedrally coordinated atoms that are stacked in an ABABAB pattern. Mishra et al. demonstrated that ZB and WZ structures of InP NWs have different band gaps (1.42 eV for ZB and 1.48 eV for WZ) [19]. They also have different optical properties such as different polarization direction in photoluminescence (PL) measurements.

An interesting aspect of III-V nanowire growth is the existence of both crystal structures in a single nanowire. Caroff et al. shows a mixture of wurtzite (WZ) and zinc-blende (ZB) segments by controlling the growth temperature and pressure, as shown in Fig. 2.7 [20]. This image shows the careful control of InAs nanowire growth needed to form hybrid crystal structures (WZ-ZB).

Fig. 2.7. Realization of WZ-ZB polytypic superlattice[20].
In our system, we observed stacking faults in some nanowire structures. Figure 2.8 shows these stacking faults along the nanowire growth direction. Each stack has very small thickness (1 ~ 5 nm) and the fault is not well identified from growth condition (there were variations of NWs from one growth: some of them are single crystal and some of them have stacking faults). Nanowires having stacking faults show wiggling surface due to the different crystal orientations so we avoid these nanowires for the TEM analysis.

![Stacking faults in InP nanowire grown in PLD system. Each stack has 1 ~ 5 nm thickness.](image)

Even though the evaporation target for InP nanowire growth contains 1% of Se, it is very difficult to estimate the actual doping level in nanowire due to the VLS growth mechanism. Non-uniform doping profiles on both axial and radial directions in a single nanowire are investigated in Ref. [21]. They used scanning photocurrent microscopy (SPCM) to obtain an axial doping profile and pulsed laser atom probe (PLAP) tomography to obtain a radial doping profile [22][23]. They demonstrated that there is an enhanced concentration of electrically active impurities at the surface of VLS grown nanowires. This suggests most of impurities (or defects) are distributed close to the
surface of nanowires. Even though the expected doping level is 1% based on the weight ratio in evaporation target, the actual doping level may be smaller than 1%. In chapter 3, the gate and temperature dependent I-V measurements will reveal that defect states play important role in electrical transport mechanisms and energy level of defect states is much deeper (~60 meV) than that expected from Se doping (~7 meV below conduction band). This implies that the desired doping level is not achieved and the effect of Se doping is suppressed by defect states.
2.3 Device fabrication

2.3.1 Preparing nanowire substrate

With the nanowires grown on a substrate (grown in Dr. Yang’s group), I created a fabrication process to make single NW devices for electrical transport measurements. Overall procedures will be discussed in this section. To harvest nanowires from as grown substrate, the nanowire substrate is immersed in methanol and sonicated for 10 seconds. One droplet of nanowire solution is dropped onto SiO$_2$/Si (= 300 nm/450 µm) substrate. This substrate is used because it is capable of supporting a field effect transistor (FET) structure with back gating. After dropping the NWs it is quickly dried using N$_2$ gun to avoid unwanted residue on the nanowire dispersed substrate. One can determine the nanowire density on the substrate with the use of 1000× magnification of an optical microscope. Usually a quick sonication ( < 10 seconds) in methanol and careful blowing substrate right after dropping the nanowire solution provides an desired nanowire density on the substrate without any significant residue.

2.3.2 E-beam lithography for patterning electrodes

Isolated high-quality nanowires are identified using SEM and the position and axial direction of a nanowire found from a reference point are recorded. Then Pt alignment markers are deposited on either side of the NW–used as guidance for the e-beam patterning–by focus ion beam (FIB).
The key steps in e-beam lithography are finding i) the exact position of NW with reference to the Pt markers, ii) correct e-beam parameters for each step of patterning layers, iii) development parameters with the e-beam developer. The detailed procedures and important parameters for e-beam lithography will be discussed in Appendix 1. These parameters were determined from tests that I have performed with the new e-beam lithography tool (FEI Helios-600) at ENSL (ENCOMM NanoSystems Laboratory) at The Ohio State University.

2.3.3 Comparing single and bilayer e-beam resist patterning

In this work, the e-beam lithography procedure uses a single layer polymethyl-methacrylate (PMMA). In the initial work of this project, a bilayer methyl-methacrylate/polymethyl-methacrylate (MMA/PMMA) was used for e-beam patterning in order to achieve an undercut making the lift-off process easy. We used MicroChem MMA(8.5) EL 11 for bottom-layer and MicroChem 950 PMMA A4 for top-layer. First, the MMA was spun onto substrate at 2000 rpm for 90 seconds and post-baked at 180 °C for 5 minutes. Second, PMMA was spun onto substrate at 1500 rpm for 90 seconds and post-baked at 180 °C for 5 minutes. Based on the datasheet from MicroChem, the expected thicknesses for MMA and PMMA are 700 nm and 300 nm, respectively. After e-beam exposure, the developing process of bilayer resists used a solution of Isopropyl-alcohol:Methyl-isobutyl-ketone (IPA:MIBK = 30 ml:10 ml) to make a proper undercut in the MMA layer (the MMA develops faster than the PMMA).
After developing the resist layers, Hydrochloric (HCl) acid dipping was conducted to remove native oxide layer on nanowire prior to loading into the chamber for metal deposition. Figure 2.9 shows the schematic of the developed bilayer resists. There is an undercut formed in the MMA layer which is supposed to be 0.2 µm – 0.5 µm wide, this width is roughly measured in optical microscopic. This undercut makes the lift-off process easier by avoiding a continuous metal deposition through resist and developed area.

However there is a large drawback in this undercut procedure. After the metal deposition and lift-off, a large amount of damage to nanowires was discovered. The NWs were partially or completely dissolved at specific areas close to the electrodes. The HCl liquid remained inside the undercut after HCl dipping as illustrated in Fig. 2.9. As a result, the HCl kept etching nanowire. This etching was non-uniform on the surface of nanowire and sometime etched the nanowire completely. In order to solve this problem, the MMA spin coating procedure was dropped to avoid the undercut. This leaves only the 300 nm thick PMMA layer for e-beam patterning. The thickness of metal in our device is 120 nm, so there is no lift-off problem.

![Diagram of bilayer resists](image)

Fig. 2.9. After developing the bilayer resists, there is undercut which acts as reservoir of liquid acid after the HCl dip. This remaining Acid damages nanowire. The red bar represents a nanowire.
2.3.4 Metal deposition and wiring

Contact metals are deposited on the sample using E-beam evaporation. In order to remove the native oxide layer on the InP nanowire, a quick (10 seconds) dipping in diluted acid (1:20 = HCl:H₂O) is conducted immediately before loading the samples into the evaporation chamber. Ge/Au/Ni/Au (2nm/20nm/50nm/50nm) is deposited on the sample with a typical deposition rate being around 0.3 Å/s. Ge/Au is the Ohmic contact metals to InP [24]. The total thickness is determined by the effect of anisotropic metal deposition on nanowire. Because the nanowire diameter is 50 nm, a metal thickness comparable to 50 nm may cause the disconnection of electrode over nanowire due to highly anisotropic deposition. In contrast, 120 nm of metal provides a continuous connection of electrode over nanowire. Figure 2.10(a) shows a metal layer (Orange color) being discontinuous over NW for thin metal deposition (metal thickness is less than NW thickness). However, Fig. 2.10(b) shows a continuous metal layer for a thicker metal deposition.

Fig. 2.10. Metal deposition on a NW. (a) Thin metal deposition makes a discontinuous metal layer over NW. (b) Thick metal deposition (thicker than NW diameter) provides continuous metal layer.
For the lift-off processing, the sample is immersed into Acetone for 20 minutes during which PMMA layer can be completely dissolved. Extra sonication to help lift-off shouldn’t be used as it destroys the nanowire.

Rapid thermal annealing (RTA) in forming gas (H\(_2\)/N\(_2\) = 5%/95%) environment is performed to reduce contact resistance between the metal stack and nanowire. The annealing temperature used is 320 °C and annealing time is 60 seconds. Ramping up the temperature is conducted in two steps to avoid overshooting: i) ramp up 200 °C and hold for 30 seconds, ii) ramp to 320 °C and hold for 60 seconds. 320 °C as annealing temperature is decided because vaporizing temperature of Indium atom from nanowire is around 400 °C.

Fig. 2.11(a) shows the SEM image of single nanowire device after finishing all device fabrication. Total nanowire length is 20 µm and the spacing between electrodes vary from 1.5 – 2 µm. Figure 2.11(b) shows an optical image of the device with four large contact pads that will be electrically connected to gold wires.

![Figure 2.11](image_url)

Fig. 2.11. (a) SEM image of a single nanowire device with 4 contacts. The substrate consists of SiO\(_2\)/Si = 300 nm/450 µm, with SiO\(_2\) as the gating dielectric layer. (b) Optical image of whole structure of device after metal deposition, there are four large contact pads (100 µm × 100 µm) for electrical wiring.
The sample is mounted on a chip-carrier with 20 pin connectors and a metal surface at the bottom. Instead of using hot soldering on contact pads, we connect gold wires to contact pads by pressing Indium solder. Back gate voltage is applied via the metal surface at the bottom of chip-carrier and only four connectors in the chip-carrier are wired to sample. The left picture in Fig. 2.12 is the sample mounted chip-carrier and holder which is located at the end of cryogenic sample stick. The sample stick is loaded into a magneto-optical cryostat (Oxford) where temperature and gate dependent electrical transport measurements are conducted. Measurement temperature varies from 300 K to 1.4 K and the maximum magnetic field available using superconducting magnet is 8 T (Field dependence is not conducted in this study). At the bottom chamber of this cryostat, there are view ports for optical measurement. The right picture in Fig. 2.12 is the magneto-optical cryostat used.

Fig. 2.12. Left is the cryogenic sample stick with chip-carrier and holder, right is an 8 T Magneto-optical cryostat.
2.4 Reference

15. X. W. Zhao et al., Nanotechnology 18, 485608 (2007).


Chapter 3: Charge transport mechanisms in high bias

3.1 Experimental Set-up

Electrical transport measurements are performed with typical 4-probe configuration, applying source-drain current to two outer electrodes and measure voltage from two inner electrodes, as shown in Fig 3.1(a). A DC power supply (Yokogawa 7651) and electrometer (Keithley 6514) are used for the current-source and voltage-meter. A Keithley 2400 is operated in order to apply gate voltage. For connecting the gate voltage source to the nanowire device, the positive output of the Keithley 2400 is connected to the back side of sample and the negative output of it is connected to ground, this ground point is also connected to the negative output of the current-source.

Careful wiring is required to prevent ground-loops that cause parasitic current which could destroy the nanowire.Appling a gate voltage between nanowire and back side of sample may induce a leakage current through 300 nm SiO_2 layer. Usually the leakage current is less than 1 nA for up to ±30 V of gate voltage. So, the maximum gate voltage we choose to use is ±30 V. Before completing temperature dependent IV measurements in cryostat, we did a preliminary I-V measurement at room temperature with a homemade circuit box which has same circuit configuration as that in the cryostat.
Figure 3.1(a) shows the schematic circuit diagram for 4-probe measurement and gate dependent I-V measurement. The substrate has a 300 nm thick SiO$_2$ insulating layer allowing it to be used as a field-effect-transistor (FET) device with back-gating. Figure 3.1(b) shows the homemade circuit box for room temperature electrical measurement. The measurement software used is LabVIEW version 2010 (National Instrument Co.).

![Diagram](image)

Fig. 3.1 (a) Schematic circuit diagram for a 4-probe measurement, (b) Homemade circuit box for room temperature I-V measurement.

A single nanowire has a very narrow conducting channel (average of 50 nm in diameter) with kΩ – MΩ range in resistance. As a result, a surge current while switching or plugging in BNC connectors can destroy nanowires. Figure 3.2 is the SEM image of a burned nanowire and its electrodes caused by surge current. In order to protect the nanowire from surges, we made a low pass filter circuit which passes a low frequency signal (DC bias in our system) but attenuates signals with frequencies higher than the cutoff frequency. This circuit is simply designed with capacitors and resistors. Static discharge (surge current) at the instant of switching passes through the capacitors, but will not flow through the nanowire. As a result, only the applied (DC) current passes...
through nanowire. All electrical lines and nanowire devices are shielded in grounding enclosures where the nanowire is protected from noise.

Fig. 3.2 SEM image of burned nanowire and electrodes due to static charge (surge current).

Figure 3.3 is the circuit diagram for the protection circuit which consists of resistors \((R_P)\) and capacitors \((C_P)\). Three \(R_{NW}\) represent resistances of left, middle and right sections of single nanowire which are divided by four electrodes. \(R_P\) and \(C_P\) are elements of one set of low pass filters used for each section of nanowire, where \(R_P\) is 10 kΩ and \(C_P\) is 2 nC. The cutoff frequency can be calculated as follow:

\[
f_{\text{cutoff}} = \frac{1}{2\pi R_P C_P}
\]

It suggests that a frequency higher than 8 kHz (usually surge current) will bypass the nanowire and pass through capacitor \((C_P)\), because the high frequency impedance is small in capacitor. Each electrode is connected to a toggle switch to either close or ground the circuit.
Fig. 3.3 Circuit diagram which has a low pass filter for each section of nanowire ($R_{NW}$). $R_P$ and $C_P$ provide a cutoff frequency for each section.
3.2 I-V characteristics

3.2.1 Comparing resistances by 2-probe and 4-probe I-V measurements

In order to find the contact resistance between the semiconductor nanowire and metal electrode, we compared resistances measured by 2-probe and 4-probe I-V measurements. In each case, the middle section of nanowire is measured to allow direct comparison. The measured resistance in the 2-probe I-V measurement includes two contact resistances, so the resistance of one contact is roughly calculated from a half of difference between the 2-probe and 4-probe resistances. From Fig. 3.4, the contact resistance is around 0.04 MΩ which is almost 1% of nanowire resistance value. So, the effect of the contact resistance on the charge transport mechanisms is largely negligible in our systems. All I-V data shown in chapter 3 and 4 are measured in the 4-probe configuration.

![I-V Characteristics graph](image)

Fig. 3.4 Comparison of resistances measured by 2-probe and 4-probe I-V measurements. The contact resistance is around 0.04 MΩ which is less than 1% of nanowire resistance.
In Fig. 3.4, the nanowire resistance is about 4.8 MΩ which is in the range of typical nanowire resistance (1.7 MΩ ~ 10 MΩ) showing trapped space charge limited current (trapped-SCLC) at high bias regime (discussed in Chapter 3) and hopping transport mechanisms at low bias regime (discussed in Chapter 4). Beyond this resistance range, many devices (70% of fabricated devices) have shown large resistance (close to GΩ range) at room temperature. The resistances of these nanowires increase as temperature decreases and shown almost flat I-V curves (tens of GΩ) below 200 K. As a result, the analyses (showing power-law behaviors and fitting for extraction of zero-bias resistances) create errors larger than the resistance variations as temperature changes. Therefore these high resistance nanowires could not be well studied to observe trapped-SCLC and hopping mechanisms. Here we report the transport properties of the typical nanowire whose resistance is in between 1.7 MΩ and 10 MΩ.

3.2.2 Gate dependent current behavior

In our system, InP is doped with Se which in principle makes it an n-type semiconductor. The typical way to check the doping is through a gate response measurement. A gate voltage \( V_g \) is applied to the substrate to populate or extract electrons from nanowire. Constant source-drain bias \( V = 0.03 \) V is applied to the two inner electrodes (2-probe measurement for middle section of NW) and the current is measured while sweeping the gate voltage from \(-30 \) V to \(+30 \) V. Figure 3.5 is the measured current plotted as a function of gate voltage in a constant source-drain bias. The gate voltage is limited to ± 30 V due to the leakage current between the nanowire and
substrate. Usually, the leakage current is less than 1 nA when the $|V_g|$ is less than 30 V. However, it begins to increase to more than 1 nA when $V_g > +30$ V or $V_g < -30$ V. If this happens, it inhibits an accurate electrical measurement from nanowire.

![Image of graph showing gate dependent current measurement](image.png)

**Fig. 3.5** Gate dependent current measurement in a constant source-drain bias. The plot shows $n$-type behavior of semiconductor in positive gate voltage and shows saturation in negative gate voltage.

In Fig. 3.5, the plot clearly shows linear behavior above $\pm 10$ V of gate voltage as expected for $n$-type FET device. More electrons are accumulated in the conduction band when a positive gate voltage is applied; however the plot is saturated in the negative gate voltage regime. Applying $V_g = +30$ V increases the current by factor of two compared to the current at $V_g = 0$ V, while at $V_g = -30$ V the current is reduced only by 20%. This behavior at a negative gate voltage is not expected in a properly $n$-doped semiconductor FET device.

By applying a negative gate voltage, the electrons are depleted from conduction band which should cause the current to decrease to zero by completely depleting the conduction band. However, there is still a measurable (even saturating) current in the
negative gate voltage regime. This suggests that there are two distinct transport regimes in this system: i) Band conduction in positive gate voltage regime ($V_g > \sim 10$ V), ii) Other transport mechanism in small and negative gate voltage regime ($V_g < \sim 10$ V). These gate dependent behaviors are discussed in chapter 3 and 4 where tuning of transport mechanisms is described.
3.3 Space charge limited current (SCLC)

3.3.1 Temperature dependent I-Vs

At the beginning of transport measurements, we conducted the measurements in a 2-probe configuration and observed the non-linear I-V curves. This nonlinearity is exacerbated at low temperature, Fig. 3.6(a). Because the Schottky barrier is a potential barrier formed typically at a metal-semiconductor junction, we first compare our data (measured in a 2-probe configuration) with the Schottky diode equation. As discussed in Chapter 1, the current over Schottky barrier can be expressed in the case of thermionic emission [1]:

\[ J \propto J_0 \exp \left( -\frac{q \phi_b}{kT} \right) \exp \left( \frac{qV}{nkT} \right) - 1 \]  \hspace{1cm} (3.1)

where \( \phi_b \) is Schottky barrier height, \( q \) is elementary charge, \( k \) is Boltzmann constant and \( n \) is the ideality factor.

![Fig. 3.6](image)

Fig. 3.6 (a) Linear plots of temperature dependent I-V curves measured in a 2-probe configuration, (b) Semi-log plot of (a) is showing non-linear behavior.
The first thing to determine the Schottky diode behavior is to create a semi-log plot of the I-V curves. Because the current density in Eq. (3.1) is an exponential function of applied bias ($V$), the semi-log plot of I-V should exhibit linear characteristics for Schottky diode behavior. We plot Fig. 3.6(a) in semi-log scale, with the result shown in Fig. 3.6(b) where we see non-linear curves. As a result, we believe that the I-Vs in Fig. 3.6(a) do not have Schottky diode characteristics.

As a further investigation of Schottky diode behavior, we fit the I-Vs in Fig. 3.6(a) to Eq. (3.1). The black-solid curves, for positive $V$ region in Fig. 3.6(a) are these fitted results. The only $V$ dependent term in Eq. (3.1) is $\exp(qV/nkT)$, and the ideality factors ($n$) can be extracted from the fitting parameter $q/nkT$ at specific temperature $T$. The result is that $n$ varies from 124 (300 K) to 72 (110 K). These ideality factors are extremely large, they should be less than 2 in a real Schottky junction ($n = 1$ for an ideal Schottky junction). These further confirm that the I-Vs in Fig. 3.6(a) cannot be explained by the Schottky diode equation, Eq. (3.1).

Now all I-V measurements in the following sections are taken in a 4-probe configuration, and we expect a linear behavior of the I-Vs because of the low contact resistances (as shown in Fig. 3.4). However, the I-V curves show non-linear behaviors for most temperature regimes as similar as 2-probe measurements (Fig. 3.6(a)). Because we do not expect the Schottky effect in a 4-probe measurement, we need further analysis to find the transport mechanism at high bias regime.
3.3.2 Trapped space charge limited current (Trapped-SCLC)

The I-V curves in a 4-probe measurement show non-linear behaviours and are not expected to be the current in Schottky junction. Now we are exploring whether these are power-law, and log-log plot of I-Vs is the best way to check for that.

![Log-log plot of I-V curves](image)

Fig. 3.7 (a) Log-log plot of I-Vs measured in a 4-probe configuration, showing linear behaviors at high bias regime and the slopes increase as temperature decrease, (b) Extension of linear slopes may converge to a single point.

Figure 3.7(a) shows the log-log plot of the temperature dependent I-V curves measured in a 4-probe configuration. These clearly show a linear behavior in the high bias regime, above 0.2 V for 300 K and 0.5 V for 90 K. This indicates that the current is not an exponential function of $V$, but rather a power law function. There are two key features of the data in Fig. 3.7(a) that provide further insight into the transport mechanism: i) the slope is temperature dependent and ii) linear extrapolation of the data for high temperatures ($T > 150$ K, solid lines in Fig. 3.7(b)) converge to a single voltage, $V_C$, which shows a similar behavior to Fig. 1.4. In chapter 1, these characteristics were
discussed in conjunction with the trapped space charge limited current (trapped-SCLC) model, expressed as [2]:

\[ J_i \propto V^{i+1}, \quad I = T_i / T \quad (3.2) \]

From Fig. 3.7(a) only the linear regime is valid for the SCLC model, which can be denoted as \( I \sim V^\delta \) with the slope increasing as temperature decreases. The range of the linear fits is determined by systematically reducing the range of fitting until no significant variation in \( \chi^2 \) is observed. The fit results are shown as black solid lines with temperature dependent slopes (1.21 at 300 K and 1.84 at 90 K). Fig. 3.8(b) is the extension of these slopes to determine their convergence. The high temperature slopes converge around 21 V (average value of converging points: 300 K and 270 K meets at ~14 V, 300 K and 180 K meets at ~ 28 V). The lowest three temperatures (150 K ~ 90 K) show deviation from this converging behavior. This may suggest that there is a different transport mechanism in the low temperature regime. These phenomena – different transport mechanisms at high and low temperatures – are also observed when investigating hopping transport mechanisms which will be analyzed based on zero-bias resistances vs. \( I/T \) plots and will be discussed in Chapter 4.
3.4 Discussion

3.4.1 Calculations of trap concentration

In Fig. 3.7, there is a crossover point where the current is nearly temperature independent. This behaviour is similar to the plot from the trapped-SCLC model, Fig. 1.4. Again the current density from trapped-SCLC model can be written as [3]:

\[ J = \frac{\mu q NV}{d} \exp \left\{ \frac{E_t}{k_BT} \ln \left( \frac{qH_t d^2}{2eV} \right) \right\} \]  \hspace{1cm} (3.3)

From Fig. 3.7(b), the high temperature (T > 150 K, solid lines) slopes converge to a single point, \( \sim 21 \) V. Here we estimate the defect state density in nanowire. At this converging point, the current density from Eq. (3.3) is temperature independent, and the trap concentration can be derived, see Eq. (1.7),

\[ H_t = \frac{2eV_C}{qd^2} \]  \hspace{1cm} (3.4)

where \( d \) is channel length and \( \varepsilon \) is permittivity of InP. Here we use \( d = 3 \) \( \mu \)m and \( \varepsilon = 12 \varepsilon_0 \) (bulk value of InP). The data from Fig. 3.7(b) gives values of \( H_t \) that vary from \( 1.4 \times 10^{16} \) cm\(^{-3} \) to \( 2.8 \times 10^{16} \) cm\(^{-3} \), yielding an average \( H_t \) of \( 2.1 \pm 0.4 \times 10^{16} \) cm\(^{-3} \). \( H_t \sim 2.1 \times 10^{16} \) cm\(^{-3} \) can be estimated to be the total trap density in nanowire.

Figure 3.8 is a cartoon illustrating how electrons move through a nanowire while trapped in defect states. We expect that trap states are mainly distributed close to the surface of the nanowire. Some of electrons injected by applying source-drain bias \( (V) \) will be trapped in these states. These localized (trapped) electrons induce localized electric field which affects the conduction band transport behavior.
Fig. 3.8 Cartoon for illustrating electron transport behavior. Injected electrons are trapped in defect states in nanowire; the electric field induced by trapped electrons can affect the conduction band transport behavior.

3.4.2 Gate dependence of trapped-SCLC behaviour

In Fig. 3.5, the gate dependence of the current can be viewed as two regimes based on the linearity of graph. The first regime is the linear slope at positive gate voltage which reveals the $n$-type semiconductor characteristic. Meanwhile, the second regime is the saturation at negative gate voltage which is considered a transport mechanism differing from band transport. This analysis in turn allows us to better understand the gate dependence of electron transport mechanisms. If we interpret the transition at $V_g = +9$ V as the Fermi level moving from the defect states into the conduction band of InP, then at $V_g = +9$ V the electron density is equal to the total trap density, i.e. $n_e = 2.1 \times 10^{16}$ cm$^{-3}$.

This idea can be represented in the gate dependent current plot. Figure 3.9 shows two distinct regimes based on filling the trap states (moving the Fermi level) by applying gate voltage. The gray region in this plot is where the defect states are fully filled and the conduction band transport dominates. The yellow region shows the partially filled defect states and a different transport mechanism.
Fig. 3.9 Gate dependent current measurement at a constant source-drain bias. It has two distinct regimes which show filling the trap states and conduction band transport.

In order to better understand these phenomena the schematic diagram for charge transport and its dependence on gate voltage is illustrated in Fig. 3.10. When the Fermi level goes into the conduction band at $V_g > +9$ V, the SCLC behavior is the dominant mechanism because the conduction band transport is affected by localized charges. When $V_g < +9$ V, the Fermi level moves below the conduction band and SCLC behavior is suppressed due to charge transport within the defect states.

Fig. 3.10. Schematic diagram of charge transport by varying the Fermi-level through gate voltage.
This hypothesis is further supported by the dependence of the SCLC regime on gate voltage. The SCLC model is valid where band carriers and trap states coexist, and this regime of validity extends to lower $V$ and lower temperature as the gate voltage, and consequently $n_e$, increases above $V_g = +9$ V (the opposite trend is seen for gate voltage decreasing below $V_g = +9$ V).

Figure 3.11 (a) – (c) show I-V characteristics of a nanowire FET on a log-log scale for positive gate voltages. The region of linearity extends to increasingly lower bias and lower temperature as the gate voltage increases, so the region of validity for the SCLC model increases (coexistence of band carriers and traps). Figure 3.11 (e) – (f) show similar plots for negative gate voltages (all plots have the same current and voltage scale). The region of linearity for these gate voltages shows opposite behaviour trend (shrinking as gate voltage increases in the negative direction) and pure hopping transport dominates SCLC.

Because these two-channel transport properties are observed in nanowires whose resistances range in $1.7 \text{ M}\Omega \sim 10 \text{ M}\Omega$ and trap density is about $2 \times 10^{16} \text{ cm}^3$, it is expected that this specific value of defect (trap) density is the crucial value to observe the trapped-SCLC behaviour and the crossover of hopping mechanisms (see Chapter 4) from a single nanowire systems.
Fig. 3.11. (a) – (f) I-V characteristics on log-log scale for different gate voltages. At the largest negative gate voltage (-30 V, panel (f)) the Fermi level lies deep in the trap states, far from the conduction band, and hopping transport dominates at all but the highest temperatures and highest source-drain bias. As the gate voltage increases towards positive values mixed band- and trap-mediated transport (the SCLC regime) dominates to increasingly lower temperatures and lower source-drain bias. At a gate voltage of +30 V (panel (a)) the SCLC regime dominates almost the entire measurement window.
3.4.3 Density-functional theory (DFT) calculation of defect level

In order to provide insight into the nature of the defects giving rise to the trap states, we determine the formation energy of competitive defects in “bulk” InP from density-functional theory (DFT). This calculation is performed by Prof. Wolfgang Windl’s group in Department of Materials Science and Engineering at The Ohio State University.

The trapped-SCLC model implicitly assumes the presence of relatively shallow trap states, i.e. states within a few times $k_B T$ of the conduction band with coupling to the band states. The calculations are performed for supercells with 108 formula units using the VASP package and potentials [4]; the Generalized-Gradient Approximation (GGA) [5], cross-checked by the HSE06 hybrid-functional [6]; and a $2 \times 2 \times 2$ $k$-points mesh for the Brillouin zone integration. Charge states are treated in analogy to Ref. [7]. XPS measurements suggest that the native oxide on InP is P rich at the interface, and that the oxidation reaction happens at the surface [8]. This suggests that InP close to the interface initially becomes In rich, and the excess In eventually migrates to the surface for further oxidation. Thus, we assume In-rich conditions in the nanowire for determining the chemical potentials for defect calculations. Using the method of constitutional defects [9], we find $\text{In}_p^{-1}$ and $\text{O}_p^0$ to be the most stable defects that also create a trap state near the conduction band edge. Assuming that the oxidation reaction indeed happens at the surface [8], it is however less likely that $\text{O}_p^0$ defects will form (and if they do, are found to form an atomic-like deep level), leaving $\text{In}_p^{-1}$ with a shallow level ~60 meV below the
conduction-band edge (see Fig. 3.12) as a plausible candidate for the trap states identified above [10].

![Band structures by DFT calculation. It demonstrates the band structure for “bulk” InP at three cases: InP$^{-1}$, O$_P$ and P$_{in}^{+2}$. InP$^{-1}$ is the most plausible candidate for the trap states identified by DFT calculation.](image)

3.4.4 Mobility determination

Electron mobility ($\mu$) can be determined from the trapped-SCLC model, Eq. (3.3), where $d$ is nanowire length and $N$ is band density of states. Because the SCLC model is valid in the high bias regime, mobility from trapped-SCLC model at $V = 0.9$ V is plotted in Fig. 3.13 (red-circles). This is the mobility contributed by the band transport. This graph shows that the mobility is inversely proportional to the temperature and varies from $\sim 2000$ cm$^2$/V·s (100 K) to $\sim 200$ cm$^2$/V·s (300 K). These values are similar to the reported mobility in III-V nanowires grown in CVD [11]. The trapped-SCLC model is not valid for mobility calculation at low bias because the number of injected charges is too small to generate a space charge effect. Thus in order to determine the mobility at low bias regime
we used charge-control model (CC model) which determines the mobility using nanowire capacitance \(C_{NW}\) and gate voltage to cut-off the source-drain current [12].

In a 1D system, the total charge in nanowire can be determined from \(Q = C_{NW}V_g\), where \(V_g\) is the gate voltage to completely deplete (cut-off) charges in nanowire. This cut-off gate voltage is determined through an extrapolation from \(I\) vs. \(V_g\) graph in Fig. 3.9. The intersection of the extrapolated slope and the x-axis is the cut-off voltage. The NW capacitance per unit length is given by:

\[
\frac{C_{NW}}{L} \approx \frac{2\pi \varepsilon}{\ln(2h/r)}
\]

where \(r\) and \(L\) are the NW radius and length, and \(h\) and \(\varepsilon\) are the thickness and the permittivity of the gate oxide layer. The NW is considered to be a metallic cylinder, which is a good approximation as long as the density of states at the Fermi level is high. Using these parameters in our systems, the calculated capacitance between cylindrical nanowire and infinite conducting plane (separated by 300 nm SiO\(_2\) layer) is \(1.4 \times 10^{-16}\) F.

The mobility can be calculated from \(\mu = 1/qn\rho\), where \(q\) is the elementary charge, \(n\) is the carrier density and \(\rho\) is the resistivity of nanowire. The carrier density \(n\) can be calculated from total charge \(Q\) divided by volume of NW. The blue-squares in Fig. 3.13 show the calculated mobility at \(V = 0.03\) V from CC model. This graph is directly proportional to temperature and varies from \(0.2\) cm\(^2/V\cdot s\) \((T = 120\) K\) to \(3\) cm\(^2/V\cdot s\) \((T = 300\) K\). This mobility value for low bias is three orders smaller than that of band transport electron and increases as temperature increases. These behaviours (low mobility and proportional to temperature) can be considered properties of phonon assisted hopping transport [13][14].
Even though trapped-SCLC model gives the mobility only contributed by band transport, the mobility from CC model gives the effective mobility contributed by both band transport and defect states mediated transport. As discussed in section 3.4.2, there is coexistence of band carriers and trap states. The mobility in SCLC model shows the mobility from single channel (conduction band), revealing high mobility values. However this behaviour can be suppressed at low bias regime (defect mediated transport dominates), revealing low mobility values which is determined by CC model. The comparison of these two mobility values provides the evidence of the coexistence of two conducting channels in our NW systems.

![Graph showing mobility comparison between SCLC and CC models](image)

Fig. 3.13. The red-circles show the mobility calculation from trapped-SCLC model. The blue-squares show the mobility calculations from charge-control (CC) model. The mobility by trapped-SCLC model represents the mobility of electrons which transport in conduction band (reveals high mobility values). The mobility by CC model represents the effective mobility by the overall electron transport.

Further, the calculated capacitance of the nanowire FET allows the determination of the carrier concentration at any arbitrary voltage. From Fig. 3.9, the carrier density at zero gate voltage can be estimated from the extrapolation of linear slope in the positive
gate voltage regime. This is $1.4 \times 10^{16} \text{ cm}^{-3}$. Given the 3 $\mu$m length and 50 nm diameter of the channel this corresponds to $N_e \sim 53$ and $\sqrt{N_e} \sim 7$ (where $N_e$ is the total number of electrons), placing these nanowires solidly within the statistical doping regime [15].
3.5 Reference


10. O. D. Restrepo *et al*., to be published.


Chapter 4: Hopping transport in semiconductor nanowire

4.1 Introduction

As discussed in Chapter 3, we believe there is a coexistence of band carriers and trap states in our NW system. A high source-drain bias ($V$) injects a large number of electrons into the nanowire; some of these electrons occupy trap states while the other portion occupies the conduction band and dominates transport. Trapped-SCLC is dominant in this high bias regime. However at a low bias (and specifically zero-bias), the band carrier density is negligible because most of the electrons are trapped, making transport through trap states (defect states) the dominant transport mechanism. Here we investigate the zero-bias resistance as a function of temperature to examine this defect mediated transport mechanism.
4.2 Hopping transport properties

4.2.1 Temperature dependence of zero-bias resistance

Here, we consider the regime where the trapped-SCLC model is not valid, i.e. low applied bias \( V \) and low temperature, where the Fermi level lies in the defect states and hopping transport is expected. Generally, the accepted models of hopping transport follow the form [1]:

\[
R = R_0 \exp\left(\frac{T_0}{T}\right)^m
\]  

(4.1)

where \( R_0 \) indicates the overall resistance of the channel, \( T_0 \) relates to the energy scale of the hopping transport and \( m \) is a constant less than or equal to 1 that indicates the mechanism of the hopping transport.

Figure 4.1(a) is the linear plot of zero-bias resistances as a function of 1000/T. In order to extract the values of constants in Eq. (4.1) for the InP NWs studied here we plot Fig. 4.1(a) on a \( \log(\ln(R)) \) vs. \( \log(1/T) \) scale in Fig. 4.1(b). In Fig. 4.1(b) one finds two slopes, \( m_{\text{high}} = 1.03 \pm 0.02 \) at \( T > 158 \) K and \( m_{\text{low}} = 0.49 \pm 0.02 \) at \( T < 158 \) K, that denote two distinct transport mechanisms.
Fig. 4.1. (a) Linear plot of zero-bias resistances as a function of $1000/T$. (b) Log-log plot of $ln(R)$ vs. $1000/T$, this reveals the different slopes in high and low temperature regimes and a crossover temperature between two regimes (158 K). This measurement is conducted at zero gate voltage ($V_g = 0$ V).

Here, different values of the exponent $m$ represent different hopping mechanisms. The slopes (measured at zero gate voltage; $V_g = 0$ V) indicate nearest-neighbor hopping (NNH) for $m_{high} = 1$ and Efros-Shklovskii variable range hopping (ES-VRH) for $m_{low} = 0.5$ [2]. Multiple nanowire samples show this crossover with values ranging from $m_{high} = 1.02 \sim 1.24$ to $m_{low} = 0.49 \sim 0.68$ with crossover temperature $156$ K $\sim 225$ K at $V_g = 0$V. This crossover phenomenon between two hopping mechanisms was also reported in hydrogenated amorphous Si-film [3] with a transition from NNH to ES-VRH at 220 K. The crossover between these two hopping regimes is schematically illustrated in Fig. 4.2. At high temperature ($k_B T$ greater than the average variation in trap energy) phonon-assisted hopping allows access to NN hopping sites. As the temperature decreases the range of energetically accessible hopping sites decreases and VRH dominates. Detailed calculations of hopping parameters in each regime are discussed in the next section.
Fig. 4.2. Schematic illustration of the two hopping mechanisms; nearest-neighbor hopping (NNH) in a high temperature regime and variable-range hopping (VRH) in a low temperature regime.

4.2.2 Determination of hopping parameters

The hopping parameters are calculated to aid in evaluating the hopping mechanisms quantitatively. The hopping energies, for both NNH and ES-VRH, can be determined by fitting Fig. 4.1(b) to following equations [2][4],

\[ R \propto \exp\left(\frac{T_{NNH}}{T}\right) \quad , \quad R \propto \exp\left(\frac{T_{ES\text{-}VRH}}{T}\right)^{1/2} \]  \tag{4.2} \\

\[ E_{NNH} = k_B T_{NNH} \quad , \quad \Delta_{hop, ES} = \frac{1}{2} k_B \left(T_{ES\text{-}VRH} T\right)^{1/2} \]  \tag{4.3}

where \( T_{NNH} \) and \( T_{ES\text{-}VRH} \) are the characteristic temperatures in each hopping mechanism, they are determined by fitting data to Eq. (4.2). \( E_{NNH} \) is the NNH energy and \( \Delta_{hop, ES} \) is the ES-VRH energy (they are the average hopping energy difference between sites in NNH and ES-VRH). We find that \( E_{NNH} = 58 \text{ meV} \) (in good agreement with our DFT calculations of the Inp\(^{1+}\) defect; see section 3.4.3), while \( \Delta_{hop, ES} = 19 \text{ meV} \) at 100 K. In the VRH model, the accessible sites vary as the temperature changes. So the hopping energy also varies as temperature changes, see Eq. (4.3). Additionally the hopping distance variation in VRH with respect to temperature changes the strength of the coulomb
interaction which causes the temperature dependent ES-VRH energy. As a result the NNH energy is 58 meV and the ES-VRH energy varies from 23 meV (at 158 K) to 19 meV (at 100 K) in this system. These two numbers indicate that NNH happens at high temperature regime and ES-VRH at low temperature regime because VRH prefers long range hopping with small energy excitations, illustrated in Fig. 4.2.

The average separation between carriers \((r_0)\) is calculated with the simple relation:

\[
\frac{4}{3} \pi (r_0)^3 = \frac{1}{n_e}
\]

For a typical sample at \(V_g = 0\) V we have \(n_e = 1.4 \times 10^{16} \text{ cm}^{-3}\), giving \(r_0 \sim 25\) nm. At the same time, the thermal deBroglie wavelength is given by:

\[
\lambda_t = \frac{h}{\sqrt{2\pi m_e k_B T}}
\]

where \(h\) is Plank constant, \(m_e\) is the effective mass of electron in InP \((m_e = 0.08 \times m_0)\) and \(k_B\) is Boltzmann’s constant.

In our samples \(\lambda_t\) varies from 27 nm at \(T = 100\) K to 16 nm at \(T = 300\) K, showing that these two length scales are comparable at zero gate potential and the system becomes more quantum effect dominant with increasing gate voltage or \(n_e\) \((r_0 \sim 22\) nm at \(V_g = +9\) V). By this simple estimate, our samples exist in a quantum regime for the entire phase space covered by our measurements, while both NNH and ES-VRH are considered in a classical regime with electron-electron interactions.

Here we extract several parameters to aid in understanding hopping dimensionality. Localization length of electron in defect state and average hopping distance in ES-VRH can be written by [5]
\[ \xi = \beta \frac{e^2}{k_B T_{ES} \varepsilon}, \quad R_{hop,ES} = \frac{\xi}{4 \left( \frac{T_{ES}}{T} \right)^{1/2}} \]

where \( \varepsilon = 12\varepsilon_0 \) (the static dielectric constant is the bulk value for InP) and \( \beta \) is the percolation coefficient in the ES-VRH model [5]. \( \beta \) is predicted theoretically to be between 3D (\( \beta = 2.8 \)) and 2D (\( \beta = 6.5 \)) hopping systems [6]. In order to estimate \( \beta \) for our system, we used the crossover temperature (~158 K) from Fig. 4.1(b).

From above equation, \( R_{hop,ES} \) decreases as the temperature increases because higher temperatures cause a reduction in VRH distance, therefore the shortest variable range hopping distance should be the nearest-neighbor distance at high temperature (\( T > 158 \) K). Thus the two hopping distances (NNH and ES-VRH) can be the same value at a crossover temperature. As a result \( r_0 \) and \( R_{hop,ES} \) become 25 nm at \( T = 158 \) K and \( V_g = 0 \) V. From \( R_{hop,ES} = 25 \) nm, localization length \( \xi \) is 23 nm and \( \beta \) is calculated as 3.9 in this particular system. This value is an intermediate value between a 2D and 3D hopping network which implies that the hopping transport occurs in a 3D hopping network with 2D contributions—hopping in a bulk system but close to the surface of the nanowire.
4.3 Gate dependent hopping transport

4.3.1 Gate dependence of $R$ vs. $I/T$ plot

We have found two different slopes in the temperature dependent zero-bias resistance plot which indicates a crossover between two hopping mechanisms. Here we investigate the gate dependence of the crossover temperature and the changes of hopping parameters. In Fig. 4.3(a), the crossover temperature (158 K at $V_g = 0$ V) depends on gate voltage and shifts to lower temperature with increasing positive gate voltage: 156 K at $V_g = 10$ V, 145 K at $V_g = 20$ V and 130 K at $V_g = 30$ V. For negative gate voltages, the shape of the curve becomes more complex and does not exhibit a well-defined crossover for much of our measurement window (nanowire resistance exceeds 1 GΩ for low temperatures and large negative gate voltage), as shown in Fig. 4.3(b).

![Fig. 4.3. Gate dependent log-log plot of ln(R) vs. 1000/T.](image)

(a) Plots for positive gate voltages show the shift of crossover temperature ($T_{cr}$ move to lower temperature with increasing $V_g$), (b) Plots for negative gate voltages shows not well defined crossover.
4.3.2 Gate dependence of hopping parameters

When the crossover temperature between NNH and ES-VRH, \( T_{cr} \), is plotted as a function of the gate voltage, the same critical value of +9 V is identified as a point of departure from the physics at zero gate voltage (Fig. 3.9). This trend is confirmed when a similar analysis is performed for \( m_{\text{low}} \), \( T_{\text{NNH}} \) and \( T_{\text{ES-VRH}} \) in Fig. 4.4. While this variation lies beyond the scope of current theory, we can gain a qualitative understanding by referring to the two-channel model presented in 3.4.2 (Gate dependence of trapped-SCLC).

At high temperature NNH, or Arrhenius, transport is characterized by thermal activation to the conduction band followed by re-trapping at a NN site. In this regime the increased gate voltage merely increases the number of carriers capable of executing these hops, resulting in a relatively weak perturbation from the zero gate voltage case (\( T_{\text{NNH}} \) increases by about 12%, yellow plot in Fig. 4.4(b), and \( m_{\text{high}} \) does not vary to within experimental error).

![Gate dependent plot of hopping parameters](image)

Fig. 4.4. Gate dependent plot of hopping parameters. (a) Plot for \( T_{cr} \) and \( m_{\text{low}} \) which show significant deviation when \( V_g > +9 \) V. (b) Plot for \( T_{\text{NNH}} \) and \( T_{\text{ES-VRH}} \), \( T_{\text{NNH}} \) varies in ~ 12 % at \( V_g = +30 \) V, but \( T_{\text{ES-VRH}} \) varies up to 300% at \( V_g = +30 \) V.
In contrast, at low temperature the hopping transport undergoes a more dramatic change as the Fermi energy enters the conduction band (the increase in $T_{ES-VRH}$ is ~300%, purple plot in Fig. 4.4(b)). Focusing on the behavior of $m_{low}$, one might expect an increase towards $m = 1$ as the presence of carriers in the conduction band opens a channel for NNH or band transport; what is actually observed is a decrease in $m_{low}$ in Fig. 4.4(a).

In order to understand this phenomenon we discuss it and the possibility of the existence of ES-VRH through a disorder potential.
4.4 Disorder potential by trap states

In the previous section, we found that $m_{\text{low}}$ decreased as the gate voltage increased. While attempting to understand this result, it is useful to consider two structural shortcomings of both the NNH and ES-VRH models.

First, both models assume that transport physics can be described by a single conduction channel with a well-defined energy scale, localization length, etc. However, our analysis of the trapped-SCLC regime indicates that for $V_g > +9$ V both trap states and conduction band states are occupied, Fig. 3.9. Moreover, while transport through defect states proceeds through ES-VRH (as demonstrated by the $V_g = 0$ V data in Fig. 4.3), transport within the conduction band occurs in the presence of a disorder potential defined by the spatial distribution and the occupancy of trap states. This disorder potential can lead to the breakup of the conduction band into grains and, at low temperature and low bias, likely leads to hopping transport in the conduction band as well [7]. A theoretical study of disorder potential is discussed in Appendix 2 and was performed by Prof. Igor S. Beloborodov at California State University at Northridge.

As a result, a full theoretical description of the transport in this regime needs to account for two parallel conduction channels that are correlated by the interplay between trap state occupation and the disorder potential in the conduction band. Figure 4.5 shows the schematic diagram illustrating transport mechanisms. The Fermi level ($E_F$) moves into the conduction band edge when $V_g > +9$ V at low temperature, then electron
transport occurs on the disorder potential in the conduction band as described by the ES-VRH mechanism.

Second, and more generally, the low-temperature low-bias (V) regime is characterized by a competition between correlation effects and disorder. The average separation between carriers, $r_0$, is comparable to the thermal deBroglie wavelength for all temperatures considered here (roughly 25 nm and 16 – 27 nm, respectively; see previous section 4.2.2). This result implies both that the electron-electron interactions are important (i.e. Mott-VRH does not apply) and that this system is well into the quantum regime while both NNH and ES-VRH treat electron-electron interactions classically. The primary effect of these quantum correlations will be to modify the low-energy density of states, suggesting future studies exploiting tunneling physics to directly probe this variation.
4.5 Conclusion in charge transport in InP NW systems

4-probe I-V measurements in InP nanowires reveal that there are two transport channels: i) conduction band and ii) trap states. Transport mechanisms through these two channels can be tuned by applying a gate voltage, and detailed characteristics were investigated with a temperature dependent experiment. Our comprehensive exploration of defect- and disorder-mediated transport in semiconducting nanowires reveals a rich interplay between localized trap states, conduction band transport, quantum effects and electron-electron correlations in the statistical doping regime. These experimental results provide a foundation for extending current models of hopping transport to account for multiple conduction channels and the competition between correlation and disorder as well as suggesting promising directions for further experiments to determine the detailed nature of the low-energy density of states. These fundamental studies provide critical insight into the transport mechanisms likely to be found in next-generation nanoscale electronic devices.
4.6 Reference


Chapter 5: Si nanowire array by sub-lithographic patterning

5.1 Introduction

5.1.1 Overview of superlattice nanowire pattern transfer (SNAP)

Superlattice nanowire pattern transfer (SNAP) is a process used to fabricate nanowires array with a nanowire width of several nanometers. This process was developed in Prof. James Heath’s group [1-5] and can be applied to many types of materials – such as semiconductors, metals and graphene – to obtain patterned nanowires or nanoribbons. The SNAP process for fabricating graphene-nanoribbon (GNR) was developed by Ke Li, a former member of the Johnston-Halperin group [6]. Here we focus on the fabrication and electrical measurement of Si NW arrays produced by the SNAP process.

SNAP has several key advantages in NW-based integrated nanoelectronics. It offers extremely narrow width distribution, high aspect ratios of length-to-width up to $10^6$, and a highly defined array of NWs and pitches. These properties can be adapted to many applications such as logic circuits, crossbar molecular memory circuits [4] and thermoelectronics [7][8].
SNAP is a ‘top-down’ NW fabrication process where the channels are etched into the substrate. Si or metal NWs are aligned over millimeter length scale with NW width and pitch (center to center distance) as small as 7 nm and 15 nm, respectively. Compared to VLS grown nanowires, the big advantage of SNAP nanowires is that the purity of the NWs is limited only by the purity of substrate, which can be much better than VLS grown nanowire systems because impurity can be readily incorporated during VLS growth of the NWs. The VLS growth of Si NWs needs metal nanoparticles to seed growth, which can also serve as an impurity dopant [9].

In addition, the doping process in SNAP can provide much more control over the doping level due to the ease with which bulk Si can be doped [1]. In the SNAP process, a spin-on method is typically used to dope Si NWs. Transport data in SNAP Si NWs shows bulk-like conductivity characteristics [2]. Here, I study SNAP Si-NW systems as a spin transport channel.

5.1.2 Spin transport in Silicon: Hanle effect

After discovering giant-magnetoresistence effect (GMR) in 1988, the study of spintronics has been an emerging field in the fundamental study of materials and the application of next generation spin based electronics [10][11]. Spin based electronics use a spin signal to transport information; these spintronics devices have the potential to provide a high density of circuit integration and low-power dissipation.

Spin transport measurements have been conducted on many materials including: metals, semiconductors and graphene. One of the most important materials for future
spintronic devices is silicon. Silicon is expected to exhibit long spin lifetimes and diffusion lengths due to a relatively weak spin-orbit coupling and a low nuclear hyperfine interaction. Spin-orbit effects which cause spin relaxation are much smaller in Si than in GaAs owing to the lower atomic mass and the inversion symmetry of the crystal structure. The dominant naturally occurring isotope, $^{28}\text{Si}$, has no nuclear spin, suppressing hyperfine interaction. Consequently, spin lifetimes are expected to be long.

Spin lifetime can be measured using the Hanle effect. This effect is the modulation and suppression of the spin signal due to precession and dephasing in a transverse magnetic field [12]. The Hanle effect was described by using a drift-diffusion model [13][14]. Spins are electrically injected at a point $x_1$ at time $t = 0$ and diffuse towards a detector located at $x_2$. Figure 5.1 shows the schematic diagram for the spin transport behavior when a perpendicular magnetic field is applied to the channel. While they are diffusing, the electron spins relax at a rate $\tau_s^{-1}$ and precess about the applied field $\mathbf{B} = B\hat{z}$ at the Larmor frequency $\Omega = g\mu_B B/\hbar$, where $g$ is the electron $g$-factor, $\mu_B$ is the Bohr-magneton and $\hbar$ is the reduced Planck’s constant. The steady-state spin polarization at the detector is [15]

$$S(x_1, x_2, B) = S_0 \int_0^\infty \frac{1}{\sqrt{4\pi D t}} e^{-(x_2-x_1-v_{dt}t)^2/4Dt} \cos\left(\frac{g\mu_B Bt}{\hbar}\right) e^{-t/\tau_s} dt$$  \hspace{1cm} (5.1)

where $S_0$ is the spin injection rate and $D$ is the electron diffusion constant. The drift velocity, $v_{dt}$, is zero for purely diffusive transport. $S(x_1, x_2, B)$ is then integrated over the widths of the source and detector to obtain $S(B)$, which is proportional to the spin-dependent voltage. As a result, the second term $\cos(\Omega t)$ in Eq. (5.1) reflects the
oscillation of the spin signal with Lamor frequency (spin precess) and the last term \( \exp(-t/\tau_s) \) reflects the decay of spin signal (spin relaxation). Then the spin lifetime \( \tau_s \) is determined by the fitting the data to Eq. (5.1).

![Diagram of spin transport](image)

Fig. 5.1. Spin transport from injector \( (x_1) \) to detector \( (x_2) \) in perpendicular magnetic field. Spin precesses during the diffusion with Larmor frequency.

Hanle effect measurements in bulk Si channel were reported in literatures [16][17]. Erve et al. demonstrate the results of the fits to Eq. (5.1) and extracts the spin lifetimes in their systems, \( \tau_s = 0.9 \) ns for Fig. 5.2(a) [16] and Sasaki et al. show \( \tau_s = 9.21 \pm 0.23 \) ns for Fig. 5.2(b) [17].

![Graphs of Hanle measurements](image)

Fig. 5.2. (a) Hanle measurements at 10 K for positive and negative currents. The dashed lines are fits to Eq. (5.1) and reveals \( \tau_s = 0.9 \) ns [16]. (b) Hanle measurement at 25 K. The injection current is set at 1 mA. The solid lines are the results of the fits to Eq. (5.1) and reveals \( \tau_s = 9.21 \pm 0.23 \) ns [17].
5.1.3 Spin injection and detection: Spin-valve effect

Beyond exploring long spin lifetime media, spin injection and detection properties are important aspects in spintronics systems. A typical spin injection and detection measurement is the non-local measurements which detect pure spin signal from the channel. A non-local measurement minimizes some background effects by placing a spin detection electrode outside the path of the charge current. The geometry is shown in Fig. 5.3(a). Spin-polarized electrons are injected into the channel at contact 3 and flow towards contact 4 (red arrow) while the voltage, \( V_{1-2} \), is measured between contacts 1 and 2. Although electrons flow from contact 3 to contact 4, the non-equilibrium spin polarization in channel (blue arrows) diffuse in either direction from the source. The spin polarization \( P \) results in an electrochemical potential difference, \( \Delta \mu \), for the two spin states in the channel. This leads to a change in \( V_{1-2} \) when the magnetization of contact 2 is switched from the antiparallel to the parallel configuration with respect to contact 3. If contacts 1 and 4 are placed far from contacts 2 and 3, much further than spin diffusion length, then the chemical potential difference between spin up and down is almost zero so the magnetization of contact 1 and 4 does not affect the measurement. The spin-valve measurement is carried out by sweeping the magnetic field along the magnetic easy axis of FM electrodes and looking for a change in voltage over the field range in which contacts 2 and 3 become parallel or antiparallel configuration.
The plot in Fig. 5.3(a) is the chemical potential as a function of displacement in channel. Red curve is the chemical potential for spin-up and blue is the chemical potential for spin-down. If spin-up electrons are injected from contact 3, \( V_{1,2} \) measures the chemical potential difference in contact 1 and 2 from the red-curve, for parallel configuration, or from the blue curve, for antiparallel configuration. Figure 5.3(b) is the band structure for spin-up and spin-down electrons in magnetized FM electrode. FM material has different density of state (DOS) for spin-up and spin-down when it is magnetized. The spin polarization is defined as \( P = (n_\uparrow - n_\downarrow)/(n_\uparrow + n_\downarrow) \), where \( n_\uparrow \) and \( n_\downarrow \) are the total densities in each of the two spin bands. The corresponding electrochemical potential difference in the limit \( \Delta \mu \ll E_F \) is \( \Delta \mu = (n_\uparrow - n_\downarrow)/N(E_F) \), where \( N(E_F) \) is the DOS at the Fermi level in channel. The conditions for electrochemical equilibrium lead to a voltage difference [12]

\[
V_{\uparrow\downarrow} - V_{\uparrow\uparrow} = \frac{\eta P}{e} \Delta \mu
\]  (5.2)
5.1.4 Spin transport in 1D system

A. Kiselev et al. discussed spin transport properties in narrow 2D systems [18]. They revealed theoretically that, in case of narrow channel, the spin lifetime is inversely proportional to the channel width. They focused on the D’yakonov and Perel (DP) mechanism which is the spin scattering mechanism due to the lack of symmetry in crystal structure (for example zinc-blend semiconductors). In DP mechanism, the effective magnetic field $B_{\text{eff}}$ – induced by the spin splitting of the conduction band in the broken inversion symmetry – causes the electron spins to precess and thus relax. In 3D zinc-blende semiconductors, the orientation of the $B_{\text{eff}}$ is random with respect to the trajectory of the electrons. This results in spin precession along random directions and loss of spin coherence. In the 2D case, such as a quantum well, the spin Hamiltonian is expressed: $H = \eta \sigma \cdot [\mathbf{k} \times \hat{z}] \equiv \eta (\sigma_x k_y - \sigma_y k_x)$ where $\sigma$ is Pauli matrix and $\eta$ is the strength of spin splitting in the conduction band. Then $B_{\text{eff}}$ is in the plane of quantum well but still random because of the spread of $\mathbf{k}$ in the $x$-$y$ plane. This leads to similar spin relaxation as 3D case. However, if we look at the 1D case, where the axial direction of the NW defines a single axis direction, $B_{\text{eff}}$ is restricted to the direction of the axis. As a result, all spins precess along the same direction and the spin coherence is maintained much more.

A. Kiselev et al. derived the expression for average spin as [18],

$$\langle S_y \rangle \sim S_y^0 \exp \left( -\frac{1}{4} \frac{\eta_{\text{DP}}^2 L_p^2}{\tau_p} \frac{t}{\tau_p} \right)$$
where $\eta_{DP}$ is the strength of the spin splitting in DP mechanism, $L_p$ is the electron mean free path and $\tau_p$ is the momentum relaxation time.

In 2D case, $\eta_{DP}$ can be small ($\eta_{DP}L_p < 1$), so the spin relaxation equation follows

$$\tau_s^{2D} \sim \tau_p (\eta_{DP}L_p)^{-2} \quad (5.3)$$

where $\tau_s^{2D}$ defines the time of spin relaxation in 2D system. This behavior is valid until $\eta_{DP}L$ approaches one by from narrowing the width of the 2D channel ($L$). For smaller channel widths ($\eta_{DP}L < 1$), where the 2D channel is smaller than the mean free path $L_p$, the channel width $L$ acts as a new mean free path in the system substituting $\eta_{DP}L_p < 1$ in Eq. (5.3). DP spin relaxation is effectively suppressed as $\tau_s \sim \tau_s^{2D} (\eta_{DP}L)^{-2}$. This means that when the channel width in a 2D system is reduced to the order of electron mean free path, a much longer spin relaxation time is expected. Kieselv et al. shows a plot of the spin relaxation time as a function of channel width in Fig. 5.4, it shows that $\tau_s$ is proportional to $L^2$ when $L < 40L_p$. They estimated $\eta_{DP} = 9 \times 10^4 \text{ cm}^{-1}$ in the GaAs/AlGaAs quantum well with channel electron concentration of $10^{12} \text{ cm}^{-2}$, then $L_p = 5 \text{ nm}$. The samples with $L < 20L_p (= 100 \text{ nm})$ are readily available in the laboratories, and one can expect the increase of the spin lifetime in narrow channel.
Fig. 5.4. Log-log plot of spin relaxation time as a function of channel width [18].

5.1.5 Anisotropic magneto-resistance (AMR)

In spintronics studies, it is important to characterize the ferromagnetic (FM) electrodes. The anisotropic magneto-resistance (AMR) measurement reveals the coercive field characteristic of each FM electrode which is needed for spin injection and detection.

AMR gives resistance changes in a ferromagnetic electrode where the resistance depends on the relationship between the axis of current flow and the orientation of the magnetization [19]. This phenomenon was discovered by William Thomson in 1857 (called the “Orientation effect” at that time). In general, the electrical resistance is at its maximum when the axis of magnetization orientation and the current flow are parallel (or anti-parallel) and is at its minimum when the magnetization is orthogonal to the axis of current flow. The angular dependence of the resistivity for the AMR effect can be described by the following [19]:

$$\rho(\theta) = \rho_\perp + \delta \rho \cos^2(\theta)$$
where $\delta \rho$ is the resistivity difference when angle between current and magnetization is parallel and perpendicular, and $\rho_{\perp}$ is the resistivity in the case of perpendicular. The magnitude of this effect depends on the material and is usually expressed as a ratio of the resistance change. The AMR ratio is defined as the ratio of the change in resistance $\delta \rho$ and the average resistance. For FM metals and their alloys this value can be as large as a few percent. AMR is used to investigate magnetic properties (coercive fields in our system) of magnetic systems.
5.2 Superlattice nanowire pattern transfer

5.2.1 Introduction of SNAP Si NWs device

The SNAP process creates a Si NW array whose nanowires can be used as the spin transport channels shown in Fig. 5.5. Our device is adapted for non-local spin transport measurements. In order to perform a non-local spin transport measurements, we must examine several aspects in this system: i) Determine the doping level on Si channel ii) The two middle electrodes should have different coercive fields to perform the spin injection and detection functions iii) Find the optimum interface structure between channel and FM electrodes. This chapter focuses on the fabrication of a spin transport device and the preliminary measurements used to modify the device geometry.

Fig. 5.5. Diagram of SNAP Si NWs device for spin transport measurement.

5.2.2 Growth and etching test of superlattice template

The growth of a superlattice consisting of GaAs/Al$_x$Ga$_{(1-x)}$As is the first step in SNAP processing. The superlattice used here was grown in Prof. Steven Ringel’s group at the Ohio State University via molecular beam epitaxy (MBE) onto <100> GaAs substrate. The MBE growth rate is ~ 0.6 µm/hour, and the mole fractions, x, of
GaAs/Al\textsubscript{x}Ga\textsubscript{1-x}As layer during growth are 0.5, 0.7 and 0.87. Due to the selective etching of GaAs layer, the width of the SNAP NW is determined by the thickness of AlGaAs layer, while the separation between NWs becomes the thickness of GaAs layer. The MBE has sub-monolayer control over film thickness so, in principle, the SNAP technique is capable of fabricating NWs with atomic-level width and separation. However, in practice, SNAP NWs dimensions have been limited to 7 nm in width and 15 nm in pitch.

GaAs layers are etched selectively in a Citric-Acid, DI Water, and H\textsubscript{2}O\textsubscript{2} solution in the weight ratio of 4:4:1. The observed etch rate of GaAs is \textasciitilde1.5 nm/s, and the target depth is 30 nm, so the time used for etching was 20 seconds. Figure 5.6 shows the etched superlattice templates which have different aluminum compositions. Both templates have two sets of five alternating layers of GaAs/AlGaAs. The first set has layers of 10 nm widths while the second has widths of 20 nm. The etching solution slightly attacks the AlGaAs layers, giving the top of the ridges a round shape in templates with 50% Al composition, as in Fig. 5.6(a). However, the etching selectivity is improved in templates with 70% Al composition where the top of the AlGaAs layers become sharp, as in Fig. 5.6(b). Etching tests show clear (no residue) etching results for the 20 nm portion of array, while there is some residue (maybe extra Ga) on the 10 nm portion of array in 50% Al composition template.

The etching test for the 70% Al template shows better results than the 50% Al, so we worked with this Al composition for the superlattice template in SNAP processing. We also tested 87% Al composition template, but this showed a low etching rate of \textasciitilde0.2 nm/s and had residue remaining after etching.
Fig. 5.6. Selective etching (GaAs) test in Citric-acid:DI:H$_2$O$_2$ = 4:4:1 solution of superlattice templates grown in MBE system. (a) Al composition of AlGaAs layer is 50%, (b) Al composition of AlGaAs layer is 70%. Etch rate for both templates is $\sim$ 1.5 nm/s.

5.2.3 SNAP procedure

The SNAP process to transfer the NW patterns from the superlattice to the substrate is described in Fig. 5.7. This process was developed by Ke Li, a former graduate student in the Johnston-Halperin group. He focused on creating graphene-nanoribbons (GNR) using the SNAP process. In particular, he worked with exfoliated graphene on a SiO$_2$ substrate while I focus on to creating a Si NW array using a Silicon-on-insulator (SOI) wafer. The only difference between Ke Li’s and my work is the substrate materials, so I will not discuss the detailed process here. The detailed technical process is described in Ke Li’s master thesis [6].
Step (a) – (e) in Fig. 5.7 are well described in Ke Li’s master thesis for GNR fabrication, but he could not get good results due to the lack of a reliable anisotropic etching tool. In section 5.2.4, I discuss the anisotropic etching process used to create Si NWs array with a new etching tool.

5.2.4 Transfer SNAP NW pattern to Si

The final step of transferring SNAP nanowires to a Si substrate is an anisotropic dry etch. The user facility, NanotechWest laboratory, at The Ohio State University has a reactive ion etcher (RIE: Plasma Therm SLR770) which is used for high performance
anisotropic etching of the Si substrate. Pt NW arrays on the Si substrate are used as an etch mask in anisotropic RIE etching. RIE etching allows the successful transfer of the NW pattern to the substrate without an observable undercut, Fig. 5.7(f). To determine the optimal dry etching recipe, RIE etching tests were carried out on a SIMOX (separation by implantation of oxygen) SOI (silicon-on-insulator) wafer which consists of a 34 nm epilayer of intrinsic Si and 150 nm buried oxide layer on a 0.5 mm thick Si substrate (purchased from Simgui, Shanghai, China).

The Si epilayer is etched using a combination of CF$_4$ and Ar (at a ratio of 20 sccm/3 sccm) plasma at a power condition of $P_1 = 30$ W and $P_2 = 100$ W, where $P_1$ is the cathode RF power which controls the plasma ion energy and $P_2$ is the RF power of ICP (Inductively-coupled-plasma) which controls the plasma density. Figure 5.8 shows the thickness change of Si/SiO$_2$ layers as a function of etching time. The etch rate for Si is 18 nm/min and for SiO$_2$ is 37 nm/min. It may worthwhile to determine a recipe with improved etch selectivity, where the etch rate of Si is larger than that of SiO$_2$. Ellipsometry is used to measure the thickness of layers. An etching time of 2 minutes 40 seconds was used for our NW structures. These conditions proved to smooth sidewall with no observable undercutting.
Fig. 5.8. RIE etching test with SIMOX SOI wafer consisting of 34 nm of Si and 150 nm of SiO$_2$. Etch rate for Si is 18 nm/min and for SiO$_2$ is 37 nm/min.

After successfully imprinting the superlattice template onto the Si substrate, the Si is etched in using a RIE with the recipe described in the previously. Figure 5.9 shows SEM images before and after the RIE process. Figure 5.9(a) shows the Pt NW array after imprinting onto the Si substrate and (b) is a higher magnification of (a). The dark black is an area without Pt and gray is an area with Pt. The brightest areas (seen as white lines in (b)) represent the most conductive regions in the SEM images. This SEM image corresponds to the “L” shape of Pt nanowires from the 45° angle deposition step. Figure 5.9(c) is an image taken after the RIE etch which forms the Si NW array. The Pt is removed in an aqua-regia dip and epoxy is removed in N-Methyl-2-Pyrrolidone (NMP). Aqua-regia is a mixture of 60 mL of HCl and 20 mL of HNO$_3$. The etching time is 30 minutes at a temperature of 60°C. The epoxy is then removed in hot NMP at 100°C for ~20 minutes. For complete epoxy removal, the NWs are sonicated for 10 minutes while sitting in NMP.
Figure 5.9(d) is a tilted (30°) image of Fig. 5.9(c) which shows the vertical sidewalls of NWs without any undercut. The wiggling of sidewalls comes from the rough edge of the Pt NWs. An E-beam evaporator is used for the Pt deposition with a deposition rate of 0.2 Å/s. High quality Pt deposition without wiggling edge of Pt NWs can be expected with improved control over Pt deposition. The measured height of Si NW (RIE etching depth) is 45 nm, which is approximately 10 nm further in the SiO$_2$ layer.

Fig. 5.9. RIE etch of the Si substrate using the Pt NWs array as etching mask. (a) SEM image of Pt NWs array. (b) Higher magnification of (a). (c) SEM image of Si NW array after RIE etching and removing the Pt and Epoxy. (d) A tilted image of Si NW array which shows the sidewalls of NWs.

A Si NW array is successfully produced by using SNAP processing. As described above, SNAP is a ‘top-down’ technique making NW arrays by imprinting a template. By changing the substrate materials SNAP could be used to fabricate NW arrays of the new materials using similar anisotropic dry etching. Graphene is one of the most attractive
materials for this application because the graphene nanoribbon is an emerging system for electrical and spin transport study. SNAP processing for the fabrication of graphene nanoribbons was developed by Ke Li. In addition, I also have developed several processing steps, such as protecting the graphene against the wet acid-etching and a method of imprinting the template on chemical-vapor-deposition (CVD) grown graphene.

For nano-patterning on graphene, there are still several remaining challenges including the cleaning the sample surface without damaging graphene, protecting graphene against wet etching and transferring the pattern to the graphene. SNAP processing for fabricating graphene nanoribbon is mainly discussed in Ke Li’s Master degree thesis, thus I skip this topic in this thesis and will focus on the Si NW array system. Si NWs produced in SNAP processing now can be used to fabricate the FET type devices used to measure electrical transport properties; this will be discussed in the next section.
5.3 Fabrication of FET device with SNAP nanowires

5.3.1 Sectioning SNAP NWs array

After producing the Si NWs, there is a large rectangular Si pattern (2 mm × 0.5 mm) on the substrate which is the shape of template. One edge of the rectangular pattern includes Si NW array which extends over 2 mm in length. It is desirable to measure the electrical transport through a small number of nanowires, so a sectioning procedure is needed to define discreet sections of the Si NW array. One section of the NW array has 6–7 NWs and a length of 10–20 µm. To protect nanowires from etching process, Al is used as sectioning material. To pattern the Al mask, e-beam lithography, as described in Chapter 2, is used.

Pt alignment markers are deposited near the sectioning area and PMMA is spun onto the substrate. E-beam writing is conducted by aligning to Pt markers. Then Al is deposited over the written portions of the NW array using electron beam metal deposition. The thickness of the Al is 120 nm so that the 45 nm height of Si NWs is covered. Lift-off process in Acetone leaves several sectioned Al masks which are the shadow masks for the RIE etching process.

The Si NWs are protected from CF₄/Ar RIE etching (same recipe as previous RIE etching of Si) by the Al masks. The etching time is 2 minutes and 40 seconds to etch through any exposed Si. Finally the Al masks are removed in phosphoric acid solution, where the sample is dipped in phosphoric acid for 20 minutes at the temperature of 60 °C.
Figure 5.10 shows the one section of NWs array after sectioning process. One substrate produces 3 – 5 sections of NWs, and one of these is used for FET device fabrication.

![Image of NWs array after sectioning process]

Fig. 5.10. Si NWs after the sectioning process. Al mask for one section is 20 µm × 0.5 µm that generates an array of 6 – 7 NWs.

5.3.2 Device fabrication using E-beam lithography

After the sectioning process, isolated NW arrays are selected using the SEM to find the NW array which has a continuous set of NWs in a section. Then the contact electrodes are patterned using the e-beam lithography procedures as described in Chapter 2 and Appendix 1.

Figure 5.11(a) shows an optical image of a device after all processing steps: e-beam lithography with single layer resist, metal deposition and lift-off. There are 3 pairs of yellow dots at the center of image. Each pair represents two Pt alignment markers placed 30 µm away from a NW array. Only one set of markers is used to fabricate a device, the right set is selected for this device. The light-gray area at bottom-left of Fig. 5.11(a) is the area imprinted by the superlattice template.

The device has 4-contact electrodes on Si NW array for non-local spin transport measurement, Fig. 5.11(b). However there are total 6 electrical pads on the NWs because
the middle two contacts have extended electrodes on both ends. In addition, the two middle electrodes have different width for proposing different coercive fields of them.

These extended electrodes can provide the measurement of anisotropic magneto-resistance (AMR) signal. We need to know the coercive field of each electrode from AMR measurements because one of two electrodes becomes spin injector and the other becomes detector. After knowing the coercive fields, we can define the parallel and antiparallel configurations of the two ferromagnetic (FM) electrodes which is an important step to detect spin-valve signal.

Fig. 5.11. FET device with 4-contact electrodes on one SNAP Si NW array. (a) Optical image of device with 4 contacts where the middle two contacts have extended electrodes on both ends to measure AMR. (b) SEM image of NWs area which shows the contact between metal and NWs.

5.3.3 Comparison of metal thicknesses on SNAP NWs

The height of SNAP NWs is 50 nm and each NW has vertical sidewall. The anisotropc metal deposition in a sputter system can make a discontinuity of metal electrode over the NWs. This discontinuous channel causes an unreliable resistance variation in the electrode. A quick solution for this problem is to either over-deposit the
metal or deposit the metal at an angle during evaporation. However, the sputter system (equipped in NanotechWest Lab.) does not have the capability to deposit at an angle so we use thicker layer of metal to overcome this problem.

Permalloy (Ni/Fe = 80/20) is deposited in sputter system as a FM contact metal. A thickness of 200 nm is used to make continuous contact over NW height. In addition 50 nm Al is deposited on top of the Py as capping layer to prevent oxidization. Figure 5.12 shows a comparison between two metal depositions with different Py/Al thicknesses. In Fig. 5.12(a), the total thickness of metal is 130 nm (Py/Al = 100nm/30nm) which reveals a discontinuity of metal electrode over the NWs. In Fig. 5.12(b), the total thickness of the metal is 250 nm (Py/Al = 200nm/50nm). The continuous electrode over the NWs provides a reliable resistance of the electrode.

Fig. 5.12. A comparison of two different thicknesses in metal deposition. (a) Total thickness of metal is 130 nm (Py/Al = 100nm/30nm) and shows discontinuity of an electrode over the NWs. (b) Total thickness of metal is 250 nm (Py/Al = 200nm/50nm) showing a continuous electrode over the NWs.
5.4 Electrical measurements with SNAP NWs device

5.4.1 n-type doping on Si substrate

In order to prepare the Si substrate for electrical and spin transport measurements, it needs to be doped before SNAP processing. We use a diffusion doping method with a phosphorus-silica-film to make n-type doped Si substrate. Usually diffusion doping in Si gives better performance in NW conductivity than ion implantation [2]. Diffusion doping profile is obtained by exposing the Si surface to the dopant atoms which diffuse into Si at a high temperature. The high temperature creates vacancies in the crystal lattice and the impurity (dopant) atoms diffuse into the Si vacancies by hopping [20]. By controlling the temperature and time, the dopant profile within Si substrate can be well characterized.

The ion implantation method of doping Si damages the lattice so a subsequent thermal anneal is needed to restore the lattice. These lattice defects play a significant role in the electrical transport properties of the NW systems due to reduced channel size. The defect mediated transport properties of NWs were studied in previous chapters of this thesis. Because of this, doping via ion implantation is not appropriate method in nanoscale structures.

For spin-on doping of the Si substrate, a phosphorus-silica-film with a phosphorus ion concentration of $5 \times 10^{20} \text{ cm}^{-3}$ from Emulsitone Co. is diluted 10-fold in methanol. The dopant solution is then spun onto the SOI wafer at a speed of 4000 rpm for 30 seconds and baked at 100 °C for 10 minutes to remove any extra solvent. The wafer is next loaded into rapid thermal annealer (RTA) for diffusion doping at high temperature. Figure 5.13
is a plot of the doping concentration as a function of annealing temperature. The doping concentration corresponds to the resistivity of Si substrate found by a four-point measurement [21]. The average resistivity in 4-point probe is expressed as

$$\rho = \frac{\pi V}{\ln 2 I} = 4.523 \frac{V}{I}$$

where $I$ is applied current to outer two probes, $V$ is the measured voltage across inner two probes and $t$ is the thickness of channel. This simple formula above works for when $t$ is less than half of the probe spacing.

Recently in spin transport and accumulation experiments in bulk Si systems, the $n$-doping concentration was demonstrated to vary between $2 \times 10^{18} \text{ cm}^{-3}$ and $5 \times 10^{19} \text{ cm}^{-3}$ [16][17][22][23]. In our system, a doping level of $\sim 2 \times 10^{19} \text{ cm}^{-3}$ is selected for our SNAP Si NWs. To attain this value the diffusion doping is performed at $850 ^\circ \text{C}$ for a time of 10 minutes. This doping level is an average doping in 34 nm thickness of Si substrate.

![Doping concentration vs. annealing temperature](image)

Fig. 5.13. Doping concentration as a function of annealing temperature in the RTA. The annealing time for doping is 10 minutes.
5.4.2 I-V measurement on NWs

The field effect transistor (FET) type device is fabricated with four contacts on the SNAP Si NWs. The resistance of a 7 NW array is nearly 200 MΩ/µm which larger than the expected value of 100 kΩ. Comparison 2- and 4-probe measurements reveals contact resistance of ~10 MΩ.

Figure 5.14 shows I-V curves of three portions of a set of NWs which are divided by four contacts. The NW length of left and right portions is 3 µm, and for middle portion it is 1 µm. As expected from the nanowire length difference between middle and left (or right) portions, middle has the smallest resistance (190 MΩ). The resistance of NWs themselves is too high to perform spin injection and transport measurements. This high resistance problem in NWs can be solved by controlling the doping level and device fabrication process (we suspect that the NWs are contaminated by acid process).

![I-V curves for different portions of nanowire](image)

Fig. 5.14. 2-probe I-V curves for left (red), middle (green) and right (blue) portion of nanowire divided by 4 contacts.
5.4.3 Anisotropic magneto-resistance (AMR) measurements of FM electrodes

As discussed in the introductory section of this chapter, AMR measurement is the method to characterize the ferromagnetic (FM) electrodes used for spin injector and detector. Here, the coercive fields of two middle electrodes are determined by AMR measurements. These electrodes have high length-to-width aspect ratio so the magnetic domains in each electrode have high exchange energy. A specific value of the magnetic field is needed to flip the magnetization of one electrode from antiparallel to parallel with respect to the magnetic field. The magnetic field needed to achieve this flip is called the coercive field of the electrode. By comparing the different coercive fields of two electrodes, we can determine the parallel and antiparallel configurations of the spin injector and detector which are a key point for the spin valve measurement.

The two middle electrodes crossing SNAP NWs, seen in Fig. 5.11(b), are used for AMR measurement. Figure 5.15 shows the change in resistance as a function of the magnetic field applied parallel to the electrode axis. A constant current of 0.5 mA is applied across the left electrode (Fig. 5.15(a)) and the right electrode (Fig. 5.15(b)). The width of left electrode is 0.9 µm and 1.4 µm for right electrode. Because the exchange energy of magnetization in a narrower channel is higher than that of a wider channel, we expect that the left electrode has higher coercive field than the right one.
Fig. 5.15. AMR measurements of the two middle electrodes. (a) AMR of the left electrode (0.9 µm in width) shows 31 ± 0.6 Gauss of coercive field. (b) AMR of the right electrode (1.4 µm in width) shows 17 ± 3 Gauss of coercive field.

In Fig. 5.15(a), blue plot represents the resistance change while sweeping up through the magnetic field and red plot while sweeping down through the magnetic field. The conductance jumps occur at –31 Gauss and +32 Gauss, which is nearly symmetric. The coercive field is determined by finding where the direction of magnetization of the electrode is flipped from anti-parallel to parallel while sweeping through the magnetic field. This investigation reveals that the coercive field of left electrode is 31 ± 0.6 Gauss.

In Fig. 5.15(b), the AMR ratio is a bit smaller (0.092%) than that of Fig. 5.15(a) and the overall shapes of blue and red plots are not quite as symmetric. Because the electrode is wider (1.4 µm compared to 0.9 µm) its coercive field may be affected by the large extended electrode. The coercive field of the right electrode, 17 ± 3 Gauss, is a reasonable value and can be distinguished from the left electrode, 31 ± 0.6 Gauss.
5.4.4 Improvement in FET device fabrication

A recent paper on spin transport in bulk Si stated that the spin resistance-area product $R \cdot A$ for spin injection in their systems varies from $1200 \, \Omega \cdot \mu m^2$ to $6000 \, \Omega \cdot \mu m^2$ with $150 \times 100 \, \mu m^2$ contacts [24]. Our system, however, has $R \cdot A \sim 10^6 \, \Omega \cdot \mu m^2$ with $0.2 \times 4 \, \mu m^2$ contacts ($R$ is contact resistance). This value is nearly three orders of magnitude higher than that reported in Ref. [24]. In order to overcome this high $R \cdot A$ value, absolute value of the contact resistance should be reduced because it is difficult to reduce the contact area in our system. This contact resistance may come from the contamination on the surface of NWs.

In addition, to improve spin injection and detection efficiency, an oxide tunnel barrier can be inserted between the FM metal and semiconducting NWs. This extra insulating layer can resolve the conductance mismatch problems [17]. Because this oxide layer is usually thin, several nm scale, it needs the clean surface treatment before deposition to avoid any unexpected faults.

In order to resolve the contamination problem at the interface between metal/oxide barrier and NWs we introduce the alternative way for patterning metal layer in this section.

The current e-beam lithography using positive resist has drawbacks for the interface quality. PMMA is spun onto Si NWs substrate and is developed after e-beam writing. Even if an UV-O$_3$ cleaning is conducted, there is still unwanted residue on the surface of the NWs. Further cleaning procedure is limited to avoid damaging the e-beam patterns. In order to reduce contact resistance and solve contamination problems at the
interface between metal and NWs, new procedures have been developed recently. In particular, we attempt the e-beam lithography step after the metal deposition.

For this new process, a negative e-beam resist (SU-8 2000.1) is used. The metal deposition is performed before e-beam lithography, providing a clean interface between the metal and NWs. Spin-coating and developing negative resist are conducted only on top of metal layers which avoids the interface contamination. Metal layers are etched in diluted HCl where the negative e-beam resist becomes an etching mask.

The etching of metal layers is performed as a preliminary study. Because e-beam lithography processing happens after metal deposition, there are several important parameter changes.

i) The e-beam voltage is reduced to 5 – 8 kV. Since the e-beam is exposed on a metal surface, the reflected electron flux from metal surface is higher than before. Therefore reflected (secondary) electrons create a broad exposed area at the boundary of patterns. As a result, there are developing failures in the submicron scale. Figure 5.16(a) shows that the 0.5 µm gap between the middle two channels are not fully developed. This problem is solved by reducing the beam voltage from 10 kV to less than 8 kV.

ii) Since Su-8 2000.1 is designed to be deposited with a thickness of ~ 100 nm, it needs to be exposed to a lower dose of 10 µC/cm², compared to the higher dose of 50 ~ 200 µC/cm² used for the 300 nm thickness of 4% PMMA. Figure 5.16(b) shows well etched metal patterns with adjusted e-beam writing parameters, 8 kV and 10 µC/cm².
Fig. 5.16. Optical images of etched metal layers by using negative e-beam lithography. (a) 10 kV of beam voltage results in the over expose on 0.5 µm gap due to reflected electrons. (b) Successful metal etching at 8 kV of beam voltage. Both (a) and (b) have 10 µC/cm² of beam dose.

The metal layers consist of MgO/Fe/Al (= 2nm/10nm/20nm) which are grown in the molecular-beam-epitaxy (MBE) system of Prof. Roland Kawakami’s group at University of California at Riverside. MgO is a tunnel barrier to overcome conductance mismatch problem in order to increase the spin injection efficiency [17]. The conductance mismatch problem has been one of the most important issues in spin injection studies between ferromagnetic conductors and semiconducting channels. A tunnel junction or a Schottky barrier has been theoretically proposed as a solution for this problem [25][26]. Al is a capping layer to avoid oxidization of Fe. The etching of metal layers with 20-fold diluted HCl acid (HCl:DI-H₂O = 1:20) can introduce an undercut due to the isotropic wet etching, which could peel off the narrow metal channel (0.7 µm width). The etching time should be carefully controlled to avoid this. Finally resist on top of the metal must be removed for electrical wiring.

To remove resist layer after etching, N-methyl-2-pyrrolidone (NMP) is used as remover. Because of its good solvency properties, NMP is used to dissolve a wide range
of chemicals, especially polymers. However, baked SU-8 after exposure and development is a hard material to remove. SU-8 is epoxy based resist which shows a highly cross-linked structure after exposure. Therefore an aggressive removing procedure is performed which doesn’t damage the metal patterns. The sample is immersed into NMP overnight, and it is then sonicated for 10 minutes to remove resist completely. This etching test has been successfully conducted with negative e-beam patterns. This etching procedure will be applied to real SNAP Si NWs to fabricate a spin injection and detection device.
5.5 Reference


Appendix

A1: E-beam lithography for single nanowire device

For the electrical measurement of a single nanowire, we developed an e-beam lithography process for scanning electron microscope (SEM: FEI Helios-600). Here are the detailed descriptions of the processing will be discussed. For our sample fabrication with a single NW, the yield of successful nanowire devices can be more than 80 % (meaning successfully making four contacts to a 10 μm long NW) and the processing duration (From Pt markers deposition to the lift-off of the metal) is usually 2 days.

After selecting isolated single nanowire in SEM, Pt alignment markers are deposited around nanowire using a focused ion beam (FIB), as shown in Fig. A1(c). Figure A2(a) is a SEM image of Fig. A1(c) after the deposition of Pt alignment markers. These Pt markers are separated by 30 μm from nanowire (placed at the center of image). 950 PMMA A4 (MicroChem) is spun on the substrate at a rate of 1500 rpm for 80 seconds resulting in a 300 nm thick layer of PMMA, see Fig. A1(d). The e-beam writing process is performed using the FEI Helios-600. A 4-electrode pattern is exposed on the selected single nanowire after aligning the write field to the Pt-markers, see Fig. A1(e). The exposed PMMA layer is then developed in MIBK:IPA = 1:3 developer.
Subsequently, the sample is rinsed immediately in IPA for 1 minute. Bilayer (MMA/PMMA) e-beam patterning was also performed to generate undercut which helps control the lift-off process. However, in our pattern processing, there was no issue in the lift-off even with a single layer resist (PMMA) patterning. Therefore, only single layer resist (PMMA) is used for our e-beam processing.

![Processing flow for e-beam lithography with a single nanowire.](image)

**Fig. A1.** Processing flow for e-beam lithography with a single nanowire. (a) Sonicate as grown substrate in methanol, (b) Disperse nanowires onto SiO₂ substrate, (c) Deposit Pt alignment markers around selected nanowire, (d) Spin coat PMMA on the substrate, (e) E-beam writing electrode patterns while aligning to Pt markers.

For the e-beam writing process on a PMMA layer, a 4-step patterning procedure is used for precise and effective control of the patterning process.

The 1ˢᵗ step makes the smallest patterns, usually the electrodes which directly contact the nanowire. This step provides a nanoscale patterned edge and submicron scale alignment using a low current and dose (11 pA and 150 µC/cm²).
The 2\textsuperscript{nd} step is an intermediate step connecting the smallest pattern to the 3\textsuperscript{rd} (long and wide electrode) pattern. In this step the same e-beam parameters as 1\textsuperscript{st} step are used for accurate control of the writing.

The 3\textsuperscript{rd} step creates long and wide (400 µm × 20 µm) electrodes which connect steps to the final contact pads. In this step, a high current and dose are used because precise control of writing is not needed and this reduces a writing time. Medium levels of current and dose (86 pA and 200 µC/cm\textsuperscript{2}) are selected for a reasonable writing time (2 ~ 3 minutes).

The 4\textsuperscript{th} step makes the contact pads for electrical wiring. The size of a contact pad is 100 µm × 100 µm, and a high current and dose (690 pA and 300 µC/cm\textsuperscript{2}) is used. Each step is carried out using a different magnification (2500× – 80×). Offset values between different magnifications are calibrated and inserted into the nano-patterning software (NPGS). Figure A2(b) shows the optical image of e-beam patterned electrodes after developing the exposed PMMA layer.

Fig. A2. (a) SEM image of two Pt alignment markers. Distance between nanowire (placed at center) and alignment markers are 30 µm in which prevents nanowire contamination from Pt gas. (b) The optical image of developed e-beam patterns.
Table A1 is the summary of the e-beam writing parameters for a 4-step patterning procedure. Spacing is the parameter used to decide the separation between each beam spot in $x$ and $y$ axis. This should be correlated with beam size in order to attain a smooth edge. The beam size is called the Configuration Parameter in the NPGS software. Finally, the last column is the time it takes to write each layer.

<table>
<thead>
<tr>
<th>Layers</th>
<th>Magnification</th>
<th>Offset (µm)</th>
<th>Spacing (nm)</th>
<th>Beam size</th>
<th>Current (pA)</th>
<th>Voltage (kV)</th>
<th>Dose (µC/cm²)</th>
<th>Time (Sec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Layer1</td>
<td>2500x</td>
<td>0,0</td>
<td>20,20</td>
<td>-8</td>
<td>11</td>
<td>10</td>
<td>150</td>
<td>12</td>
</tr>
<tr>
<td>Layer2</td>
<td>600x</td>
<td>2.2,-2.9</td>
<td>20,20</td>
<td>-8</td>
<td>11</td>
<td>10</td>
<td>150</td>
<td>86</td>
</tr>
<tr>
<td>Layer3</td>
<td>100x</td>
<td>20,-21</td>
<td>100,100</td>
<td>-4</td>
<td>170</td>
<td>10</td>
<td>200</td>
<td>245</td>
</tr>
<tr>
<td>Layer4</td>
<td>80x</td>
<td>20,-20</td>
<td>200,200</td>
<td>-2</td>
<td>690</td>
<td>10</td>
<td>300</td>
<td>172</td>
</tr>
</tbody>
</table>

Table A1. E-beam writing parameters for a 4-step patterning in FEI Helios-600.
A2: Absence of Mott-VRH and disorder potential in conduction band

A theoretical study of ES-VRH in our system is performed by Prof. Igor S. Beloborodov at California State University at Northridge to aid in understanding the formation of disorder potential in conduction band.

We expect in highly disordered nanowires Coulomb interactions should dominate at low temperatures. Mott variable range hopping arises from non-interacting electrons in a random potential gives an exponent $m = 1/(d + 1)$ and equals $1/2$ in $d = 1$, whereas ES-VRH that arises in the classical limit from the combined role of disorder and Coulomb interactions also gives an exponent of $1/2$ independent of dimensionality. However we believe that the physics of these low dimensional wires is determined by the combined effects of correlations and disorder and therefore expect that ES-VRH, rather than Mott-VRH, dominates in our samples.

It is possible that the random distribution of charged traps give rise to a granular morphology in the conduction band. Indeed, in granular samples the role of the Coulomb interaction is strongly enhanced and thus Mott-VRH is difficult to observe. This can be understood as follows: in semiconductors, the Efros-Shklovskii law may turn to the Mott behavior with the increase of temperature. This happens when the typical electron energy $\varepsilon$ involved in a hopping process becomes larger than the width of the Coulomb gap $\Delta_c$, i.e., when it falls into the flat region of the density of states where Mott behavior is expected. To estimate the width of the Coulomb gap $\Delta_c$, one compares the ES expression for the density of states
\[ \nu(\Delta_c) \propto (\kappa / e^2)^d |\Delta_c|^{d-1}, \]  

(A.1)

with the bare density of states \( \nu_0 \) i.e., the DOS in the absences of the long-range part of the Coulomb interactions. Using the condition \( \nu(\Delta_c) \propto \nu_0 \), we obtain

\[ \Delta_c = \left( \frac{\nu_0 e^{2d}}{\kappa^d} \right)^{1/(d-1)}. \]  

(A.2)

Inserting the value for the bare DOS, \( \nu_0 = 1/E_c^{gd} \) (\( E_c \) is the charging energy for a single grain), into Eq. (A.2) we finally obtain

\[ \Delta_c \propto E_c. \]  

(A.3)

Eq. (A.3) means that there is no flat region in the density of ground states and, thus, the Mott regime is difficult to observe in granular wires. To conclude this section we present some estimates for the Coulomb gap \( \Delta_c \) and the charging energy \( E_c \).

The typical grain sizes in our nanowires are in the range \( 5 \text{ nm} < a < 20 \text{ nm} \). These grain sizes are justified by the facts that i) our samples are stable meaning that each nanowire has more than one grain in diameter, and ii) our data clearly show the variable range hopping behavior; this behavior may not hold for a nanowire with a single grain in diameter. Using these numbers for the charging energies of a single grain \( E_c = e^2 / \kappa a \) we obtain \( 10^2 \kappa K < E_c < 10^3 \kappa K \). The typical dielectric constant \( \kappa \) for our samples is \( 3 - 4 \) reflecting the fact that our samples are pure conductors. We would like to point out that the charging energy \( E_c \) is larger than the characteristic energy \( e^2 / \kappa r_{\text{hop}} \), scale related to the typical electron hopping distance \( r_{\text{hop}} \). This is a consequence of the fact that the typical
hoping distance $r_{hop}$ is several times larger than the characteristic size of a single grain $r_{hop} > a$. Physically this inequality means that an electron propagates through several grains in one hop. As discussed in Chapter 3 and 4, there are two parallel conduction channels: trap states and band carriers. Because of the disordered potential in conduction bands defined by localized electrons, these band carriers involve the ES-VRH transport at low temperature and low bias regimes.
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