Front End Circuit Module Designs for A Digitally Controlled Channelized SDR Receiver Architecture

DISSERTATION

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By

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ABSTRACT

With the rapid development of wireless communication systems and increasing wireless communication applications in human life, more and more new communication standards are proposed, which introduce additional frequency bands or modulation schemes. The growing number of wireless communication systems and the increasing demands for bandwidth necessitate the evolvable receiver hardware.

To meet this requirement, this work proposes a digitally controlled channelized Software Defined Radio (SDR) architecture which is compatible with most applications in 0.5-10.5 GHz frequency range. In the proposed SDR, the digitally controlled channelized front end divides the entire frequency into seven 1.6 GHz sub bands, and further channelization is realized using a digital filter bank structure so that the proposed SDR could deal with both ultra-wideband and narrow band signals. Link-Budget analysis is performed in the system design, and the detailed specifications for the front end signal processing blocks is provided. A system simulation is performed in ADS to verify the proposed SDR.
The circuit design considerations for the proposed SDR system is discussed. The major characteristics of the SDR front end are its ultra-wideband spectrum access, software programmability, and its ability for digitally controlled channelization. The circuit design discussion is focused on those aspects, and gives an idea of some possible design techniques or circuit structures which may be used for the proposed SDR system. Using those techniques, specific circuits are designed as examples, including an LNA with tunable output frequency, an active mixer design with extended IF bandwidth, as well as a quadrature coupler structure with ultra wideband operating frequency range. The simulated results for each circuit block are presented, and the proposed techniques are verified.

Key words: Software Defined Radio (SDR), Channelization, Ultra-Wideband (UWB), Link-Budget, Low Noise Amplifier (LNA), Mixer, Quadrature Coupler.
DEDICATION

To my family
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CHAPTER 1

INTRODUCTION

1.1 Wireless Communication Systems

Wireless communications enables information exchange and multimedia communication among peoples or devices from anywhere in the world. In recent decades, wireless communication has been growing rapidly, and now impacts most aspects of human life. Systems [1] such as the Mobile/Cellular Communication system, GPS Communications Systems, Bluetooth, and Wireless Local Area Networks (WLAN) have contributed to this impact. Since 2002, the Federal Communications Commission (FCC) has released the frequency range of 3.1-10.6 GHz, Ultra-Wideband (UWB) technologies have been developed quickly, and UWB communication system has become a most important composition for the Wireless Personal Area Networks (WPAN).

With the development of wireless communication systems, wireless communication standards are proposed and developed by different organizations, such as the Institute of Electrical and Electronics Engineers (IEEE), European Telecommunications Standards
Institute (ETSI), International Standards Organization (ISO), etc., and decided by national or international committees, such as the Telecommunications Industry Association (TIA). The purposes of the wireless communication standards include ensuring a robust and reliable wireless communication, and performing as a guide for system and circuit design. Another objective of wireless communication standards is to ensure the interoperability of different wireless communication applications. [2]

In wireless communication systems, the frequency allocation and modulation schemes are the two most important characteristics. Figure 1.1 shows the frequency chart of different wireless communication systems [1], including the Mobile/Cellular Communication systems (GSM, CDMA, and WCDMA), the GPS satellite communication system, the wireless personal networks (Bluetooth and WLAN), and the Ultra Wideband (UWB) communications systems.

Figure 1.1: Frequency Chart of Wireless Communication Systems
For the UWB communication systems, there are two standards based on different frequency channelization, the DS-UWB standards and the OFDM/MBOA standards, which are also displayed in Figure 1.1.

In addition to different frequency allocations and channel participations, wireless communication systems have also adopted a variety of modulation schemes. The modulation could be considered as a coding procedure of the exchanged information. After modulation, the signals is changed and incorporated to a high frequency carrier in order to ensure efficient transmission. The modulation can be processed in both the analog and digital domain. Analog modulations fall into one of the following three major types: Amplitude Modulation (AM), Frequency Modulation (FM) and Phase Modulation (PM). The digital modulation has more variations. Table 1.1 list the most often used digital modulation types as well as their applications [3].

<table>
<thead>
<tr>
<th>Digital Modulation Types</th>
<th>Selected Applications</th>
</tr>
</thead>
<tbody>
<tr>
<td>GMSK / MSK</td>
<td>GSM, CDPD</td>
</tr>
<tr>
<td>BPSK</td>
<td>GPS, WLAN</td>
</tr>
<tr>
<td>QPSK, π/4 DQPSK</td>
<td>CDMA, WCDMA, WiMax, UWB WPAN</td>
</tr>
<tr>
<td>OQPSK</td>
<td>CDMA</td>
</tr>
<tr>
<td>FSK, GFSK</td>
<td>Bluetooth, DECT, Paging</td>
</tr>
<tr>
<td>8PSK</td>
<td>Satellite, aircraft, broadband</td>
</tr>
<tr>
<td>16 QAM / 32 QAM / 64 QAM</td>
<td>WLAN, digital radio, Modems</td>
</tr>
</tbody>
</table>

Table 1.1: Selected Digital Modulation Types and Applications

The frequency spectrum and modulation schemes are defined in the standards so the interference between different applications can be minimized. Once the frequency
allocation and modulation scheme is determined, the signal path could be well defined and the wireless communication can be performed smoothly between the transmitters and receivers.

1.2 Objective of the Research

As wireless communication technology evolves, more and more standards would be proposed and put into markets for the ever growing applications. The frequency spectrum of wireless communication systems is expanding, and more modulation schemes will also be introduced. It is desirable to have a “super-intelligent” communication device, which could support most standards, or even has the ability to evolve along with the development of standards.

Software Defined Radio (SDR) introduces digital control to the traditional transceiver architectures and brings flexibility to the transceivers, which could be a preferable solution. Thanks to the development of the digital signal processor, digital modulators or demodulators could be adjustable and easily programmed in the digital domain for different modulation schemes. The real challenge is in the analog or RF front end design, which needs to deal with different requirements in the frequency spectrums.

The objective of the research is to try to find a possible solution for a SDR receiver front end, which could be compatible for most wireless communication applications illustrated in section 1.1. A suitable SDR candidate should be able to:

- Operate in the frequency range between 0.5 – 10 GHz
- Process both wideband signals and narrow band signals
• Share the front-end circuits to some extent and minimize the complexity

• Use plausible ADC speed

• Enable the frequency / bandwidth configurator in either a digitally controlled front end / or a digital domain signal processor.

The research will include both system architecture proposals and CMOS circuit design considerations. The system architecture is proposed, the plausibility of the proposed system architecture is analyzed, the circuit design methods are discussed, and circuit design examples are presented.

1.3 Dissertation Organization

The organization of the dissertation is as follows:

Chapter 1 introduces the application backgrounds and the motivation of the work.

Chapter 2 reviews the software defined radio (SDR) technology, as well as the current system realization methods. The advantages and disadvantages of each current system design are analyzed, and the design challenges are discussed.

Chapter 3 introduces the channelization technology and its application in the wireless communication receivers. Subband signal models and subband signal processing methods are also introduced in this chapter, and its applicability in a SDR system is analyzed.

Chapter 4 gives the proposed system architecture design. The channelized front end adopts the digital controlled channel selection to reduce redundancy. The baseband adopts the filter bank structure as a subband signal processing technology. The frequency
plan, system specifications, as well as the link-budget system analysis are included in the chapter. The chapter concludes with ideal system block simulations.

Beginning from Chapter 5, the dissertation is focused on circuit design considerations for some selected functional block. In chapter 5, the LNA design consideration is discussed. The frequency compatibility and the noise optimization of the LNA are addressed in the discussion. As an example, a digitally controlled frequency tunable LNA is designed, simulated, and presented in this chapter.

Chapter 6 discusses the mixer design considerations for the proposed SDR architecture. The idea of extending IF frequency bandwidth is proposed and the implementation technology is discussed. A UWB mixer with a 1.6 GHz IF bandwidth is designed, simulated, and presented as an example.

Chapter 7 looks into the quadrature signal generations in the receiver. Quadrature couplers are proposed to replace the traditional phase shifter architecture. In order to implement the quadrature coupler for the proposed UWB applications, a technology to extend the operating bandwidth of the quadrature coupler is proposed and analyzed. A design example of a wideband quadrature coupler is presented and simulated at the end of the chapter.

Chapter 8 provides a summary of the work and gives a conclusion.
Chapter 1 gave an overview of different frequency allocations and modulation schemes for various applications in wireless communication systems. As the wireless communication systems continue to evolve, more and more new standards will be introduced into the market, which may include new frequency bandwidths, modulation schemes, or carrier frequencies. In order to reduce the development cost for the expanding wireless communication systems, the concept of software defined radio was proposed. This chapter will introduce briefly the concept of software defined radio, its advantages, implementations, as well as the design challenges.

2.1 The Concept of SDR

The concept of Software Defined Radio (SDR) can be traced back to the 1980s [4]. The idea is to introduce digital control, or software configuration, to the traditional radio architecture, and to bring flexibility to the devices so they may be more easily adapt to various standards and modulation modes.
SDR has a flexible open-architecture receiver which makes the dynamic selection of parameters for individual modules possible due to its reconfigurable implementation [5]. The main goal in the software approach receiver design is to substitute the traditional hardware implemented components with software and thus incorporate flexibility into the receivers.

2.2 The Advantages of SDR Technology

Software defined radio is a promising technology and could be used in many civilian, commercial, and military radio applications, including Bluetooth, WLAN, GPS, Radar, WCDMA, and GPRS. The advantage of the SDR technology can be summarized below: [6-7]

- The flexibility and reprogrammable nature of the software enables the SDR receiver to operate in a multiservice environment without being constrained by particular standards. The system can easily upgrade through software modifications and can adopt new frequency channels or standards conveniently.

- By using software, the SDR receiver can collect a complex signal with both imaginary and real part in the digital domain, or digitize the signal with various sampling frequency, which makes it easier to adopt new modulation schemes, or to apply different coding systems.

- Since a SDR receiver usually adopts a wideband RF front end, the nonlinearity performance and the frequency dependent errors of conventional hardware
receivers can be easily corrected or calibrated, which enables the SDR receiver to achieve a higher degree of performance.

- Fourthly, since SDR receiver processes in a wider frequency range, collects and digitizes the signals in the software domain, the receiver gains the flexibility to monitor, evaluate and even test the signal. Thus the SDR receiver can achieve a better performance with regarding to the signal tracking, frequency hopping, and anti-interference applications.

- Lastly, the SDR platform provides an effective simulation environment in which the development of new communication standards can be performed and tested in software. In this way, SDR helps to reduce the component costs of extra hardware devices in the exploration of growing applications.

There are many other advantages of SDR technology which are too numerous to list. Since the SDR is able to perform multi-frequency and multi-mode operations in the expanding wireless communication systems and can be continuously updated to new frequency bands, modulation and application areas, the SDR technology has been and will continue to be an important topic in the design of next generation’s receivers.

### 2.3 The Ideal SDR Architecture

Figure 2.1 shows the ideal SDR architecture proposed by Joe Mitola [8]. In the ideal SDR receiver, the only analog component is the wideband A/D converter, which is supposed to capture all the signals from the entire frequency spectrum. The other signal processings, including the extraction, down conversion, and demodulation, are performed
in the digital domain using a software processor. The ideal SDR receiver is a super powerful receiver, which can receive and process the signals from every channel and for every application at the same time. The ideal SDR transmitter is similar, whose signal processing is performed in pure digital domain, and the only analog component is a wideband D/A converter.

![Figure 2.1: Ideal SDR Architecture](image)

Such an ideal SDR model is hard to realize due to the prohibitive cost of the ultra high speed ADC, super powerful DSP as well as the extremely large memory. Although people are trying to diminish the hardware part in the receivers, it is still not possible in present technologies [9]. Applicable SDR structures usually include certain analog front end to relax those harsh demands and to reduce the costs.
2.4 Applicable SDR Architectures

Applicable SDR architectures are categorized by their different front end structures. There are a lot of choices in the SDR receiver front end structures, including the digital-IF heterodyne structure, the direct conversion / zero IF structure, the digital low IF structure, the band-pass sampling structure, the direct RF sampling structure, and the six port network structure [9-18].

Among those candidates [10][11], the digital IF heterodyne structure can easily adapt itself to different requirements with a good sensitivity and selectivity; the direct conversion / zero IF structure diminishes the off chip high frequency band pass filters and guarantees a high level of integration; the digital low IF structure takes advantage of the digital signal processing to achieve a good integration with a reasonably low cost; the bandpass sampling and direct RF sampling structures use a series of decimation and filtering blocks so that the receivers may enjoy a good flexibility with an achievable ADC specification; the wideband six port network is a newly developed technology in the SDR design and has the advantages in wideband operation, low cost and simplicity.

The following parts in this section will further discuss the six candidates in detail.

2.4.1 The Digital IF Heterodyne Structure

Figure 2.2 shows the digital IF heterodyne structure [12]. Different from traditional heterodyne structure, after converting the received signal into the first IF (a few MHz), the front end does not further convert the signal into the baseband, but digitizes the signal
at the first IF. After this, further signal processing blocks, such as frequency down conversions and filters, are performed in the digital domain using FPGA or DSP.

Figure 2.2: Digital IF Heterodyne Structure

The advantage of the digital IF heterodyne structure is that the structure does not have the I/Q imbalance issues because the complex signal data is extracted in digital domain. By changing the frequency of the digital LO, the structure is easy to adapt to different channels within the first IF frequency range when keeping the same front end circuit. However, the drawback of the structure is the need for large external analog filters, which prevent it from high level integration.

2.4.2 The Direct Conversion / Zero IF Structure

Figure 2.3 shows the direct conversion / zero IF structure [13]. After a band pass filter and a LNA, the RF signal is converted directly into zero frequency (DC) by an I/Q
demodulator. Since the LO frequency is equal to the RF frequency, the direct conversion structure is also called zero IF structure.

The advantage of the direct conversion structure lies in its simplicity. Since the signal is directly converted to DC, a large number of IF passive filters and mixers can be avoided. The drawbacks of the direct conversion signal include the I/Q mismatch and flicker noise. Since the I/Q demodulator is operated in RF frequency, the structure is easily corrupted by I/Q mismatches. When digitizing in DC frequency, large flicker noise in the low frequency range may also increase the digitization errors.

![Figure 2.3: Direct Conversion / Zero IF Structure](image)

When tuning the LO frequency with the RF frequency, the direct conversion receiver can adapt to different frequencies easily. The RF frequency tuning range is only limited by the LO tuning capability. Ref [9] proposed a method of integrating the decimation filters in the I/Q signal path, which adds more flexibility to the structure. Now the direct conversion structure has become a popular candidate in today’s SDR or multi-band systems.
2.4.3 The Digital Low IF Structure

As shown in Figure 2.4, the digital low IF structure first converts the RF signal into a low IF signal, whose frequency is between the digital IF heterodyne and the direct conversion structures. Then, the signal is digitized at that frequency. In the digital domain, the signal is converted into baseband through a digital I/Q demodulator.

The advantages of the digital low IF structure include that it has the flexibility of the digital IF heterodyne structure, and, at the same time, has a higher level of integration due to its inheritance relationship with a direct conversion structure [14]. While at the same time, the I/Q mismatch and the flicker noise are compromised by the non-zero IF frequency. However, in this structure, a flexible antenna and RF pre-filters are still needed in the structure, and the ADC requirement is also a bit tough due to the non-zero IF frequency.

Figure 2.4: Digital Low IF structure
2.4.4 The Band Pass Sampling Structure

For a limited bandwidth signal, proper sampling can generate an image of the signal in the low frequency band, which contains all the information of the original signal. The band pass sampling structure [15] shown in Figure 2.5 takes advantage of this theorem. The structure first filters and amplifies the RF signal, down converts the signal into a middle IF frequency (hundreds of MHz), and then directly samples the IF signal and digitizes it in the discrete time domain.

![Figure 2.5: Band Pass Sampling Structure](image)

The advantage of the band pass sampling structure is that by first converting the signal into the discrete time domain, the ADC requirements are relaxed. A discrete time ADC with a reduced resolution at a lower speed is enough for the discrete signal. The disadvantage of the structure is that the filters preceding the sampling stage need a high...
selectivity performance, which made the design of the filters rather tough and the designed filters are hard to integrate.

2.4.5 The Direct RF Sampling Structure

The direct RF sampling structure uses the same idea of the band pass sampling structure but goes a little further. Figure 2.6 shows the architecture of a direct RF sampling structure [16]. Rather than first converting the signal into a lower frequency, the receiver directly samples the signal in RF right after the LNA. The sampled signal is down converted, down sampled, filtered, and amplified in the discrete analog domain, and then digitized at a much lower frequency.

![Figure 2.6: Direct RF Sampling Structure](image)

In the direct RF sampling architecture, most analog signal processing has been moved to the discrete time domain, thus the design complexity is highly reduced. The discrete
time domain signal processing could be more power efficient. It is easier to be implemented in reconfigurable environments, which is another advantage of the direct RF sampling structure.

2.4.6 The Six Port Network Structure

The six port technology was first used to measure the amplitude and phase of high frequency signals. Since it can obtain the frequency, phase and amplitude information of RF signals, it might also be a possible solution for the SDR application. Recently, there has been some research on six port networks being used as a direct demodulator in a SDR application [17].

![Six Port Network Receiver Structure](image)

Figure 2.7: Six Port Network Receiver Structure

Figure 2.7 shows the SDR structure using a six port network. Six port networks have six ports: one input port, one reference port, and four output ports. When connecting the input port to the RF signal and the reference port to a pre-defined VCO, the powers at the
four output ports contains the amplitude, frequency, and phase difference between the received RF signal and the referenced VCO. In this way, the modulation states can be determined and the demodulated signal can be obtained by simply analyzing the four output powers in a DSP.

The six port network SDR can achieve a desirable demodulation at a wideband frequency with a simple structure and a relatively low cost. Since the demodulation process is performed in DSP, it can achieve a high flexibility. Now six port technology has drawn much attention and could be one of the promising candidates for the SDR implementation in the future [11].

2.5 SDR Design Challenges

The previous section discussed the background and system realizations of SDR receivers. The main considerations in the SDR receivers include the power cost, integration level, flexibility, and configurability. The main challenges of the SDR receiver design are related to these considerations [19].

2.5.1 Flexible and Configurable Hardware Design

Flexibility and configurability are the main characteristics of SDR systems. Since the digital part of the SDR system is easily programmable in software with FPGA or microprocessor, the major challenge of the SDR design lies in the flexible or configurable design of the hardware part, including the RF filters, front end circuits, etc.
When reviewing the candidate SDR structures in section 2.4, one consideration is the applicability to flexible or tunable implementations. A flexible SDR design not only requires the selection of a proper architecture, but also requires reconfigurable designs of analog blocks in the selected front end, including the wideband or tunable LNA design, the frequency selectable mixers, the wide tuning local oscillators, the programmable filters, the reconfigurable ADCs, and so on. Finding a suitable way to implement those analog components requires innovations in the circuit design.

2.5.2 Real Time Digital Signal Processing in Software

The SDR receiver receives the microwave signals in a very large frequency range. After the front end processing, the received signals need to be demodulated and further processed in the digital domain. Thus a huge number of computations are included in the digital domain signal processing.

In wireless communication systems, the response time is important for a reliable connection. Real time signal processing is usually needed, which requires a sufficient speed in the ADC and software calculation. An optimized algorithm in both analog and digital signal path is necessary for the system to reduce the signal reception time, especially when the frequency channel or modulation scheme is changed.

In some cases, the optimization of the software algorithm is necessary but not enough. Processor architectures may also need to be optimized in order to speed up the calculation and to ensure the reliability. For example, parallel or pipeline microprocessor architectures could also be included in the SDR receiver design.
2.5.3 Power Consumption and Integration Level

The third challenge in the SDR implementation lies in the requirement of the power cost and the integration level, which is especially important for the portable wireless communication applications. In order to make the system suitable to different frequency bands while at the same time achieving a good signal property, the SDR hardware is usually more complex than traditional single application receivers. A lot of components should be added to adjust the frequencies, including multiple signal paths and different band pass filters, which increases the complexity of the system, leverages the power consumption, and even increases the sizes of the devices.

For this reason, power consumption and integration levels are critical in the system and circuit design of the SDR devices. Innovative ideals need to be proposed to minimize the power consumption for each individual circuit blocks, and the system architecture selection should also take the integration level into consideration. Maximum reuse of the circuit blocks is preferable in reducing the complexity of the system. To minimize the use of SAW filters can help to increase the integration level.
CHAPTER 3

THE CHANNELIZATION TECHNOLOGY AND SUBBAND SIGNAL PROCESSING THEORY

3.1 Channelization Technology

The word channelization originally refers to the technology of sharing communication median with different users, so that many conversations can be submitted simultaneously on a signal band, with each conversation being on a separate channel [20]. By this means, each channel is used to transfer different information simultaneously. The commonly known multiplexing methods including TDMA (time-division multiplexing), FDMA (frequency-division multiplexing), and CDMA (code-division multiplexing), belong to the channelization concepts.

In recent years, especially after the development of the UWB communication, the word channelization refers specifically to the frequency channel separation of a wide band. Signals are transferred in different channels of a pre-defined frequency band. In the UWB communication systems, the entire UWB frequency range is split into several bands, and
each band has many channels. Depending on different channelization methods, the UWB communication systems fall into two categories: the OFDM-UWB system and the DS-UWB system, which has been illustrated in Figure 1.1 of Chapter 1.

Originating from the same concept, channelization technology can be used in UWB receiver designs by splitting the desired receiving frequency band into several channels (or bands) and processing the signal in each channel respectively. After channelization, the bandwidth requirements of the RF front end circuit blocks can be relaxed, and the system complexity is reduced.

The following section will discuss in more detail the channelization technology, its application in UWB receiver design and SDR development.

3.1.1 Channelization Technology in UWB Applications

A receiver with channelization technology was first used in UWB applications. One of the primary challenges in the implementation of UWB communication systems is the bandwidth limitation of the analog circuits, especially the speed requirements of ADC. For example, to ensure a non-distortion reception, the signal should be digitized at least twice the highest frequency according to the Nyquist sampling theorem. However, the fastest ADC in current CMOS process technology can only operate at 1.5 GHz [21], which means that the signal should never exceed 0.75GHz. Even after frequency down conversion, the maximum complex signal bandwidth is only 1.5 GHz.

The channelization technology is used in the UWB systems to overcome the speed limitation of ADCs. Figure 3.1 shows an example of a frequency channelized UWB
receiver [22]. The receiver receives the signal in the 3.5 - 7.5 GHz UWB frequency range. The 4 GHz bandwidth signal is first split into four subbands, with each subband being only 1 GHz bandwidth. The subband signals are processed separately using separate mixers and filters. After down conversion to baseband, the highest frequency of each subband is only 500 MHz, and the subband signals can be easily digitized at 1 GHz speed. The digitized subband signals are combined in the digital domain and the original wideband signal is reconstructed in the DSP unit.

Figure 3.1: A Channelized Receiver Structure after [22]

In summary, the channelization method is an important technology in overcoming the ADC speed limits or circuit bandwidth limit in the ultra-wideband receivers. Even for the narrow band wireless communication systems, channelization technology is also helpful.
in improving the system reliability, since the oversampling ADCs can be used to increase the resolution of the digitized signals [23].

3.1.2 Channelization Technology for SDR Applications

In the previous section, the concept of channelization technology has been discussed and its application in UWB receivers was also presented. The channelization technology in the receiver design refers to the method of dividing the signals into multiple frequency channels, and processing each channel separately. After the sub-channel processing, the receiver could choose to either combine all channels to reconstruct the original wideband signal, or just extract the signal from one narrow channel. The SDR applications usually involve a wide frequency band and many channels, thus the channelization technology plays an important role in the SDR receiver design.

The main consideration in applying the channelization technology to the SDR receivers lies in its software realization, or digitally controlled channelization. In other words, the channel participations and selections should be configurable or programmable. This can be realized through three methods: the digitally controlled channel selection in the analog domain, the direct channel selection in the digital domain, and the combination of the previous two.

3.1.2.1 Analog Domain Channel Selection

Channel selection could be performed in the analog domain with a digital controller. The UWB channelized receiver presented in section 3.1.1 is an analog domain
channelization. When a digital controller is introduced, the analog front end can be reused, and the power consumption or system complexity can be reduced.

Figure 3.2: A Direct Conversion Receiver Front End with Digitally Controlled Channel Selection

The digitally controlled channel selective receiver is also referred to as a frequency tunable receiver [24]. Figure 3.2 shows the structure of a direct conversion receiver front end with digitally controlled channel selection. A uniform analog front end can be adjusted to different frequencies with different control bits. The digital controller generates the channel selection signal and tunes the analog front end to the desired operating frequency.

3.1.2.2 Digital Domain Channel Selection

Figure 3.3 shows a SDR receiver structure whose channel selection is performed in the digital domain [12]. The SDR receiver has a wideband front end, and the signals from all
the objective channels are digitized by a high speed ADC. In the receiver, the channel selections and I/Q demodulations are performed in the digital domain.

Figure 3.3: Receiver Architecture with Digital Domain Channel Selection

The advantage of the digital domain channel selection is that the signals in different channels may be extracted simultaneously, and the response time is shorter compared to the analog channelization especially when the frequency is hopping among different channels. However, the disadvantage lies in the relatively tough requirement of the RF front end bandwidth and the ADC speed limit.

3.1.2.3 A SDR Structure with Both Analog and Digital Domain Channelization

Combination of both analog and digital domain channel selections can improve the channel selection flexibility of the SDR and remain a relaxed front end requirement, which might be a preferable solution for the channelized SDR structure.
Figure 3.4 shows the structure illustration of a multi-band multi-channel SDR architecture using both the analog and digital domain channelization technology [25]. The analog domain channelization uses multiple signal paths with each path for a separate frequency band. After digitizing, the signals from different channels are routed through a switch matrix to one or more digital channelization units, where each unit could operate independently to extract the signal from each sub channel.

3.2 Subband Signal Processing Theory

Subband signal processing theory is one of the modern DSP topics. In the channelized SDR receiver, a good subband signal processing method can help reduce the calculation time and the power consumption. This section will introduce the basic DSP theories for
the subband signal processing, the filter bank structures, as well as its applications in the SDR receivers.

3.2.1 Frequency Domain Representation of Signals

When talking about the subband signal processing in DSP domain, it is necessary to first have a look at the frequency domain representation of signals. A signal can be represented in either time domain or frequency domain. In the time domain, the signal is a function of the time, denoted as $x(t)$. In the frequency domain, the spectrum of the signal is used to represent the signal, denoted as $X(f)$. For any continuous time signal, the time domain and frequency domain representations are equivalent and can convert to each other using either the Continuous Time Fourier Transform (CTFT) or its inverse transform.

Equations (3-1) and (3-2) shows the definition of CTFT and its inverse transform [26]. CTFT calculates the frequency spectrum of a continuous time domain signal; while its inverse transform gets the time domain signal from its frequency spectrum.

\[
X(j\Omega) = \int_{-\infty}^{\infty} x(t)e^{-j\Omega t} dt \tag{3-1}
\]

\[
x(t) = \frac{1}{2\pi} \int_{-\infty}^{\infty} X(j\Omega)e^{j\Omega t} d\Omega \tag{3-2}
\]

where $\Omega = 2\pi f$.

The digital signal processing is used in the discrete time domain. The continuous time domain signals can be sampled into the discrete time domain. The frequency
representation of the discrete time domain signals is obtained using Discrete Time Fourier Transform (DTFT), as defined in Equation (3-3). Equation (3-4) gives its inverse transform.

\[ X(e^{j\omega}) = \sum_{n=-\infty}^{\infty} x[n]e^{-j\omega n} \]  \hspace{1cm} (3-3)

\[ x[n] = \frac{1}{2\pi} \int_{-\pi}^{\pi} X(e^{j\omega})e^{j\omega n}d\omega \]  \hspace{1cm} (3-4)

When sampling the original continuous time signal at a time interval of \( T_s \), the relationship between the original continuous time signal and the sampled discrete time signal can be shown in Figure 3.5 [27].

---

**Figure 3.5: Relationship Between CTFT and DTFT**
The frequency spectrum of the sampled discrete time domain signal has a period of $2\pi$, which is corresponded to the sampling frequency $f_s = 1/T_s$. In Nyquist sampling, the original signal bandwidth is within one period of the DFT spectrum, thus no spectrum overlap would happen during the sampling, the original frequency information is maintained, and the original time domain signals can be reconstructed.

### 3.2.2 The Concept of Filter Bank in Subband Signal Processing

Subband signal processing is the method of first dividing a wideband signal into several subband and then reconstructing the original signal from the subband signals. Filter banks are usually included in the subband signal processing, for either extracting the subband signal, or reconstructing the original signal. This section will look at the concept of the filter bank subband signal processing [28][29] for both continuous time and discrete time signals. The frequency domain representations of the signals are used to illustrate the function of the filter banks.

Figure 3.6 shows the filter bank subband signal processing for continuous time signals. The frequency spectrums at each node in the signal path are also presented in the figure. There are two sets of band pass filters in the structure. The first set of filters is called analysis filter bank, which divides the original wideband signal $x(t)$ into $M$ subbands. After the analysis filter bank, the subband signals are processed separately and can be combined in the last step into a wideband signal $y(t)$. The second set of filters located before the signal combination block is called synthesis filter bank, whose objective is to make sure the signal in each subband will not corrupt the others in the combination
process. In this example, the frequency spectrum of the output signal $y(t)$ is exactly the same as the input signal $x(t)$, so the original input signal is perfectly reconstructed.

![A Simple Filter Bank Structure for Continuous Time Signal](image)

Figure 3.6: A Simple Filter Bank Structure for Continuous Time Signal

In real application, each subband signal is sampled into the discrete time domain after the analysis filter bank with a reduced sampling speed. The synthesis filter bank is a little complex because of the spectrum duplication in each $2\pi$ period.

Figure 3.7 shows the discrete time domain filter bank counterpart of the previous continuous time domain structure. The input signal is the same continuous time domain signal $x(t)$. The analysis filter bank divides the wideband signal into $M$ subbands. Nyquist sampling is performed immediately after the analysis filter bank. Due to the subband division, the sampling frequency can be reduced to only $1/M$ of the original signal bandwidth. The DFT spectrum of the sampled signal is displayed in the figure, and the subband spectrum has occupied the entire $2\pi$ period. In order to reconstruct the original spectrum, up-sampling is performed to squeeze the DFT spectrum, and the discrete time domain band pass filter is used to get rid of the unwanted frequency spectrums before the
final combination. The combined output discrete signal $y[n]$ has the same frequency spectrum shape as the input continuous signal $x(t)$ in a $2\pi$ period. Thus $y[n]$ is equivalent to the Nyquist sampling of the original wideband signal if time delay is neglected.

By moving the sampling stage up to the first stage, the analysis filter bank can also be implemented in the discrete time domain. Figure 3.8 shows the equivalent discrete time realization of the previous analysis filter bank. The DFT spectrum at each node of the analysis filter bank is illustrated, the synthesis filter bank is exactly the same as in the previous version, and the final output equals the original signal sample with some delays.
3.2.3 The Application of Filter Bank in SDR Receivers

The filter bank subband signal processing theory can be used in the channelized SDR receivers. Figure 3.9 shows a channelized receiver example [30] using the filter bank concept illustrated in the previous section. After a wideband LNA, the continuous time domain signal \( g(t) \) is first channelized into \( M \) subbands with an analysis filter bank \( H_k(j\Omega) \). Differing from the previous section, the analysis filter \( H_k(j\Omega) \) is composed of a down converted mixer followed by uniform low pass filters. From this modification, the complex RF frequency bandpass filters are avoided, and the subband signals are first transformed into baseband before being digitized. The ADCs in each subband path only need to operate at \( 1/M \) of the effective frequency \( f_{\text{eff}} \). The digitized subband signals are first up-sampled, processed through a digital domain synthesis filter bank \( F_k(z) \), and then combined to reconstruct the original wideband signal.

![Figure 3.9: A Channelized Receiver Structure using M-Channel Filter Banks after [30]](image-url)
CHAPTER 4

SYSTEM ARCHITECTURE DESIGN

The previous chapters have introduced the SDR backgrounds and summarized the previous research efforts in either SDR receivers or multi-band receivers. This chapter focuses on the system design of the proposed SDR receiver. The proposed system architecture is presented and the detailed system considerations such as the specification determination and link-budget analysis are also discussed in the chapter. In the end, the system simulations are performed using Agilent Advanced Design System (ADS) to illustrate the theoretical performance of the proposed architecture.

4.1 Proposed SDR Architecture

Figure 4.1 shows the proposed SDR architecture. The SDR architecture uses both analog and digital channelization. In the analog domain, the entire ultra-wideband frequency is divided into 20 subbands, with each subband 528 MHz bandwidth, which is exactly the bandwidth of an OFDM band. A digitally controlled front end is used to convert any selected band into low IF frequency. Then, the low IF signal is converted
into the digital domain. In the digital domain, the channelization technology is realized by a filter bank structure so the proposed SDR could extract an even narrower signal and could be applicable for narrowband communication systems.

The following parts will discuss in detail the proposed realization of channelized front end and digital filter banks.

**4.1.1 Front End Structure**

Figure 4.2 shows the front end structure for the proposed SDR. The front end is a dual down conversion structure which converts the desired RF signal into a 3 subbands group at the first step and then further converts the desired signal band into 0-528 MHz frequency range before digitizing.

There are two reasons that the dual down conversion structure is used in the proposed front end. Firstly, since the UWB OFDM standards divided the UWB frequency range into 14 subbands of 528 MHz bandwidth, and groups 3 or 2 subbands into different band
groups. The front end subband frequency setting makes the proposed SDR architecture be compatible with the OFDM standards. Especially when the OFDM frequency hopping is used, the dual down conversion structure can help reduce the acquisition time when the frequency hops between different subbands in the same band group. Secondly, since the first down conversion not directly converts the signal to low IF or DC, the dual down conversion structure can help minimize the effects of the DC interference or flicker noise.

Figure 4.2: Proposed SDR Front End Architecture

The first down conversion step uses the image rejection structure. Considering that the image and signal bands are exchangeable by different compensation methods, an LO frequency can be shared with two individual subbands. A switch between two 45 degrees
phase shifters is used to select the signal on the desired side of the LO and to reject the image on the other side.

The second down conversion step converts the desired signal into low IF frequency of 0-528 MHz frequency range. Since the spectrum in each 528 MHz is not necessarily symmetrical especially when narrow band wireless communication signals is involved, the DC direct conversion is avoided so that the two half spectrums should not overlap with each other.

<table>
<thead>
<tr>
<th>RF Frequency</th>
<th>OSC1</th>
<th>Signal/Image Selection</th>
<th>1st IF Frequency</th>
<th>OSC2</th>
<th>Applications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Min</td>
<td>Center</td>
<td>Max</td>
<td>Min</td>
<td>Center</td>
<td>Max</td>
</tr>
<tr>
<td>0.000</td>
<td>0.264</td>
<td>0.528</td>
<td>0.792</td>
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<td>1.848</td>
<td>2.112</td>
<td>2.375</td>
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<td>2.376</td>
<td>2.640</td>
<td>1.320</td>
<td>1.584</td>
<td>1.848</td>
</tr>
<tr>
<td>2.640</td>
<td>2.904</td>
<td>3.168</td>
<td>0.792</td>
<td>1.056</td>
<td>1.320</td>
</tr>
</tbody>
</table>

Table 4.1: Frequency Plan of the Proposed Architecture

Table 4.1 shows the subband division, the down conversion frequency plan, as well as the applications in each subband of the proposed front end. From this table, it can be seen
that the proposed architecture can operate at the entire frequency range as in Figure 1.1 from 0.4-10.6GHz. Only four oscillator frequencies are needed for the first down conversion: 2.628GHz, 3.960GHz, 7.128GHz and 8.712GHz. The first down conversion divides the entire band into seven subband groups and converts them into IF frequency of 0.7GHz to 2.4GHz. The second oscillator frequency is then selected from three values, 0.792GHz, 1.320GHz and 1.848GHz, and the baseband frequency range is from 0 to 528MHz.

4.1.2 Proposed Filter Bank Realization

The previous section has discussed the front end channelized structure from the antenna to the ADC. The ADC performs the sampling and digitalizing function. After the ADC, the digital discrete time signal is processed in DSP or FPGA.

Although the front end has channelized the signal into 528 MHz wide subbands, the digital channelization may still be necessary in order to deal with some even narrower bandwidth signals, such as GSM (which is 200 KHz bandwidth), Bluetooth (2 MHz), and so on. The discrete time filter bank discussed in Chapter 3 has the ability of analyzing each subband or synthesizing them into the original wide band, which could be used in the digital domain of the proposed SDR.

The proposed digital channelization adopts the filter bank structures, which is shown in Figure 4.1. The analysis filter bank divides the 528 MHz subbands into $M$ subchannels, and the synthesis filter bank can either select one subchannel to further process, or combine several subchannels and reconstruct a wide band signal for the next signal.
processing. While the synthesis filter bank is implemented in the digital domain, the analysis filter banks may be partly converted into the analog domain and the realizations might be different.

Current analysis filter bank in the multi-band receivers uses both the mixers and LPF structures in either analog or digital domain, as discussed previously in Figure 3.4 and Figure 3.9. This realization corresponds to the basic discrete time uniform modulated filter bank structure as shown on the left side of Figure 4.3 [28]. In the digital domain, the uniform low pass filter $H(z)$ is implemented using FIR (finite impulse response) filters. When using the property that the DFT has a $2\pi$ period, the digital uniform modulated filter bank structure can be implemented using its polyphase decomposition counterpart [31]. As shown on the right side of Figure 4.3, $P_k(z)$ is defined as the $k$th polyphase filter of original FIR filter $H(z)$ in the equation: $p_k[m]=h[mM+k]$, and $W_M$ is a $M\times M$ matrix defined as $W_M[l,n]=e^{-j2\pi ln/M}$. The detailed deduction procedures could be referred to [29].

Figure 4.3: Uniform Modulated Analysis Filter Bank Structure (left side), and its Polyphase Decomposition Realization (right side)
The filter bank realization of the proposed SDR is based on the polyphase filter bank structure, and there could be two realizations for it: either using one high speed ADC, or using multiple lower speed ADCs. The following parts will discuss in detail the two proposed realizations.

4.1.2.1 Filter Bank Realization with One High Speed ADC

Since the front end structure has already channelized the entire frequency and reduced the frequency bandwidth into around 528 MHz, it is possible to directly use a high speed ADC to sample and digitalize the signal, and the entire analysis filter bank could be realized in the digital domain, as shown in Figure 4.4. The sampling rate is twice the signal bandwidths, which is around 1GHz. The serial to parallel conversion block is transferred from the delay and down-sampling block in traditional polyphase filter banks.

![Figure 4.4: Filter Bank Realization with One High Speed ADC](image)

When $M = 8$, the proposed analysis filter bank separates the 528 MHz bandwidth into 8 sub bands, and each band is 66 MHz bandwidth. After the filter bank, each output
contains the information of the corresponding individual sub band. Cascaded filter bank structure may be used to further isolate the signal of a narrower channel.

4.1.2.2 Filter Bank Realization with Multiple ADCs

When the ADC speed is limited, or the digitizing resolution is important and the oversampling ADC is preferred, the serial to parallel conversion in the previous one high speed ADC realization could be converted into a multiple ADC structure as shown in Figure 4.5. The serial to parallel conversion is moved to the analog domain before the ADC by using sample and hold arrays, and the sampling rate of each ADC only needs to be $1/M$ of the previous ADC rate. However, the system CLK should still remain at around 1 GHz, so that the sampling pulse of the $M$ branches have an equal time interval.

![Figure 4.5: Filter Bank Realization with Multiple ADCs](image)

In conclusion, this section has discussed in detail the top level system architecture, especially the channelization implementation of the proposed SDR. In the following parts
of this chapter, the system parameters and block specifications will be defined and system simulation results will be presented to verify the designed architecture and specifications.

4.2 System Specification Determination

When the system architecture is determined, the detailed system specifications need to be designed for further circuit designs. This section presents the proposed system specification including the detailed design parameters for each circuit block.

4.2.1 System Performance Requirements

The proposed SDR is supposed to be compatible with most wireless communication in the operating frequency range shown in Figure 1.1 in chapter 1, or as listed in Table 4.1. For different applications, the desired system requirements are different due to different wireless communication standards, which defines the required system performance for each specific application, including the received signal power range, minimum SNR (signal noise ratio) or CNR (carrier noise ratio), sustainable intermodulation distortion (IMD) level, etc. The system specification parameters, such as noise figure (NF), receiver sensitivity ($P_{in, min}$), as well as nonlinearity performance ($IIP2$, and $IIP3$), can be obtained from those defined system performance requirements using the following equations [1].

$$P_{in, min} = -174dBm + CNR_{min} + NF + 10\log_{10} BW \quad (4-1)$$

$$IIP3 = IMD + \frac{IMD - IM3}{2} = \frac{3}{2} IMD - \frac{1}{2} \left( P_{in, min} - CNR_{min} + 3dB \right) \quad (4-2)$$

$$IIP2 = IMD + (IMD - IM2) = 2IMD - \left( P_{in, min} - CNR_{min} + 3dB \right) \quad (4-3)$$
Table 4.2 [32-33] summarizes the detailed wireless receiver performance requirements for different applications. The receiver specifications are calculated for each application using Equation (4-1) to (4-3), and are also listed in the table.

<table>
<thead>
<tr>
<th>Application</th>
<th>AMPS</th>
<th>GSM</th>
<th>CDMA (1995)</th>
<th>IS54 /IS136</th>
<th>WiMax</th>
<th>WCDMA</th>
<th>Bluetooth</th>
<th>UWB PAN</th>
<th>WLAN</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rx Frequency Spectrum</td>
<td>869 - 894 MHz</td>
<td>935 - 960 MHz</td>
<td>169 - 194 MHz</td>
<td>869 - 894 MHz</td>
<td>2.15-2.69 GHz, 3.41-4.2 GHz, 4.94-4.99 GHz, 5.15-5.85 GHz, 10-10.88 GHz</td>
<td>2170 MHz</td>
<td>2400 MHz</td>
<td>3.1 - 10.6 GHz</td>
<td>2400 - 2497 MHz</td>
</tr>
<tr>
<td>Modulation</td>
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<td>QPSK</td>
<td>π/4 QPSK</td>
<td>BPSK, QPSK, 1QAM, 6QAM</td>
<td>QPSK</td>
<td>GFSK</td>
<td>QPSK/PM</td>
<td>BPSK, QPSK, 1QAM, 6QAM</td>
</tr>
<tr>
<td>Data Rate</td>
<td>N/A</td>
<td>270.8kb/s</td>
<td>1.228Mbs</td>
<td>48kbs</td>
<td>75Mbs</td>
<td>3.84Mbs</td>
<td>1Mbs</td>
<td>224Mbs</td>
<td>54Mbs</td>
</tr>
<tr>
<td>Signal Bandwidth</td>
<td>30kHz</td>
<td>200kHz</td>
<td>1.23Mhz</td>
<td>30kHz</td>
<td>20MHz</td>
<td>5MHz</td>
<td>1MHz</td>
<td>500MHz</td>
<td>22MHz</td>
</tr>
<tr>
<td>Minimum Power (dBm)</td>
<td>-116</td>
<td>-102</td>
<td>-104</td>
<td>-110</td>
<td>-80</td>
<td>-107</td>
<td>-70</td>
<td>-79.3</td>
<td>-76</td>
</tr>
<tr>
<td>Maximum Power (dBm)</td>
<td>-20</td>
<td>-15</td>
<td>-25</td>
<td>-25</td>
<td>-30</td>
<td>-25</td>
<td>-20</td>
<td>-41</td>
<td>-10</td>
</tr>
<tr>
<td>CNRmin (dB)</td>
<td>3.5</td>
<td>8</td>
<td>-1</td>
<td>10</td>
<td>9</td>
<td>-7.5</td>
<td>13</td>
<td>-1</td>
<td>13</td>
</tr>
<tr>
<td>BER</td>
<td>N/A</td>
<td>1e-3</td>
<td>5e-3</td>
<td>1e-5</td>
<td>1e-6</td>
<td>1e-3</td>
<td>1e-5</td>
<td>1e-3</td>
<td></td>
</tr>
<tr>
<td>Receiver NF (dB)</td>
<td>9.7</td>
<td>10.9</td>
<td>10.93</td>
<td>9.23</td>
<td>7</td>
<td>7.5</td>
<td>29</td>
<td>7</td>
<td>9.6</td>
</tr>
<tr>
<td>IMD (dBm)</td>
<td>-51</td>
<td>-49</td>
<td>-43</td>
<td>-48</td>
<td>-35</td>
<td>-43</td>
<td>-36</td>
<td>-32</td>
<td>-35</td>
</tr>
<tr>
<td>IIP3 (dBm)</td>
<td>-18</td>
<td>-20</td>
<td>-14</td>
<td>-12</td>
<td>-9.5</td>
<td>-17</td>
<td>-14</td>
<td>-10.3</td>
<td>-9.5</td>
</tr>
<tr>
<td>IIP2 (dBm)</td>
<td>15</td>
<td>9</td>
<td>14</td>
<td>21</td>
<td>17</td>
<td>14</td>
<td>11</td>
<td>20</td>
<td>16</td>
</tr>
</tbody>
</table>

Table 4.2: Receiver Specifications Summary for Different Wireless Standards

Table 4.3: Desired System Specification
The proposed SDR should meet the most stringent requirements in the summarization to ensure an acceptable performance for all applications. Table 4.3 shows the desired system specifications for the proposed SDR summarized from Table 4.2.

4.2.2 Link-Budget Analysis

Link budget analysis is an efficient method to help determine the detail specifications of each block in the signal path of a receiver. Link budget analysis treats each block as a black box, simply adds or subtracts the gains or losses of each black box within the Rx signal path, and then calculates an estimated end-to-end system performance of the designed receiver architecture [1]. When compared with the required system performance, the achieved system performance can be adjusted by changing the specifications for each block.

According to the system specifications derived from the previous section, after several trials and calculations, the requirements for each circuit blocks are determined from the link-budget analysis. Table 4.4 shows the link-budget results with the specifications for each circuit block, and the detailed link-budget analysis is shown in Table 4.5.

<table>
<thead>
<tr>
<th>Stages</th>
<th>Gain</th>
<th>Noise Figure</th>
<th>Interference Rejection</th>
<th>IIP3</th>
<th>IIP2</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ant.</td>
<td>-1</td>
<td>1</td>
<td>0</td>
<td>30</td>
<td>60</td>
</tr>
<tr>
<td>LNA</td>
<td>10</td>
<td>2.5</td>
<td>0</td>
<td>5</td>
<td>25</td>
</tr>
<tr>
<td>BPF</td>
<td>15</td>
<td>3</td>
<td>15</td>
<td>5</td>
<td>40</td>
</tr>
<tr>
<td>IR Mixer</td>
<td>-3</td>
<td>5</td>
<td>0</td>
<td>5</td>
<td>40</td>
</tr>
<tr>
<td>Filter</td>
<td>8</td>
<td>6</td>
<td>15</td>
<td>5</td>
<td>40</td>
</tr>
<tr>
<td>IFA</td>
<td>17</td>
<td>6</td>
<td>15</td>
<td>5</td>
<td>40</td>
</tr>
<tr>
<td>IF BPF</td>
<td>-3</td>
<td>8</td>
<td>0</td>
<td>5</td>
<td>40</td>
</tr>
<tr>
<td>I/Q Mixer</td>
<td>17</td>
<td>8</td>
<td>0</td>
<td>5</td>
<td>40</td>
</tr>
<tr>
<td>Filter</td>
<td>30</td>
<td>8</td>
<td>0</td>
<td>5</td>
<td>40</td>
</tr>
<tr>
<td>BBA</td>
<td>35</td>
<td>14</td>
<td>0</td>
<td>10</td>
<td>50</td>
</tr>
<tr>
<td>ADC</td>
<td>0</td>
<td>10</td>
<td>0</td>
<td>27</td>
<td>50</td>
</tr>
</tbody>
</table>

Table 4.4: Circuit Block Specifications from Link-Budget Analysis
## Table 4.5: RF Front End Link Budget Analysis

<table>
<thead>
<tr>
<th>Stage</th>
<th>Antenna</th>
<th>UA</th>
<th>RF BPF</th>
<th>BB Mixer</th>
<th>IF BPF</th>
<th>IF BPF</th>
<th>IF BPF</th>
<th>12x IFB</th>
<th>Fiber</th>
<th>IF BPF</th>
<th>BB</th>
<th>Fiber</th>
<th>BBA</th>
<th>UDC</th>
</tr>
</thead>
<tbody>
<tr>
<td>High-Side Mode / Minimum Input Signal Level</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power Gain at the Receiver (dB)</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>-3.00</td>
<td>0.00</td>
<td>-3.00</td>
<td>0.00</td>
<td>-3.00</td>
<td>0.00</td>
<td>-3.00</td>
<td>0.08</td>
<td>-3.00</td>
<td>0.00</td>
<td>0.00</td>
</tr>
<tr>
<td>Insertion Loss at the Receiver (dB)</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
</tr>
<tr>
<td>Overall Power Gain at the Receiver (dB)</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
</tr>
<tr>
<td>Overall Insertion Loss at the Receiver (dB)</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
</tr>
<tr>
<td>Noise Temperature at the Receiver (K)</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
</tr>
<tr>
<td>Noise Figure at the Receiver (dB)</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
</tr>
<tr>
<td>Output Power of the Stage (mW)</td>
<td>116.00</td>
<td>116.00</td>
<td>116.00</td>
<td>116.00</td>
<td>116.00</td>
<td>116.00</td>
<td>116.00</td>
<td>116.00</td>
<td>116.00</td>
<td>116.00</td>
<td>116.00</td>
<td>116.00</td>
<td>116.00</td>
<td>116.00</td>
</tr>
<tr>
<td>Signal Power of the Stage (mW)</td>
<td>116.00</td>
<td>116.00</td>
<td>116.00</td>
<td>116.00</td>
<td>116.00</td>
<td>116.00</td>
<td>116.00</td>
<td>116.00</td>
<td>116.00</td>
<td>116.00</td>
<td>116.00</td>
<td>116.00</td>
<td>116.00</td>
<td>116.00</td>
</tr>
<tr>
<td>Signal Power of the Stage (dBm)</td>
<td>116.00</td>
<td>116.00</td>
<td>116.00</td>
<td>116.00</td>
<td>116.00</td>
<td>116.00</td>
<td>116.00</td>
<td>116.00</td>
<td>116.00</td>
<td>116.00</td>
<td>116.00</td>
<td>116.00</td>
<td>116.00</td>
<td>116.00</td>
</tr>
</tbody>
</table>

**Linear and Interference Factor Analysis**

- **Interference Factor at the Stage (mW):**
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00

- **Interference Factor at the Stage (dB):**
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00

- **IF of the Stage (nW):**
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00

- **IF of the Stage (mW):**
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00

- **Linear and Interference Factor Analysis after the Stage (mW):**
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00

- **Linear and Interference Factor Analysis after the Stage (dB):**
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00

- **Linear and Interference Factor Analysis after the Stage (nW):**
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00

- **Linear and Interference Factor Analysis after the Stage (mW):**
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00
  - 0.00

**System Requirements**
- Minimum Signal Power: -155 dBm
- ADC Dynamic Range: 92 dB

**Designed Specifications**
- Minimum Signal Power: -155 dBm
- ADC Dynamic Range: 92 dB
4.3 ADS System Simulation

Agilent Advanced Design System (ADS) provides a platform for the RF front end system simulations. Although the system simulation in ADS uses only pure theoretical mathematical models, it is still a useful tool to help analyze the system’s function with the existence of specific non-ideal performance. To further illustrate the proposed SDR architecture and the derived block specifications, and to show the functionality of the proposed front end architecture, the entire RF front end architecture is simulated in ADS for different wireless communication applications and different modulation schemes. The simulation procedure and simulated results are presented in this section.

Figure 4.6 shows the snapshot of front end architecture and the block settings from the ADS platform. All the front end blocks, including the LNA, Filter, mixer and OSC, and
all the test probes are mathematical models from the internal library provided by ADS. Figure 4.7, which only includes the front end blocks, is an illustration of the signal path from Figure 4.6. The block parameter settings are also displayed in Figure 4.7. The signal path and blocks settings are according to the results derived in previous sections. Only the most commonly considered non-ideal properties of each front end blocks are defined in the system simulation. For amplifiers and mixers, the Gain, NF (Noise Figure), TOI (Third Order Interception), and SOI (Second Order Interception) are considered. The first mixer, the image rejection property is considered and the image rejection is assumed as 15 dB, which is a quite loose requirement. For the Band Pass Filter, the pass band, the stop band, the A pass (pass band attenuation), the A stop (stop band attenuation) and the center frequency are considered. For the LO signal, the LO frequency is pre-defined from the input, and the phase noise parameters are set using the default parameters of the ADS model. For the Low Pass Filter (LPF), the pass frequency and the A pass are set.

For the frequency settings, the LO frequencies for the two step down conversions are set using two variables, LO1_Freq and LO2_Freq. According to the frequency plan discussed in section 4.1, LO1_Freq is selected from [2.376, 3.960, 7.128, 8.172] GHz, and LO2_Freq is selected from [0.792, 1.320, 1.848] GHz. The center frequencies of the two bandpass filters, the RF_BPF and the IF_BPF, are set using two other parameters, RF_center and IF_center. The RF_center and IF_center for the two BPF are selected from [0.792, 2.376, 3.960, 5.544, 7.128, 8.712, 10.296] GHz, and [1.056, 1.584, 2.112] GHz, respectively. The last block is an LPF with the stop frequency fixed at 528 MHz.
Figure 4.7: Front End Architecture and Block Settings in ADS Platform (Redrawn from Figure 4.6)
4.3.1 System Simulation Results for Different Applications

The ADS has provided system simulation testbenches for different applications in its RF Systems Design Guide. The ADS testbenches of communication examples have provided the signal modulation and demodulation blocks according to the signal definitions of different applications, thus the functionality of a proposed RF front end architecture is easier to be analyzed by simply substitute the designed RF front end into the testbench block. In this section, the front end architecture is simulated for several selected applications, and the simulated results are presented as follows.

4.3.1.1 System Simulation for Bluetooth

Figure 4.8 is a snapshot of the ADS simulation testbench for Bluetooth systems. The proposed RF front end architecture in Figure 4.6 is embedded in the symbol “DUT – My Design” in the “Receiver Co-Simulation Block”. Figure 4.10 shows the detailed illustration of Figure 4.8, the Receiver Co-Simulation Block in Figure 4.8 is consisted of the designed RF front end block and the envelop detector block. According to the Bluetooth standards, the signal frequency is 2.4 GHz, the data rate is to 1Mbs, and the baseband signal bandwidth is 1 MHz. In this simulation, the signal power is -70 dBm.

According to the frequency plan, RF_center is 2.4 GHz, LO1_Freq is 3.960 GHz, IF_center is 1.560 GHz, and LO2_Freq is 1.320 GHz. After the RF front end, the signal frequency is converted to 0.260 GHz at the output. The output frequency information is sent into the digital demodulator, and the demodulated signal is compared with the original signal.
Figure 4.8: ADS Testbench for Bluetooth System Simulation

Figure 4.9: Bluetooth System Simulation Results
Figure 4.10: ADS Testbench for Bluetooth System Simulation (Redrawn from Figure 4.8)
Figure 4.9 shows the simulation results of the system performance. The modulated signal spectrum is displayed and compared with the received spectrum. The time domain input and output demodulated data are also simulated and compared. The Bit Error Rate (BER) is calculated as $9.901 \times 10^{-23}$, the CNR ratio is 20.7 dB, with an over 7 dB margin compared to the Bluetooth standard.

4.3.1.2 System Simulation for GSM900

GSM900 is a commonly used standard in mobile/cellular application, and it operates at 900 MHz, with 200 KHz channel bandwidth. The communication examples have also the GSM receivers’ test bench. Figure 4.11 shows the ADS testbench for the GSM900 application.

![Figure 4.11: ADS Testbench for GSM900 System Simulation](image-url)
GSM Standards Parameters:
Tstep = 0.185185185 µs
Bit Time = 3.7037037 µs
Sequence Pattern = 8
Repeat: Yes

GSM SIGNAL GENERATION

DUT
My_Design

BB SIGNAL PROCESS

OUTPUT DATA

GSM SIGNAL GENERATION

INPUT DATA

INPUT SPECTRUM

OUTPUT SPECTRUM

Figure 4.12: ADS Testbench for GSM900 System Simulation (Redrawn from Figure 4.11)
Figure 4.12 shows the detailed illustration of the testbench including the frequency settings. Similar to the Bluetooth system schematic, the same designed front end is embedded in the symbol “DUT-My Design” in the testbench. The *GSM signal generation* blocks, preceding the front end architecture, as well as the BB signal processing block, after the front end architecture, are provided from the ADS library. In these two blocks, signal modulation and demodulation are modeled ideally and the system simulation only reflects the non-ideal performance defined in the RF front end architecture.

For the frequency setting, the frequency variables in the simulation are set as RF_Freq = 0.9 GHz, LO1_Freq = 2.376 GHz, IF_center = 1.476 GHz, and LO2_Freq = 1.320 GHz. The output frequency of the RF front end is 0.156 GHz, which is also defined in the BB signal process block. The input signal power is set as -102 dBm, which is the minimum signal power required from the GSM standard.

![GSM900 Simulation Results](image)

Figure 4.13: GSM900 Simulation Results
Figure 4.13 shows the simulation results of GSM900 system performance including the time domain input and output data sequence, as well as the input and output signal spectra. The decoded output data sequence follows well with the input data, and the signal is well demodulated.

4.3.2 System Simulation for Different Modulations

For wideband wireless communications, such as WLAN, WiMax, and UWB applications, QPSK, 16QAM, and 64 QAM modulation methods are used. The ADS also provides a system performance simulation testbench for different modulations with a pre-defined bandwidth.

Figure 4.14 shows the testbench for the system simulation on modulations. The proposed SDR architecture is presented in the symbol “My_design DUT”. Different modulation signal sources, including the QPSK, 16 QAM and 64 QAM modulation sources, can be obtained from the internal library of the ADS. In the front end modulation simulation testbench, the input of the receiver can be selected from either modulation signal source. In this example, the QPSK modulation source is selected. The signal carrier frequency (RF frequency) and the signal bandwidth can be edited as the properties in the modulation signal source block, and a modulation source signal is generated according to the requirements of frequency and bandwidth. The front end architecture receives the modulated signal and its output is connected to a terminal. Two test probes are placed separately at the input and output of the front end to monitor the original modulated signals and the received signals. The test probe measures the current and...
voltage at the test point. From the measured current and voltage, the power spectrum and
the constellation diagram can be calculated in the ADS testbench.

Figure 4.14: System Simulation Schematic for Different Modulation Types

To present the compatibility performance of the proposed front end at different
frequencies, two RF frequencies are simulated. One is 3.96 GHz, and the other is 5.016
GHz. For each frequency, three modulation types are simulated: QPSK modulation,
16QAM modulation, and 64QAM modulation. The signal bandwidth is set at 20 MHz,
which is comparable to the WiMax application. For each modulation type, the input and
output signal spectra and constellation diagrams are simulated, and the Error Vector
Magnitude (EVM) is calculated.

Figure 4.15 to Figure 4.17 shows the system performance simulation results on different
modulations when the RF frequency is 3.96 GHz, the signal bandwidth is set as 20 MHz,
and the signal power is set to be -80 dBm, which is the minimum power for WiMax
application. The other frequency settings for the front end system are LO1_Freq = 2.376
GHz, LO2_Freq = 1.320 GHz, and IF_Center = 1.584 GHz. The output frequency is 0.264 GHz. Figure 4.15 shows the QPSK modulation results, Figure 4.16 shows the 16QAM modulation results, and Figure 4.17 shows the 64QAM modulation results. From those simulated results, it can be seen that the proposed system can achieve an EVM of 4.13% for QPSK, 3.50% for 16QAM, and 4.54% for 64QAM modulations theoretically when modeled non-idealities in the front end architecture are considered. The EVM results for the front end signal chain only reflects that the designed front end architecture can meets with the requirements of the desired CNR for WiMax application. Further reduction of the system EVM performance can be achieved with proper calibration or equalization in digital domain.

Figure 4.15: System Simulation on QPSK Modulation: RF Freq = 3.96 GHz
Figure 4.16: System Simulation on 16QAM Modulation: RF Freq = 3.96 GHz

Figure 4.17: System Simulation on 64QAM Modulation: RF Freq = 3.96 GHz
Figure 4.18 to Figure 4.20 shows the system performance simulation results on different modulations when the RF frequency is 5.016 GHz. Similar to the previous one, the signal bandwidth is 20 MHz, and the signal power is set to be -80 dBm. The other frequency settings for the front end system are LO1_Freq = 3.960 GHz, LO2_Freq = 0.792 GHz, and IF_Center = 1.056 GHz. The output frequency is 0.264 GHz. The QPSK modulation results are shown in Figure 4.18, the 16QAM modulation results in Figure 4.19, and the 64QAM modulation results in Figure 4.20. From the simulation results, the proposed system can achieve an EVM of 4.32% for QPSK, 3.62% for 16QAM, and 4.60% for 64QAM modulations at the front end. The EVM results when RF is at 5.016 GHz are a little worse than the 3.96 GHz counterparts, which is as we expected. However, the degraded EVM results still meet the specification for the WiMax application.
Figure 4.19: System Simulation on 16QAM Modulation, RF Freq = 5.016 GHz

Figure 4.20: System Simulation on 64QAM Modulation, RF Freq = 5.016 GHz
4.3.3 Summary on the ADS System Simulation

The ADS RF system design guides provide a convenient method to evaluate the theoretical function of the proposed RF front end architecture using the designed parameters. As it was discussed in the beginning of this section, the RF blocks from the ADS internal library use mathematic defined models, which only include certain non-ideal effects from the limited selection options. Many other non-ideal effects are not considered in the previous discussed system simulation, or are hardly to be modeled in the ADS system models, such as the frequency-dependent gain variations, power reflection and leakage properties. Due to these reasons, the actual performance from the real front end may be worse than the simulated results. However, taking into consideration of some margins, the system simulation results are sufficient in reflecting the functionality and performance of the proposed RF front end.

From ADS system simulation results, it can be seen that the proposed front end works well in various applications and modulation schemes with sufficient margins. For example, in Bluetooth applications, the CNR has around 7 dB margin compared to the standard requirements, for the simulation on different modulation schemes, the EVM values are well below 5%, which is also above the requirements according to the CNR requirements of WiMax standards.

In conclusion, although the ADS system simulation only presents the theoretical performance of the proposed RF front end with the limited pre-defined non-ideal performance, the functionality of the proposed RF front end using the designed
parameters is evaluated thorough the simulation, and the proposed front end architecture can be used in the proposed SDR system.

4.4 SDR System Architecture Summary

In this chapter the SDR system architecture is proposed, the frequency plan of the proposed SDR is presented, the link-budget analysis is performed, and the detailed specifications for each circuit blocks are discussed. The channelization of the SDR architecture has been applied in both the analog domain and the digital domain, and the realizations are discussed in detail. The system simulations are performed using ADS platform. Different applications, RF frequencies, signal bandwidths, and modulation types are used in the system simulation, the system performance of the proposed front end architecture is illustrated in ADS simulation, and the feasibility of the proposed architecture is justified.

The system architecture simulations in the ADS environment use pure mathematic models for the front end circuit blocks, more accurate models can be obtained only after the front end circuits are implemented using specific CMOS technologies. The following chapters will focus on the design of those specific circuit blocks and present some design examples of the selected blocks in the proposed SDR. The circuit simulations performed using Cadence Spectre for each circuit design example will be presented and more non-ideal performance including the frequency-related performance will be observed from the detailed circuit simulation.
CHAPTER 5

LNA DESIGN

As the first signal processing stage in the receiver front ends, the low noise amplifier (LNA) amplifies the received signal with the requirement of minimizing noise contribution. The design specifications of LNAs include matching, noise figure, gain, linearity, power, etc. In the proposed SDR the LNA needs to receive a wideband input signal and also to be frequency tunable. This section will discuss the design considerations of LNA for the proposed SDR application, including the topology selection, input matching, noise analysis and optimization, and so on. Design examples will be presented. The main content of this chapter has been published in [34] - [35].

5.1 LNA Topology

This section will first introduce general structures and possible matching networks in the current LNA design, and then discuss in detail the cascoded source degeneration LNA topology. The cascoded source degeneration LNA topology will be selected as the LNA
core for the remaining chapter, and the design examples based on this topology will be introduced later in this chapter.

### 5.1.1 Different LNA Structures

Generally speaking, the CMOS LNA can be designed with either the common source or the common gate structures [36]. The common drain structure is not often used in the LNA design because its gain is less than unity. Both common source and common gate topologies have differential-ended or single-ended realizations. Figure 5.1 shows their single-ended structures.

![Figure 5.1: Basic LNA Structures: (a) Common Source Structure; (b) Common Gate Structure](image)

An important consideration in the LNA design is the input matching. For an efficient power transmission, it is desired for the LNA to match its input impedance to the source impedance of the transmission line or the antenna (usually 50 Ohms). For the common gate LNA, the input admittance is equal to the transconductance of the input transistor. If neglecting the frequency variation, no additional input matching network is needed to
achieve the desired input resistance as long as the bias of the input transistor is designed properly [37]. For the common source structure, the input impedance is the parasitic capacitance $C_{gs}$ of the input transistor, and an input matching network is needed.

$$R_{sh} = 50 \text{ Ohms}$$

![Figure 5.2](image_url)

Figure 5.2 : Input Matching for Common Source LNAs: (a) Matching with a direct shunt resistor; (b) Matching with resistive feedback; (c) Matching with source degeneration inductor

Depending on different input matching design methods, the common source LNAs have different realizations as shown in Figure 5.2 [38]. The direct shunt resistor matching directly uses a 50 Ohms shunt resistor at the input. The advantage of the direct shunt resistor matching is that it achieves a desired resistance in a wide frequency range theoretically when the parasitic capacitance of the MOSFET is neglected. However, the disadvantage is that the shunt resistor introduces a high resistive noise. The feedback resistive matching structure could lower the resistive noise current when using the miller effect to increase the resistance, but the isolation between the input and the output is degraded. The source degeneration structure is a frequently used matching method, and the desired resistive matching is realized with a source degeneration inductor as shown in
Equation (5-1). The advantages of the source degeneration structure include that no additional resistive noise is introduced ideally and the source degeneration inductor can also help to increase the linearity. The gate inductor in the structure is used to compensate the parasitic gate capacitor at the matching frequency $\omega$, as shown in Equation (5-2).

$$R = \frac{g_{ms} L_s}{C_{gr1}}$$  \hspace{1cm} (5-1)

$$\frac{1}{(L_g + L_s) C_{gr}} = \omega^2$$  \hspace{1cm} (5-2)

### 5.1.2 Cascoded LNA Topology with Source Degeneration

Figure 5.2 shows a cascoded LNA topology with source degenerated inductor. The cascoded structure is commonly used for LNA designs [39] since it has a better isolation and a reduced miller effect.

![Cascoded LNA Topology with Source Degeneration](image)

**Figure 5.3: A Cascoded LNA Topology with Source Degeneration**
The cascoded structure can be viewed as a common source stage followed by a common gate stage. Since the input stage is a common source structure, the input matching can be achieved in the same way as discussed in Figure 5.2. The cascoded LNA in Figure 5.3 uses the source degeneration matching network. With a source degeneration inductor and a gate inductor, the input impedance can be calculated using Equation (5-3).

\[
Z_{in} = \left( L_g + L_x \right) s + \frac{1}{\left( C_{gs} + C_x \right)s} + \frac{g_m L_x}{C_{gs} + C_x} \quad (5-3)
\]

In this topology, the additional capacitor \( C_x \), in parallel with the gate capacitor \( C_{gs} \), adds another degree of freedom to the LNA design, which can help to reduce the input transistor size and increase the input transconductance.

To achieve a good power matching, it is desired that \( Z_{in} = R_S \). The power matching conditions are listed in equation (5-4) and (5-5) as follows:

\[
\frac{g_m L_x}{C_{gs} + C_x} = R_S, \quad (5-4)
\]

\[
\frac{1}{\left( L_g + L_x \right)\left( C_{gs} + C_x \right)s} = \omega^2, \quad (5-5)
\]

where \( \omega \) is the designed matching frequency.

At the matching frequency, the gain of the cascoded LNA can be calculated as the product of the input transconductance and the output impedance. In the selected LNA architecture, the input transconductance is decreased by the source degeneration inductor; and the output impedance can be approximately simplified to the drain inductance.

Taking the matching condition into the consideration, the transducer gain of the LNA can
be calculated as in Equation (5-6). From the equation, it can be seen that the LNA gain is approximated to the rate of the drain and source inductors [40], which is another preferable property in the cascoded LNA design.

\[
Gain = -G_m Z_{out} = \frac{-s \times j \omega L_d}{1 + j \omega C_{gs} s + j \omega L_d s} \approx -\frac{L_d}{L_s}
\]  

(5-6)

5.2 Noise Consideration for the Cascoded Source Degenerated LNA

The previous section has discussed the cascoded LNA with source degeneration inductor as a design candidate for the proposed SDR. This section will further discuss the noise analysis and calculation of this topology, and a software based noise optimization method with a limited power consumption requirement will be introduced [34].

5.2.1 Noise Modeling and Calculation

The equivalent circuit for the noise analysis of the cascoded LNA topology is shown in Figure 5.4 [41]. Since the upper transistor (M2) has little effect on the overall noise behavior or on the input matching network, its noise contribution is neglected.
Three noise contributions are considered in this circuit: the source resistive noise, the channel noise, and the gate noise. The first noise contribution is the input thermal noise of the source resistance, which is defined as follows:

\[ \overline{V_{n,S}} = 4k_BT R_s \]  

(5-7)

where \( k_B \) is the Boltzmann’s constant.

The second noise contribution is the channel current thermal noise of the input transistor M1, which is defined as:

\[ \overline{I_{n,d}} = 4k_BT \cdot \gamma g_{d0} \]  

(5-8)

where \( g_{d0} \) is the drain source conductance and \( \gamma \) is the channel noise factor. For long channel transistors, \( \gamma \) is approximately 2/3; it can grow to 2 or 3 for short channel transistors [37].

The third noise contribution is the gate induced current noise of M1, which is correlated to \( I_{n,d} \) by a factor \( c \approx 0.395 \) and can be approximated as:

\[ \overline{I_{n,g}} = 4k_BT \cdot \delta g_g \]  

(5-9)

where \( g_g = \frac{\alpha^2 C_{gs}}{1 + \beta R_S} \) is the gate noise conductance, and \( \delta \) is the gate noise coefficient, which is approximately twice \( \gamma \).

When using the input referred noise model, the noise figure of the LNA is defined as:

\[ NF = \frac{SNR_{in}}{SNR_{out}} = \frac{4k_BT R_S \cdot \left( \overline{I_{n,d}^2} + \left( r_n + R_S \right) \right)}{\left( \overline{I_{n,d}^2} + \left( r_n + R_S \right) \right) \cdot \frac{1}{g_m} + \frac{4k_BT R_S}{4\pi g_c}} \]  

(5-10)
where the parameter $G_m$ is the effective transconductance of the amplifier.

After a tedious calculation, the noise figure can be obtained as in equation (5-11) [41]:

$$NF = 1 + \frac{\gamma g d_0}{g_m^2 R_s} \cdot \frac{\delta \alpha^2}{5\gamma} \cdot \omega^2 C^2 \left( R_S^2 + L_S^2 \omega^2 \right) + \frac{\gamma g d_0}{g_m} \omega^2 L_S C_{gs} \left( 2\alpha |\epsilon| \sqrt{\frac{\delta}{5\gamma} + \frac{C_{gs}}{C_x}} \right)$$ (5-11)

### 5.2.2 Noise Optimization Methods

For LNA design, the noise optimization should be considered in order to minimize the noise figure. Since the noise figure is mostly determined by the transistor size, finding out an optimum transistor size is a most important step in the noise optimization procedure. One traditional noise optimization method assumes that the optimum transistor width can be approximated using the following equation [37]:

$$W_{opt} = \left( \frac{1}{3\alpha \omega C_{ox}} \right) R_S$$ (5-12)

However, this approximation holds true only without the parallel capacitor $C_x$. Even in this situation, it is not always the optimum, especially when the power consumption limits or other design parameters are changed.

In the design procedure of an LNA, once the maximum power consumption or the current of the transistor is defined, the entire circuit can then be determined only by the transistor width from the previous power matching conditions, and the noise figure can be calculated. In other words, the noise figure is a function of only the maximum current and the transistor width. Thus, the optimum transistor width can be theoretically calculated from the maximum current requirement. Figure 5.5 shows a relationship between the
current and the optimum transistor width. It can be seen that the optimum transistor width can change dramatically especially at low power conditions.

Figure 5.5: The Relationship between Current and Optimum Transistor Width

Figure 5.6: Noise Figure as a Function of $W$ and $A$
Using an extra capacitor \( C_x \) in parallel with the gate capacitor \( C_{gs} \) is a commonly referenced noise optimization technology [42]. When the ratio \( A \) is defined as \( A = \frac{C_{gs}}{C_{gs} + C_x} \), the noise figure can be determined by the transistor width \( W \) and ratio \( A \) at any given current. Figure 5.6 shows the plotted noise figure as a function of transistor width \( W \) and \( A \) based on the above equations.

It may be misunderstood from Figure 5.6 that decreasing the ratio \( A \) or shrinking the width is a good method to improve the noise performance. However, this method may increase the values of inductance and decrease the transducer gain. Besides, when the noise contribution of the inductors is considered, this method may also degrade the noise performance. To achieve an accurate noise optimization method, it is necessary to first look at the noise performance of non-ideal inductance.

5.2.3 Improved Noise Modeling with Non-Ideal Inductors

When calculating the noise performance, traditional calculation assumes that the inductors are ideal and noiseless. However, when the inductors are integrated on the chip they are far from ideal and their noise contributions should not be neglected.

Figure 5.7 compares the noise figure simulation results of an LNA using ideal inductors with the noise figure simulation results of the LNA using real integrated inductors. It can be seen that the noise contributions of the real inductors can dramatically degrade the LNA’s noise performance. An improved noise model which takes into consideration the real inductors’ noise contribution is necessary for a good noise optimization.
Figure 5.7: Noise Figures with Real and Ideal Inductors

Figure 5.8: Noise Performance of a Single Inductor

Figure 5.8 shows the simulated noise of a single on chip inductor with different inductances and at different frequencies. It can be seen from the figure that at low frequencies, the noise contribution of a single inductor can be approximated by a linear function of its inductance as in equation (5-13).
\[ \overline{v}_{n,L}^2 = 4k_BT \cdot (h_L + h_0) \]  

(5-13)

Figure 5.9: Equivalent Circuit for on chip Spiral Inductor

On chip inductors are typically implemented as spiral inductors. Figure 5.9 is an equivalent circuit of an on chip spiral inductor [37], from which it can be seen that the previous approximation of equation (5-13) is reasonable. The first term \( (b_1 \text{ term}) \) of the estimation comes from the series resistance, which is proportional to the length of the inductor. The second term \( (b_0 \text{ term}) \) tends to be constant, since it is related to the implementation technology and the fixed connecting contacts. Figure 5.10 shows the relationship between the two noise factors \( (b_1 \text{ and } b_0) \) and the frequency.

When considering the effect of the matching inductors’ noise contribution in the LNA design, the input referred noise figure definition is still used, and the noise figure can be recalculated as in equation (5-14).
In the above equation, \( NF_0 \) represents the noise figure calculated from equation (5-11), \( \overline{I_{n,\text{out},g}}^2 \) and \( \overline{I_{n,\text{out},s}}^2 \) are the output noise current from the inductor \( L_g \) and \( L_s \), \( G_m \) is the effective transconductance from the input transistor, while \( G_{Lg} \) and \( G_{Ls} \) are the transconductance from the inductors. Further calculation reveals that \( G_{Lg} = G_{Ls} = G_m \) and the noise figure of equation (5-14) can be simplified as Equation (5-15), which is an improved modeling of the noise performance of the LNA.

\[
NF = NF_0 + \frac{\overline{I_{n,\text{out},g}}^2 + \overline{I_{n,\text{out},s}}^2}{4kTR_S} = NF_0 + \frac{h_1 \left( L_g + L_s \right)}{R_S} + h_0 \quad (5-15)
\]
5.2.4 Proposed Noise Optimization Method and A Design Example

Figure 5.11 shows the proposed LNA design procedure for the noise Optimization based on the above analysis. The capacitor ratio $A$ is initially set to be 1 in optimizing the transistor width. Then the ratio $A$ is optimized. A smaller on chip capacitor is also preferable when the area efficient is taken into consideration.

![Diagram of LNA Design Procedure with Noise Optimization]

The following part of this section gives a 2 GHz LNA design example using the proposed design procedure. The LNA is designed using the TSMC 0.18 μm technology. When the maximum current is set as 3 mA at a 3.3 V power supply, Figure 5.12 shows the result of the optimum transistor width estimation.

For a better implementation, the transistor width is chosen as 360μm. When using the equation (5-15) and substituting the values of $b_1, b_0$ at the working frequency as labeled in Figure 5.10, the optimum ratio $A$ can be estimated. Figure 5.13 shows the calculated...
results of the optimum ratio $A$, the calculated optimum noise figure with the inductors’ noise contribution is also labeled in the figure.

Figure 5.12: Transistor Width Estimation (μm) at the 3 mA current

Figure 5.13: Optimum Ratio $A$ Estimation when Width = 360 μm
Table 5.1 lists the calculated design parameters from the proposed noise optimization. Figure 5.14 shows the simulated result of the designed LNA, and Table 5.2 summarizes the simulated performance.

<table>
<thead>
<tr>
<th>Parameter / Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Working Frequency</td>
<td>2GHz</td>
</tr>
<tr>
<td>Maximum Current I</td>
<td>3mA</td>
</tr>
<tr>
<td>Transistor Width $W$</td>
<td>360μm (8μm *45 )</td>
</tr>
<tr>
<td>Transistor Length $L$</td>
<td>0.4μm</td>
</tr>
<tr>
<td>Capacitor Ratio $A$</td>
<td>0.70</td>
</tr>
<tr>
<td>Parallel Capacitor $C_x$</td>
<td>58.92 fF</td>
</tr>
<tr>
<td>Source Degradation Inductor $L_s$</td>
<td>1.3257 nH</td>
</tr>
<tr>
<td>Gate Matching Inductor $L_g$</td>
<td>7.7674 nH</td>
</tr>
<tr>
<td>Drain Inductor $L_d$</td>
<td>3.9761 nH</td>
</tr>
</tbody>
</table>

Table 5.1: Design Parameters
<table>
<thead>
<tr>
<th>Simulated Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Estimated Noise Figure with Ideal Inductors</td>
<td>1.4403dB</td>
</tr>
<tr>
<td>Simulated Noise Figure with Ideal Inductors</td>
<td>1.681dB</td>
</tr>
<tr>
<td>Estimated Noise Figure with real inductors</td>
<td>2.8256dB</td>
</tr>
<tr>
<td>Simulated Noise Figure with real inductors</td>
<td>3.186dB</td>
</tr>
<tr>
<td>Input Return Loss (S11)</td>
<td>-40.82dB</td>
</tr>
<tr>
<td>Output Return Loss (S22)</td>
<td>-26.86dB</td>
</tr>
<tr>
<td>Transducer Gain (S21)</td>
<td>11.68dB</td>
</tr>
</tbody>
</table>

Table 5.2: Simulated Performance

It can be seen from the simulated result that the designed LNA has achieved a perfect input matching (S11 less than -40 dB) at the designed frequency, and a transducer gain is about 11 dB. The simulated noise figure is a little higher than the estimated one because of the existence of the miller capacitor from the parasitic capacitor $C_{gd}$, especially when the transistor width or the ratio $A$ is decreased. The miller capacitor also affects the input matching, so the parallel capacitor $C_t$ may need to be changed accordingly in the real design.

5.2.5 Summary on Noise Consideration

In this section, the noise performance of the cascoded source degeneration LNA is analyzed, modeled, and calculated. The noise performance of the on-chip inductors is also investigated and modeled. A power-constrained noise optimization design procedure is proposed based on the analysis, and the process is verified through a 2 GHz LNA design example. The simulated result justifies the noise modeling and the proposed optimization methods. The proposed design procedure is easy to implement and can also be integrated in software automation. Further improvement of the noise modeling and optimization
method includes a thorough analysis on the influences of the miller capacitor. However, for most LNA design with only a small parallel capacitor, the proposed procedure is precise and good enough for the input matching network design with the target at an optimized noise performance.

5.3 UWB Realization and Frequency Tunable Design

The limitation of the source degeneration LNA is that the input matching is narrow band oriented, and the matching frequency is a single point restricted by the matching conditions. For UWB applications, the most challenging thing is to achieve all the design specifications for the entire ultra-wide frequency band. Although much research has been done and many LNA architectures have been proposed, none of them could meet all the requirements in the entire frequency range at the same time [43].

Figure 5.15: Proposed LNA Architecture

Figure 5.15 shows the top architecture of a LNA, which is composed of a wideband input matching network, a core amplifying stage, and an output matching network. For the input matching network, present reconfigurable LNAs either use switches at the input
matching network [44], or apply different amplifying cores for different frequencies [45]. However, the former implementation highly increases the noise figure by the triode mode MOS switches on the signal path, and the later implementation increases the area and cost.

Since in the cascoded structure, most noise contributions come from the input stage, a possible design technique is to extend the input frequency range and to use digitally controlled frequency tunable network at the output. The following parts of this section will discuss in more detail the specific design method [35].

5.3.1 Input Matching Frequency Range Extension Methods

![Figure 5.16: Input Matching Network with Bandwidth Extension](image)

(a) shows the circuit of the input matching network and the amplifying stage; (b) shows the equivalent Circuit of the input matching network.
Figure 5.16 shows the input matching with a bandwidth extension method for the discussed cascoded LNA. The equivalent circuit of the input matching is shown on the right side, and the input impedance can be expressed in Equation (5-16).

$$Z_m = \left[ j\omega C_m - \frac{1}{\omega C_m} \right] \left[ \frac{g_m}{C_p} + j\omega (L_s + L_a) - \frac{1}{\omega C_p} \right]^{-1}$$  \hspace{1cm} (5-16)

A closer look at the input equivalent circuit reveals that the input is a second order band pass filter structure with 50 Ohms at the input and output. Figure 5.17 shows a more general band pass passive filter structure. When $R_s = R_L = 50$ Ohms, the filter achieves a match from the input to the output in its pass band. The stage number of the filter equals the total number of the inductor and capacitor pairs. The higher the stage number is, the flatter the filter’s pass band is and the wider the pass band can be.

![Figure 5.17: A Generalized Structure of Band Pass Filter](image)

Since $R_L$ in the band filter structure is realized from the source degeneration inductor, and since its resistance is independent with the operational frequency, the input matching frequency range of the source degeneration LNA can be extended by simply designing a pass band filter with the pass band at the desired frequency range. Once the stage number is determined, the filter can be designed using the Look Up Table [46] according to the...
filter type selection, such as the maximum flat filter, equalripple filter, chebyshev filter, etc.

5.3.2 A Tunable Output Matching Network

The equivalent output impedance of a cascoded LNA with a load inductor is shown in Figure 5.18(a). The equivalent output circuit is a parallel circuit of the load inductor \( L_d \), the parasitic capacitor \( C_{gd} \), and the impedance \( Z_{out} \) looking down from the drain of transistor M2. Because of the cascoded connection, \( Z_{out} \) is quite large, as shown in equation (5-17).

\[
Z_{out} = (r_{o1} + r_{o2} + g_{m2}r_{o1}r_{o2}) + j\omega L_d (1 + g_{m2}r_{o2})(1 + g_{m1}r_{o2})
\]  

(5-17)

Figure 5.18: Output Matching Network for the Cascoded LNA: (a) Equivalent output impedance; (b) Reconfigurable output matching network using capacitor array

The purpose of the output matching network of the LNA is to transform the output impedance of the LNA to the desired impedance for optimum power transmission. A
shunt capacitor with a series inductor is usually used as the output matching network for the LNA. Since $Z_{out}$ has a large real part, a capacitor array can be used so that the output matching frequency can be tunable, as shown in Figure 5.18(b). The capacitor array is controlled by the digital switches so that different output frequency can be selected.

5.3.3 A 3-5 GHz Frequency Tunable LNA Design Example

Figure 5.19 shows the schematic of a design example of a 3-5 GHz LNA with the frequency tunable property. The LNA adopts the differential input differential output cascoded source degeneration topology. The differential architecture can help minimize the second order interference and improve the linearity.

![Overall LNA circuit](image)

Figure 5.19: Overall LNA circuit
The input matching network uses the bandwidth extension method discussed in section 5.3.1. Since the desired frequency range is from 3 to 5 GHz, a second order band pass filter is enough. To determine the passive components of the band pass filter, the equalripple filter type is selected and the passive components values are calculated.

The output matching of the LNA uses the frequency tunable structure as discussed in section 5.3.2. There are four switches in the capacitor array and all switches are controlled by the digital control signals. Table 5.3 shows the definition of the digital frequency selection control signals, the 3-5 GHz frequency range is divided into 3 sub-bands, and each sub-band has 3 mini-bands.

<table>
<thead>
<tr>
<th>Sub-Bands</th>
<th>Mini-Bands</th>
<th>Center frequency</th>
<th>Control Signals</th>
<th>Simulated Center Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>Subband1</td>
<td>Low</td>
<td>3.256 GHz</td>
<td>00</td>
<td>00 3.28GHz</td>
</tr>
<tr>
<td></td>
<td>Median</td>
<td>3.432 GHz</td>
<td>01</td>
<td>01 3.42GHz</td>
</tr>
<tr>
<td></td>
<td>High</td>
<td>3.608 GHz</td>
<td>10</td>
<td>10 3.64GHz</td>
</tr>
<tr>
<td>Subband1</td>
<td>Low</td>
<td>3.784 GHz</td>
<td>01</td>
<td>01 3.76GHz</td>
</tr>
<tr>
<td></td>
<td>Median</td>
<td>3.96 GHz</td>
<td>10</td>
<td>10 3.95GHz</td>
</tr>
<tr>
<td></td>
<td>High</td>
<td>4.136 GHz</td>
<td>10</td>
<td>10 4.12GHz</td>
</tr>
<tr>
<td>Subband1</td>
<td>Low</td>
<td>4.312 GHz</td>
<td>00</td>
<td>00 4.31GHz</td>
</tr>
<tr>
<td></td>
<td>Median</td>
<td>4.488 GHz</td>
<td>10</td>
<td>10 4.48GHz</td>
</tr>
<tr>
<td></td>
<td>High</td>
<td>4.664 GHz</td>
<td>10</td>
<td>10 4.63GHz</td>
</tr>
</tbody>
</table>

Table 5.3: Frequency Selection Control Signals
The entire LNA was implemented using the TSMC 0.18µm technology and the supply voltage is 3.3 Volts. The cadence simulation results of S11, S22, S21, and NF are shown in Figure 5.20. The output frequency selection network has little influence on S11 or NF but has an obvious influence on S22 and S21. From the simulation results of S22 and S21, the performance of the frequency selection is clearly displayed: the simulated center frequencies of the output matching are listed in Table 5.3 as a comparison with the desired frequency selection. The S22 in each operating bands are below -15 dB, and the S21 is about 8-12 dB.
5.4 LNA Design Summary

This chapter has discussed the LNA design considerations for the proposed SDR. Various LNA topologies are introduced in the beginning, and then the cascoded source degeneration LNA is selected as a candidate topology and discussed in detail. The noise analysis and optimization methods of the selected topology are discussed, and the input matching bandwidth extension technique is also presented. For the channelized SDR applications, a digitally controlled frequency tunable structure with capacitor arrays in the output matching network is presented, and a UWB frequency tunable LNA is designed as an example. The designed LNA has an operational frequency range of 3-5 GHz, and the capability of 9 mini-bands selection with a digitally control method. From the simulation result of the LNA design example, it can be seen that the digitally controlled frequency tunable LNA is possible and could be used as a candidate for the proposed channelized SDR.
CHAPTER 6

MIXER DESIGN

The mixer is another important design block in the receiver front end, and it performs
the frequency conversion function. In the receiver, the mixer converts down the RF signal
into IF, and its function can be modeled as a multiplier. The down conversion mixer has
two signal inputs: RF signal and LO signal. The output of the mixer is the IF signal,
whose frequency is the difference between the two input frequencies. This chapter will
address the design considerations of the down conversion mixer for the proposed SDR,
and a design example with simulated results will be presented. The mixer design example
has been published in [47].

6.1 Active and Passive Mixers

There are two types of mixer topologies, namely the passive mixer and the active mixer
[37], as shown in Figure 6.1. The passive mixer is actually a switch controlled by the LO
signal. The switch is turned on when the LO signal is above a certain voltage. The
mathematical model of a passive mixer is a multiplication of the RF signal with a square
wave. The fundamental frequency of the square wave is exactly the LO frequency. The passive mixers can enjoy high linearity but usually has either no gain or a negative gain.

Different from the passive mixers, the active mixers can achieve some higher conversion gain but usually has a worse linearity. The Gilbert cell is commonly used in the active mixer design. The Gilbert structure was proposed by Gilbert in the 1960s [48], and it was first used as an analog multiplier. The output of a Gilbert mixer is proportional to the product of RF and LO signals. Figure 6.1(b) shows a Gilbert double balanced mixer structure. The Gilbert mixer has a higher port to port isolation. Compared to the single balanced Gilbert cell, the double balanced Gilbert mixer is more desirable because of its second order harmonic suppression. Many ultra wide band mixer designs [49]-[51] use the double balanced Gilbert mixer structure.

Figure 6.1: Passive Mixer and Active Mixer
Both the active and passive mixers are important mixer candidates in the receiver design, the selection of the mixer topologies includes the tradeoff among gain, linearity, and other specification requirements such as the cost, area, isolation, and so on.

6.2 A Mixer Design Example for the Proposed SDR

From the SDR architecture and block specifications discussed in Chapter 4, the desired mixer needs a gain of 5-8 dB. Thus, the active Gilbert mixer should be used. This section will present a double balanced Gilbert mixer design example [47] which could be used for the proposed SDR structure.

6.2.1 Frequency Considerations for the SDR Mixer Design

For a down conversion mixer, the output IF frequency is the difference between the input radio frequency \( f_{RF} \) and the local oscillator frequency \( f_{LO} \), that is \( f_{IF}=|f_{LO}-f_{RF}| \). In most existing mixers, the IF signal frequency is fixed and the IF bandwidth is only a few hundred MHz at most. Thus, in UWB applications, the local oscillator (LO) frequency should be able to change in a large frequency range to follow the change of the RF frequency [49][50]. For example, in a 3.1-10.6 GHz adaptive or reconfigurable UWB communication system, a LO with 7.5 GHz tuning range is desired. However, there is no such LO which can provide such a wide tuning range with an acceptable phase noise performance at all frequencies in present technology. Even if there is a LO which can satisfy the requirements in the entire spectrum, the frequent change of the LO will dramatically slow down the operation of the communication systems. This limitation is
significant especially in the frequency hopping receivers where the acquisition and synchronization time is important [52].

For the objective SDR application, the entire frequency range is divided into several band groups and the signal in any given band group needs to be received at the same time. A mixer with an IF bandwidth covering the entire band group (approximately 1.6 GHz) can decrease the response time and will have promising applications, especially in the frequency hopping technology. However, there are few published mixers that support such a large IF bandwidth at the output.

A desired down conversion mixer for the proposed SDR should be operating in the frequency range of 3.1-10.6 GHz and with an extended IF frequency bandwidth of around 1.6 GHz. By extending the IF bandwidth, the LO frequency no longer needs to continuously and frequently follow the input RF frequency at the entire operating bandwidth but only needs to be selected from several fixed values, which makes it extremely suitable for the proposed SDR.

6.2.2 Proposed Mixer Design Example

Figure 6.2 shows the top architecture of the designed mixer. The proposed mixer uses a differential input and differential output structure. It is composed of an input matching network, an output network, as well as a Gilbert mixer core. The entire schematic of the proposed mixer is shown in Figure 6.3. The mixer’s three compositions in the top architecture have been illustrated in the circuit schematic already. The detailed design analysis for each part of the mixer is discussed in the following section.
6.2.2.1 Gilbert Mixer Core

The proposed mixer adopts the Gilbert cell structure. The transistors M1-M6 compose the double balanced Gilbert mixer core. Among those transistors, M1 and M2 work as the RF transducer stage which converts the input RF voltage into current. Transistors M3-M6
work as the LO switch stage. When the LO signal is large enough, the LO switch stage switches the RF current from one side to the other side of the differential output pairs, and the signal frequency is down converted. The conversion gain of the Gilbert mixer can be approximately calculated using Equation (6-1).

\[ A_v = \frac{2}{\pi} g_{m,2} R_L \]  (6-1)

where \( g_{m,2} \) is the trans-conductance of the transducer transistors M1 or M2, and \( R_L \) is the load impedance looking into the output, or in other words, looking at the drain of the LO switch transistors M3-M6.

Different from the traditional Gilbert mixer cells, the tail current source is eliminated in the proposed mixer so that the voltage to current transconductance could be more linear over a wide range by getting rid of the non-linear voltage drop at the tail current source [53]. Another advantage of removing the tail current source is to increase the signal swing and to make it more suitable for the low voltage application [54].

6.2.2.2 Input Matching Network

In the proposed SDR application, a BPF between the LNA and mixer is needed. The input impedance of the mixer is the load of the filter. To avoid large ripples caused by the mismatch between the filter and the mixer, which might affect the operation of the filter and deteriorate the performance of system, a wide band input matching network is necessary and should be added in the mixer.
Since the input transistor of the Gilbert mixer is also a common source structure, the ultra wideband input matching network design method discussed in Chapter 5 can still be used. In the proposed mixer schematic, the matching network is composed of a series capacitor and inductor pair, a parallel capacitor and inductor pair, a gate inductor, an input transducer transistor, as well as the source degeneration inductors. The source degeneration structure of the input transducer transistors is used here to generate the frequency independent resistance $R_0$, where $R_0$ can be calculated using Equation (6-2):

$$R_0 = \frac{g_{m,2} L_{n,2}}{C_{g_{n,2}}} \quad (6-2)$$

The equivalent circuit of the input matching network at either differential input ports can be redrawn as shown in the upper right corner of Figure 6.3, which forms a three stage band pass filter [49][51]. When using the equiripple band pass filter design [46] with an objective pass band of 3.1-10.6GHz, the inductance and capacitance in the filter can be determined. The input transistors’ sizes can be approximated from equation (6-3), and all the other parameters in the input matching network can be determined.

$$C_{g_{s}} \approx \frac{2}{3} W L C_{w} \quad (3)$$

### 6.2.2.3 Output Loads

The equivalent output load looking into the IF output ports is shown in the lower right corner of Figure 6.3, where the impedance $Z_{down}$ is the transistor impedance looking down from the drain of the switched transistors. Since there are two transistors in cascode connection, the impedance $Z_{down}$ is very large, thus the output impedance is dominated by
the passive components connected to the drain of the switches transistors, including the drain resistors $R_d$, the parallel inductor $L_d$, and the capacitor $C_d$.

In the circuit, the drain resistor $R_d$ is connected with a parallel inductor and capacitor pair. The parallel inductor and capacitor pair is used here as a simple one stage band stop filter. Since the band stop filter is connected in parallel with the resistor, the resistor is shorted when the parallel filter operates at its pass band. In this case, the conversion gain of the mixer is very low according to Equation (6-1). In other words, the mixer can achieve a positive gain only when the parallel filter operates in its stop band. When the band stop filter with a stop band around 0.7-2.5 GHz is carefully designed and the ripple at its stop band is minimized, the mixer can have an extended IF output bandwidth.

In the mixer circuit, there is another $R_d'$ $L_d'$ parallel circuit connected in series with the RLC network. It is used to compromise the decrease of the voltage gain at the two ends of the IF frequency range and to minimize the variation of the conversion gain in the IF pass band. Thus, the mixer can achieve an acceptably flat conversion gain through the entire 1.6 GHz IF bandwidth.

6.2.2.4 DC Bias Voltage Generation Circuit

The proposed mixer needs two DC bias voltages respectively for the RF and LO transistors. Figure 6.4 shows the bias circuit for the mixer. The bias circuit uses a traditional current mirror topology [38] and generates the two bias voltages in different branches. The transistors’ sizes in the bias circuits are proportional to their counterparts in the mixer core circuit. Thus the transistors in the bias circuit mimic the operating
conditions of the core transistors. For example, the currents in the LO switch transistors are only half of that in the output loads or RF transistors, thus the currents in $M_{BN.1}$ is twice the current in $M_{BN.3}$. The two input bias voltages VBP-H, VBP-L can be trimmed in order to optimize the bias position of the mixer.

![Bias Voltage Generation Circuit for the Mixer](Image)

Figure 6.4: Bias Voltage Generation Circuit for the Mixer

### 6.2.3 Simulated Results of the Proposed Mixer

The proposed mixer was implemented in IBM 0.13 μm CMOS technology, and simulated with RF Spectre in Cadence. The simulations are performed under a 1.6 V power supply voltage. The power consumption of the entire mixer including the bias circuit is about 30 mW.

Figure 6.5 shows the simulated input matching result of the designed mixer. From the figure, it can be seen that the RF input return loss is less than -10 dB in the entire operating frequency range from 3.1-10.6 GHz.
The mixer’s conversion gain is simulated with an input LO power of 5 dBm. Figure 6.6 shows the simulated voltage conversion gain versus the IF frequency. With the extended 1.6 GHz IF bandwidth, only 5 different LO frequencies are needed through the entire UWB RF frequency range, with each LO related to one band group.
When the RF signal frequency is in the first band group from 3.168-4.752 GHz and the LO frequency is 2.376 GHz, the voltage conversion gain can be above 12 dB in the entire IF range of 0.792-2.376 GHz, and can achieve as high as 15 dB at around 1.5 GHz.

Although the conversion gain decreases in the higher frequency band groups, the voltage conversion gain variation remains less than ±1.5 dB throughout the IF bandwidth in each band group. The gain in the higher band groups may also be boosted by trimming $R_d'$ and $L_d'$ at the outputs.

Figure 6.7 shows the simulated noise figure of the mixer in the five band groups. The noise figure in the entire operating frequency range is less than 13 dB and can be as low as 8.7 dB when RF is around 3.4 GHz (in this case, $IF$ is 1 GHz and $LO$ is 2.376 GHz).

![Figure 6.7: Noise Figure vs. IF Frequency](image)
The linearity performance of the mixer is also simulated with Cadence using the QPSS two tone test with the initial RF power of -50 dBm. The simulated IIP3 (input referred third order intercept point) of the mixer in the five band groups is shown in Figure 6.8 as a relationship with the IF signal frequency. The corresponding RF signal frequency is the sum of the IF and the LO frequencies. It can be seen that the IIP3 point of the mixer is above 4 dBm in the entire frequency range. As the RF frequency increases, the IIP3 can increase to above 10 dBm.

![Figure 6.8: IIP3 vs. IF Frequency](image)

### 6.2.4 Summary of the Proposed Mixer Design

This section presents a double balanced Gilbert cell down conversion mixer which could be used for the proposed SDR. The mixer employs an ultra-wideband input.
matching network which allows a RF frequency range from 3.1 GHz to 10.6 GHz. Band-
stop filters are used at the outputs to extend the IF bandwidth. With the extended
bandwidth, only 5 different LO signals are needed for the entire operating frequency
range, and each OFDM band group is converted into a fixed IF frequency range of 0.792-
2.376 GHz. The mixer is implemented in a 0.13 μm CMOS process and the simulated
results show that the proposed mixer achieved an input return loss better than -10dB
through the entire RF operating frequency range. Under a 1.6 V power supply and with a
5 dBm LO power, the voltage conversion gain can be as high as 12 dB in the first band
group. The gain variation is less than ±1.5 dB in each 1.6 GHz IF band. In the UWB
frequency range, the noise figure is 8-13 dB, the IIP3 is above 4 dBm and the power
consumption is about 30 mW.

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<td>5.3-8.2</td>
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Table 6.1: Comparison of Mixer Performance

Table 6.1 has summarized the performance of the proposed mixer, and compared it with
recently published ultra wideband mixers, it can be seen that the proposed mixer has
achieved a comparable performance as the other mixers with narrow IF bandwidth, and it is more suitable to the proposed SDR structure due to its extended IF bandwidth.

6.3 Mixer Design Summary

This chapter has discussed the mixer design considerations for the proposed SDR. The first down conversion mixer is investigated in this chapter since its requirement is different from current existing mixers, which only operate with narrow IF bandwidth. The second down conversion mixer is very similar to the current existing mixer designs, so the specific design consideration is not discussed here.

The mixer function can be realized using either the passive or the active structures. Since the first mixer needs a positive gain, an active Gilbert mixer structure is selected. The proposed mixer employs the differential balanced Gilbert structure to improve the second order non-linearity. Band-stop filters are used at the outputs to extend the IF bandwidth to around 1.6 GHz. With the extended bandwidth, the LO frequencies are fixed and the LO design specifications are relaxed. The mixer is implemented in a IBM 0.13 μm CMOS process and the simulated results show that the proposed mixer meets the expectation and that the design method can be used in the mixer design of the proposed SDR.
CHAPTER 7

QUADRATURE STRUCTURE DESIGN

The LNA and Mixer are the two most important circuit blocks in the signal path. After discussed the LNA and Mixer design, this chapter will turn to the quadrature structures implementation in the receivers. The quadrature structures are used in various function blocks of the receiver front end where the extraction of the complex signals is necessary, such as in the I/Q demodulator and in the image rejection block. Quadrature structures need quadrature input signals from either the processed RF signal or the oscillator. This chapter will focus on the generation of quadrature signals. A quadrature coupler is proposed for this generation, and a design example is presented in this chapter. The proposed quadrature coupler is published in [56].

7.1 Needs for Quadrature Structures

Most present receiver architectures include certain quadrature structures. One of the most important reasons of adopting the quadrature structures is in the consideration of the image interference. As discussed in Chapter 6, in the frequency down conversion, the
output IF signal frequency is the difference between the RF signal frequency and the LO frequency. The image signal, located at the other side of the LO, is symmetrical with the RF signal frequency, will fall into the same frequency as the IF signal after the frequency down conversion, and may corrupt the desired IF signal [38], as illustrated in Figure 7.1.

![Figure 7.1: Illustration of Image Interference](image)

One method to deal with the image problem is to use the quadrature structures. The quadrature structure is used to separate the In-phase (I) and Quadrature (Q) signals, so the image interference could be compromised after proper I/Q signal processing. Figure 7.2 (a) shows an image rejection block [38], the quadrature structures are used in the block to generate quadrature LO signals and combine the I/Q signals.

![Figure 7.2: Quadrature Structures in Receivers](image)
In addition to the image rejection block, the quadrature structure is also used in the I/Q demodulator [37], which is another function block in the receiver architecture, as shown in Figure 7.2(b).

7.2 Quadrature Signal Generation

The generation of quadrature signals is necessary for the quadrature structures. For the image rejection block or the I/Q demodulator, the quadrature signals could be generated from either the input signal (such as the RF signal or the IF signal), or the LO signal.

One method to generate quadrature signals is to use phase shifters to shift the original signal with either ±45 degrees or 90 degrees. The disadvantage of using phase shifter circuits is that active amplifiers are usually needed for the phase shifter, thus additional power consumption can be included. In addition, the active circuits may introduce more noise to the circuit. The non-linearity of the active amplifiers is another issue for this kind of generation, and the signal may be deteriorated by this non-linearity performance.

Another method is to use a quadrature directional coupler. The quadrature coupler splits the original input signal, and outputs two signals with 90° phase shift between each other.

![Block Diagram of a Quadrature Directional Coupler](image)

Figure 7.3: Block Diagram of a Quadrature Directional Coupler
Figure 7.3 is an illustration of a quadrature coupler, and there is a 90° phase shift between the *through* and *coupled* output. At the designed center frequency, the scattering parameter matrix of a quadrature coupler can be described as in equation (7-1).

\[
[S] = e^{i\theta} \begin{pmatrix}
0 & a & jb & 0 \\
jb & 0 & 0 & a \\
a & 0 & 0 & jb \\
0 & jb & a & 0
\end{pmatrix}
\] (7-1)

Because the quadrature couplers can be designed using passive components only, no additional power consumptions will be introduced in the system. It could be a preferable method in the quadrature signals generation. The following section will discuss in more detail the design considerations of quadrature couplers in the proposed SDR system.

### 7.3 Challenges of Quadrature Couplers Design in Wireless Systems

The traditional quadrature couplers are usually implemented with distributed techniques, such as microstrip lines and waveguides [57]. However, the main drawback of those distributed structures is their large physical area, especially for the frequency less than 20 GHz [58], which is exactly in the frequency spectrum range of the proposed SDR application.

To reduce the chip area and fabrication cost, quadrature couplers in today’s wireless communication systems are usually implemented with off-chip distributed techniques or lumped elements [59]. Although the chip areas are decreased due to the off chip components, the additional input/output interfaces always increase the loss and aggravate the mismatching issues.
State-of-the-art CMOS technology provides high performance passive components on a silicon substrate, and makes it possible for the quadrature couplers to be implemented with lumped elements in CMOS technology and to be integrated on the same chip with the other system components. Therefore, the lumped-element couplers have attracted research interests in recent years [60-62].

However, the existing CMOS lumped-element quadrature couplers, which are based on the narrow band and targeted at one specific frequency point, cannot satisfy the requirements of today's wide band applications. Many techniques were proposed to extend the operating frequency bandwidth of quadrature couplers, such as coupling two-section π-networks [62] [63]. However, the existing wide band couplers utilize too many inductors which occupy a large area in CMOS technology. Besides, having too many different passive components in those structures also creates a circuit that is very sensitive to CMOS process variations.

7.4 Proposed CMOS UWB Quadrature Coupler Design Example

To overcome the design challenges listed above, this section will present a quadrature coupler design example for the proposed SDR system, which can operate in a wide band frequency range, and suitable for CMOS integration. The designed center frequency of the quadrature coupler is 6 GHz, and the objective operating bandwidth should be extended to at least one band group, or 1.6 GHz.

In the proposed quadrature coupler, the operating bandwidth of the proposed structure is extended and the phase shift difference error is reduced by introducing two quasi
matching frequency points. The proposed coupler structure is first analyzed with the even-odd mode analysis method, and then is verified by Matlab calculation and post-layout simulation in Cadence Spectre.

### 7.4.1 Proposed Wideband Quadrature Directional Coupler Structure

Figure 7.4 shows the proposed wide band quadrature coupler structure, where $Z_1$ and $Z_2$ represent the impedance of the two different lumped element components, either inductors or capacitors. The circuit is a symmetrical network, and thus its scattering parameter matrix can be described as follows in equation (7-2):

$$
[S] = egin{pmatrix}
S_{\text{match}} & S_{\text{thru}} & S_{\text{coup}} & S_{\text{iso}} \\
S_{\text{thru}} & S_{\text{match}} & S_{\text{iso}} & S_{\text{coup}} \\
S_{\text{coup}} & S_{\text{iso}} & S_{\text{match}} & S_{\text{thru}} \\
S_{\text{iso}} & S_{\text{coup}} & S_{\text{thru}} & S_{\text{match}}
\end{pmatrix}
$$

(7-2)
where $S_{\text{match}}$, $S_{\text{thru}}$, $S_{\text{coup}}$, and $S_{\text{iso}}$ represent matching, through, coupling, and isolation parameters. Those four unknown parameters can be calculated with the conventional even- and odd- mode analysis [46].

![Figure 7.5: Half Circuit for (a) Even Mode, and (b) Odd Mode, Analysis](image)

This coupler structure in Figure 7.4 is symmetrical and any port can be used as the input port. In this analysis, port 1 is chosen as the input port. Figure 7.5 gives the half circuit for the even- and odd- mode analysis. According to the circuits shown in Figure 7.5, the ABCD parameters matrix of the even- and odd- mode half circuits can be derived and they are:
\[
\begin{bmatrix}
A & B \\
C & D
\end{bmatrix}_{\text{even}} = \begin{bmatrix}
1 + 4 \frac{Z_1}{Z_2} + 2 \frac{Z_1^2}{Z_2^2} & 2Z_1 \left( 2 + 3 \frac{Z_1}{Z_2} + \frac{Z_1^2}{Z_2^2} \right) \\
2 + 2 \frac{Z_1}{Z_2} & 1 + 4 \frac{Z_1}{Z_2} + 2 \frac{Z_1^2}{Z_2^2}
\end{bmatrix}, \quad (7-3)
\]

\[
\begin{bmatrix}
A & B \\
C & D
\end{bmatrix}_{\text{odd}} = \begin{bmatrix}
11 + 17 \frac{Z_1}{Z_2} + 6 \frac{Z_1^2}{Z_2^2} & Z_1 \left( 8 + 10 \frac{Z_1}{Z_2} + 3 \frac{Z_1^2}{Z_2^2} \right) \\
15 + 28 \frac{Z_1}{Z_2} + 12 \frac{Z_1^2}{Z_2^2} & 11 + 17 \frac{Z_1}{Z_2} + 6 \frac{Z_1^2}{Z_2^2}
\end{bmatrix}. \quad (7-4)
\]

The unknown parameters in the scattering parameters matrix (7-2) can also be presented as: [46]

\[
S_{\text{match}} = \frac{\Gamma_{\text{even}} + \Gamma_{\text{odd}}}{2}, \quad (7-5)
\]

\[
S_{\text{thr}} = \frac{T_{\text{even}} + T_{\text{odd}}}{2}, \quad (7-6)
\]

\[
S_{\text{coup}} = \frac{T_{\text{even}} - T_{\text{odd}}}{2}, \quad (7-7)
\]

\[
S_{\text{iso}} = \frac{\Gamma_{\text{even}} - \Gamma_{\text{odd}}}{2}, \quad (7-8)
\]

where \(\Gamma_{\text{even}}\) and \(\Gamma_{\text{odd}}\) are the reflection coefficients at the input port of the even- and odd-half circuits respectively, and \(T_{\text{even}}\) and \(T_{\text{odd}}\) are the transmission coefficients. \(\Gamma_{\text{even}}, \Gamma_{\text{odd}}, T_{\text{even}}, T_{\text{odd}}\) can be calculated with the parameters in the \textit{ABCD} matrixes (7-3) and (7-4) [46].
\[ \Gamma_{\text{even/odd}} = \left( \frac{A + \frac{B}{Z_0} - C \cdot Z_0 - D}{A + \frac{B}{Z_0} + C \cdot Z_0 + D} \right)_{\text{even/odd}}, \quad (7-9) \]

\[ T_{\text{even/odd}} = \left( \frac{2}{A + \frac{B}{Z_0} + C \cdot Z_0 + D} \right)_{\text{even/odd}}, \quad (7-10) \]

So, all the unknown parameters in the scattering parameter matrix can be represented with the design parameters in Figure 7.4. Comparing the scattering parameter matrix in (7-2) with that of the ideal quadrature coupler in (7-1), the following conditions should be fulfilled:

\[ S_{\text{match}} = S_{\text{iso}} = 0, \quad (7-11) \]

\[ S_{\text{thru}} \perp S_{\text{coup}}. \quad (7-12) \]

Substituting (7-5)-(7-8) into (7-11)-(7-12), \( \Gamma_{\text{even}}, \Gamma_{\text{odd}}, T_{\text{even}}, T_{\text{odd}} \) should satisfy the following conditions.

\[ \Gamma_{\text{even}} = \Gamma_{\text{odd}} = 0 \quad (7-13) \]

\[ |T_{\text{even}}| = |T_{\text{odd}}| \quad (7-14) \]

According to (7-9)-(7-10) and (7-13)-(7-14), the relationships among the \( \text{ABCD} \) parameters and characteristic impedance \( Z_0 \) are

\[ A_{\text{even}} + \frac{B_{\text{even}}}{Z_0} = C_{\text{even}} Z_0 + D_{\text{even}}, \quad (7-15) \]
\[ A_{\text{odd}} + \frac{B_{\text{odd}}}{Z_0} = C_{\text{odd}}Z_0 + D_{\text{odd}}, \quad (7-16) \]

\[
\begin{vmatrix}
A_{\text{even}} + \frac{B_{\text{even}}}{Z_0} + C_{\text{even}}Z_0 + D_{\text{even}} \\
A_{\text{odd}} + \frac{B_{\text{odd}}}{Z_0} + C_{\text{odd}}Z_0 + D_{\text{odd}}
\end{vmatrix}
= \begin{vmatrix}
A_{\text{odd}} + \frac{B_{\text{odd}}}{Z_0} + C_{\text{odd}}Z_0 + D_{\text{odd}}
\end{vmatrix}
\quad (7-17)
\]

Substituting the ABCD parameters shown in (3) - (4) into (15) - (17), the relationship between the design parameters \( Z_1 \) and \( Z_2 \) can be obtained. Equations (18) and (19) display the two solutions from (3) – (4) and (15) - (17).

**Solution 1:**
\[
\begin{cases}
1 + \frac{Z_1}{Z_2} = 0 \\
Z_0^2 = Z_1Z_2
\end{cases}
\quad (7-18)
\]

**Solution 2:**
\[
\begin{cases}
5 + 3\frac{Z_1}{Z_2} = 0 \\
Z_0^2 = \frac{Z_1Z_2}{3}
\end{cases}
\quad (7-19)
\]

Suppose both \( Z_1 \) and \( Z_2 \) are implemented with lumped-element components: inductors or capacitors.

\[
Z_{1,2} = joL \text{ or } \frac{1}{joC_p} \quad (7-20)
\]

In case A, when the \( Z_1s \) are capacitors and the \( Z_2s \) are inductors, according to the coupler operating conditions (7-18) - (7-19), the design parameters \( L \) and \( C_p \) should satisfy the following equation.
\begin{align*}
\begin{cases}
\omega_{a1}^2 L_{a1} C_{p,a1} = 1 \\
\frac{L_{a1}}{C_{p,a1}} = Z_0^2
\end{cases}
\quad \text{or} \quad
\begin{cases}
\omega_{a2}^2 L_{a2} C_{p,a2} = \frac{3}{5} \\
\frac{L_{a2}}{C_{p,a2}} = 3Z_0^2
\end{cases} \tag{7-21}
\end{align*}

In case B, when the \(Z_i\)s are inductors and the \(Z_2\)s are capacitors, the design parameters \(L\) and \(C_p\) should satisfy (7-22)

\begin{align*}
\begin{cases}
\omega_{bl}^2 L_{bl} C_{p,bl} = 1 \\
\frac{L_{bl}}{C_{p,bl}} = Z_0^2
\end{cases}
\quad \text{or} \quad
\begin{cases}
\omega_{b2}^2 L_{b2} C_{p,b2} = \frac{5}{3} \\
\frac{L_{b2}}{C_{p,b2}} = 3Z_0^2
\end{cases} \tag{7-22}
\end{align*}

From the previous analysis, the proposed coupler topology can have two matching frequency points in both Case A and B. For Case A, they are:

\begin{align*}
\omega_{a1} &= \frac{1}{\sqrt{L_{a1} C_{p,a1}}} , \quad \text{when} \quad L_{a1} = \frac{Z_0}{\omega_{a1}} , \quad C_{p,a1} = \frac{1}{\omega_{a1} Z_0} ; \tag{7-23}
\omega_{a2} &= \frac{3}{\sqrt{5L_{a2} C_{p,a2}}} , \quad \text{when} \quad L_{a2} = \frac{3Z_0}{\sqrt{5\omega_{a2}}}, \quad C_{p,a2} = \frac{1}{\sqrt{5\omega_{a2}} Z_0} . \tag{7-24}
\end{align*}

For Case B, they are:

\begin{align*}
\omega_{bl} &= \frac{1}{\sqrt{L_{bl} C_{p,bl}}} , \quad \text{when} \quad L_{bl} = \frac{Z_0}{\omega_{bl}} , \quad C_{p,bl} = \frac{1}{\omega_{bl} Z_0} ; \tag{7-25}
\omega_{b2} &= \frac{3}{\sqrt{5L_{b2} C_{p,b2}}} , \quad \text{when} \quad L_{b2} = \frac{\sqrt{5}Z_0}{\omega_{b2}}, \quad C_{p,b2} = \frac{\sqrt{5}}{3\omega_{b2} Z_0} . \tag{7-26}
\end{align*}
In both A and B cases, the final design parameters can be determined with the following equations to approximately satisfy the matching conditions at two separate frequency points.

Case A:

\[
L_a = \sqrt{L_{a1}L_{a2}} = \frac{\sqrt{3}Z_0}{\omega_0}, \quad C_a = \sqrt{C_{p1}C_{p2}} = \frac{1}{\sqrt{3}\omega_0 Z_0},
\]  

(7-27)

Case B:

\[
L_b = \sqrt{L_{b1}L_{b2}} = \frac{\sqrt{3}Z_0}{\omega_0}, \quad C_b = \sqrt{C_{p1}C_{p2}} = \frac{1}{\sqrt{3}\omega_0 Z_0},
\]  

(7-28)

where \(\omega_0\) is the design center frequency. Through this method, the operating bandwidth of the proposed coupler is extended.

### 7.4.2 Circuit Realization and Ideal Calculation of the Proposed Coupler Structure

Figure 7.6 shows two circuits for the proposed coupler structure. The circuit of Case A is shown in Figure 7.6(a), where the \(Z_1\)s are capacitors and the \(Z_2\)s are inductors. That of Case B is shown in Figure 7.6(b), where the \(Z_1\)s are inductors and the \(Z_2\)s are capacitors. Their design parameters with a designed center frequency of 6 GHz are calculated in Matlab. In Case A, the design parameters are calculated from (27), \(L=1.54\) nH, \(C_p=354.78\) fF; while in Case B, the design parameters are calculated from (28), \(L=1.98\) nH, \(C_p=458\) fF.
Figure 7.6: Two Types of the Circuits for the Proposed Coupler Structure:
(a) Case A, (b) Case B.
The theoretical scattering parameters for both couplers are also calculated in Matlab and the calculated results are shown in Figure 7.7.

Figure 7.7: Theoretical Performance for Case A and Case B: (a) Matching and Isolation characteristics, (b) Through and Coupling characteristics, (c) Phase Shift Difference between Through and Coupled ports.

Figure 7.7(a) shows that there are two matching frequency points as the analysis in section 2, and the theoretical operating bandwidth is about 2 GHz (5.2 GHz – 7.2 GHz) if -10 dB is considered as the acceptable standard for $S_{\text{match}}$ and $S_{\text{iso}}$. Figure 7.7(b) presents the through and coupling factors of both cases and the maximum through loss is 5 dB. Figure 7.7(c) shows the phase shift differences between through and coupled ports. In a
single T/π matching frequency design, the phase difference curves are monotonic, while there is an approximately flat line in the proposed structure as shown in Figure 7.7(c) even though there are ripples. Ideal quadrature couplers have a 90° phase shift difference. According to Figure 7.7(c), the phase shift difference error ranges from -5.9° to 1.76° in the operating frequency range from 5.2 GHz to 7.2 GHz for both Case A and B. The theoretical performance of both cases is similar. However, there are only four inductors in Case A while eleven inductors in Case B. When considering the chip area, Case B is not a good candidate for CMOS integration and only Case A is appropriate in a real circuit design.

Figure 7.8: Two Traditional Lumped-Element Quadratures [58]

Figure 7.8 presents two existing well-known lumped-element couplers with four inductors [58]. Their theoretical performance are calculated and summarized, and compared with the two proposed couplers in Table 7.1. According to Table 7.1, the
The proposed coupler (Case A) can provide a wider operating frequency range with less phase difference error (~50% reduction) theoretically than existing lumped-element quadratures with four inductors.

<table>
<thead>
<tr>
<th></th>
<th>Bandwidth (GHz)</th>
<th>Phase Errors</th>
<th>Number of Inductors</th>
</tr>
</thead>
<tbody>
<tr>
<td>Figure 9 (a)</td>
<td>1.59 (5.25 - 6.84)</td>
<td>-1.6° - 9.36°</td>
<td>4</td>
</tr>
<tr>
<td>Figure 9 (b)</td>
<td>1.59 (5.25 - 6.84)</td>
<td>-1.7° - 10.2°</td>
<td>4</td>
</tr>
<tr>
<td>Ref [64]</td>
<td>1.88 (5.30 - 7.18)</td>
<td>-10.5° - 0°</td>
<td>4</td>
</tr>
<tr>
<td>Ref [65]</td>
<td>1.74 (5.42 - 7.16)</td>
<td>-9.2° - 0.68°</td>
<td>4</td>
</tr>
<tr>
<td>Case A</td>
<td>2.0 (5.2 - 7.2)</td>
<td>-5.9° - 1.76°</td>
<td>4</td>
</tr>
<tr>
<td>Case B</td>
<td>2.0 (4.9 - 6.9)</td>
<td>-5.9° - 1.76°</td>
<td>11</td>
</tr>
</tbody>
</table>

Table 7.1: Comparison of the Proposed and Existing Lumped-Element Couplers

7.4.3 CMOS Implementation and Post Layout Simulation of the Quadrature Coupler

In order to verify the theoretical calculation, and to further analyze its performance, especially the effects of parasitic components in IC implemented capacitors and inductors, Case A is designed in a 0.13 μm CMOS process and simulated with Cadence Spectre.

Figure 7.9 shows the layout of Case A. To diminish the effects of the process variations on its performance, the layout should be drawn as symmetrical as possible. The active area is 560 μm × 640 μm. The post-layout simulation is done with Cadence Spectre and the post-layout simulated results are shown in Figure 7.10 and Figure 7.11.
Figure 7.9: Layout of the Circuit in Case A

Figure 7.10 and Figure 7.11 present the post-layout simulated results in comparison with theoretical calculated results. The discrepancies (Δ) between the post-layout simulated scattering parameters and their theoretical calculated counterparts are also included. For the magnitude responses in Figure 7.10, the discrepancies are calculated using (7-29). While for the phase responses in Figure 7.11, the discrepancies are calculated using (7-30).

\[ \Delta = \text{dB}(|S_{\text{calculated}}|) - \text{dB}(|S_{\text{simulated}}|) \]  
\[ \Delta = \text{Phase}(S_{\text{calculated}}) - \text{Phase}(S_{\text{simulated}}) \]
According to Figure 7.10(a), there are large discrepancies between the simulated and calculated $S_{\text{match}}$ at the two matching frequencies, and the maximum magnitude is 15 dB. However, the simulated $S_{\text{match}}$ is still acceptable. Similar phenomenon happens in the isolation parameter as shown in Figure 7.10(b). The operating bandwidth is not affected and still ranges from 5.2 GHz to 7.2 GHz, if -10 dB is considered as an acceptable matching and isolation standard. Both simulated parameters meet this standard. Figure 7.10(c) and 7.10(d) show that the post layout simulated $S_{\text{thru}}$ and $S_{\text{coup}}$ curves are lower than the theoretical $S_{\text{thru}}$ and $S_{\text{coup}}$ curves respectively. The maximum discrepancies in the
operating frequency range for $S_{thru}$ and $S_{coup}$ are 3.8 dB and 4.7 dB respectively. The simulated $S_{thru}$ ranges from -3.4 dB to -6.3 dB and simulated $S_{coup}$ ranges from -0.6 dB to -5.0 dB.

Figure 7.11: Post-layout Simulated Phase Responses

phase shift (a) from input port to through port (b) from input port to coupled port.

The phase shift from input port to through and coupled ports are shown in Figure 7.11(a) and (b). Within the operating bandwidth, the discrepancies between the calculated and simulated phase shifts are from -14.7° to -5.9° for the through port and from -3.7° to 6.9° for the coupled port. The parasitic resistance of each on-chip inductor, which is the main contributor to those discrepancies, is about 4 Ω at the center frequency. This is the parasitic parameter that leads to the differences between the calculated and simulated results. However, the performance still remains reasonable and is not seriously deteriorated. Higher Q-factor capacitors and inductors are required to reduce these differences.
Figure 7.12: Monte Carlo simulations depicting the process variations and the parameter mismatch effects on (a) input-matching s-parameter $S_{\text{match}}$, (b) through s-parameter $S_{\text{thru}}$, (c) coupling s-parameter $S_{\text{coup}}$, and (d) isolation s-parameter $S_{\text{iso}}$.

To demonstrate the effects of process variation and parameter mismatches on this circuit, a series of simulations was run. Figure 7.12 shows the output generated by Monte Carlo analysis in Cadence across 500 runs at the designed center frequency of 6 GHz. Figure 7.12(a) shows the distribution of the input matching parameter; the mean $S_{\text{match}}$ at 6 GHz is -13.3 dB with a standard deviation (sd) of 0.363 dB. Figure 7.12(b) shows the
distribution of the $S_{thru}$ parameter, where the mean is -3.48 dB and the standard deviation is 0.074 dB. Figure 7.12 (c) is the coupling factor, where the mean is -9.2 dB and the standard deviation is 0.573 dB. Figure 7.12(d) is the isolation, where the mean is -21.24 dB and the standard deviation is 0.595 dB. As demonstrated by the graphs, this design, a quadrature coupler, has good tolerance to process variation and parameter mismatches.

### 7.5 Summary on the Quadrature Structure Design

This chapter discussed the quadrature signal realization for the proposed UWB SDR application. The quadrature signals can be generated using quadrature couplers from either RF/IF signal or LO signal. When generating quadrature signals from RF signal, it is desired that the operating frequency bandwidth could be extended to cover at least an entire band group (1.6 GHz).

By introducing two quasi matching frequency points, a lumped-elements quadrature coupler structure with extended operating bandwidth is proposed, presented, analyzed, and calculated. At the center operating frequency of 6 GHz, the calculated results show that its operating bandwidth is up to 2 GHz with a phase shift difference error range from -5.9° to 1.76°, which is much better than the existing lumped-elements quadratures with four inductors. As an example, a CMOS realization of the proposed quadrature coupler structure is designed, and the post-layout simulation results are presented in this chapter.
CHAPTER 8

CONCLUSION

To meet the requirements of the ever expanding wireless system, today’s receiver requires flexibility and tunability, which can be configured through software. The hardware based RF front end circuit is then a bottleneck for this design trends. This work focused on the design considerations of several RF front end circuit modules in the signal path of a proposed digitally controlled channelized SDR receiver architecture. The objective of the circuit design considerations is to give an idea of possible circuit design techniques for the proposed SDR system, and also to prove the plausibility of the proposed SDR. To meet this objective, a system investigation of a proposed SDR receiver architecture is first performed to address the requirements and challenges for the RF front end circuit modules design. Then the detailed circuit level investigations are performed on each individual front end circuit modules in the signal path chain, including the LNA, mixer, and quadrature generating circuits. Design examples of the discussed front end circuit modules are presented, and the simulated results are also included in this work.
In more detail, the specific contributions in the system investigation include:

1) Proposed a channelized SDR architecture for the 0.5 – 10.6 GHz application, the frequency plan is addressed. The channelization is achieved by the combination of a digital controlled front end as well as a digital filter-bank channelizer. The RF front end channelizes the entire bandwidth into seven 1.6 GHz sub bands. Instead of using an individual signal path for each frequency band, the proposed SDR allows all the frequency bands to share the same front end to reduce the costs. The requirements of the wideband spectrum access and digitally controlled frequency tunability in the front end circuit modules design are discussed.

2) The link-budget analysis is performed to determine the detail specifications for each front end circuit blocks in the signal chain of the proposed SDR. The objective applications are summarized and the system requirements are concluded. System simulation is performed in ADS with different applications, modulations, and at different frequencies and bandwidths. The simulated results illustrate the theoretically performance of the proposed system with the consideration of several non-ideality in the front end circuit modules.

And the specific contributions in the circuit level investigation of the front end circuit modules design include:

1) For the selected cascoded source degeneration LNA structure, a noise analysis, modeling and optimization technique is proposed. Using the proposed procedure, the design parameters can be calculated in software. A specific design example is
given using the proposed procedure and the simulated results matches with the anticipation.

2) A frequency tunable LNA design is presented as an example. Bandwidth extension methods have been used in the source degeneration structure to extend the input matching bandwidth to 3-5GHz. Frequency tunable capacitor arrays are used at the output of the LNA, and desired signals can be selected from the 9 mini-bands using the digital control signals.

3) A differential double balanced Gilbert mixer with an ultra wide IF bandwidth covering one entire band group of 1.6 GHz is presented and simulated. The IF bandwidth is extended by an innovative idea of attaching a band pass filter at the output loads. In the proposed mixer design, the variation in the conversion gain in each band group is less than 3 dB.

4) A quadrature coupler structure is proposed as a quadrature signal splitter in the proposed SDR. By introducing two quasi matching frequency points, the proposed quadrature coupler has an extended operating bandwidth of around 2 GHz. The proposed quadrature coupler is implemented using lumped-elements in CMOS technology, the layout has been generated, and the post-layout simulated results matches well with the theoretical calculation.

In conclusion, this work is focused on the front end circuit modules designs of a proposed digitally controlled channelized SDR receiver. The design considerations, challenges, non-ideal performances, and circuit implementation methods are discussed. Specific circuit design examples are presented with simulated results.
BIBLIOGRAPHY


