The Design Methodology and Optimization of Varactors Based Tunable Matching Network for Power Amplifiers with Load Adaptation Technique

THESIS

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Abstract

This thesis presents two tunable matching network designs relying on varactors. The matching network should provide and instantaneous optimized impedance according to different power levels of the power amplifier. The matching networks are designed for an high efficiency class B power amplifier operating at 2 G Hz. Two topologies for the load matching network are considered in this thesis: the Pi network and the T network. The varactors are integrated as part of the load network. By changing the biasing voltages on the varactors, the value of capacitors can be varied and the output impedance modified. The design procedure followed consists in determining the design parameters yielding the maximum load impedance range that can be provided by the network.

The major research steps followed include (1) the computational algorithm development, (2) ADS simulations, (3) circuit fabrication and (4) measurements.
Dedicate this to my dearest family, who always support me and provide me with endless love.
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Finally, I am grateful to my parents for their unconditional supports, and for providing me with their love and encouragements.
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Chapter 1
Introduction

Wireless communication systems, such as cellular phones, wireless modems, Global Positioning System (GPS), require power amplifiers to amplify the signal before transmitting it to the antenna. Power amplifiers are considered to be one of the most power consuming device. In order to enhance the battery operation time and increase the cellular phone operating time, improving efficiency of the power amplifier has became one of the most important topic. Multitude of techniques have been pursued to increase the efficiency. For example, multiple/dual biasing control have been proposed, in order to find the maximum efficiency by moving the operation point with a change of the base bias and collector bias on BJT amplifier [2]. However, the multiple biasing control require efficient dc to dc convertors. Doherty amplifiers is presently the most popular technique to increase the PA efficiency for a wide range of operating power (dynamic range) [3]. Doherty amplifiers require a main amplifier, and auxiliary amplifier and 3 dB coupler which complicates the circuit and also increases the cost and the size of the topology [4]. As a result, a tunable matching network could provide an attractive alternative.
Wireless communication systems which support multiple standards includes several parallel amplifier/filtering path which rely on duplexers or switches to switch between the different circuits for the different bands supported. Nowadays, a more sophisticated method is to use a tunable network to replace the parallel path, this can lower the cost, size and power dissipation [1]. Unlike a fixed matching network which requires different matching networks to match different power levels, the power amplifier only need one tunable matching network and it can tune the impedance automatically according to the different power input to the PA. There are lots of components available for the tuning purpose, such as microelectromechanical systems, ferroelectric capacitors. Varactor tuning is the most common and simplest tuning technique [5]. Since the varactors are passive devices consisting of a reverse biased diodes, no power is consumed and it can be easily integrated into the PA circuit without yielding complicated circuits.

The varactors that will be used in this thesis are GaAs Hyperabrupt varactor diodes MGV07508 from Aeroflex Metelica Inc. These high Q varactor diodes have tuning characteristic which is superior than silicon diodes. The main reason is that the high electron mobility in the low doped parts of the active region cause low series resistance. The operation frequency is up to 40 GHz and the voltage range is from 2 volts to 22 volts which meets the requirement of power amplifiers.
1.1 Objective of The Thesis

In the tunable network based on GaAs varactors, the impedance changes by varying the DC bias voltages. The work is motivated by the research work of another member of the Non Linear RF group, Headong Jang who is working on PA amplifiers based upon load modulation. We work as a team and he is in charge of designing the class B power amplifier design and I am in charge of designing the tunable matching network. This high power class B amplifier output is 40 dBm (10 Watts) operating at 2 GHz. The tunable matching network design is seeking to obtain the maximum tuning range, in other words, the reflection coefficient should map a maximum area on the Smith chart. By using the mathematical formalism of transmission line theory, the equations for the whole matching network can be obtained. Further by implementing those equations in MATLAB one can numerically calculate the coverage area of the reflection coefficient on the Smith Chart. The best layout result will be first obtained using MATLAB and verified using simulations in ADS.

1.2 Organization of the Thesis

The thesis is organized as follows: a brief introduction to power amplifiers, modern tunable matching networks, and design goals will be presented in Chapter 2. The theoretical derivation and computational algorithms will be presented in this chapter. In Chapter 3, we will derive the characteristics of the matching network, including loss, gain
and sensitivity. In Chapter 4, the circuit simulation and optimization, IMD (intermodulation distortion) and harmonic balance will be discussed in ADS. Chapter 5 will present the performance of the matching network. Chapter 6 the conclusion will a brief discussion for further work.
Chapter 2
Topologies Design

In the first section of this chapter, we will introduce the design goal for the matching networks. This will include an overview of high efficiency power amplifiers. In particular we will review the ideal class B power amplifiers characteristics review and the real-world characteristics of the particular class B power amplifier that is considered for this thesis. The second section, will present a review of matching networks, and the previous works which inspired this work. The third section will present the analytic formula derivations for the matching network for two topologies: Pi and T. The last section is the computational algorithm which was implemented for the matching networks analysis in MATLAB.

2.1 Design Goals

2.1.1 PA and Design Goal, Class A B AB C

In the wireless communication, power amplifiers are used in order to boost the signal power delivered to the antenna. Power amplifier is one of the fundamental devices in the long distance communication. With novel electronic growth, for example, PDA (personal digital assistant), cellular phone...etc, power amplifiers have became very common and
are highly demanded by the wireless industry. There are several types of operations of power amplifier: class A, B, C, D, E, F and AB.

![Diagram of wireless communication]

**Figure 2.1 The concept of wireless communication**

Fig. 2.2 shows the schematic of Class A, B, AB and C power amplifiers. All those power amplifiers are differentiated by their conduction angle. Conduction angle is the time period in which the device is conducting. Class A power amplifier is the simplest amplifier. It also provides the best linearity and lowest distortion. Its conduction angle is $2\pi$ (100%). The bias voltage at gate of the transistor is always much higher than the threshold voltage $V_T$, this makes the transistor works in saturation (active) mode in the entire cycle, so the drain current is greater than zero. Its operating current and voltage waveforms are shown in Fig 2.3. Although it provides high linearity, its efficiency is low: its DC to RF conversion efficiency is only 50%.
Figure 2.2 Conceptual schematic for Class A, B, AB and C PA

Figure 2.3 Ideal Voltage/Current Waveforms: class A, B, C
Figure 2.4 The bias voltage of Class A power amplifier

Figure 2.5 The bias voltage of Class B power amplifier
Another linear power amplifier is the Class B power amplifier. In the case of the Class B power amplifier, the conduction angle is $\pi$ and the gate bias voltage for an ideal Class B power amplifier is around the threshold voltage $V_T$. As is shown in Fig. 2.3, in half the cycle, the voltage is greater than $V_T$, so the conduction current exits, the voltage of another half circle is smaller than $V_T$, in this half circle, the conduction current is zero. The efficiency of Class B theoretically can reach 80%, depending on the FET I-V characteristics. A decrease of the conduction angle, increases the efficiency. Therefore, the conduction angle of Class C power amplifier is between 0 and $\pi$, furthermore, the bias voltage of Class C power amplifier is below $V_T$. Theoretically, when the conduction angle is close to zero, the Class C amplifiers can provides a high efficiency that can even approach 100%. However, distortion increases with the decrease of conduction angle, due to the instability in the collector/drain. Class C amplifier are practical at low frequencies. Class AB is a compromise between Class A (higher linearity) and Class B (higher efficiency) amplifier. The conduction angle is between $\pi$ and $2\pi$. Table 2.1 presents the brief summary of Class A, B, AB and C power amplifiers.
Figure 2.6 Bias voltage of Class AB power amplifier

Figure 2.7 The bias voltage of Class C power amplifier
Table 2.2 Characteristics Summary of Class A, B, AB and C power amplifiers

<table>
<thead>
<tr>
<th>PA Classes</th>
<th>A</th>
<th>B</th>
<th>AB</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conduction Angle (θ)</td>
<td>2π</td>
<td>π</td>
<td>π ~2π</td>
<td>0 ~ π</td>
</tr>
<tr>
<td>Maximum Drain Efficiency (%)</td>
<td>50</td>
<td>78.5</td>
<td>50~78.5</td>
<td>100</td>
</tr>
<tr>
<td>Output Power Capability</td>
<td>large</td>
<td>medium</td>
<td>medium</td>
<td>low</td>
</tr>
</tbody>
</table>
2.1.2 Switching Power Amplifiers

Class D power switching amplifier includes two transistors. These two transistors switch alternately so that they are driven 180 degree out of phase; in other words, only one transistor operates at a time. Fig. 2.4 is its schematic. The voltage and current waveforms are non-overlapping rectangular waveforms that makes this Class D amplifier reach up to 100% efficiency. However, the loss in the switch is the major drawback at the moment which prevent high frequency operation. Generally there is a short time where both transistors are active. This generates a short circuit between the power supply and the ground. This short circuit induces a large current which creates a significant energy loss. Furthermore, if there is a capacitance in the output side of the amplifier, this capacitance will be charged and discharged thought the transistor switch. As a result, the voltage waveform is not a perfect rectangular shape anymore. Due to the loss, Class D power amplifier is seldom used at RF frequencies.
Figure 2.8 Schematic for Class D power amplifiers
Switching power amplifiers include Class D, E, and F. Among all these amplifiers, Class E is the most common and basic form [13]. For Class E amplifier, by activating the transistor as a switch, can reach a very high dc to RF efficiency. When the transistor switch to on mode, a high current is induced and the voltage is nearly 0; vice versa, in the switch off mode, the current reduces to zero and generates high voltages. Therefore, the current and voltage waveforms are non-overlapping. The power dissipated by transistor which is the product of the transistor voltage and current at each time in in the RF period is then greatly reduced. Therefore, ideally, the Class E amplifier can reach 100% efficiency without power dissipation, however efficiency values around 60% are typically achieved [6]. The schematic of Class E power amplifier are shown in Fig. 2.5 below.

![Class E Power Amplifier Schematic](image)

**Figure 2.9 Conceptual schematic for Class E PA [6]**
The last switching power amplifiers that will be presented in this thesis is the Class F power amplifier in Fig. 2.6 [6]. This is another switching method that makes the circuit operate in on and off mode, in order to induce non-overlapping voltage and current. This class amplifier utilizes parallel inductor and capacitor tanks and also quarter wave transmission line. In the fundamental frequency, the input impedance is a real number impedance. In odd harmonic frequency, the output circuit becomes an open circuit which prevents the current from flowing in. In the even harmonic mode, the output circuit is equal to a short circuit and the voltage is zero. With this technique, the class F amplifier achieves non-overlapping IV curve and high efficiency.

\[
Z_{in}(nf_0) = \begin{cases} 
Z_1^2 / R & \text{open at } f_0 \\
\text{@ odd harmonics} & (n = 3, 5, \ldots) \\
\text{short @ even harmonics} & (n = 2, 4, \ldots)
\end{cases}
\]

Figure 2.10 schematic for Class E PA

[6]
2.2 Class B Power Amplifier Characteristics and Efficiency

The matching network to be designed in this thesis is for a Class B power amplifier. The characteristics of Class B amplifier will be briefly introduced in this section. In Class B amplifier, the dc drain current is the average value of the half sin waveform. From Fourier analysis we have,

\[ I_{dc} = \frac{I_{max}}{\pi} \]  \hspace{1cm} (2.1)

And the amplifier’s dc power is

\[ P_{dc} = V_{dd} \frac{I_{max}}{\pi} \]  \hspace{1cm} (2.2)

\[ P_L = \frac{1}{2} I_L |V_L| \]  \hspace{1cm} (2.3)

Again from Fourier analysis

\[ I_L = \frac{1}{2} I_{max} \]  \hspace{1cm} (2.4)

\[ P_L = \frac{1}{2} (\frac{1}{2} I_{max}) V_{dd} = \frac{1}{4} I_{max} V_{dd} \]  \hspace{1cm} (2.5)

So, the dc to RF efficiency is

\[ \eta_{dc} = \frac{P_L}{P_{dc}} = \frac{\pi}{4} = 78\% \]  \hspace{1cm} (2.6)
2.3 The Modern Matching Network

For the high power amplifiers in the communication system, the efficiency decreases as the power level reduces. In order to solve this problem, some method has been studied. In this section, I will briefly review one unique load adaptation technique which uses switch transformer. This study is not only the motivation of my thesis but also provide us with some background knowledge. A part from using varactors for the tunable matching network [7], designers have also switches to realize tunable impedance transformers. This transformer consists of several transmission lines with different characteristic impedance arranged in parallel. The switches are inserted on each transmission line to control the line connection, the switcher connect to corresponding transmission line output base on the power level detect be from the input detector. The output network use quarter wave transmission line, for which the input impedance can be expressed as:

\[ Z_{in} = \frac{Z_T^2}{Z_L} = f(Z_T) \]  

(2.7)

where \( Z_L \) is the load impedance. By choosing a quarter wave transmission line, the input impedance of the output matching network can be expressed as a function of \( Z_L \), the transforming impedance.

The topology of this design is shown in Fig.2.8
Figure 2.11 A basic structure of the tunable impedance transformer

[7]

However, in this technique, the output impedance can only be matched to certain prescribed values defined by the transformers’ characteristic impedance. Mismatch loss will be induced when choosing the next adjacent impedance value instead of the exact value. Increasing the number of transmission line transformers for the purpose of increased impedance tuning, will however complicate the circuit. Beside, this dynamic load transformer circuit is outside of the power amplifier instead of integrated into the PA and this will not only complicate the circuit but also increase its loss.
2.4 Tunable Matching Networks Formula Derivation

2.4.1 Design Goal and T parameter

Fig. 2.12 illustrates the reflection coefficient $S_{11}$ of Class B power amplifier that needs to be matched with the tunable matching network. Its power level is 10 Watts. The data is enclosed in Appendix. In order to match the impedance region, the reflection coefficient equations of the entire matching network need to be derived. In this section we will present the analytical derivation for Pi-topology network and the T-topology network will be introduced in next section. To cascade the sub-circuits of the matching network, the T parameters, also called the scattering transfer parameters or chain scattering parameters are used [11].

![Figure 2.12 The Reflection Coefficient of Power Amplifier](image)
First, the definition of T parameters will be briefly introduced. Fig.2.13 shows the definition of T parameter:

\[
\begin{bmatrix}
    a_1(l_1) \\
    b_1(l_1)
\end{bmatrix} =
\begin{bmatrix}
    T_{11} & T_{12} \\
    T_{21} & T_{22}
\end{bmatrix}
\begin{bmatrix}
    a_2(l_2) \\
    b_2(l_2)
\end{bmatrix}
\]  

(2.8)

And, the transform function between S and T parameters is [11]

\[
\begin{bmatrix}
    T_{11} & T_{12} \\
    T_{21} & T_{22}
\end{bmatrix} =
\begin{bmatrix}
    \frac{1}{s_{21}} & -\frac{s_{22}}{s_{21}} \\
    \frac{s_{11}}{s_{21}} & \frac{s_{11}s_{22}}{s_{21}}
\end{bmatrix}
\]  

(2.9)

and [11]

\[
\begin{bmatrix}
    S_{11} & S_{12} \\
    S_{21} & S_{22}
\end{bmatrix} =
\begin{bmatrix}
    \frac{T_{21}}{t_{11}} & \frac{T_{21}T_{12}}{t_{11}} \\
    \frac{1}{t_{11}} & \frac{T_{12}}{t_{11}}
\end{bmatrix}
\]  

(2.10)

Figure 2.13 A basic structure of the tunable impedance transformer

[11]
2.4.2 Pi Topology Analytical Derivation

Fig. 2.14 shows my pi topology matching network design. This is a symmetric circuit which include three transmission lines and two varactors. Next, in order to derive the cascaded T parameter matrix for the entire matching network, we separate the matching network in to three parts, as shown in Fig 2.14. Starting from the input side block adjacent to the power amplifier, the first block includes one open stub transmission line in series with a varactor, the second block is a transmission line in the center connected both sides, and the third block like for the first block includes an open stub transmission line in series with a varactor. The T parameter matrix of a single transmission line can be expressed as [9]

\[
T_{\text{line}} = \begin{bmatrix}
    e^{j\theta} & 0 \\
    0 & e^{-j\theta}
\end{bmatrix}
\]  

(2.11)

The physical impact of the transmission line is to introduce a phase difference. The result of Eq. 2.11 is \( a_1 = e^{j\theta} b_2 \) and \( b_1 = e^{j\theta} a_2 \). These two equations present the phase difference between two ports which verify Eq.2.11.
Figure 2.14 The Pi tunable matching network topology.

The next step is to derive the T parameter matrix for the open stub transmission line in series with a varactor. The ABCD matrix of a parallel admittance between port 1 and port 2 in Fig. 2.15 [10] can be express as:

\[
\begin{bmatrix}
1 & 0 \\
\gamma & 1
\end{bmatrix}
\]  
(2.12)

Figure 2.15 The admittance of transmission line in parallel

\[
\frac{1}{\gamma} = Z_{in} = Z_0 \frac{Z_L + iZ_0 \tan(\beta l)}{Z_0 + iz_0 \tan(\beta l)}
\]  
(2.13)
Eq. 2.13 applies the transmission theory and shows the input impedance which includes one transmission line and one varactor. Next, transforming this ABCD parameters to S parameters with the purpose of transforming to T parameters. The S parameters transformed from ABCD parameters are

$$[S] = \begin{bmatrix} -\frac{YZ_0}{2+YZ_0} & \frac{2}{2+YZ_0} \\ \frac{2}{2+YZ_0} & -\frac{YZ_0}{2+YZ_0} \end{bmatrix}$$

(2.14)

Next, we transform the S parameters to T parameters.
where $Y_1, Y_2$ are the characteristic impedance of $l_1$ and $l_2$ transmission line stub, the default value of both is 50 Ohm. Now that the the matrix for each block has been derived, the next step is to cascade together all the three matrices. The total matrix $T_F$ is

$$T_F(\theta, l) = [T_1][T_{\text{line}}][T_2]$$

$$[T] = \begin{bmatrix} 1 + \frac{1}{2} Y Z_0 & \frac{1}{2} Y Z_0 \\ -\frac{1}{2} Y Z_0 & \frac{4 - (Y Z_0)^2}{2(2 + Y Z_0)} \end{bmatrix}$$

$$[T_1] = \begin{bmatrix} 1 + \frac{1}{2} Y_1 Z_0 & \frac{1}{2} Y_1 Z_0 \\ \frac{1}{2} Y_1 Z_0 & \frac{4 - (Y_1 Z_0)^2}{2(2 + Y_1 Z_0)} \end{bmatrix}$$

$$[T_2] = \begin{bmatrix} 1 + \frac{1}{2} Y_2 Z_0 & \frac{1}{2} Y_2 Z_0 \\ \frac{1}{2} Y_2 Z_0 & \frac{4 - (Y_2 Z_0)^2}{2(2 + Y_2 Z_0)} \end{bmatrix}$$

From [9] the reflection coefficient ($S_{11}$) for fundamental matching can express as

$$\frac{T_{F21}}{T_{F11}}$$

Next, implementing the equations in MATLAB we can computationally calculate and plot the reflection coefficient and map the area covered on the Smith chart as the voltages are varied.

The initial design is shown in Fig. 2.16. The reflection coefficient tuning cover area in Fig. 2.16 was not efficiently large enough so it was necessary to further develop the
MATLAB code to calculate the tuning area and find the maximum tuning area by sweeping the different length of the transmission lines.

![Diagram](image)

Figure 2.16 The initial mapping area of Pi topology matching network

2.4.3 Pi-Topology Tuning Area Calculation

In order to scientifically analyze and optimize the range of tuning, we proposed to use the area covered by the reflection coefficient. Thus a computational method is needed to calculate the mapping area. The reflection coefficients used for the mapping plot shown in the previous section are stored in a matrix where column and rows are associated with the two swept voltage used. The calculation method used consists in first determining the area contributed by each non-overlapping triangles sustained by three adjacent data.
points and then summing them to acquire the total area. The sub-areas for the general triangle shown in Fig. 2.17, can be calculated by applying the basic vector rule that the area of each sub-triangle is given by $\mathbf{a} \cdot \mathbf{b} = \frac{1}{2} |\mathbf{a}| |\mathbf{b}| \sin \theta$ where $\mathbf{a}$ and $\mathbf{b}$ are the vectors between point AB and AC, and $|\mathbf{a}|$ and $|\mathbf{b}|$ are their length. The coverage area of the initial design is only 0.2273 % over the whole smith chart which is obviously low.

![Figure 2.17 The S11 area calculation schematic](image)

With the purpose of finding the best length combination of the three transmission lines which maximizes the tuning range of the matching network, we first plot the contour plot of the area versus the transmission line $l$ and $l_1$. The relation between $l$ and $l_1$ is defined as $l = \alpha l_1$, $\alpha$ sweep from 1 to 2 by 0.01 step. Because a symmetric circuit is targeted, the transmission line $l_1$ is equal to $l_2$, so that sweeping between $l_1$ and $l_2$ is not necessary. Example of the sweeping contour plots are shown in Fig.2.18. Next we plot the maximum area value from contour plot versus $\alpha$ and chose the maximum area for the design. By doing this, the best design of all the two dimensional sweepings can be obtained. The result is shown in Fig.2.19.
Figure 2.18  Example of contour plots obtained by sweeping the transmission line length $l_1$ and $l_2$. 

27
Figure 2.19 The area coverage ratio versus alpha value

Figure 2.20 Two dimensional plot for the optimal values of 0.75 \(l_1\) and 0.75 \(l_2\).
Figure 2.21 The reflection coefficient mapping after MATLAB code optimization.
2.5 T-Topology

Another tunable matching network design topology design is T-shape circuit. Fig 2.22. This circuit includes one transmission line and three varactor diodes. An analytical method similar to the previous section will be followed.

Figure 2.22 The Pi tunable matching network topology

The next step is to derive the T parameter matrix for the open stub transmission line in series with a varactor. The ABCD matrix of a parallel impedance between port 1 and port 2 in Fig.2.23 is [10]

\[
\begin{bmatrix}
1 & Z \\
0 & 1
\end{bmatrix}
\]  (2.20)
Figure 2.23 The impedance of transmission line in series

The input impedance in the center which includes one transmission line and one varactor is

\[ Z = Z_{in} = Z_0 \frac{Z_L + iZ_0 \tan(\beta l)}{Z_0 + iZ_L \tan(\beta l)} \]  

(2.21)

Transferring Eq. 2.20 from ABCD parameter metric to S parameter gives:

\[
[S] = \begin{bmatrix}
\frac{Z}{Z_0} & \frac{2Z}{2+Z_0} \\
\frac{Z_0}{2+Z_0} & \frac{Z}{Z_0}
\end{bmatrix}
\]  

(2.22)

Transferring the above matrix from S parameter metric to T parameter gives:

\[
[T] = \begin{bmatrix}
\frac{Z_0}{2+Z_0} & \frac{-Z}{Z_0} \\
\frac{Z}{Z_0} & \frac{Z_0}{2}\frac{4-(\frac{Z}{Z_0})^2}{2(2+\frac{Z}{Z_0})}
\end{bmatrix}
\]  

(2.23)
\[ [T_F] = \begin{bmatrix}
\frac{2 + \frac{Z_1}{Z_0}}{2} & \frac{-\frac{Z_1}{Z_0}}{2} & \frac{2 + \frac{Z_2}{Z_0}}{2} & \frac{-\frac{Z_2}{Z_0}}{2} & \frac{2 + \frac{Z_3}{Z_0}}{2} & \frac{-\frac{Z_3}{Z_0}}{2}
\frac{2}{2} & \frac{2}{2} & \frac{2}{2} & \frac{2}{2} & \frac{2}{2} & \frac{2}{2}
\frac{4 - (\frac{Z_1}{Z_0})^2}{2} & \frac{4 - (\frac{Z_2}{Z_0})^2}{2} & \frac{4 - (\frac{Z_3}{Z_0})^2}{2} & \frac{2}{2} & \frac{2}{2} & \frac{2}{2}
\frac{2}{2(2+\frac{Z_1}{Z_0})} & \frac{2}{2(2+\frac{Z_2}{Z_0})} & \frac{2}{2(2+\frac{Z_3}{Z_0})} & \frac{2}{2} & \frac{2}{2} & \frac{2}{2}
\end{bmatrix} \]

\[ Z_1 = Z_3 = \frac{1}{j\omega c} \]

\[ Z_2 = Z_{in} = Z_0 \frac{Z_L + iZ_0 \tan(\beta l)}{Z_0 + iZ_L \tan(\beta l)} \]

Fig. 2.22 shows the initial design of T topology matching network, vice versa, the similar analysis method of Pi topology. Fig. 2.24 shows some tuning range mapping of this Pi topology design. However, the cover range cannot achieve an efficient tuning range, so this design will not be chosen.
Figure 2.24 The initial mapping area of T topology matching network
Chapter 3

The Characteristics of Tunable Matching Network

In this chapter, the characteristics of the tunable matching network designed will be first introduced and evaluated. This will include the power gain which is expressed by the S parameter and their sensitivity to the matching network when the frequency varies. Also, the loss of the matching network will be derived and discussed.

3.1 Power Gain

The power gain is an important factor for tunable matching networks because the main purpose of the matching network is to transfer the maximum of the input power to the output. The analysis method used in this chapter consists in plotting on the Smith chart using a contour plot, the power gain obtained versus the reflection coefficient. This representation enables us to correlate the relation between S11 and the power gain. The operating power gain [10]

\[
\text{Power Gain} = \frac{P_L}{P_{in}} = \frac{|S_{21}|^2 (1 - |\Gamma_L|)^2}{(1 - |\Gamma_{in}|^2)|1 - S_{22}\Gamma_L|^2} = \frac{|S_{21}|^2}{1 - |S_{11}|^2} \text{ for } \Gamma_L = 0 \tag{2.24}
\]
The result of the power gain plotted in MATLAB using Eq 2.24 are shown in Fig. 3.1. All the gains are higher than 0.9555 % and even reach 0.99 % of the input power which shows that a good result is obtained with the lossy varactor model assuming ideal transmission lines.

Figure 3.1 Contour plot of the power gain (colored lines) versus reflection coefficient.
3.2 Sensitivity

The sensitivity represents the stability of this tunable matching network when the instantaneous frequency (1MHz) departs from the center frequency. It is also indicative of the bandwidth the circuit. The figure in this chapter shows the contour plot on Smith Chart with the reflection coefficient mapping area. The sensitivity is expressed as the difference of the absolute value of Gamma obtained for two different frequencies. The result in Fig. 3.2 shows that the sensitivity of the reflection coefficient value when the frequency variation is below 0.023 which is small.

![Figure 3.2 The sensitivity (color lines) versus reflection coefficient.](image)

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3.3 The loss

The two main losses in microstrip line are dielectric loss and conduction loss [11].

\[ \alpha = \alpha_d + \alpha_c \]  

(3.1)

Where \( \alpha \) is the main loss, \( \alpha_d \) is dielectric loss and \( \alpha_c \) is conduction loss. \( \alpha_d \) can be expressed in terms of dielectric constant and effective dielectric constant. The formula for \( \alpha_d \) is derived below:

\[ \frac{W}{h} = \frac{2}{\pi} \left\{ B - 1 - \ln(2B - 1) + \frac{\varepsilon_r - 1}{2\varepsilon_r} \left[ \ln(B - 1) + 0.39 - \frac{0.61}{\varepsilon_r} \right] \right\} \]  

(3.2)

Where, the \( W \) and \( h \) are the width and length of microstrip line shown in Fig.3.3, in the substrate \( \varepsilon_r = 2.2 \) and with

\[ B = \frac{377\pi}{2\varepsilon_0\sqrt{\varepsilon_r}} \]  

(3.3)

The effective dielectric constant is

\[ \varepsilon_{ef} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r + 1}{2} \left( 1 + 12 \frac{h}{W} \right)^{-\frac{1}{2}} \]  

(3.4)

The dielectric loss coefficient is

\[ \alpha_d = 27.3 \frac{\varepsilon_r}{\sqrt{\varepsilon_{ef}}} \frac{\varepsilon_{ef} - 1}{\varepsilon_r - 1} \frac{\tan \delta}{\lambda_0} \]  

(3.5)

Where the substrate tangent loss is \( \tan \delta = 0.0009 \).
Next, we derive the formula for $\alpha_c$ the conductive loss. The first step is to calculate the effective width:

$$\frac{W_{\text{eff}}}{h} = \frac{W}{h} + \frac{t}{\pi h} \left( 1 + \ln\frac{2h}{t} \right)$$  \hspace{1cm} (3.6)

where, $t$ is the dielectric substrate thickness. The conductive loss is then:

$$\alpha_c = \frac{8.68R_s Q}{Z_0 h} \left\{ \frac{W_{\text{eff}}}{h} + \frac{2}{\pi} \ln \left[ 2\pi e \left( \frac{W_{\text{eff}}}{2h} + 0.94 \right) \right] \right\}^{-2}$$ \hspace{1cm} (3.7)

Where we define $R_s = \sqrt{\frac{\pi f \mu_0}{\sigma}}$ and where we have

$$Q = 1 + \frac{h}{W_{\text{eff}}} + \frac{h}{\pi W_{\text{eff}}} \left( \ln\frac{2h}{t} - \frac{t}{h} \right).$$ \hspace{1cm} (3.8)
Finally, after accounting for all the material and structure parameters, the loss of the microstrip line is 0.0048 dB/per meter. The next step is applying this loss to the transmission line equation and the MATLAB code.

For a lossless transmission line, the input impedance can be express as [14]

\[ Z_{in} = Z_0 \frac{Z_L + iZ_0 \tan(\beta l)}{Z_0 + iZ_L \tan(\beta l)} \]  \hspace{1cm} (3.9)

where \( Z_0 \) is the characteristic impedance, \( Z_L \) is the load impedance and \( l \) is the length of the transmission line. The input impedance of a lossy transmission line is then

\[ Z_{in} = Z_0 \frac{Z_L + Z_0 \tanh(\alpha + i\beta l)}{Z_0 + Z_L \tanh(\alpha + i\beta l)} \]  \hspace{1cm} (3.10)

Fig. 3.4 and Fig. 3.5 show the revised MATLAB result after loss is included. The tuning area (reflection coefficient S11) decreases from 64.51 % to 38.52 % but it merely affects sensitivity. However the loss significantly degrades the tuning range.
Figure 3.4 Power gain when the line loss is taken into consideration.

Figure 3.5 Tuner sensitivity when the line loss is taken into consideration.
Chapter 4

Tunable Matching Network in ADS

In this chapter, a varactor-based matching network based on the MATLAB algorithm developed in the previous chapter, will be designed, simulated and analyzed in ADS (advanced design system). Next the layout will be generated. For a realistic circuit to be simulated in ADS, it is necessary to include the layout parasitic effects. In our circuit microstrip Tee junctions should be used wherever stubs are connected to the circuit. We will find that the circuit is greatly sensitive to the TEE parasitic resulting in a dramatic degradation of the tuning range. As a result, an optimization needs to be developed. However, the ADS optimization tool is readily amenable to the optimization of the tuning area. A new optimization criteria will be presented in the chapter to overcome this handicap. Last but not the least, nonlinear effects will be investigated using harmonic balance and IMD (intermodulation distortion) results will be reported and discussed in this chapter.
4.1 Varactor Model

The varactors in the matching network are Aeroflex.Inc MGV07508 GaAs hyperabrupt varactor diodes. Since Aeroflex does not provide an ADS model, the diode model was used in ADS together with the model parameters of the spice model Aeroflex provided. Therefore, the first step is to verify that the model characteristics simulation is as the same as the data sheet from Aeroflex. Fig. 4.1 shows the capacitance value when voltage change. The DC voltage is from 2 to 20 volt and the capacitance is from 0.11 pF to 0.35 pF.

Figure 4.1 Characteristics of the varactor: Capacitance versus voltage from Aeroflex.Inc

Fig. 4.2 and Fig. 4.3 show the diode model characteristics obtained in ADS simulation. It indicates that after applying the parameter provided by Aeroflex, the diode
The model in ADS matches the data sheet from Aeroflex fairly very well. The main difference is that the voltage range of the physical diode is from 2 to 20 volt but the diode model simulation is only from 2 to 16 volt.

Figure 4.2 The topology of varactor model

\[ \text{Eqn 1: } C = \frac{1}{(2\pi \cdot \text{freq})^2 \cdot z} \]

Figure 4.3 Characteristics of the varactor: Capacitance versus Voltage in ADS.
4.2 Ideal Pi topology simulation

Since the algorithm in MATLAB is using ideal transmission line, in order to verify the results obtained in MATLAB, the first step in ADS uses ideal transmission lines for the simulations.

Figure 4.4 The ideal topology with ideal transmission line and ideal DC block.
Fig. 4.5 shows the reflection coefficient simulation result which exhibits a good match with the MATLAB results. In the next steps we gradually replace the ideal components by the physical component models that will be used or fabricated. Fig. 4.6 and Fig. 4.7 show the slightly degraded results obtained when we replace the ideal transmission lines by microstrip lines and replace the ideal DC block by a 27 pF capacitor.

Figure 4.6 Circuit using microstrip line and finite dc block capacitors.
However, when the microstrip Tee is added to the circuit, the tuning performance of the circuit is completely destroyed indicating that the circuit topology is very sensitive to the Tee junction parasitics. The circuit topology and the resulting mapping are shown in Fig. 4.8. and Fig. 4.9. The later figures shows an obvious collapse of the mapping area which makes the circuit useless. The optimization tool in ADS are used next to recover from this major handicap. Since our goal is an area, we can pick up the 4 edge points associated with the minimum and maximum tuning voltages to develop a cost function for the optimization. From the 4 edge points we can define 6 interconnecting lines. Next we will optimize these six lengths to approach as much as possible the values predicted by the ideal MATLAB model. The optimization syntax work very well and tune the circuit close to its ideal performance. The optimized result is shown in Fig. 4.9-10. In
addition the final circuit topology, circuit layout and fabricated circuit are shown in Fig. 4.11-12.

Figure 4.8 Matching network circuit using M Tee’s.
Figure 4.9 Mapping of the reflection coefficient after adding M Tee to the circuit.

Figure 4.10 Mapping of S11 figure after ADS optimization.
Figure 4.11 The final circuit used for generating the layout.

Figure 4.12 The layout of my design.
4.3 IMD – Intermodulation distortion analysis

In order to analyze the nonlinear effects in the varactor and the matching circuit, an IMD analysis is needed. Intermodulation distortion is a multi-tone distortion product generated when two or more tone signals are present at the input of a nonlinear device. Spurious intermodulation products are generated due to the nonlinear device. The circuit shown in Fig. 4.13 presents the topology with a two tone, two frequency input. The frequency of the two input excitations is 2.1 GHz and 1.9 GHz respectively.

Figure 4.13 Testbed topology for IMD analysis.
Figure 4.14 The output power in different frequency which show the intermodulation terms generated for various power using harmonic balance simulation.

Figure 4.15 The load voltage and current waveforms exhibit the expected signal beating effect.
Fig. 4.16 Fundamental and 3\textsuperscript{rd} order intermodulation signal results (top) and IMD difference (bottom) between the fundamental and the 3\textsuperscript{rd} order intermodulation product.
Figure 4.16 shows the IMD versus the input power. The IMD reduces below 25 dB when the input power is above 10 dBm. Note however that at 40 dBm the IMD is about 25 dBm. 40 dBm corresponds to the maximum power level for the power amplifier. However between 20 and 30 dB input power the IMD reduces to 15 dB. This indicates that some linearization will be required.
Chapter 5

Conclusion and Future Work

This thesis analyzed the Pi and T topologies for matching network realized using varactors. An optimization algorithm was developed in MATLAB to maximize the tuning area coverage. A varactor model was also implemented in ADS to verify the design using S-parameter and harmonic balance simulations. It was found that the MATLAB design is no longer applicable after MTee’s are added to the circuit. Thus a new optimization criteria was developed for optimizing the circuit in ADS. ADS simulations demonstrated that it is possible to approach the optimal tuning range predicted in MATLAB when accounting for the MTee’s in the circuit topology.

Further work for this research will include implementing the matching network together with the power amplifier, analyze the nonlinear response of the circuit, and perform the testing of the complete circuit.
Appendix A

Reflection Coefficient of Class B PAThat will be matched

Real Part:

-8.9519652e-01
-8.6050713e-01
-8.3212789e-01
-8.0820239e-01
-7.8404547e-01
-7.6180973e-01
-7.4310517e-01
-7.2700587e-01
-7.138197e-01
-7.0240159e-01
-6.9329234e-01
-6.8537345e-01
-6.7735680e-01
-6.6933462e-01
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