SIMULATION AND IMPLEMENTATION OF TWO-LEVEL AND THREE-LEVEL INVERTERS BY MATLAB AND RT-LAB

THESIS

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By

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Abstract

A power electronics device which converts DC power to AC power at required output voltage and frequency level is known as an inverter. Two categories into which inverters can be broadly classified are two level inverters and multilevel inverters. Some advantages that multilevel inverters have compared to two level inverters are minimum harmonic distortion, reduced EMI/RFI generation, and operation on several voltage levels. A multilevel inverter can be utilized for multipurpose applications, such as an active power filter, a static VAR compensator and a machine drive for sinusoidal and trapezoidal current applications. Some drawbacks to the multilevel inverters are the need for isolated power supplies for each one of the stages, the fact that they are a lot harder to build, they are more expensive, and they are more difficult to control in software.

This focus of this thesis is the simulation study of single phase, three phase, two-level, and three-level inverters. Full analysis for two-level and three-level inverter are included. Software packages MATLAB/SIMULINK and RT-LAB were used to study and simulate inverter waveforms in off time and in real time, respectively. Firstly, single phase and three phase inverters are modeled with resistive load and inductive load and their waveforms are observed. Secondly, a two-level inverter (single phase and three phase two-level inverter) is modeled by different ways and suitable switching control strategies (PWM technique) to carry out harmonic elimination. Thirdly, a three-level inverter (single phase and three phase three-level inverter) is modeled by different ways and
suitable switching control strategies (PWM technique) to carry out harmonic elimination. Finally, all inverters models are modeled and run in real time by using RT-LAB and the results in both cases (off time and real time) are the same. Two level and multilevel inverters in both cases for single-phase and three-phase are modeled, run and compared. It is formed that in both real time and off time the results were acceptable. Also, some derivations, such as thirteen segments of region 1 for each sector, nine segments of region 2 in each sector, seven segments of region 3 for each sector for three-level inverter, which have never been mentioned before, are derived and the switching sequence for each region in each sector is drawn.
Dedication

I wish to dedicate this thesis to my family:

   My son Yazed
   My daughter Arowa
   My daughter Tasneem

My mother, my wife, my older sister, my father, my friend Dan Aikens and his family thank you for your unending love, support, and above all for being my inspiration which made the completion of this thesis possible.
Acknowledgments

I wish to thank all those who helped me complete my M.S. in Electrical Engineering at the Ohio State University. I would like to thank Professor Longya Xu for giving me an opportunity to work on this thesis by supervising my research, serving as my major professor, providing valuable advice from time to time and for his guidance, encouragement, and support during my graduate study. I would like to thank Professor Jin Wang for serving on my thesis committee, and teaching ECE 624 and ECE793 which helped me towards my research. I would like to thank Professor Donald G. Kasten for his valuable ECE 740, ECE741 and ECE643 classes.

I would also like to thank my lab mates, Wang for his heartfelt support, and making my graduate school experience so much more enjoyable.

A special thanks to all my Libyan friends at The Ohio State University and my friend in Libya

Finally, I want to extend my deepest thanks and appreciation to my dear wife and my family for their never-ending support and kindness.
Vita

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Chapter 1: Introduction

1.1 Introduction: DC power can be converted into AC power at desired output voltage and frequency by using a power electronics device that is called an inverter. Industrial applications of inverters are for adjustable-speed AC drives, UPS (uninterruptible power supply), HVDC transmission lines and other. DC power inputs that inverters can use are power supply network or rotating alternator through rectifier, full cell, or photovoltaic array.

There are two common types of inverters, voltage source inverters (VSI) and current source inverters (CSI). When an inverter has a DC source with small or negligible impedance, which means the inverter has a stiff DC voltage source at its input terminal, it is called a VSI or voltage fed inverter (VFI). When the input DC source has a high impedance, which means the DC source has a stiff DC current source, the inverter is called a CSI or current fed inverter (CFI). In this chapter single phase and three phase voltage source inverters will be discussed along with their simulations.

1.2 Single-Phase Half-Bridge Inverter

The power circuit diagram of a single phase half bridge inverter is shown in Fig. 1.1
A half-bridge voltage source-inverter with resistive load can be considered as shown in Fig. 1.1 with representing load by only resistance. The circuit is operated by switching S1 (T1 & D1) and S2 (T2 & D2) alternatively at 50% duty cycle. It is seen that for $0 < t < \pi$, Transistor T1 conducts and the load is subjected $V_s/2$ due to the upper voltage source $V_s/2$. At $t = \pi$, transistor T1 is commutated and T2 is gated on. During the period $\pi < t < 2\pi$, transistor T2 conducts and the load is subjected to a voltage $(-V_s/2)$ due to the lower voltage source $V_s/2$. Fig. 1.2 shows simulation circuit by Matlab Simulink of a single phase half bridge inverter and Fig. 1.3 shows switching function, voltage, and current waveforms.
Figure 1.2 Single-Phase Half-Bridge Inverter Simulink circuit with resistive load
Fig. 1.3 The Gating Signals for transistors and the resulting output voltage and current waveforms (resistive load) for Half-Bridge Inverter
1.2.2 Single Phase Half Bridge Inverter with Inductive-Resistive Load

A half-bridge voltage source-inverter with inductive-resistive load can be considered as shown in Fig. 1.1 with representing load by only resistance and inductance. The circuit is operated by switching S1 (T1 & D1) and S2 (T2 & D2) alternatively at 50% duty cycle. To understand the operation of the circuit, the inverter is started by giving signal to T1. There was no current in any part of the circuit earlier. A signal to T1 turns it on and connects the load to upper Vs/2. A positive current develops form upper Vs/2 through T1 to load. During the time period $0 < t < \pi$ current through the load (through T1 and upper Vs/2) has grown from zero to $I_{\text{max}}$. The current will be reduced to zero through D2. T2 is forward biased now; the current grows in the negative direction and the current flows through D2, load, lower Vs/2 until the current falls to zero. Similarly, when T2 is turned off at $2\pi$, the load current flows through D1, load, and upper Vs/2. The energy will be fed back to DC source when D1, and D2 conduct. Fig. 1.4 shows simulation circuit by Matlab Simulink and Fig. 1.5 shows switching function, voltage, and current waveforms.
Figure 1.4 Single-Phase Half-Bridge Inverter Simulink circuit with inductive-resistive load
Fig. 1.5 The Gating Signals for transistors and the resulting output voltage and current waveforms (inductive-resistive load)
1.3 Single Phase Full-Bridge Inverter

The power circuit diagram of a single phase full bridge inverter is shown in Fig. 1.6. When T1 and T2 are connected, the input voltage $V_d$ appears across the load. If T3 and T4 are connected the voltage across the load is $-V_d$. Table 1.1 shows the main principle of a single phase full bridge inverter.

<table>
<thead>
<tr>
<th>Switching states</th>
<th>$V_{out}$</th>
<th>$I_{out}&gt;0$</th>
<th>$I_{out}&lt;0$</th>
</tr>
</thead>
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<tr>
<td>On   On   Off   Off</td>
<td>$V_S$</td>
<td>S1 and S2 conduct</td>
<td>D1 and D2 conduct</td>
</tr>
<tr>
<td>Off  Off  On   On</td>
<td>$-V_S$</td>
<td>D4 and D3 conduct</td>
<td>S3 and S4 conduct</td>
</tr>
<tr>
<td>On   Off  On   Off</td>
<td>0</td>
<td>S1 and D3 conduct</td>
<td>D1 and S3 conduct</td>
</tr>
<tr>
<td>Off  On   Off  On</td>
<td>0</td>
<td>D4 and S2 conduct</td>
<td>S4 and D2 conduct</td>
</tr>
<tr>
<td>Off  Off  Off  Off</td>
<td>$-V_S$</td>
<td>D4 and D3 conduct</td>
<td></td>
</tr>
<tr>
<td>Off  Off  Off  Off</td>
<td>$V_S$</td>
<td></td>
<td>D1 and D2 conduct</td>
</tr>
</tbody>
</table>

Figure 1.6 Single-Phase Full-Bridge Inverter
1.3.1 Single-Phase Full-Bridge Inverter with Resistive Load

A full-bridge voltage source-inverter with resistive load can be considered as shown in Fig. 1.6 with representing load by only resistance. The circuit is operated by switching S1, S2, S3, and S4. S1-S2 and S3-S4 are switched on and off at a 50% duty cycle. When T1 and T2 are connected, the input voltage $V_s$ appears across the load. If T3 and T4 are connected the voltage across the load is $-V_s$. Table 1.1 can be considered the operation table for a single-phase full-bridge Inverter with resistive load. Fig. 1.7 shows simulation circuit by Matlab Simulink and Fig. 1.8 shows switching function, voltage, and current waveforms.

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1.3.2 Single Phase Full-Bridge Inverter with Inductive-Resistive Load

A full-bridge voltage source-inverter with inductive-resistive load can be considered as shown in Fig. 1.6 with representing load by only resistance and inductance. The circuit is operated by switching S1, S2, S3, and S4. S1-S3 and S2-S4 are switched on and off at a 50% duty cycle. When T1 and T2 are connected, the input voltage Vs appears across the load. If T3 and T4 are connected, the voltage across the load is –Vs. Fig. 1.9 shows simulation circuit by Matlab Simulink and Fig. 1.10 shows switching function, voltage, and current waveforms.

![Simulation Circuit by Matlab Simulink for Full-Bridge Inverter with Inductive-Resistive Load](image)

Figure 1.9 Simulation Circuit by Matlab Simulink for Full-Bridge Inverter with Inductive-Resistive Load
Fig. 1.10 The Gating Signals for transistors and the resulting output voltage and current waveforms (inductive-resistive load)
1.4 Three-Phase Inverter

A three phase inverters are used to provide industrial applications by adjustable frequency power. Three phase inverters are more common than single phase inverters. DC supply for three phase inverters is taken from a battery or usually from a rectifier.

A six steps bridge is used for three phase inverter by using six switches, two switches for each phase. Each step is defined as a change in the time operation for each transistor to the next transistor in proper sequence. For one cycle $360^\circ$, each step would be of $60^\circ$ interval for a six step inverter. Fig. 1.11 shows the power circuit diagram of a three phase bridge inverter using six IGBTs. Large capacitors are connected at the input terminal to make the DC input constant and also suppress the harmonics fed back to the source.

![Figure 1.11 The power circuit diagram of a three phase bridge inverter using six IGBTs](image-url)
There are two patterns of gating transistors. In one pattern, each transistor conducts for 180° and in the other, each transistor conducts 120°. But both patterns’ gating signals are applied and removed at 60° intervals of the output voltage waveform. Both modes require a six step bridge inverter.

1.4.1 Three-Phase 180° Degree Mode VSI

By referring to Fig. 1.11, each switch conducts for 180° of a cycle. Transistor pair in each arm, i.e. T1, T4; T3, T6 and T5, T2 are turned on with a time interval of 180°. It means that T1 conducts for 180° and T4 for the next 180° of a cycle. Transistors in the upper group i.e. T1, T3, and T5 conduct at an interval of 120°. It implies that if T1 is operated at $\omega t = 0^\circ$, then T3 must be operated at $\omega t = 120^\circ$ and T5 at $\omega t = 240^\circ$, the same thing for lower group of transistors. Table 1.2 shows the switching states for six switches. Fig. 1.12 shows simulation circuit for three phase inverter for 180° mode.

Table 1.2 Switching states for Three-Phase Voltage Source Inverter 180° Degree conduction

<table>
<thead>
<tr>
<th>State No.</th>
<th>S1</th>
<th>S2</th>
<th>S3</th>
<th>S4</th>
<th>S5</th>
<th>S6</th>
<th>$V_{ab}$</th>
<th>$V_{bc}$</th>
<th>$V_{ca}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>On</td>
<td>On</td>
<td>Off</td>
<td>Off</td>
<td>Off</td>
<td>On</td>
<td>$V_S$</td>
<td>0</td>
<td>-$V_S$</td>
</tr>
<tr>
<td>2</td>
<td>On</td>
<td>On</td>
<td>On</td>
<td>Off</td>
<td>Off</td>
<td>Off</td>
<td>0</td>
<td>$V_S$</td>
<td>-$V_S$</td>
</tr>
<tr>
<td>3</td>
<td>Off</td>
<td>On</td>
<td>On</td>
<td>On</td>
<td>Off</td>
<td>Off</td>
<td>-$V_S$</td>
<td>$V_S$</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>Off</td>
<td>Off</td>
<td>On</td>
<td>On</td>
<td>On</td>
<td>Off</td>
<td>-$V_S$</td>
<td>0</td>
<td>$V_S$</td>
</tr>
<tr>
<td>5</td>
<td>Off</td>
<td>Off</td>
<td>Off</td>
<td>On</td>
<td>On</td>
<td>On</td>
<td>0</td>
<td>-$V_S$</td>
<td>$V_S$</td>
</tr>
<tr>
<td>6</td>
<td>On</td>
<td>Off</td>
<td>Off</td>
<td>Off</td>
<td>On</td>
<td>On</td>
<td>$V_S$</td>
<td>-$V_S$</td>
<td>0</td>
</tr>
<tr>
<td>7</td>
<td>On</td>
<td>Off</td>
<td>On</td>
<td>Off</td>
<td>On</td>
<td>Off</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>8</td>
<td>Off</td>
<td>On</td>
<td>Off</td>
<td>On</td>
<td>Off</td>
<td>On</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>
Fig. 1.13 shows waveforms for phase to neutral voltage and line to line voltage waveforms. Fig. 1.14 shows source block parameters for 180° degree pulses.
Figure 1.13 Voltage waveforms for 180° mode 3-phase VSI
1.4.2 Three-Phase 120° Degree Mode VSI

The power circuit diagram of this inverter is the same as shown in Fig. 1.11. For the 120° degree mode VSI, each transistor conducts for 120° of a cycle. Like 180° mode, 120° mode inverter also requires six steps, each of 60° duration, for completing one cycle of the output AC voltage.

In first 120° T1 conducts with T6 for 60° then conducts with T2 for another 60°. T3 will conducts for 120° (from 120° to 240°) 60° (from 120° to 180°) with T2 and then conducts another 60° (from 180° to 240°) with T4. T5 will conducts 120° (from 240° to 360°) 60° (from 240° to 300°) and then conducts for another 60° (from 300° to 360°) with T6. The conduction sequence can be written as follows:

T6T1, T1T2, T2T3, T3T4, T4T5, T5T6, and T6T1
Fig. 1.15 shows simulation circuit for Three-Phase Inverter for 120° mode.

![Simulink Matlab circuit for Three-Phase Inverter 120° mode VSI](image)

**Figure 1.15 Simulink Matlab circuit for Three-Phase Inverter 120° mode VSI**

Fig. 1.16 shows waveforms for phase to neutral voltage and line to line voltage waveforms. Fig. 1.17 shows source block parameters for 120° degree pulses.
Figure 1.13 Voltage waveforms for 180° mode Three-Phase VSI
1.5 Three-Phase Inverter Application

The basic operation of the six step voltage inverter can be understood by considering the inverter to effectively consist of six mechanical switches as shown in Fig. 1.18. While it is possible to energize the motor by having only two switches closed in sequence at one time it is now accepted that it is preferable to have three consecutive switches closed at any instant. Three-Phase bridge inverters are a natural extension of the single-phase full bridge circuit. It uses three legs instead of two legs. The switching signals of each inverter leg will now be displaced by 120° with respect to the adjacent legs. The line to line voltage will then be determined by the potential

Figure 1.17 Source block parameters for 120° degree pulses
differences between the output terminals of each leg and will also have the phase displacement of 120°. Three-Phase Inverter with ideal switch as shown in Fig. 1.18.

Figure 1.18 Three-Phase Inverter with ideal switch
Switching function for the circuit diagram in Fig. 1.18 are shown in Fig. 1.19 and circuit model was used in the simulation (Fig 1.20) shows six ideal switches, two for each leg of the inverter. In order to produce an AC voltage, switches in the pairs S1, S4 and S3, S6 and S5, S2 should be switched ON for equal duration. For instance, in this simulation S1 will be ON for 180° (half cycle) and S4 will be ON for the next half cycle. Since this inverter is intended to generate a three phase symmetrical set of

Figure 1.19 Switching function for switches in figure 1.18
voltages, gating signals for any two legs are displaced 120°. That can be explained by Fig. 1.21 which shows the switching functions were used as gating signals for the switches. It can be noticed that for each one-sixth of the cycle (60°) one switch in each leg will be ON, that means only three switches will be ON for the 60° period. The control circuit was used to supply the switching signals is shown in Fig.20.

Figure 1.20 Control Circuit to generate the desired switching functions
Figure 1.21 Simulink circuit Model for subsystem in figure 1.20
The inverter line to neutral voltage and line to line voltage waveforms are shown in Fig. 1.22. It shows a six-step-shape ac waveform, each step has a width of one-sixth of a cycle (60°) and a height of one-third of the input DC voltage for line to neutral voltage.

![Waveforms for line to neutral and line to line inverter output voltages](image)

**Figure 1.22 Waveforms for line to neural and line to line inverter output voltages**

### 1.5.1 Output Current

The three phase load, which was connected to the output of the inverter, has back emf, 60 Hz. Note that harmonics of orders three and multiples of three are absent from both the line to line and line to neutral voltages (and consequently absent from the currents).

The load current waveform is dependent of the phase difference between the back emf (denoted $V_{An}$ for phase A) and the fundamental component of the inverter output voltage (denoted $V_{an}$ for phase-a).

Since the system has balanced currents in phases b and c which can be obtained by adding 120° and 240° phase shift respectively with respect to the current of phase a. It is observed that it is required to run the simulation for more than 15 seconds to obtain a steady state waveform.
Fig. 1.23 shows the current waveforms for phases a, b, and c for the case in which the fundamental component of Van is **in phase** with V\textsubscript{an}.

![Current Waveforms for Phases a, b, and c](image)

Figure 1.23 The current waveforms for phases a, b, and c for the case in which the fundamental component of Van is in phase with V\textsubscript{an}.

Fig. 1.24 illustrate the current waveform for phases a, b, and c for the case in which the fundamental component of Van **leads** V\textsubscript{an} by 90°.
Figure 1.24 The current waveform for phases a, b, and c for the case in which the fundamental component of $V_{an}$ leads $V_{an}$ by 90°.

Fig. 1.35 shows the current waveform for phases a, b, and c for the case in which the fundamental component of $V_{an}$ lags $V_{an}$ by 90°.
1.6 Experimental Results

1.6.1 Single-Phase Full-Bridge inverter with R-L load

This section contains selected results, verified experimentally on the laboratory configurations of the single phase full bridge inverter with R-L load by using RT-Lab (see appendix A). The inverter switches that were used for the configurations were power IGBTs. Fig 1.26 shows the main circuit was used in the Lab for a single phase full bridge inverter and Fig 1.27 shows Circuit Subsystem sm_maincircuit in Fig 1.26. Fig 1.28 shows Circuit Subsystem sc_output in Fig 1.26 and Fig 1.29 shows output current and voltage for single phase inverter by RT-LAP. As in the case of the single phase full bridge inverters results by Matlab, the results by both RT-Lab and Matlab are almost the same.

Figure 1.25 The current waveform for phases a, b, and c for the case in which the fundamental component of $V_a$ lags $V_a$ by $90^\circ$.
Figure 1.26 Main circuit for single phase inverter by RT-LAB

Figure 1.27 Subsystem Circuit sm_maincircuit in Figure 1.26
Figure 1.28 Subsystem Circuit sc_output in Figure 1.26

Figure 1.29 Outputs current and voltage for single phase inverter by RT-LAP
1.5.2 Three-Phase Inverter feed three phase R-L load with lagging 90°

This section contains selected results, verified experimentally on the laboratory configurations of the three phase inverter feed three phase R-L load with lagging 90° by using RT-Lab (see appendix A). The inverters switches that were used for the configurations were power IGBTs. Fig 1.30 shows the main circuit was used in the Lab for a Three-Phase Inverter feed three phase R-L load with lagging 90° and Fig 1.31 shows Circuit Subsystem sm_maincircuit in Fig 1.30. Fig 1.32 shows Circuit Subsystem sc_output in Fig 1.30 and Fig 1.33 shows line-to-neutral output voltage for Three-Phase Inverter feed three phase R-L load with lagging 90°. Fig 1.34 shows three phase output current for Three-Phase Inverter feed three phase R-L load with lagging 90° by RT-LAP. As in case of Three-Phase Inverter feed three phase R-L load with lagging 90° results by Matlab, the results by both RT-Lab and Matlab almost the same.

Figure 1.30 Main circuit for three phase inverter feed three phase R-L load with lagging 90° by RT-LAB
Figure 1.31 Subsystem Circuit sm_maincircuit in Figure 1.30
Figure 1.32 Subsystem Circuit sc_output in Figure 1.30

Figure 1.33 Output line-to-neutral voltage for three phase inverter feed three phase R-L load with lagging 90° by RT-LAB
Figure 1.34 Output three phase current for three phase inverter feed three phase R-L load with lagging 90° by RT-LAB
1.7 Conclusion

This chapter investigates and successfully simulates and implements single phase and three phase inverters with their application. A brief review of the operating principles of single phase and three-phase are provided and experimental modules are shown. The single phase and the three phase inverters configurations were individually modeled by Matlab and selected results were verified experimentally by TR-LAB. Waveforms for the voltage-source inverters, either single phase or three phase configurations, were figured out in off time by Matlab and in real time by RT-LAB. The whole simulated models of the main circuit and the sub-circuit were made for both single phase and three phase inverters. The obtained results in both cases (Matlab and RT-LAB) had approximately the same shape. Single phase and three phase inverters were tested with resistive load and inductive-resistive load by Matlab. It is recommended that harmonics for single phase and three phase inverters should be simulated and implemented by Matlab and RT-LAB in the future to gain a deeper understanding of the off time and real time behaviors of both single phase and three phase inverters.
Chapter 2: Two Level Inverter Analysis and Simulations

2.1 Introduction: - A voltage source inverter (VSI) is used to convert a fixed DC voltage to three phase AC voltage. The circuit diagram for a two-level voltage source inverter for power applications is shown in Fig. 2.1.

![Figure 2.1 circuit diagram for two-level inverter](image)

The inverter is composed of six groups of active switches, S1 to S6. Depending on the DC operating voltage of the inverter, each switch is an IGBT switching device. This part focuses on pulse width modulation (PWM) schemes for two-level inverter and analysis on space vector modulation (SVM) algorithms. Space Vector modulation (SVM) technique was originally developed as a vector approach to pulse-width modulation (PWM) for three-phase inverters. It is a more sophisticated technique for generating a sine wave that provides a higher voltage to the motor with lower total harmonic distortion. It confines space vectors to be applied according to the region where the output voltage vector is located. A different approach to PWM modulation is based on the space vector representation of voltage in the $\alpha,\beta$ plane. The $\alpha,\beta$ components are
found by transformations. The determination of the switching instant may be achieved using space vector modulation technique based on the representation of switching vectors in $\alpha,\beta$ plane. The Space Vector modulation technique is an advanced, computation intensive PWM technique and is possibly the best among all the PWM techniques for drives applications. Because of its superior performance characteristics, it is been finding wide spread application in recent years. The purpose of this chapter is to present the space vector modulation technique and then to simplify the explanation of how it can be implemented by using Matlab software packages (off time) and RT-LAB (real time).

2.2 Space Vector Modulation

Space vector modulation (SVM) is one of the preferred real-time modulation techniques and is widely used for voltage source inverters.

2.2.1 Switching States

The operating status of the switches in the two-level inverter in Fig. 2.1 can be represented by switching states. As indicated in Table 2.1, switching state ‘1’ denotes that the upper switch in an inverter leg is on and the inverter terminal voltage ($V_{an}$, $V_{bn}$, $V_{cn}$) is positive ($+V_d$) while ‘0’ indicates that the inverter terminal voltage is zero due to the conduction of the lower switch. There are eight possible combinations of switching states in the two-level inverter as listed in Table 2.2. The switching state [100], for example, corresponds to the conduction of $S_1$, $S_6$, and $S_2$ in the inverter legs $A$, $B$, and $C$, respectively. Among the eight switching states, [111] and [000] are zero states and the others are active states.
Table 2.1 Definition of Switching States

<table>
<thead>
<tr>
<th>Switching state</th>
<th>Leg A</th>
<th>Leg B</th>
<th>Leg C</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>S1</td>
<td>S4</td>
<td>Van</td>
</tr>
<tr>
<td>1</td>
<td>On</td>
<td>Off</td>
<td>Vd</td>
</tr>
<tr>
<td>0</td>
<td>Off</td>
<td>On</td>
<td>0</td>
</tr>
</tbody>
</table>

Table 2.2 Space Vectors, Switching States, and On-State Switches

<table>
<thead>
<tr>
<th>Space Vector</th>
<th>Switching State (Three Phases)</th>
<th>On-State Switch</th>
<th>Vector Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Zero Vector</td>
<td>$\tilde{V}_0$</td>
<td>$[1\ 1\ 1]$</td>
<td>$S1, S3, S5$</td>
</tr>
<tr>
<td></td>
<td>$[0\ 0\ 0]$</td>
<td>$S4, S6, S2$</td>
<td></td>
</tr>
<tr>
<td>Active Vector</td>
<td>$\tilde{V}_1$</td>
<td>$[1\ 0\ 0]$</td>
<td>$S1, S6, S2$</td>
</tr>
<tr>
<td></td>
<td>$\tilde{V}_2$</td>
<td>$[1\ 1\ 0]$</td>
<td>$S1, S3, S2$</td>
</tr>
<tr>
<td></td>
<td>$\tilde{V}_3$</td>
<td>$[0\ 1\ 0]$</td>
<td>$S4, S3, S2$</td>
</tr>
<tr>
<td></td>
<td>$\tilde{V}_4$</td>
<td>$[0\ 1\ 1]$</td>
<td>$S4, S3, S5$</td>
</tr>
<tr>
<td></td>
<td>$\tilde{V}_5$</td>
<td>$[0\ 0\ 1]$</td>
<td>$S4, S6, S5$</td>
</tr>
<tr>
<td></td>
<td>$\tilde{V}_6$</td>
<td>$[1\ 0\ 1]$</td>
<td>$S1, S6, S5$</td>
</tr>
</tbody>
</table>

2.2.2 Space Vectors Concept

The concept of space vectors is derived from the rotating field of AC machine which is used for modulating the inverter output voltage. In this modulation technique the three phase quantities can be transformed to their equivalent 2-phase quantity either in synchronously rotating frame or stationary frame. From this 2-phase component the reference vector magnitude can be found and used for modulating the inverter output.
The process for obtaining the rotating space vector is explained in the following section, considering the stationary reference frame.

The active and zero switching states can be represented by active and zero space vectors, respectively. A typical space vector diagram for the two-level inverter is shown in Fig. 2.2, where the six active vectors $\vec{V}_1$ to $\vec{V}_6$ form a regular hexagon with six equal sectors (I to VI). The zero vector $\vec{V}_0$ lies on the center of the hexagon.

For the two-level inverter in Fig. 2.1. Assuming that the operation of the inverter is three-phase balanced, we have

$$V_{ao} + V_{bo} + V_{co} = 0$$

(2.1)

Where $V_{ao}$, $V_{bo}$, and $V_{co}$ are the instantaneous load phase voltages. From a mathematical point of view, one of the phase voltages is redundant when given any two phases.

Let the three phase sinusoidal voltage component be,

$$V_a = V_m \sin \omega t$$
$$V_b = V_m \sin (\omega t - 2\pi / 3)$$
$$V_c = V_m \sin (\omega t - 4\pi / 3)$$

(2.2)

When these 3-phase voltages are applied to the AC machine, they produce a rotating flux in the air gap of the AC machine. This rotating flux component can be represented as a single rotating voltage vector. The magnitude and angle of the rotating vector can be found by the mean of Clark’s Transformation as will be explained in the stationary reference frame. The representation of rotating vector in complex plane is shown in Fig 2.3.
Figure 2.2 Space vector diagram for two-level inverter.

\[ \vec{V}_{\text{ref}} = V_\alpha + jV_\beta = \frac{2}{3} (V_a + aV_b + a^2V_c) \]  

(2.3)

Where

\[ a = e^{j2\pi/3} \]

\[ |\vec{V}_{\text{ref}}| = \sqrt{V_\alpha^2 + V_\beta^2}, \quad \alpha = \tan^{-1}\left(\frac{V_\beta}{V_\alpha}\right) \]  

(2.4)

\[ V_\alpha + jV_\beta = \frac{2}{3} \left( V_a + e^{j\frac{2\pi}{3}} V_b + e^{-j\frac{2\pi}{3}} V_c \right) \]  

(2.5)

\[ V_\alpha + jV_\beta = \frac{2}{3} \left( V_a + \cos \frac{2\pi}{3} V_b + \cos \frac{2\pi}{3} V_c \right) + j \frac{2}{3} \left( \sin \frac{2\pi}{3} V_b - \sin \frac{2\pi}{3} V_c \right) \]
Equating real and imaginary parts:

\[
V_\alpha = \frac{2}{3} \left( V_a + \cos \frac{2\pi}{3} V_b + \cos \frac{2\pi}{3} V_c \right) \tag{2.6}
\]

\[
V_\beta = \frac{2}{3} \left( 0 V_a + \sin \frac{2\pi}{3} V_b - \sin \frac{2\pi}{3} V_c \right) \tag{2.7}
\]

\[
\begin{bmatrix}
V_d \\
V_q
\end{bmatrix} = \frac{2}{3} \begin{bmatrix}
1 & \cos \frac{2\pi}{3} & \cos \frac{2\pi}{3} \\
0 & \sin \frac{2\pi}{3} & -\sin \frac{2\pi}{3}
\end{bmatrix}
\begin{bmatrix}
V_a \\
V_b \\
V_c
\end{bmatrix} \tag{2.8}
\]

### 2.2.3 Principle of Space Vector PWM

- Treats the sinusoidal voltage as a constant amplitude vector rotating at constant frequency.
- This PWM technique approximates the reference voltage \( V_{\text{ref}} \) by a combination of the eight switching patterns (\( V_0 \) to \( V_7 \)).
- Coordinate Transformation (\( abc \) reference frame to the stationary \( d-q \) frame): A three-phase voltage vector is transformed into a vector in the stationary \( d-q \) coordinate frame which represents the spatial vector sum of the three-phase voltage.

### 2.2.4 Realization of Space Vector PWM

The space vector PWM is realized based on the following steps:

Step 1. Determine \( V_d, V_q, V_{\text{ref}}, \) and angle \( \alpha \).

Step 2. Determine time duration \( T_1, T_2, T_0 \).

Step 3. Determine the switching time of each transistor (S1 to S6).
A. Determine $V_d$, $V_q$, $V_{ref}$, and Angle ($\alpha$):

Coordinate transformation: abc to dq. The Voltage Space vector and its components in dq plane is shown in Fig. 2.3

\[
\begin{align*}
V_d &= V_{an} - V_{bn} \cdot \cos 60 - V_{cn} \cdot \cos 60 \\
&= V_{an} - \frac{1}{2} V_{bn} - \frac{1}{2} V_{cn} \\
V_q &= 0 - V_{bn} \cdot \cos 30 - V_{cn} \cdot \cos 30 \\
&= -\frac{1}{2} V_{bn} - \frac{\sqrt{3}}{2} V_{cn} \\
\therefore \begin{bmatrix} V_d \\ V_q \end{bmatrix} &= \begin{bmatrix} 1 & -\frac{1}{2} \\ \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} \\
V_{ref} &= \sqrt{V_d^2 + V_q^2} \\
\alpha &= \tan^{-1} \left( \frac{V_q}{V_d} \right) = \omega_S t = 2 \pi f_s t
\end{align*}
\]

where $f_s$ Fundamental frequency

The voltage $V_d$, $V_q$, $V_{ref}$, and angle $\alpha$ are calculated by using the above equations.
The three phase output voltages in the full bridge inverter at any instant of time in Fig. 2.1 can be represented by a set of eight base space vectors according to eight switching positions of the inverter. Fig. 2.2 shows these base vectors $V_1$ through $V_6$ and the two zero vectors which correspond to switching positions resulting in zero output voltage.

**B- Determine Time Duration $T_1$, $T_2$, $T_Z$:**

With considering that $T_Z$ is sufficiently small, then the reference voltage $\tilde{V}_{ref}$ could be constant during $T_Z$. When the reference voltage $\tilde{V}_{ref}$ falls into sector I as shown in Fig. 2.4 the reference voltage $\tilde{V}_{ref}$ can be found by two adjacent active vectors $\tilde{V}1$ and $\tilde{V}2$ and one zero vector $\tilde{V}0$ and the equation of the reference voltage $\tilde{V}_{ref}$ can be written as follows:-

$$\begin{align*}
\tilde{V}_{ref} &= \tilde{V}_1 \frac{T_1}{T_Z} + \tilde{V}_2 \frac{T_2}{T_Z} + \tilde{V}_0 \frac{T_0}{T_Z} \\
\tilde{V}_{ref} &= \tilde{V}_1 T_1 + \tilde{V}_2 T_2 + \tilde{V}_0 T_0
\end{align*}$$

(2.11)

Where $$T_Z = T_1 + T_2 + T_0$$

$T_1$, $T_2$, and $T_0$ the time for $\tilde{V}1$ and $\tilde{V}2$ and $\tilde{V}0$ respectively. Therefore, the space vector can be written as follows:-

$$\begin{align*}
\tilde{V}_{ref} &= \tilde{V}_{ref} e^{j\theta} \\
\tilde{V}_1 &= \frac{2}{3} V_d \\
\tilde{V}_2 &= \frac{2}{3} V_d e^{j\pi/3} \\
\tilde{V}_0 &= 0
\end{align*}$$

$$T_z |\tilde{V}_{ref}| \begin{bmatrix} \cos(\alpha) \\ \sin(\alpha) \end{bmatrix} = T_1 \frac{2}{3} V_{dc} \begin{bmatrix} 1 \\ 0 \end{bmatrix} + T_2 \frac{2}{3} V_{dc} \begin{bmatrix} \cos(\pi / 3) \\ \sin(\pi / 3) \end{bmatrix}$$

(2.12)
Figure 2.4 Reference vector as a combination of adjacent vectors at sector 1

By solving the above equations, $T_1$ and $T_2$ can be expressed as below:

$$
\begin{align*}
\text{Real part} & \quad T_Z V_{\text{ref}} \cos(\alpha) = T_1 \frac{2}{3} V_{dc} + T_2 \frac{1}{3} V_{dc} \\
\text{Imaginary part} & \quad T_Z V_{\text{ref}} \sin(\alpha) = T_2 \frac{1}{\sqrt{3}} V_{dc}
\end{align*}
$$

(2.13)

By solving the above equations, $T_1$ and $T_2$ can be expressed as below:

$$
\begin{align*}
\therefore T_1 &= T_z \cdot a \cdot \sin(\pi / 3 - \alpha) \\
\therefore T_2 &= T_z \cdot a \cdot \sin(\alpha)
\end{align*}
$$

(2.14)
Where \( 0 \leq \alpha \leq 60 \)
\[
a = \frac{\sqrt{3} V_{\text{ref}}}{V_{dc}} \quad \text{modulation index}
\]
\[
T_z = \frac{1}{f}
\]

Where \( T_1, T_2, T_0 \) represent the time widths for vectors \( V1, V2, V0 \). \( T0 \) is the period in a sampling period for null vectors should be filled. As each switching period (half of sampling period) \( Tz \) starts and ends with zero vectors i.e. there will be two zero vectors per \( Tz \) or four null vectors per \( Tz \), duration of each null vector is \( Tz/4 \). Figure 2.5 to Figure 2.7 gives switching pattern for all sectors. Table 2.3 shows switching sequence table for each sector.

### 2.2.5 Switching Time Duration at Any Sector:

\[
T_1 = \frac{\sqrt{3} \cdot T_z \cdot V_{\text{ref}}}{V_{dc}} \left( \sin \left( \pi - \alpha + \frac{n-1}{3} \pi \right) \right) = \frac{\sqrt{3} \cdot T_z \cdot V_{\text{ref}}}{V_{dc}} \left( \sin \frac{n}{3} \pi \cos \alpha - \cos \frac{n}{3} \pi \sin \alpha \right)
\]

\[
T_2 = \frac{\sqrt{3} \cdot T_z \cdot V_{\text{ref}}}{V_{dc}} \left( \sin \left( \alpha - \frac{n-1}{3} \pi \right) \right) = \frac{\sqrt{3} \cdot T_z \cdot V_{\text{ref}}}{V_{dc}} \left( - \cos \alpha \sin \frac{n-1}{3} \pi + \sin \alpha \cos \frac{n-1}{3} \pi \right)
\]

\[
T_z = T_1 + T_2 + T_0
\]

Where \( n = 1 \) through 6 ( that is sector 1 to 6 )
\[
0 \leq \alpha \leq 60^o
\]

Figures 2.5, 2.6, and 2.7 show Space Vector PWM switching patterns for all sectors. Table 2.3 shows times \( T_1, T_2 \) and \( T_0 \) for all sectors and Table 2.4 shows Switching sequence time for each switch in each leg.
2.2.6 Determine The Switching Time For Each Switch (S1 To S6):

Figure 2.5 Space Vector PWM switching patterns at (a) sector I and (b) sector II.
Figure 2.6 Space Vector PWM switching patterns at (a) sector III and (b) sector IV
Figure 2.7 Space Vector PWM switching patterns at (a) sector V and (b) sector VI
### Table 2.3 Times $T_1$, $T_2$ and $T_0$ for all sectors

<table>
<thead>
<tr>
<th>Sector</th>
<th>$T_1$</th>
<th>$T_2$</th>
<th>$T_0$</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>$T_z a \sin \left( \frac{\pi}{3} - \alpha \right)$</td>
<td>$T_z a \sin(\alpha)$</td>
<td>$T_z - T_1 - T_2$</td>
</tr>
<tr>
<td>II</td>
<td>$T_z a \sin \left( \frac{2\pi}{3} - \alpha \right)$</td>
<td>$T_z a \sin \left( \alpha - \frac{\pi}{3} \right)$</td>
<td>$T_z - T_1 - T_2$</td>
</tr>
<tr>
<td>III</td>
<td>$T_z a \sin(\pi - \alpha)$</td>
<td>$T_z a \sin \left( \alpha - \frac{2\pi}{3} \right)$</td>
<td>$T_z - T_1 - T_2$</td>
</tr>
<tr>
<td>IV</td>
<td>$T_z a \sin \left( \frac{4\pi}{3} - \alpha \right)$</td>
<td>$T_z a \sin(\alpha - \pi)$</td>
<td>$T_z - T_1 - T_2$</td>
</tr>
<tr>
<td>V</td>
<td>$T_z a \sin \left( \frac{5\pi}{3} - \alpha \right)$</td>
<td>$T_z a \sin \left( \alpha - \frac{4\pi}{3} \right)$</td>
<td>$T_z - T_1 - T_2$</td>
</tr>
<tr>
<td>VI</td>
<td>$T_z a \sin(2\pi - \alpha)$</td>
<td>$T_z a \sin \left( \alpha - \frac{5\pi}{3} \right)$</td>
<td>$T_z - T_1 - T_2$</td>
</tr>
</tbody>
</table>

### Table 2.4 Switching sequence table for each switch in each leg

<table>
<thead>
<tr>
<th>Sector</th>
<th>Upper Switches (S1, S3, S5)</th>
<th>Lower Switches (S4, S6, S2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>S1 = $T_1 + T_2 + T_0 / 2$</td>
<td>S4 = $T_0 / 2$</td>
</tr>
<tr>
<td></td>
<td>S3 = $T_2 + T_0 / 2$</td>
<td>S6 = $T_1 + T_0 / 2$</td>
</tr>
<tr>
<td></td>
<td>S5 = $T_0 / 2$</td>
<td>S2 = $T_1 + T_2 + T_0 / 2$</td>
</tr>
<tr>
<td>2</td>
<td>S1 = $T_1 + T_0 / 2$</td>
<td>S4 = $T_2 + T_0 / 2$</td>
</tr>
<tr>
<td></td>
<td>S3 = $T_1 + T_2 + T_0 / 2$</td>
<td>S6 = $T_0 / 2$</td>
</tr>
<tr>
<td></td>
<td>S5 = $T_0 / 2$</td>
<td>S2 = $T_1 + T_2 + T_0 / 2$</td>
</tr>
<tr>
<td>3</td>
<td>S1 = $T_0 / 2$</td>
<td>S4 = $T_1 + T_2 + T_0 / 2$</td>
</tr>
<tr>
<td></td>
<td>S3 = $T_1 + T_2 + T_0 / 2$</td>
<td>S6 = $T_0 / 2$</td>
</tr>
<tr>
<td></td>
<td>S5 = $T_2 + T_0 / 2$</td>
<td>S2 = $T_1 + T_0 / 2$</td>
</tr>
<tr>
<td>4</td>
<td>S1 = $T_0 / 2$</td>
<td>S4 = $T_1 + T_2 + T_0 / 2$</td>
</tr>
<tr>
<td></td>
<td>S3 = $T_1 + T_0 / 2$</td>
<td>S6 = $T_2 + T_0 / 2$</td>
</tr>
<tr>
<td></td>
<td>S5 = $T_1 + T_2 + T_0 / 2$</td>
<td>S2 = $T_0 / 2$</td>
</tr>
<tr>
<td>5</td>
<td>S1 = $T_2 + T_0 / 2$</td>
<td>S4 = $T_1 + T_0 / 2$</td>
</tr>
<tr>
<td></td>
<td>S3 = $T_0 / 2$</td>
<td>S6 = $T_1 + T_2 + T_0 / 2$</td>
</tr>
<tr>
<td></td>
<td>S5 = $T_1 + T_2 + T_0 / 2$</td>
<td>S2 = $T_0 / 2$</td>
</tr>
<tr>
<td>6</td>
<td>S1 = $T_1 + T_2 + T_0 / 2$</td>
<td>S4 = $T_0 / 2$</td>
</tr>
<tr>
<td></td>
<td>S3 = $T_0 / 2$</td>
<td>S6 = $T_1 + T_2 + T_0 / 2$</td>
</tr>
<tr>
<td></td>
<td>S5 = $T_1 + T_0 / 2$</td>
<td>S2 = $T_2 + T_0 / 2$</td>
</tr>
</tbody>
</table>
2.2.7 Switching Sequence

By selecting the space vectors and their times calculated, switching sequence is going to be the next step to arrange. Generally, $V_{\text{ref}}$ is not unique because of the switching sequence design, but the following two requirements for the minimization of the device switching frequency should be satisfied:

(a) By involving only two switches in the same inverter leg, one is switched on and the other switched off at any time.

(b) No or minimum number of switchings is required to move $V_{\text{ref}}$ from sector to the next in the vector diagram.

A typical seven-segment switching sequence and inverter output voltage waveforms for $V_{\text{ref}}$ in sector I is shown in Fig. 2.8, where $V_1$, $V_2$ and $V_0$ synthesize $V_{\text{ref}}$. The sampling period $T_z$ for the selected vectors can be divided into seven segments. The following can be observed:

- The total time for the seven segments equals to $(T_z = T_1 + T_2 + T_0)$.
- Design requirement (a) is satisfied. For instance, the transition from [000] to [100] is accomplished by turning $S_1$ on and $S_4$ off, which involves only two switches.
- The redundant switching states for $V_0$ are utilized to reduce the number of switchings per sampling period. For the $T_{0/4}$ segment in the center of the sampling period, the switching state [111] is selected, while for the $T_{0/4}$ segments on both sides, the state [000] is used.
- Each of the switches in the inverter turns on and off once per sampling period.

The switching frequency $f_{\text{sw}}$ of the devices is thus equal to the sampling frequency.
fsp, that is, \( f_{sw} = f_{sp} = 1/T_s \).

Figure 2.8 Seven-segment switching sequence for \( V_{\text{ref}} \) in sector I.
Obviously, there are two possible switching directions for each sector, clockwise and counter clockwise. However, only one direction each sector has as shown in Fig. 2.9

Table 2.4 gives the seven-segment switching sequences for Vref residing in all six sectors. Note that all the switching sequences start and end with switching state [000], which indicates that the transition for Vref moving from one sector to the next does not require any switchings.

Table 2.5 seven-segments switching sequence for all sector

<table>
<thead>
<tr>
<th>Sector</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
</tr>
</thead>
<tbody>
<tr>
<td>I.</td>
<td>$\tilde{V}_0$</td>
<td>$\tilde{V}_1$</td>
<td>$\tilde{V}_2$</td>
<td>$\tilde{V}_0$</td>
<td>$\tilde{V}_2$</td>
<td>$\tilde{V}_1$</td>
<td>$\tilde{V}_0$</td>
</tr>
<tr>
<td></td>
<td>000</td>
<td>100</td>
<td>110</td>
<td>111</td>
<td>110</td>
<td>100</td>
<td>000</td>
</tr>
<tr>
<td>II.</td>
<td>$\tilde{V}_0$</td>
<td>$\tilde{V}_3$</td>
<td>$\tilde{V}_2$</td>
<td>$\tilde{V}_0$</td>
<td>$\tilde{V}_2$</td>
<td>$\tilde{V}_3$</td>
<td>$\tilde{V}_0$</td>
</tr>
<tr>
<td></td>
<td>000</td>
<td>010</td>
<td>110</td>
<td>111</td>
<td>110</td>
<td>010</td>
<td>000</td>
</tr>
<tr>
<td>III.</td>
<td>$\tilde{V}_0$</td>
<td>$\tilde{V}_3$</td>
<td>$\tilde{V}_4$</td>
<td>$\tilde{V}_0$</td>
<td>$\tilde{V}_4$</td>
<td>$\tilde{V}_3$</td>
<td>$\tilde{V}_0$</td>
</tr>
<tr>
<td></td>
<td>000</td>
<td>010</td>
<td>011</td>
<td>111</td>
<td>011</td>
<td>010</td>
<td>000</td>
</tr>
<tr>
<td>IV.</td>
<td>$\tilde{V}_0$</td>
<td>$\tilde{V}_5$</td>
<td>$\tilde{V}_4$</td>
<td>$\tilde{V}_0$</td>
<td>$\tilde{V}_4$</td>
<td>$\tilde{V}_5$</td>
<td>$\tilde{V}_0$</td>
</tr>
<tr>
<td></td>
<td>000</td>
<td>001</td>
<td>011</td>
<td>111</td>
<td>011</td>
<td>001</td>
<td>000</td>
</tr>
<tr>
<td>V.</td>
<td>$\tilde{V}_0$</td>
<td>$\tilde{V}_5$</td>
<td>$\tilde{V}_6$</td>
<td>$\tilde{V}_0$</td>
<td>$\tilde{V}_6$</td>
<td>$\tilde{V}_5$</td>
<td>$\tilde{V}_0$</td>
</tr>
<tr>
<td></td>
<td>000</td>
<td>001</td>
<td>101</td>
<td>111</td>
<td>101</td>
<td>001</td>
<td>000</td>
</tr>
<tr>
<td>VI.</td>
<td>$\tilde{V}_0$</td>
<td>$\tilde{V}_1$</td>
<td>$\tilde{V}_6$</td>
<td>$\tilde{V}_0$</td>
<td>$\tilde{V}_6$</td>
<td>$\tilde{V}_1$</td>
<td>$\tilde{V}_0$</td>
</tr>
<tr>
<td></td>
<td>000</td>
<td>100</td>
<td>101</td>
<td>111</td>
<td>101</td>
<td>100</td>
<td>000</td>
</tr>
</tbody>
</table>
2.3 Simulations and Experimental Results

Based on the analysis of SVPWM of two-level inverter, a simulation module by MATLAB and lab module by RT-LAB are set up to study the working process of the two-level inverter. Based on the simulation results, a two-level inverter was designed in different ways by MATLAB, and an experiment by RT-LAB is done to verify the performance and the waveforms of the inverter. The simulation results of three phase current, line to neutral voltage and line to line voltage by MATLAB were modeled in different way either single phase two level inverter or three phase two level inverter. When the output voltage is high suitable and the system parameters are properly selected, the output phase voltage is three-level and the output line voltage is two-level states, and the output line current is almost sinusoidal. The experimental results for three phase current, line to line voltage, and line to neutral voltage by RT-LAB were figured out. Results by both MATLAB (off time) and RT-LAB are the same. As a result, the experimental results by RT-LAB mostly agree with the simulation results by MATLAB.

2.3.1 Single Phase Two-Level Inverter

A two-level inverter had been simulated in different ways by Matlab. First of all, single phase two-level inverter was simulated and Simulink circuit is shown in Fig. 2.10, Fig. 2.12 shows the setting of universal bridge. Fig. 2.11 shows the output voltage and Fig. 2.13 shows output current.
Figure 2.10 Simulink circuit for single phase two-level inverter

Figure 2.11 The output voltage for single phase two-level inverter
Figure 2.12 Parameters of universal block in single phase two level inverter

Figure 2.13 The output current for single phase two level inverter
2.3.2 Three Phase Two-Level Inverter by Using Universal Bridge

A three phase two-level inverter can be configured by using a universal bridge and a PWM generator as shown in Simulink circuit in Fig. 2.15. Fig. 2.14 shows parameters for universal block and the output phase voltage, line to line voltage and three phase current are shown in Fig. 2.16, Fig. 2.17 and Fig. 2.18 respectively.

![Block Parameters: Universal Bridge](image)

Figure 2.14 Parameters of universal block in three phase two level inverter
Figure 2.15 Simulink circuit for three phase two-level inverter by using universal block
Figure 2.16 The output phase voltage for three phase two-level inverter by using universal block

Figure 2.17 The output line to line voltage for three phase two-level Inverter by using universal block

Figure 2.18 The output three phase current for three phase two-level Inverter by using universal block
2.3.3 Three Phase Two-Level Inverter by Using SVPWM Algorithm

Fig. 2.19 shows line to line output voltage for three phase two level inverter by using SVPWM algorithm and phase output voltage as shown in Fig. 2.20. Fig. 2.21 shows three phase output current for three phase two level inverter by using SVPWM algorithm (see appendices B and C Matlab files for SVPWM in fig. 2.22 and sector selection in Fig. 2.22). Simulink circuit is shown in Fig. 2.22. Fig. 2.23 shows subsystem of full bridge inverter.
Figure 2.21 Three phase output current for three phase two level invert by using SVPWM algorithm
Fig. 2.22 Simulink circuit for two level inverter by using SVPWM algorithm
Figure 2.23 Subsystem circuit of full bridge inverter in figure 2.20
2.3.4 Experimental Results of two-level inverter by RT-LAB

Three phase two-level inverter was run by using RT-LAB. Main circuit of the module is shown in Fig. 2.24. Fig. 2.25 shows two-level inverter during compilation by RT-LAB and subsystem circuit sm_maincircuit in Fig. 2.24 shows in Fig. 2.26. Fig. 2.27 shows three phase output current, line to line voltage and line to neutral voltage from top to bottom. Results by both MATLAB (off time) and RT-LAB (real time) are the same. As a result, the experimental results by RT-LAB approximately agree with the simulation results by MATLAB. The simulation and experimental results of the output line to neutral voltage of the two-level inverter operated as a six-step inverter.

![Main circuit for two-level inverter by RT-LAB](image1)

**Figure 2.24 Main circuit for two-level inverter by RT-LAB**

![Subsystem circuit sc_output](image2)

**Fig. 2.25 Subsystem circuit sc_output in Figure 2.24**
Fig. 2.26 Subsystem circuit sm_maincircuit in Figure 2.24
Fig. 2.27 Output three phase current, line-to-line voltage and line-neutral voltage for two-level inverter by RT-LAB
2.4 Conclusion

This chapter provides a comprehensive analysis on the two-level inverter. A number of issues were investigated, including the inverter configuration, operating principle, space vector modulation (SVM) techniques, and neutral point voltage control. The performance of the three-phase two-level six switches inverter had been simulated and improved by employing SVPWM control scheme. The use of a two-level inverter reduces the harmonic components of the output voltage compared with the traditional three phase inverter at the same switching frequency. It needs no additional reactors or transformers to reduce the harmonic components. Then, it is suitable for medium voltage and medium power systems. The designed and implemented two-level inverter realized the requirements, and fed R-L load by the required values of voltage and frequency. Three-phase two-level inverter configuration was individually modeled by Matlab and experimentally by TR-LAB. The obtained results in both cases (Matlab and RT-LAB) had approximately the same shape. The two-level inverter configuration was moduled by Matlab in different ways and the results were verified in real time by RT-LAB. The obtained results in both cases [Matlab and RT-LAB] had mostly the same shape. It is recommended that two-level inverter harmonics should be simulated and implemented by Matlab and RT-LAB to gain a deeper understanding of two-level inverter behavior in both off time and real time.
Chapter 3: Analysis of Three-Level Inverter

3.1 Introduction: - The power electronics device which converts DC power to AC power at required output voltage and frequency level is known as an inverter. Two categories into which inverters can be broadly classified are two level inverters and multilevel inverters. One advantage that multilevel inverters have compared to two level inverters is minimum harmonic distortion. A multilevel inverter can be utilized for multipurpose applications, such as an active power filter, a static VAR compensator and machine drive for sinusoidal and trapezoidal current applications. Some drawbacks to the multilevel inverters are the need for isolated power supplies for each one of the stages, the fact that they are a lot harder to build, they are more expensive, and they are more difficult to control in software.

This chapter focuses on the analysis of a three-level inverter. Full analysis for the three-level inverter is given. Desirable voltage and frequency have been achieved; however, harmonics distortion should be investigated during three-level inverter operation.

When AC loads are fed through inverters, an output voltage of required magnitude and frequency has to be achieved. A variable output voltage can be obtained by varying the input DC voltage and maintaining the gain of the inverter constant. On the other hand, if the DC input voltage is fixed and it is not controllable, a variable output voltage can be obtained by varying the gain of the inverter, which is normally accomplished by pulse-width-modulation (PWM) control within the inverter. The inverters which produce an output voltage or a current with medium or low rate power are known as two level inverters. In high-power and high-voltage applications these two-
level inverters have some limitations in operating at high frequency mainly due to
switching losses and constraints of device rating. This is where three level inverters are
advantageous. Increasing the number of voltage levels in the inverter without requiring
higher rating on individual devices which can increase power rating.

The pulse width modulation (PWM) strategies are the most effective to control multilevel
inverters. Even though space vector modulation (SVPWM) is complicated, it is the
preferred method to reduce power losses by decreasing the power electronics devices
switching frequency, which can be limited by pulse width modulation. Different aspects
of the three-level NPC inverter will be discussed including the inverter topology. The
operation theory will be discussed with the aspect of space vector pulse width
modulation. Three-level inverter NPC inverter is shown in Fig. 3.1. Each leg contains
four active switches $S_1$ to $S_4$ with antiparallel diodes $D_1$ to $D_4$.

The capacitors at the DC side are used to split the DC input into two, to provide a neutral
point $Z$. The clamping diodes can be defined as the diodes connected to the neutral point,
$D_{Z1}$, $D_{Z2}$. When switches $S_2$ and $S_3$ are connected, the output terminal $A$ can be taken to
the neutral through one of the clamping diodes. The voltage applied to each of the DC
 capacitors is $E$, and it equals half of the total DC voltage $V_d$.

![Figure 3.1 Three-level NPC inverter](image)

**3.2 Three-level inverter**

Figure 3.1 Three-level NPC inverter
3.2.1 Switching States

Switching states that are shown in Fig. 3.1 can represent the operating status of the switches in the three-level NPC inverter. When switching state is ‘1’, it is indicated that upper two switches in leg A connected and the inverter terminal voltage \( v_{AZ} \), which means the voltage for terminal A with respect to the neutral point Z, is +E, whereas ‘-1’ denotes that the lower two switches are on, which means \( v_{AZ} = -E \). When switching state ‘0’, it indicates that the inner two switches S2 and S3 are connected and \( v_{AZ} = 0 \) through the clamping diode, depending on the direction of the load current \( i_A \).

When \( D_{Z1} \) is turn on, the load current will be positive \( (i_A > 0) \) and the terminal A will be connected to the neutral point Z through the conduction of \( D_{Z1} \) and S2. Table 3.1 shows switching status for leg A. Leg B and leg C have the same concept.

Table 3.1 Definition of Switching States

<table>
<thead>
<tr>
<th>Switching State</th>
<th>Device Switching Status (Phase A)</th>
<th>Inverter Terminal Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>S1 S2 S3 S4</td>
<td>( v_{AZ} )</td>
</tr>
<tr>
<td>1</td>
<td>On On Off Off</td>
<td>E</td>
</tr>
<tr>
<td>0</td>
<td>Off On On Off</td>
<td>0</td>
</tr>
<tr>
<td>-1</td>
<td>Off Off On On</td>
<td>-E</td>
</tr>
</tbody>
</table>

3.2.2 Space Vector Modulation

3.2.2.1 Stationary Space Vectors

Three switching states [1], [0] and [-1] can represent the operation of each leg. By taking all three phases into account, the inverter has a total of 27 possible switching states. Table 3.2 shows the possibility of three phase switching states that are represented by
three letters in square brackets for the inverter phases A, B, and C. Table 3.2 shows the 27 switching states that are shown in Fig. 3.2. The voltage has four groups.

I. Zero vector ($V_0$), representing three switching states $[1 \ 1 \ 1]$, $[0 \ 0 \ 0]$ and $[-1 \ -1 \ -1]$. The magnitude of $V_0$ is Zero.

II. Small vector ($V_1$ to $V_6$), all having a magnitude of $V_d/3$. Each small sector has two switching states, one containing $[1]$ and the other containing $[-1]$ and they classified into P- or N- type small vector.

III. Medium vectors ($V_7$ to $V_{12}$), whose magnitude is $\frac{\sqrt{3}}{3}V_d$.

IV. Large vectors ($V_{13}$ to $V_{18}$), all having a magnitude of $\frac{2}{3}V_d$. 
Table 3.2 Voltage and Switching States

<table>
<thead>
<tr>
<th>Space Vector</th>
<th>Switching State</th>
<th>Vector Classification</th>
<th>Vector Magnitude</th>
</tr>
</thead>
<tbody>
<tr>
<td>V₀</td>
<td>[1 1 1]</td>
<td>Zero vector</td>
<td>0</td>
</tr>
<tr>
<td>V₁</td>
<td>P-type [1 0 0]</td>
<td>N-type [0 -1 -1]</td>
<td></td>
</tr>
<tr>
<td>V₂</td>
<td>P₂P [1 1 0]</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V₃</td>
<td>P₃P [0 1 0]</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V₄</td>
<td>P₄P [0 1 1]</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V₅</td>
<td>P₅P [0 0 1]</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V₆</td>
<td>P₆P [1 0 1]</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V₇</td>
<td>[1 0 -1]</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V₈</td>
<td>[0 1 -1]</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V₉</td>
<td>[-1 1 0]</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V₁₀</td>
<td>[-1 0 1]</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V₁₁</td>
<td>[0 -1 1]</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V₁₂</td>
<td>[1 -1 0]</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V₁₃</td>
<td>[1 -1 -1]</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V₁₄</td>
<td>[1 1 -1]</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V₁₅</td>
<td>[-1 1 -1]</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V₁₆</td>
<td>[-1 1 1]</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V₁₇</td>
<td>[-1 -1 1]</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V₁₈</td>
<td>[1 -1 1]</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Figure 3.2 Space vector diagram of the three-level inverter

Figure 3.3 Division of sectors and regions for three-level inverter
3.2.2.2 Determining the sector

$\theta$ is calculated and then the sector, in which the command vector $V^*$ is located, is determined as follows:

- If $0^\circ \leq \theta < 60^\circ$, then $V_{\text{ref}}$ will be in sector I.
- If $60^\circ \leq \theta < 120^\circ$, then $V_{\text{ref}}$ will be in sector II.
- If $120^\circ \leq \theta < 180^\circ$, then $V_{\text{ref}}$ will be in sector III.
- If $180^\circ \leq \theta < 240^\circ$, then $V_{\text{ref}}$ will be in sector IV.
- If $240^\circ \leq \theta < 300^\circ$, then $V_{\text{ref}}$ will be in sector V.
- If $300^\circ \leq \theta < 360^\circ$, then $V_{\text{ref}}$ will be in sector VI.

3.2.3 Time Calculation

The space vector diagram that is shown in Fig. 3.2 can be used to calculate the time for each sector (I to VI). Each sector has four regions (1 to 4), as shown in fig. 3.3, with the switching states of all vectors.

By using the same strategy that was used in chapter two, the sum of the voltage multiplied by the interval of chosen space vector equals the product of the reference voltage $V_{\text{ref}}$ and sampling period $T_s$. To illustrate, when reference voltage is located in region 2 of sector I then the nearest vectors to reference voltage are $V_1$, $V_7$, and $V_2$ as shown in Fig. 3.4, and the next equations explain the relationship between times and voltages:

$$
\begin{align*}
&V_1 T_a + V_7 T_b + V_2 T_c = V_{\text{ref}} T_s \\
&T_a + T_b + T_c = T_s
\end{align*}
$$

(3.1)

Where $T_a$, $T_b$, and $T_c$ are the times for $V_1$, $V_7$, and $V_2$ respectively.
From Fig. 4 voltage sectors $V_1$, $V_2$, and $V_7$ can be observed as follow:

\[
\begin{align*}
\vec{V}_1 &= \frac{1}{3} V_d \\
\vec{V}_2 &= \frac{1}{3} V_d e^{j\pi/3} \\
\vec{V}_7 &= \frac{\sqrt{3}}{3} V_d e^{j\pi/6} \\
\vec{V}_{\text{ref}} &= V_{\text{ref}} e^{j\theta}
\end{align*}
\]

(3.2)

By substituting equation (3.2) into (3.1)

\[
\left\{ \frac{1}{3} V_d T_a + \frac{\sqrt{3}}{3} V_d \left( \cos \frac{\pi}{6} + j \sin \frac{\pi}{6} \right) T_b + \frac{1}{3} V_d \left( \cos \frac{\pi}{3} + j \sin \frac{\pi}{3} \right) T_c = V_{\text{ref}} (\cos \theta + j \sin \theta) T_s \right\}
\]

(3.3)
From equation (3.3) real part and imaginary part can be determined by following equations

\[
\begin{align*}
\text{Re} \quad & T_a + \frac{3}{2} T_b + \frac{1}{2} T_c = 3 \frac{V_{\text{ref}}}{V_d} (\cos \theta) T_s \\
\text{Im} \quad & \frac{3}{2} T_b + \frac{\sqrt{3}}{2} T_c = 3 \frac{V_{\text{ref}}}{V_d} (\sin \theta) T
\end{align*}
\] (3.4)

By solving equation (3.4) with the equation for total time \( T_s = T_a + T_b + T_c \).

\[
\begin{align*}
T_a &= T_s \left[ 1 - 2 m_a \sin \theta \right] \\
T_b &= T_s \left[ 2 m_a \sin \left( \frac{\pi}{3} + \theta \right) - 1 \right] \quad \text{for } 0 \leq \theta \leq \frac{\pi}{3} \quad (3.5) \\
T_c &= T_s \left[ 1 - 2 m_a \sin \left( \frac{\pi}{3} + \theta \right) \right]
\end{align*}
\]

Where \( m_a \) is the modulation index and can be expressed as follow:

\[
m_a = \sqrt{3} \frac{V_{\text{ref}}}{V_d} \quad (3.6)
\]

The maximum value for \( V_{\text{ref}} \) can be derived at medium vector voltage \((V_7, V_8, V_9, V_{10}, V_{11}, \text{and } V_{12})\)

\[
V_{\text{ref,max}} = \frac{\sqrt{3}}{3} V_d \quad (3.7)
\]

By solving both equations (3.6) and (3.7) together, the maximum value for modulation index can be expressed as follow:

\[
m_{a,max} = \sqrt{3} \frac{V_{\text{ref,max}}}{V_d} = 1 \quad (3.8)
\]
And the modulation index can be given as below

\[ 0 \leq m_a \leq 1 \] \hspace{1cm} (3.9)

The equations for the calculation of times for \( \tilde{V}_{\text{ref}} \) in sector I can are given in table 3.3 as below.

<table>
<thead>
<tr>
<th>Region</th>
<th>( T_a )</th>
<th>( T_b )</th>
<th>( T_c )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>( \tilde{V}_1 )</td>
<td>( T_s \left[ 2m_a \sin\left(\frac{\pi}{3} - \theta\right)\right] )</td>
<td>( \tilde{V}_0 )</td>
</tr>
<tr>
<td>2</td>
<td>( \tilde{V}_1 )</td>
<td>( T_s \left[ 1 - 2m_a \sin \theta\right] )</td>
<td>( \tilde{V}_7 )</td>
</tr>
<tr>
<td>3</td>
<td>( \tilde{V}_1 )</td>
<td>( T_s \left[ 2 - 2m_a \sin \left(\frac{\pi}{3} + \theta\right)\right] )</td>
<td>( \tilde{V}_7 )</td>
</tr>
<tr>
<td>4</td>
<td>( \tilde{V}_{14} )</td>
<td>( T_s \left[ 2m_a \sin \theta - 1\right] )</td>
<td>( \tilde{V}_7 )</td>
</tr>
</tbody>
</table>

The times can be calculated for sectors (II to VI) by using the equations in table 3.3 with multiple of \( \pi/3 \) subtracted from the actual angular displacement \( \theta \), such that modified angle falls into the range between zero and \( \pi/3 \) for use in the equations as in chapter two.
3.2.4 Relationship between $\vec{V}_{\text{ref}}$ Location and Time

By using the example in Fig. 3.8, the relationship can be observed between $\vec{V}_{\text{ref}}$ location and time. By assuming the location of $\vec{V}_{\text{ref}}$ at point Q located at the center of region 3. Because the distances for the nearest vectors $\vec{V}_1$, $\vec{V}_7$, and $\vec{V}_{13}$ from Q are the same, the times for these vectors should be identical.

Three triangles in region 3 are equilibrium triangles. From triangle $V_0, X, \text{and Q}$ $V_{\text{ref}} = 0.509175 V_d$, and $\theta = 10.89^\circ$. By substituting in equation (3.6), $m_a = 0.882$ and $T_a = T_b = T_c = 0.3333 T_s$ from the equations in table 3.3.

Figure 3.5 An example to determine the relationship between the location of $V_{\text{ref}}$ and times
3.2.5 The Switching States by Using Switching Sequence.

By considering the switching transition and using sequences direction, shown in Fig. 3.6. and Fig. 3.7, the direction of the switching sequences for all regions in six sectors can be derived and the switching orders are given in the tables below, which are obtained for each region located in sectors I to VI, if all switching states in each region are used. Tables 3.4 shows thirteen segments of region 1 for each sector, Table 3.5 shows nine segments of region 2 for each sector, Table 3.6 shows seven segments of region 3 for each sector and Table 3.7 shows seven segments of region 4 for each sector.

Figure 3.6 Switching sequence for three-level SVPWM inverter

Figure 3.7 Sectors and their regions for three-level inverter
Table 3.4 thirteen segments of region 1 for all sectors

<table>
<thead>
<tr>
<th>Sector</th>
<th>Switching Segments</th>
</tr>
</thead>
<tbody>
<tr>
<td>I.</td>
<td>$\tilde{V}_0$ $\tilde{V}_1N$ $\tilde{V}_2N$ $\tilde{V}_0$ $\tilde{V}_1P$ $\tilde{V}_2P$ $\tilde{V}_0$ $\tilde{V}_1P$ $\tilde{V}_2P$ $\tilde{V}_0$ $\tilde{V}_2N$ $\tilde{V}_1N$ $\tilde{V}_0$</td>
</tr>
<tr>
<td>-1-1-1</td>
<td>0-1-1 00-1 000 110 111 110 110 000 00-1 0-1-1 -1-1-1</td>
</tr>
<tr>
<td>II.</td>
<td>$\tilde{V}_0$ $\tilde{V}_2N$ $\tilde{V}_3N$ $\tilde{V}_0$ $\tilde{V}_2P$ $\tilde{V}_3P$ $\tilde{V}_0$ $\tilde{V}_2P$ $\tilde{V}_3P$ $\tilde{V}_0$ $\tilde{V}_3N$ $\tilde{V}_2N$ $\tilde{V}_0$</td>
</tr>
<tr>
<td>-1-1-1</td>
<td>00-1 -10-1 000 110 111 110 110 000 -10-1 00-1 -1-1-1</td>
</tr>
<tr>
<td>III.</td>
<td>$\tilde{V}_0$ $\tilde{V}_3N$ $\tilde{V}_4N$ $\tilde{V}_0$ $\tilde{V}_3P$ $\tilde{V}_4P$ $\tilde{V}_0$ $\tilde{V}_3P$ $\tilde{V}_4P$ $\tilde{V}_0$ $\tilde{V}_4N$ $\tilde{V}_3N$ $\tilde{V}_0$</td>
</tr>
<tr>
<td>-1-1-1</td>
<td>-10-1 -100 000 011 111 111 011 010 000 -100 -10-1 -1-1-1</td>
</tr>
<tr>
<td>IV.</td>
<td>$\tilde{V}_0$ $\tilde{V}_5N$ $\tilde{V}_4N$ $\tilde{V}_0$ $\tilde{V}_5P$ $\tilde{V}_4P$ $\tilde{V}_0$ $\tilde{V}_5P$ $\tilde{V}_4P$ $\tilde{V}_0$ $\tilde{V}_5N$ $\tilde{V}_4N$ $\tilde{V}_0$</td>
</tr>
<tr>
<td>-1-1-1</td>
<td>-100 -1-10 000 011 111 111 011 010 000 -1-10 -100 -1-1-1</td>
</tr>
<tr>
<td>V.</td>
<td>$\tilde{V}_0$ $\tilde{V}_6N$ $\tilde{V}_5N$ $\tilde{V}_0$ $\tilde{V}_6P$ $\tilde{V}_5P$ $\tilde{V}_0$ $\tilde{V}_6P$ $\tilde{V}_5P$ $\tilde{V}_0$ $\tilde{V}_6N$ $\tilde{V}_5N$ $\tilde{V}_0$</td>
</tr>
<tr>
<td>-1-1-1</td>
<td>0-10 0-1-1 000 101 110 111 101 100 000 0-1-1 0-10 -1-1-1</td>
</tr>
</tbody>
</table>

Table 3.5 nine segments of region 2 for each sector

<table>
<thead>
<tr>
<th>Sector</th>
<th>Switching Segments</th>
</tr>
</thead>
<tbody>
<tr>
<td>I.</td>
<td>$\tilde{V}<em>{1N}$ $\tilde{V}</em>{2N}$ $\tilde{V}<em>7$ $\tilde{V}</em>{1P}$ $\tilde{V}<em>{2P}$ $\tilde{V}</em>{1P}$ $\tilde{V}<em>7$ $\tilde{V}</em>{2N}$ $\tilde{V}_{1N}$</td>
</tr>
<tr>
<td>0-1-1</td>
<td>00-1 10-1 100 110 100 10-1 00-1 0-1-1</td>
</tr>
<tr>
<td>II.</td>
<td>$\tilde{V}<em>{2N}$ $\tilde{V}</em>{3N}$ $\tilde{V}<em>8$ $\tilde{V}</em>{2P}$ $\tilde{V}<em>{3P}$ $\tilde{V}</em>{2P}$ $\tilde{V}<em>8$ $\tilde{V}</em>{3N}$ $\tilde{V}_{2N}$</td>
</tr>
<tr>
<td>00-1</td>
<td>-10-1 01-1 110 010 110 01-1 -10-1 00-1</td>
</tr>
<tr>
<td>III.</td>
<td>$\tilde{V}<em>{3N}$ $\tilde{V}</em>{4N}$ $\tilde{V}<em>9$ $\tilde{V}</em>{3P}$ $\tilde{V}<em>{4P}$ $\tilde{V}</em>{3P}$ $\tilde{V}<em>9$ $\tilde{V}</em>{4N}$ $\tilde{V}_{3N}$</td>
</tr>
<tr>
<td>-10-1</td>
<td>-100 -110 010 011 010 -110 -100 -10-1</td>
</tr>
<tr>
<td>IV.</td>
<td>$\tilde{V}<em>{4N}$ $\tilde{V}</em>{5N}$ $\tilde{V}<em>{10}$ $\tilde{V}</em>{4P}$ $\tilde{V}<em>{5P}$ $\tilde{V}</em>{4P}$ $\tilde{V}<em>{10}$ $\tilde{V}</em>{5N}$ $\tilde{V}_{4N}$</td>
</tr>
<tr>
<td>-100</td>
<td>-1-10 -101 011 001 011 -101 -1-10 -100</td>
</tr>
<tr>
<td>V.</td>
<td>$\tilde{V}<em>{5N}$ $\tilde{V}</em>{6N}$ $\tilde{V}<em>{11}$ $\tilde{V}</em>{5P}$ $\tilde{V}<em>{6P}$ $\tilde{V}</em>{5P}$ $\tilde{V}<em>{11}$ $\tilde{V}</em>{6N}$ $\tilde{V}_{5N}$</td>
</tr>
<tr>
<td>-1-10</td>
<td>0-10 0-11 001 101 001 0-11 0-10 -1-10</td>
</tr>
<tr>
<td>VI.</td>
<td>$\tilde{V}<em>{5N}$ $\tilde{V}</em>{1N}$ $\tilde{V}<em>{12}$ $\tilde{V}</em>{6P}$ $\tilde{V}<em>{1P}$ $\tilde{V}</em>{6P}$ $\tilde{V}<em>{12}$ $\tilde{V}</em>{1N}$ $\tilde{V}_{6N}$</td>
</tr>
<tr>
<td>0-10</td>
<td>0-1-1 1-10 101 100 101 1-10 0-1-1 0-10</td>
</tr>
</tbody>
</table>
Table 3.6 seven segments of region 3 for each sector

<table>
<thead>
<tr>
<th>Switching Segments</th>
<th>Sector 1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
</tr>
</thead>
<tbody>
<tr>
<td>I.</td>
<td>$V_{1N}$</td>
<td>$V_{13}$</td>
<td>$V_{7}$</td>
<td>$V_{1P}$</td>
<td>$V_{7}$</td>
<td>$V_{13}$</td>
<td>$V_{1N}$</td>
</tr>
<tr>
<td></td>
<td>0-1-1</td>
<td>1-1-1</td>
<td>10-1</td>
<td>100</td>
<td>10-1</td>
<td>1-1-1</td>
<td>0-1-1</td>
</tr>
<tr>
<td>II.</td>
<td>$V_{2N}$</td>
<td>$V_{14}$</td>
<td>$V_{8}$</td>
<td>$V_{2P}$</td>
<td>$V_{8}$</td>
<td>$V_{14}$</td>
<td>$V_{2N}$</td>
</tr>
<tr>
<td></td>
<td>00-1</td>
<td>11-1</td>
<td>01-1</td>
<td>110</td>
<td>01-1</td>
<td>11-1</td>
<td>00-1</td>
</tr>
<tr>
<td>III.</td>
<td>$V_{3N}$</td>
<td>$V_{15}$</td>
<td>$V_{9}$</td>
<td>$V_{3P}$</td>
<td>$V_{9}$</td>
<td>$V_{15}$</td>
<td>$V_{3N}$</td>
</tr>
<tr>
<td></td>
<td>-10-1</td>
<td>11-1</td>
<td>-110</td>
<td>010</td>
<td>-110</td>
<td>-11-1</td>
<td>-10-1</td>
</tr>
<tr>
<td>IV.</td>
<td>$V_{4N}$</td>
<td>$V_{16}$</td>
<td>$V_{10}$</td>
<td>$V_{4P}$</td>
<td>$V_{10}$</td>
<td>$V_{16}$</td>
<td>$V_{4N}$</td>
</tr>
<tr>
<td></td>
<td>-100</td>
<td>-111</td>
<td>-101</td>
<td>011</td>
<td>-101</td>
<td>-11-1</td>
<td>-100</td>
</tr>
<tr>
<td>V.</td>
<td>$V_{5N}$</td>
<td>$V_{17}$</td>
<td>$V_{11}$</td>
<td>$V_{5P}$</td>
<td>$V_{11}$</td>
<td>$V_{17}$</td>
<td>$V_{5N}$</td>
</tr>
<tr>
<td></td>
<td>-1-10</td>
<td>-11-1</td>
<td>0-11</td>
<td>001</td>
<td>0-11</td>
<td>-1-11</td>
<td>-1-10</td>
</tr>
<tr>
<td>VI.</td>
<td>$V_{6N}$</td>
<td>$V_{18}$</td>
<td>$V_{12}$</td>
<td>$V_{6P}$</td>
<td>$V_{12}$</td>
<td>$V_{18}$</td>
<td>$V_{6N}$</td>
</tr>
<tr>
<td></td>
<td>0-10</td>
<td>1-11</td>
<td>1-10</td>
<td>101</td>
<td>1-10</td>
<td>1-11</td>
<td>0-10</td>
</tr>
</tbody>
</table>

Table 3.7 seven segments of region 4 for each sector

<table>
<thead>
<tr>
<th>Switching Segments</th>
<th>Sector 1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
</tr>
</thead>
<tbody>
<tr>
<td>I.</td>
<td>$V_{2N}$</td>
<td>$V_{7}$</td>
<td>$V_{14}$</td>
<td>$V_{2P}$</td>
<td>$V_{14}$</td>
<td>$V_{7}$</td>
<td>$V_{2N}$</td>
</tr>
<tr>
<td></td>
<td>00-1</td>
<td>10-1</td>
<td>11-1</td>
<td>110</td>
<td>11-1</td>
<td>10-1</td>
<td>00-1</td>
</tr>
<tr>
<td>II.</td>
<td>$V_{3N}$</td>
<td>$V_{8}$</td>
<td>$V_{15}$</td>
<td>$V_{3P}$</td>
<td>$V_{15}$</td>
<td>$V_{8}$</td>
<td>$V_{3N}$</td>
</tr>
<tr>
<td></td>
<td>-10-1</td>
<td>01-1</td>
<td>-11-1</td>
<td>010</td>
<td>-11-1</td>
<td>01-1</td>
<td>-10-1</td>
</tr>
<tr>
<td>III.</td>
<td>$V_{4N}$</td>
<td>$V_{9}$</td>
<td>$V_{16}$</td>
<td>$V_{4P}$</td>
<td>$V_{16}$</td>
<td>$V_{9}$</td>
<td>$V_{4N}$</td>
</tr>
<tr>
<td></td>
<td>-100</td>
<td>-110</td>
<td>-111</td>
<td>011</td>
<td>-111</td>
<td>-110</td>
<td>-100</td>
</tr>
<tr>
<td>IV.</td>
<td>$V_{5N}$</td>
<td>$V_{10}$</td>
<td>$V_{17}$</td>
<td>$V_{5P}$</td>
<td>$V_{17}$</td>
<td>$V_{10}$</td>
<td>$V_{5N}$</td>
</tr>
<tr>
<td></td>
<td>-1-10</td>
<td>-101</td>
<td>-1-11</td>
<td>001</td>
<td>-1-11</td>
<td>-101</td>
<td>-1-10</td>
</tr>
<tr>
<td>V.</td>
<td>$V_{6N}$</td>
<td>$V_{11}$</td>
<td>$V_{18}$</td>
<td>$V_{6P}$</td>
<td>$V_{18}$</td>
<td>$V_{11}$</td>
<td>$V_{6N}$</td>
</tr>
<tr>
<td></td>
<td>0-10</td>
<td>0-11</td>
<td>1-11</td>
<td>101</td>
<td>1-11</td>
<td>0-11</td>
<td>0-10</td>
</tr>
<tr>
<td>VI.</td>
<td>$V_{1N}$</td>
<td>$V_{12}$</td>
<td>$V_{13}$</td>
<td>$V_{7P}$</td>
<td>$V_{13}$</td>
<td>$V_{12}$</td>
<td>$V_{1N}$</td>
</tr>
<tr>
<td></td>
<td>0-1-1</td>
<td>1-10</td>
<td>1-1-1</td>
<td>100</td>
<td>1-1-1</td>
<td>1-10</td>
<td>0-1-1</td>
</tr>
</tbody>
</table>
Figures 3.8 to 3.11 show switching sequence for Vref in sector I-1,2,3, and 4.

Figure 3.8 Switching sequence of thirteen segments for Vref in sector I region 1

Figure 3.9 Switching sequence of nine segments for Vref in sector I region 2
Figure 3.10 Switching sequence of nine segments for Vref in sector I region 3

Figure 3.11 Switching sequence of nine segments for Vref in sector I region 4
Figures 3.12 to 3.15 show switching sequence for $V_{\text{ref}}$ in sector II-1,2,3, and 4.

Figure 3.12 Switching sequence of thirteen segments for $V_{\text{ref}}$ in sector II region 1

Figure 3.13 Switching sequence of nine segments for $V_{\text{ref}}$ in sector II region 2
Figure 3.14 Switching sequence of nine segments for Vref in sector II region 3

Figure 3.15 Switching sequence of nine segments for Vref in sector II region 4
Figures 3.16 to 3.19 show switching sequence for $V_{\text{ref}}$ in sector III-1,2,3, and 4.

Figure 3.16 Switching sequence of thirteen segments for $V_{\text{ref}}$ in sector III region 1

Figure 3.17 Switching sequence of nine segments for $V_{\text{ref}}$ in sector III region 2
Figure 3.18 Switching sequence of nine segments for Vref in sector III region 3

Figure 3.19 Switching sequence of nine segments for Vref in sector III region 4
Figures 3.20 to 3.23 show switching sequence for Vref in sector IV-1,2,3, and 4.

Figure 3.20 Switching sequence of thirteen segments for Vref in sector IV region 1

Figure 3.21 Switching sequences of nine segments for Vref in sector IV region 2
Figure 3.22 Switching sequence of nine segments for Vref in sector IV region 3

Figure 3.23 Switching sequence of nine segments for Vref in sector IV region 4
Figures 3.24 to 3.27 show switching sequence for Vref in sector V-1,2,3, and 4.

Figure 3.24 Switching sequence of thirteen segments for Vref in sector V region 1

Figure 3.25 Switching sequence of nine segments for Vref in sector V region 2
Figure 3.26 Switching sequence of nine segments for Vref in sector V region 3

Figure 3.27 Switching sequence of nine segments for Vref in sector V region 4
Figures 3.28 to 3.31 show switching sequence for Vref in sector VI-1,2,3, and 4.

Figure 3.28 Switching sequence of thirteen segments for Vref in sector VI region 1

Figure 3.29 Switching sequence of nine segments for Vref in sector VI region 2
Figure 3.30 Switching sequence of nine segments for Vref in sector VI region 3

Figure 3.31 Switching sequence of nine segments for Vref in sector VI region 4
3.3 Conclusion

This chapter provides a comprehensive analysis on the three-level diode clamped inverter, also known as neutral-point clamped (NPC) inverter. A number of issues were investigated, including the inverter configuration, operating principle, space vector modulation (SVM) techniques, and neutral point voltage control. The performance of the three-phase three-level twelve switch inverter has been explained and improved by employing SVPWM control scheme. The use of three-level inverters reduces the harmonic components of the output voltage compared with the two-level inverter at the same switching frequency. It needs no additional reactors or transformers to reduce the harmonic components. Then, it is suitable for high voltage and high power systems. Switching sequence for each region in each sector had been explained in details which were utilized in the designed and implemented diode clamped three-level inverter to realize the requirements, and fed R-L load by the required values of voltage and frequency. Also, some derivations, such as thirteen segments of region 1 for each sector, nine segments of region 2 in each sector, seven segments of region 3 for each sector for three-level inverter, which have never been mentioned before, were derived and the switching sequence for each region in each sector was drawn.
Chapter 4: Simulation and Hardware in the loop Results for Three-Level Inverter

4.1 Introduction: - A computer simulation is one of the most widely used operation research tools presently available and is one of several methods used to evaluate, improve, and optimize many types of processes. This chapter deals with simulation and implementation of three-level inverter to improve the power quality. The three-level inverter is also capable of improving AC power. It is the most important power electronic system for reducing harmonics distortion in an electrical power system. The circuit model is developed for three-level inverter using twelve switches, four switches for each leg as was explained in chapter three. The Matlab simulation results are presented to validate the model and the experimental results are compared with the simulation results.

4.2 Matlab Results

A three-level inverter had been simulated either single phase or three phase three-level inverter, by Matlab Simulink in different ways. Single phase three-level inverter had been modeled by using three-level inverter NPC clamped diode. Three-phase three-level inverter had been modeled by three-level inverter NPC clamped diode, universal bridge, and nine switches with SVPWM algorithm.

4.2.1 Single Phase Three-Level Inverter

A single phase three-level inverter was simulated by Matlab and Simulink circuit is shown in Fig. 4.1, Fig. 4.2 shows the switching signals of single phase three level inverter in Fig. 4.1. Fig. 4.3 and Fig. 4.3 show output voltage waveform and output current waveform respectively.
Figure 4.1 Simulink circuit for single phase three level inverter
Figure 4.2 Simulink circuit for the switching signals of single phase three level inverter in Fig. 4.2
Figure 4.3 The output voltage waveform for single phase three level inverter

Figure 4.4 The output current waveform for single phase three level inverter
4.2.2 Three Phase-Three Level Inverter By Using Clamped Diode

Three phase three-level inverter can be configured by using clamped diodes as shown in Simulink circuit in Fig. 4.6. Fig. 4.5 shows switching signals for the circuits in Fig. 4.6. Fig. 4.7 shows line to neutral voltage waveform, Fig. 4.8 shows line to line voltage waveform and Fig. 4.9 shows three phase current waveform.

Figure 4.5 Simulink circuit for the switching signals of three phase three level inverter in Fig. 4.2
Figure 4.6 Simulink circuit for three phase three level inverter
Figure 4.7 The output line to neutral voltage waveform for three phase three level inverter

Figure 4.8 The output line to line voltage waveform for three phase three level inverter
Figure 4.9 The output three phase currents waveform for three phase three level inverter
4.2.3 Three Phase Three-Level Inverter By Using SVPWM Algorithm

Fig. 4.10 shows Simulink circuit for three phase three level inverter By Using SVPWM Algorithm and Fig. 4.11 shows subsystem full bridge three level inverter in Fig. 4.10. (M-file for SVPWM in Fig. 4.9 see appendix C).

Figure 4.10 Simulink circuit for three phase three level inverter by using SVPWM algorithm
Figure 4.11 Simulink circuit subsystem full bridge three level inverter in Fig. 4.10
Fig. 4.11 shows phase voltage waveform, Fig. 4.12 shows line to line voltage and Fig. 2.13 show three phase current waveform.

Figure 4.12 The output line to neutral voltage waveform for three phase three level inverter in Fig. 4.10.

Figure 4.13 The output line to line voltage waveform for three phase three level inverter in Fig. 4.10.
4.2.4 Three-Level Inverter by Using Three Level Bridge.

Three-level inverter had been simulated by Discrete 3-phase PWM Generator block and three level bridge block. Simulink circuit is shown in Fig. 4.16, Fig. 4.17 shows the setting of three level bridge. Fig. 4.18 shows the setting of discrete 3-phase PWM generator block.

Fig. 4.19, Fig. 4.20, and Fig 4.21 show the phase voltage waveform, line to line voltage waveform and three phase current waveforms respectively.
Figure 4.15 Simulink circuit for three phase three level inverter by using three level bridge block

Figure 4.16 Block parameters for three level bridge in Fig. 4.15
Figure 4.17 Block parameters for Discrete 3-phase PWM Generator block Fig. 4.15

Figure 4.18 Phase voltage waveform for the circuit in Fig. 4.15
Figure 4.19 Line to line voltage waveform for the circuit in Fig. 4.15

Figure 4.20 Three phase current waveform for the circuit in Fig. 4.16
4.2 Experimental Results by RT-LAB

A three-level inverter had been run by RT-LAB as part of this thesis to achieve the three-level inverter results in real time. Circuit module for three-level inverter had been designed and run by RT-LAB and the results were obtained as well as Matlab results. Three phase three-level inverter was run by using RT-LAB. Main circuit of the module is shown in Fig. 4.22. Fig. 2.23 shows three-level inverter during compilation by RT-LAB and subsystem circuit sm_maincircuit in Figure 4.22 shows in Figure 2.24. Fig. 2.25 show three phase output current, line to line voltage and line to neutral voltage from top to bottom. Results by both MATLAB (off time) and RT-LAB are the same. As a result, the experimental results by RT-LAB mostly agree with the simulation results by MATLAB. The simulation and experimental results of the output line to line voltage of the three-level inverter operated as a six-step inverter.
Figure 4.22 Subsystem Circuit sc_output in Figure 4.21
Figure 4.23 Subsystem Circuit sm_maincircuit in Figure 4.21
Figure 4.24 Output three phase current, line-to-line voltage and line-neutral voltage for three-level inverter by RT-LAB
4.3 Conclusion

This chapter provides the performance of the three-phase three-level inverter. The inverter has been simulated and improved by employing SVPWM control scheme. The use of three-level inverters reduces the harmonic components of the output voltage compared with the two-level inverter at the same switching frequency. Based on the analysis of SVPWM, a simulation system by both MATLAB and RT-LAB are set up to study the working process of the three-level inverter. Based on the simulation results, a three-level inverter was designed by MATLAB, and an experiment by RT-LAB was done to verify the performance and the waveforms of the inverter. The simulation results of three phase current, line to neutral voltage and line to line voltage by MATLAB were shown. When the output voltage is suitable and the system parameters are properly selected, the output phase voltage is of five-level and the output line voltage is of three-level, and the output line current is almost sinusoidal. Results by both MATLAB (off time) and RT-LAB are the same. As a result, the experimental results by RT-LAB mostly agree with the simulation results by MATLAB.

The simulation and experimental results of the output line to line voltage of the three-level inverter operated as a six-step inverter.
Appendices

Appendix A:-- Overview about RT-LAB

RT-LAB is the real-time technology that is revolutionizing the way model-based design is performed. Through its openness, it has the flexibility to be applied to any simulation and control problem, and its scalability provides a low-risk entry point for any application, allowing the developer to add compute-power where and when needed - whether it is to speed up simulations or for real-time hardware in the loop applications. RT-LAB provides tools for running and monitoring your simulations or controls on various runtime targets. An open architecture enables RT-LAB to work with the popular diagramming tools MATLAB Simulink and MATRIXX System Build[1].

[1] RT-LAB guide line
Appendix B: M-file for SVPWM in Fig. 2.20

function y = sv(u)

angle = u(1);
Vm = u(2);
time = u(3);

V = 8;
gamma = mod(angle, pi/3);
Va = Vm * cos(gamma);
Vb = Vm * sin(gamma);
A = [2/3*650 650/3 0; 0 650/sqrt(3) 0; 1 1 1];
b = [Va/5400; Vb/5400; 1/5400];
c = (inv(A))*b;

T1 = c(1,1);
T2 = c(2,1);
T0 = c(3,1);

tt1 = T0/4;
 tt2 = tt1 + T1/2;
 tt3 = tt2 + T2/2;
 tt4 = tt3 + T0/2;
 tt5 = tt4 + T2/2;
 tt6 = tt5 + T1/2;
t1 = T0/4;
t2 = t1 + T2/2;
t3 = t2 + T1/2;
t4 = t3 + T0/2;
t5 = t4 + T1/2;
t6 = t5 + T2/2;

if (0 < angle) && (angle <= pi/3)
S = 1;
elseif (pi/3 < angle) && (angle <= 2*pi/3)
S = 2;
elseif (2*pi/3 < angle) && (angle <= pi)
S = 3;
elseif (pi < angle) && (angle <= 4*pi/3)
S = 4;
elseif (4*pi/3 < angle) && (angle <= 5*pi/3)
S = 5;
elseif (5*pi/3 < angle) && (angle <= 2*pi)
S = 6;
else
S = 1;
end

if (S == 1)
if (0 < time) && (time <= tt1)
V = 8;
elseif (tt1 < time) && (time <= tt2)
V = 1;
else
V = 1;
end
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elseif (tt2 < time) && (time <= tt3)
    V = 2;
elseif (tt3 < time) && (time <= tt4)
    V = 7;
elseif (tt4 < time) && (time <= tt5)
    V = 2;
elseif (tt5 < time) && (time <= tt6)
    V = 1;
else
    V = 8; % tt6 < time
end

elseif (S == 2) %8, 3, 2, 7, 2, 3, 8
    if (0 < time) && (time <= t1)
        V = 8;
    elseif (t1 < time) && (time <= t2)
        V = 3;
    elseif (t2 < time) && (time <= t3)
        V = 2;
    elseif (t3 < time) && (time <= t4)
        V = 7;
    elseif (t4 < time) && (time <= t5)
        V = 2;
    elseif (t5 < time) && (time <= t6)
        V = 3;
    else
        V = 8; % tt6 < time
    end

elseif (S == 3) %8, 3, 4, 7, 4, 3, 8
    if (0 < time) && (time <= tt1)
        V = 8;
    elseif (tt1 < time) && (time <= tt2)
        V = 3;
    elseif (tt2 < time) && (time <= tt3)
        V = 4;
    elseif (tt3 < time) && (time <= tt4)
        V = 7;
    elseif (tt4 < time) && (time <= tt5)
        V = 4;
    elseif (tt5 < time) && (time <= tt6)
        V = 3;
    else
        V = 8; % tt6 < time
    end

elseif (S == 4) %8, 4, 5, 7, 5, 4, 8
    if (0 < time) && (time <= t1)
        V = 8;
    elseif (t1 < time) && (time <= t2)
        V = 5;
    elseif (t2 < time) && (time <= t3)
        V = 4;
    elseif (t3 < time) && (time <= t4)
        V = 7;
    elseif (t4 < time) && (time <= t5)
        V = 4;
    elseif (t5 < time) && (time <= t6)
        V = 5;
else
    V = 8; % tt6 < time
end

elseif (S == 5)%8, 5, 6, 7, 6, 5, 8
    if (0 < time) && (time <= tt1)
        V = 8;
    elseif (tt1 < time) && (time <= tt2)
        V = 5;
    elseif (tt2 < time) && (time <= tt3)
        V = 6;
    elseif (tt3 < time) && (time <= tt4)
        V = 7;
    elseif (tt4 < time) && (time <= tt5)
        V = 6;
    elseif (tt5 < time) && (time <= tt6)
        V = 5;
    else
        V = 8; % tt6 < time
    end
end

elseif (S == 6)%8, 1, 6, 7, 6, 1, 8
    if (0 < time) && (time <= t1)
        V = 8;
    elseif (t1 < time) && (time <= t2)
        V = 1;
    elseif (t2 < time) && (time <= t3)
        V = 6;
    elseif (t3 < time) && (time <= t4)
        V = 7;
    elseif (t4 < time) && (time <= t5)
        V = 6;
    elseif (t5 < time) && (time <= t6)
        V = 1;
    else
        V = 8; % tt6 < time
    end
end

if (V == 1)
    y(1) = 1;
    y(3) = 0;
    y(5) = 0;
    y(4) = 0;
    y(6) = 1;
    y(2) = 1;
elseif (V == 2)
    y(1) = 1;
    y(3) = 1;
    y(5) = 0;
    y(4) = 0;
    y(6) = 0;
    y(2) = 1;
elseif (V == 3)
    y(1) = 0;
    y(3) = 1;
    y(5) = 0;
    y(4) = 1;
y(6) = 0;
y(2) = 1;

elseif (V == 4)
y(1) = 0;
y(3) = 1;
y(5) = 1;
y(4) = 1;
y(6) = 0;
y(2) = 0;

elseif (V == 5)
y(1) = 0;
y(3) = 0;
y(5) = 1;
y(4) = 1;
y(6) = 1;
y(2) = 0;

elseif (V == 6)
y(1) = 1;
y(3) = 0;
y(5) = 1;
y(4) = 0;
y(6) = 1;
y(2) = 0;

elseif (V == 7)
y(1) = 1;
y(3) = 1;
y(5) = 1;
y(4) = 0;
y(6) = 0;
y(2) = 0;

elseif (V == 8)
y(1) = 0;
y(3) = 0;
y(5) = 0;
y(4) = 1;
y(6) = 1;
y(2) = 1;

else
y(1) = 0;
y(3) = 0;
y(5) = 0;
y(4) = 1;
y(6) = 1;
y(2) = 1;

end

y(7)=S;

end
Appendix C: M-file for sector selection in Fig. 2.20

```matlab
function y = sector(u)
    angle = u(1);
    if (0 < angle) && (angle <= pi/3)
        y = 1;
    elseif (pi/3 < angle) && (angle <= 2*pi/3)
        y = 2;
    elseif (2*pi/3 < angle) && (angle <= pi)
        y = 3;
    elseif (pi < angle) && (angle <= 4*pi/3)
        y = 4;
    elseif (4*pi/3 < angle) && (angle <= 5*pi/3)
        y = 5;
    elseif (5*pi/3 < angle) && (angle <= 2*pi)
        y = 6;
    else
        y = 1;
    end
```
function y = svpwm(u)
    % Input management
    time = u(1);
    angle = u(2); % angle
    m = u(3);
    Ts = u(4); % sampling time

    % Decide in which sector
    if (0 <= angle) && (angle <= pi/3)
        S = 1;
    elseif (pi/3 < angle) && (angle <= 2*pi/3)
        S = 2;
    elseif (2*pi/3 < angle) && (angle <= pi)
        S = 3;
    elseif (pi < angle) && (angle <= 4*pi/3)
        S = 4;
    elseif (4*pi/3 < angle) && (angle <= 5*pi/3)
        S = 5;
    elseif (5*pi/3 < angle) && (angle <= 2*pi)
        S = 6;
    end

    % Decide in which region
    alpha = mod(angle, pi/3);

    % calculate m1, m2
    m2 = (2/3^.5)*m*sin(alpha);
    m1 = m*cos(alpha) - sin(alpha)/sqrt(3);

    % decide in which region
    if (m1 < .5) && (m2 < .5) && ((m1+m2)<.5)
        reg = 1; % region one
    elseif (m1 > .5)
        reg = 2;
    elseif (m2 > .5)
        reg = 4;
    elseif (m1 < .5) && (m2 < .5) && ((m1+m2)>.5)
        reg = 3;
    elseif m1==.5 && m2==0
        reg = 1;
    % elseif m1==0.5
    % if m2==0
% reg = 1;
% else
% reg = 3;
% end
elseif m2==.5 && m1==0
    reg = 1;
end

%% Switching time calc
%
% if reg==1; % Region 1 Time calcualtion
%    % I multiplied each by 2 to get Ts not Ts/2 as the paper says
% ta=2*1*m*Ts*sin((pi/3)-alpha); %Ta
% tb=Ts*(1-2*1*m*sin((pi/3)+alpha)); %Tb
% tc=2*1*m*Ts*sin(alpha); %Tc
% %y(3)=Ts-(y(1)+y(2)); %Tc=Ts-Ta-Tb
%
% elseif reg==2; % Region 2 Time calcualtion
%    % I multiplied each by 2 to get Ts not Ts/2 as the paper says
% ta=2*Ts*(1-1*m*sin((pi/3)+alpha));
% tb=2*1*m*Ts*sin(alpha);
% tc=Ts*(2*1*m*sin((pi/3)-alpha)-1);
% %y(3)=Ts-(y(1)+y(2)); %Tc=Ts-Ta-Tb
%
% elseif reg==3; % Region 3 Time calcualtion
%    % I multiplied each by 2 to get Ts not Ts/2 as the paper says
% ta=Ts*(1-2*1*m*sin(alpha));
% tb=Ts*(2*1*m*sin((pi/3)+alpha)-1);
% tc=Ts*(1+2*1*m*sin(alpha-(pi/3)));
% %y(3)=Ts-(y(1)+y(2)); %Tc=Ts-Ta-Tb
%
% elseif reg==4; % Region 4 Time calcualtion
%    % I multiplied each by 2 to get Ts not Ts/2 as the paper says
% ta=Ts*(2*1*m*sin(alpha)-1);
% tb=2*1*m*Ts*sin((pi/3)-alpha);
% tc=2*Ts*(1-1*m*sin((pi/3)+alpha));
% %y(3)=Ts-(y(1)+y(2)); %Tc=Ts-Ta-Tb
% % else
% %
% % end
% % SECTOR 1
if (S == 1) && (reg==1) % first sector
    ta=2*1*m*Ts*sin((pi/3)-alpha); %Ta
    tb=Ts*(1-2*1*m*sin((pi/3)+alpha)); %Tb
    tc=2*1*m*Ts*sin(alpha); %Tc

    if (0 <= time) && (time <= ta)
V=3; %
elseif (ta < time) && (time <= ta+tb)
  V=27;
elseif (ta+tb < time) && (time <= ta+tb+tc)
  V=8;
else
  V=1;
end

elseif (S == 1) && (reg==2)  % first sector
  ta=2*Ts*(1-1*m*sin((pi/3)+alpha));
  tb=2*1*m*Ts*sin(alpha);
  tc=Ts*(2*1*m*sin((pi/3)-alpha)-1);
    if (0 < time) && (time <= ta)
      V=4;
    elseif (ta < time) && (time <= tb+ta)
      V=6;
    elseif (ta+tb < time) && (time <= ta+tb+tc)
      V=5;
    else
      V=1;
    end

elseif (S == 1) && (reg==3)  % first sector
  ta=Ts*(1-2*1*m*sin(alpha));
  tb=Ts*(2*1*m*sin((pi/3)+alpha)-1);
  tc=Ts*(1+2*1*m*sin(alpha-(pi/3)));
    if (0 < time) && (time <= ta)
      V=4;
    elseif (ta < time) && (time <= tb+ta)
      V=6;
    elseif (ta+tb < time) && (time <= ta+tb+tc)
      V=8;
    else
      V=1;
    end

elseif (S == 1) && (reg==4)  % first sector
  ta=Ts*(2*1*m*sin(alpha)-1);
  tb=2*1*m*Ts*sin((pi/3)-alpha);
  tc=2*Ts*(1-1*m*sin((pi/3)+alpha));
    if (0 < time) && (time <= ta)
      V=9;
    elseif (ta < time) && (time <= tb+ta)
      V=6;
    elseif (ta+tb < time) && (time <= ta+tb+tc)
      V=8;
    else
      V=1;
    end
%% SECTOR 2

elseif (S == 2) && (reg==1)
    ta=2*1*m*Ts*sin((pi/3)-alpha);  \%Ta
    tb=Ts*(1-2*1*m*sin((pi/3)+alpha)); \%Tb
    tc=2*1*m*Ts*sin(alpha); \%Tc
    if (0 < time) && (time <= ta)
        V=7;
    elseif (ta < time) && (time <= tb+ta)
        V=1;
    elseif (ta+tb < time) && (time <= ta+tb+tc)
        V=13;
    else
        V=1;
    end
end

elseif (S == 2) && (reg==2)
    ta=2*Ts*(1-1*m*sin((pi/3)+alpha));
    tb=2*1*m*Ts*sin(alpha);
    tc=Ts*(2*1*m*sin((pi/3)-alpha)-1);
    if (0 < time) && (time <= ta)
        V=8;
    elseif (ta < time) && (time <= tb+ta)
        V=10;
    elseif (ta+tb < time) && (time <= ta+tb+tc)
        V=9;
    else
        V=1;
    end
end

elseif (S == 2) && (reg==3)
    ta=Ts*(1-2*1*m*sin(alpha));
    tb=Ts*(2*1*m*sin((pi/3)+alpha)-1);
    tc=Ts*(1+2*1*m*sin(alpha-(pi/3)));
    if (0 < time) && (time <= ta)
        V=7;
    elseif (ta < time) && (time <= tb+ta)
        V=10;
    elseif (ta+tb < time) && (time <= ta+tb+tc)
        V=12;
    else
        V=1;
    end
end

elseif (S == 2) && (reg==4)
    ta=Ts*(2*1*m*sin(alpha)-1);
    tb=2*1*m*Ts*sin((pi/3)-alpha);
    tc=2*Ts*(1-1*m*sin((pi/3)+alpha));
    if (0 < time) && (time <= ta)
        V=11;
    elseif (ta < time) && (time <= tb+ta)
        V=10;
    end

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elseif (ta+tb < time) && (time <= ta+tb+tc)
    V=12;
else
    V=1;
end

%% SECTOR 3
elseif (S == 3) && (reg==1)
    ta=2*1*m*Ts*sin((pi/3)-alpha);  %Ta
    tb=Ts*(1-2*1*m*sin((pi/3)+alpha)); %Tb
    tc=2*1*m*Ts*sin(alpha);  %Tc
    if (0 < time) && (time <= ta)
        V=13;
    elseif (ta < time) && (time <= tb+ta)
        V=2;
    elseif (ta+tb < time) && (time <= ta+tb+tc)
        V=15;
    else
        V=1;
    end

elseif (S == 3) && (reg==2)
    ta=2*Ts*(1-1*m*sin((pi/3)+alpha));
    tb=2*1*m*Ts*sin(alpha);
    tc=Ts*(2*1*m*sin((pi/3)-alpha)-1);
    if (0 < time) && (time <= ta)
        V=13;
    elseif (ta < time) && (time <= tb+ta)
        V=16;
    elseif (ta+tb < time) && (time <= ta+tb+tc)
        V=11;
    else
        V=1;
    end

elseif (S == 3) && (reg==3)
    ta=Ts*(1-2*1*m*sin(alpha));
    tb=Ts*(2*1*m*sin((pi/3)+alpha)-1);
    tc=Ts*(1+2*1*m*sin(alpha-(pi/3)));
    if (0 < time) && (time <= ta)
        V=12;
    elseif (ta < time) && (time <= tb+ta)
        V=16;
    elseif (ta+tb < time) && (time <= ta+tb+tc)
        V=14;
    else
        V=1;
    end
elseif (S == 3) && (reg==4)
ta=Ts*(2*1*m*sin(alpha)-1);
tb=2*1*m*Ts*sin((pi/3)-alpha);
tc=2*Ts*(1-1*m*sin((pi/3)+alpha));
if (0 < time) && (time <= ta)
    V=17;
elseif (ta < time) && (time <= tb+ta)
    V=16;
elseif (ta+tb < time) && (time <= ta+tb+tc)
    V=14;
else
    V=1;
end

%% SECTOR 4
elseif (S == 4) && (reg==1)
ta=2*1*m*Ts*sin((pi/3)-alpha); %Ta
tb=Ts*(1-2*1*m*sin((pi/3)+alpha)); %Tb
tc=2*1*m*Ts*sin(alpha); %Tc
if (0 < time) && (time <= ta)
    V=14;
elseif (ta < time) && (time <= tb+ta)
    V=2;
elseif (ta+tb < time) && (time <= ta+tb+tc)
    V=19;
else
    V=1;
end

elseif (S == 4) && (reg==2)
ta=2*Ts*(1-1*m*sin((pi/3)+alpha));
tb=2*1*m*Ts*sin(alpha);
tc=Ts*(2*1*m*sin((pi/3)-alpha)-1);
if (0 < time) && (time <= ta)
    V=15;
elseif (ta < time) && (time <= tb+ta)
    V=18;
elseif (ta+tb < time) && (time <= ta+tb+tc)
    V=17;
else
    V=1;
end

elseif (S == 4) && (reg==3)
ta=Ts*(1-2*1*m*sin(alpha))
tb=Ts*(2*1*m*sin((pi/3)+alpha)-1); 
tc=Ts*(1+2*1*m*sin(alpha-(pi/3)));
if (0 < time) && (time <= ta)
    V=14;
elseif (ta < time) && (time <= tb+ta)
    V=18;

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elseif (ta+tb < time) && (time <= ta+tb+tc)
    V=19;
else
    V=1;
end

elseif (S == 4) && (reg==4)
ta=Ts*(2*1*m*sin(alpha)-1);
tb=2*1*m*Ts*sin((pi/3)-alpha);
tc=2*Ts*(1-1*m*sin((pi/3)+alpha));

    if (0 < time) && (time <= ta)
        V=21;
    elseif (ta < time) && (time <= tb+ta)
        V=18;
    elseif (ta+tb < time) && (time <= ta+tb+tc)
        V=20;
    else
        V=1;
    end

elseif (S == 5) && (reg==1)
ta=2*1*m*Ts*sin((pi/3)-alpha);  %Ta
tb=Ts*(1-2*1*m*sin((pi/3)+alpha)); %Tb
tc=2*1*m*Ts*sin(alpha);  %Tc

    if (0 < time) && (time <= ta)
        V=20;
    elseif (ta < time) && (time <= tb+ta)
        V=1;
    elseif (ta+tb < time) && (time <= ta+tb+tc)
        V=23;
    else
        V=1;
    end

elseif (S == 5) && (reg==2)
ta=2*Ts*(1-1*m*sin((pi/3)+alpha));
tb=2*1*m*Ts*sin(alpha);
tc=Ts*(2*1*m*sin((pi/3)-alpha)-1);

    if (0 < time) && (time <= ta)
        V=19;
    elseif (ta < time) && (time <= tb+ta)
        V=22;
    elseif (ta+tb < time) && (time <= ta+tb+tc)
        V=21;
    else
        V=1;
    end

elseif (S == 5) && (reg==3)
ta=Ts*(1-2*1*m*sin(alpha));
tb=Ts*(2*l*m*sin((pi/3)+alpha)-1);
tc=Ts*(1+2*l*m*sin(alpha-(pi/3)));
if (0 < time) && (time <= ta) 
V=20;
  elseif (ta < time) && (time <= tb+ta) 
V=22;
  elseif (ta+tb < time) && (time <= ta+tb+tc) 
V=24;
  else
    V=1;
end

elseif (S == 5) && (reg==4)
ta=Ts*(2*l*m*sin(alpha)-1);
tb=2*l*m*Ts*sin((pi/3)-alpha);
tc=2*Ts*(1-1*m*sin((pi/3)+alpha));
if (0 < time) && (time <= ta) 
V=25;
  elseif (ta < time) && (time <= tb+ta) 
V=22;
  elseif (ta+tb < time) && (time <= ta+tb+tc) 
V=24;
  else
    V=1;
end

%% SECTOR 6

elseif (S == 6) && (reg==1)
ta=2*l*m*Ts*sin((pi/3)-alpha);  %Ta
tb=Ts*(1-2*l*m*sin((pi/3)+alpha)); %Tb
tc=2*l*m*Ts*sin(alpha);  %Tc
if (0 < time) && (time <= ta) 
V=23;
  elseif (ta < time) && (time <= tb+ta) 
V=2;
  elseif (ta+tb < time) && (time <= ta+tb+tc) 
V=4;
  else
    V=1;
end

elseif (S == 6) && (reg==2)
ta=2*Ts*(1-1*m*sin((pi/3)+alpha));
tb=2*l*m*Ts*sin(alpha);
tc=Ts*(2*l*m*sin((pi/3)-alpha)-1);
if (0 < time) && (time <= ta) 
V=24;
  elseif (ta < time) && (time <= tb+ta) 
V=26;
  elseif (ta+tb < time) && (time <= ta+tb+tc) 
V=25;
else
  V=1;
end

elseif (S == 6) && (reg==3)
ta=Ts*(1-2*1*m*sin(alpha));
tb=Ts*(2*1*m*sin((pi/3)+alpha)-1);
tc=Ts*(1+2*1*m*sin(alpha-(pi/3)));
if (0 < time) && (time <= ta)
  V=23;
  elseif (ta < time) && (time <= tb+ta)
  V=26;
  elseif (ta+tb < time) && (time <= ta+tb+tc)
  V=3;
  else
  V=1;
  end
end

elseif (S == 6) && (reg==4)
ta=Ts*(2*1*m*sin(alpha)-1);
tb=2*1*m*Ts*sin((pi/3)-alpha);
tc=2*Ts*(1-1*m*sin((pi/3)+alpha));
if (0 < time) && (time <= ta)
  V=5;
  elseif (ta < time) && (time <= tb+ta)
  V=26;
  elseif (ta+tb < time) && (time <= ta+tb+tc)
  V=4;
  else
  V=1;
  end
else
  V=1;
end

%% Switching VECTORS: V0 to V26
if (V == 1) % switching pattern corresponds to base vector V1 '000'
y(1)=0 ; y(2)=1 ; y(3)=0 ; % phase A leg switches '+ 0 -'
  repectively
y(4)=0 ; y(5)=1 ; y(6)=0 ; % phase B leg
y(7)=0 ; y(8)=1 ; y(9)=0 ; % phase C leg
elseif (V == 27) % second zero vector '111'
y(1)=1 ; y(2)=0 ; y(3)=0 ;
y(4)=1 ; y(5)=0 ; y(6)=0 ;
y(7)=1 ; y(8)=0 ; y(9)=0 ;
elseif (V == 2) % third zero vector'-1-1-1'
y(1)=1 ; y(2)=0 ; y(3)=0 ;
y(4)=1 ; y(5)=0 ; y(6)=0 ;
y(7)=1 ; y(8)=0 ; y(9)=0 ;
y(1)=0 ; y(2)=0 ; y(3)=1 ; % phase A leg switches
y(4)=0 ; y(5)=0 ; y(6)=1 ; % phase B leg
y(7)=0 ; y(8)=0 ; y(9)=1 ; % phase C leg

elseif (V == 3) %'100'
    y(1)=1 ; y(2)=0 ; y(3)=0 ; % phase A leg switches
    y(4)=0 ; y(5)=1 ; y(6)=0 ; % phase B leg
    y(7)=0 ; y(8)=1 ; y(9)=0 ; % phase C leg
elseif (V == 4)
    y(1)=0 ; y(2)=1 ; y(3)=0 ;
    y(4)=0 ; y(5)=0 ; y(6)=1 ;
    y(7)=0 ; y(8)=0 ; y(9)=1 ;
elseif (V == 5)
    y(1)=1 ; y(2)=0 ; y(3)=0 ;
    y(4)=0 ; y(5)=0 ; y(6)=1 ;
    y(7)=0 ; y(8)=0 ; y(9)=1 ;
elseif (V == 6)
    y(1)=1 ; y(2)=0 ; y(3)=0 ;
    y(4)=0 ; y(5)=1 ; y(6)=0 ;
    y(7)=0 ; y(8)=0 ; y(9)=1 ;
elseif (V == 7)
    y(1)=1 ; y(2)=0 ; y(3)=0 ;
    y(4)=1 ; y(5)=0 ; y(6)=0 ;
    y(7)=0 ; y(8)=1 ; y(9)=0 ;
elseif (V == 8)
    y(1)=0 ; y(2)=1 ; y(3)=0 ;
    y(4)=0 ; y(5)=1 ; y(6)=0 ;
    y(7)=0 ; y(8)=0 ; y(9)=1 ;
elseif (V == 9)
    y(1)=1 ; y(2)=0 ; y(3)=0 ;
    y(4)=1 ; y(5)=0 ; y(6)=0 ;
    y(7)=0 ; y(8)=0 ; y(9)=1 ;
elseif (V == 10)
    y(1)=0 ; y(2)=1 ; y(3)=0 ;
    y(4)=1 ; y(5)=0 ; y(6)=0 ;
    y(7)=0 ; y(8)=0 ; y(9)=1 ;
elseif (V == 11)
    y(1)=0 ; y(2)=0 ; y(3)=1 ;
    y(4)=1 ; y(5)=0 ; y(6)=0 ;
    y(7)=0 ; y(8)=0 ; y(9)=1 ;
elseif (V == 12)
    y(1)=0 ; y(2)=1 ; y(3)=0 ;
    y(4)=1 ; y(5)=0 ; y(6)=0 ;
    y(7)=0 ; y(8)=1 ; y(9)=0 ;
elseif (V == 13)
    y(1)=0 ; y(2)=0 ; y(3)=1 ;
    y(4)=0 ; y(5)=1 ; y(6)=0 ;
    y(7)=0 ; y(8)=0 ; y(9)=1 ;
elseif (V == 14)
    y(1)=0 ; y(2)=1 ; y(3)=0 ;
    y(4)=1 ; y(5)=0 ; y(6)=0 ;
    y(7)=1 ; y(8)=0 ; y(9)=0 ;
elseif (V == 15)
    y(1)=0 ; y(2)=0 ; y(3)=1 ;
    y(4)=0 ; y(5)=1 ; y(6)=0 ;
y(7)=0 ; y(8)=1 ; y(9)=0 ;

elseif (V == 16)
  y(1)=0 ; y(2)=0 ; y(3)=1 ;
  y(4)=1 ; y(5)=0 ; y(6)=0 ;
  y(7)=0 ; y(8)=1 ; y(9)=0 ;

elseif (V == 17)
  y(1)=0 ; y(2)=0 ; y(3)=1 ;
  y(4)=1 ; y(5)=0 ; y(6)=0 ;
  y(7)=1 ; y(8)=0 ; y(9)=0 ;

elseif (V == 18)
  y(1)=0 ; y(2)=0 ; y(3)=1 ;
  y(4)=0 ; y(5)=1 ; y(6)=0 ;
  y(7)=1 ; y(8)=0 ; y(9)=0 ;

elseif (V == 19)
  y(1)=0 ; y(2)=1 ; y(3)=0 ;
  y(4)=0 ; y(5)=1 ; y(6)=0 ;
  y(7)=1 ; y(8)=0 ; y(9)=0 ;

elseif (V == 20)
  y(1)=0 ; y(2)=0 ; y(3)=1 ;
  y(4)=0 ; y(5)=0 ; y(6)=1 ;
  y(7)=0 ; y(8)=1 ; y(9)=0 ;

elseif (V == 21)
  y(1)=0 ; y(2)=1 ; y(3)=0 ;
  y(4)=0 ; y(5)=0 ; y(6)=1 ;
  y(7)=1 ; y(8)=0 ; y(9)=0 ;

elseif (V == 22)
  y(1)=0 ; y(2)=1 ; y(3)=0 ;
  y(4)=0 ; y(5)=0 ; y(6)=1 ;
  y(7)=0 ; y(8)=1 ; y(9)=0 ;

elseif (V == 23)
  y(1)=1 ; y(2)=0 ; y(3)=0 ;
  y(4)=0 ; y(5)=1 ; y(6)=0 ;
  y(7)=1 ; y(8)=0 ; y(9)=0 ;

elseif (V == 24)
  y(1)=0 ; y(2)=1 ; y(3)=0 ;
  y(4)=0 ; y(5)=0 ; y(6)=1 ;
  y(7)=0 ; y(8)=1 ; y(9)=0 ;

elseif (V == 25)
  y(1)=1 ; y(2)=0 ; y(3)=0 ;
  y(4)=0 ; y(5)=0 ; y(6)=1 ;
  y(7)=1 ; y(8)=0 ; y(9)=0 ;

elseif (V == 26)
  y(1)=1 ; y(2)=0 ; y(3)=0 ;
  y(4)=0 ; y(5)=0 ; y(6)=1 ;
  y(7)=0 ; y(8)=1 ; y(9)=0 ;
else  %zero vector for elseif
    y(1)=1 ; y(2)=0 ;  y(3)=0 ;
    y(4)=1 ; y(5)=0 ;  y(6)=0 ;
    y(7)=1 ; y(8)=0 ;  y(9)=0 ;
end

y(10)=reg;
y(11)=S;
end
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