Ballistic Electron Emission Microscopy and Internal Photoemission Study on Metal Bi-layer/Oxide/Si, High-k Oxide/Si, and “End-on” Metal Contacts to Vertical Si Nanowires

DISSERTATION

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ABSTRACT

In this thesis, three separate experiments involving electronic materials are described. Nanometer-spatial resolution ballistic electron emission microscopy (BEEM) is used to study the inhomogeneity of metal-bialayer/SiO$_2$ interface, and small size and restricted geometry effect of “end-on” metal contacts to vertical Si NWs embedded in spin-on glass. BEEM and internal photoemission (Int-PE) are also combined for the first time to study conduction band and valence band offsets between Si and promising high-$k$ (high dielectric constant) oxides: Sc$_2$O$_3$ and Lu$_2$O$_3$.

In the first experiment, a comparison of the dependence on gate voltage of the average energy barrier measured by BEEM of a metal bi-layer Pt/Al/SiO$_2$/Si sample and a Pt/SiO$_2$/Si sample suggests that the metal/oxide interface of the Pt/Al/SiO$_2$/Si sample is laterally inhomogeneous at nm length scales. However, BEEM images of the bi-layer sample do not show significantly larger lateral variations than observed on a (uniform) Pt/SiO$_2$/Si sample, indicating that any inhomogeneous “patches” of lower energy barrier height have size smaller than the lateral resolution of BEEM, estimated for these samples to be $\sim$10 nm. Finite element electrostatic simulations of an assumed inhomogeneous interface with nm size patches of different effective work function can fit the
experimental data of the bi-layer sample much better than an assumed homogenous interface, indicating that bi-layer film is in fact laterally inhomogeneous at the nm scale.

Int-PE measurements on 20 nm-thick epitaxial Sc$_2$O$_3$ and Lu$_2$O$_3$ film on Si (111) show the existence of a lower “tail state” conduction band (CB) extending ~1 eV below the upper CB (similar to that reported for amorphous Sc$_2$O$_3$ and Lu$_2$O$_3$ films), indicating that these states are not simply due to disorder in amorphous films. BEEM measurements on epitaxial Sc$_2$O$_3$/Si also show that this lower CB supports elastic hot-electron transport even against an applied electric field, indicating transport via extended rather than localized states.

BEEM measurements on “end-on” Au contacts to vertical Si NWs show strong suppression of hot-electron injection at higher injected current in the NWs (produced either by increasing the tip voltage or the tunneling current) comparing to a regular Au/Si junction, suggesting that this current suppression is due to a steady-state charge build-up in the NW that increase as more current is injected into the NW. The BEEM current suppression of most NWs was also found to increase strongly as the temperature was decreased, indicating more charge build-up at lower temperature. Time-dependent current suppression due to changing steady-state charge build-up in the NWs was observed when the tunnel current was abruptly increased and decreased, directly supporting a model in which the BEEM current suppression is due to (temperature-dependent) steady-state charge build up. Those electrons might be trapped at the Si NW/SiO$_2$ interface close to the metal/Si NW contact, which is consistent with finite element electrostatic simulations. Our BEEM measurements also show that the local Schottky barrier height (SBH) at the
edge of two separate NWs is ~20 meV lower than at the NWs center. Finite element simulation suggests that the lower SBH at the contact edge might be due to the NW/oxide interface states charge together with the geometry enhanced electric field effect (the NWs protruding ~8 nm out of the spin-on glass).
Dedicated to my parents
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VITA

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CHAPTER 1

Overview

Results of three different studies are presented in this work: ballistic electron emission microscopy (BEEM) measurement and modeling of lateral variations of the effective work function at bi-layer Pt/Al/SiO₂ interface; BEEM and internal photoemission (Int-PE) measurements of energy band alignment at metal/high-\(k\) oxide and high-\(k\) oxide/Si interfaces; and BEEM studies on “end-on” metal contacts to vertical Si nanowires (NWs) embedded in spin-on glass.

The metal-oxide-semiconductor field-effect transistor (MOSFET) is well known to be the most important device for very-large-scaled (VLS) integrated circuits such as micro processors and semiconductor memories [1]. However, in order to keep pace with the modern high technology, many improvements still need to be made for the MOSFET technology.

One of the future complementary MOS technology requirements is that it needs metal gates with effective work function (EWF) that can be “tuned” to precisely adjust the transistor turn-on voltage. Macroscopic \(C-V\) measurements [2,3] showed that this could be done by using a \textit{metal bi-layer} as the MOS gate electrode, the EWF of which
could be tuned by adjusting the thickness of a very thin low work function metal covered by a high work function metal film (or vice-versa) on a SiO₂ film. However surprisingly, the EWF could be adjusted over a very wide thickness range of the bottom metal film (about 3-10 nm in Reference [3]), because one would expect no effects of the top metal film due to the screening of the bottom metal film after the bottom film is more than a few monolayers thick. This would make more sense if the metal/SiO₂ interface were actually laterally inhomogeneous with small “pinholes” in the bottom film filled in by the top film, and the decrease in average pinhole coverage and diameter with increasing bottom metal thickness would then result in the tunability [3]. This motivates our first study, because our nm-spatial resolution BEEM technique may be possible to reveal this inhomogeneity.

The continued scaling of MOSFET raises interest in replacing SiO₂ with a “high-$k$” (higher dielectric constant) material [4]. Because if the energy barriers for electron and hole tunneling remain sufficiently large, a thicker high-$k$ film could have the same capacitance as a thinner SiO₂ film but with reduced direct tunnel current. This motivates intensive studies of the band structure of potential high-$k$ materials, and in particular the conduction and valence band offsets to Si, by Int-PE and photoconductivity (PC). Surprisingly, a variety of amorphous oxide films [5-11] (HfO₂, Sc₂O₃, LaAlO₃, GdScO₃, DyScO₃, LaScO₃, Lu₂O₃, and La₂Hf₂O₇) were found to have nearly the same band gap (~5.6 - 5.8 eV), conduction band (CB) offset (~2.0 – 2.1 eV), and valence band (VB) offset (~2.4 – 2.6 eV). Furthermore, many of these films were also reported to have a secondary conduction band (sometimes referred to as a “tail state” band) extending ~1 eV
below the assumed primary CB, with possible physical origin attributed to disorder in the amorphous oxide film [5,8], or the different symmetries or \( d \)-state coupling in complex oxides with mixed metal cations [9]. In order to explore the nature of those “tail-states”, BEEM and Int-PE were combined for the first time in our second study to study the energy band alignment of metal/epitaxial \( \text{Sc}_2\text{O}_3/\text{Si} \) and metal/epitaxial \( \text{Lu}_2\text{O}_3/\text{Si} \) structures.

As the lateral dimensions of MOSFETs continue to be scaled down, conventional planar MOSFET faces increasingly challenge issues such as short channel effects and scaling of gate oxide thickness [12]. To further miniaturize the transistor while still maintaining control over power consumption, new device geometries such as Si NW based FETs need to be considered [13]. However contacts to NWs (which are of great importance for potential NW FETs) are still poorly understood. It is widely believed that carrier transport through contacts to these devices are affected by the small size [14-15] and restricted geometry [16] inherent to such structures. For example, Lonard & Tersoff argued that ultra-narrow “end-on” metal contacts made to the end of a narrow nanotube (NT) or NW in a vertical geometry should have intrinsically weaker Fermi-level pinning than wider contacts [14]. This motivates our study on “end-on” metal contacts to vertical Si NWs.

This work is organized in the following way:

First a brief introduction of the basic physics of metal-semiconductor contacts with the focus on a simple Schottky barrier formation model, Fermi-level pinning, and image-force lowering is given at the beginning of chapter 2. Then the energy band
alignment of a MOS structure at different conditions is discussed in detail. Finally a brief discussion of the $C-V$ characteristics of a MOS structure is provided.

In chapter 3, we first briefly introduce the general information about the Int-PE technique including the simplest theoretical model of Int-PE, the basic Int-PE experiment setup, and example Int-PE and photoconductivity (PC) studies on a MOS capacitor. Then the basic information about our major experiment technique, BEEM, is given with a focus on the basic configuration of BEEM, the two basic BEEM modes of operation, the Bell-Kaiser theoretical model that is used to fit measured BEEM data, and example BEEM studies on MOS structures. Typical experimental procedures are discussed shortly at the end of the chapter.

The results of our work on metal bi-layer Pt/Al/SiO$_2$ samples are presented in chapter 4. A brief review of the background of this study is first presented, and followed with an introduction of the sample preparation. Then experimental results of the barrier height dependence on gate voltage of Pt/SiO$_2$/Si and bi-layer Pt/Al/SiO$_2$/Si are presented. Theoretical modeling the dependence of the barrier height on gate voltage is then discussed in detail. Finally the main conclusions of this study are presented, in which the highlight is that it suggests the large reported “tunability” of the EWF of metal bi-layer samples [2,3] is due to an inhomogeneous metal/SiO$_2$ interface, with the top metal filling in “pinholes” in the bottom metal film.

Chapter 5 presents our studies on metal/epitaxial Sc$_2$O$_3$/Si and metal/epitaxial Lu$_2$O$_3$/Si samples. We will first introduce the background of the study of metal/high-$k$ oxide/Si structures. Then our detailed BEEM and Int-PE studies of the band alignment of
metal/epitaxial Sc$_2$O$_3$/Si samples are presented, in which we found that the lower “tail states” conduction band of Sc$_2$O$_3$ supports elastic hot-electron transport even against an applied electric field (indicating transport via extended rather than localized states). Then BEEM, Int-PE/photoconductivity and C-V measurements on metal/epitaxial Lu$_2$O$_3$/Si sample are discussed in detail. Finally the major findings of those studies are summarized.

Our study on “end-on” metal contacts to vertical Si NWs embedded in spin-on glass are presented in Chapter 6. First a brief review of the background of this project is given. Then a procedure of fabrication of “end-on” metal contacts to vertical Si NWs is introduced. A study which indicates that hot-electron injection can produce significant steady-state charge build-up in vertical Si NWs is then discussed in detail. Measurements of lateral variations of Schottky barrier height across “end-on” metal contacts to vertical Si NWs and corresponding theoretical modeling are then presented. Finally, an (unsuccessful) trial procedure for using PECVD deposition of SiO$_2$ on as-grown Si NWs to improve the procedure of making “end-on” metal contacts to vertical Si NWs is discussed briefly. Major findings and future directions of this project are presented at the end of this chapter.

Finally, major findings of all the work in this thesis are summarized in chapter 7.
CHAPTER 2

Introduction

2.1 Metal-Semiconductor contacts

There has been substantial long term interest in understanding, characterizing and controlling metal-semiconductor (M/S) contacts in modern semiconductor device technology, since M/S contacts are an essential part of virtually all semiconductor electronic and optoelectronic devices. For most types of semiconductor devices developed with different materials or structures, M/S contacts have been the fundamental gateways for carries to enter and exit the devices.

In this section, a basic Schottky barrier formation model, Fermi-level pinning, and Schottky barrier lowering due to the image force will be briefly reviewed. Some of the formulas and concepts discussed here will be used in Chapter 4, 5 and 6. Detailed discussion about M/S contacts can be found in References [1,17-19].

2.1.1 Schottky Barrier

The first model of potential barrier formation at the metal-semiconductor interface was proposed by Walter Schottky in 1938 [20]. Figure 2.1(a) show the energy band
diagram of a metal and a n-type semiconductor, each assumed to have a planar surface, when they are far away from each other. $W_m$ is the work function of the metal (which is defined as the energy difference between the vacuum level and the Fermi level), $E_F$ is the Fermi level, $E_c$ and $E_v$ are the conduction and valance bands of the semiconductor, and $\chi_S$ is the electron affinity measured from the bottom of the semiconductor conduction band $E_c$ to the vacuum level [1]. The work function of the metal is assumed to be larger than the work function of the semiconductor $W_s$ (which is defined as $\chi_S + (E_c - E_F)$) as in Fig. 2.1(a). If a wire is connected between the metal and semiconductor, the charge will flow from the semiconductor to the metal until the Fermi levels on both sides line up and thermal equilibrium is established (in Figure 2.1(b)). The Fermi level of the Semiconductor is lowered by $W_m - (\chi_S + (E_c - E_F))$ (which is called the contact potential) relative to its original position (before being connected). There is a negative charge build-up at the metal surface, and an equal positive charge build-up in the semiconductor. This positive charge (ionized donors) is distributed over a depletion region near the semiconductor surface due to the relative low carrier concentration of the semiconductor.

The potential drop across the vacuum gap between the metal and the semiconductor ($V_i$) and the built-in potential in the semiconductor due to the positive ionized donors in the depletion region are together responsible for the contact potential drop between the metal and the semiconductor.

As the metal and the semiconductor were brought closer to each other, the negative (positive) charge build up at the metal surface (in the semiconductor) will both increase. The built-in potential in the semiconductor increases, and the potential drop ($V_i$)
Figure 2.1 (adopted from Reference 1): Energy band diagrams of ideal metal-semiconductor (n-type) contacts without considering interface states. (a) The metal and the semiconductor are far away from each other and not electrically connected. (b) The metal and the semiconductor are electrically connected but still far away from each other. (c) The metal and the semiconductor are brought close to each other. (d) The metal and the semiconductor are in contact.
Figure 2.2: Energy band diagrams of ideal metal on p-type semiconductor contacts without considering interface states. For a p-type semiconductor, the electric field and band bending are opposite compared to the n-type case. The holes “float” in p-type semiconductor.

across the vacuum gap between the metal and the semiconductor decreases, given the fixed contact potential (in Figure 2.1(c). When the distance of the vacuum gap $d$ becomes small enough to be comparable with interatomic distances, the gap becomes transparent to electrons and the total contact potential drops across the semiconductor depletion region. So for the limiting case, as shown in Figure 2.1(d), the Schottky barrier height (SBH) is simply the difference between the work function of the metal and the electron affinity of the semiconductor [1], as given by

$$\phi_{Ba} = W_m - \chi_S. \quad (2.1)$$
The idea of Schottky barrier formation between a metal and a n-type semiconductor discussed above of course also applies for a contact between a metal and a p-type semiconductor (as in Figure 2.2), with the barrier height given by

$$\phi_{Bn} = E_g - (W_m - \chi_0),$$

(2.2)

where $E_g$ is the band gap of the semiconductor. So for a given metal and a semiconductor, the sum of the barrier heights of metal on n-type and p-type semiconductor is expected to be the same as the band gap of the semiconductor [1].

As discussed above for a metal and a n-type semiconductor, the potential barrier would cause a depletion region of positive ionized donors in the semiconductor. Under the abrupt depletion approximation, which assumes that

$$\rho \approx q \times N_d \text{ for } x < W,$$

and

$$\rho \approx 0 \text{ for } x > W,$$

where $\rho$ is the net charge (which is the sum of free carrier concentration and concentration of n- or p-type dopants), $q$ is the elementary charge, $N_d$ is the concentration of donors of the n-type semiconductor and $W$ is the depletion width, we obtain [1]

$$W = \sqrt{\frac{2\varepsilon_0\varepsilon_r(V_{bi} - kT)}{qN_d}}.$$

(2.3)

$V_{bi}$ is the built-in potential in the semiconductor $qV_{bi} = \phi_{Bn} - (E_c - E_F)$, $\varepsilon_0$ and $\varepsilon_r$ are the permittivity in vacuum and relative dielectric constant of the semiconductor, respectively. For a 0.85 eV Schottky barrier height and a moderate n-type doping of $N_d \approx 1 \times 10^{16}/\text{cm}^3$, the depletion width ($W$) of the Si is $\sim 0.3 \mu m$.

2.1.2 Fermi-level pinning

According to the simplest Schottky barrier model, the SBH of a metal-semiconductor contact is linearly proportional to the metal work function. However, it
was found experimentally that the SBH at the metal-semiconductor interface only weakly
depends on the metal work function, and often shows some dependence on the
preparation of the metal-semiconductor interface. To solve this discrepancy, Bardeen [21]
proposed another model, which includes the effect of interface states at the metal-
semiconductor interface. It made two major assumptions (as in Figure 2.3): (1) there is an
insulating interfacial layer (labeled \(d\) in Fig.2.3) about a few angstroms thick (which is
transparent to electrons) between the metal and the semiconductor; (2) there is a
continuous distribution of interface states in energy at the semiconductor surface, which
is a property of semiconductor surface and are independent of the metal. The metal-
semiconductor interface properties are characterized by the charge neutrality level (CNL)
(referenced from the semiconductor valence band maximum) and the interface state
density \(D_{it}\), states/eV/cm\(^2\)) at the semiconductor surface. If the Fermi level at the
interface is at the CNL, then the net interface charge is assumed to be zero. If the Fermi
level at the semiconductor surface lies below the CNL, the interface states located
between the Fermi level and CNL would be filled with positive charge (as in Figure 2.3)
while other interface states stay neutral. The positive interface states charge would then
bring the semiconductor CB and the surface CNL down and so that the CNL lines up
closer to the Fermi level. If the Fermi level lies above the CNL, the interface states
located between the Fermi level and CNL would be filled with negative charge, which
would then bring the semiconductor CB and the CNL up so that the CNL lines up closer
to the Fermi level. In the limit of an infinitely large interfaces state density, the CNL is
completely “pinned” at the Fermi level at the semiconductor surface regardless of the
work function of the metal. This pinning of the CNL close to the Fermi level due to charging of interface states is called “Fermi-level pinning”. Note that in common usage, one usually says that the Fermi level is pinned close to the CNL, when in fact it is more accurate to say that the CNL is pinned close to the Fermi level.

Figure 2.3 (adopted from Reference 1): Energy band diagrams of metal-semiconductor contacts with interface states (Bardeen model [21]).

Figure 2.3 illustrates the Fermi-level pinning effect between a metal and a n-type semiconductor. When the CNL lies above the Fermi level, there is a surface state charge density on the semiconductor given by [1]

\[
Q_{ss} = qD_u (\phi_{Bn} + CNL - E_g),
\]

(2.4)
where $D_{it}$ is assumed to be constant over the entire energy range. Using Gauss’s law, one can determine that the potential drop across the metal-semiconductor interfacial layer is given by

$$V_i = \frac{Q_{ss} d}{\varepsilon_0 \varepsilon_r}. \quad (2.5)$$

And from the energy band diagram of Figure 2.11, one can get:

$$\phi_{bn} = \phi_{b0} - qV_i = W_m - \chi_S - qV_i. \quad (2.6)$$

From Equation 2.4, 2.5 and 2.6 we can obtain:

$$W_m - \chi_S - \phi_{bn} = \frac{q^2 D_{it} d}{\varepsilon_0 \varepsilon_r} (\phi_{bn} + CNL - E_g). \quad (2.7)$$

We can then solve Equation 2.7 for $\phi_{bn}$:

$$\phi_{bn} = \frac{1}{1 + \gamma} (W_m - \chi_S) + \frac{\gamma}{1 + \gamma} (E_g - CNL), \quad (2.8)$$

where the factor $\gamma$ is given by

$$\gamma = \frac{q^2 D_{it} d}{\varepsilon_0 \varepsilon_r}. \quad (2.9)$$

We next consider two limiting cases [1]. (1) For an infinitely large interface state density ($D_{it} \to \infty$), $\gamma \to \infty$ and Eq. 2.8 becomes

$$\phi_{bn} = E_g - CNL. \quad (2.10)$$

In this case, the Fermi level is pinned at the position of CNL by the interface states, and the Schottky barrier is independent of the metal work function. (2) If there are almost no interface states ($D_{it} \to 0$), $\gamma \to 0$ and Eq. 2.8 becomes

$$\phi_{bn} = W_m - \chi_S = \phi_{b0}, \quad (2.11)$$
here $\phi_{0}$ is the ideal Schottky barrier discussed in section 2.1.1. For this case, the Schottky barrier would then be linearly proportional to the metal work function.

**Figure 2.4:** Experimental results of barrier heights for metal on n-type Si contacts (Figure taken from Reference [22]).
Figure 2.4 shows the experimental results of barrier heights for metal on n-type Si contacts measured by Cowley and Sze, where the least-squares straight line fit to the data yields [22]

$$\phi_{\text{m}} = 0.27W_m^{-0.55}. \quad (2.12)$$

From Eq. 2.12, one can clearly see that the Schottky Barrier of metal on Si contacts only weakly depend on the metal work function. Similar weak Schottky barrier dependence on the metal work function for other semiconductors was also reported [22]. A charge neutrality level (CNL) of 0.33 eV and interface states density of $4 \times 10^{13}$ states/eV/cm$^2$ for Si were obtained by comparing the theoretical calculations with the above expression (Eq. 2.12) of the experimental results [1]. The interfacial layer distance is assumed to be ~4 angstroms and the dielectric constant of the interfacial layer is taken to be $\varepsilon_0$ in reference [1]. Note that by assuming the dielectric constant of the interfacial layer to be the same as for Si ($\varepsilon_r = 11.9$) and an interface state density of $47.6 \times 10^{13}$ states/eV/cm$^2$, one would get the same pinning behavior for metal/Si contacts. Since the interfacial layer resides in the Si, it would make more sense to assume a dielectric constant of the interfacial layer to be the same as for Si than for vacuum (in [1]). So in chapter 6, a dielectric constant of $\varepsilon_r = 11.9$ and an interface state density of $47.6 \times 10^{13}$ states/eV/cm$^2$ are assumed for the metal/Si interfacial dipole layer for finite element electrostatic simulations.

Note that there are also interface states at the Si/SiO$_2$ interface, which would cause either positive or negative interface state charge developed at the Si/SiO$_2$ interface depending on the position of charge neutrality level for Si/SiO$_2$ interface states relative to the Fermi-level of Si [1,23]. This behavior of the Si/SiO$_2$ interface states is somewhat
similar to the metal/semiconductor interface states described above, except that (i)
interface states at the Si/SiO$_2$ interface have a different physical origin, and (ii) the
charge neutrality level (CNL) for Si/SiO$_2$ interface states is generally assumed to be
located close to mid-gap. Details about the physical origin and effects of Si/SiO$_2$ interface
states will be discussed in section 6.4.

2.1.3 Image force lowering

When a point charge (in vacuum) is brought a certain distance $x$ away from a
metal surface, electrons in the metal will rearrange to screen the external charge. If the
metal surface could be treated as an infinite plane, then the electrostatic force exerted on
the external charge by the induced opposite charge at the metal surface is the same as that
of a virtual “image charge” with an equal and opposite charge located at $-x$. The
attractive image force is given by [1]

$$ F = \frac{-q^2}{4\pi\epsilon_0 (2x)^2} = \frac{-q^2}{16\pi\epsilon_0 x^2}. \quad (2.13) $$

As the external charge moves away from (perpendicular to the surface) the metal surface
from $x$ to infinity, the work done by the image charge on the external charge is given by

$$ W(x) = \int_{x}^{\infty} F dx = \frac{-q^2}{16\pi\epsilon_0 x}. \quad (2.14) $$

So at any distance $x$ away from the metal, the external charge would have an “image
potential energy” of $\frac{-q^2}{16\pi\epsilon_0 x}$.

For a metal-semiconductor system, as the external charge inside the
semiconductor moves towards or away from the metal, the charge in the semiconductor
could rearrange to partially screen the external charge, so the image potential energy of the external charge in this case decreases to \( \frac{-q^2}{16\pi\varepsilon_0\varepsilon_r x} \). The value of the dielectric constant \( \varepsilon_r \) of the semiconductor would depend on how fast the charge in the semiconductor could respond to the moving external charge (assumed to have a velocity of the order of \( 10^5 \text{m/s} \) [1]).

As in Figure 2.5 for a metal-semiconductor contact, the total potential energy \( PE \) (relative to the CB minimum of the semiconductor at the surface) (blue curve) of an external charge is the sum of the image potential energy (red dashed curve) and the potential energy caused by the depletion electric field \( E \) (pink dashed line) in the semiconductor given by

\[
PE = \frac{-q^2}{16\pi\varepsilon_0\varepsilon_r x} - qEx. \quad (2.15)
\]

And hence the Schottky barrier would be lowered by \( \Delta\phi \) [1] given by

\[
\Delta\phi = q \sqrt{\frac{qE}{4\pi\varepsilon_0\varepsilon_r}}, \quad (2.16)
\]

with the maximum energy barrier location of

\[
x_m = \sqrt{\frac{q}{16\pi\varepsilon_0\varepsilon_r E}}. \quad (2.17)
\]

Note that here the Schottky barrier is defined as the maximum energy of the PE of an electron as it moves between the metal and the semiconductor. Note also that the metal-semiconductor interfacial insulating layer was not considered in the above discussion for simplicity. For the calculations to be discussed in Chapter 6, both the metal-
semiconductor interface states and the image force lowering effect were included to calculate the Schottky barrier at metal/Si contacts.

From Eq. 2.16, one can get that the image force lowering $\Delta \phi$ of Schottky barrier is linearly proportional to the square root of the electric field $\sqrt{E}$ near the semiconductor surface. For an electric field $E$ of $\sim 10^6$–$10^7$ V/m, the Schottky barrier lowering $\Delta \phi$ is $\sim 11$–$35$ meV and the location of the lowering $x_m$ is $\sim 5.5$–$1.7$ nm (the relative dielectric constant $\varepsilon_r$ in Eq. 2.16 is assumed to be 11.9 as for Si).

**Figure 2.5** (adopted from Reference 1): Energy band diagram of a metal-semiconductor system with image force lowering. The blue curve is the sum of the red dashed curve and pink dashed line. The potential energy barrier at the metal-semiconductor interface is lowered by $\Delta \phi$ due to the image force.
2.2 Metal-oxide-semiconductor (MOS) structures

The metal-oxide-semiconductor (MOS) capacitor is the heart of the metal-oxide-semiconductor field-effect transistor (MOSFET), which is well known to be the most important device for very-large-scaled (VLS) integrated circuits [1, 24]. Since part of this dissertation is about BEEM and Int-PE studies on metal bi-layer/oxide/Si and metal/high-$k$/Si MOS structures, a brief review of the energy band diagrams and $C-V$ characteristics of a MOS structure will be presented in this section. Some of the formulas and concepts discussed here will be used in Chapters 4 and 5. Detailed discussion about the fundamentals of MOS capacitors and MOSFETs can be found in References [1,24].

2.2.1 Semiconductor band bending in MOS structures

Figure 2.6 shows the energy band diagrams of an ideal MOS structure at $V_{\text{gate}} = V_{\text{FB}}$ (a) and $V_{\text{gate}} = 0$ (b), which assumes that there is no excess charge in the oxide or at the oxide/semiconductor interface. Here $\chi_{\text{ox}}$ is the electron affinity of the oxide, $\chi_S$ is the electron affinity of the semiconductor, $V_{\text{FB}}$ is the flat-band voltage, $E_i$ is the intrinsic level of the semiconductor (near the middle of the semiconductor band gap), $\psi_B$ is the potential difference between $E_F$ and $E_i$, and $\psi_s$ is the surface potential. The flat-band voltage $V_{\text{FB}}$ is defined as the applied gate voltage $V_{\text{gate}}$ such that there is no band bending in the semiconductor [24]. The surface potential $\psi_s$ is the potential difference between $E_i$ measured at the surface and $E_i$ measured deep in the bulk semiconductor (representing the band bending at the semiconductor surface). According to this definition [1], for a p-type semiconductor, $\psi_s$ is positive when the bands bend downward and $\psi_s$ is negative.
when the bands bend upward. Here we only consider a p-type semiconductor, but the same basic physics also apply for a n-type semiconductor.

At $V_{gate} = V_{FB}$, there is no band bending in the semiconductor and $\psi_s$ is 0 (Figure 2.6(a)). From the energy band diagram, one can get the energy barrier between the metal and the oxide given by

$$\phi_{bar} = W_m - \chi_{ox}.$$  \hspace{1cm} (2.18)

And one can also obtain

$$V_{FB} = \frac{W_m - W_s}{q}.$$  \hspace{1cm} (2.19)

As in Figure 2.6 (a), $W_m < W_s$, so the $V_{FB}$ is smaller than zero. For an ideal MOS structure with $W_m = W_s$, $V_{FB}$ is equal to zero and there is no band bending in the semiconductor without applying any gate voltage.

Figure 2.6 (b) shows the energy band diagram of the MOS structure at $V_{gate} = 0$. Since $W_m$ is smaller than $W_s$ as in Figure 2.6(b), the Fermi level of the metal is higher than the Fermi level of the semiconductor before the metal and the semiconductor are connected. If a wire is connected between the metal and the semiconductor, the electrons will flow from the metal to the semiconductor to build up some positive charge in the metal surface and an equal amount of negative charge distributed over the depletion region of the semiconductor so that the Fermi levels on both sides are lined up. This would cause a voltage drop across the oxide ($\Delta V$) and some bands bending in the semiconductor with a positive surface potential $\psi_s$ as in Figure 2.6(b). From the band alignment in Figure 2.6(b) we can get
Figure 2.6: Energy band diagrams of the MOS structure at flat-band condition ($V_{\text{gate}} = V_{\text{FB}}$) (a) and $V_{\text{gate}} = 0$ (b), assuming there is no oxide charge and the oxide resistivity is infinite.
Figure 2.7: Energy band diagrams of the MOS structure at accumulation ($\psi_s < 0$) (a) and inversion ($\psi_s > \psi_B > 0$) (b), assuming there is no oxide charge and the oxide resistivity is infinite.
\[ W_m - \chi_{ox} + q\Delta V = W_s - \chi_{ox} - q\psi_s. \]  

(2.20)

And Eq. 2.20 can be simplified to be

\[ q(\Delta V + \psi_s) = W_s - W_m = -qV_{FB}, \]

(2.21)

and

\[ \Delta V + \psi_s = -V_{FB}. \]

(2.22)

So the contact potential difference between the metal and the semiconductor \((W_m-W_s)\) are distributed across the oxide and the semiconductor depletion region at \(V_{gate} = 0\).

Figure 2.7(a) shows the energy band diagram of the MOS structure at \(V_{gate} < V_{FB} < 0\). At this negative gate voltage, there are negative charge built up at the metal surface and there are holes accumulated at the semiconductor surface. The semiconductor bands bend up and the \(\psi_s\) is negative. And from the band alignment in Figure 2.7(a) one can get

\[ \Delta V + \psi_s = V_{gate} - V_{FB}. \]

(2.23)

Eq. 2.23 shows that the additional applied negative gate voltage \((V_{gate} - V_{FB})\) is partially dropped across the oxide \((\Delta V < 0)\) and partially dropped across the semiconductor accumulation region \((\psi_s < 0)\) as compared to the case of \(V_{gate} = V_{FB}\) in Figure 2.6(a) where the bands are flat everywhere. Note that at \(V_{gate} = 0\), Eq. 2.23 yields to Eq. 2.22.

According to Eq. 2.23 the bands will bend more with larger positive \(V_{gate}\), as shown in Figure 2.7(b). When the \(E_i\) of the semiconductor bends below the Fermi-level at the semiconductor surface \((\psi_s > \psi_B)\), the number of electrons (minority carriers) at the surface is larger than the number of holes (majority carriers), and the surface is inverted [1]. So right at the semiconductor surface, it behaves like a n-type semiconductor.
Since right at the oxide/semiconductor interface, the \( x \) component of the electric displacement field is continuous (\( \vec{x} \) is perpendicular to the semiconductor surface), one can obtain

\[
e_{\text{ox}} E_{\text{ox}} = e_x E_x. \tag{2.24}
\]

And if there is no free charge in the oxide (as assumed in Figure 2.6 and 2.7), the oxide electric field \( E_{\text{ox}} \) is constant throughout the whole oxide thickness (\( \Delta t \)) and the voltage drop across the oxide is

\[
\Delta V = -E_{\text{ox}} \Delta t. \tag{2.25}
\]

As discussed in details in reference [1], one can solve the one-dimensional Poisson equation of the potential \( \psi \) (band bending) as a function of distance \( x \) and then get the relationship between the surface potential \( \psi_s \) and its electric field \( E_s \) given by

\[
E_s^2 = \frac{2kT}{e_s} p_{p0} \left[ \left( e^{\frac{-q\psi_s}{kT}} + \frac{q\Psi_s}{kT} - 1 \right) + \frac{n_{p0}}{p_{p0}} \left( e^{\frac{q\psi_s}{kT}} - \frac{q\Psi_s}{kT} - 1 \right) \right], \tag{2.26}
\]

where \( p_{p0} \) and \( n_{p0} \) are the equilibrium densities of electrons and holes deep in the bulk of the semiconductor. For a \( p \)-type semiconductor \( p_{p0} = N_A \) (\( N_A \) is the concentration of acceptors of the \( p \)-type semiconductor) and \( p_{p0} \gg n_{p0} \), then if \( \psi_s \) is not very large (\( \psi_s < \frac{2kT}{q} \text{Ln} \left( \frac{p_{p0}}{n_{p0}} \right) \)), we can simplify Eq. 2.26 to get

\[
E_s^2 = \frac{2kT}{e_s} N_A \left( e^{\frac{q\psi_s}{kT}} + \frac{q\Psi_s}{kT} - 1 \right). \tag{2.27}
\]
(a) Uniformly distributed negative charge in oxide

Figure 2.8: (a) Schematic illustration of the oxide bands bending with the presence of a uniformly distributed negative oxide charge. \( \Delta \phi \) is the potential difference between the middle and the boundary of the oxide. (b) Energy band diagram of the MOS structure at inversion with an assumed uniformly distributed negative charge in the oxide. The position of the oxide left surface is defined as \( x = 0 \).
And from Eq. 2.23, 2.24 and 2.25 one can obtain

\[- \frac{\varepsilon_s E_s}{\varepsilon_{ox}} \Delta t + \psi_s = V_{\text{gate}} - V_{FB}. \]  \hspace{1cm} (2.28)

Combining Eq. 2.27 (or Eq. 2.26) and Eq. 2.28, one can now solve for \( \psi_s \) at any \( V_{\text{gate}} \). So we can theoretically calculate the detailed energy band alignment of the MOS structure at any applied \( V_{\text{gate}} \) (and so the dependence of the metal-oxide barrier height \( \phi_{\text{bar}} \) on \( V_{\text{gate}} \), with the image-force lowering effect included).

In some cases there may be charge trapped in the oxide film, which would cause band-bending within the oxide. For example, if there is charge uniformly distributed in the oxide with a certain bulk density \( (n_{\text{bulk}}) \), the oxide bands would then bend as shown in Figure 2.8 (a) (negative oxide charge assumed), assuming that the potential at both front and back surface of the oxide are the same. We can solve the one dimensional Poisson equation

\[ \frac{d^2 V}{d^2 x} = -\frac{n_{\text{bulk}}}{\varepsilon_{ox}} \]  \hspace{1cm} (2.29)

to get the potential \( V \) as a function of distance in the oxide. If the potential \( V \) is defined as zero at the both oxide surfaces \( (V(x = 0) = 0 \) and \( V(x = \Delta t) = 0) \), we can obtain

\[ V(x) = \frac{n_{\text{bulk}}}{2\varepsilon_{ox}} (x - \frac{\Delta t}{2})^2 - \frac{n_{\text{bulk}}}{8\varepsilon_{ox}} (\Delta t)^2. \]  \hspace{1cm} (2.30)

And the potential at the middle of the oxide is \( V(x = \frac{\Delta t}{2}) = -\frac{n_{\text{bulk}}}{8\varepsilon_{ox}} (\Delta t)^2 \).

For a MOS structure, if there are charge uniformly distributed in the oxide, the oxide bands would also bend, however the potential at both front and back surface of the
oxide won’t necessarily be equal (in Figure 2.8 (b)). In this case the boundary condition for Eq. 2.29 would depend on the MOS capacitor properties and the applied bias $V_{\text{gate}}$. Since now the potential profile in the oxide is curved, Eq. 2.25 becomes

$$\Delta V = \frac{n_{\text{bulk}} (\Delta t)^2}{2\varepsilon_{\text{ox}}} - E_{\text{ox}} \Delta t,$$  \hspace{1cm} (2.31)

and Eq. 2.28 becomes

$$\frac{n_{\text{bulk}} (\Delta t)^2}{2\varepsilon_{\text{ox}}} - \frac{\varepsilon_{\text{s}} E_{\text{s}}}{\varepsilon_{\text{ox}}} \Delta t + \psi_s = V_{\text{gate}} - V_{\text{FB}}.$$

(2.32)

Combining Eq. 2.27 (or Eq. 2.26) and Eq. 2.32, one can again solve for $\psi_s$ at any $V_{\text{gate}}$. In the following chapter 4 and 5, we will use these equations to theoretically calculate dependence of the metal/oxide barrier height $\phi_{\text{bar}}$ on $V_{\text{gate}}$, including image-force lowering.

### 2.2.2 C-V characteristics

The capacitance versus voltage or C-V characteristics of a MOS capacitor is widely used to obtain the basic information of a MOS device, such as the flat-band voltage of a MOS capacitor, possible charge in the oxide or at the oxid/Si interface, etc. [24].

Here we will first consider the ideal C-V characteristics of a MOS capacitor without charge in the oxide or at the oxide/Si interface. Figure 2.9 shows the charge distribution in the MOS structure at accumulation ((a)) and depletion ((c)), and their corresponding simplified circuit diagrams ((b) and (d)) respectively. When the MOS capacitor is at accumulation, any small differential change in voltage would cause a differential change in charge in the metal film and also a change in holes accumulated at
Figure 2.9: Charge distribution in a MOS capacitor at accumulation ((a)) and depletion ((c)), and their corresponding simplified circuits ((b) and (d)) respectively.
the semiconductor (assumed p-type) surface [24], so the capacitance (per unit area) of the MOS capacitor (as in Figure 2.9(b)) is the same as the oxide capacitance (per unit area) given by

$$C(\text{accumulaion}) = C_{\text{ox}} = \frac{\varepsilon_{\text{ox}}}{t_{\text{ox}}},$$

(2.33)

where $t_{\text{ox}}$ is the oxide thickness. However, when the MOS capacitor is at depletion, there is a space charge region with depletion width of $x_d$. Any small differential change in voltage would cause a differential change in charge in the metal film and also a change in holes at the edge of the depletion region. So now we can think of the the oxide capacitance $C_{\text{ox}}$ and the capacitance of the semiconductor depletion region $C_D$ as connected in series as shown in Figure 2.9(d). In this case the capacitance of the MOS capacitor is given by [24]

$$C(\text{depletion}) = \frac{C_{\text{ox}} C_D}{C_{\text{ox}} + C_D} = \frac{\varepsilon_{\text{ox}}}{t_{\text{ox}} + \left(\frac{\varepsilon_{\text{ox}}}{\varepsilon_s}\right)x_d}.$$  

(2.34)

When $\psi_s = \psi_B$, the width of the depletion region $x_d$ reaches its maximum value (named $x_{dT}$) and there is no inversion charge at the semiconductor surface. So this condition yields a minimum capacitance $C_{\text{min}}$ given by [24]

$$C_{\text{min}} = \frac{\varepsilon_{\text{ox}}}{t_{\text{ox}} + \left(\frac{\varepsilon_{\text{ox}}}{\varepsilon_s}\right)x_{dT}}.$$  

(2.35)

When $\psi_s > 2\psi_B$, the MOS capacitor is in strong inversion condition and any small differential change in voltage would cause a differential change in electrons at the semiconductor surface. So the capacitance of MOS at strong inversion is again the same
Figure 2.10 (adopted from Reference 24): (a) Characteristic $C-V$ curves of a MOS capacitor measured at low (dashed curve) and high frequency (solid curve). (b) Shift of the $C-V$ curves due to positive charge at the oxide/semiconductor interface (both measured at high frequency).
as oxide capacitance $C_{ox}$, as shown in the $C-V$ curve in Figure 2.10(a) measured with low frequency. When the $C-V$ curve is measured with high frequency, the electrons (minority carriers) accumulated at the semiconductor surface can’t be created or removed fast enough, so the differential change in charge needed to produce the differential change in voltage would need to occur at the edge of the depletion region. So in this case the capacitance of the MOS capacitor remains at the minimum value even at large applied $V_{gate}$.

$C_{FB}$ shown in Figure 2.10(a) is the flat-band capacitance of a MOS capacitor at $V_{gate} = V_{FB}$, given by [24]

$$C_{FB} = \frac{\varepsilon_{ox}}{t_{ox} + \left(\frac{\varepsilon_{ox}}{\varepsilon_{s}}\right) \left[\frac{kT}{q}\left(\frac{\varepsilon_{s}}{eN_A}\right)\right]}.$$  \hfill (2.36)

So the flat-band voltage $V_{FB}$ (and so the work function difference between the metal and semiconductor) of a MOS capacitor could be obtained from the $C-V$ measurements.

Next we will consider the $C-V$ characteristics of a MOS capacitor with charge at the oxide/Si interface. As shown in Figure 2.10(b), the $C-V$ curve of the MOS capacitor is found to shift due to the presence of an interface oxide charge. For the pink dashed curve in Figure 2.10(b), a fixed positive interface charge of density $Q_{ss}$ is assumed in the oxide/semiconductor surface. As discussed in section 2.2.1 for the band bending in semiconductor, one can get [24]

$$V_{FB} = \frac{W_m - W_s}{q} - \frac{Q_{ss}}{C_{ox}}.$$  \hfill (2.37)

31
Eq. 2.37 predicts that the $C-V$ curve of the MOS capacitor would shift to more negative gate voltage with the presence of positive oxide/semiconductor surface charge as shown in Figure 2.10(b). Hence, we can use the measured flat-band voltage $V_{FB}$ to determine if there is fixed charge in the oxide bulk or at the Si/oxide interface.
CHAPTER 3

Experimental Methods

3.1 Internal Photoemission (Int-PE)

Determining and controlling conduction and valence band offsets at buried dielectric/channel and dielectric/gate interfaces is important for future CMOS technologies. The technique of Internal Photoemission (Int-PE) [25,26] is a valuable tool for determining these band offsets in a variety of dielectric materials, since it can, in principle, directly measure the energy barrier height at either buried interface of a metal-dielectric-semiconductor stack. This is done by analyzing measured photo-current spectra to determining the minimum (threshold) photon energy necessary to excite electrons (holes) into the conduction (valence) band of the dielectric film.

The Internal photoemission process can be defined as photon-stimulated transition of charge carriers from one solid into another over the barrier height at their interface [26,27], which is similar as the photoemission process except that for photoemission the charge carriers would make a transition from solid into the vacuum [28]. In this section, I will first briefly review the simplest theoretical model of Int-PE proposed by Powell [27],
which was widely used to fit the experimental Int-PE data in literature (other more sophisticated models to describe the photoemission process could be found in references [28-33]). Then it is followed by an introduction of the Int-PE experiment setup. Finally, typical Int-PE and photoconductivity (PC) studies on a MOS capacitor will be discussed shortly. We note that Int-PE can be applied to metal/semiconductor and metal/insulator/semiconductor samples. In this chapter we focus on how Int-PE is applied to MOS structures.

3.1.1 A simple theoretical model of Int-PE

The internal photoemission process is most successfully described [26-30] as a process composed of three consecutive steps as illustrated in Figure 3.1: (a) the injected photons stimulate carriers in a solid; (b) photoexcited carriers transport to the surface or interface of the emitter; (c) photoexcited carriers escape from the surface into vacuum or enter into another solid by surmounting the potential barrier.

In Powell’s simple theoretical model [27], the first two processes are simply accounted for describing the energy distribution of excited carriers at the emitter surface, $N(E, h\nu)$, where $E$ is the energy of the exited carrier and $h\nu$ is the photon energy. The escape process was described as an energy-dependent surface transmission probability $P(E)$ using the well known Fowler condition [12]

$$
    P(E_n) = \begin{cases} 
        1 & \text{if } E_n > \phi_{bar} \\
        0 & \text{if } E_n < \phi_{bar}
    \end{cases}
$$

(3.1)
Figure 3.1 (adopted from Reference 26): Schematic representation of Int-PE process: (a) carrier photoexcitation, (b) transport to the emitter surface, and (c) escape over the potential barrier at the interface.

where $E_n$ is the kinetic energy normal to the surface, $\phi_{\text{bar}}$ is the energy barrier between the metal and insulator as in Figure 3.1. In terms of the total energy $E$, the transmission probability is given by [27]

$$P(E) = \begin{cases} C(E - \phi_{\text{bar}}) & \text{if } E > \phi_{\text{bar}} \\ 0 & \text{if } E < \phi_{\text{bar}} \end{cases},$$

(3.2)

where $C$ is a constant. For Eq. 3.1 and 3.2, relaxation of the momentum conservation at the emitter surface is assumed [27,28]. Powell argued that this simplification is appropriate because [27]: (1) simultaneous conservation of energy and crystal momentum are not possible for the photon and electron energy ranges considered; (2) multiple bands
contribute to the density of states of the initial or final states; (3) the effects of scattering
confine the initial and final states wave functions to small spatial extent.

So the Int-PE quantum yield $Y$ (the number of emitted electrons normalized to the
number of absorbed photons) may be written [27]

$$Y(h\nu, \phi_{\text{bar}}) = \int_{\phi_{\text{bar}}}^{h\nu} N(E, h\nu)P(E)dE,$$ (3.3)

with $N(E, h\nu)$ given by

$$N(E, h\nu) = AN_o(E - h\nu)N_u(E)|M_{if}|^2 S(E, h\nu),$$ (3.4)

where $N_o$ is the density of initial (occupied) states, $N_u$ is the density of final (unoccupied)
states, $M_{if}$ is the matrix element coupling initial and final states, and $S(E, h\nu)$ is the
electrons scattering factor. Assuming $N_u(E), M_{if}$, and $S(E, h\nu)$ are approximately constant
over small energy ranges, $N(E, h\nu)$ becomes a function of $(E - h\nu)$ only [27] as given by

$$N(E, h\nu) = N(E - h\nu).$$ (3.5)

From Eq. 3.2, 3.3 and 3.5, one can obtain

$$Y(h\nu, \phi_{\text{bar}}) = C\int_{\phi_{\text{bar}}}^{h\nu} N(E - h\nu)(E - \phi_{\text{bar}})dE.$$ (3.6)

And the quantum yield usually can be expressed as follows:

$$Y(h\nu) = A(h\nu - \phi_{\text{bar}})^p,$$ (3.7)

if $h\nu > \phi_{\text{bar}}$, where $p$ depends on the energy distribution of excited carriers at the emitter
surface [27].

For the metal emitters, it should be a good first order approximation to assume
that $N(E - h\nu)$ is a step function ($\alpha U(h\nu - E))$ [27,28], where $\alpha$ is a constant. However for
many semiconductors, it was observed experimentally in vacuum photoemission that \( N(E - h\nu) \) is a linear ramp \( (\alpha \cdot (h\nu - E)) \) [27,29]. So for Eq. 3.7, we would then get \( p = 2 \) for the quantum yield for carriers emitted from metal into insulator, and \( p = 3 \) for the quantum yield for carriers emitted from semiconductor into insulator. So the \( \phi_{\text{bar}} \) at the metal/insulator interface or the semiconductor/insulator interface could be experimentally determined by linear extrapolating the measured \( Y^{1/2} \) or \( Y^{1/3} \) to zero yield [25,26], which will be discussed in detail in the next subsection.

### 3.1.2 Experimental setup of Int-PE

Figure 3.2 shows the experimental setup of our Int-PE that we applied to MOS capacitors. A 150 watt Xenon (or 90 watt Tungsten-Halogen) light source and a ¼ meter light-path diffraction-grating monochromator are used to provide monochromatic photons with energy range from 1.8 eV to 6.5 eV (or from 0.7 eV to 1.8 eV). The proper light source would be chosen based on the expect measured barrier height, for example the Xenon light source is chosen to study the MOS capacitors since almost all the barrier heights at the metal/oxide and semiconductor/oxide interface are larger than 2 eV. Since the light coming out of the monochromator actually includes a small amount of high order diffracted light (at multiples of the energy of the lowest-order light), a suitable long-wavelength (low-energy) pass filter would then be chosen to fileter out the higher-order light. After that, a concave reflector is used to focus the light into an optical fiber and the optical fiber would then guide the light to shine on the sample surface (metal film electrode). A semi-transparent metal (~10-30 nm in thickness) or semiconductor electrode [26] or an optically transparent conducting electrolyte contact [35] needs to be
chosen to allow photoexcitation of charge carriers at both the metal/oxide and semiconductor/oxide interfaces. Finally the photocurrent is collected from the substrate as in Figure 3.2. We note a voltage is normally applied across the MOS sample to create a strong electric field in the oxide to sweep injected carriers across the oxide film and enhance the photocurrent. In order to suppress dark current, environmental light needs to be carefully excluded.

![Figure 3.2: Schematic of experimental setup of Int-PE.](image)

150 watt Xenon or 90 watt Tungsten-Halogen lamp → Monochromator → filter → concave reflector → optical fiber → Metal oxide → Silicon

$I$ $V_{gate}$
The quantum yield and photocurrent are related by

\[ I = \frac{P}{h \nu} \cdot Y, \]

where \( I \) is the photocurrent in number of electrons, \( P \) is the power of absorbed light, and \( h \nu \) is the photon energy [27]. The power of the absorbed light \( P \) is calibrated by inserting a photodiode (with known spectral response, defined as \( I/P \) a function of photon frequency) at the same place as the sample to measure its photocurrent.

### 3.1.3 Int-PE measurements on MOS capacitor

Figure 3.3 shows typical Int-PE measurements on a MOS capacitor at both forward \((V_{\text{gate}} < 0)\) (a) and reverse \((V_{\text{gate}} > 0)\) (b) biases. One can easily see from Fig. 3.3 that for Int-PE carriers excited on both sides of the oxide may contribute to the photocurrent: For the forward bias case (Fig. 3.3(a)) there could be (1) electrons excited from the metal transporting across the oxide conduction band (CB), or (2) holes excited in the semiconductor valence band (VB) transporting across the oxide VB. For the reverse bias case (Fig. 3.3(b)) there could be (3) holes excited in the metal transporting across the oxide VB; (4) electrons excited from the semiconductor VB transporting across the oxide CB. Since the measured Int-PE current is the sum of all of these processes, it is common to enhance the current from particular processes by applying a large metal bias \( V_{\text{gate}} \) to create a large “forward” (or “reverse”) electric field \( E_{\text{ox}} \) that pushes electrons toward the semiconductor and holes toward the metal (or pushes electrons toward the metal and holes toward the semiconductor). The forward and reverse electric field correspond to \( E_{\text{ox}} < 0 \) and \( E_{\text{ox}} > 0 \) (the electric field is defined as positive if it points from the metal to the semiconductor), respectively, as in Figure 3.3. The intrinsic barrier heights (BHs) are
Figure 3.3: Int-PE measurements on a MOS capacitor at forward ($V_{\text{gate}} < 0$) (a) and reverse ($V_{\text{gate}} > 0$) (b) biases. Four different processes which might contribute to the photocurrent and their corresponding energy barriers needed to be overcome are shown respectively.
determined by extrapolating measured BHs to zero $E_{ox}$ [25,26]. Note that creation of electron-hole pairs (at sufficiently high photon energy) within the oxide could also contribute to the photocurrent (PC measurement), which will be discussed later.

However even at large positive or negative gate voltage, there are still two processes might contribute to the current simultaneously. For example, for large negative gate voltage (Figure 3.3(a)), electrons excited from the metal and holes excited from the semiconductor VB both might contribute to the current. This makes it very hard to immediately indentify the major process contributing to the photocurrent, and so to determine the corresponding interface BH. One way to address this difficulty [26] is by comparing Int-PE characteristics of various metals (with very different work functions) on the same oxide/semiconductor. As in Figure 3.3(a), the barrier height ($\phi_{bar1} = W_m - \chi_{ox}$) at the metal/oxide interface would increase linearly with the metal work function $W_m$, while the barrier height ($\phi_{bar2} = E_c(\text{semiconductor}) - E_v(\text{oxide})$) at the semiconductor/oxide interface is independent of $W_m$. Note most metal/oxide interfaces do not have significant interface state density, and so the ideal Schottky model introduced in Chapter 2 is suitable for relating the barrier height to metal work function. So a change of $W_m$ would lead to a shift of Int-PE spectra threshold if the photocurrent is dominated by the process happening at the metal side. However if there is no Int-PE spectra shift observed, the dominant contribution to the current comes from the semiconductor side [26].

Figure 3.4 shows an example Int-PE measurement from our lab on a Pt/epi-Sc$_2$O$_3$/Si MOS sample. For this particular case, at $V_{gate} = 1.5V$ (reverse $E_{ox}$ as in Figure 3.3(b)), electrons excited from the Si VB dominate the photocurrent, Int-PE probes the
BHs at the Sc$_2$O$_3$/Si interface. As we discussed in section 3.1.1, the quantum yield $Y$ is proportional to $(h\nu - \phi_{bar})^3$ for the semiconductor emitter. So we linear extrapolate the measured $Y^{1/3}$ data to zero yield to determine the barrier height at the Sc$_2$O$_3$/Si interface. There are obviously two thresholds in $Y^{1/3}$ data as in Figure 3.4. In order to get the higher threshold, current with a lower threshold was first subtracted. The modified $Y^{1/3}$ data was then linearly extrapolated to zero yield to get the higher barrier height. At $V_{gate} = 0$ V (forward $E_{ox}$ as in Figure 3.3(a)), electrons excited from the metal dominate the photocurrent, Int-PE probes the BH at the Pt/Sc$_2$O$_3$ interface. Since the quantum yield $Y$
is proportional to \((h\nu - \phi_{\text{bar}})^2\) for the metal emitter, we linearly extrapolate the measured \(Y^{1/2}\) data to zero yield to determine the barrier height at the Pt/Sc\(_2\)O\(_3\) interface. Since for the Powell model [27], temperature effects (thermal broadening) are not included, a certain range of Int-PE data with the lowest photon energy several \(k_B T\) (~0.1 eV) higher than the barrier height was chosen for the linear fits.

For sufficient high photon energy, hot electron-hole pairs are also created within the oxide and also produce a current, which is designated as photoconductivity (PC), as shown in Figure 3.5. The sign of the PC current depends on the oxide electric field \(E_{\text{ox}}\). Of course some Int-PE processes (not shown in Figure 3.5) still happen and contribute to the photocurrent at such high photon energies. The intrinsic PC quantum yield of the oxide is found to be proportional to \((h\nu - E_g)^2\) [9,26,36], where \(E_g\) is the oxide band gap. So after subtracting the current contributed by lower Int-PE thresholds, the PC threshold \(E_g\) would be determined by linearly extrapolating the \(Y^{1/2}\) data to zero yield, similar to the fitting procedure for the multiple thresholds case discussed above. Since the intrinsic PC current usually dominates the total photocurrent at high photon energy, it makes it relative easy to fit the experimental PC data.

Finally I would like to discuss how accurately Int-PE spectral thresholds could be determined. The uncertainty in Int-PE threshold determination could come from the following sources [26]: (1) the uncertainty in photon energy due to the resolution of the Monochromator (~0.01-0.03 eV); (2) fluctuations of the dark current and photocurrent; (3) the uncertainty stemming from the light source intensity calibration; (4) the uncertainty to determine the zero quantum yield point; (5) the uncertainty of
Figure 3.5: PC measurements on a MOS capacitor at forward ($V_{\text{gate}} < 0$) (a) and reverse ($V_{\text{gate}} > 0$) (b) biases. PC current is negative at $V_{\text{gate}} < 0$ (a), and is positive at $V_{\text{gate}} > 0$ (b). Note Int-PE processes are not shown.
extrapolating thresholds measured at different electric fields to zero field to get the intrinsic threshold; and (6) the fact that the Powel power-law model is a simplification of the actual physics situation, so the \((\text{Yield})^{1/2}\) or \((\text{Yield})^{1/3}\) fits might actually not be perfectly linear. Since there is always sub-threshold photocurrent due to Int-PE of band tails or photoionization of localized electron states etc. [26], it makes it very difficult to accurately determine the zero quantum yield point, which would strongly depend on how the sub-threshold current is subtracted and which data range was used to fit. So the uncertainty of determining the zero quantum yield point (with uncertainty ranging from \(\pm 0.03\) to \(\pm 0.08\) eV [26]) was believed to be the largest source of uncertainty in our Int-PE threshold determinations, consistent with the typical \(\pm 0.05\) to \(\pm 0.10\) eV uncertainties quoted in the literature [26]. As a consistency check, we made multiple measurements of the same energy barrier, and the results were reproducible to the above quoted uncertainties.

### 3.2 Ballistic Electron Emission Microscopy (BEEM)

BEEM, which is an extension of Scanning Tunneling Microscopy (STM) [37], was first used by Kaiser and Bell to study the microscopic properties of metal/semiconductor Schottky barriers [38,39], and was subsequently applied to the study of MOS structures [40-44]. It uses similar physics as Int-PE to measure the SBH at the metal/semiconductor interface or BH at the metal/insulator interface except that carriers can only be injected from metal side by a biased STM tip. Since for BEEM carriers were injected only from metal side, it makes it much easier to interpret BEEM spectra than Int-
PE spectra, which could have multiple processes happening at the same time. Another major advantage of BEEM over Int-PE is that BEEM has much higher spatial (~10 nm) resolution, and in many cases higher energy resolution (~10 meV) than Int-PE does. However, one major disadvantage of BEEM compared to Int-PE is that BEEM can only work in a very restricted environment: it needs a very thin and “clean” metal film that does not oxidize (often requiring measurements to be made in ultra high vacuum) and the STM tip might not be stable at high tip voltages (>3 V), particularly for “soft” metals such as Au, and when there is water vapor or other contaminants on the surface [45].

In this section, the configuration of BEEM technique will be first introduced, followed by a brief introduction of two basic BEEM operational modes, which I refer to as taking “BEEM images” and “BEEM spectra,” respectively. Then I will briefly review the Bell-Kaiser model [38,39], which is widely used to fit experimental BEEM spectra to determine the SBH at the metal/semiconductor interface or BH at the metal/insulator interface. Finally typical BEEM studies on MOS structures will be discussed shortly. Detailed review of the BEEM technique can be found in references [46] and [47], if the reader is interested in it.

3.2.1 Configuration of BEEM

The configuration of the BEEM technique for metal/semiconductor (M/S) structure and the corresponding energy level diagrams is shown in Figure 3.6. Compared to STM (which is a two-terminal measurement (tip and substrate)), BEEM has one more terminal to contact a thin layer of metal film on top of semiconductor (or oxide/semiconductor). When the STM tip is brought close to the metal film with a
negative bias (corresponding to $V_T > 0$ with polarities defined in Figure 3.6(a)), electrons will be locally injected from the tip into the metal film with a range of energy close to the Fermi level of the tip, which is $eV_T$ above the Fermi level in the metal film. The hot-electron energy, location, and flux can be controlled by varying the voltage, position, and tunnel current of the tip, respectively. Provided the metal film is sufficiently thin (comparable with the electron mean-free-path in the metal, typically ~10 nm for noble metals such as Au or Cu), a fraction of the injected hot electrons can transport across the metal film and reach the metal/oxide interface without losing significant energy. Some of the hot electrons having sufficient energy to overcome the energy barrier at the M/S interface can enter into the Si substrate and be collected as the external current $I_c$ (often referred as the “collector current” or “substrate current” in BEEM) while others will be scattered back into the metal and will drain out through the third contact to the metal film. The local Schottky barrier height (SBH) at the M/S contact can be determined as $SBH = eV_{th}$, where $V_{th}$ is the threshold tip voltage for electrons to cross the M/S interface.

A similar configuration of the BEEM technique for metal/oxide/semiconductor (MOS) structure and the corresponding energy level diagrams will be shown in Figure 3.9 in section 3.2.4, accompanied with detailed discussion of an example BEEM study on a MOS capacitor.
Figure 3.6: Schematic configuration of BEEM experiment on M/S contact (a) and the corresponding energy level diagram (b). The horizontal axis in (b) corresponds to the z axis in (a).
3.2.2 Example BEEM spectra and images

There are two basic BEEM working modes: BEEM spectra and BEEM images. For both BEEM modes the tunneling current $I_T$ is kept constant (~10 nA) by a feedback loop in the STM control electronics. So as the tip scans across the sample surface, the STM feedback loop will control the movement of the piezocrystal scanner in $z$ direction to keep the same distance between the tip and sample surface so that to maintain constant $I_T$. The relative movement of the piezocrystal scanner in the $z$ direction will be recorded and so the topography of the sample surface will then be obtained. Figure 3.8(a) shows the example STM topography of 10nm thick Au/n-type bulk Si, obtained by plotting the height ($z$-position) of the STM tip as color-scale, as a function of the lateral ($x$- and $y$-) position of the tip. This image was measured with the tip voltage $V_T = 1.00$ V and tip current $I_T = 10$ nA. Au grains can be seen clearly with a size comparable to the metal film thickness.

One major BEEM working mode is the taking of BEEM spectra. A example average BEEM spectrum (also referred to as a BEEM $I_c$-$V_T$ curve) of an Au/n-type Si interface is shown as the open-circle data points in Figure 3.7. In this mode, the STM tip is held at a fixed $x$-$y$ lateral location, and an individual BEEM $I_c$-$V_T$ curve will be taken by linearly increasing the tip voltage up to a certain value much higher than the expected threshold voltage ($V_{th}$). The BEEM $I_c$-$V_T$ curves (typically ~50) taken at different locations during the scan can, if desired then be averaged to get the average BEEM $I_c$-$V_T$ spectrum. Note of course individual BEEM $I_c$-$V_T$ curves could also be analyzed if the signal-to-noise is sufficiently high, but usually several BEEM $I_c$-$V_T$ curves are averaged
together to improve the signal-to-noise. As in Figure 3.7, a “turn-on” of the BEEM current around 0.8 eV can be clearly seen in the $I_c-V_T$ spectrum (open circles). By fitting the average BEEM $I_c-V_T$ curve using a conventional Bell-Kaiser (B-K) model fit (solid line in Figure 3.7), the SBH at the Au/n-type bulk Si interface (~0.8 eV) could then be obtained. A briefly review of the Bell-Kaiser theory will be give in the following subsection.

\[
\text{SBH} = eV_{th}^{\text{Au/n-Si}}
\]

**Figure 3.7**: Example average BEEM $I_c-V_T$ spectra (open circles) of 10nm thick Au/n-type bulk Si and the corresponding Bell-Kaiser fit (solid line). $I_T = 10$ nA.
Figure 3.8: Example STM topography (a) and BEEM image (b) of 10nm thick Au/n-type bulk Si.
Another major BEEM working mode is the taking of BEEM images. An example BEEM image (taken simultaneous with the STM topography shown in Fig. 3.8(a)) of Au/n-type bulk Si is shown in Figure 3.8(b). At this mode, the STM tip is hold at a voltage (1.00 V) higher than the expected threshold voltage of the sample (~0.8V for an Au/n-Si interface). So as the tip scans across the sample surface, a plot of BEEM current $I_c$ versus tip position will be obtained. The power of this mode is that it can possible distinguish the non-uniform distribution of barrier heights (if they exist) at the metal/semiconductor interface (or metal/oxide interface for MOS). For example, if there are two regions with different barrier heights ($\phi_{bar1}$ and $\phi_{bar2}$) mixed with each other in the sample, by setting a tip voltage between those two barrier heights, the region with lower barrier height would have a finite BEEM signal while the region with higher barrier height would not, in which case there would be a sharp contrast in the BEEM image. This mode has been demonstrated very powerful in finding the edge of quantum wells in previous self-forming 3C-SiC inclusion in 4H SiC [48,49] and AlGaAs/GaAs/AlGaAs [50] quantum well studies, and was used to find the vertical nanowires (NWs) embedded in SiO$_2$ in the study discussed in chapter 6. For the BEEM image of Au/n-type bulk Si sample shown in Figure 3.8 (b), there is BEEM current everywhere, even though the current amplitude varies with location. Since there were no substantial lateral variations in the measured SBH in this case, the measured variation of BEEM current with tip location was believed to come from local variations in electron transmittance through the metal film (due to variations in metal thickness or the crystal orientation of grains in the polycrystalline metal film) for this particular Au/n-type bulk Si sample.
3.2.3 The Bell-Kaiser Model

In Kaiser and Bell’s original paper, a simple one-dimensional theory was proposed to explain the fundamental characteristics of BEEM spectra [38]. The energy dependence of ballistic electron mean-free-path in the metal, the energy distribution of the electrons tunneling from the tip into the metal, and the quantum mechanical reflection of electrons at the metal/semiconductor interface are all neglected. This “Kaiser-Bell” model further assumes that the transmission probability of ballistic electron through the metal/semiconductor interface only depends on its total energy. According to this simple model [38], the BEEM collector current as a function of tip bias at constant $I_T$ is

$$I_c(V_T) = RI_T \int_0^\infty dE [f(E) - f(E - eV_T)] \times \theta(E - (E_F - eV_T + eV_{th})),$$  \hspace{1cm} (3.9)

where $R$ is the scaling factor independent of tip bias, $\theta$ is the Heaviside step function, and the Fermi function $f(E)$ is defined as

$$f(E) = \frac{1}{1 + \exp\left(\frac{E - E_F}{kT}\right)}.$$  \hspace{1cm} (3.10)

Eq. 3.9 is fitted to experimental BEEM spectra by adjusting $R$ and $V_{th}$ [38].

In their second paper (this time with Bell as the first author), conservation of both energy and transverse momentum at the metal/semiconductor interface was included [39]. This gives

$$\hbar k_{m,t} = \hbar k_{s,t}$$  \hspace{1cm} (3.11)

$$\frac{(\hbar k_{m,t})^2}{2m_e} + E_{m,z} = \frac{(\hbar k_{s,t})^2}{2m_t} + E_{s,z},$$  \hspace{1cm} (3.12)
where \( k_{m,t} \) and \( k_{s,t} \) are the transverse momentum of an electron in the metal and the semiconductor respectively, \( E_{m,z} \) and \( E_{s,z} \) are the z-components of the electron kinetic energy in the metal and semiconductor, \( m_e \) is the free electron mass, and \( m_t \) is the “transverse” electron effective mass parallel to the interface within the semiconductor.

From Eq. 3.11 and 3.12, one can obtain

\[
E_{m,t} + E_{m,z} = \frac{m_e}{m_t} E_{m,t} + E_{s,z},
\]

(3.13)

where \( E_{m,t} \) is the transverse component of energy in the metal. From Eq 3.13, one can immediately see that there is a restriction on the transverse energy \( E_{m,t} \) in the metal if \( m_t < m_e \) (\( m_t/m_e \) is 0.19 for Si and 0.067 for GaAs [1]). Since the minimum energy electrons needed to overcome the barrier height at the metal/semiconductor interface is

\[
E_{m,z,min} = E_F + eV_{th},
\]

(3.14)

one can get the restriction on the transverse energy in the metal given by

\[
E_{m,t} \leq \frac{m_t}{m_e - m_t} (E_{m,z} - E_F - V_{th}),
\]

(3.15)

with the maximum transverse energy \( E_{m,t,max} \) of \( \frac{m_t}{m_e - m_t} (E_{m,z} - E_F - eV_{th}) \) in the metal [39]. Since the perpendicular kinetic energy \( (E_z) \) in the tip is equal to \( (E_{m,z} - eV) \) and the transverse energy in the tip \( (E_t) \) is the same as the transverse energy in the metal \( E_{m,t} \), Eq 3.14 and 3.15 can be rewritten as

\[
E_{z,min} = E_F - e(V - V_{th}),
\]

(3.16)

and

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\[ E_t \leq \frac{m_t}{m_e - m_i} (E_z - E_F + e(V - V_{th})) \, , \quad (3.17) \]

with the maximum transverse energy \( E_{t,\text{max}} \) of \( \frac{m_t}{m_e - m_i} (E_z - E_F + e(V - V_{th})) \) in the tip [39]. Then the BEEM collector current as a function of tip bias at constant \( I_T \) becomes

\[ I_c = RC \int_{E_{z,\text{min}}}^{E_{z,\text{max}}} D(E_z) \int_{0}^{E_{z,\text{max}}} f(E) dE_t dE_z \, , \quad (3.18) \]

where \( R \) is the scaling factor as in Eq. 3.9, \( C \) is a constant, and \( D(E_z) \) is the transmission probability for an electron to tunnel through the vacuum barrier [39].

From the well-known formalism for tunneling between planar electrodes [51], the tunnel current from the tip into the metal is given by

\[ I_T = C \int_{0}^{\infty} D(E_z) \int_{0}^{\infty} \left[ f(E) - f(E + eV_T) \right] dE_t dE_z \, . \quad (3.19) \]

From Eq. 3.18 and 3.19, one can obtain [25]

\[ I_c = RI_T \frac{\int_{E_{z,\text{min}}}^{E_{z,\text{max}}} D(E_z) \int_{0}^{E_{z,\text{max}}} f(E) dE_t dE_z}{\int_{0}^{\infty} D(E_z) \int_{0}^{\infty} \left[ f(E) - f(E + eV_T) \right] dE_t dE_z} \, . \quad (3.20) \]

The Eq. 3.20 is then used to fit the experimental BEEM spectra to obtain the barrier height at the metal/semiconductor interface by adjusting the two free parameters \( R \) and \( V_{th} \). While the basic physics assumed by this refined model (often referred to as the “Bell-Kaiser model” is still controversial (in particular whether transverse momentum is conserved and whether hot-electrons in the metal can experience multiple elastic scattering events before crossing into the semiconductor), the fact is that this model fits
measured BEEM data very well for a variety of samples, and so is very widely used. An example fit using the Bell-Kaiser model is shown by the pink line in Fig. 3.7. We see that it fits the data very well, including in the near- and sub-threshold regions where thermal broadening of electrons in the tip allow some current to be measured even when the tip voltage is slightly below the SBH. The Bell-Kaiser model was used to fit our experimental BEEM data shown in chapter 4, 5, and 6.

3.2.4 Example BEEM studies on MOS structure

The configuration of the BEEM technique for metal/oxide/semiconductor (MOS) structure and the corresponding energy level diagrams is shown in Figure 3.9. In contrast to the configuration of BEEM on M/S shown in Figure 3.6, a large gate bias may be applied across the oxide for MOS structures without producing a large background current, provided the insulating oxide layer is sufficiently thick and resistive. This is generally not possible for M/S contacts, especially at room temperature and under forward bias. This is because the BEEM signal is usually very small (typically ~pA), which requires very low leakage current in the sample (the resistance of MOS is typically ~Tera Ohms, while the resistance of M/S contact is typically ~tens of Mega Ohms at room temperature).

As discussed in section 3.2.1, by monitoring the “threshold” tip voltage $V_{th}$ at which the BEEM current starts to turn on, the local energy barrier height $\phi_{bar}$ in the oxide film can be determined as $\phi_{bar} = eV_{th}$. And Figures 3.9(b) and (c) also show that the energy barrier in the oxide can be changed by changing the gate bias $V_{gate}$. For the “forward” electric field case as in Figure 3.9(b), BEEM probes the energy barrier at the
Figure 3.9: Schematic configuration of BEEM experiment on MOS structures (a) and the corresponding energy level diagrams for both forward (b) and reverse (c) oxide electric field. The horizontal axis in (b) and (c) corresponds to the z axis in (a). The metal/oxide (oxide/Si) interface is probed in (b) ((c)). In (c), hot electrons from the metal side must cross the oxide film against an electric field to contribute to the substrate current $I_c$. 
Figure 3.10: (a) Energy level diagram of MOS structure with fixed charge in the oxide. (b) Example Energy barrier $\phi_{\text{bar}}$ dependence on $V_{\text{gate}}$ with (dark circles) or without (blue triangles) fixed charge in the oxide and the corresponding model fits (solid lines), respectively. Data and fits in (b) are all taken from reference [44] for their Pd/10nm-SiO$_2$/Si study. The charge in the oxide is created on purpose by injecting hot electrons for an extended time period [44].
metal/oxide interface. The energy barrier will decrease slightly because of “image force lowering” [1] (see section 2.1.3) as \( V_{\text{gate}} \) is made more negative. For the “reverse” electric field case as in Figure 3.9(c), the maximum energy barrier location switches to the oxide/Si interface, and the energy barrier will increase linearly with \( V_{\text{gate}} \). Note in this case, hot electrons from the metal side must cross the oxide film against an electric field to contribute to the substrate current \( I_c \). Thus one can get the \( \phi_{\text{bar}} \) dependence on \( V_{\text{gate}} \) curve as shown in Figure 3.10(b) (dark circles) (Figure 3.10(b) is taken from Reference [44]). The black line in Figure 3.10(b) is the theoretical calculation of the \( \phi_{\text{bar}} \) dependence on \( V_{\text{gate}} \) using Eq. 2.27 and 2.28 discussed in section 2.2.1. By comparing the experimental data and the theoretical calculation, the intrinsic barrier height \( \phi_0 \) at the metal/oxide interface and the flat band voltage \( V_{\text{FB}} \) can be obtained as shown in Figure 3.10(b) [44]. Note that Figure 3.9 and the dark circles and the black line in Figure 3.10(b) all assume no trapped charge in the oxide film [44].

Figure 3.10 (a) shows an example energy level diagram of the Pd/SiO\(_2\)/Si structure with fixed charge in the oxide. One can easily see that at some \( V_{\text{gate}} \) the maximum barrier is located inside the oxide film, while it is either located at the metal/oxide or oxide/Si interface in Figure 3.9 assuming no charge in the oxide. Consequently one would get a much more gradual change of \( \phi_{\text{bar}} \) on \( V_{\text{gate}} \) as shown in Figure 3.10(b) (blue triangles). But one can still theoretically fit the \( \phi_{\text{bar}} \) on \( V_{\text{gate}} \) data by assuming some fixed charge in the oxide as the blue curve shown in Figure 3.10 (b) [44]. By doing so, the intrinsic barrier height \( \phi_0 \) and possible oxide charge information can be obtained. From a model fit to the experimental data in Figure 3.10 (b)), it was estimated
that an areal density of $\sim 1.3 \times 10^{13} \text{ cm}^{-2}$ injected electrons became trapped in the SiO$_2$ film (see Ref. [44]).

### 3.3 Experiment Setup

Two different BEEM systems were used in the study of this dissertation: a custom-built UHV STM/BEEM system which was first developed by Darrell Jones for STM study and then further upgraded to have BEEM capability by Benjamin Kaczer; and a BEEM-modified UHV Omicron varying temperature (VT) STM system that was first assembled and implemented by Eric Heller. Details about the constructions and upgrades of the home build UHV STM/BEEM system can be found in dissertations of Jones [52], Kaczer [45], and Heller [53]. Since most of the work done in this dissertation was using the home-built STM/BEEM system, a brief discussion of this experiment setup is given here, with more detailed discussion of this equipment found in Kaczer’s dissertation [45].

Figure 3.11 shows the normal experimental procedures of BEEM study. The sample was usually first cut into 9×20mm or 7×7 mm pieces, which are the best size to fit in two different sample holders (one type of sample holder was shown in Figure 3.13), respectively. The sample was then de-greased using a sequence of ultrasonic trichloroethylene, acetone, and methanol (each ~5-10 min), finally rinsed in de-ionized water. Special treatments might be needed to prepare the sample before being transported into the UHV chamber, which will be discussed in detail in the sample preparation section in chapter 4, 5 and 6 if appropriate. The sample was then put into the airlock connected to the UHV preparation chamber (as in Figure 3.12, taken from Park’s
dissertation [54]) and was pumped down using a turbo-pump station. After the pressure of the airlock reach $\sim 10^{-7}$ Torr, the gate valve between the airlock and the preparation chamber would be opened manually and the sample was transported into UHV. The base pressure in the UHV preparation and STM/BEEM chamber is usually $\sim 1-2 \times 10^{-10}$ Torr.

**Figure 3.11:** Schematics of experimental steps of the typical BEEM study.
Figure 3.12 (taken from Park’s dissertation [54]): Photograph of the custom-built UHV preparation chamber (right) and STM/BEEM chamber (left).
Figure 3.13 (taken from Ding’s dissertation [55]): Photograph of the BEEM measurement setup. The inchworm which controls the sample stage movement is not shown (located at the left side of the sample block). Inset: a close view of the tip and the gold wire. The gold wire is in contact with a particular metal dot, which can barely be seen. There is ~1 nm separation between the tip and the sample surface, even thought it looks like the tip is in contact with the sample. Mirror images (left side) of both the wire and the tip are clearly seen in the picture.
The sample was then heated to a pyrometer reading of ~ 340°C (for oxide samples) for 10 min to desorb water and hydrocarbons prior to deposition of the thin metal film, which was found to be crucial for oxide sample to get BEEM current. After that a thin metal film was deposited by electron beam evaporation through a shadow mask to form a number of 0.5 mm² diameter dots. It should be noted that for some types of metal deposition (such as Pt), only a small area of the source metal was evaporated, which would leave a hole in the source and might break the crucible if used for a long time. In order to avoid that, either the electron beam was swept during deposition or the electron beam voltage was manually changed from time to time to avoid continuously hitting one spot. All sample operation (grabbing or flipping) in the preparation chamber was handled by a manipulator (in Figure 3.12).

The sample was then transported into the UHV STM/BEEM chamber adjacent to the preparation chamber (as in Figure 3.12). A manipulator in this chamber was used to operate the sample transportation system. After the sample was put on the STM sample stage, an electric wire held by the manipulator was used to ground the metal dot. A conventional $I-V$ measurement was done to check whether the sample diodes (typically up to 19 diodes) are leaky or not. The diodes with the largest zero-bias resistance (and so the least noise) were then chosen for BEEM study.

The BEEM measurement setup is shown in Figure 3.13 (taken from Ding’s dissertation [55]). The tip (a Tungsten or Pt/Ir tip) is held at the end of the STM scanner which controls the $x$, $y$ and $z$ position of the tip relative to the sample surface during scanning. Since the maximum distance that a tip can be moved by the STM scanner is
limited (several μm), the STM scanner and the sample stage are connected with two “inchworms” which can move a large distance (~ 1 cm) with steps of several hundred nm. The coarse distance between the tip and the sample in x (or z) direction are controlled by the inchworm connected to the sample stage (or scanner). The y position of the tip is coarsely controlled by adjusting the tip vertical position relative to the scanner, using a fine-threaded screw in the STM base, which is manually turned using a mechanical feedthrough. After being brought close to the sample surface, the tip is finally brought into tunneling by the “Inchworm UHV3” program developed by Kaczer [45]. The final separation between the tip (in tunneling) and the sample is ~1 nm, which appears as direct contact in the zoom-in picture at the left corner of Figure 3.13. Since the working space is very limited in the STM chamber, a microscope is used to assist positioning of the tip and sample during these operations.

Finally the BEEM measurements are taken, which are controlled by an MS-DOS program written in MS Basic. The BEEM raw data were then analyzed mainly in MS Excel.
CHAPTER 4

Nanometer-resolution measurement and modeling of lateral variations of the effective work function at bi-layer Pt/Al/SiO₂ interface

4.1 Tunable Effective Work Function

Future complementary metal-oxide-semiconductor (CMOS) technology will require metal gates with an effective work function (EWF) that can be “tuned” to precisely adjust the transistor turn-on voltage. It was shown using macroscopic C-V measurements that the EWF could be adjusted using a metal bi-layer as the MOS gate electrode, by adjusting the thickness of a very thin low work function metal covered by a high work function metal film (or vice-versa) on a SiO₂ film [2,3]. For instance, Figure 4.1(a) (taken from I. S. Jeon et al. [3]) clearly shows that for Ti/Pt/SiO₂/Si MOS structure, the C-V curves shifts toward positive voltage as the bottom Pt layer thickness increases, which suggests that the EWF of bi-layer metal electrode was increased from that of Ti to that of Pt by increasing of the Pt layer thickness. Conversely the C-V curves shifts toward negative voltage as the bottom Ti layer thickness increases for Pt/Ti/SiO₂/Si
(in Figure 4.1(b)). A schematic view of MOS capacitor with bi-layer metal film is illustrated in Figure 4.2(a).

Figure 4.1 (a) The C-V curves of Ti/Pt/SiO$_2$/Si capacitors with different target range thickness of Pt as bottom metal A. (b) The C-V curves of Pt/Ti/SiO$_2$/Si system with different thickness of Ti as bottom metal A (taken from I. S. Jeon et al. [3]).

Figure 4.2: A schematic view of MOS capacitor with bi-layer metal film. Proposal (a): the bottom metal film is laterally homogeneous and covers the oxide completely. Proposal (b): the bottom metal film is laterally inhomogeneous with small “pinholes” in the bottom film filled in by the top film.
However, it was observed that the EWF could be adjusted over a very wide thickness range of the bottom metal film (about 3-10 nm in Figure 4.1 from Ref. [3]). This is surprising because one would naively expect that the effects of the top metal film would be effectively screened once the bottom metal film was more than a few monolayers thick (in Figure 4.2(a)). However, as discussed by Jeon et al. [3] this behavior would make more sense if the metal/SiO\textsubscript{2} interface were actually laterally inhomogeneous, with small “pinholes” in the bottom film filled in by the top film, as illustrated in Figure 4.2(b). The tunability would then come from the decrease in average pinhole coverage and diameter with increasing bottom metal thickness. If so, it may be possible to use the nm-resolution Ballistic Electron Emission Microscopy (BEEM) technique [38,39] to reveal this inhomogeneity.

4.2 Sample Preparation

Si(100) wafers (n-type with resistivity 0.004-0.02 Ω·cm) with 10nm of high quality commercial oxide were cut into 9×20mm pieces, de-greased using a sequence of ultrasonic trichloroethylene, acetone, and methanol, finally rinsed in de-ionized water. Samples were then immediately introduced into an ultrahigh vacuum (UHV) preparation chamber and attached UHV STM/BEEM system [42], and heated to a pyrometer reading of ~ 340°C for 10 min to desorb water and hydrocarbons. Then either a ~5 nm thick Pt or a 5nm Pt/1.4nm Al metal bi-layer film were deposited by electron beam evaporation through a shadow mask to form a number of 0.5 mm\textsuperscript{2} diameter dots. Samples were then transported \textit{in-situ} to the attached STM/BEEM chamber without any post-metallization
anneal. A 0.1 mm diameter Au wire positioned with a mechanical manipulator was used to contact particular metal dots for the BEEM measurements.

4.3 Results and Discussion

4.3.1 BEEM Measurements

Figure 4.3(a) shows example average BEEM $I_c-V_T$ curves for the 5nm Pt/SiO$_2$/Si (open squares) and 5nm Pt/1.4nm Al/SiO$_2$/Si (open circles) samples. Each curve represents an average of ~ 45 individual BEEM $I_c-V_T$ curves taken sequentially at different locations. The Bell-Kaiser model [39] was used to fit (solid lines) the experimental BEEM curve to determine the threshold voltage $V_{th}$ and in turn the energy barrier $\phi_{bar} = eV_{th}$, using a 0.5 V range of data centered self-consistently around the best-fit value of $V_{th}$. As can be seen in Figure 4.3(a), at $V_{gate} = 0$ V, $\phi_{bar}$ for the metal bi-layer sample is ~ 0.2eV lower than for the pure Pt/SiO$_2$ sample, which shows that by inserting a lower work function metal film the effective work function of the gate stack is indeed adjustable, in agreement with prior studies [2,3]. Note that effective work function is used instead of work function, since the band alignment at the metal/oxide interface can depend on other factors besides the metal work function such as material-dependent charge transfer at metal/oxide interface etc.

Figure 4.3(b) plots the measured barrier height $\phi_{bar}$ (as determined from BEEM $I_c-V_T$ curves such as shown in Figure 4.3 (a)) as a function of $V_{gate}$. One can see several important features in this data: (a) $\phi_{bar}$ is lower for the bi-layer sample (open circle) than
Figure 4.3: (a) Typical BEEM $I_c-V_T$ data for bi-layer Pt/Al/SiO$_2$ (open circle) and pure Pt/SiO$_2$ sample (open square) and Bell-Kaiser(BK) model fits (solid lines) and best-fit barrier heights (arrows) at $V_{gate} = 0$V. Each data is an average of ~ 45 individual $I_c-V_T$ curves measured at different locations. Top curve has been vertically offset for clarity. Tip current was 10 nA. (b) Best-fit barrier heights vs. $V_{gate}$ determined by BEEM for both pure Pt/SiO$_2$ (solid square) and bi-layer Pt/Al/SiO$_2$ (open circle).
the pure Pt sample (solid square) below \(\sim 0.5 \) V, but becomes essentially the same at higher \( V_{\text{gate}} \). (b) Both curves have a transition “knee” to a larger slope close to \(\sim 0.5 \) V. (c) The transition is more abrupt for the pure Pt film than the bi-layer film. As discussed in section 3.2.4, for negative \( V_{\text{gate}} \) (which corresponds to forward electric field as in Figure 3.9(b)) BEEM probes the energy barrier at the metal/SiO\(_2\) interface, so any difference in the EWF between pure Pt and the Pt/Al bi-layer should be directly observable as a difference in the energy barrier \( \phi_{\text{bar}} \) measured by BEEM. The weak \( \phi_{\text{bar}} \) dependence on \( V_{\text{gate}} \) for both samples in this forward electric field case is consistent with the image-force lowering effect [1] expected at the metal/SiO\(_2\) interface. For large positive \( V_{\text{gate}} \) (which corresponds to reverse electric field as in Figure 3.9(c)), the maximum energy barrier location switches to the SiO\(_2\)/Si interface, with a subsequent strong direct dependence of the barrier height \( \phi_{\text{bar}} \) on \( V_{\text{gate}} \). In this case, the barrier height \( \phi_{\text{bar}} \) is mainly determined by the electron affinity difference between SiO\(_2\) and Si, the doping of the Si, and the value of \( V_{\text{gate}} \), but is only weakly dependent on the metal EWF. Consequently, \( \phi_{\text{bar}} \) for both the pure Pt and bi-layer samples should become nearly the same at large positive \( V_{\text{gate}} \), as observed in Figure 4.3(b). The transition knee close to \( \sim 0.5V \) for both samples corresponds to the value of \( V_{\text{gate}} \) at which the average electric field in oxide \( E_{\text{ox}} \) is zero. We note that zero \( E_{\text{ox}} \) typically does not occur at zero \( V_{\text{gate}} \) due to the contact potential difference between the metal and the semiconductor substrate.

We next consider whether BEEM is able to directly observe increased spatial inhomogeneity at the metal bi-layer/SiO\(_2\) interface as compared to the pure Pt/SiO\(_2\) interface. Typical BEEM images at \( V_{\text{gate}} = -1V \) (which corresponds to the forward electric
Figure 4.4: STM topography of Pt/SiO$_2$ (a) and Pt/Al/SiO$_2$ (c) and corresponding BEEM images ((b) and (d)) with $V_{\text{gate}} = -1$V. Tip current was 10 nA. The STM topography and BEEM image are taken simultaneously.

field case for both samples) and $I_T = 10$ nA on the 5nm Pt/SiO$_2$/Si and 5nm Pt/1.4nm Al/SiO$_2$/Si samples are shown in Figure 4.4. The forward electric field condition is critical for BEEM to directly observe any spatial inhomogeneity in the energy barrier at

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metal/oxide interface since BEEM probes the energy barrier at front metal/oxide interface only for forward electric field. The tip voltages in Figure 4.4(b) and (d) were chosen to be slightly above the respective threshold voltages for the two samples at $V_{\text{gate}} = -1\text{V}$ in order to reduce the amount of charge injected into the SiO$_2$ film and so reduce possible effects of trapped charge on the BEEM images [42]. In Figure 4.4 both the STM topography ((a) and (c)) and BEEM images ((b) and (d)) of pure Pt and metal bi-layer samples look very similar. The BEEM images of both samples show inhomogeneous patches of larger and smaller BEEM current. Such variations in the local BEEM current could result from local variations in $\phi_{\text{bar}}$, but could also result from local variations in electron transmittance through the metal film (due to variations in metal thickness or the crystal orientation of grains in the polycrystalline metal film) or across the metal/oxide interface.

In order to determine whether the bi-layer sample has larger variations in local barrier height than the pure Pt same, we analyzed about 45 individual BEEM $I_c-V_T$ curves measured at different locations across each of the two samples. We found that the standard deviation (SD) of $\phi_{\text{bar}}$ was about the same for both the pure Pt/SiO$_2$ (SD $\approx$ 85 meV) and the metal bi-layer/SiO$_2$ (SD $\approx$ 95 meV) samples. This indicates that either the two samples have roughly the same degree of inhomogeneity in local barrier height, or that the spatial resolution of BEEM is not sufficient to directly resolve large local variations in barrier height, or that the measurement uncertainty for a single BEEM $I_c-V_T$ curve is larger than the local variations in barrier height. We estimate the BEEM spatial resolution for these samples to be $\approx$ 8 - 10 nm, based on previous BEEM studies [48,56].
of 4 nm-thick, 5 nm-thick, and 8 nm-thick Pt films deposited on 4H-SiC samples with embedded stacking faults that behaved as quantum wells of very narrow width (0.5 nm – 1.25 nm), where the SBH height over the stacking fault was much smaller than over the surrounding Pt/SiC. In those studies, the averaged full-width at half-maximum of BEEM profiles over the stacking faults was found to range from ~8 nm for the 4 nm-thick Pt film to ~10 nm for the 8 nm-thick Pt film, most likely due to lateral spreading of the injected hot electrons in the Pt film before entering the semiconductor [57]. So if the metal bi-layer sample has very small (< ~10 nm) local patches with significantly-varying barrier height, they may not be directly visible in BEEM images or by measurement of local BEEM $I_c-V_T$ curves. We note that if inhomogeneity in the bi-layer film is caused by pinholes in the 1.4 nm thick bottom Al film, the expected length scale would be comparable to the average grain size of the Al film, which should have as an upper limit the 5 – 10 nm grain size of the complete bi-layer film determined from Figure 4.4(c). However, very small patches of varying local barrier height should still produce observable effects in the spatially-averaged barrier height, as discussed below.

4.3.2 Modeling the Dependence of the Spatially-averaged Barrier Height

$\phi_{\text{bar}}$ on $V_{\text{gate}}$

We next examine whether we can theoretically fit the experimental measurements of the spatially-averaged barrier height $\phi_{\text{bar}}$ vs $V_{\text{gate}}$ for pure Pt and metal bi-layer samples that are shown in Figure 4.3(b). Assuming a uniform interface and no trapped charge in the oxide, the dependence of the energy barrier $\phi_{\text{bar}}$ (including image force
Figure 4.5: BEEM energy barrier $\phi_{\text{bar}}$ dependence on $V_{\text{gate}}$ data (symbols) and model fits (solid lines) by assuming uniform interface for both pure Pt/SiO$_2$ (a) and bi-layer Pt/Al/SiO$_2$ (b). In (b), there is a small curvature of BEEM data around flat band voltage that can’t be fitted by assuming uniform interface.
lowering effects) on $V_{\text{gate}}$ can be calculated based on [1] the Si electron affinity $\chi_{\text{Si}}$, the Si doping $N_d$, the SiO$_2$ electron affinity $\chi_{\text{SiO}_2}$, the SiO$_2$ layer thickness $t_{\text{oxide}}$, the SiO$_2$ high-frequency dielectric constant $\varepsilon_{\text{high}}$, and the work function of metal. The Solid lines in Figure 4.5(a) and (b) are the theoretical calculated results of $\phi_{\text{bar}}$ vs $V_{\text{gate}}$ for pure Pt and metal bi-layer samples respectively. Known parameters used in the calculation are $\chi_{\text{Si}} = 4.05$ eV, $N_d = 5 \times 10^{18}/\text{cm}^3$, $\chi_{\text{SiO}_2} = 0.89$ eV, $t_{\text{oxide}} = 10$ nm and $\varepsilon_{\text{high}} = 2.15$. The effective work function $W$ of the metal used in the calculation is adjustable to fit the experimental data of $\phi_{\text{bar}}$ vs $V_{\text{gate}}$ for both samples. Figure 4.5(a) shows that the theoretical calculation fits the experimental data of pure Pt sample very well with the best fit of $W_{\text{Pt}} = 5.1$ eV, which in turn suggests that the pure Pt sample interface is uniform and does not have significant oxide trapped charge (see below). However, the best fit (with $W_{\text{Pt/Al}} = 4.8$ eV) is much worse for the metal bi-layer sample as shown in Figure 4.5(b). In particular, the metal bi-layer sample has a much more gradual change of $\phi_{\text{bar}}$ vs $V_{\text{gate}}$ close to the knee at $\sim 0.5$ V than the pure Pt sample.

We next consider two possible origins of the gradual change of $\phi_{\text{bar}}$ vs $V_{\text{gate}}$ at $V_{\text{gate}} \approx 0.5$ V for the bi-layer sample: (1) It may come from a large trapped charge density in the SiO$_2$, which was previously shown to produce significant “rounding” of $\phi_{\text{bar}}$ vs $V_{\text{gate}}$ curves [44]. (2) It may be due to an inhomogeneous EWF at the metal/oxide interface. For the first possible origin, by assuming a uniform EWF at the metal/oxide interface but with trapped charge in the oxide, we can indeed fit the experimental data of $\phi_{\text{bar}}$ vs $V_{\text{gate}}$ of bi-layer sample pretty well by assuming $W_{\text{Pt/Al}} = 4.7$ eV and a (large)
Figure 4.6: BEEM energy barrier $\phi_{\text{bar}}$ dependence on $V_{\text{gate}}$ data (open circle) and model fit (solid line) of bi-layer Pt/Al/SiO$_2$ by assuming uniform interface with a large uniform trapped charge in the SiO$_2$.

Figure 4.7: The $C-V$ curves of pure Pt/SiO$_2$ (black line) and bi-layer Pt/Al/SiO$_2$ (pink line) capacitors.
uniform trapped charge density in the SiO$_2$ of $n_{\text{bulk}} = -3.6 \times 10^{18}$ cm$^{-3}$ (which corresponds to $-3.6 \times 10^{12}$ cm$^{-2}$ projected areal charge density for a 10 nm thick SiO$_2$) as shown in Figure 4.6. The same known parameters of $X_{\text{Si}}$, $N_d$, $X_{\text{SiO}_2}$, $t_{\text{oxide}}$ and $\varepsilon_{\text{high}}$ are used in the calculation as listed above. However, such a large trapped charge density would also result in $\sim +1$V flat band voltage shift in $C-V$ measurements (estimated from Eq. 2.37) of the bi-layer sample as compared to the pure Pt sample. While as in Figure 4.7, the $C-V$ curve of the bi-layer sample shifts $\sim 0.4$V toward negative (rather than positive) gate voltage compared to the pure Pt sample, which is (possibly) due to the $\sim 0.4$eV lower EFW of the bi-layer sample than the pure Pt sample (as from Eq. 2.19). We conclude that the more gradual change of the $\phi_{\text{bar}}$ vs $V_{\text{gate}}$ behavior of the bi-layer sample is unlikely to be simply due to a large trapped charge density in the oxide.

Tung [58,59] considered the expected electrical behavior of metal/semiconductor contacts with spatially inhomogeneous barrier height $\phi_{\text{bar}}(x,y)$ where the lateral length scale of the inhomogeneity is comparable to or smaller than the depletion width of the semiconductor. He showed that the electrostatic potential below low barrier height regions could experience a “potential pinch-off” effect produced by surrounding high barrier height regions that would strongly increase the local barrier height. For the metal-SiO$_2$-Si structures considered here, such potential pinch-off effects should become strong when the size of low barrier patches is less than the thickness of the SiO$_2$ film (10 nm in our case), as illustrated in Figure 4.8. The circular patches in Figure 4.8(a) represent low $\phi_{\text{bar}}(x,y)$ regions at the metal-oxide interface (produced by low EWF Pt/Al alloy regions) that are surrounded by high $\phi_{\text{bar}}(x,y)$ regions (produced by high EWF pure Pt regions).
Figure 4.8: (a) The assumed inhomogeneous geometry at the bi-layer Pt/Al/SiO$_2$ interface. 50% Pt/Al alloy circular patches with 4nm diameter are uniformly distributed and surrounded by pure Pt patches at the metal/oxide interface. (b) The demonstration of the Tung-effect. The potential under a uniform high EWF patch (upper dashed line) will be pulled down (upper solid line) and the potential under a uniform low EWF patch (lower dashed line) will be pulled up (lower solid line) by considering the inhomogeneous geometry as shown in (a).
The upper dashed line and lower dashed line Figure 4.8(b) are the calculated vertical potential profiles for a uniform interface (with no trapped oxide charge), using the known parameters listed above and assuming an EWF of 5.1 eV and 4.7 eV respectively. As expected, the metal-oxide barrier heights (determined by the maximum in the potential profile) for these two cases differ by \(~0.4\) eV, which is the difference of the assumed EWFs of the high- and low-barrier regions. For comparison, the upper and lower solid lines in Figure 4.8(b) show calculated potential profiles along two different paths normal to an inhomogeneous interface, consisting of a 50% coverage of 4 nm diameter circular patches of a low (4.7 eV) EWF metal surrounded by a high (5.1 eV) EWF metal, determined by finite element electrostatic simulations done with the commercial software package Flex PDE [60] (image force lowering was added after calculation) (see Appendix A.1 for a sample modeling program). For the finite element electrostatic simulations, Dirichlet boundary conditions were assumed at the metal/SiO₂ and SiO₂/Si interfaces with the values of the electron potential energy given by \(W_{\text{metal}} - \chi_{\text{SiO}2}\) and by \((\chi_{\text{Si}} - \chi_{\text{SiO}2}) + qV_{\text{gate}}\) respectively. Heavy n-doping of the Si is assumed. Periodic boundary conditions were assumed parallel to the interface. The lower and upper solid lines in Figure 4.8(b) show potential profiles along a path through the center of a low EWF patch and midway between the patches, respectively. We see from these two curves that the local barrier height (the maximum along the potential profile) through a low-EWF region is pulled up by the surrounding high-EWF regions, (as compared to a uniform low-EWF interface) while that barrier through a high-EWF region is pulled
down by the nearby low-EWF regions. The barrier height through other locations on this surface should fall between these two extreme values.

In order to compare these simulations of an inhomogeneous interface with the measured BEEM data shown in Figure 4.5, we used the following procedure. For a given value of $V_{\text{gate}}$, the maximum and minimum barrier heights were determined as described above, and then for each barrier an expected BEEM $I_c-V_T$ curve was simulated (using the Bell-Kaiser model [39]), and the two simulated BEEM $I_c-V_T$ curves were averaged together, and then were fit using the Bell-Kaiser model to determine an “average” barrier height for that value of $V_{\text{gate}}$. This procedure was then repeated for other values of $V_{\text{gate}}$, producing the simulated $\phi_{\text{bar}}$ vs $V_{\text{gate}}$ curve shown in Figure 4.9. We see that this simulated curve for an inhomogeneous interface fits the measured data for the bi-layer sample much better than does a model that assumes a uniform interface (shown in Figure 4.5(b)). We note that since lateral potential variations produced by the inhomogeneous metal/SiO$_2$ interface could deflect electrons preferentially towards the low-barrier regions located below the low effective work function patches, we also considered the extreme case where 100% of the BEEM electrons could find the low-barrier regions. As shown in Figure 4.10, this resulted in almost the same simulated $\phi_{\text{bar}}$ vs $V_{\text{gate}}$ curve (dashed line) compared to the simulated $\phi_{\text{bar}}$ vs $V_{\text{gate}}$ curve (solid line) shown in Figure 4.9, which assumes “50%-low and 50%-high”. Since threshold values in BEEM $I_c-V_T$ curve fits are mostly determined by the lowest threshold present, it is to be expected that fits to the “50%-low and 50%-high” and the “100%-low” simulated curves should produce similar threshold values. We note that other combinations of small patch size (<10 nm), coverage,
Figure 4.9: BEEM energy barrier $\phi_{\text{bar}}$ dependence on $V_{\text{gate}}$ data (open circle) and finite element simulation fit (solid line) of bi-layer Pt/Al/SiO$_2$ by assuming inhomogeneous metal/oxide interface with certain geometry as shown in Figure 4.8 (a).

Figure 4.10: BEEM energy barrier $\phi_{\text{bar}}$ dependence on $V_{\text{gate}}$ data (open circle) and finite element simulation fits for “50% electrons can find low-EFW regions, 50% find high-EFW” case (solid line) and for “100% electrons can find low-EFW regions” (dashed line) of bi-layer Pt/Al/SiO$_2$ by assuming inhomogeneous metal/oxide interface with certain geometry as shown in Figure 4.8 (a).
and assumed values for the low- and high-EWF regions can also produce good fits to the bi-layer data, but a model that assumes a uniform interface cannot. Furthermore, our simulations indicate that a model with larger patch size produces progressively worse fits as the patch size is increased above ~10 nm (the SiO$_2$ film thickness), because the “potential pinch-off” effects of the bi-layer sample become progressively weaker. For patch size larger than 20nm, the simulation essentially produces a “parallel conduction model” with little potential pinch-off effect. As in Figure 4.11, the best fit (dashed line) in this case (with EWF of 4.75 eV and 5.10 eV for the two regions and 50% coverage for the low EWF patches) is very close to the solid line fit in Figure 4.5(b) for a uniform

![Figure 4.11: BEEM energy barrier $\phi_{bar}$ dependence on $V_{gate}$ data (open circle) and model fits by assuming a uniform interface with EFW of 4.8eV (solid line) and a “parallel conduction band” model with EFW of 4.75 eV and 5.10 eV for the two regions and 50% coverage for the low EWF patches (dashed line) for bi-layer Pt/Al/SiO$_2$.](image)
interface (also shown in Figure 4.11 for comparison), which assumed a uniform EWF of 4.8 eV. Again this is because the low-EWF patches essentially determine the threshold voltage of the simulated BEEM $I_c-V_T$ curves, and exhibit almost the same $\phi_{bar}$ vs $V_{gate}$ behavior as a uniform interface. The simulations can only reproduce the more gradual $\phi_{bar}$ vs $V_{gate}$ behavior measured for the bi-layer sample if a smaller (<~10 nm) patch size is assumed.

### 4.4 Conclusions

In summary, a comparison of BEEM measurements made on a pure Pt/SiO$_2$/Si and bi-layer Pt/Al/SiO$_2$/Si sample reveal a qualitatively different dependence of the measured barrier height on gate voltage, suggesting that the metal/oxide interface of bi-layer Pt/Al/SiO$_2$/Si sample is laterally inhomogeneous at the nm scale. This proposal is supported by finite element electrostatic simulations, which show that a model with a uniform interface can adequately describe the data for the pure-Pt sample, but that a model interface with small (<10 nm) “patches” of different EWF is necessary to describe the data for the bi-layer sample. We could not directly see these small patches in BEEM images, most likely because they are smaller than the estimated ~10 nm BEEM spatial resolution for these samples. This study suggests that the large reported “tunability” of the EWF of metal bi-layer samples [2,3] is due to an inhomogeneous metal/SiO$_2$ interface, with the top metal filling in “pinholes” in the bottom metal film.
CHAPTER 5

BEEM and Int-PE study on metal/high-\textit{k} oxide/Si

5.1 Introduction

The continued scaling of Si-based metal-oxide-semiconductor electronics raises interest in replacing SiO\textsubscript{2} with a “high-\textit{k}” (higher dielectric constant) material [4]. A thicker high-\textit{k} film could have the same capacitance as a (thinner) SiO\textsubscript{2} film but with reduced direct tunnel current, provided the energy barriers for electron and hole tunneling remain sufficiently large. This makes it critical to understand the band structure of potential high-\textit{k} materials, and in particular the conduction and valence band offsets to Si. Recently, photoconductivity (PC) and internal photoemission (Int-PE) measurements have been used to investigate the band gaps and band offsets to Si of a number of possible high-\textit{k} amorphous metal oxide films [5-11] (including amorphous HfO\textsubscript{2}, Sc\textsubscript{2}O\textsubscript{3}, LaAlO\textsubscript{3}, GdScO\textsubscript{3}, DyScO\textsubscript{3}, LaScO\textsubscript{3}, Lu\textsubscript{2}O\textsubscript{3}, and La\textsubscript{2}Hf\textsubscript{2}O\textsubscript{7}). Surprisingly, most of these amorphous films were found to have nearly the same band gap (~5.6 - 5.8 eV), conduction band (CB) offset (~2.0 – 2.1 eV), and valence band (VB) offset (~2.4 – 2.6 eV), as shown in Figure 5.1. Furthermore, many of these films were also reported to have a secondary conduction band (sometimes referred to as a “tail state” band) extending ~1
eV below the assumed primary CB, with possible physical origin attributed to disorder in the amorphous oxide film [5,8], or the different symmetries or $d$-state coupling in complex oxides with mixed metal cations [9].

So in order to answer whether the “tail state” band is due to disorder in amorphous oxide film, a 20 nm-thick crystalline Sc$_2$O$_3$ film and Lu$_2$O$_3$ film grown epitaxially at 700 °C on a Si(111) substrate were studied by Int-PE here. Furthermore, since BEEM can measure electrons injected even against an applied electric field for a thin oxide film as discussed in section 3.2.2, by combining both BEEM and Int-PE it could possibly tell whether the “tail state” band consists of extended or localized states.

![Figure 5.1: Typical band alignment of amorphous high-k oxide/Si (data taken from References [5-11]). The pink dashed line shows the “tail state” band of the amorphous oxide, which is ~1 eV below the assumed primary CB (red solid line).](image)
5.2 Conduction band energies and hot-electron transport characteristics in epitaxial Sc$_2$O$_3$/Si (111) studied by BEEM and Int-PE

The work in this section was done in collaboration with L. F. Edge and D. G. Schlom of the Materials Science and Engineering Dept. of Pennsylvania State University.

In this section, we will show measurements using ballistic electron emission microscopy (BEEM) [38-44] in combination with Int-PE and PC to investigate band alignment and carrier transport in a 20 nm-thick crystalline Sc$_2$O$_3$ films grown epitaxially at 700 °C on a Si(111) substrate, using both Pt and Al metal contacts. Int-PE measurements from the Si-side of the epi-Sc$_2$O$_3$ film show a ~1.9 eV Sc$_2$O$_3$/Si CB offset, similar to the recently reported [10] ~2.0 eV CB offset for amorphous Sc$_2$O$_3$, and also a lower CB extending ~0.9 eV below the main CB, similar to reports for amorphous Sc$_2$O$_3$ [10] and a variety of other amorphous oxide films [9,10]. This indicates that these tail states are not simply due to disorder in the amorphous films. PC measurements of the epi-Sc$_2$O$_3$ film also show the same ~6.0 eV band gap as seen on crystallized Sc$_2$O$_3$ [61,62]. Both BEEM and Int-PE from the metal side show strong electron transport through the lower CB. Most significantly the BEEM data clearly shows that this lower CB supports elastic transport across the 20 nm-thick epi-Sc$_2$O$_3$ even against an applied electric field, and so is a robust CB consisting of extended rather than localized states.

5.2.1 Sample Preparation

The 20-nm-thick epitaxial Sc$_2$O$_3$ film was grown at 700°C on a $p^+$ (0.02 – 0.06 Ω·cm) boron-doped Si(111) substrate by reactive molecular-beam epitaxy (MBE) by our collaborators at Penn State University [63] at a background pressure of molecular oxygen.
of $2 \times 10^{-6}$ Torr, which is 100 times greater than that needed to fully oxidize the incident scandium metal flux at room temperature. Before growth, the bare Si(111) substrate was heated in ultra-high vacuum (UHV) to 950°C to desorb the native oxide and provide a 7×7 reconstructed Si(111) surface for the growth of Sc$_2$O$_3$ at $T_{\text{sub}} = 700°C$. Four-circle x-ray diffraction (done by our collaborators at Penn State University) indicated that the Sc$_2$O$_3$ film was epitaxial with (111) Sc$_2$O$_3$ // (111) Si and mixed $A$-type and $B$-type alignment to the underlying Si(111) [64], i.e., the epitaxial films contain two twin variants related by a 180° in-plane rotation. The full width at half maximum of the rocking curve of the 222 Sc$_2$O$_3$ reflection was 0.064°.

After exposure to air and shipment to Ohio State the Sc$_2$O$_3$/Si samples were degreased using a sequence of ultrasonic trichloroethylene, acetone, and methanol, then rinsed in de-ionized water and coated with AZ5214E photoresist. Photolithography was used to open a number of 45μm square “windows” as well as a large clear region on one side of the sample. After a 30 min bake at 170 °C and a brief UV-ozone clean (to removed photoresist residue over the open regions) samples were immediately introduced into a UHV preparation chamber, and heated to a pyrometer reading of ~250 - 340°C for 10 min to desorb water and hydrocarbons. ~5 nm thick Pt or Al films were then deposited by electron beam evaporation through a shadow mask to form a number of 0.5 mm diameter “dots.” Samples were then transported in situ to an adjacent UHV for BEEM and Int-PE measurements. Metal dots over the 45μm windows were used for the BEEM measurements (to reduce the metal/Sc$_2$O$_3$ contact area and hence leakage current), while metal dots over the large open area were used for Int-PE (to maximize the signal).
The BEEM measurements were done with a custom-built UHV STM/BEEM system [42], modified with a fiber-optic feedthrough to permit in situ Int-PE up to ~6 eV photon energy [54]. Monochromatic photons were provided by a xenon lamp and a ¼ meter monochromator. An adjustable Au wire was used to contact particular metal dots for the BEEM and Int-PE measurements.

5.2.2 Int-PE Measurement of electrons injected from Si side (reverse $E_{ox}$) and PC measurement

A typical Int-PE spectrum for the Pt/epi-Sc$_2$O$_3$/Si samples at $V_{gate} = 1.5$ V is shown in Figure 5.2. We note that for large positive gate voltage (which we will call “reverse $E_{ox}$”), electrons injected from Si side dominate as discussed in section 3.1. The Int-PE signal clearly shows abrupt increase in slope at two different photon energies, which would suggest two different conduction bands in the oxide. The Int-PE spectrum was fit in the conventional way [7] using a linear fit of a selected 0.2 eV range of above-threshold electron quantum yield $Y$ data raised to the 1/3 power for electrons injected from Si side [7] (see Figure 5.2) and extrapolating to zero yield. In case of multiple thresholds (e.g., Figure 5.2), current with a lower threshold was first subtracted [10]. We estimate a statistical uncertainty of ~30 meV for the extracted Int-PE barrier heights (BHs), and a systematic uncertainty of ~80 meV. Systematic errors were estimated by varying the fitting range (while maintaining a good fit) to determine the effect on the best-fit threshold energy. A lower threshold energy of ~2.1 eV and a higher threshold of ~3.0 eV were obtained using the fitting procedure described above to fit the Int-PE spectrum in Figure 5.2. On our epitaxial samples these threshold energies were found to
Figure 5.2: Typical Int-PE yield $Y^{1/3}$ data (open symbol) and linear fit (solid line) versus photon energy extrapolated to zero yield to determine barrier heights at the oxide-Si.

Figure 5.3: Int-PE yield $Y^{1/2}$ data (open symbol) and linear fit (solid line) versus photon energy extrapolated to zero yield to determine the oxide band gap.
be almost the same when (lower work function) Al contacts were used instead of Pt, indicating that they are indeed due to electron injection at the Sc$_2$O$_3$/Si interface. As discussed in Ch. 3, if the Int-PE current were due to hole injection from the metal side, then the threshold energies should be very sensitive to the work function of the metal film.

Figure 5.3 shows the photoconductivity (PC) measurement of the Pt/epi-Sc$_2$O$_3$/Si at $V_{\text{gate}} = 0\text{V}$ (see Chapter 3 for a discussion of the difference between Int-PE and PC). The abrupt PC signal increase around 6 eV indicates that the injected photons start to excite electrons from Sc$_2$O$_3$ valence band to its conduction band to form electron-hole pairs, which will be separated by the oxide electric field and then contribute to the PC current. Using the same fitting procedure described above for Int-PE except that using above-threshold electron quantum yield $Y$ data raised to the 1/2 power rather than 1/3 law (see Ch. 3), one can get ~6.0 eV threshold energy which corresponds to the band gap of the epi-Sc$_2$O$_3$. Note that the band gap of epi-Sc$_2$O$_3$ measured by PC did not change when we varied the gate bias. However, the PC current value and direction did change with gate biases.

Figure 5.4 shows the band alignment at the epi-Sc$_2$O$_3$/Si interface based on the Int-PE measurement for electrons injected from Si side and PC measurement. For the determination of the Sc$_2$O$_3$/Si band alignment from the Int-PE data, we assumed that electrons were excited from the Si VB so that the measured 2.1 eV threshold means a band exists at $(2.1\text{ eV} – 1.12\text{ eV}) = 1.0\text{ eV}$, and the measured 3 eV threshold means (by the same procedure) that another CB exists at 1.9 eV above the Si CB. The ~6.0 eV
band gap of epi-Sc$_2$O$_3$ measured by PC is consistent with the report for annealed (crystallized) Sc$_2$O$_3$ [63,64]. Most importantly we still see the low-energy “tail state” CB even though the sample is crystalline (epitaxial), which suggests that the “tail state” CB is not simply due to disorder in the amorphous oxide film.

Figure 5.4: Schematic of the band alignment at the epi-Sc$_2$O$_3$/Si interface based on the Int-PE measurement for electrons injected from Si side and PC measurement.

5.2.3 Measurements of Electrons injected from the Pt side by BEEM and Int-PE

Example BEEM and Int-PE (electrons injected form metal side) spectra for the Pt/epi-Sc$_2$O$_3$/Si samples are shown in Figure 5.5. The sign of the measured Int-PE current
from the Si substrate switched from negative for $V_{gate} < -1V$ (where electrons injected from metal side dominate) to positive for $V_{gate} > -1V$ (where electrons injected from the metal side dominate). The voltage at which this cross-over occurs indicates that the electric field in the oxide $E_{ox} \approx 0$ at $V_{gate} \approx 1V$. The BEEM current measured with negative tip voltage (i.e., electrons injected into the metal) was found to be negative for all $V_{gate}$. No BEEM current was observed for positive tip voltage (injected holes). The $V_{th}$ for each BEEM spectrum was determined by fitting the Bell-Kaiser model [39] for a 0.5 V range of data self-consistently centered around the best-fit value of $V_{th}$, as shown in Figure 5.5(a). The Int-PE spectrum for electrons injected from metal side (Fig. 5.5(b)) were fit using the same procedure discussed above for electrons injected from Si side except that the electron quantum yield $Y$ data raised to the $\frac{1}{2}$ power was used rather than $Y^{1/3}$ (see Chapter 3). The statistical and systematic fitting uncertainty of the Int-PE data with a large positive gate bias (which we call “reverse $E_{ox}$”, where the electric field in the oxide film pushes electrons towards the metal side) still holds for Int-PE data with a small gate bias (“forward $E_{ox}$”, where the electric field in the oxide film pushes electrons towards the Si side). We also estimate a statistical uncertainty of $\sim 30$ meV for the extracted BEEM BHs, and a systematic uncertainty of $\sim 40$ meV, which was again estimated by varying the fitting range (while maintaining a good fit) to determine the effect on the best-fit threshold energy. We note that one can easily see in Fig. 5.5(a) that the measured BEEM BHs change substantially with the change of $V_{gate}$ from 0 V to 1 V.
Figure 5.5: (a) Typical BEEM $I_c-V_T$ data (circles) and Bell-Kaiser (BK) model fits (solid lines) and best-fit barrier heights (arrows) for two different values of $V_{gate}$. Each data curve is an average of 45-49 individual $I_c-V_T$ curves measured at different locations. Curves have been vertically offset for clarity. The tip current was 10-15 nA. (b) Int-PE yield $Y^{1/2}$ data (open symbols) and linear fit (solid line) versus photon energy extrapolated to zero yield to determine barrier height at the metal-oxide interface.
5.2.4 Modeling the dependence of the barrier height $\Phi_{bar}$ on $V_{gate}$

The BHs for the samples with Pt gate electrodes measured by BEEM and Int-PE are summarized in Figure 5.6(a). As discussed in section 5.2.2, two distinct thresholds were observed in the Int-PE spectra for $V_{gate} > 1$ V (reverse $E_{ox}$) at nearly the same energies as previously reported for amorphous Sc$_2$O$_3$ [10]. These were identified [10] as electron injection from the Si substrate into the regular Sc$_2$O$_3$ CB (upper threshold) at $\sim$3.0 eV above the Si valence band (VB), and a lower CB at $\sim$2.1 eV above the Si VB.

For $V_{gate} < 1$ V (forward $E_{ox}$) Figure 5.6(a) shows that the BHs measured by BEEM and Int-PE both had nearly the same energy (with systematic $\sim$80 meV offset) and nearly the same weak dependence on $V_{gate}$. These BHs were also found to be substantially reduced when Al was used instead of Pt, indicating that both BEEM and Int-PE measured the same electron energy barrier at the metal/Sc$_2$O$_3$ interface. The weak dependence on $V_{gate}$ is consistent with the “image-force lowering” effect [1] expected at the metal/Sc$_2$O$_3$ interface, and the small offset is probably due to differences in the fitting models and energy ranges used for the BEEM and Int-PE data. We note that the in situ pre-metallization sample outgassing $\geq \sim$250 °C (as discussed earlier) was necessary to observe electron injection from the metal side, using either BEEM or Int-PE, suggesting that adsorbates at the metal/Sc$_2$O$_3$ interface can prevent electron injection from the metal.

For $V_{gate} \geq 1$ V, Figure 5.6(a) shows that the BHs measured by BEEM have a sharp transition to a much stronger dependence on $V_{gate}$, with an approximate slope given by $dE_{bar}/d(eV_{gate}) \approx 1$. This behavior has been observed in prior BEEM measurements of metal/SiO$_2$/Si structures [40, 44] (see Fig. 3.10 in Section 3.2.4). With the transition from
Figure 5.6: (a) Best-fit barrier heights vs. $V_{\text{gate}}$ determined by BEEM (solid diamonds) and Int-PE (solid triangles and open symbols). Vertical dashed line separates conditions with forward and reverse $E_{\text{ox}}$. Under reverse $E_{\text{ox}}$, Int-PE measures two distinct barriers at the oxide Si interface. (b) BEEM data (symbols) and model fits assuming zero oxide charge (dashed line) and $n_{\text{bulk}} = 2.2 \times 10^{12}/\text{cm}^2$ (solid line).
forward $E_{ox}$ to reverse $E_{ox}$, the high point in the CB profile abruptly switches from the (front) metal/oxide interface to the (back) oxide/Si interface, with a subsequent strong direct dependence of the BH on $V_{gate}$ (see Fig. 3.9). One immediate conclusion is that at least some of the hot electrons injected into the Sc$_2$O$_3$ CB from the metal must have a long inelastic mean free path, since they can transport across the 20 nm–thick Sc$_2$O$_3$ film 	extit{even against an electric field}. We return to this point below.

Since BEEM can measure the BH continuously from forward $E_{ox}$ to reverse $E_{ox}$, we should be able to determine which of the two CBs measured by Int-PE at the Si interface (with reverse $E_{ox}$) corresponds to the CB measured by Int-PE and BEEM at the metal interface (with forward $E_{ox}$). Figure 5.6(b) compares the BEEM data to model fits, which calculate how the barrier (i.e., the high-energy point in the Sc$_2$O$_3$ CB profile) varies with $V_{gate}$. Known parameters are the Si electron affinity $\chi_{Si} = 4.05$ eV, the Si doping ($\sim 1 \times 10^{18}$/cm$^3$, $p$-type), and the Sc$_2$O$_3$ high-frequency dielectric constant $\varepsilon_{high} = 3.57$, which is necessary to calculate image force lowering at the metal interface [1]. The adjustable parameters in the fits are the metal work function ($W_{Pt}$), electron affinity of Sc$_2$O$_3$ ($\chi_{ox}$), and possible negative bulk charge density in the oxide Sc$_2$O$_3$ ($n_{bulk}$). The dashed line in Figure 5.6(b) shows the fit assuming $n_{bulk} = 0$, with best fit values $W_{Pt} = 5.88$ eV and $\chi_{ox} = 2.79$ eV, while the solid line shows the fit with $n_{bulk}$ as a free parameter, with $W_{Pt} = 5.97$ eV and $\chi_{ox} = 2.91$ eV, and $n_{bulk} = 2.2 \times 10^{12}$ cm$^{-2}$ [projected areal electron density]. The solid line in Figure 5.7 shows the corresponding calculated CB profile (with $n_{bulk} = 2.2 \times 10^{12}$ cm$^{-2}$) at a ~1.5 V gate bias.
Figure 5.7: Solid line is the energy band diagram of Pt/Sc$_2$O$_3$/Si for $V_{\text{gate}} = +1.5$ V determined from the solid-line model fit to the BEEM data in Figure 5.6(b). The dashed lines show the energies of the two CB minima at the oxide/Si interface determined by Int-PE with reverse $E_{\text{ox}}$. At the oxide/Si interface, the CB determined by BEEM best matches the lower of the two CBs determined by Int-PE. The curvature of the conduction band of Sc$_2$O$_3$ is caused by the fixed charge in the oxide.

For comparison, the two dashed lines in Figure 5.7 represent the upper and lower CBs as determined by Int-PE from the Si side (as shown in Figure 5.4). We see that the CB measured by BEEM and Int-PE from the metal side most closely lines up with the lower CB measured by Int-PE from the Si side. This indicates that the lower band extends all the way through the 20 nm thick Sc$_2$O$_3$ film, and is not localized only at the Sc$_2$O$_3$/Si interface. Furthermore, Figure 5.6 shows that BEEM is able to inject hot electrons completely across the Sc$_2$O$_3$ film up to $V_{\text{gate}} = +1.5$ V, where the electrons must move against an electric field in the Sc$_2$O$_3$ film. This indicates that the inelastic mean free path
in this CB must be a sizeable fraction of the 20 nm film thickness. Consequently, electron conduction in this CB cannot consist only of thermally-activated electron hopping as one might expect of a band of localized “tail-states.” So this lower CB consists of extended rather than localized states.

5.2.5 Laterally inhomogeneous BEEM images of Pt/epi-Sc$_2$O$_3$/Si

Figure 5.8 shows the STM topography and BEEM images of Pt/epi-Sc$_2$O$_3$/Si at $V_{\text{gate}} = -1$V (which corresponds to forward $E_{\text{ox}}$) and at $V_{\text{gate}} = 1.5$V (reverse $E_{\text{ox}}$). For both gate voltages, the tip voltage was chosen to be ~1 V higher tip voltages than the corresponding BEEM $I_e-V_T$ threshold voltages, so that substantial BEEM current could be measured in the BEEM images. The tunneling current was chosen slightly higher at $V_{\text{gate}} = 1.5$V (15 nA) than at $V_{\text{gate}} = -1$V (10nA) to enhance the signal at $V_{\text{gate}} = 1.5$V, since there is always much smaller BEEM signal at reverse oxide electric field than at forward oxide electric field. In Figure 5.8(b) and (d) the BEEM images at both gate voltages show laterally inhomogeneous patches of larger and smaller BEEM current, which suggests those extended states are laterally inhomogeneous. Previous transmission electron microscopy (TEM) study of similar epi-Sc$_2$O$_3$ films by Klenov et al. have seen extended defects across those Sc$_2$O$_3$ films [63], which might suggest those laterally inhomogeneous extended states observed in BEEM images could possibly be related to extended defects that thread/cross the Sc$_2$O$_3$ films.

In summary, BEEM and Int-PE measurements on 20 nm-thick epitaxial Sc$_2$O$_3$/Si (111) films show the existence of a lower conduction band extending ~1 eV below the main CB, as have been reported for a variety of amorphous oxide films [9,10], indicating
that these states are not simply due to disorder in the amorphous films. This lower CB supports \textit{ballistic} hot-electron transport across the epi-Sc$_2$O$_3$ even against an applied electric field, indicating that it consists of \textit{extended} rather than localized states.

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{figure5.8}
\caption{STM topography of Pt/epi-Sc$_2$O$_3$ at $V_{\text{gate}} = -1$V (a) and $V_{\text{gate}} = 1.5$V (c) and corresponding BEEM images ((b) and (d)). $\sim 1$V higher tip voltages than the corresponding BEEM $I_c$-$V_T$ threshold voltages were chosen at both gate voltages. The STM topography and BEEM images were taken simultaneously.}
\end{figure}
5.3 Oxide charge and band alignment in Pt/epi-Lu$_2$O$_3$/Si (111) studied by BEEM, Int-PE/photoconductivity and $C-V$ measurements

The work in this section was done in collaboration with Carolina Adamo, Wei Tian, and Darrell G. Schlom of the Materials Science and Engineering Dept. of Pennsylvania State University.

A 20 nm-thick crystalline Lu$_2$O$_3$ films grown epitaxially at 700 °C on a Si(111) substrate were studied by BEEM, Int-PE/PC and $C-V$ measurements. Int-PE measurements from the Si-side of the epi-Lu$_2$O$_3$ film show a ~2.0 eV Lu$_2$O$_3$/Si CB offset, and also a lower CB extending ~1.0 eV below the main CB, similar to recently reported for amorphous Lu$_2$O$_3$ [11] and a variety of other amorphous oxide films [9,10], and our previous study on epi-Sc$_2$O$_3$ (see section 5.2 above) This again indicates that these tail states are not simply due to disorder in the amorphous films. However, BEEM measurements on Pt/epi-Lu$_2$O$_3$/Si found ~0.3-0.4 eV higher energy barrier at the metal/oxide interface than found by Int-PE. In contrast, in the above study of Pt/epi-Sc$_2$O$_3$/Si, BEEM and Int-PE found nearly the same barrier height. One possible explanation for the higher barrier height (BH) found by BEEM on Pt/epi-Lu$_2$O$_3$/Si might be that significant transient charge trapping occurred in this Lu$_2$O$_3$ sample at high injected electron flux density, while it did not occur for Sc$_2$O$_3$. Later in this section we present PC and $C-V$ data, where we will see that there is a substantial difference between the oxide- and Si- “flat band” voltages (measured by PC and $C-V$ respectively), which indicates a large positive charge in the oxide. And most of those charge could be removed by a ~350°C post-metallization vacuum anneal. Most surprisingly, Int-PE measurements
of Pt/epi-Lu$_2$O$_3$/Si (111) indicates the CB measured from the metal-side lines up between the “tail states” and “primary” CB measured from the Si side, in contrast with our finding on Pt/epi-Sc$_2$O$_3$/Si (111) that the metal-side CB aligned with the “tail states” CB.

5.3.1 Sample preparation

The 20-nm-thick epitaxial Lu$_2$O$_3$ film was grown by reactive MBE [65] (done by our collaborators at Penn State University) on a $p^+$ (0.02 – 0.06 $\Omega \cdot$ cm) boron-doped Si(111) substrate held at 700°C using an elemental Lu source in a partial oxygen pressure of $2 \times 10^{-6}$ Torr. Before growth, the bare Si(111) substrate was heated in ultra-high vacuum (UHV) to 950°C to desorb the native oxide and provide a 7×7 reconstructed Si(111) surface for the growth of Lu$_2$O$_3$ at $T_{\text{sub}} = 700$°C.

After exposure to air and shipment to Ohio State the Lu$_2$O$_3$/Si samples were degreased using a sequence of ultrasonic trichloroethylene, acetone, and methanol, then rinsed in de-ionized water. Samples were then immediately introduced into a UHV preparation chamber, and heated to a pyrometer reading of $\sim$ 340°C for 10 min to desorb water and hydrocarbons. A $\sim$5 nm thick Pt film was then deposited by electron beam evaporation through a shadow mask to form a number of 0.5 mm diameter “dots.” Samples were then transported in situ to an adjacent UHV for BEEM and Int-PE measurements.

5.3.2 Oxide charge and possible charge trapping in epi-Lu$_2$O$_3$/Si

The barrier heights (BHs) for Pt/epi-Lu$_2$O$_3$/Si measured by BEEM and Int-PE (with electrons injected from metal side at forward $E_{\text{ox}}$) are summarized in Figure 5.9.
Surprisingly, BEEM measurements on Pt/epi-Lu$_2$O$_3$/Si found a ~0.3-0.4 eV higher energy barrier at the metal/oxide interface than found by Int-PE (while in the Pt/epi-Sc$_2$O$_3$/Si study, the BEEM and Int-PE BHs agreed with each other very well). Since BEEM and Int-PE measurements of dielectric films are based on similar physics in that they induce “hot” carriers with known energy distribution in a metal or semiconductor close to the dielectric film, and measure internal energy barrier heights by determining the minimum “threshold” carrier energy required to enter and conduct across the dielectric CB, one would expect to get the same measured BHs for both techniques. However, those two techniques do have one big difference between them: the local \textit{flux} of injected “hot” electrons flux density by BEEM in the immediate vicinity of the tip is six orders of magnitude larger than that by Int-PE. While the total injected \textit{current} (typically in the 1-100 pA range) is similar in the two techniques, in BEEM it is all concentrated within ~10-20 nm of the tip, while in Int-PE is spread uniformly over a large area sample (~500 \(\mu\)m in diameter). So if we suppose there exist electron traps in the Lu$_2$O$_3$ film, the \textit{local} density of trapped electrons would be much larger for BEEM than for Int-PE. It is known that a high density of trapped electrons will increase the local BH [42], and so this could cause a higher measured BH for BEEM than Int-PE.

Therefore, in the following we will focus on the Int-PE data since it is less likely to be affected by electron trapping.

We next examine whether there is fixed charge in the Lu$_2$O$_3$ produced during the growth or processing of the film. Figure 5.10 shows the schematic of Pt/Lu$_2$O$_3$/Si band bending at zero average electric field in the oxide, assuming no oxide charge (a) and with
Figure 5.9: Best-fit barrier heights vs. $V_{\text{gate}}$ determined by BEEM (blue diamonds) and Int-PE (pink triangles).

negative oxide charge (b). At zero average $E_{\text{ox}}$, if free carriers are excited in the oxide with photon illumination during a PC experiment, there should be the same number of carriers flowing in both directions so the net PC signal is almost zero. So by determining the gate voltage $V_{\text{gate}}$ at which the PC current changes its sign, one can determine the so-called oxide-“flat band” voltage, which is the voltage that must be applied across the sample so the average $E_{\text{ox}} = 0$ in the oxide film. We shall refer to this oxide flat-band voltage as $V_{\text{FB-oxide}}$. We note that C-$V$ measurements can also be used to determine the flat band voltage in the Si film (as discussed in section 2.2.2), which we will call it $V_{\text{FB-Si}}$.

Hence, if one can determine both $V_{\text{FB-oxide}}$ and $V_{\text{FB-Si}}$ and finds that they are equal, then this indicates that there is no oxide charge. This is illustrated in Figure 5.10(a) which
Figure 5.10: Schematic of Pt/Lu$_2$O$_3$/Si band bending at zero average electric field in the oxide, assuming no oxide charge (a) and with negative oxide charge (b).
shows that if there is no oxide charge, there can be zero average electric field across the oxide and zero electric field in the Si film at the same time. However, $V_{FB-\text{oxide}}$ will be different from $V_{FB-\text{Si}}$ if there is net trapped charge in the oxide film as illustrated in Figure 5.10(b). We made both PC and C-V measurements on our Pt/Lu$_2$O$_3$/Si samples, which indicated that the $V_{FB-\text{oxide}} = \sim (+0.5)$ V, while the $V_{FB-\text{Si}} = \sim (-0.8)$ V, which suggests that there is a large amount of charge in the oxide. By annealing the sample at $\sim 350^\circ$C in UHV for half an hour, the $V_{FB-\text{oxide}}$ becomes $\sim 0$ V and the $V_{FB-\text{Si}}$ turns to $\sim (-0.2)$ V, which suggests that most of those oxide charge could be removed by a $\sim 350^\circ$C post-metallization vacuum anneal.

As discussed in section 5.2.4, by modeling the dependence of the barrier height $\Phi_{\text{bar}}$ on $V_{\text{gate}}$ one could possibly obtain information about fixed charge in the oxide. Figure 5.11 shows the Int-PE data (at forward $E_{\text{ox}}$) before UHV annealing (a) and after annealing (b), and corresponding model fits, which calculate how the barrier (i.e., the high-energy point in the Lu$_2$O$_3$ CB profile) varies with $V_{\text{gate}}$. The same known parameters are used as discussed in section 5.2.4. The adjustable parameters in the fit are the metal work function ($W_{\text{Pt}}$), electron affinity of Lu$_2$O$_3$ ($\chi_{\text{ox}}$), and possible positive bulk charge density in the Lu$_2$O$_3$ ($n_{\text{bulk}}$), but $W_{\text{Pt}}$ and $\chi_{\text{ox}}$ are forced to be the same in both fits (assuming $W_{\text{Pt}}$ and $\chi_{\text{ox}}$ do not change after $\sim 350^\circ$C UHV anneal). The solid lines in Figure 5.11 show the fits, with best fit values $W_{\text{Pt}} = 5.2$ eV, $\chi_{\text{ox}} = 2.6$ eV, and $n_{\text{bulk}} = 4 \times 10^{12}$ cm$^{-2}$ for Int-PE data before annealing and $n_{\text{bulk}} = 1 \times 10^{12}$ cm$^{-2}$ after annealing. This again indicates
that there is a large amount of charge in the oxide, and most of those charge could be removed by a \(~350^\circ\text{C}\) post-metallization vacuum anneal.

\begin{figure}
\centering
\includegraphics[width=\textwidth]{figure5_11.png}
\caption{Int-PE data (symbols) and model fits (solid lines) before (a) and after UHV anneal (b). All Int-PE data measured at forward $E_{\text{ox}}$. Note that the larger increase of BH with $V_{\text{gate}}$ around 0.5V (in (a)) (close to zero averaged, but still at forward $E_{\text{ox}}$) results from that the maximum BH is switched from the metal/oxide interface (at small $V_{\text{gate}}$) to some place located inside the oxide film (close to zero $E_{\text{ox}}$), which would have a larger BH dependence on $V_{\text{gate}}$ than that only due to image-force lowering effect.}
\end{figure}
5.3.3 Energy band diagram of Pt/epi-Lu$_2$O$_3$/Si

An Int-PE spectrum for the Pt/epi-Lu$_2$O$_3$/Si sample at $V_{\text{gate}} = 1.5$ V (reverse $E_{\text{ox}}$) is shown in Figure 5.12. The Int-PE signal (open circles) again clearly shows abrupt increase at two different photon energies, which would suggest two different conduction bands in the Lu$_2$O$_3$. A lower threshold energy of $\sim 2.0$ eV and a higher threshold of $\sim 3.0$ eV were extrapolated from the fits (solid lines) in Figure 5.12 using the same fitting procedure discussed in section 5.2.2. Since these Lu$_2$O$_3$ films are epitaxial (crystalline), this again indicates that these tail states are not simply due to disorder in the amorphous films.

![Figure 5.12: Int-PE yield $Y^{1/3}$ data (open circle) and linear fit (solid lines) versus photon energy extrapolated to zero yield to determine barrier heights at the epi-Lu$_2$O$_3$/Si interface.](image)

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Figure 5.13: The pink solid line is the CB of Lu$_2$O$_3$ for $V_{gate} = +1.5$ V determined from the model fit to the Int-PE data at forward $E_{ox}$ in Figure 5.11(a). The dashed lines show the energies of the two CB minima at the oxide/Si interface determined by Int-PE with reverse $E_{ox}$. The CB measured by Int-PE from the metal-side lines up between the “tail states” and “primary” CB measured from the Si side. The curvature of the conduction band of Lu$_2$O$_3$ is caused by the fixed charge in the oxide.

The upper and lower CBs as determined by Int-PE from the Si side were shown as two dashed lines in Figure 5.13. For comparison, the calculated conduction band profile (with $n_{bulk} = 4 \times 10^{12}$ cm$^{-2}$) at a $\sim 1.5$ V gate bias was also shown as a pink solid line in Figure 5.13 based on the model fit of the dependence of the Int-PE BHs on $V_{gate}$ in Figure 5.11(a) (measured from the metal side). Surprisingly, the CB measured by Int-PE from the metal-side lines up between the “tail states” and “primary” CB measured from the Si side.
side for Pt/epi-Lu$_2$O$_3$/Si (111), in contrast with our finding on Pt/epi-Sc$_2$O$_3$/Si (111) that the metal-side CB aligned with the “tail states” CB. We suspect this might be due to two layers of different composition in Lu$_2$O$_3$ (for example, there is one type of Lu$_2$O$_3$ at the metal/oxide interface, while another type of Lu$_2$O$_3$ at the oxide/Si interface). Further experiments need to be done to resolve this puzzle.

5.4 Conclusions

In summary, Int-PE measurements on 20 nm-thick epitaxial Sc$_2$O$_3$/Si (111) and epitaxial Lu$_2$O$_3$/Si (111) films show the existence of a lower conduction band extending ~1 eV below the main CB, as have been reported for a variety of amorphous oxide films [9-11], indicating that these states are not simply due to disorder in the amorphous films. BEEM and Int-PE measurements on Pt/epi-Sc$_2$O$_3$/Si show that the CB measured from the metal-side lines up with the “tail states” CB measured from the Si side. Most importantly BEEM measurements show this lower CB supports \textit{ballistic} hot-electron transport across the epi-Sc$_2$O$_3$ even against an applied electric field, indicating that it consists of \textit{extended} rather than localized states. However, for Pt/epi-Lu$_2$O$_3$/Si the CB measured from the metal-side lines up between the “tail states” and “primary” CB measured from the Si side, which was suspected to be due to two layers of different composition in Lu$_2$O$_3$. Int-PE/PC and \textit{C-V} measurements on Pt/epi-Lu$_2$O$_3$/Si indicate that there is a large amount of positive charge in the oxide, most of which could be removed by a ~350$^\circ$C post-metallization vacuum anneal. BEEM measurements on Pt/epi-Lu$_2$O$_3$/Si found ~0.3-0.4 eV higher energy barrier at metal/oxide interface than found by Int-PE (while BEEM and
Int-PE agree with each other well in Pt/epi-Sc₂O₃/Si study), which might suggest significant transient charge trapping in this Lu₂O₃ sample at high injected electron flux density.
CHAPTER 6

Nanometer-scale BEEM studies on “end-on” metal contacts to vertical Si nanowires

The work in this chapter was done in collaboration with Eric R. Hemesath and Lincoln J. Lauhon of the Materials Science and Engineering Dept. of Northwestern University.

6.1 Introduction

In recent years, there have been great interests in semiconducting nanowire (NW) and nanotube (NT) devices for potential future applications and for fundamental studies of low-dimensional systems. It is critical to understand carrier transport through contacts to these devices, in particular how transport is affected by the small size [14,15] and restricted geometry [16] inherent to such structures. For example, Leonard & Tersoff [14] argued that ultra-narrow “end-on” metal contacts made to the end of a narrow NT or NW in a vertical geometry should have intrinsically weaker Fermi-level pinning than wider contacts.
Figure 6.1: Illustration of simple physics of weaker Fermi-level pinning of ultra-narrow “end-on” metal contacts made to the end of a narrow nanotube (NT) or nanowire (NW) than wider contacts. (a) metal contact on regular bulk semiconductor. (b) metal contact on a NT or NW.
A simple physics picture about the small size contact effect is illustrated in Figure 6.1. Figure 6.1(a) assumes a large planar metal/semiconductor (M/S) interface. For many metal contacts to a large bulk semiconductor, interface states near the M/S interface form and can develop a sheet of charge several angstroms away from the interface [1] (see Chapter 2 for more background). If this interface charge is positive as assumed in Fig. 6.1), it would pull the semiconductor electron potential energy down and this shift in electron potential energy persists deep into the semiconductor. In contrast, the situation is quite different for a small-area contact. For example, Fig. 6.1 (b) shows a small “end-on” contact to a semiconductor (NW). In this case we can treat the interface states charge as a small interface charge disk. A simple calculation shows that the small interface charge disk would pull the potential energy down within the interface dipole layer, but the potential would then recover quickly to its initial value over a length scale comparable to the diameter of the NW. As discussed in section 2.2, Fermi-level pinning is due to interface states charge formed at the metal/semiconductor interface, which would cause a potential energy drop or increase at the interface so as to change the Schottky barrier height (SBH) of a M/S contact. Since the interface states charge of a small contact has much less ability to modify the semiconductor electron potential energy than a wider contact, a weaker Fermi-level pinning would then be expected for a small size contact.

Figure 6.3 (taken from Leonard & Tersoff [14]) illustrates the weakened Fermi-level pinning effect for a hypothetical end-on contact to a 1.4nm diameter carbon nanotube (schematic of the structure for simulation is shown in Figure 6.2). The solid (dotted) line corresponds to strong (zero) pinning due to interface states. In this case,
Figure 6.2: Schematic of end-on metal contacts to vertical NT or NW.

![Diagram](image)

Figure 6.3 (taken from Reference [14]): Calculated CB profiles in 1.4 nm diameter carbon NT near end-on contact to a high WF (a) and low WF (b) metal. Insets show corresponding profiles in bulk contacts. $D_0$ represents the interface states density.
bending of the conduction band (CB) due to these interface states occurs only with \( \sim 2 \) nm of the interface (as seen on the left side of Figure 6.3(a) and 6.3(b)) which is comparable to the diameter of the nanotube. While for a bulk contact (insets) with an infinitely wide interface dipole layer, this shift in CB energy persists to infinite depth. But since the dipole layer for an end-on NT or NW contact is limited in lateral size, the CB in a NT or NW recovers to its unpinned value at a depth roughly equal to 2 times the diameter of the NT or NW. Figure 6.4 shows our example finite element electrostatic simulation results of a Si NW CB profile (measured down through the center of a NW, as the dashed arrow indicated in Figure 6.2) for end-on Au/Si NW contact with different NW diameters (detailed simulation description will be introduced later in this chapter). Again, one can easily see that the NW CB energy was pulled down by the interface states charge. But it could gradually recover close to its initial value for a small size NW (for example, for a 10nm in diameter NW), while not for a 100nm in diameter (or even bigger) NW. This weakened Fermi-level pinning effect could cause \( \sim 70 \) meV SBH increase for a Au/Si NW contact if we decrease the NW diameter from 100 nm to 10 nm, which could possibly be revealed by our nm-spatial and meV energy resolution BEEM technique [38,39,47,49].

Here, we report measurements using BEEM [38,39,42] to study individual “end-on” Schottky metal contacts to \( \sim 100 \) nm in diameter vertical Si NWs (intrinsic) grown epitaxially on a n-Si (111) substrate by chemical vapor deposition (CVD) [66]. These measurements differ from prior NW/NT studies in several important ways, in particular that they can directly measure the local SBH, use hot electrons as opposed to near-Fermi
Figure 6.4: Finite element electrostatic simulation of NW CB profiles near end-on Au/Si NW contact with different NW diameters. NW length is assumed to be 500 nm.

energy carriers, and use small-area end-on contacts as opposed to longer side contacts used in most prior studies of NW/NT transport. While the diameter of these NWs is not small enough to directly reveal the weakened Fermi-level pinning discussed above, we did observe several other nm-scale effects that are related to the small size of the NW. In particular, our BEEM $I_c-V_T$ measurements show (1) that a strong suppression of electron injection occurs at higher hot-electron flux (produced either by increasing the tip voltage $V_T$ or the tip-metal tunnel current $I_T$), as compared to regular Au/n-type bulk Si reference samples, and (2) that the local SBH at the edge of two separate NWs is ~20 meV lower than that at the NW center. These results will be discussed in detail in the following sections.
6.2 Sample Preparation

The procedure for making “end-on” NW contact samples is adapted from procedures developed by others to make vertical NW field effect transistors (FETs) [13,67-73], and is sketched in Figure 6.5. First, vertical intrinsic Si NWs were epitaxially grown on a n-Si (111) substrate using the vapor-liquid-solid (VLS) chemical vapor deposition (CVD) process by our collaborators at Northwestern University [66]. Figure 6.6(a) is a scanning electron microscopy (SEM) image of one sample (grown in this case using Au catalyst colloid particles of nominal 80 nm diameter) and shows that some of these NWs are indeed vertical, but that there are “angled” NWs grown as well. The diameter of the NWs was found to vary from 80 to 150 nm with most NWs about 100 nm in diameter. Then Futurrex IC1-200 spin-on glass (SOG) made from a Polysiloxane resin was spin coated on the Si NW sample (as illustrated in Fig. 6.5(b)), and then was annealed at 100°C and 200°C for 1 min, respectively. This process was repeated 1 or 2 more times resulting in a SOG film with total thickness of ~ 450 to 550 nm, so that only the ends of the vertical NWs will be exposed, and not the strongly “angled” NWs. The sample was then annealed for 30 min at 850°C in air to densify the SOG and make it more like SiO₂. If this high-temperature annealing were not used, the etch rate of the SOG in buffered hydrofluoric acid (BHF) would be too fast to control the last processing step right before Au deposition (Figure 6.5(d)). We note that if the total SOG film thickness is more than ~600 nm then it will form cracks during the 850°C annealing step. There were also “craters” surrounding the Si NWs which were believed to be due to the
Figure 6.5: Schematic of the fabrication process to make “end-on” NW metal contacts. (a) Vertical NW growth. (b) Dielectric fill. (c) CMP planarization. (d) Deposition of thin metal film contact.

Figure 6.6: SEM images of (a) as grown vertical Si NWs by CVD and (b) vertical Si NWs embedded in spin-on glass after dielectric fill and then after CMP polish (inset). The perspective of those SEM images is 52°, 45° and 0°, respectively.
Figure 6.7: AFM image of the sample surface after CMP polish. The RMS roughness of the sample surface is ~0.5 nm for a 5 μm × 5 μm scan. Color scale: 5nm.

850°C anneal after spin coating (due to the spin-on glass pulling away from the Si NWs during the high temperature annealing). After that annealing step, a chemical mechanically polish (CMP) of the Si NWs embedded in the SOG was done to make the sample surface smooth (Fig. 6.5(c)). We estimate that ~50 nm of the SOG was removed together with the protruding NWs end. The inset of Figure 6.6(b) shows an SEM image of one Si NW after the CMP polish. The RMS roughness of the sample surface was ~0.5 nm after CMP planarization, as measured by atomic force microscopy (AFM) with a 5 μm × 5 μm scan (as shown in Figure 6.7). We see from Figs. 6.6 and 6.7 that only a few vertical NWs (with an areal density of ~0.25 NW/μm²) survived this dielectric fill/anneal/CMP process. Finally a brief BHF etch (1:10 BHF, further diluted 10 times with deionized water) was used to remove the native SiO₂ at the NW ends, after which
the samples were immediately introduced into either an ultrahigh vacuum (UHV) preparation chamber or a thermal evaporation chamber for metal deposition. Then a ~15 nm thick Au film or a ~8 nm thick Pt film was then deposited (Fig. 6.5(d)) either by electron beam evaporation or thermal evaporation through shadow masks to form a number of 0.5 mm or 0.4 mm metal contact diameter “dots”.

The samples were then transported into a custom build UHV scanning tunneling microscopy (STM)/BEEM system [42] or a BEEM-modified UHV Omicron VT STM system [50], as described in Chapter 3. A 0.1 mm diameter Au wire positioned with a mechanical manipulator was used to contact particular metal dots for the BEEM measurements.

6.3 Characterization of hot-electron trapping in vertical Si nanowires

6.3.1 Basic Measurements

Figure 6.8 demonstrates that BEEM can locate the Si NW ends under the metal film. Figures 6.8(a), 6.8(c), and 6.8(e) show 800 × 530 nm STM topographic images of a 15 nm thick Au film deposited over vertical Si NWs denoted as #13NW_5, 13NW_22, and #13NW_30, respectively, (each embedded in spin-on glass), while Figs 6.8(b), 6.8(d), and 6.8(f) show the simultaneously-measured BEEM images (recall from section 3.2.2 that “BEEM images” are plots of the collector current $I_c$ vs tip position), measured with tip voltage $V_T = 1.3\text{V}$ and tunnel current $I_T = 10\text{nA}$. Regarding the labeling scheme for the NW samples, we note that “#13NW_5” represents the 5th individual NW found in the sample #13. In Fig. 6.8, the images of #13NW_5 and #13NW_22 were taken at 80K, 121
Figure 6.8: STM images ((a), (c) and (e)) of a 15 nm thick Au film over three different vertical Si NWs embedded in spin-on glass and simultaneous taken BEEM images ((b), (d) and (f)) at the same area. The bright spots in the BEEM images correspond to the Si NWs, which are correlated with the circular protruding features (which is due to surface preparation) in the STM topography. The STM and BEEM images of #13NW_5 and #13NW_22 are taken at 80 K, while images of #13NW_30 are taken at 200 K. Color scale: 8 nm for (a), 6 nm for (c) and (e), 0–20 pA for (b) and (f) and 0–3 pA for (d). All data taken with $V_T = 1.3$ V and $I_T = 10$ nA.
while images of #13NW_30 were taken at 200K. The subsurface Si NWs are clearly visible in Figures 6.8(b), (d), and (f) as circular spots with non-zero BEEM current, since at $V_T = 1.3V$ injected hot electrons have energy high enough to overcome the local Au/Si NW SBH (which is ~0.79 eV for the NWs studied at room temperature) and then conduct across the NW and substrate to be collected as BEEM current, while hot electrons with this energy could not transport across the Au/spin-on glass interface (the Au/SiO$_2$ interface has ~3.5 eV barrier height [42]). We see that the bright circular spots in the BEEM images (corresponding to Si NWs) in Figs. 6.8(b), (d), and (f) are also strongly correlated with the circular protruding features (~6-10 nm higher than the surrounding surface) in the corresponding STM topographic images (Figure 6.8(a), (c), and (e)). We believe the NW ends protrude ~6-10 nm above the surrounding spin on glass due to the much faster BHF etch rate of the spin-on glass (~4-5 Å/s) than on the native SiO$_2$ (~1 Å/s) and on the Si NWs (with approximately zero etch rate). We also note that the STM topographic image of #13NW_5 (Fig. 6.8(a)) shows a “crater” surrounding the NW (probably due to the spin-on-glass pulling away from the NW during the 850 °C anneal), while #13NW_22 (Fig. 6.8(c)) and #13NW_30 (Fig. 6.8(e)) do not reveal a significant crater. We do not yet understand why craters form around some NWs and not others.

The diameter of these three NWs appears to be about 130 nm, 100 nm, and 140 nm, respectively, based on the STM images in Figures 6.8(a), (c), and (e), which are ~20 nm smaller than those estimated from the BEEM images. The apparent larger size of the BEEM images compared to the topography is believed to be due to the spreading of the hot electrons in the 15nm Au film (the BEEM spatial resolution of 15 nm thick Au
deposited on cleaved AlGaAs/GaAs/AlGaAs quantum wells (QWs) of different width (9, 12, and 15 nm) was reported to be ~22 nm [57]). So the estimated NW diameters (measured from BEEM and STM images) varied from 100 nm to 150 nm, which is consistent with the SEM measurements of the as grown Si NW sample. We also note that the BEEM signal of #13NW_22 (Fig. 6.8(d)) is ~7 times smaller than that of #13NW_5 (Fig. 6.8(b)) even though both image were measured at 80 K. Approximately 50 different Si NWs were studied at different temperatures. In general the BEEM current at a given temperature was found to vary dramatically for different NWs. And the BEEM current of most NWs was found to decrease strongly with lower temperature, which will be discussed later in detail.

Figure 6.9 shows example average BEEM $I_c-V_T$ curves from several Au/Si NWs measured at room temperature. Each curve is an average of ~100 individual $I_c-V_T$ curves measured at different locations of the same NW. An average BEEM $I_c-V_T$ curve measured on a regular large area Au/Si junction at room temperature is also shown in the inset for comparison. Compared to the BEEM $I_c-V_T$ curve from a regular Au/Si junction, the BEEM $I_c-V_T$ curves of Au/Si NWs show a strong suppression of hot-electron injection at higher tip voltages, which appears as a “roll off” of the BEEM $I_c-V_T$ curves at higher tip voltage. Approximately 15 different Si NWs on sample #10 were studied at room temperature, and most showed BEEM current suppression at higher tip voltages (as in Fig. 6), even though the magnitude of the BEEM current and the degree of suppression varied dramatically for different NWs. We note that NW sample #13 was fabricated from a new supply of spin-on glass, which was purchased when sample fabrication with
the old supply of spin-on glass became unreliable, probably due to aging of the liquid spin-on glass (the samples became less insulating and the CMP polishing rate changed over time). More than 30 different Si NWs from sample #13, were studied at different temperatures. We found that the degree of BEEM current suppression of the NWs from #13 was much weaker than NWs from sample #10 at room temperature, although most of them still showed very strong BEEM current suppression at lower temperatures (the temperature dependence will be discussed later in detail). We also note that sample #13 was found to have a smoother surface after CMP than sample #10, for reasons we do not yet understand.
We next consider two possible origins of the BEEM current suppression at higher tip voltages of the Si NWs. (1) It may be due to strongly energy dependent hot-electrons scattering in the NWs, in which case hot-electrons would be scattered back much more easily at higher energy than at lower energy and so would result in BEEM current suppression at higher tip voltage (as illustrated in Figure 6.10). (2) It may be due to a current-dependent steady-state charge build-up (SSCB) in those NWs, in which case more charge would build-up at higher tip voltage (simply because the BEEM current is larger at higher tip voltage), which in turn suppresses the collected BEEM current more strongly. As shown in Figure 6.11, for low injected current, there is almost no charge build-up and so no current suppression; for high injected current, there is charge build-up and the built-up charge would change the Si NW CB near the contact so that to suppress the collected BEEM current $I_c$. Since the BEEM current suppression would not depend on the tunnel current $I_T$ if the first origin is responsible, but would depend on $I_T$ (higher $I_T$ would result in more BEEM current $I_c$ at a particular tip voltage) if the second origin is responsible, we should be able to distinguish between these two mechanisms by measuring BEEM $I_c$-$V_T$ curves at different $I_T$, as discussed below.

6.3.2 Dependence of the BEEM current suppression in Si NWs on $I_T$

Figure 6.12 shows the dependence of the BEEM $I_c$-$V_T$ suppression on $I_T$ for an example NW (#10NW_10). At a certain high tip voltage, for example at 1.2V, the BEEM current $I_c$ of the NW is $\sim$5.5 pA at $I_T = 10$ nA (blue line), which is only two times of the $I_c \approx 2.8$ pA measured at $I_T = 1.3$ nA (green line). In contrast, for normal BEEM we would expect $I_c$ to scale approximately linearly with $I_T$, and so would expect $I_c$ to be $\sim$7 times
Figure 6.10: Illustration of one possible current suppression origin: suppression is due to strongly energy dependent hot-electrons scattering in the NWs.

Figure 6.11: Illustration of another possible current suppression origin: suppression is due to a steady-state charge build-up in the NWs.
Figure 6.12: Si NW BEEM $I_c$-$V_T$ curves (in color) for sample #10NW_10 measured at different $I_T$ at room temperature, compared to a BEEM $I_c$-$V_T$ curve measured on a regular Au/Si junction (black curve). Each data curve is an average of ~100 individual $I_c$-$V_T$ curves measured at different locations of the same NW. The inset shows the NW’s BEEM $I_c$-$V_T$ data at different $I_T$ scaled in amplitude and each shifted 30 mV towards higher tip voltage so their near-threshold behavior is the same as that for the regular Au/Si junction.

larger at $I_T = 10$ nA. This indicates that there is much more current suppression for higher injected current, even when the tip voltage is held fixed. In order to show the dependence of the NW BEEM current suppression on $I_T$ more clearly, the inset of Fig. 6.12 shows the NW BEEM $I_c$-$V_T$ data at different $I_T$ were scaled in amplitude and each shifted 30mV towards higher tip voltage so their near-threshold behavior is the same as that for a regular Au/Si junction. The scale factor for the BEEM current of the NW at 1.3 nA
(green line), 5 nA (pink line) and 10 nA (blue line) \( I_T \) is 6.8, 1.9, and 0.95, respectively. We see that at higher \( I_T \) the BEEM \( I_c-V_T \) curve of the NW deviates from that of the regular Au/n-Si junction at much lower tip voltage, indicating a much stronger BEEM current suppression. This strong dependence on \( I_T \) of the BEEM current suppression suggests that the current suppression is due to a steady-state charge build-up in the NW that increases as more current is injected into the NW.

Instead of the scaling procedure shown in the inset of Fig. 6.12, we note that we could also quantify the degree of suppressing of the NW BEEM \( I_c-V_T \) curves by scaling and shifting the \( I_c-V_T \) curve of the regular Au/n-Si junction so that it matches the NW \( I_c-V_T \) curve just above threshold, as shown in Fig. 6.13(a). In this case, the difference between the two curves measured at a certain tip voltage represents the “rejected current” \( I_{\text{rej}} \) for a particular value of the tunnel voltage \( V_T \) and tunnel current as illustrated in Fig. 6.13(a). We performed this procedure for the three NW BEEM \( I_c-V_T \) curves from Fig. 6.12 (which were measured at \( I_T = 1.3 \text{ nA}, 5 \text{ nA}, \text{ and } 10 \text{ nA}, \text{ respectively} \) and then plotted in Fig. 6.13(b) the resulting \( I_{\text{rej}} \) vs. \( I_c \) data for all three curves. We see from Fig. 6.13(b) that when plotted this way, the data from all three curves collapses to a single \( I_{\text{rej}} \) vs. \( I_c \) curve, indicating that the amount of “rejected” current only depends on \( I_c \), and not on the tip voltage \( V_T \). This further confirms that the BEEM current suppression in this NW depends only on the hot-electron current, but not on the tip voltage. This is consistent with a model in which the BEEM current suppression is due to a current-dependent, steady-state charge build-up in the NW.
Figure 6.13 (a) Illustration of the procedure of determining the dependence of the “rejected current” $I_{rej}$ of a NW on tip voltage $V_T$ and tunnel current $I_T$. The curves of the NW at different $I_T$ were still each shifted 30mV towards higher tip voltage. (b) The dependence of the Si NW rejected BEEM current $I_{rej}$ on the measured current $I_c$ for three BEEM $I_c$-$V_T$ curves measured at different $I_T$. 

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6.3.3 Temperature-dependent BEEM measurements

The BEEM $I_c-V_T$ curves shown in Figure 6.14(a) were all measured on #13NW_30 with a tunneling current $I_T = 10$ nA, but at different temperatures. We see strong current suppression, and that the BEEM current amplitude decreases strongly with temperature. The BEEM $I_c-V_T$ curves in Figure 6.14(b) were also all measured on NW30 at these same temperatures, but now all with a smaller $I_T = 1$ nA. In this case there is also a strong temperature dependence (but not as strong as at $I_T = 10$ nA), and also that the saturation behavior is weaker. All of this behavior can be explained by a (qualitative) model in which (a) for a given temperature, tip voltage, and tunnel current, there exists a steady-state charge accumulation in the NW which suppresses BEEM current, (b) this steady-state charge accumulation (and hence the suppression) is larger when more current is injected into the NW, and (c) the steady-state charge accumulation increases at lower temperature.

One way to quantify the degree of suppression at a particular temperature and tip voltage is the ratio of the measured BEEM current with $I_T = 10$ nA to that with $I_T = 1$ nA. For a regular Au/bulk n-Si reference sample (which has no BEEM current suppression), this ratio of $I_{c, 10nA}/I_{c, 1nA}$ is $\approx 10$. However for a Si NW with current suppression, the ratio of $I_{c, 10nA}/I_{c, 1nA}$ is much smaller than 10 as indicated in Figure 6.12. And the smaller this ratio is, the stronger the current suppression it represents. Figure 6.15 shows the ratio of $I_{c, 10nA}/I_{c, 1nA}$ for different NWs at different temperatures (all with a tip voltage of 1.3 V). We see that the degree of suppression is different for different NWs, but all show
stronger suppression at lower temperature, which suggests that there is more charge accumulated at lower temperatures.

**Figure 6.14:** BEEM $I_c$-$V_T$ curves of #13NW_30 for 10 nA (a) and 1 nA tunneling current (b) at different temperatures.
6.3.4 Direct observation of time-dependent current suppression due to changing steady-state charge build-up in Si NWs

We next examine whether BEEM is able to directly observe dynamic charge trapping and de-trapping in those Si NWs. Figure 6.16(a) shows BEEM $I_c-V_T$ curves of #13NW_5 (pink line) and #13NW_30 (blue line) scaled in amplitude and shifted 38 mV (for #13NW_5) and 10 mV (for #13NW_30) respectively towards lower tip voltage so their near-threshold behavior is the same as that for the regular Au/Si junction BEEM $I_c-V_T$ curve (black line). The scale factor for the BEEM current of the #13NW_5 (pink line) and #13NW_30 (blue line) is 2.4 and 0.82, respectively. All data were taken at $I_T = 10$ nA. It is clear that the BEEM $I_c-V_T$ curve of #13_NW5 has almost the same shape as the
Figure 6.16: (a) BEEM $I_c-V_T$ curves of #13NW_5 (pink line) and #13NW_30 (blue line) scaled in amplitude and shifted 38 mV (for #13NW_5) and 10 mV (for #13NW_30) respectively towards lower tip voltage so their near-threshold behavior is the same as that for the regular Au/Si junction BEEM $I_c-V_T$ curve (black line). BEEM $I_c$-t curves of #13NW_5 (b) and #13NW_30 (c). The STM tip was held at 1.3 V all the time. (1), (2) and (3) correspond to the time period with 1 nA, 10 nA and 1 nA tunneling current, respectively.
curve for the regular Au/Si junction (so #13NW_5 has almost no suppression even at 80K), while the curve of #13NW_30 at 200K shows a very strong current suppression. If the BEEM current suppression is in fact due to a current-dependent steady-state charge buildup (SSCB), then this SSCB would be larger in #13NW_30 at 200K than in #13NW_5 at 80K. One would then expect that it might be possible observe dynamic charge trapping and de-trapping in #13NW_30, while not in #13NW_5.

Figure 6.16(b) and (c) show the time-dependence of the BEEM current on #13NW_5 (at 80K) and #13NW_30 (at 200 K) respectively, when the tunnel current is abruptly increased from 1 nA to 10 nA and then decreased back to 1 nA. The STM tip was held at 1.3V all the time. In Figure 6.16(b), the BEEM current of #13NW_5 increases suddenly as the tunneling current increases from 1 nA to 10 nA (process (1) to (2)), and decreases suddenly as the tunneling current decreases from 10 nA to 1 nA (process (2) to (3)). No significant transient behavior is observed after the tunnel current is abruptly changed, consistent with the assumption that there is little current-dependent SSCB and hence little BEEM current suppression in #13NW_5 (as shown in Figure 6.16(a)). In contrast, the BEEM current of #13NW_30 (in Figure 6.16(c)) initially increases abruptly when the tunnel current is increased to 10 nA, then slowly decreases to a lower steady-state value during a 100-200 ms time period. This is consistent with a slow build-up of charge to a steady-state value that is larger for $I_T = 10$ nA than at 1 nA (more charge build-up would cause stronger current suppression, hence the slow decrease in the observed BEEM current after the tunnel current is abruptly increased). Then when $I_T$ is reduced back to 1 nA, the BEEM current initially drops to a very low value.
(consistent with a large charge build-up that occurred when $I_T$ was 10 nA), then slowly relaxes back up to a steady-state value of $\sim$5 pA, presumably due to a decrease in the steady-state charge build-up for this lower tunnel current of 1 nA. Similar time-dependent current suppression behavior at different temperatures (presumably due to changing steady-state charge build-up) was also observed in other Si NWs that exhibited strong BEEM current suppression in their BEEM $I_c-V_T$ curves. So indeed it is possible to directly observe dynamic charge trapping and de-trapping in Si NWs exhibiting strong BEEM current suppression, giving direct support to a model in which the BEEM current suppression is due to a temperature-dependent and current-dependent steady-state charge build up.

Figure 6.17 shows that the dynamic time-dependent change in suppression following an abrupt change in tunnel current can be approximately fit by an exponential function. The decay time obtained from the fit for the charge build-up and "build-down" process respectively for #13NW_30 at 200 K (Figure 6.17(a)) was found to be $\sim$ 65 ms and 40 ms respectively, while it was found to be $\sim$120 ms and $\sim$300 ms respectively for at 120 K (Figure 6.17(b)). So we see that the decay time does increase with lower temperature, but that the temperature dependence is rather weak ($\sim$ factor of 3 increase when the temperature is lowered from 200K to 120K). We think this dependence is too weak to be due to a simple Arrhenius behavior one would expect for independent traps (one would have to assume a very low activation energy ($\sim$36 meV) and an unphysically low attempt rate of $\sim$ 150/s). The reason of this weak dependence of decay time on temperature is still not clear.
6.3.5 Finite element electrostatic simulation of a possible mechanism responsible for BEEM current suppression

We next consider two possible mechanisms, which might be responsible for BEEM current suppression at higher tip voltages of the Si NWs. One possible mechanism is that the built-up charge in the NW causes a shift of quasi-Fermi level in the Si NW.
(which is assumed to be raised by $\Delta V$ relative to the metal Fermi level as the charge builds up), which according to the thermionic emission theory would result in an approximately exponential increase with $\Delta V$ of the current $I_{rej}$ that leaks back into the metal film, while only would result in an linear increase with $\Delta V$ of the collector current $I_c$. However if this mechanism is responsible for the BEEM current suppression, one would then expect that the rejected current $I_{rej}$ should respond as fast as the collector current $I_c$ to the abrupt change of the injected current. However from Fig. 6.16 (c), one can see that the collector current $I_c$ responds quickly to reach a high value and then decay slowly to a smaller value due to the slower increase (or response) of the rejected current $I_{rej}$, as the tunneling current was abruptly changed from 1nA to 10nA. So the observed different time scale of the response time between the rejected current $I_{rej}$ and the collector current $I_c$ to the abrupt change of injected current suggests that the above proposed mechanism for BEEM current suppression does not apply for our Si NWs.

Another possible mechanism by which built-up charge in the NW could suppress the BEEM current is illustrated in Fig. 6.11(b), namely that built-up charge close to the Au/NW contact produces an increase in the local Si NW conduction band energy, which in turn scatters some of the incident hot electrons back into the Au film. To evaluate the feasibility of this mechanism, finite element simulations were used to calculate conduction band bending close to the Au/NW interface assuming different amounts of trapped charge at the NW Si/SiO$_2$ interface. Figure 6.18 shows the calculated conduction band energy profiles along the center of the NW with and without trapped charge in the Si/SiO$_2$ NW interface. These simulations were done using the commercial software
Figure 6.18: (a) The assumed geometry for finite element electrostatic simulation: NW diameter = 100 nm, NW length = 500 nm, the surrounding oxide is 2 μm wide and the Si substrate is 5 μm thick. (b) The calculated Si conduction band minimum energy along the center of the NW with no electrons trapped (black line), 20 electrons trapped (pink line), 50 electrons trapped (blue line) and 100 electrons trapped (light blue line) at the first 100 nm length Si NW/SiO2 interface, respectively. Z = 0 corresponds to the metal/Si NW interface.
package Flex PDE [60] (image force lowering [1] was added after these calculations). One can easily see that the conduction band maximum of the Si NW increases dramatically even with as few as 50 -100 electrons trapped at the SiO$_2$/Si NW interface near the Au/Si NW opening, which in turn would strongly suppress the collected BEEM current. This indicates that trapped electrons at the SiO$_2$/Si NW interface near the Au/Si NW contact is a feasible mechanism by which built-up charge could suppresses the BEEM current.

The finite element simulation of the Au/Si NW is discussed in detail in the following. A 100 nm in diameter and 500nm in length NW surrounded by 2μm wide SiO$_2$ is assumed for the simulation as shown in Figure 6.18(a). Dirichlet boundary conditions were assumed at the metal/Si NW (or SiO$_2$) interface and the back side of Si substrate with the values of the electron potential energy given by $W_{Au} - \chi_{Si}$ and by $E_c - E_F$ respectively. The known parameters used in the calculation are the Si electron affinity $\chi_{Si} = 4.05$ eV, the dielectric constant of Si $\varepsilon_{Si} = 11.9$, and the dielectric constant of SiO$_2$ $\varepsilon_{SiO_2} = 3.9$. The doping of the intrinsic Si NW is assumed to be $N_d = 1 \times 10^{15}$/cm$^3$. These simulations include partial Fermi-level pinning of the Si conduction band at the Au/Si contact interface, as discussed in section 2.1.2. The parameters used for the Fermi-level pinning at the Au/Si NW interface are the interfacial layer thickness $d = 0.4$ nm, the metal/Si interface charge neutrality level $q\phi_0 = 0.33$ eV (above the Si valence band) [1], the dipole layer dielectric constant $\varepsilon_{dipole} = 11.9$, and the interface state density $D_{it} = 4.76 \times 10^{14}$ states/cm$^2$/eV. Note that a dielectric constant of $\varepsilon_{dipole} = 11.9$ and an interface state
density of $D_{it} = 4.76 \times 10^{14}$ states/eV/cm$^2$, instead of $\varepsilon_{dipole} = 1$ and $D_{it} = 4 \times 10^{13}$ states/eV/cm$^2$ (in [1]), are assumed for the Au/Si interfacial layer, even though they would result in the same pinning behavior for Au/Si contacts (see discussion in section 2.1.2). Since the Schottky barrier height of a regular Au/Si junction at room temperature was measured (by us) to be $\sim 0.80$ eV with $\sim 5 \times 10^{15}$/cm$^3$ n-type doping, a work function of $W_{Au} = 4.95$ eV needs to be assumed to get the same calculated barrier height from the finite element simulation for a Au/Si structure with the Fermi-level pinning parameters used above. So the work function of $W_{Au} = 4.95$ eV was chosen for the finite element simulation of the Au/Si NW contacts.

Another question is where and how the charge builds up? It could be piled up in the NW given the electric field in the NW is very weak? Or it could be trapped either in the bulk Si NW or at the SiO$_2$/Si NW interface (or both)? Our finite element simulation suggests that the electrons build up near the Au/Si NW opening will contribute most for the Si NW conduction band change. But the built-up charge could not stay there against a so strong internal electric field of Si NW (as shown in Figure 6.18(b)) unless they are trapped there. In fact it was extensively reported that there are surface and interface charge trapping states on the nanowire surface [67,74-77], which would cause hysteretic behavior of the threshold voltage in a NW field effect transistor (FET) device. Furthermore, by growing a very high quality layer of gate SiO$_2$ surrounding the vertical Si NW (thermal oxidizing $\sim 30$ nm of the as-grown vertical Si NW), Goldberger et al. [13] demonstrated almost no hysteretic behavior of the threshold voltage in their Si NW FETs, indicating much fewer electron traps at this NW Si/SiO$_2$ interface. Therefore, we suspect
that an improved procedure of making “end-on” NW metal contacts by introducing a very high quality layer of SiO₂ surrounding the vertical Si NWs before the dielectric fill might dramatically decrease the BEEM current suppression of the NWs. The Pelz group hopes to study this further in future experiments.

6.4 Direct measurements of lateral variations of Schottky barrier height across “end-on” metal contacts to vertical Si nanowires

The above sections showed that there was strong suppression for large BEEM current, but very little suppression for small BEEM current, as you would get just above threshold. So if BEEM is used to measure the SBH just above threshold, it should be measuring the “intrinsic” SBH. In the following section, we measured lateral variation in the intrinsic SBH, in particular comparing the SBH measured at the center with that measured at the edge.

Figure 6.19 shows the zoom-in STM topography and BEEM images of a 15nm Au film over two example NWs, which was shown in Figure 6.8(a), (b), (e) and (f) before. The STM and BEEM images of NW5 are taken at 80K, while images of NW30 are taken at 200K. The bright circular spots in the BEEM images of Figure 6.19(b) and (d) correspond to two Si NWs, which are correlated with the circular protruding features in the STM topography of Figure 6.19(a) and (c). The diameter of the two Si NWs in Figure 6.19(b) and (d) was estimated to be ~130-140 nm, as discussed in section 6.3.1.

After finding a Si NW, the STM tip was then brought onto that Si NW and a number of BEEM $I_c-V_T$ curves were taken at several particular locations of that NW. As
Figure 6.19. (a) and (c): STM images of a 15 nm Au film over two different vertical Si NWs embedded in spin-on glass. (b) and (d) simultaneous measured BEEM images over the same area. The STM and BEEM images of NW5 were taken at 80 K, while the corresponding images of NW30 were taken at 200 K. Color scale: 11 nm for (a), 7 nm for (c), and 0—20 pA for (b) and (d). All data measured with $V_T = 1.3$ V and $I_T = 10$ nA. Each circle or square mark in the images represents the location where 5 BEEM $I_c-V_T$ curves were measured in a particular STM/BEEM scan. ~ 30 (10) curves from 6 (2) different locations were averaged to get the SBH of the NW edge (center) for that scan.

shown in Figure 6.19, each circle or square mark represents 5 BEEM $I_c-V_T$ curves measured at that particular location in a particular STM/BEEM scan. ~ 30 (or 10) curves from 6 (or 2) different locations were averaged to get the averaged BEEM $I_c-V_T$ curves measured close to the edge (or center) of an end-on Au/Si-NW contact. Example
averaged BEEM $I_c-V_T$ data at NW5 center (circles) and edge (diamonds) are shown in Figure 6.20. The Bell-Kaiser model [39] was used to fit (solid lines) the experimental BEEM $I_c-V_T$ curve to determine the threshold voltage $V_{th}$ and in turn the SBH $\phi_{bar} = eV_{th}$, using a 0.3 V range of data centered self-consistently around the best-fit value of $V_{th}$. This was repeated for a total of six scans. These six values of SBH at the edge (or center) were then used to determine the average SBH at the edge (or center) and its statistical uncertainty.

![Figure 6.20](image.png)

**Figure 6.20**: Typical BEEM $I_c-V_T$ data (circles and diamonds) and Bell-Kaiser (BK) model fits (solid lines) and best-fit barrier heights (arrows) at the NW5 center and edge. The data of NW center (edge) is an average of 10 (30) individual $I_c-V_T$ curves measured at 2 (6) different locations labeled as in square (circle) marks in Figure 6.19(a) and (b). The top curve has been vertically offset for clarity. Tip current was 10 nA for both sets of data.
Using the data analysis procedure described above, the average barrier height at the center of NW5 at 80 K was found to be $0.850 \pm 0.002\text{eV}$, while the average barrier height along the edge of NW5 was found to be $0.828 \pm 0.001\text{eV}$. For NW 30 at 200K, the average barrier height at the NW center was found to be $0.809 \pm 0.002\text{eV}$, while the average barrier height at the NW edge was $0.785 \pm 0.001\text{eV}$. Hence we observe a statistically significant and reproducible decrease of the SBH close to the edge of an end-on Au/Si NW contact, as compared to that measured close to the center of the Au/Si NW contact. The local SBH at the edge of these two separate NWs is $\sim 23 \pm 3 \text{ meV}$ lower than at the NWs center. Note that the slightly higher SBH measured at NW5 compared to NW30 is due to the lower temperature measured at NW5 (80K) than NW30 (200K), which is consistent with previous reports in the literature [78] for large-area Au/Si contacts. The increased SBH at lower temperature is mainly due to the larger bandgap of Si at lower temperature [78].

We next investigate different possible reasons that might cause the SBH to be lower at the edge than at the center. First, in “case 1”, we assume a flat metal/Si NW interface and there are no charge along the SiO$_2$/Si NW interface, to see if the presence of metal/Si interfaces states are sufficient to account for the lower SBH at the NW edge. However in this case, the simulated SBH at the edge of the NW is $\sim 15 \text{ meV}$ higher (instead of 20 meV lower as observed from experiments) than that at the center due to the weakened Fermi-level pinning at the metal/Si NW contact edge. In “case 2”, we assume a flat metal/Si NW interface and a uniform fixed negative or positive charge along the NW Si/SiO$_2$ interface. Finite element electrostatic simulations indicate that a large amount of
positive fixed charge at the NW Si/SiO₂ could produce the (observed) lower SBH at the NW edge as compared to the NW center, due to the much stronger electric field close to the NW edge than near the NW center, with a resulting larger image force lowering of the SBH. However, a large positive fixed charge appears to contradict other recent measurements of interface charge on Si NWs [79]. In “case 3”, we assume a flat metal/Si NW interface and interface states along the Si/SiO₂ NW interface. By assuming \( \sim 5 \times 10^{12} \) e/cm²/eV interface states density (slightly higher than the density of \( \sim 2-4 \times 10^{12} \) e/cm²/eV reported in the literature [79-81]), the finite element simulation fits the observed \( \sim 20 \) meV lower SBH at the NW edge very well. Finally in “case 4”, we assume the NW protruding several nm beyond the spin-on glass and interface states along the Si/SiO₂ NW interface. In this case the simulations can also fit the observed \( \sim 20 \) meV lower SBH at the NW edge very well, but now only need to assume a smaller \( \sim 2 \times 10^{12} \) e/cm²/eV interface state density as compared to the \( \sim 5 \times 10^{12} \) e/cm²/eV interface state density needed to match experiment for the flat (non-protruding) NW geometry. Detailed discussions of the above four cases are described in the following.

First, in case 1, a flat metal/Si NW interface (non-protruding NW geometry) and no charge along the SiO₂/Si NW interface are assumed. Finite element electrostatic calculation (done with the commercial software package Flex PDE [60]) of local NW conduction band profile (image force lowering was already included) is shown in Figure 6.21(b). The assumed geometry for finite element electrostatic simulation is shown in Figure 6.21(a) with a 130 nm diameter NW (500nm long) based on the measurements discussed before. The calculated conduction band profiles under the center and edge of
the NW are shown in Figure 6.21(b). Z = 0 corresponds to the top metal/Si NW interface and the Fermi level of the Au film (ground) is defined as zero potential energy. Dirichlet boundary conditions were assumed at the metal/Si NW (or SiO₂) interface and the back side of Si substrate with the values of the electron potential energy of conduction band given by $W_{Au} - \chi_{Si}$ and by $E_c - E_F$ respectively. The known parameters used in the calculation are the Si bandgap $E_g(80K) = 1.163$ eV, the Si electron affinity $\chi_{Si}(80K) = 4.01$ eV, the Si substrate doping $N_d = 1 \times 10^{15}$/cm³, the intrinsic Si NW doping $N_{d,NW} = 1.45 \times 10^{10}$/cm³, the dielectric constant of Si $\varepsilon_{Si} = 11.9$, and the dielectric constant of SiO₂ $\varepsilon_{SiO₂} = 3.9$. The parameters used for the Fermi-level pinning at the Au/Si NW interface are the interface dipole layer thickness $d = 0.4$ nm, the Si surface charge neutrality level $q\phi_0 = 0.33$ eV [1], the dipole layer dielectric constant $\varepsilon_{dipole} = 11.9$, and the interface state density $D_{it} = 4.76 \times 10^{14}$ states/cm²/eV (the same as the parameters used in section 6.3.5 for finite element simulations). Since the SBH of a regular Au/n-Si junction (measured by us) is ~0.800 eV at 300K and ~0.845 eV at 80K with ~5 × 10^{15}/cm³ doping, a work function of Au $W_{Au} = 4.95$ eV need to be assumed to get about the same calculated barrier height at both temperatures from the finite element simulation for a regular Au/n-Si reference sample with the same Fermi-level pinning parameters used above. So a work function of Au of 4.95 eV was chosen for the simulations in this section. The simulations in this section were all done at 80K.

As seen in Fig. 6.21(b), if no Si/SiO₂ interface charge are assumed, the simulations indicate that the conduction band profile along the edge of the NW (pink line,
Figure 6.21: (a) The assumed geometry for finite element electrostatic simulation for case 1 (no interface states at the Si/SiO$_2$ interface): NW diameter = 130 nm, NW length = 500 nm, the surrounding oxide is 2 $\mu$m wide and the Si substrate is 5 $\mu$m thick. (b) The calculated conduction band profiles (image force lowering was already added) under the center (blue line) and edge (pink line) of the NW without interface charge at the Si NW/SiO$_2$ interface. Z = 0 corresponds to the top metal/Si NW interface. Profile 2 is $\sim$1 nm (radial distance) away from the NW/SiO$_2$ interface. The Si NW is intrinsic, and the Si substrate doping $N_d = 1 \times 10^{15}$/cm$^3$. The Fermi level of the Au film (ground) is defined as zero potential energy.
1nm away from the NW/SiO₂ interface) should be ~15 meV **higher** than that along the center of the NW (blue line), instead of ~23 meV **lower** as observed in the experiments. We note that the slightly higher simulated SBH at the edge of the NW from the simulation is due to the weakened Fermi-level pinning at the metal/Si contact edge, similar to that discussed in section 6.1 for the small size contact. In short, at Au/Si interfaces, the M/S interface states develop a positive charge, which tends to pull the Si conduction band down to lower energy. But at the edge of the Au/Si NW contact, the average density of these M/S interface states is smaller than at the NW center, and so the Si conduction band will not be pulled down as much as at the NW center, resulting in a slightly higher SBH near the NW edge.

It has been reported that for some Si NWs, there may be a large density of excess charge at the NW Si/SiO₂ interface, with a density of ~1-2 ×10¹² e/cm²) [80,81]. Recently, off-axis electron holography measurements on 60nm in diameter n-Si NWs by Hertog et al. [79] indicated a large negative surface charge of ~1×10¹² e/cm² at the NW/SiO₂ interface. So we next model the possible effects of large uniform surface charge on the SBH (case 2) measured at the center and edge of Au/Si-NW contacts.

Figure 6.22(b) shows the calculated conduction and valance band profiles under the center of the NW assuming a uniform density of 1×10¹² e/cm² fixed negative charge (red lines), without charge (black lines), and with 1×10¹² e/cm² fixed positive charge (blue lines) at the Si NW/SiO₂ interface. The assumed geometry for finite element simulation is shown in Figure 6.22(a), which is the same as in Figure 6.21(a) except that
some negative or positive interface charge along the NW Si/SiO$_2$ interface was added. The fixed parameters used for the simulations are the same as discussed above.

Figure 6.22(b) shows that if we assume a density of $1 \times 10^{12} \text{ e/cm}^2$ fixed (negative) electron charge (red lines) along the NW Si/SiO$_2$ interface, that this would produce a very strong **upward** bending of the Si conduction band close to the Au/NW interface. This would produce a SBH of $\sim 1.1 \text{ eV}$ or roughly 250 meV larger than what we measured at the center of the NW at 80K. Furthermore, this upward band bending (due to negative NW/SiO$_2$ interface charge) should be even larger close to the edge of the NW. But as discussed above, we actually measured a slightly lower SBH (by $\sim 20 \text{ meV}$) close to the contact edge. So for our “end-on” metal contact to vertical Si NW sample, it does not appear possible for a large fixed negative charge density at the NW Si/SiO$_2$ interface to account for our measurements.

We also considered the effect that fixed positive charge at the NW Si/SiO$_2$ interface would have. The band profile at the NW center without surface charge (black lines) and with $1 \times 10^{12} \text{ e/cm}^2$ positive surface charge (blue lines) are also shown in Figure 6.22(b). The band profiles at the NW center for both cases bend downwards with a $W_{\text{Au-Si}} = 0.94 \text{ eV}$ potential energy difference between the Si conduction band and the metal Fermi level at the contact. But the band profile with positive surface charge bends downward much more strongly than the band profile without NW Si/SiO$_2$ interface charge. In this case (large positive fixed interface charge) the simulation also shows that the SBH at the edge of the NW is $\sim 15 \text{ meV}$ lower than that at the NW center for a uniform $1 \times 10^{12} \text{ e/cm}^2$ positive charge at the NW/oxide interface. This lowering is due to
Figure 6.22: (a) The assumed geometry for finite element electrostatic simulation for case 2 assuming large negative or positive fixed charge. (b) The calculated conduction and valance band profile along the center of the NW with $1 \times 10^{12}$/cm$^2$ negative fixed charge (red lines), without charge (black lines), and with $1 \times 10^{12}$/cm$^2$ positive fixed charge (blue lines) at the Si NW/SiO$_2$ interface. Z = 0 corresponds to the top metal/Si NW interface.
the much stronger electric file close to the NW edge than near the NW center, with a
resulting larger image force lowering of the SBH (see section 2.1.3).

So finite element simulations indicate that a large amount of positive fixed charge
at the NW Si/SiO₂ could produce the (observed) lower SBH at the NW edge as compared
to the NW center. However, a large positive fixed charge appears to contradict other
recent measurements of interface charge on Si NWs. For example, Hertog et al. [79]
reported a large negative surface charge of ~1×10¹² e/cm² at the NW/SiO₂ interface for
their long, isolated n-type NW. How can we resolve this apparent contradiction?

In the simulations described above, we assumed a large density of fixed interface
charge. However, it is well known that positive or negative charge can also reside in
interface states at a Si/SiO₂ interface [1,23]. The fixed oxide charge at a Si/SiO₂
interface does not depend the position of the Si conduction band (CB) and valence band
(VB) relative to the Fermi-level, and so stays constant even if the conduction and valence
band energies are changed, for example by application of an external electric field. That
is why it is called fixed charge. However, the interface state charge does depend on the
energy of the VB (for example) relative to the Fermi-level, and will gain or loose
interface charge in response to changes in this relative energy. Extensive electron-spin-
resonance studies showed that these interface states are mainly caused by the so called Pb
resonance centers [82-86], which were identified as trivalent silicon atoms bonded to
three underlying silicon atoms [85,86]. And it was found that the Pb centers are
amphoteric [87]. This means that in the lower half of the band gap, a Pb center is donor-
like (Pb → e⁻ + Pb⁺), which means that if the Fermi-level at the Si/SiO₂ interface is
located below mid-gap, then the \( P_b \) centers with energy between the Fermi-level and middle of the band gap become positively charged, while the \( P_b \) centers below the Fermi-level are neutral. In contrast, \( P_b \) centers in the upper half of the band gap are acceptor-like \((P_b + e^- \rightarrow P_b^-)\), which means that if the Fermi-level at the Si/SiO\(_2\) interface is located above mid-gap, then the \( P_b \) centers located between the Fermi-level and middle band gap become negatively charged, while the \( P_b \) centers above the Fermi-level are neutral [23]. This behavior is somewhat similar to the metal/semiconductor interface states described in section 2.1.2, except that (i) interface states at the Si/SiO\(_2\) interface have a different physical origin, and (ii) the charge neutrality level (CNL) for Si/SiO\(_2\) interface states is generally assumed to be located close to mid-gap, as discussed above.

Since the interface states charge are widely believed to be the most important source of charge at the Si NW/native SiO\(_2\) interface, in the following discussion we will assume that there is no fixed charge, and only concentrate on the effect of NW/SiO\(_2\) interface states charge on the Si NW band structure.

Figure 6.23 shows the expected band bending (along the radial direction as the red dashed line indicated in (a)) for a long, isolated n-type or p-type Si NW that has Si/SiO\(_2\) interface states, and is assumed to have a large enough doping that it behaves like bulk Si close to the center of the NW. Here, by isolated we assume that the NW is located far from other interfaces or contacts. Following the above discussion, the CNL of the interface states is assumed to be located at the intrinsic Fermi-level \( E_i = \frac{E_g}{2} + kT \frac{N_i}{N_C} \), (close to the middle of the Si band gap [1]). This means that if the Fermi energy \( E_F \) at the Si/SiO\(_2\) interface is above \( E_i (E_i < E_F) \), then the net
Figure 6.23: The expected band bending (along the radial direction illustrated by the red dashed line in (a)) for a long, isolated (b) n-type or (c) p-type Si NW that has Si/SiO$_2$ interface states. By isolated, it is assumed that the NW is located far from other interfaces or contacts.
interface charge is negative, while if \( E_F \) is below \( E_i \) (\( E_i > E_F \)) the interface charge will be positive. This will tend to pin \( E_F \) close to \( E_i \) at the interface, as described below. The interface charge density \( Q_{it} \) can be described by \( Q_{it} = D_{it} \times (E_i - E_F) \), where the interface state density \( D_{it} \) has units of \((\text{cm}^{-2} \text{eV}^{-1})\) [23]. For isolated n-type NWs, the donors ionize to become positively charged for regions of the NW where the CB is far above \( E_F \), which pulls the conduction band (CB) down toward \( E_F \). This causes \( E_i \) to be pulled below \( E_F \) at the Si/SiO\(_2\) interface, causing negative interface charge to form, and resulting in upward band-bending at the Si/SiO\(_2\) interface as illustrated in Figure 6.23 (b). In contrast, for isolated p-type NWs (Figure 6.23 (c)) acceptors in the NW ionize to become negatively charged, which pushes the valence band (VB) up toward \( E_F \), which pushes \( E_i \) above \( E_F \) at the Si/SiO\(_2\) interface, leading to positive interface charge and resulting downward band-bending at the Si/SiO\(_2\) interface. This would explain why Hertog et al. [79] observed a large negative surface charge of \( \sim 1 \times 10^{12} \text{e}/\text{cm}^2 \) at the NW/SiO\(_2\) interface for their long, isolated n-type NW.

Now let us model the possible effects of interface states charge on the Si NW conduction band bending (case 3) of our “end-on” Au contact on vertical Si NW, which is assumed to be intrinsic (no doping at all). We note that for our NW geometry (~130 nm in diameter, 500 nm long in Figure 6.24(a)) any doping less than \( \sim 10^{15}/\text{cm}^3 \) behaves nearly the same as an intrinsic NW, because the total number of dopant atoms in the volume of this small NW would be extremely small (at \( 10^{15}/\text{cm}^3 \), there would only be \( \sim 7 \) dopant atoms in the entire volume of the NW). The biggest difference here compared to an isolated NW is that close to the Au contact, the high work-function Au metal causes
**Figure 6.24:** (a) The assumed geometry for the finite element electrostatic simulation for case 3 assuming no fixed charge, but assuming interface states along the Si/SiO₂ interface. (b) The calculated conduction band profile along the center of the NW assuming $5 \times 10^{12} \text{e/cm}^2/\text{eV}$ interface states density at the Si NW/SiO₂ interface. $Z = 0$ corresponds to the top metal/Si NW interface. The pink dashed line indicates the end of the NW. The resulting non-uniform interface charge at the NW/SiO₂ interface is illustrated in (a).
the Schottky barrier to be large (~0.8 eV), which means that the Si CB is pulled up to ~0.8 eV above \( E_F \). This pulls \( E_i \) of the Si NW well above \( E_F \) (in the part of the NW close to the contact), which would result in large positive charge forming at the Si/SiO\(_2\) interface in that part of the NW. The simulated Si NW conduction band profile along the NW center is shown in Figure 6.24(b), assuming an interface state density \( D_{it} = 5 \times 10^{12} \) \( e/\text{cm}^2/\text{eV} \), which is similar to what is assumed in the literature (~2-4 \( \times \) \( 10^{12} \) \( e/\text{cm}^2/\text{eV} \)) for a Si/native SiO\(_2\) interface [79-81] (see Appendix A.2 for the sample modeling program).

The three most important points here are: (a) close to the Au contact, the large positive interface charge produces a large electric field in the NW, pulling the CB down as you move down the NW. (b) Moving down the NW, the CB drops from ~0.8 eV above \( E_F \) to close to mid-gap, at which point \( E_i \) is close to \( E_F \) causing the interface charge to become nearly zero. (c) Close to the (n-type) Si substrate, ionized donors in the substrate pull the NW CB down more strongly until it is close to \( E_F \) near the NW/substrate interface. This pulls \( E_i \) below \( E_F \), causing some negative charge along the Si/SiO\(_2\) interface at the substrate end of the NW.

We next consider the Si NW band bending along six different paths as shown in Figure 6.25. Figure 6.26 shows the Si NW conduction band profiles along the radial direction at different depth \( Z \) (profiles 3 to 6 as in Figure 6.25). For regions close to the “end-on” contact (\( Z = 10 \) nm in Figure 6.26(a)), \( E_i > E_F \), so there is positive charge accumulated at the NW/SiO\(_2\) interface, which would pull the conduction band down more at the edge than at the NW center. For regions close to the NW/Si substrate junction (\( Z = 450 \) nm in Figure 6.26(d)), \( E_i < E_F \), so there is negative charge accumulated at the
NW/SiO₂ interface, which would pull the conduction band up more at the edge compared to the NW center. Midway down the NW (Z = 300 nm in Figure 6.26(c)) there is little interface charge and so little lateral bend-bending.

**Figure 6.25:** Six different paths in the Si NW for the following band bending calculation. Profile 1: along the NW center, Profile 2: Parallel to profile 1, but 1 nm away from the NW/SiO₂ interface, Profiles 3 -6 are perpendicular to the NW long axis, with Profile 3: Z = 10 nm, Profile 4: Z = 100 nm, Profile 5: Z = 300 nm, Profile 6: Z = 450 nm.

Finally, Figure 6.27 compares the CB profile along the NW center to a CB profile at the edge of the NW. Since there is positive interface charge at the Si/SiO₂ interface close the Au contact, the electric field is stronger close to the edge, causing a ~20 meV lower SBH at the edge (image force lowering was already included). This slight lowering of the SBH close to the NW edge is in very good agreement with our measurements.
Figure 6.26: The simulated Si NW conduction band bending profiles along the radial direction at different depth $Z$, with $D_{it} = 5 \times 10^{12} \text{e/cm}^2/\text{eV}$. NW diameter = 130 nm. Close to the NW contact ($Z = 10$ nm), the NW CB is pulled down more at the edge than at the center; while close to the n-Si substrate ($Z = 450$ nm), the NW CB is pushed up more at the edge than at the center.
Figure 6.27: The simulated CB profiles along the NW center (blue line) and a parallel path close to edge (pink line), with $D_{it} = 5 \times 10^{12} \text{e/cm}^2/\text{eV}$. Image force lowering was added after finite-element simulation simulation.

So our finite element simulation indicates that the interface state charge should be distributed non-uniformly along the Si NW/SiO$_2$ interface for our “end-on” Au contacts to vertical Si NWs. There should be a large amount of positive interface charge formed near the contact due to the presence of ~0.8 eV Au/Si NW SBH at the contact, which would not be seen for a long, isolated n-Si NW reported before [79]. By assuming ~$5 \times 10^{12} \text{e/cm}^2/\text{eV}$ interface states density (slightly higher than the density of ~2-4$\times 10^{12}$ e/cm$^2$/eV reported in the literature [79-81]), the finite element simulation agrees with our experiment results very well.

For the finite element simulations discussed so far, it was assumed that the polished ends of the NWs were at the same level as the surrounding polished spin-on
glass, so that the resulting Au interfaces would be flat. However, as we discussed in section 6.3.1, the NWs usually protrudes several nm beyond the surface of the spin-on glass (~6-10 nm higher than the surrounding surface) as shown in the STM topographic images of Figure 6.8(a), (c), and (e). So we next consider possible effects of this special geometry on the SBH at the NW center and edge (case 4).

Figure 6.28(a) shows the modified drawing of our “end-on” Au contact to vertical Si NWs sample with the NW protruding ~8 nm out of the spin-on glass (very close to the real geometry). The calculated NW conduction band profiles along its center and edge are shown in Figure 6.28(b) without or with interface states charge (image force lowering was added after calculation). The same finite element simulation parameters are used as discussed above except for the protruding NW geometry and a different NW Si/SiO$_2$ interface states density (which will be discussed below). If there are no interface states at the NW/SiO$_2$ interface, these simulations indicated that the CB profile at the NW edge (red line in Figure 6.28) would be slightly higher than that at the NW center (black line), which is similar to the simulation shown in Figure 6.21(b), which assumed no interface states and without the NW protruding beyond the spin-on glass.

But with the assumed protruding NW geometry shown in Fig. 6.28 and now assuming $\sim2\times10^{12}$ $e$/cm$^2$/eV interface state density at the NW/SiO$_2$ interface, the SBH at the NW edge is found to be $\sim$20 meV lower than at the NW center. So in this case the simulations can fit the observed $\sim$20 meV lower SBH at the NW edge very well, but now only need to assume a smaller $\sim2\times10^{12}$ $e$/cm$^2$/eV interface state density as compared to the $\sim5\times10^{12}$ $e$/cm$^2$/eV interface state density needed to match experiment for the flat
Figure 6.28: (a) The assumed geometry for finite element electrostatic simulation (for case 4) as in Figure 6.21(a) except that the NW now protrudes 8 nm beyond the surrounding polished spin-on glass. (b) The simulated CB profiles along the NW center (Profile 1 in (a)) and the NW edge (Profile 2 in (a)), both without or with an interface state density of $2 \times 10^{12}$ e/cm$^2$/eV. Image force lowering was added after the simulation.
(non-protruding) NW geometry. This smaller $\sim 2 \times 10^{12} \text{e/cm}^2/\text{eV}$ interface state density agrees much better with the interface state density of $2 - 4 \times 10^{12} \text{e/cm}^2/\text{eV}$ for NW/native oxide interface reported in the literature [79-81]. This is because the protruding NW geometry produces a geometry-enhanced electric field effect at the NW edge, similar to the “lightening rod effect” that occurs close to sharp edges of conductor surfaces. This amplifies the electric fields at the NW edge, so a smaller interface state density along the NW/SiO$_2$ interface is needed to produce the same magnitude of electric field at the NW edge needed to reduce the SBH by $\sim 20$ meV, as compared to the SBH at the NW center.

In summary, at near-threshold electron injection (with the hot-electron energy just above the $\sim 0.8$ eV SBH and with small injection current), we observe lateral variations of the local SBH across individual end-on Au Schottky contacts, with the SBH at the contact edge of two separate NWs found to be $23 \pm 3$ meV lower than at the NW center. Finite element electrostatic simulations suggest that this is due to a larger interface electric field at the contact edge due to positively charged Si/SiO$_2$ interface states near the Au/NW contact, with this (equilibrium) interface state charge induced by local band bending due to the high work function Au contact.

### 6.5 Trial of PECVD deposition of SiO$_2$ on as-grown Si NWs

As discussed in section 6.2, we found that “craters” formed around most of the Si NWs embedded in spin-on glass, probably due to the 850°C annealing step after depositing the spin-on glass. And due to the much faster BHF etch rate of the annealed
spin-on glass (~4-5 Å/s for the spin-on glass compared to ~1 Å/s for native SiO₂) (because it was not as high quality as thermal SiO₂), the Si NWs were left protruding several nm beyond the surrounding spin-on glass before the Au film deposition step. In order to improve the sample surface smoothness, we tried to use plasma-enhanced chemical vapor deposition (PECVD) to deposit SiO₂ on as-grown 80nm in diameter vertical Si NWs. The PECVD was done at the Penn State Materials Research Institute using AMAT 5000 PECVD System (http://www.mri.psu.edu/facilities.asp).

Figure 6.29 (a) shows an example SEM image of the Si NWs after a nominally 500 nm thick PECVD SiO₂ film was deposited. After this coating layer of PECVD SiO₂, the NW diameter was observed to increase to ~500 nm, which indicates that ~200 nm thick SiO₂ layer was deposited on the Si NWs. Figure 6.29 (b) shows the AFM image of the NWs sample after the CMP polish, where μm-size holes were seen everywhere on the sample. Samples made this way were found to be very leaky (~200 Ohm zero bias resistance at room temperature) after the Au film deposition step. A reference n-Si wafer was also coated with PECVD SiO₂ along with the NW sample. The reference sample surface after PECVD deposition is very smooth even before CMP polish (~1nm RMS roughness) and shows very high zero bias resistance (>10 TOhm), which indicates a high quality SiO₂ film. So we think that the μm-size holes were caused by non-uniform SiO₂ deposition due to the presence of vertical Si NWs, which may have allowed direct contact between the deposited Au film and the Si substrate, resulting in an extremely leaky NW sample.
Figure 6.29: (a) An example SEM image of PECVD SiO₂ (nominally 500 nm thick) deposition on 80 nm in diameter vertical Si NWs. The perspective of the SEM image is 45°. (b) AFM image of the NW sample after 20 min CMP polish. Color scale: 50nm.
Figure 6.30: An example SEM (a) and AFM (b) image of PECVD SiO₂ deposition on 80 nm diameter vertical Si NWs followed by one layer of spin-on glass coating and CMP polish.
Figure 6.31: (a) An example SEM image of PECVD SiO$_2$ (nominally 150 nm thick) deposition on 80 nm in diameter vertical Si NWs. The perspective of the SEM image is 45°. (b) AFM image of the polished NW sample with 3 layers of spin-on glass coating after PECVD SiO$_2$ deposition.
In order to improve this, we also tried to spin coat one layer of spin-on glass on the NW sample after the PECVD SiO\textsubscript{2} deposition, to try to fill in the holes. Figure 6.30 shows the SEM and AFM images after the CMP polish of this sample. We can clearly see vertical Si NWs embedded in oxide and even some lying down NWs buried underneath the oxide. Furthermore, the \(\mu\)m-size holes seen in the NW sample with only with PECVD SiO\textsubscript{2} deposition no longer are seen. However, the sample was still found to be very leaky, with \(~\)10 kohm zero bias resistance (compared to \(~\)3Mohm zero bias resistance of samples with only the spin-on glass coating). Since for the “end-on” metal contacts to vertical Si NWs sample discussed before, we often applied 2 or 3 layers of spin-on glass, we suspect that one layer of spin-on glass might not be sufficient. So we next tried a thin layer of PECVD SiO\textsubscript{2} deposition followed by 3 layers of spin-on glass.

Figure 6.31(a) shows an example SEM image of the Si NWs after a nominally 150 nm thick PECVD SiO\textsubscript{2} deposition. The SiO\textsubscript{2} layer surrounding the NWs was estimated to be \(~\)50 nm thick. We then spin coated 3 layers of spin-on glass and annealed it as discussed in section 6.2. The AFM image shows that sample surface is very smooth (\(~\)0.7 nm RMS roughness) after the CMP polish (as in Figure 6.31(b). However, we again found the final sample to be very leaky (\(~\)4 Kohm zero bias resistance). This is very puzzling since for the new procedure of making “end-on” metal contacts to vertical Si NWs sample we only added one more step, the PECVD SiO\textsubscript{2} deposition, and the PECVD SiO\textsubscript{2} quality by itself was found to be very good. So we can only suspect that the plasma might damage the Si NWs during plasma-enhanced CVD SiO\textsubscript{2} deposition. Further experiments need to be done to verify this.
6.6 Conclusions

In summary, a procedure has been introduced to make “end-on” metal contacts to vertical Si NWs. BEEM measurements of most of the “end-on” Au contacts to 80-nm-diameter vertical Si NWs showed a strong suppression of hot-electron injection at higher tip voltages, as compared to regular Au/Si junctions. The strong increase of this BEEM current suppression with increasing tunneling current suggests that this current suppression is due to a steady-state charge build up in the NWs, which increases as more current is injected into the NW. The BEEM current suppression of the NWs was also found to increase strongly as the temperature was decreased, which indicates more steady-state charge build-up at lower temperature. Time-dependent BEEM current suppression in these Au/NW contacts was observed when the tunnel current was abruptly increased and decreased, directly supporting a model in which the BEEM current suppression is due to (temperature-dependent) steady-state charge build up. We postulate that these electrons might be held in meta-stable traps at the Si NW/SiO₂ interface in the part of the NW close to the metal/Si NW contact. This model is supported by finite element electrostatic simulations, which show that as few as 50 trapped electrons close to the end-on contact would strongly raise the conduction band energy, which would strongly suppress hot electron injection.

At tip voltages just above threshold, the BEEM current is very small and the current suppression effects discussed above are negligible. In this case, BEEM can be used to measure the “intrinsic” SBH at different parts of the end-on Au/Si NW contact. We have successfully used nm-spatial resolution BEEM to distinguish the SBH
difference between NW’s center and edge, and found that the local SBH at the edge of
two separate NWs is ~20 meV lower than at the NWs center, most likely due to a
stronger local electric field at the contact edge caused by positive charge at the NW/oxide
interface near the contact. Assuming \(2 \times 10^{12} \text{ e/cm}^2/\text{eV} \) interface states density (as
reported in the literature for NW/native oxide interface [79-81]) and including the special
geometry of our sample (where the NW protrudes ~8 nm beyond the surrounding spin-on
glass), the simulated SBH at the NW edge was found to be 20 meV lower than that at the
NW center, in good agreement with our BEEM measurements. This study also indicates
that BEEM is quite sensitive to surface charge on the NW and could be an efficient tool
for NW surface electronic characterization.

6.7 Future directions

6.7.1 Try “end-on” Cu contacts to vertical Si NWs

Figure 6.32(b) shows the calculated Si NW CB profiles along the NW center
(blue line) and edge (pink line) for “end-on” contacts to vertical Si NWs, where the metal
Cu is used instead of Au to make the Schottky contacts. The sample geometry (Figure
6.32(a)) used for the finite element simulation is the same as that in Figure 6.28(a). The
Cu work function was assumed to be 4.375 eV in order to get a ~0.65 eV SBH, which is
what was measured for a regular Cu/bulk n-Si sample (with \(N_d = 5 \times 10^{15}/\text{cm}^3 \)) by Che and
Pelz [88]. In the simulations, we again assumed a ~2 \times 10^{12} \text{ e/cm}^2/\text{eV} interface state
density at the NW/oxide interface, with the other parameters assumed to be the same as
those used for the simulations of end-on Au/Si NW contacts as shown in Figure 6.28(b).
Figure 6.32: (a) The assumed geometry for finite element electrostatic simulation of end-on Cu/Si contacts. (b) The calculated conduction band profiles (image force lowering was added after the simulation) along the center (blue line) and edge (pink line) of the Cu/Si NW contact, assuming an interface states density of $2 \times 10^{12} \text{e/cm}^2/\text{eV}$ at the Si NW/SiO$_2$ interface. $Z = 0$ corresponds to the top metal/Si NW interface. The arrows indicate the profile paths along the NW center and edge, respectively.
We note two important results from these new simulations of end-on Cu/Si NW contacts:

1. The simulated SBH at the NW edge was found to be \(~70\) meV lower than that at the center, a much larger decrease at the NW edge as compared to the measurements and simulations of end-on Au/Si NW contacts. (2) Since the Cu/Si NW SBH of \(~0.65\) eV is much smaller than the \(~0.8\) eV SBH for Au/Si NW contacts, in this case the intrinsic energy \(E_i\) of the Si is very close to the Fermi-level \(E_F\) in the part of the NW close to the Cu contact, which would result in very little interface charge at the NW/oxide interface. So for Cu/Si NW contacts, the presence of interface states at the Si/SiO\(_2\) interface should have little effect on the SBH, in contrast to the case of Au/Si NW contacts. Indeed, finite element simulations assuming no Si/SiO\(_2\) interface states at all were found to show almost the same SBH difference (\(~65\) meV) between the NW center and edge as the \(~70\) meV difference for the case with a \(2\times10^{12}\) e/cm\(^2\)/eV interface state density. So in the case of Cu/Si NW contacts, the very large (\(~70\) meV) predicted SBH difference between the NW center and NW edge mostly due to weakened Fermi-level pinning at the NW edge.

In short, for the case of a low-work-function metal/Si contact, the metal/Si interface states that produce Fermi-level pinning in metal/Si contacts (see section 2.1.2) would develop a negative interface charge, which increases the SBH above what would be expected in the absence of metal/Si interface states. But at the edge of the end-on contact the average interface state density is smaller since metal/Si interface states only exist on one side on the contact (they don’t exist at the metal/SiO\(_2\) interface on the other side of the contact). So in this case, we would expect a much lower SBH close to the NW edge as compared to the NW center. So by studying this low work function Cu “end-on” contact to vertical
Si NWs, we should be able to directly observe weakened Fermi-level pinning effects, similar to those expected for very small diameter Si NWs (<30 nm), as discussed in Section 6.1.

6.7.2 Improve the procedure of making “end-on” metal contact to vertical Si NWs

It was intensively reported in the literature that the NW/oxide interface states density [23, 80] and surface traps density [13] could be decreased by a factor or several tens by growing a high quality SiO\textsubscript{2} surrounding the Si NW. The best way to get a high quality SiO\textsubscript{2} surrounding the Si NW is thermally oxidizing a fraction of the NW. But since Au diffuses very fast at high temperatures (~1100°C was normally used for dry oxidization of Si), the Au catalyst particles at the NWs end should be removed before thermal oxidization. Yang et al. [13] have proved that they can make NW devices with much lower interface trap density at the NW/oxide interface using this method.

So we should be able to modify our procedure of making “end-on” metal contacts to vertical Si NWs (discussed in section 6.2) by adding two more steps right before the spin-on glass fill: (1) perform an Au catalyst etch, and (2) then thermally oxidizes the Si NWs to produce a high-quality Si/thermal SiO\textsubscript{2} interface around the Si NWs. Using this modified procedure, we should expect a much lower Si/SiO\textsubscript{2} interface state density, and so should see much weaker NW Si/SiO\textsubscript{2} interface effects. In particular, we should see much smaller BEEM current suppression (discussed in section 6.3) and smaller difference in the SBH between the center and edge of end-on Au/Si NW contacts.
(discussed in section 6.4). Improving the quality of the NW Si/SiO$_2$ interface will be the goal of future experiments.
CHAPTER 7

Summary

We have performed BEEM experiments on 5 nm-Pt/10 nm-SiO₂/Si and 5 nm-Pt/1.4 nm-Al/SiO₂/Si gate stack MOS structures. Direct BEEM images do not reveal significantly larger spatial variations on the metal bi-layer sample than observed on the uniform Pt film sample, indicating that any inhomogeneities along the metal bi-layer/SiO₂ sample are smaller than the estimated ~10 nm BEEM spatial resolution for a sample with a ~5 nm thick Pt film. However, BEEM measurements of the dependence on gate voltage of the average energy barrier height show a different behavior for a metal bi-layer/SiO₂ sample as compared with the uniform Pt/SiO₂/Si sample, consistent with finite element electrostatic simulations that assume nm-scale “patches” of different EFW for the metal bi-layer sample, indicating that the bi-layer sample is in fact inhomogeneous at the nm-scale. This study suggests that the large reported “tunability” of the EWF of metal bi-layer samples [2,3] is due to an inhomogeneous metal/SiO₂ interface, with the top metal filling in “pinholes” in the bottom metal film.

We have used BEEM in combination with Int-PE and PC to investigate band alignment and carrier transport in 20 nm-thick epitaxial Sc₂O₃/Si (111) and epitaxial
Lu$_2$O$_3$/Si (111) films grown epitaxially at 700 °C on a Si(111) substrate. Int-PE measurements on both epi-Sc$_2$O$_3$/Si and epi-Lu$_2$O$_3$/Si films show the existence of a lower conduction band extending ~1 eV below the main CB, as have been reported for a variety of amorphous oxide films [9-11], indicating that these states are not simply due to disorder in the amorphous films. BEEM and Int-PE measurements on metal/epi-Sc$_2$O$_3$/Si show that the CB measured from the metal-side lines up with the “tail states” CB measured from the Si side. Most significantly the BEEM data clearly shows that this lower CB supports elastic transport across the 20 nm-thick epi-Sc$_2$O$_3$ even against an applied electric field, and so is a robust CB consisting of extended rather than localized states. However, for Pt/epi-Lu$_2$O$_3$/Si the CB measured from the metal-side lines up between the “tail states” and “primary” CB measured from the Si side, possibly due to two layers of different composition in Lu$_2$O$_3$. Int-PE/PC and C-V measurements on Pt/epi-Lu$_2$O$_3$/Si indicates that there is a large amount of positive charge in the oxide, most of which could be removed by a ~350ºC post-metallization vacuum anneal. And BEEM measurements on Pt/epi-Lu$_2$O$_3$/Si found ~0.3-0.4 eV higher energy barrier at metal/oxide interface than found by Int-PE (while BEEM and Int-PE agree with each other well in Pt/epi-Sc$_2$O$_3$/Si study), which might suggest significant transient charge trapping in this Lu$_2$O$_3$ sample at high injected electron flux density.

We have successfully developed a procedure of making “end-on” metal contacts to vertical Si NWs. As compared to a regular Au/Si junction, the hot-electron BEEM current through Au/Si NWs end-on contacts show strong suppression of hot-electron injection at higher injected current in the NWs (produced either by increasing the tip
voltage or the tunneling current), suggesting that this current suppression is due to a steady-state charge build-up in the NW that increase as more current is injected into the NW. The BEEM current suppression of most NWs was also found to increase strongly as the temperature was decreased, indicating larger steady-state charge build up at lower temperature. Time-dependent current suppression due to changing steady-state charge build-up in the NWs was observed when the tunnel current was abruptly increased and decreased, respectively, giving direct support to a model in which the BEEM current suppression is due to (temperature-dependent) steady-state charge build up. Finite element electrostatic simulation suggests that those electrons might be trapped at the Si NW/SiO₂ interface close to the metal/Si NW contact. We also found that the local SBH at the edge of two separate NWs is ~20 meV lower than at the NWs center, most likely due to a stronger local electric field at the contact edge. Assuming ~2×10¹² e/cm²/eV interface states density (as reported in the literature for NW/native oxide interface [79-81]) and considering the special geometry of our sample (the NW protrudes ~8 nm out of the spin-on glass), the simulated SBH at the NW edge is ~20 meV lower than at the NW center, which agrees with our experimental measurements very well. This study also indicates that BEEM is quite sensitive to surface charge on the NW and could be an efficient tool for NW surface electronic characterization.
A.1 Sample FlexPDE script of finite-element modeling of barrier height dependence on gate voltage of bi-layer Pt/Al/SiO$_2$/n-Si (heavily doped)

{This program is for calculating the potential profiles along two different paths normal to an inhomogeneous metal/oxide interface, consisting of a 50% coverage of 4 nm diameter circular patches of a low EWF metal (Pt/Al alloy) surrounded by a high EWF metal (Pt).}
{The substrate bias is zero here and can be changed.}
{The SiO$_2$ thickness is 10nm.}

TITLE ' bi-layer Pt/Al on SiO$_2$ ' 

SELECT 
  errlim = 1.0e-4 

coordinates 
cartesian3 

VARIABLES 
Phi 

DEFINITIONS 
  SB1=4.22 {BH between Pt and SiO$_2$}
  SB2=3.81 {BH between Pt/Al alloy and SiO$_2$}
  SB3=3.23 {BH between Si and SiO$_2$}
  Vb=0 {external bias on substrate}
  R1=2.03e-9 {radius of Al circle}
  R2=2e-9 {radius of Pt-Al boundary circle}
EQUATIONS
\[ \text{div}( \text{grad}(\Phi) ) = 0 \]

Extrusion
Surface 'bottom' z=0
Layer 'material'
Surface 'top' z=10e-9

BOUNDARIES
Surface 'top' Value(\(\Phi\))=SB3-Vb
Region 1 'Pt-background'
  Surface 'bottom' Value(\(\Phi\))=SB1
  Start(-2.51e-9,-2.51e-9)
  Layer 'material' Natural(\(\Phi\))=0 Line To (2.51e-9,-2.51e-9)
  Layer 'material' Natural(\(\Phi\))=0 Line To (2.51e-9,2.51e-9)
  Layer 'material' Natural(\(\Phi\))=0 Line To (-2.51e-9,2.51e-9)
  Layer 'material' Natural(\(\Phi\))=0 Line To Finish
Region 2 'Pt-Al-boundary'
  Surface 'bottom' Value(\(\Phi\))=SB2+(SB1-SB2)*(sqrt(x*x+y*y)-R2)/(R1-R2)
  Start 'ring'(R1,0) Arc(Center=0,0) Angle=360 To finish
Region 3 'Al-circle'
  Surface 'bottom' Value(\(\Phi\))=SB2
  Start 'ring'(R2,0) Arc(Center=0,0) Angle=360 To finish

PLOTS
CONTOUR(\(\Phi\)) on x=0
  Elevation(\(\Phi\)) From (0,0,0) to (0,0,10e-9) export(2500) file "Pt-Al-3dimensional-2nm_2.51nm_0v_A13.txt" format "#x #b #y #b #z #b #1"
  Elevation(\(\Phi\)) From (2.51e-9,2.51e-9,0) to (2.51e-9,2.51e-9,10e-9) export(2500) file "Pt-Al-3dimensional-2nm_2.51nm_0v_Pt3.txt" format "#x #b #y #b #z #b #1"

END
A.2 Sample FlexPDE script of finite-element modeling of lateral variations of SBH across “end-on” metal contacts to vertical Si NWs with the presence of interface charge

{This program is for calculating the Si NW conduction band profiles along different paths with the presence of interface charge.}
{The diameter and length of the Si NW is 130 nm and 500 nm, respectively.}
{The Si NW is intrinsic, and the doping of the n-Si substrate is 1e21 (1/m³).}
{Interface states density is 5e16 (e/eV/m²).}
{T = 80 K}

TITLE ' Au/intrinsic Si NW-SiO₂/n-Si '

SELECT
  errlim = 1.0e-6

coordinates
  XCYLINDER

VARIABLES
  Phi(range=-5,5)

DEFINITIONS
  w1=4.95           {work function of metal}
  w2=4.007          {electron affinity of Si}
  eps0=8.854e-12    {vacuum permittivity, F/m}
  eps1=11.9         {dielectric constant of Si}
  eps2=3.9          {dielectric constant of SiO₂}
  elec=1.602e-19    {electron charge, coulomb}
  Nc=3.85577e24     {effective density of states of Si}
  Nv=1.43214e24     {effective density of states of p-Si}
  Ec=0.057          {conduction band relative to Fermi-level in bulk Si}
  Eg = 1.163        {band gap of Si}
  Ei = Eg/2-(0.0259*80/300)/2*ln(Nv/Nc)  {intrinsic Fermi-level}
  Nd1=Nc*exp(-Ec/(0.0259*80/300))       {donor density in Si}
  Na1=Nv*exp(-(Eg-Ec)/(0.0259*80/300))  {acceptor density in Si}
  Nd2=Nc*exp(-Ei/(0.0259*80/300))       {donor density in intrinsic Si NW}
  Na2=Nv*exp(-(Eg-Ei)/(0.0259*80/300))  {acceptor density in intrinsic Si NW}
  Dit = 42.84E17    {interface density of states in Si}
  Den = 5e16        {interface states density at SiO₂/Si surface}
CNL = 0.33 \{\text{charge neutrality level, V}\}
R1 = 6.5e-8 \{\text{radius of the nanowire}\}
R2 = 1e-6 \{\text{radius of the oxide}\}
D_{is} = 4e-10 \{\text{dipole layer thickness}\}
L1 = 5e-7 \{\text{length of the nanowire}\}
L2 = 5e-6 \{\text{total length of the Si Substrate}\}
Nd
Na
eps
n_c
n_a

EQUATIONS
\[ \text{div}(\epsilon * \epsilon_0 * \nabla \Phi) = \text{elec}(\text{Nd} - \text{n}_c - \text{Na} + \text{n}_a) \]

BOUNDARIES
Region 1 'dipole layer'
\[ \text{Nd} = \text{Nd1} \]
\[ \text{n}_c = \text{Nd1} \]
\[ \text{Na} = \text{Na1} \]
\[ \text{n}_a = \text{Na1} \]
\[ \text{eps} = \text{eps1} \]
\[ \text{Start}(0,0) \]
\[ \text{value}(\Phi) = w1-w2 \text{ Line to } (0,R1) \]
\[ \text{natural}(\Phi) = 0 \text{ Line to } (D_{is},R1) \]
\[ \text{natural}(\Phi) = -\text{elec} * \text{Den} * (\Phi - E_i) \text{ Line to } (D_{is},0) \]
\[ \text{natural}(\Phi) = 0 \text{ Line to Finish} \]
Region 2 'Si NW'
\[ \text{Nd} = \text{Nd2} \]
\[ \text{n}_c = \text{Nc} * \exp(-\Phi) / (0.0259*80/300) \]
\[ \text{Na} = \text{Na2} \]
\[ \text{n}_a = \text{Nv} * \exp(-(E_g-\Phi)/(0.0259*80/300)) \]
\[ \text{eps} = \text{eps1} \]
\[ \text{Start}(D_{is},0) \]
\[ \text{Line to } (D_{is},R1) \]
\[ \text{natural}(\Phi) = -\text{elec} * \text{Den} * (\Phi - E_i) \text{ Line to } (L1,R1) \]
\[ \text{natural}(\Phi) = 0 \text{ Line to } (L1,0) \]
\[ \text{natural}(\Phi) = 0 \text{ Line to Finish} \]
Region 3 'Au-SiO2'
\[ \text{Nd} = \text{Nd1} \]
\[ \text{n}_c = \text{Nd1} \]
\[ \text{Na} = \text{Na1} \]
\[ \text{n}_a = \text{Na1} \]
\[ \text{eps} = \text{eps2} \]
Start(0,R1)
value(\Phi)=w1-w2 Line to (0,R2)
natural(\Phi)=0 Line to (L1,R2)
natural(\Phi)=0 Line to (L1,R1)
natural(\Phi)=0 Line to Finish
Region 4 'Si substrate'
Nd = Nd1
n_c=Nc * exp(-(\Phi) / (0.0259*80/300))
Na = Na1
n_a = Nv*exp(-(Eg-\Phi)/(0.0259*80/300))
eps=eps1
Start(L1,0)
natural(\Phi)=0 Line to (L1,R2)
natural(\Phi)=0 Line to (L2,R2)
value(\Phi)=Ec Line to (L2,0)
natural(\Phi)=0 Line to Finish

PLOTS
CONTOUR(\Phi) on 'Si NW'
VECTOR(-\text{grad}(\Phi)) on 'Si NW'
Elevation(\Phi) From (0,0) to (L2,0) export(2500) file "3Au-SiO2-SiNW_sheet江县1.txt" format "#x #b #y #b #1"
Elevation(\Phi) From (0,0) to (2e-8,0) export(2500) file "3Au-SiO2-SiNW_sheet江县_zoom1.txt" format "#x #b #y #b #1"
Elevation(\Phi) From (0,0) to (1e-6,0) export(2500) file "3Au-SiO2-SiNW_sheet江县_zoom2.txt" format "#x #b #y #b #1"
Elevation(\Phi) From (0,6.0e-8) to (2e-8,6.0e-8) export(2500) file "3Au-SiO2-SiNW_edge_zoom1.txt" format "#x #b #y #b #1"
Elevation(\Phi) From (0,6.4e-8) to (2e-8,6.4e-8) export(2500) file "3Au-SiO2-SiNW_edge_zoom2.txt" format "#x #b #y #b #1"
Elevation(\Phi) From (0,5.7e-8) to (2e-8,5.7e-8) export(2500) file "3Au-SiO2-SiNW_edge_zoom3.txt" format "#x #b #y #b #1"
Elevation(\Phi) From (2e-9,0) to (2e-9,R1) export(2500) file "3Au-SiO2-SiNW_radial1.txt" format "#x #b #y #b #1"
Elevation(\Phi) From (1e-8,0) to (1e-8,R1) export(2500) file "3Au-SiO2-SiNW_radial2.txt" format "#x #b #y #b #1"
Elevation(\Phi) From (5e-8,0) to (5e-8,R1) export(2500) file "3Au-SiO2-SiNW_radial3.txt" format "#x #b #y #b #1"
Elevation(\Phi) From (1e-7,0) to (1e-7,R1) export(2500) file "3Au-SiO2-SiNW_radial4.txt" format "#x #b #y #b #1"
Elevation(\Phi) From (3e-7,0) to (3e-7,R1) export(2500) file "3Au-SiO2-SiNW_radial5.txt" format "#x #b #y #b #1"
Elevation(\Phi) From (4.5e-7,0) to (4.5e-7,R1) export(2500) file "3Au-SiO2-SiNW_radial6.txt" format "#x #b #y #b #1"

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Elevation(Phi) From (0,R1) to (0.684e-8,4.62e-8) export(2500) file "3Au-SiO2-SiNW_sheet charge_angle70.txt" format ":#x #b #y #b #1"
Elevation(Phi) From (0,R1) to (1.0e-8,4.77e-8) export(2500) file "3Au-SiO2-SiNW_sheet charge_angle60.txt" format ":#x #b #y #b #1"
Elevation(Phi) From (0,R1) to (1.29e-8,4.97e-8) export(2500) file "3Au-SiO2-SiNW_sheet charge_angle50.txt" format ":#x #b #y #b #1"
Elevation(Phi) From (0,R1) to (1.53e-8,5.21e-8) export(2500) file "3Au-SiO2-SiNW_sheet charge_angle40.txt" format ":#x #b #y #b #1"
Elevation(Phi) From (0,R1) to (1.88e-8,5.816e-8) export(2500) file "3Au-SiO2-SiNW_sheet charge_angle20.txt" format ":#x #b #y #b #1"
Elevation(Phi) From (0,R1) to (1.73e-8,5.5e-8) export(2500) file "3Au-SiO2-SiNW_sheet charge_angle30.txt" format ":#x #b #y #b #1"
END
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