Broadband Low Noise Frequency Synthesizers for Future Wireless Communication Systems

Dissertation

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By

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ABSTRACT

In this thesis the design of low phase noise frequency synthesizers for emerging wireless applications is investigated. The future wireless applications employ Orthogonal Frequency Division Multiplexing (OFDM) in order to combat the harsh mobile environment effects on the signal, such as Doppler effect or Multi-path fading. However, OFDM imposes the stringent integrated phase noise requirement to maintain the orthogonality of the subcarriers. The emerging applications also require broadband functionality to cover the multiple bands specified by different application using a single frequency synthesizer.

Particularly, this thesis focuses on the design of $\Sigma\Delta$ fractional-N frequency synthesizers for OFDM based applications. $\Sigma\Delta$ fractional-N PLLs have proven to be a very good candidate for the emerging OFDM-based radios which require employment of fast switching low phase noise frequency synthesizers. The issue of spectral Purity in $\Sigma\Delta$ PLLs is discussed, and the issue of phase noise and fractional spurs is investigated. Considering the loop dynamics, the optimal design for low phase noise is described. The problem of noise folding and its impact on spur cancellation is studied.

A type-I second order PLL is designed which inherently eliminates the sources of nonlinearity in the signal path. The LO generation scheme is proposed to cover the three
bands of WiMAX application centered at 2.5, 3.5 and 5.5 GHz by utilizing a broadband PLL. The design employs a uniformly sampled PFD and discrete on-chip filter. A cancellation DAC in embedded in the PFD which is used to cancel out the phase induced by quantization error. The design enhances the noise folding and spur performance and satisfies the stringent integrated phase noise requirement of the application.

As a critical part of the top-down design, a system study for a dual-band DVB-H tuner is presented. The tuner’s various requirements in terms of linearity, gain and noise are derived. The required of phase noise of the PLL is calculated on the basis of the blocker profile of the tuner. The direct conversion architecture is adopted for the design and the specification of various blocks in the radio is derived in order to satisfy the required performance. The LO generation scheme for dual band local oscillator is proposed.

Finally, the design of key circuits in the PLL loop is presented: The wideband VCO for triple WiMAX application is utilizing an amplitude regulation scheme to minimize supply pushing and improve the spectral purity. The high-speed multi-modulus divider design is presented. The design of high-speed broadband divide-by-32/33 dual modulus prescaler is described.
To my dear mom

To the memory of my father, Mohammad who inspired me to peruse my dreams, “who made me who I am, for better or worse”

To all who write, fight and die for the greatest wish

To all the wanderers who take the roads less explored

“All hope abandon ye who enter here”
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CHAPTER 1

INTRODUCTION

In the last two decades, the wireless market has seen tremendous growth. The 3G enabled devices are vastly used and 4G devices which enable all-the-time-connectivity and supporting different applications are gaining popularity. Consumers would like to have all-in-one device which allows them to connect to phone, data, internet and video streaming with a good quality and speed everywhere. The growing trend for portable consumer electronics devices along with the increasing demand for integrating different application on the handheld has led to evolution of the wireless standards which require higher data rates and wider bandwidths. Furthermore, the trend towards low power and small devices has been motivated by the demand for more battery life and lower cost. This has driven the push towards development of fully integrated solutions, system on chip (SOC).

Most of the future communication systems enabling high data rate communications and high spectral efficiency are based on Orthogonal Frequency Division Multiplexing (OFDM). OFDM is a multi-carrier modulation scheme that is
widely adopted in major emerging wireless applications due to its ability to combat impulsive channel noise and multipath fading effects while making better use of the system available bandwidth. It has been adopted for the European Digital Audio Broadcasting (DAB) [1] and Digital Video Terrestrial Broadcasting (DVB) [2] standards, and has been standardized for new wireless LAN generations [3]. More recently, Coded OFDM (COFDM) modulation is adopted for fixed wireless access (FWA) communication systems that can deliver point-to-multipoint wideband access with the IEEE 802.16a WiMAX standard [16].

Frequency synthesizers are fundamental building blocks in every wireless transceiver system. Future broadband wireless standards utilizing dense modulation schemes are presenting new challenges to today’s synthesizers in four areas:

1. The synthesizer should cover multi bands across a wide frequency range.
2. It should dynamically support variable channel bandwidths for link adaptation and variable data rate.
3. It should allow for wide range of OFDM sub-channel frequencies hence it must meet the stringent requirement of extremely low integrated phase noise over multiple frequency decades.
4. It should enable fast settling time between transmit and receive time slots.

To satisfy the above mentioned requirements, the new architectures and techniques have been introduced to overcome the various trade-off in the PLL loop. Fractional-N PLLs were introduced to achieve the fine resolution while having a wider bandwidth and faster settling time. However, fractional spurs due to periodical toggling of the division ratio show at the small frequency offset from the VCO oscillation frequency [4]. These
spurs are very high in energy and degrade the phase noise if they are not filtered properly. If the filtering is done solely by PLL dynamics, the bandwidth should be chosen very narrow in order to filter the spurs. As a result, traditional fractional-N PLL frequency synthesizers are limited to narrow loop-bandwidth, single standard radios where the channel spacing is fixed.

Fractional-N $\Sigma\Delta$ synthesizers are becoming increasingly attractive since they offer very fine frequency resolution, while achieving low phase noise. This is achieved by using a $\Sigma\Delta$ modulator which moves the in-band quantization noise generated by the divider to higher frequencies where they can be removed by the loop filter. The $\Sigma\Delta$ Fractional-N PLLs enhance the trade-off between bandwidth and resolution, but since they rely on the loop dynamics for spur reduction, loop bandwidth cannot be widened arbitrarily [5], [6].

At the same time the emerging wireless standards demand faster settling, higher spectral purity and wider bandwidth RF synthesizers. Recently, several techniques have been proposed to reduce or cancel in-band phase noise by utilizing deterministic quantization noise generated by the divider controller, enabling a wideband loop filter. The correction charge can be generated by a separate D/A converter [7][8], or by integrating the D/A converter into PFD itself [9][10]. These bandwidth extension techniques depend on precise matching of timing and loop parameters between calibration circuitry and the RF synthesizer core. Although analog techniques can be utilized to minimize these matching errors, short time-constants associated with wideband synthesizers make this approach difficult. Also due to the time-varying nonlinear nature of fractional-N synthesizers, out of band quantization noise and
spurious emissions can intermodulate and fold in-band, increasing \( \text{rms} \) phase error.

Furthermore, the noise of different elements in the PLL loop contributes to the total phase noise of the PLL through different dynamics dictated by the feedback loop. To achieve the very stringent phase noise required by the OFDM, not only the subblocks in the PLL should exhibit low noise, but also the choice of loop parameter should ensure the minimum integrated phase noise.

In this work, the design of PLL frequency synthesizer for the OFDM based applications is described and the challenges of different architectures are investigated. The design and implementation of a 5.7GHz type-I second order PLL for multi-band WiMAX application has been presented. A system study of a zero-IF dual band DVB-H tuner is described and the results are presented. At last, the design and implementation of key circuits in the PLL loop is presented.

The manuscript is organized as follows: An overview of the frequency synthesizers in the wireless receivers is presented in Chapter 2. The problem of phase noise and its impact on OFDM application is described. The PLL frequency synthesizers are introduced, and the PLL model is discussed. Different PLL architectures are presented and the challenges associated to each architecture are discussed.

In chapter 3, analysis of phase noise in PLL is presented. The linear AC model is discussed and various techniques and consideration for optimizing the integrated phase noise is given. Although the above mentioned method provides an insightful analysis, it doesn’t account for the quantization noise induced by \( \Sigma \Delta \) modulator. So, in the second part of the chapter, the problem of fractional spurs in \( \Sigma \Delta \) fractional-N architecture is presented and the existing methods for spur reduction are described. At last, the impact
of the non-linearity in the signal path and $\Sigma\Delta$ modulator noise folding on the total phase noise is investigated.

The design and implementation of a $\Sigma\Delta$ PLL for triple-band WiMAX application is presented in Chapter 4. The choice of architecture, type I PLL with discrete on chip loop filter, is discussed. The different blocks associated with the architecture, namely, two state PFD, single polarity charge pump and discrete loop filter are described. The loop parameter design, the physical implementation and the simulation results are presented. The design of the VCO and the divider for this PLL is presented in details in Chapter 6.

A system study for dual DVB-H tuner operating in UHF band and L band is given in Chapter 5. The DVB-H system requirements in terms of gain, linearity and noise are analyzed and specification for different blocks in the proposed zero-IF tuner is derived. The phase noise mask of the PLL is derived. To cover both band with a single PLL, a frequency plan has been proposed.

In Chapter 6, the design and implementation of key blocks in the PLL is presented. The implementation of wideband VCO and a Divider for the multi-band WiMAX PLL which is presented in chapter 4 is given. The performance results are presented. The issue of supply pushing and its effect on the phase noise of the VCO is described, and a novel amplitude regulated VCO is designed to minimize the impact. The implementation of wideband low power prescaler design for multi-band PLLs is described. Chapter 7 summarizes the achievement and gives future directions.
CHAPTER 2

PLL FREQUENCY SYNTHESIZERS IN THE RF TRANSCEIVERS

Frequency synthesizers are widely used in wireless transceivers as a local oscillator (LO) to provide precise and fine-tunable local oscillation frequencies for frequency translation; their maximum frequency of operation and spectral purity are often critical to the system performance. The modern synthesizer should achieve stringent performance requirement imposed by the emerging wireless radios. In particular they should cover multi bands across a wide frequency range. Besides, they should dynamically support variable channel bandwidths for link adaptation and variable data rate. Also, they should allow for wide range of OFDM sub-channel frequencies hence it must meet the stringent requirement of extremely low integrated phase noise over multiple frequency decades.

Zero-IF radio architecture has gained popularity because of its reduced complexity, lower cost, smaller form factor and lower power consumption. This architecture requires fewer external components and eliminates the need for image
suppression fliers. A typical Zero-IF or direct conversion receiver is shown in Figure 2.1. The received signal at the antenna is amplified by LNA. The amplified signal is mixed by the output of the LO and passes through a LPF, generating a signal at the frequency FRF-FLO. The signal passes from VGA and gets converted to digital through the ADC.

![Figure 2.1: Block diagram of a RF receiver](image)

### 2.1 Phase Noise

The commonly used phase noise phrase refers to rapid, short-term, random fluctuations in the phase of a wave caused by time-domain instabilities in an oscillator. The spectrum of the output of the ideal oscillator is an impulse, \( w_0 \), as it shown in Figure 2.2, meaning all the energy is at the center frequency. The time domain representation of the output is given by

\[
y(t) = A \cos(wt + \theta)
\]

(2.1)

In reality, all the oscillators have phase modulated components which spread the energy to the adjacent frequencies resulting in sidebands as shown in Figure 2.2. Equation 2.2 formulates the output of a practical LO where \( A(t) \) and \( \theta(t) \) represent amplitude and phase fluctuations respectively. The amplitude fluctuation is not of concern and can be removed by using a limiter.
There are two types of phase terms showing in Equation (2.2). The first term appears at distinct frequency offsets from center frequency which are referred to as spurious tones. The second term, phase noise, appears as random phase fluctuations, skirting around the center frequency. The spurious terms have deterministic character since they are generated due to noise of external elements, such as the noise on the control voltage, the quantization noise and the power supply. On the other hand, the phase noise is random and generated as a result of internal noise sources, such as active device noise, thermal noise and flicker noise. These two mechanisms are the major factors affecting the spectral purity of the LO.

The phase noise of an oscillator is typically quantified by the single-sideband (SSB) phase noise, which is defined as the ratio of noise power in a 1 Hz bandwidth at an offset, $f_m$, to the signal power.
2.2 Impact of phase noise in Wireless Radios

From system point of view, the phase noise of PLL contributes to the overall radio performance in two ways:

- Reciprocal mixing: Noise coming from different blocks in the PLL loop will change the amplitude and the frequency of the LO signal.

The random variation in frequency due to the noise makes the LO output to deviate from a pure sinusoidal wave [4]. Instead of a single tone, the spectrum of LO output signal will show a skirt of frequencies around the fundamental component. At the mixer, desired signal and all the blockers (interferers) are down converted by the LO and due to this extra tail, their spectrum will as illustrated in Figure 2.3. The overlap causes a part of blocker to mix with the signal and hence the signal is corrupted with phase noise of the LO. This effect is called “reciprocal mixing”. Equation (2.3) [4] specifies the phase noise at the offset frequency where each blocker is located. By knowing the maximum difference allowed between the power of each blocker CU and the desired signal CW and the required signal-to-noise ratio, the phase noise profile of the PLL would be determined.

![Figure 2.3: Reciprocal mixing resulting in frequency overlap between a blocker and desired signal.](image-url)
Residual FM (In-Band Phase Noise): Phase noise of the PLL also changes the phase of the carrier signal and cause phase error. The effect of in-band phase noise can be seen in the constellation diagram of the modulated signal. Figure 2.4 shows the constellation diagram of a QPSK system in the presence of the PLL phase noise. The deviation between the ideal vector and the real one on the constellation diagram can be modeled as a random signal with Gaussian distribution. The standard deviation of this random signal is equal to the RMS phase error of the PLL. If the RMS value of the phase error is large, it causes the signal to be detected erroneously and hence increases the BER. The phase noise specification would be tighter for higher order modulations (e.g. 16QAM, 64QAM,…) which have more compact constellation diagrams.

![Figure 2.4: Noise in PLL phase causes a blurred constellation diagram](image)

2.3 Effect of Phase Noise in OFDM Based Systems

In Orthogonal Frequency-Division Multiplexing (OFDM), a high speed data stream is split into several low speed streams, and closely spaced sub carriers are used to
Each sub-carrier is modulated using a conventional modulation scheme such as Binary Phase Shift Keying (BPSK) or Quadrature Amplitude Modulation (QAM). The frequency spacing of the sub-carriers is selected to be spectrally orthogonal, i.e. at the center frequency of a sub-carrier all other sub-carriers have a spectral null. Ideally each sub-carrier can then be demodulated without interference from other sub-carriers.

In general, OFDM systems are more sensitive to phase noise compared to single carrier systems. In a single carrier narrowband system, phase noise occupies a small part of the total bandwidth; while in OFDM each sub-carrier contributes its own phase noise to the overall modulated waveform. Figure 2.6 (a) shows ideal OFDM sub-carriers orthogonally spaced in the frequency domain, where the individual peaks of the sub-bands all line up with the zero crossings of the other sub-bands and therefore do not cause interference. The thermal and 1/f noise in the local oscillator (LO) circuit elements generate sideband phase noise that affects the OFDM signal during the modulation and demodulation process, as shown in Figure 2.5. Carrier phase noise impacts phase noise in two ways: Common Phase Error (CPE) and Inter-Carrier Interference (ICI). CPE is caused by self-mixing of each sub-carrier with the low frequency part of its own phase noise spectrum. The effect of CPE is that all sub-carriers are rotated by a common random phase angle. Since all carriers suffer the same CPE, it is possible to detect and correct it at baseband processing using special pilot sub-carriers.

The ICI is caused by mixing of phase noise sidebands of all neighboring sub-carriers with the desired sub-carrier. Both close-in and far-out phase noise of the LO signal contribute to ICI and this degrades the overall SNR. The SNR loss due to phase
Figure 2.5: Impact of phase noise on OFDM signal
(a) Ideal OFDM sub-carriers with orthogonal frequency spacing
(b) The effect of oscillator phase noise sidebands on the modulated sub-carrier

noise ICI is a function of the oscillator phase noise profile and sub-carrier spacing. For a fixed channel bandwidth, decreasing the sub-carrier spacing (or alternatively increasing the number of sub-carriers) will result in rapid loss of SNR.
### 2.4 System-Level Overview of PLL Frequency Synthesizers

In telecommunication application, the LOs are often implemented as PLLs. In brief the PLL feedback loop, forces the divided-down VCO output frequency to follow the reference frequency.

![Figure 2.6: A typical PLL architecture](image)

Figure 2.6 shows a typical architecture of PLL which consists of a VCO, a low pass filter, a phase/frequency detector (PFD), charge pump (CP) and a frequency divider. The PLL loop is a negative feedback loop with phases as input and output. The PFD compares the phases of $f_{ref}$ and $f_{out}$. The LPF controls the loop dynamics, such as settling time and transient response, the VCO generates the output frequency in accordance to the error. The divider in the feedback path divides the $F_{out}$ back to $F_{ref}$ such so.

$$F_{out} = F_{ref} \times N$$  \hspace{1cm} (2.4)

In order to obtain a range of frequencies in the output, the divider is designed to be programmable, so the desired frequency could be obtained with no need to change the reference frequency. This is an advantage, as cheap crystal oscillators could be used to generate the reference frequencies.
2.4.1 PLL Type and Order

According to [12], the PLL type indicates the number of integrators in the loop. The PLL order represents the number of poles in the open-loop transfer function.

- Type I: The oscillator can be viewed as a phase integrator, and since there is always at least one oscillator present in a PLL, the lowest PLL order is one.
- Type II: In a charge pump PLL, the loop filter capacitor integrates the output current from the charge-pump. Since there are two integrators in the loop, the PLL is categorized as Type-II.
- Third order type-II PLL: The most common type and order found in PLL frequency implementations targeting wireless applications is a charge-pump PLL using a second order PLL. When a second order loop filter is used in the PLL, the open-loop transfer function becomes three. The third order PLL also has the advantage of always being stable.
- PLL of higher order: To suppress noise and spurious tones, a loop filter of higher order may often be required. PLLs using more than two integrators are also used in special applications, but are not common in frequency synthesizers.

2.4.2 PLL Models

In this section, a typical CP-PLL with passive loop filter is overviewed using a linear model. A PLL is a simple negative feedback system which can generate multiplication of a reference signal. A PLL mathematical model for linear representation of the phase of a locked PLL is shown in Figure 2.7 (a) where
The term $G(s)$, the open loop transfer function can be written as [4]

$$G(s) = \frac{I_{sp}}{2\pi} F(s) \cdot \frac{2\pi K_{VCO}}{s} \quad (2.5)$$

where $\frac{I_{sp}}{2\pi}$ is the gain of PFD/CP, $2\pi K_{VCO}$ is the gain of the VCO, and $F(s)$ is the transfer function of the low pass filter. $H(s)$ represents the feedback transfer function and can be written as

$$H(s) = \frac{1}{N} \quad (2.6)$$

Figure 2.7: (a) PLL linear model (b) Second order passive loop filter
Figure 2.8 shows the corresponding open loop bode plot and pole-zero constellation for a PLL using a second order passive loop filter. The loop filter and the VCO form one pole each at the origin. The resistor together with the $C_z$ form a zero, improving the phase margin.

![Open-loop bode plot and corresponding poles and zeros](image)

The open loop has unity gain at frequency $\omega_c$, where

$$\omega_c = 2\pi BW$$  \hspace{1cm} (2.7)

The term $BW$ refers to as the loop bandwidth. The loop bandwidth is an important design parameter and is used to trade-off lock-time and phase noise. The $BW$ needs to be sufficiently low in order to allow stable PLL operation. The lower range of the bandwidth is determined by the specified settling time required by the application.

If the loop filter parameters are provided, the cross-over frequency can be expressed as [13].
\[
\omega_c = \frac{I_{cp} K_{VCO} R_z}{N} \cdot \frac{C_z}{C_z + C_p}
\]  

(2.8)

If the zero \( \omega_z = 1/T_z \) is chosen a factor \( \alpha \) below \( \omega_c \) and the third pole \( \omega_p = 1/T_p \) is chosen a factor \( \beta \) above \( \omega_c \), the phase margin for loop stability is guaranteed. The component values for loop filter is given below [9]

\[
R_z = \frac{N}{I_{cp} K_{VCO}} \cdot \omega_c
\]  

(2.9)

\[
C_z = \frac{I_{cp} K_{VCO}}{N} \cdot \frac{\alpha}{\omega_c^2}
\]  

(2.10)

\[
C_p = \frac{I_{cp} K_{VCO}}{N} \cdot \frac{1}{\beta \omega_c^2}
\]  

(2.11)

Analysis for higher order passive loop filter designs can be found in [13][14]

2.5 PLL Architectures

2.5.1 Integer-N PLLs

Figure 2.9 shows a typical block diagram of an Integer-N PLL as a feedback system. Integer PLL synthesizers generate an output signal whose frequency is a multiple of that of a reference signal \( F_{ref} \), typically generated by a crystal oscillator (XTAL). This is accomplished by a negative feedback loop where the error signal is obtained by a phase comparison between \( F_{ref} \) and the divided PLL output.
This comparison is achieved by a phase frequency detector (PFD) and usually employs a charge-pump. Its output is filtered by the loop filter (LF) and drives the control node of the voltage-controlled oscillator (VCO).

An integer synthesizer has certain intrinsic limitations. The main one is that the output frequency resolution is forced to be equal to an integer multiple of $F_{\text{ref}}$. In this case, if a fine output frequency resolution is needed, a correspondingly low $F_{\text{ref}}$ must be chosen. This forces the loop bandwidth to be very narrow since it must be much lower than $F_{\text{ref}}$ for loop stability reasons. The loop filter is therefore chosen to be one-tenth of $F_{\text{ref}}$. The immediate consequence of the loop bandwidth reduction is an increase in the PLL locking time and the channel switching time. Moreover, a low reference frequency requires a high feedback division ratio to synthesize the desired output frequency, thus causing a strong degradation of the output in-band phase noise.

### 2.5.2 Fractional-N PLL

Fractional-$N$ synthesis has been introduced to overcome the resolution-bandwidth trade-off [5]. Fractional-$N$ synthesis achieves fast locking, agile channel switching, potentially arbitrary output frequency resolution, and more freedom in the reference frequency choice. In order to achieve fine resolution frequency control, the divide value
is dithered between different integers using a multi-modulus divider. The division ratio is dynamically programmed by a control pattern with an average value that corresponds to the fractional division factor. Figure 2.11 depicts the fractional-N frequency synthesizer architecture.

Figure 2.10: Fractional-N PLL

Fractional-N synthesizers suffer from generation of fractional spurs associated with periodically toggling the loop division ratio. The fractional accumulator periodically generates the carry-outs that toggles the loop division ratio. It is expected to see spurious tones at multiples of carry-out frequency: \( F_{\text{ref}} \times \frac{K}{F} \), where \( K \) is the fractional value and \( F \) is the size of the accumulator. Fractional spur may be removed by using a higher order loop filter if the closest spur is outside the loop bandwidth. The spacing of the closest spur to fundamental is determined by the synthesizer’s step size. As a result, for a synthesizer with a fine frequency resolution, it is practically impossible to remove the fractional spur by loop filter. On the other hand, reduction of the loop bandwidth to filter the spur results in longer lock time and increased phase noise, thus losing the advantage of fractional-N PLLs.
2.5.3 ΣΔ Fractional-N PLLs

In order to decrease the periodic in-band noise a recent technique is introduced which utilizes a ΣΔ modulator and moves most of the quantization spurs energy to frequencies far away from the carrier, where it can be filtered out by the loop transfer function (shown in Figure 2.11). The modulator output generates the expected average division ratio while shaping the quantization noise to higher frequencies. The ΣΔ fractional-N frequency synthesis technique offers a good solution for LO generation. However, there are two main issues that should be considered carefully while designing the ΣΔ fractional-N PLL

![ΣΔ Fractional-N PLL](image)

Figure 2.11: ΣΔ Fractional-N PLL

First, the ΣΔ modulator imposes an upper limit on the loop bandwidth (depicted in Figure 2.12). This is because of the fact that the attenuation of the quantization noise magnitude appearing at the synthesizer output is achieved by the filtering action of the PLL dynamics on the noise. In other words, the loop bandwidth can be widened till the “shaped” quantization noise energy is attenuated sufficiently. Equation (2.5) specifies the upper limit of the PLL loop bandwidth imposed by ΣΔ modulator where $S_{ΣΔ}(f)$ represents the modulator output noise. $β$ is the relative position of two HF poles of PLL
loop relative to the cross over frequency $f_C$ and $n$ shows the order of the employed $\Sigma\Delta$ modulator[15].

$$f_{c,\text{max}} = \left[ S_{\Delta\Sigma}(f) \frac{12}{(2\pi)^{2n}} \frac{f_{\text{ref}}^{2n-1}}{\beta^4} \frac{f^{8-2n}}{2n} \right]^{1/2n} \quad (2.13)$$

![Figure 2.12: Bandwidth in $\Sigma\Delta$ Fractional-N PLL](image)

(a) Limitation due to the in-band quantization noise (b) Limitation due to the out-of-band quantization noise

Second, the critical PLL building blocks, i.e., those placed between the multi-modulus divider and the loop filter must exhibit a high degree of linearity. In fact, any nonlinearity seen by the modulated signal folds part of the high-frequency spurs energy close to the carrier. $\Sigma\Delta$ fractional-N PLLs overcome the trade-off between the reference frequency and the resolution, allowing arbitrary choice of reference frequency. This choice should enable the designer to choose a wider bandwidth. However, the induced quantization noise from the SD modulation increases, the phase noise, and should be filtered
CHAPTER 3

TECHNIQUES FOR LOW PHASE NOISE DESIGN OF WIDEBAND ΣΔ PLLS

Noise in synthesizers comes from all different circuits and components which form the PLL loop. As mentioned in Chapter 2, synthesizer noise performance is usually characterized in terms of phase noise, i.e. that the focus is on noise which causes fluctuation in the phase of the output. The fluctuation in the amplitude of the tone is usually neglected, since the synthesizer output typically has fixed, limited amplitude. In this chapter, the different sources and mechanisms contributing to noise are explored, and the techniques for phase noise reduction are discussed.

3.1 Various Noise Sources in PLL Synthesizers

All the blocks in the synthesizer contribute to overall noise in different ways, and the noise they produce has different characteristics. There are many sources of noise: The thermal energy in resistors causes more electron motion which generates noise in resistors. Noise in active devices can be thermal channel noise, 1/f noise, or shot noise.
Also noise may be coupled into the circuit under test through electromagnetic coupling from other circuits or external noise sources, such as cell phones and pagers. Furthermore, noise can be injected through the substrate due to a combination of capacitive and conductive coupling from other circuits on the same die, for example, other oscillators, power amplifiers, and digital circuits. [24]

### 3.1.1 PLL Noise Model

A linear domain phase model of PLL with additive noise sources is shown in Figure 3.1 where $\Phi_{\text{ref,n}}$ represents the noise in $\text{rad}/\sqrt{\text{Hz}}$ which appears at the reference input to the PFD. It includes the crystal oscillator, crystal buffer and reference divider noise. $\Phi_{\text{vco,n}}, \Phi_{\text{div,n}}$ and $\Phi_{\text{PFD,n}}$ all in $\text{rad}/\sqrt{\text{Hz}}$ are representing the noise due to VCO, divider and PFD respectively. $V_{\text{CNT,n}}$ is the noise at the VCO control voltage input due to the loop filter and the coupled noise sources to the control line in $V/\sqrt{\text{Hz}}$. $I_{\text{CP,n}}$ is the noise of the CP current in $A/\sqrt{\text{Hz}}$.

![Figure 3.1: PLL Noise Model](image-url)
3.1.2 In-Band and Out-of-Band Phase Noise in PLL

The noise transfer function for various noise sources in the loop is derived using the PLL linear model. There are two noise transfer functions: one from the VCO noise, and one for all other sources of noise in the loop. All noise generated by the PFD, charge pump, divider, and loop filter is referred back to the input, and the noise from VCO is referred to the output. The transfer function for in-band phase noise is given by

\[
\frac{\Phi_{\text{noise-out}}(s)}{\Phi_{\text{noise-in-band}}(s)} = \frac{F(s)K_{\text{VCO}}K_{\text{phase}}}{s + \frac{F(s)K_{\text{VCO}}K_{\text{phase}}}{N}} \tag{3.1}
\]

By substituting the models presented in chapter 2, and considering a second order filter, the transfer function becomes:

\[
\frac{\Phi_{\text{noise-out}}(s)}{\Phi_{\text{noise-in-band}}(s)} = \frac{IK_{\text{VCO}}K_{\text{phase}}}{2\pi C_1} \left(1 + \frac{RC_1 s}{1 + \frac{IK_{\text{VCO}}}{2\pi N R} + \frac{IK_{\text{VCO}}}{2\pi N C_1}}\right) \tag{3.2}
\]

This function represents a low-pass characteristics so for low frequencies (inside the loop bandwidth), the loop tracks the input phase which includes the phase noise. So within the loop bandwidth, the noise will be transferred to the output. Outside the loop bandwidth of the PLL, this noise suppressed. The transfer function for the noise due to the VCO is presented as follows:

\[
\frac{\Phi_{\text{noise-out}}(s)}{\Phi_{\text{VCO}}(s)} = \frac{s}{s + \frac{F(s)K_{\text{VCO}}K_{\text{phase}}}{N}} \tag{3.3}
\]

Using the models in section 2.4.2, the transfer function can be represented as (3.4) which acts as a high pass filter. Thus, at low offsets of frequency the VCO noise is suppressed.
by the loop; however, outside the loop bandwidth the VCO is essentially free running; thus the PLL noise approaches the VCO noise.

\[
\frac{\Phi_{\text{noise-out}}(s)}{\Phi_{\text{noise-in-band}}(s)} = \frac{s^2}{s^2 + \frac{IK_{VCO}V_C}{2\pi N}} R_S + \frac{IK_{VCO}V_C}{2\pi N C}
\]  

(3.4)

\[
\Phi_{\text{out}}^2 = \left(\frac{\Phi_{\text{noise-out}}(s)}{\Phi_{\text{noise-in-band}}(s)}\right)^2 \left[\Phi_{\text{ref,n}}^2 + \Phi_{\text{pfd,n}}^2 + \Phi_{\text{div,n}}^2 + (I_{cp,n} \cdot \frac{2\pi}{I_{cp}})^2 \right] + \left[\Phi_{VCO,n}^2 + (V_{cn,n} \cdot \frac{2\pi K_{VCO}}{s})^2 \right]
\]

(3.5)

The total noise exhibited by the PLL can be predicted using the linear model shown in Figure 3.1. The first step is to determine various model parameters, including the level of noise sources for each block, which generally involves either direct measurement, or simulating the various blocks with an RF simulator, such as SpecreRF. Assuming the noise sources are completely uncorrelated, one can calculate the PLL noise using equation 3.5. Figure 3.2 depicts the typical PLL phase noise profile when the bandwidth is set to be around 500KHz. As it is seen the PLL noise follows the detector/Xtal/divider noise when in band and follows the noise of the VCO when out of band. The alternative is to build Verilog-A models to determine the result. This approach employs noisy phase domain models for each block. These models are described in details in [58].

3.1.3 Design for Low Phase Noise

Equations (3.3) and (3.4) provide a useful insight into optimization of the phase noise of the PLL. In order to minimize the close-in phase noise (noise inside the loop...
bandwidth of the PLL) the divider, CP and PFD noises should be reduced. Also the divide ratio, N, should be reduced. This choice of this value depends on the frequency synthesizer architecture.

In integer-N architecture, this value is limited by the output frequency resolution. Namely, a fine frequency resolution leads to very large value of N in multi-GHz PLLs, which contributes significantly to the close-in phase noise. This is one of the major reasons for using Fractional-N PLLs. Furthermore, if the close-in phase noise is dominated by CP noise, increasing the $I_{CP}$ while keeping the CO noise the same level, leads to reduction of the close-in phase noise. As for the phase noise outside the loop bandwidth of the PLL, the VCO noise, and the noise on the control line should be minimized. Also VCO gain, $K_{VCO}$ should be kept small.
3.1.4 PLL Bandwidth for Optimal Phase Noise

Since noise sources within the PLL are shaped by the loop filter, the phase noise performance of the complete PLL can be optimized by tuning the loop filter parameters. The sum of the PFD, charge-pump and the divider generate a noise floor within the PLL bandwidth $\omega_1$ that is relatively flat, and drops outside the PLL bandwidth, as shown in Figure 3.3 (a). On the other hand, transfer function of the VCO has opposite behavior. Outside the PLL bandwidth the VCO noise transfer function equals to 1, meaning that the PLL output equals the VCO noise, as illustrated in Figure 3.3 (b).

The optimal loop filter bandwidth $\omega_{opt}$ is approximately where the in-band noise equals the VCO noise. If the loop filter is too narrow, the VCO noise will not be suppressed by the PLL, resulting in higher in-band phase noise. Accordingly, widening the loop filter leads to insufficient suppression of the charge-pump, PFD, divider noise and the quantization noise of $\Sigma\Delta$ modulator.

As illustrated in Figure 3.3 (a) , at the PLL bandwidth $\omega_1$ the noise transfer
function exhibits an overshoot due to finite phase margin of the PLL feedback, resulting in increased noise around $\omega_1$ or both VCO and other sources. In application where there is a requirement to keep PLL noise lower than a certain level around $\omega_1$, it may be desirable to select a smaller bandwidth which results in increased in-band phase noise, but the noise transfer function will not exhibit the overshoot. Also the overshoot can be reduced by increasing the phase margin.

3.1.5 Optimal Integrated Phase Noise

As stated in Chapter 2, the OFDM applications are susceptible to integrated phase noise, thus the choice of different parameters to achieve the desired integrated phase noise is important. For the purpose of analysis in this section, the phase noise of the PLL is approximated by Laurentain function as follows:

$$L(\Delta\omega) = \frac{L_0 \omega_1^2}{\Delta\omega^2 + \omega_1^2}$$

where $L_0$ and $\omega_1$ represent the in-and noise floor and the loop bandwidth respectively. One can realize the integrated phase noise by integrating (3.6) between two frequencies $\omega_a$ and $\omega_b$.

$$L_{int} = \int L(\Delta\omega)d\omega = L_0 \omega_1 (\arctan\left(\frac{\omega_b}{\omega_1}\right) - \arctan\left(\frac{\omega_a}{\omega_1}\right))$$

Equation (3.7) gives an insight to the trade off between VCO noise and in-band noise sources to meet a specified integrated phase noise requirement. By rearranging the equation and setting $L_{int}$ to the desired value, the required in-band noise can be determined as a function of bandwidth. The lock time of the PLL is also taken into account.
account while choosing the loop bandwidth since the lock time and the bandwidth are inversely proportional to each other.

Given a specific bandwidth and by using equation (3.6), the close-in noise and required VCO noise at the specified offset are calculated. It should be noted that this equation slightly underestimates the integrated phase noise, since the overshoot around the loop-filter bandwidth is neglected. The PLL close-in phase noise is related to the feedback divide ratio, N and the reference frequency values by [12]

\[
L_0 = L_{\text{ref}} + 20\log(N) + 10\log(f_{\text{ref}})
\]

Figure 3.4: Required close-in and VCO noise to achieve required integrated phase noise

Figure 3.4 represents the required VCO phase noise a 1 MHz offset and close-in noise versus the loop bandwidth. These parameters are chosen in order to achieve
WiMAX requirement, a total integrated phase noise of -41 dBc/Hz integrated in the interval of 1 KHz to 10MHz. It can be seen that for the loop bandwidth of 1MHz, the close-in noise should be kept around -105 dBc/Hz, while VCO phase noise at 1 MHz offset is specified as -109 dBc/Hz.

3.2 Fractional Spurs

The algorithms used to generate the division control pattern in fractional-N PLL are generally characterized by an intrinsic periodicity. This causes the generation of spurious signals around the carrier, called fractional spur. In fact, after each change in the division ratio, the phase coherence between the divider output and the reference is lost, and consequently the PFD charge-pump injects current pulses into the loop filter. A low-pass filtered version of these pulses appears on the VCO control node and is eventually up-converted by the VCO itself. Unlike an integer synthesizer, in a fractional synthesizer a classical lock condition, characterized by permanent phase coherence between input and output signals, is never reached. Only a dynamic lock can be achieved, and this is characterized by the PFD/charge-pump injecting current pulses according to the to the periodical divider control pattern.

3.2.1 Spur Reduction Techniques

In early fractional-N PLLs, the problem of suppressing the fractional spur that would otherwise result from the dithering action has been addressed using a DAC cancellation path as shown in Figure 3.6 [10]. Because the dithering pattern is generated digitally, it can be calculated by digital circuitry, converted by a DAC to an analog current, and added to the output of the charge pump. If the DAC has sufficient precision
and the correct gain, the added signal nearly cancels the component of the charge-pump corresponding to fractional spurs. Fractional spurs tend to have a high dynamic range and significant spectral power within the PLL bandwidth; therefore, excellent cancellation accuracy is required. If spurious content is only partially cancelled because of gain errors, distortion, or insufficient dynamic range in the DAC cancellation path, the remaining portion contains in-band noise and spurious tones, which contribute significantly to phase noise [8]. Consequently, the approach has been used mainly in high-accuracy, high-cost applications such as test and measurement equipments wherein component trimming and calibration are practical.

A recent technique that circumvents the DAC precision and gain matching problems uses a modulator to move most of the quantization spurs energy at frequencies far away from the carrier, where it can be filtered out by the loop transfer function, as shown in Figure 3.6. The modulator output generates the expected average division ratio

![Figure 3.5: Fractional spur cancellation using a DAC](image-url)
while shaping the quantization noise to higher frequencies.

In a typical realization, two main problems arise: first, to sufficiently filter out the quantization spurs, the loop bandwidth cannot be too wide, thus partially losing the main advantage of fractional architecture. Second, the linearity required for the critical PLL building blocks, i.e., those placed between the multi-modulus divider and the loop filter, must be much higher than in an integer synthesizer. In fact, any nonlinearity seen by the modulated signal folds part of the high-frequency spurs energy close to the carrier.

A recent approach to reduce the noise-versus-bandwidth trade-off that exists in conventional $\Sigma\Delta$ fractional-N synthesizers uses a DAC to cancel the error signal [8], as shown in Figure 3.7. This method builds on the idea behind the traditional DAC cancellation technique but utilizes signal processing techniques to reduce the impact of DAC nonlinearity. The main limitations with this architecture still center achieving good matching between the DAC output and phase-error signal, which is difficult because the
two are processed by separate circuits whose outputs are summed. Also, a high-resolution DAC is required to achieve the desired performance. In [8] a 4-bit coarse DAC and 4-bit fine DAC were used, resulting in 16-dB improvement in broad-band phase noise and suppressing fractional spur levels to 60-dBC levels. The proposed approach achieved 430 kHz bandwidth.

An alternative approach that utilizes a DAC to reduce quantization-induced phase noise is proposed in [9][10] as shown in Figure 3.8. The separate phase detector and DAC circuit elements are replaced by a hybrid structure. By embedding the two functions into one circuit, an intrinsically better gain match between the phase-error and DAC cancellation signals is obtained. The proposed architecture incorporates several digital signal processing techniques to reduce the impact of nonlinearities that occur in the PFD/DAC, such as unit element mismatch, timing mismatch, and any residual gain mismatch occurring between the PFD/DAC output and phase-error signal.

![Figure 3.7: PFD/DAC hybrid structure](image-url)

An alternative approach that utilizes a DAC to reduce quantization-induced phase noise is proposed in [9][10] as shown in Figure 3.8. The separate phase detector and DAC circuit elements are replaced by a hybrid structure. By embedding the two functions into one circuit, an intrinsically better gain match between the phase-error and DAC cancellation signals is obtained. The proposed architecture incorporates several digital signal processing techniques to reduce the impact of nonlinearities that occur in the PFD/DAC, such as unit element mismatch, timing mismatch, and any residual gain mismatch occurring between the PFD/DAC output and phase-error signal.
3.2.2 Impact of Loop Nonlinearities on Phase Noise

Nonlinearities in PLL building blocks, mainly due to charge pump PFD I/O characteristics result in a significant increase in phase noise floor. This increase is usually due to down-conversion of high frequency tones and folding of shaped quantization noise in the $\Sigma\Delta$ modulator output spectrum [4][15][16][7].

Major error sources in a PFD can be listed as dead-zone, leakage current in the charge pump; mismatch between up and down charge pump current sources and switching transient mismatch in charge pump circuits. In [22] a fast transient response PFD is utilized to minimize the dead-zone. The charge pump PFD I/O characteristic corresponding to small phase errors at its input is the most nonlinear portion of its transfer function. This nonlinearity can increase in-band phase noise even after linearization techniques are employed [21]. A typical tristate PFD and charge pump circuit is shown in Figure 3.8.

Critical signals and associated timing in a charge pump PFD with moderate phase error between the reference edge and divided VCO edge is shown in Figure 3.9. $I_{up}$ and $I_{dn}$ represent charge pump currents with different settling behaviour and mismatched DC levels. Time delay, $\tau_d$ represents the digital delay in the reset path of the PFD to alleviate the dead-zone problem, $\tau_{r,up}$ and $\tau_{f,up}$ are the rise and fall time constants of the current source in the charge pump, $\tau_{r,dn}$ and $\tau_{f,dn}$ are the rise and fall time constants of the current sink. $T_{\text{ref}}$ represents the period of the reference signal and $\delta$ is the time-equivalent of the phase-error between reference and divider output signals in the PFD input. Residual correction charge after a phase error correction cycle is represented by $\int(I_{up} - I_{dn})$. As shown in Figure 3.9, with the phase error approaching zero, the contribution of error
sources to PFD nonlinearity increases dramatically. Around 0° phase error, the non-idealities discussed earlier would start impacting the spectral response of the fractional-\( N \) synthesizer, and a piece-wise linear transfer function assumption for a PFD will lead to incorrect modeling of the loop response.

![Figure 3.8: Typical tristate charge-pump PFD and loop filter](image)

Another source of nonlinearity in a synthesizer is the loop divider. The delay through the loop divider can be modulated by the divider control code generated by the digital \( \Sigma\Delta \) modulator. This signal dependent delay may introduce folding of high frequency quantization noise, increasing in-band phase noise and spurious content at the synthesizer output.

Finally, there is an inherent nonlinearity associated with fractional-\( N \) synthesizers due to non-uniform sampling of phase errors between the reference and the divider output. The PFD generates phase-error information in a time-varying manner. Depending on the reference and divider PFD outputs, a correction pulse is generated
either earlier than, or following, a reference clock edge. The pulse width indicates the sign and magnitude of the phase error, and the pulse position indicates when this phase error occurs within a period. Due to modulation of feedback divider in $\Sigma\Delta$ fractional-\(N\) frequency synthesizers, permanent phase coherence between input and output is never reached.

![Diagram](image)

Figure 3.9: PFD/CP associated signals
(a) for moderate phase errors at the PFD input (b) for phase error close to zero
CHAPTER 4

CASE STUDY 1: PLL FOR MULTI-BAND WIMAX APPLICATION

In this chapter, the design and implementation of a SD PLL for triple band WiMAX application is presented. As stated in Chapter 3, the nonlinearities in the signal path such as dead zone and CP current mismatch degrade the in-band phase noise dramatically by folding the quantization noise into the PLL band. To overcome this, the type-I PLL with discrete loop filter is chosen which doesn’t suffer from these drawbacks.

First, WiMAX system specification is overviewed, and the challenges associated with the PLL for WiMAX application is described. Next, a frequency planning for the frequency synthesizer in a zero-IF receiver for triple band WiMAX application is presented. The proposed architecture and its advantages and drawbacks are discussed. In the following section, different blocks in the PLL are described in details. The implementation of PLL is presented and the simulated performance is given. It should be noted that the implementation of key blocks of this PLL is presented in detail in Chapter 6.
4.1 WiMAX System Specification

WiMAX (Worldwide Interoperability Microwave Access), the new revolution in wireless broadband, fills the gap between very high data rate of WLAN (Wireless Local Area Networks) and high mobility of cellular systems. WiMAX standardizes the wireless broadband connectivity and provides a wireless alternative to DSL (Digital Subscriber Line) and cable [16]. IEEE 802.16e can reach further range than WLAN and provides point to multipoint wireless access in MAN systems. In order to exploit highest available data rate based on link quality, WiMAX adaptively supports several modulation schemes QPSK, 16QAM and 64QAM. Also the channel bandwidth in WiMAX system dynamically changes. Table 4.1 lists the available channel bandwidths varying from 1.25MHz to 20MHz. The 40 MHz bandwidth is proposed for MIMO operation. The OFDM sub-channel bandwidth is fixed at 10 KHz and the number of pilots is varying depending on the bandwidth used. The proposed integrated phase noise for WiMAX PLL is -40dBC which is integrated from 1/10 of the first OFDM sub-channel bandwidth (1/10×10 KHz) to half of channel bandwidth.

<table>
<thead>
<tr>
<th>Standard WiMAX:</th>
<th>RX Frequency Range (MHz)</th>
<th>TX Frequency Range (MHz)</th>
<th>BW (MHz)</th>
<th>Modulation Scheme</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.5 GHz</td>
<td>2300-2700</td>
<td>2300-2700</td>
<td>1.25, 1.75, 2.5, 3.5, 5, 7, 10, 14, 20, 40</td>
<td>OFDM with QPSK, 16 QAM, 64 QAM</td>
</tr>
<tr>
<td>3.5 GHz</td>
<td>3300-3900</td>
<td>3300-3900</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5.5 GHz</td>
<td>5150-5850</td>
<td>5150-5850</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 4.1: WiMAX system specification
4.2 Frequency Planning

To accommodate different frequency bands the PLL may require employing multiple VCO cores in different center frequencies. This would cause an increase in cost and die area of the PLL. To resolve the mentioned problem, a frequency planning scheme using a single broadband VCO is adopted.

Figure 4.2 shows the simplified block diagram for the proposed LO generation for Zero-IF architecture, covering the all three bands: 2.5GHz , 3.5 GHz and 5.5 GHz. The VCO is centered at 5.7GHz with a tuning range of ±10%. The upper frequency band at 5.7GHz band is generated directly by the PLL.

The lowest band at 2.5GHz is generated by a divide-by-two circuit which divides the output frequency in half. The VCO output is divided by 3 to generate a 1.8 GHz band. Having this frequency and VCO output in hand, a mixing stage could be used to generate the 3.5 GHz band. One multiplexer stage is used at the output of the synthesizer to select the desired frequency based on the control word.
4.3 PLL Architecture

The stringent noise specifications of high-quality wideband wireless standards demand fast settling, high spectral purity, and wideband RF synthesizers. As mentioned in chapter 3, in a typical \( \Sigma \Delta \) fractional-\( N \) frequency synthesizer, the quantization noise generated by the divider controller is filtered by the loop filter; therefore, loop bandwidth cannot be widened arbitrarily. Deterministic quantization noise generated by the divider controller can be utilized to cancel in-band noise, enabling a wideband loop filter. The correction charge can be generated by a separate D/A converter [7], [8] or by integrating the D/A converter into PFD itself [9], [10]. These bandwidth extension techniques depend on precise matching of timing and loop parameters between calibration circuitry and the RF synthesizer core. Although analog techniques can be utilized to minimize these matching errors, short time-constants associated with wideband synthesizers make this approach difficult.

By using the nonlinear closed loop approach introduce [17], it can be shown that the dead-zone and time variant nonlinear behavior of the PFD along with transient and static mismatches in charge-pump are the main sources of close-in phase noise enhancement in \( \Sigma \Delta \) fractional-\( N \) frequency synthesizers.

Figure 4.2 shows the simulation result for a 3\textsuperscript{rd} order Butterworth loop filter, which is controlled by a MASH 111 \( \Sigma \Delta \) modulator. The reference frequency is 26 MHz, and the closed-loop bandwidth is equal to 1-MHz. The output frequency is set to 1.976 GHz. As shown in the picture, a 2\% \( T_{\text{ref}} \) dead-zone plus a 2\% dynamic mismatch in the charge-pump circuit along with a 3\% static mismatch in the charge-pump current
sources result in almost 20 dB in-band phase noise enhancement, which is not predictable by linearized models. Considering the aforementioned facts it is very critical to have a linear charge-pump PFD.

4.3.1 Type-I PLL vs Charge-Pump PLL

One way to get around the problem of noise folding in ΣΔ fractional-\(N\) synthesizers is to use a PLL loop architecture, which is immune to the circuit level nonlinearities. Type-I PLL with the double-state single polarity charge-pump PFD structure is one of the best candidates regarding the close-in phase noise enhancement and spurious emission in ΣΔ fractional-\(N\) frequency synthesizers. There exists inherent nonlinearity associated with conventional type-II charge pump PLL ΣΔ fractional-\(N\)

![Figure 4.2: Impact of the non-idealities on close-in phase noise](image_url)
loops due to non-uniform sampling of the phase errors between the reference and the divider output [8]. The tristate PFD generates phase-error information in a time-varying manner. Depending on the reference and divider PFD outputs, a correction pulse is generated either earlier than or following a reference clock edge. Due to the modulation of the feedback divider in $\Sigma\Delta$ fractional-$N$ frequency synthesizers, permanent phase coherence between input and output is never reached. Inherent nonuniform sampling operation at the PFD results in a considerable quantization noise folding. It can be proven that due to the in-band noise folding it is almost impossible to get a 3$^{rd}$ order in-band quantization noise rejection. The type I double-state single polarity PFD can avoid the aforementioned nonlinearity. Because the correction pulse in the double-state PFD is only generated following the reference clock edge, the PFD output is always synchronized with the rising edge of the reference signal.

Figure 4.3 shows the designed PLL frequency synthesizer. A low-power, digital process compatible current mode PFD along with a discrete time on-chip LPF is designed to convert the phase error information at the output of the PFD to a proportional voltage domain signal in order to modulate the control node of the VCO. Instead of using the conventional charge-pump block a current source is used to charge up a capacitor. Deterministic residual error from the 2$^{nd}$ order digital noise shaper is utilized to discharge the capacitor using a current steering DAC in order to remove the quantization induced phase noise from the VCO control line. A continuous-time RC filter can be added after the discrete-time loop filter to improve phase noise and spur performance, even though it’s not a necessary component for closed loop system stabilization.
4.4 Two-state PFD

The block diagram of the double-state single polarity PFD is shown in Figure 4.5. The two state PFD consists of only two simple logic gates, NOR and NOT. If the reference signal leads the divided VCO signal, $div$, it generates a pulse to drive the charge pump. Otherwise no output pulse is produced. Figure 4.5 shows the timing diagram of the PFD. A delay equal to $3\sigma$ deviation of $\Sigma\Delta$ output pattern is inserted between the divider output and PFD input to cover the possible negative phase errors due to the $\Sigma\Delta$ dithering pattern. Compared to the conventional tristate PFD, the differences are as follows: the gain of the two-state PFD is zero for negative input phase error and is nonzero for a positive input phase error.
The two-state phase frequency detector would drive a single polarity signal generation block to convert the phase error to a proportional voltage/current signal. A single-polarity signal generation block generates the pump ‘up’ pulse only. In contrast, the charge pump of a conventional type II charge pump PLL generates both the pump-up pulse and pump-down pulse since it is driven by a tristate PFD. One advantage of the two-state PFD single polarity charge pump combination is that the charge pump static and dynamic mismatch problems associated with the conventional architecture are eliminated.

Figure 4.4: Double state single polarity PFD

Figure 4.5: Timing diagram of the double-state single polarity PFD

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4.5 Discrete Switched Cap Loop Filter

A low-power, digital process compatible voltage mode PFD along with a discrete time on-chip LPF is designed to convert the phase error information at the output of the PFD to a proportional voltage domain signal in order to modulate the control node of the VCO. Figure 4.7 shows the first order current-source based integrator and the discrete time SC LPF. If the reference signal leads the divided VCO signal (div), two-state PFD generates a pulse to drive the lossy integrator. Otherwise, no output pulse is produced. As shown in Figure 4.7, a charge-up current is integrated on an integrator.

Deterministic residual control word from the digital noise shaper is utilized to discharge the capacitor using a current steering DAC to remove the quantization induced phase noise from the VCO control line.

The $V_{CS}$ is then sampled at the falling edge of the reference signal. Two additional out of band poles are utilized to place greater attenuation on the quantization noise and to reduce the reference feed-through. The output voltage then drives the VCO control

![Figure 4.6: The discrete switched-cap filter](image-url)
node. After sampling action, the sampling capacitor, $C_S$, is reset to the ground to avoid the integration pole. Using the discrete time sampling filter, the control voltage node of the VCO is isolated from deterministic voltage fluctuations resulting from the quantization noise suppression. Critical voltage waveforms for this operation are shown in Figure 4.7.

It is assumed that the VCO is running at 5.5 GHz and the reference signal is 50 MHz. This leaves a division ratio of 110. Phase error at the PFD output charges up $C_S$ through the current source. Charge up duration is a function of the quantization error, which is called a correction cycle in Figure 4.5.

After 30 VCO cycles the compensation path kicks in to discharge the quantization related charge error. The compensation duration is fixed to 10 VCO clock cycles, and the discharge resistor value is varied based on the deterministic quantization error.

After complete removal of the error, the charge stored in $C_S$ is shared with the charge of the holding capacitor; $C_H$. Sampling is synchronized with the ‘clean’ falling edge of the reference signal. After 80 VCO cycles it is reset to ground using the fixed reset pulse.
4.6 PLL Loop Design

Using charge conservation law, the z-domain transfer function of the discrete time LPF composed of the $C_S$, $C_{H}$ and sampling switch can be expressed as follows:

$$H(z) = \frac{V_{C_{H}}}{V_{C_S}}(z) = \frac{z^{-1/2}}{1 + \frac{C_{H}}{C_S} - z^{-1} \frac{C_{H}}{C_S}}$$

(4.1)

After substituting the $z = e^{j\omega T}$ where $T=1/F_S$ the frequency domain transfer function is found to be
\[
\frac{V_{CH}(f)}{V_{CS}} = \frac{1}{\cos \frac{\pi f}{F_S} + j(1+2\alpha)\sin \frac{\pi f}{F_S}}
\]

(4.2)

where \( \alpha = C_H/C_S \) sets the location of the dominant pole using the following equation:

\[
\omega_c = F_S \times \frac{C_S}{C_H + \frac{C_S}{2}}
\]

(4.3)

Figure 4.9 shows the transfer function of the SC filter where \( \alpha \) is set to 2.5, assuming the sampling frequency of 50-MHz the dominant pole is located at 5.4 MHz.

Considering the block diagram in Figure 2.7 (a) for the proposed PLL loop, the open loop transfer function of the PLL can be written as:

\[
G(s) = \frac{K_{PD} H(z) \cdot 2\pi K_{VCO}}{s}
\]

(4.4)

The following equation represents a one-to-one mapping between the closed-loop transfer function of the PLL, \( A(s) \), and the open-loop transfer function

\[
A(s) = \frac{G(s)}{1 + G(s)}
\]

(4.5)

Using (4.4) and (4.5) the frequency domain closed-loop transfer function of the PLL is formulated as

\[
A(f) = \frac{K_{PD} K_{VCO}}{K_{PD} K_{VCO} - N(1+2\alpha)} \left( \frac{\pi f}{F_S} \right) + j Nf \cos \frac{\pi f}{F_S}
\]

(4.6)
Figure 4.8: Transfer function of the discrete time LPF

Figure 4.9: Closed loop response of the proposed PLL

Figure 4.9 depicts the closed-loop transfer function of the 2\textsuperscript{nd} order type-I PLL designed for an output frequency of 5.5 GHz with a reference frequency of 50 MHz and a loop bandwidth of 4 MHz. The open loop gain is equal to 1.777×10\textsuperscript{7} with a VCO gain of 40-MHz/V, a divide ratio of 140, and a PFD gain equal to 48.
4.7 Cancellation DAC

Figure 4.10 shows the implementation of an 8-bit segmented current steering DAC. The first $\Sigma\Delta$ modulator in the figure is used to dither the multi modulus divider. The quantization noise generated by the modulator is re-quantized to 8-bit through a second modulator. 8-bit thermometer data lines drive bank of LSB and MSB current sources to interpolate the quantization noise. Figure 4.11 presents a close up of the critical voltage signals associated with the correction cycle and compensation process. Ideally, to have a complete compensation $V_b$ should be equal to $V_{nom}$. The deterministic quantization noise we can easily predict the required current steering DAC to completely remove the quantization induced phase noise.

Figure 4.10: 8-bit implementation of segmented resistive discharge path
4.8 PLL Performance

The proposed PLL was designed and implemented in TSMC0.18mm technology 1.8V/6 metal 1 poly and was analyzed using SpectreRF from Cadence Design Systems as shown in Figure 4.12. The PLL is designed to operate at 5.7 GHz. The reference frequency is chosen to be 40MHz. The required currents for various blocks are supplied through an on-chip P-MOS LDO. Four separate set of supply lines were specified to supply VDD and ground lines for VCO, divider, the analog circuits and the digital circuitry. As a result, the disturbances on discrete two-state PD and the digital circuitry show reduced impact on the noise of the VCO and the divider. A 2-bit 2nd order error-feedback (EFB)ΣΔ modulator output capable of generating -2, -1, 0 and integers is used to dither the divider values.
Figure 4.13 (a) represents the typical waveforms of the designed PLL from start up to lock. It can be seen the PFD output pulses shrink as PLL gets to a lock state. The 2-state PFD only generate pulses when the reference signal leads the divider. Figure 4.13 (b) shows the control voltage supplied to the VCO. It is seen that PLL reaches the lock time in about 400ns.

Figure 4.12: PLL layout
Figure 4.13: The typical waveform of the PLL
(a) PFD (b) Control voltage
The phase noise of the PLL is shown in Figure 4.14. The noise of different blocks was extracted by SpectreRF, and their effect has been calculated using the linear AC model. The quantization noise effect has been accounted for by using the non-linear time domain model presented in [17].

Figure 4.14: Phase noise of the PLL
CHAPTER 5

SYSTEM STUDY AND DESIGN FOR A MULTI-BAND DVB-H TUNER

With ever-increasing demands for mobile TV application in multi-function mobile entertainment platforms, the mobile Digital TV standards (DTV) have gained popularity in recent years. Among these standards, Digital Video Broadcasting for Handheld, DVB-H, has been considered the dominant, due to its full compatibility with DVB-T network and system to make use of DVB-T facilities which have been available for several years.

The emerging service enables reception of the video streaming on handheld mobile device, allowing the real time digital television to be watched in mobile handsets. The tuner in such a device receives the broadband DTV channels and converts the desired TV channel to baseband with enough quality for future signal processing (demodulation and decoding) and display of the image on the LCD panel. In this chapter a system design analysis for the integrated DVB-H tuner is presented.

5.1 DVB-H System and the Tuner

The DVB-H standard is an extension of DVB-T and uses the same infra-structure to broadcast digital terrestrial TV signals to the mobile screen [18]. The broadcasting
frequencies for Europe are in UHF( IV/V) band: 470-890 MHz. The upper portion of this band is excluded when in a convergence terminal with GSM900. In the US the 1670-1675 MHz band has been allocated to DVB-H application. Since the DVB-H receiver is used in a battery operated mobile device, the size and power consumption are major factors in the design. To reduce power consumption, DVB-H enables DVB-T reception in a time-slicing mode by a 1:10 on/off ratio which means that the data is transmitted in the burst mode and receiver only needs to be turned on during the burst reception time. Also it utilizes additional error coding for more robust Doppler performance which is required for mobile operation. It should be noted that this modifications do take place in link layer and do not affect the physical layer. As a result, the DVB-T broadcasting stations require only a software upgrade for DVB-H channels [19].

The DVB-H data is transmitted using OFDM modulation scheme for each carrier, the constellation scheme could be QPSK, 16QAM or 64QAM depending on service requirement. The transmitted channel bandwidth is variable from 6 MHZ to 8 MHZ. (fig) shows a simplified model of the tuner. The incoming data is amplified while the unwanted signal is attenuated by the first RF LNA, and mixed down to baseband (or an intermediate frequency). The gain is adjusted by the baseband variable gain amplifiers (VGA) based on the input power level, so that the power at the output of the tuner remains constant.

Figure 5.1 shows the spectrum for multi-band DVB-H receiver. In the UHF band, the undesired DVB-T and analog TV channels along with the desired DVB-H channels are present. Due to integration in cellular device, in addition to these in-band interferers, the uplink and down link signals of GSM or WCDMA present the strong out-of-band
5.1.1 C/N, Minimum Signal Level and Noise Requirements

Based on the required performance namely, BER at the output of the modulator, the minimum signal to noise ratio (C/N) for the tuner can be derived for each given constellation scheme. (table) lists the C/N ratios for the Gaussian channel. The maximum C/N required is 20.8 dB for 64 QAM in a Gaussian channel. If the mobile channel is considered, this value is increased to 25dB [20].

<table>
<thead>
<tr>
<th>Modulation Scheme</th>
<th>C/N</th>
</tr>
</thead>
<tbody>
<tr>
<td>QPSK(1/2 code rate)</td>
<td>5.6dB</td>
</tr>
<tr>
<td>16QAM(3/4 code rate)</td>
<td>15.1 dB</td>
</tr>
<tr>
<td>64QAM(3/4 code rate)</td>
<td>24.8 dB</td>
</tr>
</tbody>
</table>

Table 5.1: DVB-H system SNR

The DVB-H tuner sensitivity is expressed for 8 MHz channel by

\[ P_{\text{min}} = -100.2 + C / N \] (5.1)
Therefore, the sensitivity for QPSK scheme is calculated to be around -95dBm while for 64QAM is around -75dBm. Based on the sensitivity and threshold C/N ratio, the tuner noise figure (NF) is derived from

\[
NF = P_{\text{min}} + 174 - 10 \log{BW} - C/N
\]  

which is 5 dB for 8 MHz bandwidth [20].

### 5.1.2 Gain

In the absence of any interference, the maximum wanted DVB-H signal level for the DVB-H tuner is -28 dBm [18]. Therefore the tuner is required to provide 67 dB gain range to account for -95 dBm sensitivity required for QPSK constellation. The absolute gain of the tuner depends on the output power level, which is set to -8 dBm accounting for 1.4v peak-to-peak required by the standard. As a result, the tuner is required to provide the maximum gain of around 87dB.

### 5.1.3 Channel Selectivity

Another important specification for the tuner is the channel selectivity requirement. As listed in Table 5.2, the unwanted adjacent analog channel can be 38dBc higher the DVB-H desired channel. In order to prevent saturation of ADCs in the demodulator block, the tuner has to provide enough attenuation for those adjacent channels. Based on the selectivity patterns, the filter specification is derived. In order to minimize the passband ripple while maximizing the stopband attenuation, an 8\textsuperscript{th} order chebyshev filter is utilized with channel bandwidth of 4 MHz. The filter provides attenuation of 30dB at 5.25 MHz offset and 45dB at 5.75MHz offset, and over 50 dB for the higher frequencies.
Selectivity Pattern | Undesired/desired
--- | ---
S1(analog adjacent channel) | 38dBc
S2(digital adjacent channel) | 29dBc

Table 5.2: Required Sensitivity for DVB-H

5.1.4 Linearity Pattern

The nonlinear performance of the tuner degrades the output signal quality in addition to added noise. Inner-band and out-of-band blockers generate inter-modulation products due to blocks nonlinearities. The inter-modulation products that lie inside the signal bandwidth raise the noise floor and can be seen as a noise source. Among all of these terms, second order and third order inter-modulation are usually the dominant ones and therefore specific parameters are defined to measure them. In DVB-H system, the signal bands are from 470 to 865 MHz, and from 1670 to 1675 MHz. The transmitted and received cellular signals, GSM and WCDMA, act as out of band interferences which can be suppressed by the off-chip band select filter. However, those analog and digital channels in from 470-862MHz and 1670-1675 MHz are hard to be pre-filtered. In the worst case scenario the unwanted interferences can be very close to the selected band with 45dBc higher power level. The tuner system should be linear enough to receive the small signal in the presence of large interferences. The linearity scenarios for the tuner is given in Table 5.3 which indicates that the tuner is required to process the desired channel in the presence of the undesired adjacent N+2 and N+4 channels. Scenario L1 (depicted in Figure 5.2(a)) is the worst case scenario in the IIP3 calculation [20].
Due to third order non-linearity of the system, the undesired adjacent channels generate distortion components, which may fall within the desired channel. The tuner linearity performance is mainly specified as IIP3 which is given by equation (3.2), where $P_u$ and $P_w$ are the power of the unwanted signal and wanted signal respectively. The 3 dB margin is added to insure safety of the design.

\[
IIP3 = P_u + \frac{P_u - P_w + C/N + 3}{2} 
\]  

With interference level at -35dBm and the desired signal at -75dBm, IIP3 is calculated to be -1 dBm , where C/N is considered to be 25 dBc accounting for 64 QAM modulation.
5.1.5 Phase Noise Requirement

For the frequency synthesizer the key specifications are phase noise and the frequency range. The LO is required to cover both operation band, 470-862MHz and 1670-1675 MHz. The specification and design of the LO is discussed further in this chapter.

When the RF signal (including the desired channel and the undesired interferences) is mixed with LO signal, the desired RF channel is translated to baseband.
In reality, due to reciprocal mixing of phase noise of the LO the undesired signal also gets down-converted to baseband. The degradation due to reciprocal mixing depends on the power of phase noise and the interference at certain offset frequency. The phase noise requirement is derived based on the (5.4)

$$PN(dBc) = -(P_u - P_w + \frac{C}{N} + 10\log(BW) + 3)$$  \hspace{1cm} (5.4)$$

where $P_u$ is the power of undesired interference, and the $P_w$ is the power of the desired signal. To calculate the phase noise, the analog adjacent channel with the 40dB power more than the desired channel is assumed. The offset is 1.45MHZ. Considering 25dB C/N, the phase noise at the 1.45 MHz offset will be around -132 dBc/Hz.

![Figure 5.3: PLL phase noise mask](image)

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Similarly, considering the N+2 analog interference channel, the phase noise at 9.45 MHz offset is calculated to be -142dBc/Hz. The phase noise mask is derived and shown in Figure 5.3. The integrated phase noise from 1KHz to 4 MHz is less than -33dBc, satisfying the integrated phase noise requirement of the OFDM system.

5.2 Tuner Architecture

The direct conversion architecture is adopted for this tuner, to save on physical size and power consumption. It also allows addition of different front-ends, since it is not limited by the choice of a specific IF. The block diagram of the tuner is depicted in Figure 5.4.
The tuner utilizes two RF front-end to cover the UHF and L bands, but they share the LO and the baseband circuitry. Utilizing two RF front-ends supports the flexibility in the final implementation by enabling the usage of different antenna configurations which can be optimized for the desired band. Furthermore, since each RF front-end is separate, any interference at the harmonics of the local oscillator frequency is always out of band and can be rejected by the RF filter.

To keep the power consumption low while providing the high dynamic range required, the tuner uses two Automatic Gain Control (AGC) loops which is controlled from baseband: RFAGC and BBAGC. In order to detect the power of interferences, the signal power is detected at the output of the LNAs and sent to the companion demodulator, which performs the RF AGC algorithm. In the presence of a large interferer at the input of the receiver, the RF AGC loop limits the RF gain through RF LNAs, in order to prevent the mixer and baseband stages to go on saturation. This mechanism helps achieving the high linearity required in the meeting the blocking and interference specification for DVB-H.

The analog baseband path consists of two VGAs which are placed before and after the channel select filters. The AGC loop in baseband is implemented for two purposes; one is adjusting the input signal to the filter, hence, relaxing the filter requirements. The other one is to amplify the signal in order to provide constant signal level in the output.

For the RF front-end, single-ended LNA topologies may be of interest since they eliminate the need for external balanced-to unbalanced transformers (baluns); though in the fully integrated solutions harmonics of the digital circuitry such as clocks and the modulator couple to the LNA input. [21]
Digital calibration techniques should be utilized whenever possible to adjust for large variation of CMOS analog critical parameters over the wide frequency bands. These techniques can be integrated on the chip to overcome several process and architecture related imperfections, such as I/Q mismatch and baseband filter tuning.

5.3 Direct Conversion Receiver Challenges

5.3.1 DC Offset

The direct-conversion receiver suffers from DC offset which is geared the output of the mixer due to finite isolation between LO and signal Port in the mixer. As depicted in Figure 5.5(a), due to this finite isolation, the LO signal can leak to the RF port and mixes with itself, the result would be a DC offset that corrupts the signal.

In another scenario (Figure 5.5 (b)), a strong interfere from the RF port can also leak to the LO port of mixer, mixes with the original signal and make a large low frequency term at the output of mixer. The mentioned scenarios make static (constant) DC offset, however, dynamic DC offset is also possible.

As shown in Figure 5.5(c), the LO signal that has leaked to the RF port can find its way to the antenna, get radiated from antenna and subsequently reflected from other moving objects, received by the antenna again and hence makes a time varying DC offset term. To reduce the “self mixing”, the port isolation should be improved and the undesired coupling should be minimized.

To further suppress the DC offset, it is necessary to implement the DC offset cancellation which basically functions as a high pass filter. The corner frequency of this filter imposes a tradeoff. In order to preserve the corner frequency, it is desirable to have
the corner set as low as possible which results in big chip area. In the design, this corner is set as 1 KHz.
5.3.2 I/Q Mismatch

The DVB-H system uses the QPSK or QAM constellations which will result in non-symmetrical spectrum. As a result, the quadrature down-conversion is utilized to prevent the loss of information. In practice, the phase difference of the practical LO is not exactly 90° (phase imbalance) and the gain of two quadrature paths (from mixer input to baseband output) is different (gain mismatches). As a result, the signal constellation may get corrupt, increasing the BER. The mismatch can be improved a lot in the baseband by careful layout. So, the most critical blocks in the system for the I/Q mismatch are the mixer and the LO.

5.4 Block Level Specification

The gain/linearity/noise specification for each block in the cascade tuner chain is derived, so that the overall dynamic range requirement is achieved. Table 5.4 lists the block level specs for this tuner.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Variable Gain LNA</th>
<th>Mixer</th>
<th>Baseband</th>
<th>Filter1</th>
<th>VGA1</th>
<th>Filter2</th>
<th>VGA2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain (dB)</td>
<td>8/13/15</td>
<td>8</td>
<td>0</td>
<td>0/25</td>
<td>0</td>
<td>7/45</td>
<td></td>
</tr>
<tr>
<td>Noise Figure</td>
<td>1</td>
<td>4</td>
<td>5</td>
<td>5</td>
<td>5</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>IIP3 (dBm)</td>
<td>1</td>
<td>15</td>
<td>35</td>
<td>35</td>
<td>35</td>
<td>35</td>
<td></td>
</tr>
</tbody>
</table>

Table 5.4: Design Specification for main building blocks

The VGLNA should provide 7dB of the gain range to prevent saturation of the mixer and baseband stages. For the purpose of this design the -20dBm is the point of takeover, which means that the VGLNA’s gain will start to decrease when the input
power of the mixer exceeds -20 dBm. For lower gain settings, due to increase in the input power level, higher noise figure can be tolerated. In the baseband chain, in order to achieve higher SNR at the output, over 27dB variable gain should be distributed among the VGAs and the filter. Since DVB-H system is sensitive to abrupt signal variation, it is recommended to change the gain smoothly for both VGAs and the filter with setting the gain step smaller than 1 dB and using analog gain control.

![Figure 5.6: Tuner signal levels](image)

### 5.5 Frequency Synthesizer

A fractional-N PLL is proposed to cover the two bands of operation. A MASH-III modulator is proposed to shape the quantization noise out of band and facilitate the low phase noise needed for DVB-H. The reference frequency is chosen to be at 40MHz. The multi-modulus divider should divide for range of 37 to 45. The array of cascaded 2/3
dividers presented in [50] is a good candidate. A wideband VCO can be employed which covers a range of frequency: 1.5 to 1.8 GHz. Covering a large range of frequency range with a single varactor requires a high voltage–to–frequency gain which may degrade the phase noise performance. This is due to the fact that any noise coupled at the sensitive VCO control input translates to phase noise at the VCO output. By using a switched varactor bank, the operating frequency range is split into discrete regions, leading to low VCO gain. The design of the wideband VCO is explained in details in chapter 6. The block diagram of the PLL is shown in Figure 5.7.

![Figure 5.7: PLL for DVB-H tuner](image-url)
CHAPTER 6

DESIGN OF KEY BLOCKS IN FREQUENCY SYNTHESIZERS

In this chapter the design and implementation of key blocks for the frequency synthesizers are described. At first the design of the VCO for the triple-band WiMAX receiver is presented. Then, the design of the multi modulus divider for the same PLL is described. These two blocks have been integrated in the PLL presented in chapter 4. Finally, the design of a dual modulus divide-by-32/33 prescaler is discussed and results are presented.

6.1 Oscillators

The purpose of an oscillator is to generate a periodic output signal without using an input signal. This can be achieved using several principally different methods, where the oscillator topology is selected based on requirements on operation frequency, tuning range, chip area and spectral purity.

In PLL applications the frequency of the oscillator must be controllable. While the oscillator frequency is normally set by a tuning voltage, a so called Voltage Controlled Oscillator (VCO) frequency can also be controlled using a current [23] (Current Controlled Oscillator, ICO) or by digital programmable elements [24] (Digitally...
Controlled Oscillator, DCO). In reality, fully integrated oscillators often use a combination of voltage and digital methods to control the frequency to allow digital calibration.

There has been extensive research investigating the feasibility of fully integrated CMOS oscillators achieving high spectral purity [25]. The importance of inductors was realized early, and methods to improve inductor Q-value using bond-wire inductors [26], enhanced hollow inductors [27] have been proposed. The impact of different varactor types is investigated in [28] and [29].

The contribution from bias noise was recognized in [30], and the high frequency bias noise has been observed to be a dominant contributor to oscillator phase noise [31]. Methods to reduce bias noise using tail noise filtering [32][33][34] and by removing the bias current generator have been suggested [35].

The impact of device type and sizing is investigated in [36][37] and [38]. Due to the lower flicker noise PMOS devices are often preferred [98]. PMOS devices may also be selected since they often resides in separate wells and are therefore less sensitive to substrate interference [39].

The noise mechanism of the LC VCO has been subject of recent research. While early publications [27] use empirical equations for the oscillator phase noise, it was not until the arrival of the ISF theory [40] the tools for doing an analytical treatment of the oscillator phase noise was possible. Recent publications using the ISF theory to give insights to phase noise mechanisms and analytical expressions for phase noise in CMOS-LC oscillators [41].
6.1.1 CMOS LC VCO Principles

Due to the differential structure and relatively good phase noise performance, the differential LC oscillator is one of the most popular oscillator configurations in fully integrated RF CMOS applications. The typical LC VCO is shown in Figure 6.1. The LC tank determines the oscillation frequency, while the active cross coupled pair provides the negative resistance \(-gm\) which is required for sustained oscillation. The frequency of oscillation is given by

\[
f_0 = \frac{1}{2\pi\sqrt{LC}}
\]

(6.1)
In order to be able to vary the oscillation frequency the capacitor is often implemented using a voltage controlled capacitor (varactor) or an array of digitally controllable capacitors [42], or a combination thereof [43].

An alternative way to adjust the frequency is to switch the inductor [144] or by using MEMS to tune the inductance value [45]. Using these methods, wide tuning range can be achieved at the expense of increased area or complicated processing steps. A third way to tune the oscillation frequency is to change the bias current. This method has the drawback that the oscillation amplitude and the phase-noise performance is a strong function of the bias current.

6.1.2 Steady State Amplitude

As the amplitude in the oscillator increase, the circuit can no longer be analyzed using small signal approximations. Figure 6.2 shows the start transient of a typical oscillator. In a real circuit the oscillation starts due to noise or an interferer coupling into the oscillator. In simulations the oscillator may not always start unless an interference such as a current pulse or a damped sinusoidal current is injected. When the oscillation reach steady state, the transistors will act as commutating switches, steering the bias current into the resonance circuit.
6.1.3 Current Limited Region

If the Q-value of the resonance circuit is reasonably high, it can be assumed the voltage across the resonance circuit is sinusoidal. The differential peak amplitude $A$ across the oscillator can then be calculated

$$A = \frac{2}{\pi} I_{\text{bias}} R_{\text{tank}}$$

(6.2)

where $A$, $I_{\text{bias}}$ and $R_{\text{tank}}$ represent the oscillation amplitude, the tail current and the parallel resistance of the tank respectively. This can be seen in another way, as amplitude increases, the equivalent negative resistance decreases till to the point where the latter becomes equal to tank resistance.
6.1.4 Voltage Limited Region

The oscillation amplitude will grow linearly with the increasing bias as long as M1, M2 and the bias circuit operates in saturation. When the amplitude grows, the swing at the drains of M1 and M2 cause the transistors to go into the triode region, limiting the effective output current. It is usually not desirable to operate the oscillator in this condition, since the current consumption is high and without improving the oscillator performance.

6.1.5 Spectral Purity of the Integrated VCO

The stringent phase noise profile of the modern wireless application such as WiMAX or DVB-H requires the VCO to exhibit very low phase noise over a wide range of frequencies. In an integrated environment, the analog and digital functions are implemented on the same substrate. The digital circuitries inject noise into the substrate while switching. The noise can couple between blocks through various mechanisms: Coupling through the substrate or coupling through the supply and signal lines.

Noise coupled to VCO control line, supply and bias lines gets converted into noise sidebands around the oscillation frequency through FM, AM, and AM-FM conversion mechanisms [46]. The AM noise contributions are less significant, since they can be removed by a limiter. However the AM noise is often converted to FM noise through AM-FM noise conversion.

6.1.6 Effect of Control Voltage Noise on the Phase Noise of VCO

The noise coupled to the control voltage ($V_{CNTL}$) varies the tank capacitors and hence, the resonance frequency. Consequently any low frequency noise is translated
around the oscillation frequency, and can be viewed as the frequency modulation (FM) noise. The phase noise contribution of any broadband noise source with rms value of $V_n$, on the VCO control line can be described using narrow-band FM approximation[4]:

$$L_{VCN}(fm) = 10 \log \left( \frac{P_{\text{noise}}}{P_{\text{carrier}}} \right) = 10 \log \left[ \frac{(K_{VCO} V_a)^2}{2 f_m^2} \right]$$ \hspace{1cm} (6.3)

The noise on the control line is composed of the loop filter resistor thermal noise and CP current noise, in addition to any other noise coupled through substrate and signal paths. It is seen that the phase noise contribution from the control line to total PLL noise can be reduced by keeping $K_{VCO}$ low.

### 6.1.7 Effect of Amplitude Variations on Phase Noise of the VCO

The effective capacitance formed by a varactor is dependent on the voltage across the varactor as well as its bias. This means that the value of a varactor in a differential LC oscillator is depending not only on the control voltage, but also on the amplitude of the oscillation. Consequently, amplitude fluctuations modulate the effective value of the varactors, which turns the AM noise into FM noise. The sensitivity of a varactor’s effective capacitor $C_{\text{eff}}$ to amplitude of oscillation is given by:

$$\frac{\partial C_{\text{eff}}}{\partial A} = \frac{C_{\text{max}} - C_{\text{min}}}{\pi} \frac{2V_{\text{DC}}}{A^2} \sqrt{1 - \left( \frac{V_{\text{eff}}}{A} \right)^2}$$ \hspace{1cm} (6.4)

The AM-FM conversion gain in $\left( \frac{V}{\sqrt{\text{Hz}}} \right)$ is defined as [46]

$$K_{AM-FM} \equiv \frac{\partial w_0}{\partial A} = \frac{\partial}{\partial A} \left( \frac{1}{\sqrt{LC_{\text{eff}}}} \right) = -\frac{1}{2} \frac{w_0}{C_{\text{eff}}} \frac{\partial C_{\text{eff}}}{\partial A}$$ \hspace{1cm} (6.5)

From (6.4) and (6.5) it can be seen that in order to minimize the AM-FM sensitivity, the
amplitude should be as large as possible. Also it can be noted that the due to larger value of \((C_{\text{max}} - C_{\text{min}})\), the wideband VCOs are subject to more significant AM-FM noise conversion. Using narrowband-FM approximation, the AM-FM noise contribution can be calculated as:

\[
L_{\text{AM-FM}}(f_m) = 10 \log \left( \frac{K_{\text{AM-FM}} V_{n,\text{AM}}}{2 f_m^2} \right)
\]

(6.6)

where \(V_{n,\text{AM}}\) is the rms value of AM noise voltage spectral density on the oscillation envelope. Amplitude variation in wideband VCOs cause several additional effects which are of importance. The most significant one is the reduction of the effective range of varactor’s capacitive range \((C_{\text{max}}/C_{\text{min}})\) resulting in the reduction in overall tuning sensitivity [4].

6.1.8 Supply Pushing in LC VCOs

The DC supply noise or supply pushing has become a critical factor in design of integrated low phase noise VCOs in the deep submicron technology. This is due to the reduced power supply voltage, high volume of digital integration and more number of blocks sharing the substrate. In an integrated environment, the VCO supply lines are exposed to the switching noise and interference from other blocks coupled through the substrate as well as the noise from the devices in the regulator circuitries. The supply noise modulates the amplitude of oscillation and contributes to VCO phase noise through AM-FM conversion. In [48], it is stated that the supply noise among all deterministic noise sources in the VCO has the most significant contribution to the phase noise.
The VCO is considered to operate in the current limited region where the amplitude of oscillation is not yet limited by the supply voltage. The VCO differential oscillation amplitude is given by (6.2). The tail current transistor is operating in saturation, and $I_{bias}$ is given by

$$I_{bias} = \frac{\mu_n C_{ox}}{2} \left( \frac{W}{L} \right) (V_{gs} - V_{tn})^2$$

(6.7)

The variation in supply voltage changes the $V_{gs}$ of the tail current thus modulates the $I_{bias}$. From (1) and (2) it is clear that the variation of the supply voltage modulates the amplitude of oscillation which leads to increasing the AM to FM noise and degrading the phase noise performance.

### 6.1.9 Self-Regulated VCO

Figure 6.3 shows the VCO core along with the amplitude regulation feedback. The differential amplitude is measured by peak detector and compared to the $V_{reg}$ through the error amplifier. The respective output error changes the $V_{gs}$ of the tail current, regulating the VCO core current $I_{bias}$. This arrangement regulates the source coupled node; keeping the oscillation amplitude regulated and minimizing the varactor value variations, hence, decreasing the AM-FM noise.
To give a better insight to noise characteristics of this configuration, the transfer function of various noise to the output are given as:

\[
\frac{V_{\text{out}}}{V_{n,\text{vdd}}} = \frac{gm3 \times r}{1 + gm3 \times A \times r} \approx \frac{1}{A}
\]

(6.7)

\[
\frac{V_{\text{out}}}{V_{n,\text{gate}}} = \frac{gm3 \times r}{1 + gm3 \times A \times r} \approx \frac{1}{A}
\]

(6.8)

\[
\frac{V_{\text{out}}}{V_{n,\text{reg}}} = \frac{gm3 \times r \times A}{1 + gm3 \times A \times r} \approx 1
\]

(6.9)

where \(gm3\) is the transconductance of the tail current and \(r\) is the total resistance looking from the source coupled node. It can seen that within the regulator loop bandwidth the noise from VDD and the gate of the tail current are suppressed by the factor of the gain.
of the amplifier, minimizing unconverted noise and supply pulling. On the other hand, the noise from the regulator is transferred with no reduction. Therefore, a low noise reference should be utilized for generating $V_{\text{reg}}$. This topology ensures the start-up condition of oscillation at the lower end of frequency range, by setting the bias current $I_{\text{bias}}$ at the start-up, eliminating the need for the amplitude calibration circuitry.

### 6.1.10 Choice of $V_{\text{reg}}$

The voltage $V_{\text{reg}}$ adjusts the current $I_{\text{bias}}$, and regulates the amplitude oscillation through the regulator amplifier. As the bias current is increased, the oscillation amplitude becomes larger and the phase noise decreases. This holds until the differential output amplitude, $V_{pp}$, remains smaller or equal to value of the threshold voltage of the PMOS transistor, $|V_{th}|$, corresponding to the minimum phase noise. As the amplitude increases from $|V_{th}|$, the cross coupled transistors enter the triode region. As a result, the parallel resistance of the LC tank decreases, leading to reduction of $Q$ of the tank and degradation of the phase noise [49].

To ensure the optimal oscillation amplitude over a wide range of frequency and under PVT variations, a proper $V_{\text{reg}}$ should be chosen to keep the amplitude of oscillation at $|V_{th}|$. This is achieved by feeding a reference signal at the target center frequency with the amplitude of $|V_{th}|$ to a peak detector identical to the one used in the regulation path.
6.1.11 Broadband LC VCO with Capacitor Switching

The VCO tuning range must cover all selectable channels within a given VCO control voltage (VCNT). This voltage is generated by charge pump current fed into a loop filter. As the feature size shrinks, the voltage supply scales down which results in smaller range of charge pump current. Also to account for PVT variation the effective range of VCNT is smaller, resulting in a really high value for $K_{VCO}$, hence increasing the VCO sensitivity to noise and disturbances. In addition the required minimum tuning range, the on-chip varactor C-V characteristics do not exhibit a linear behavior.

As shown in Figure 6.4, in order to cover the whole tuning range with relatively low $K_{VCO}$, the broadband tuning curve is divided into several narrow sub-bands with enough overlap. The continuous tuning enable moving along a sub-band, while moving from one sub-band to another becomes possible through the discrete tuning.

![Figure 6.4: VCO tuning curves](image)

(a) single continuous tuning curve (b) Tuning curve divided into subbands
6.1.12 Broadband VCO for Multi-Band WiMAX Application

The VCO core is based on the differential cross coupled PMOS only architecture as depicted in Figure 6.3. The VCO without the tail bias offers a larger signal swing and devoids the flicker noise from the tail biased current source. Despite these advantages, it results in higher power consumption for the same phase noise performance offered by the tail-biased topology. To achieve the tuning range required the VCO frequency ranges from 5.5 GHz to 6.05GHz. As shown in Figure 6.3 the continuous tuning in a VCO is facilitated by use of a set of MOS varactors, while discrete tuning (shown in Figure 6.5), is done by a switched MIM capacitance array. The designed VCO is using four discrete control bits which are converted to a thermal code in order to switch one of the twelve fixed cap in and out of the tank. Since the thermal code is used, the switched capacitances in the bank are identical so all the subbands are subject to a conformed error due to fabrication inaccuracies.

Figure 6.5: Coarse Tuning: the Binary to thermal decoder and the switched-cap cell.
Figure 6.6 shows the VCO tuning curves for the discrete control bits changing from 0000 to 1100. To account for variation in charge pump output, the $V_{\text{CNTL}}$ effective range is considered to be between 0.3-1.4V. The output frequency ranges from 5.52GHz to 6 GHz. The phase noise at center frequency of 5.7GHz is measured to be -126dBC/Hz at 1 MHz offset, which makes the VCO suitable for WiMAX application. The phase noise shows an improvement of about 5 dB compared to the VCO with no amplitude regulation. For Supply pushing performance, the supply voltage is varied from 1.55 to 2.05 V. The output frequency compared to the one with no regulation. As it can be seen, the regulation has a significant impact in reducing the sensitivity.

Figure 6.9 presents the result for Monte Carlo statistical analysis of the VCO frequency. The VCO parameters, B4-B0 and control voltage, are chosen to set the output frequency to 5.74 GHz using typical models at 27°C. The deviation of the center frequency is shown in Figure 6.9(a) under process variations in 50 iterations. The standard deviation is about 20 MHz. This deviation can be adjusted by using proper frequency correction and calibration at VCO and baseband. Figure 6.9(b) present the deviation of a single tuning curve of the VCO under process variation for 25 iterations.

Table 6.1 summarizes the design performance of the designed VCO. The power consumption is 6.48 mA from a 1.8 V voltage supply.
Power Supply | 1.8V
---|---
Power Consumption | 6.48 mA
Frequency Range | 5.52-6 GHz
Phase Noise at 100KHz Offset | -105 dBc/Hz
Phase Noise at 1MHz Offset | -126 dBc/Hz

Table 6.1: Performance summary of the amplitude regulated VCO

Figure 6.6: Tuning curves for the VCO
Figure 6.7: Phase noise at 5.7 GHz

Figure 6.8: Voltage supply pushing of the VCO
Figure 6.9: Monte Carlo statistical simulation result for process variation
(a) histogram of the center frequency deviation=50
(b) tuning curve deviation N=20
6.2 Design of Multi-Modulus Divider for Triple WiMAX PLL

Multi Modulus dividers (MMD) are essential building blocks in the \(\Sigma\Delta\) fractional PLLs. They provide a variable division ratio, which enables the generation of frequency with fractional resolution. There are several configuration for MMDs presented in literature, [50][51][52]. All these circuits utilize the dual modulus prescaler block(s) which perform division by \(N/N+1\) to achieve flexibility in the division ratio. Design of a high-speed broadband prescaler is described in details in the next section.

For the purpose of this design, the swallow divider architecture is chosen. A typical pulse-swallow divider is shown in Figure 6.10. It includes A programmable counter, \(P\), a swallow divider, \(S\), and a dual modulus prescaler \(P/P+1\).

The dual Modulus prescaler divides by either \(P\) or \(P+1\), depending on the value of its input, Modulus Control. The programmable counter is a frequency divider with
programmable division ratio M. The programmable divider differs from the prescaler in the sense that, once it is programmed, the division ratio remains constant. When the circuit starts from reset state, the prescaler divides the VCO frequency by N+1. The prescaler output is divided by both the programmable counter and the swallow counter until the latter reaches S, which is after (N+1)S. At this point the S counter changes the modulus control, forcing the prescaler to divide the $f_{\text{in}}$ by N. Following the modulus change, the prescaler and the programmable divider keep on dividing until the latter become full, meaning that (P-S) pulses are counted after the modulus change. Thus the output generates one full cycle for every PN+S cycle at the input.

As stated in Chapter 4, the target application for this divider is the triple-band WiMAX which is centered around 5.7 GHz. The reference frequency is chosen around 40 MHz which leads to a division ratio of 142 for the MMD. The circuits in the prescaler were designed using the Source Coupled Logic (SCL) (shown in Figure 6.11)[55] to facilitate the high speed operation. The rest of the divider is implemented in CMOS logic. The swallow and program counter are implemented by one 5 bit modulo-up-counter and some logic circuitry which ensure proper generation of Modulus Control and Reset signal. The divide is capable of generating the divide ratios from 128 to 160.
6.3 Design of High Speed Broadband Dual Modulus Prescaler

Prescaler along with the VCO are the two components operating at full output frequency synthesizer; its design brings important challenges to the design of multi-gigahertz synthesizers in standard CMOS process. The spectral purity and low power consumption are two major performance factors in the design. To date, most of the high speed dual modulus prescalers use static source-coupled logic (CML) [53] resulting in a high power consumption. The dynamic logic decreases the power consumption and enhances the speed [54]. However the Extended True Single-Phase Logic (E-TSPC) has been only used in design of low speed prescaler [54][55]. The maximum frequency of operation reported in literature is 1.75GHz [54]
6.3.1 Dual Modulus Prescaler Architecture

A divide-by -32/33 dual-modulus prescaler generally consists of a synchronous divide-by -4/5 part and an asynchronous divide-by-8 part. The block diagram for the conventional architecture is shown in Figure 6.12.

The synchronous divider is the only part working at the maximum input frequency. Most of the time its control signal CTRL is low, so the output frequency F4 is determined by the loop over the first two D-flipflops and equals to 1/4 of the input frequency. This frequency is divided by 8 in asynchronous divider to obtain an output frequency F_{out} equal to F_{in}/32. The divide-by-33 operation is enabled by setting the MODE input to be high. When the outputs of all flipflops of the asynchronous divider are high, i.e. once every period of output signal F_{out}, the CNTRL signal becomes high.

This causes the loop to be closed over three flipflops instead of two. This extra delay is equivalent to a divide-by-five operation. So the prescaler divides once by 5 and 7 times by 4, which results in a division by 33.

The challenges of conventional prescaler topology are situated in the synchronous divider. The Synchronous divider is operating at the maximum frequency while the rest of the circuit is operating at most at 1/4 of input frequency. The synchronous divider contains three fully functional D-flipflops. The majority of the power in prescaler is consumed by these three flipflops. Also they are the main reason for high clock load. The NAND gates in the critical path of the synchronous divider loop will decrease the maximum input speed [54]. Thus careful consideration should be given to the design of D-flipflops. Embedding NAND in the first stage of the Flipflops will decrease their limitation on the input signal frequency [55].
6.3.2 Design and Implementation of Prescaler

In this section the design of blocks used in prescaler is discussed in details. For the purpose of this design, The Extended True Single-Phase-Clock (E-TSPC) D-flipflop topology introduced in [55] was used. Single-phase-clock strategy in flipflops design has simplified clock distribution and avoids clock racing and overlap problem, thus it improves the speed and power saving [56].

Figure 6.12 shows the Glitch-free D-flipflop used in this design. As shown in Figure 6.14, the NAND gate is embedded in the 1st and 3rd flipflops design to reduce the delay in the critical path. The divide-by-2 circuits are basically D-flipflop in toggle
configuration. The flipflop topology in [56] is used for the design. Figure 6.15 shows the divide-by-2 circuit used in the design which is optimized for divide-by-2 operation and delay performance.

Figure 6.13: E-TSPC glitch-free D-flipflop
Figure 6.14: E-TSPC glitch-free NAND embedded D-flipflop

Figure 6.15: Divide-by-two circuit topology
6.3.3 Physical Design of the Prescaler

The blocks are laid out and connected to each other according to the floorplan. The blocks are placed in two stripes sharing the GND line. To minimize the delay in the critical paths, higher level metal was used to propagate the signal through the critical paths. Figure 6.16 shows the final layout of the prescaler. The circuit occupies an area of 49\(\mu\text{m}\times26\mu\text{m}\).

![Figure 6.16: Layout of the designed prescaler](image)

6.3.4 Simulation Results

The designed prescaler has been simulated in Cadence Spectre using 0.18\(\mu\text{m}\) parameters. Figure 6.17 shows the typical waveforms for the /33 operation at 3 GHz input frequency. It is observed that at the rising edge of output, the CNTRL signal is set to 1. This enables the third flipflop in the synchronous divider which results in a one
input period delay in the output of the synchronous divider.

In Figure 6.19 the simulated maximum operating frequencies as well as the corresponding power consumption are given at different supply voltages. The prescaler can operate at the frequency 5.3GHz at 1.8v supply and operate down to 0.6v with a maximum frequency of 210MHz. Figure 6.18 shows the simulation result for the single side bend phase noise simulation. It is observed that the phase noise floor is below -167dBc/Hz.

Figure 6.17 : Waveforms of a typical cycle of /33 operation
Figure 6.18: Simulated single sideband added phase noise at the output of the prescaler

Figure 6.19: Maximum operating frequency and power consumption versus power supply voltage
<table>
<thead>
<tr>
<th>Technology</th>
<th>0.18 μm CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage supply</td>
<td>1.8V</td>
</tr>
<tr>
<td>Minimum frequency</td>
<td>210MHz &lt;1GHz</td>
</tr>
<tr>
<td>Maximum frequency</td>
<td>5.3GHz&gt;3GHz</td>
</tr>
<tr>
<td>phase noise</td>
<td>-152dBc@10KHz</td>
</tr>
<tr>
<td></td>
<td>-165dBc/Hz@1MHz</td>
</tr>
<tr>
<td></td>
<td>PN floor :-167dbc/Hz&lt;-150 dBc/Hz</td>
</tr>
<tr>
<td>Power dissipation</td>
<td>2.53mW</td>
</tr>
</tbody>
</table>

Table 6.2: Performance summary of the prescaler

<table>
<thead>
<tr>
<th>Freq</th>
<th>1GHz</th>
<th>2GHz</th>
<th>3GHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mode</td>
<td>/32</td>
<td>/32</td>
<td>/32</td>
</tr>
<tr>
<td>Mode</td>
<td>/33</td>
<td>/33</td>
<td>/33</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>659.5μw</td>
<td>675μw</td>
<td>1.297mw</td>
</tr>
<tr>
<td>Output Freq</td>
<td>31.25MHz</td>
<td>30.3MHz</td>
<td>62.5MHz</td>
</tr>
</tbody>
</table>

Table 6.3: Worst case corner simulation results: slow-slow models at 65°C
CHAPTER 7

CONCLUSIONS AND FUTURE REMARKS

This thesis focuses on the design of $\Sigma\Delta$ fractional-N frequency synthesizers for OFDM based applications. As discussed in earlier, $\Sigma\Delta$ fractional-N PLLs have proven to be a very good candidate for the emerging OFDM-based radios which require employment of fast switching low phase noise frequency synthesizers.

In this work, the mechanisms which degrade spectral purity in $\Sigma\Delta$ fractional-N PLLs i.e. block noise and fractional spurs and their effect on phase noise were explored. Solutions were proposed to enhance the low phase noise, wide-bandwidth trade-off in frequency synthesis. Furthermore, the design block for low noise performance was shown.

7.1 Conclusions

In Chapter 2 an overview of frequency synthesizers in modern wireless radios is given. Specifically, the impact of phase noise on the OFDM signals was explained. The PLL model as a negative feedback was analyzed and the different PLL architectures and their advantages and limitations were presented.

In Chapter 3, the phase noise in PLL was investigated. The contribution of
different noise sources in PLL was analyzed through using an AC small signal model. The effect of various loop parameters on phase noise and integrated phase noise was investigated and it was shown how to optimize these parameters in order to achieve a minimal phase noise. Furthermore, the fractional spur generation and cancellation techniques were presented. The impact of loop nonlinearities on folding of the quantization noise and increase of the close-in noise of PLL is shown.

In Chapter 4, the design of a ΣΔ PLL for triple-band WiMAX application was presented. The Type-I PLL is immune to the nonlinearities in PFD/CP. As a result, the quantization noise folding was decreased. The design of PLL loop and PLL blocks were presented. The physical realization of the PLL in tsmc0.18 μm was shown and the simulation results were given.

Chapter 5 focuses on the system study of a dual band DVB-H tuner. The system requirement for L-band and UHF band were studied and critical system parameters were derived. A zero-If architecture was adopted for the design; the specification of different blocks in the tuner was derived in terms, of gain/noise/ linearity. The phase noise mask of the LO was given. A frequency synthesizer was proposed to cover both UHF-band and L-band.

In chapter 6, design of low noise, high performance blocks for PLL were described in details. The design and implementation of a VCO with amplitude regulation was presented. The VCO was integrated in the PLL for WiMAX application presented in Chapter 4. The design of MMD for the above mentioned PLL was explained. A wideband low power prescaler was designed using the E-TSPC logic circuits which lead to low noise, low power performance.
7.2 Direction of Future Work

The phase noise model used in chapter 3 provides helpful insight to the contribution of noise sources in the PLL in by and avoids complexity in the analysis. However, it doesn’t account for non-linearities and non-idealties in the loop. Also, it models the digital circuit noise a simple gain. The time domain event driven PLL can account for non-linearities, such as dead-zone, and noise folding. Also jitter based models gives a better insight into the noise contribution of the digital circuits. As a result, a hybrid model could be developed which may offer the transparent insight while having a more accurate modeling of the loop dynamics.

Furthermore, the built-in test modules, such as on-chip phase noise measurement block in [57], may allow us to quantify the phase noise online and compensate for it on – chip by adjusting the charge pump current injected into the loop. It should be noted that changing the charge pump current will change the bandwidth of the loop; the effect could be studied thoroughly in order to develop the compensation mechanism.

The discrete loop filter on the designed type-I PLL offers the advantage of isolating the control node of the VCO from the noisy operation of PFD/Cancellation DAC which exhibit large transients, and makes sure that a clean signal is sampled into the loop filter at the sampling instance. However, it still suffers from sampling clock feedthrough which generates a sequence of periodic disturbances modulating the VCO and degrading the VCO performance. This problem should be addressed by proposing new charge injection compensation technique in order to reduce the magnitude of clock feedthrough.
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