MULTI-MODULUS DIVIDER IN FRACTIONAL-N FREQUENCY SYNTHESIZER FOR DIRECT CONVERSION DVB-H RECEIVER

A Thesis

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By

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ABSTRACT

Digital broadcast to mobile phones, or Mobile TV, is believed to be the future of broadcast. Among various international mobile TV standards, DVB-H emerges as the prospective global standard.

A Fractional-N Delta-Sigma frequency synthesizer is introduced for dual-band (European UHF band and USA L-band) direct-conversion DVB-H receiver. A 5-bit MOS Current-mode Logic (MCML) Multi-modulus Divider with division ratio of 32 to 63 is designed for the frequency synthesizer. The circuit is capable of operating from 1.6 to 2.5 GHz with less than 0.1 % frequency division error, -145 dBc/Hz phase noise contribution, and 23.3 mW power consumption in TSMC 0.18 μm CMOS process. A comparison in performance with existing designs is also presented.
To my parents
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CHAPTER 1

INTRODUCTION

Television has seen lots of innovations: from black and white to color broadcast, from analog cathode-ray tubes (CRT) to wide-screen digital high definition flat panels (LCD or plasma), from rabbit ear receiving to digital cable or satellite delivery. All these technologies increase the popularity of TV to such an extent that it has become an indispensable part of our life and culture.

Now TV is taking the next step: Mobile TV, i.e., digital broadcasting to mobile phones. As many have pointed out, mobile digital broadcast TV (DTV) combines the two best-selling consumer products in history - TVs and mobile devices [13]. More than 2 billion people around the world own or use mobile phones. Increasingly, people are using their mobile phones for multimedia - not just for communication, but also for entertainment, news and information services [18].

1.1 The future of broadcast: Mobile TV

There are a number of reasons why people believe that Mobile TV is the future of broadcast.

First of all, Mobile TV frees the viewer from both time and geographical constraints. Unlike older generations, who gathered in the living room during prime
time to watch nightly news and the latest TV series, the current generation prefer watching their favorite shows whenever and wherever they want. The digital cable service has already provided programs on demand. Mobile TV takes one step further: viewers don’t need to be at home in front of TV’s at all.

Secondly, Mobile TV fits into a busier life style. It is not unusual for commuters to spend as long as an hour or more everyday on the road. In countries where public transportation is popular, such as Japan and China, Mobile TV has an extremely promising outlook: commuters could use the time to watch the latest news, receive weather updates, check stock prices and so on live from their cell phones.

In addition, Mobile TV offers unique interaction between viewers and broadcast content providers. TV content providers have always been looking for strong viewer feedback and interaction through short message voting or other methods. Watching TV from cellphones would make it easier for viewers to get involved and generate more revenue for content providers.

Last but not the least, Mobile TV, like other digital broadcast technologies, provides high quality imagines and enhances viewer experience. All these reasons lead my to believe that Mobile TV would be the driving force for TV industry in the future.

1.2 Mobile TV landscape worldwide

There are several Mobile TV standards in use around the world, such as DMB, ISDB-T, DVB-H and MediaFLO.

Digital Multimedia Broadcast (DMB) is the Mobile TV standard developed by and mostly offered in South Korea. Overseas commercial business service includes
Germany (6 cities) from June 2006 and China (Beijing) from September 2006 [19]. DMB is based on digital audio broadcasting (DAB) standard, which was originally designed for mobile receivers.

Digital Video Broadcasting - Handheld (DVB-H) is Europe’s mobile TV broadcast standard. It is derived from the Digital Video Broadcasting - Terrestrial (DVB-T) standards that bring digital TV to household TV sets. It is the leading global technology and has been commercially deployed in Europe with additional trials around the world.

Integrated Service Digital Broadcasting-Terrestrial (ISDB-T) is the DTV standard in Japan. It was adopted for commercial transmission in Japan starting in December 2003. Brazil is one of the few countries outside Japan that adopted this standard.

MediaFLO is Qualcomm’s new technology to broadcast to portable devices like mobile phones and PDA’s. F-L-O stands for “forward link only” [2]. Unlike the standards mentioned above, FLO is a proprietary standard, which means only a few companies that developed the standard have access to its technical details. Current channels on air include CBS Mobile, NBC 2Go, MTV, FOX Mobile etc. Right now these services are only available through Verizon Wireless V CAST.

In addition to the standards mentioned above, China has lately announced its own digital multi-media broadcasting standard CMMB: China Multimedia Mobile Broadcasting, which many believed to be strikingly similar to DVB-SH [5].

A brief comparison among the standards is listed in table 1.1. One thing that all the standards have in common is the Orthogonal Frequency Division Multiplexing (OFDM) air interface. OFDM is a good choice for mobile TV reception because it
Table 1.1: A brief comparison of Mobile TV standards worldwide

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offers immunity to multi-path fading through the insertion of guard interval that eliminates intersymbol interference (ISI) [13]. Furthermore, OFDM enjoys high spectral efficiency and works well within single-frequency network (SFN), which uses spectrum more efficiently than conventional multi-frequency broadcast network.

It is also worth noticing that MedioFLO is not an open standard. Proprietary standards are unique to the specific commercial entity. Open standards, on the other hand, grant all layers of the value chain additional revenue opportunities from an untapped market. Many believe that working in an open ecosystem that is built on open standards is ultimately better for both consumers and the industry [13].

1.3 DVB-H: prospective global standard

Among all standards, DVB-H is increasingly gaining ground and considered to be the prospective global technology standard for mobile television.

The first reason could be that DVB-H is based on a proven technology, DVB-T [30], a global standard for digital terrestrial TV widely deployed in Europe and other parts of the world. DVB-H is an extension of DVB-T with backward compatibility [29]. The two standards have the same physical layer, but DVB-H introduces multi-protocol
encapsulation (MPE), making it possible to transport data network protocols on top of MPEG-2 transport streams [7]. An additional 4k mode is available in DVB-H for more flexibility in network planning. A forward error correction (FEC) scheme is also introduced to improve the robustness and thus the mobility of the signal.

DVB-H also has a unique power saving technique called time slicing. Figure 1.1 shows the principle of time slicing. Instead of transmitting data at fixed data rate at all times, DVB-H data are transmitted in bursts. The receiver could then switch off for the rest of time and go to “sleep” mode. It would only “wake up” when the service to which it is tuned is transmitted. This technique could add up to significant power savings as much as 90%.

Another major advantage of DVB-H is its openness. In contrast to a proprietary standard, an open standard introduces opportunities to almost everyone in the value chain. Carriers and wireless operators could add new services, content providers and broadcasters gain additional viewer, handset manufacturers and silicon vendors could develop new phones and chips, even software third parties could deliver software and
applications since there is a broad group of companies that support DVB-H [13]. After all, the consumer is the ultimate winner.

In addition, DVB-H is a standard with many commercial and trial deployments. Up to now, DVB-H mobile TV services have been launched in Italy, Finland, Vietnam, India, the Philippines and Albania. Numerous trials have taken place all over the world, including trials in the United States in Las Vegas, Nevada [9].

On July 18, 2007, European Union officially adopted DVB-H as the single European Standard for mobile TV [25], another huge boost for DVB-H toward its acceptance as the global mobile TV standard.

1.4 Organization of this Thesis

The rest of this thesis is organized as follows. Chapter 2 introduces the problem of frequency synthesizer design for a dual band DVB-H receiver. It starts with an overview on mobile TV receiver architecture and case study. Then it takes on the issue of frequency synthesizer: integer-N and fractional-N structures and delta-sigma noise shaping method. A fractional-N delta-sigma frequency synthesizer for DVB-H application in both Europe and the US is presented at the end of the chapter.

Chapter 3 describes the multi-modulus divider design for the proposed frequency synthesizer. A generic architecture and Current-Mode Logic (CML) circuit topology are chosen for the application and their design procedure and methodologies are addressed. Simulation results and layout efforts of the multi-modulus divider are also included in this chapter.

Chapter 4 summarizes the results of the thesis, and gives pointers to future research that can be based on this work.
CHAPTER 2

FREQUENCY SYNTHESIZER DESIGN

In a world where standards differ among geographical regions, or the same standard is deployed in different spectrums from country to country, as in the case of DVB-H, where UHF bands are used in the European Continent while L-band is allocated for its use in the U.S.A. [31], the best way to build chips or chip sets for mobile TV seems to be creating flexible solutions that could handle multiple standards [3].

This chapter would start with an overview on mobile TV receiver. Frequency synthesizer would be explained in details with a special focuses on fractional-N and delta-sigma noise shaping. Then we are ready to present the frequency synthesizer with a single VCO for dual-band DVB-H application.

2.1 Mobile TV receiver

There are a number of criteria in choosing a receiver architecture, such as complexity, cost, power dissipation, and the number of external components. As VLSI technologies evolve and applications differ, the relative importance of each of these criteria changes [21].

In a mobile TV application, power dissipation and the number of external components generally have a higher priority among other design considerations. A lower
power consumption could prolong the battery life of portable devices, thus increase the effective watching time of mobile TV broadcast. A compact design for mobile devices require small die size, which prohibits too many off chip components.

2.1.1 Receiver architecture: heterodyne versus homodyne

Before the discussion, it would be helpful to notice the difference between the band and the channel. A band refers to the entire spectrum in which the users of a particular standard are allowed to communicate [21]. For instance, in Global System for Mobile Communication (GSM), the available receive band spans from 935 MHz to 960 MHz; the Digital European Cordless Telephone (DECT) operates in the band 1880 MHz to 1900 MHz. A channel, however, refers to the signal bandwidth of only one user in the system. So in the case of GSM, a channel is only 200 kHz, while a single channel in DECT is 1.73 MHz wide [21]. Usually a receiver would go through both a “band selection” and a “channel selection”. The former removes the out-of-band interferers, and the latter rejects the out-of-channel (usually in-band) interferes.

There are two main receiver architectures: heterodyne and homodyne (also called direct-conversion). Figure 2.1 shows a simple heterodyne receiver.

Figure 2.1: Simple Heterodyne Receiver [21]
Heterodyne, or superheterodyne, is a receiver architecture that translates the received signal band into a much lower fixed intermediate frequency (IF) before further amplification, demodulation and processing. The frequency translation is also called “downconversion”.

Heterodyne suits a high center frequency narrow band application. As mentioned above, filtering a narrow channel that is centered at a high frequency demands prohibitively high Q’s of the filter. With the help of a mixer, heterodyne receiver moves the center of the signal spectrum linearly from high RF to a lower IF, which relax the requirements on channel selection filter.

A huge problem with heterodyne structure is its image problem, which is illustrated in figure 2.2. The bands symmetrically located above and below the LO frequency are downconverted to the same frequency. For example, if a desired band is located around $\omega_1$, interferers centered around $\omega_{\text{im}}$ is the image band, which would be converted to the same IF frequency.

The problem of image is a serious one [21]. An “image rejection” filter is often needed to suppress the image band signals. Furthermore, the image-reject filter is
Homodyne architecture is usually realized as a passive, external components. This makes heterodyne architecture less attractive to mobile TV applications, which calls for smaller die size and single chip solutions.

Alternative solutions to the image problem include image-reject topologies, like Hartley and Weaver [21]. In ideal cases, the summed outputs should be image free. But in practice, impection image-rejection results from gain and phase mismatches between the two signal paths [20].

Homodyne, also called direct-conversion or zero-IF, is the natural approach to downconverting a signal from RF to baseband. It translates the band of interest directly into zero frequency and employs low-pass filtering to suppress the nearby interferers, as shown in figure 2.3.

One of its obvious advantages over heterodyne architecture is the circumvention of the image problem because $\omega_{IF} = 0$. Thus no image rejection filter is needed. IF SAW filter and subsequent stages are replaced with low-pass filters and baseband amplifiers, which are more amenable to monolithic integration [20].
2.1.2 Mobile TV Receiver Case study

Though heterodyne receiver architecture are widely used in many applications, such as GSM mobile terminals, DVB-T television receiver, homodyne structure are more common for mobile TV reception due to its constraints of small physical size and low power consumption. In this section, we will analysis a few DVB-H tuner chips to gain a better idea on the issue.

Figure 2.4: A dual-band DVB-H tuner block diagram [31]
Figure 2.4 shows a dual-band single chip DVB-H tuner from Broadcom (formerly Athena Semiconductors), Athens, Greece [31] for both European DVB-H requirements in the UHF spectrum and US DVB-H requirements in the L-band spectrum. The receiver is a direct-conversion architecture with dual RF paths covering 470 to 890 MHz and 1.4 to 1.8 GHz bands, respectively. A single frequency synthesizer is used for LO generation and shared for both paths. The base band path is also shared, with gain controlled by digitally programmable gain amplifiers (PGA) before and after channel selection, which is performed by dual 6th order Chebyshev filters with on-chip auto-calibration loop to support different channel bandwidths from 5 to 8 MHz specified by DVB-T.

2.2 Frequency Synthesizer

In every mobile TV receiver, there is a frequency synthesizer to generate high accuracy LO frequency. Usually the frequency must also be varied in small, very precise steps. For instance, the channel spacing of GSM can be as small as 200 kHz centered at about 900 MHz. In other words, the LO frequency may be required to change by only 200 kHz to change from one channel to another. Also, the lower and upper edges of each channel are also well defined and could tolerate only very small an error. With lots of stringent requirements, synthesizer design still remains one of the challenging tasks in RF systems [21].

An RF synthesizer generates an output frequency given by \( f_{out} = f_0 + k f_{ch} \), where \( f_0 \) is the lower end of the frequency range while \( f_{ch} \) is the channel spacing. Both \( f_0 \) and \( f_{ch} \) are very well defined by the application. In order to meet the high accuracy, Phase-Locked Loops (PLL) are often used in a frequency synthesizer.
2.2.1 Synthesizer Architectures: Integer-N and Fractional-N

Similar to the design of a receiver, there are two types of frequency synthesizer scheme available: integer-N and fractional-N architectures.

Figure 2.5: Integer-N Frequency Synthesizer [21]

Figure 2.5 shows the scheme of an integer-N structure. A basic Phase-Locked Loop with Phase Detector (PD), Low Pass Filter (LPF) and Voltage Controlled Oscillator (VCO) is used as the basis for the synthesizer. Instead of having a unity feedback as in a basic PLL, a divider is used in the feedback chain. The division ratio $M$ is also called the modulus of the divider. The integer-N structure gets its name from the fact that the modulus, $M$, would change only from one integer to another.

From the system diagram, it is obvious that $f_{out} = M f_{REF}$. If $M f_{REF}$ is to be equal to $f_0 + k f_{ch}$, the $f_0$ should be equal to $f_{ch}$, because we have equation 2.1 for channel $k = 0$ and equation 2.2 for channel $k = 1$, which imply $f_0 = f_{ch}$.

\[ M_L f_{REF} = f_0 \quad (2.1) \]

\[ (M_L + 1) f_{REF} = f_0 + f_{ch} \quad (2.2) \]
The output frequency of the frequency synthesizer can then be changed by changing $M$, but by integer multiples of the reference frequency \cite{10} because $M$ has to be an integer. If finer resolution is required, i.e. a smaller $f_{ch}$, the only option is to reduce the reference frequency $f_{REF}$. There are a number of disadvantages, however, in reducing this reference frequency. It tends to reduce the maximum practical loop bandwidth, increasing the settling time of the PLL, and increase the noise contributed by VCO etc.

![Fractional-N Frequency Synthesizer with dual-modulus control](image)

Figure 2.6: Fractional-N Frequency Synthesizer with dual-modulus control \cite{21}

Figure 2.6 shows a basic fractional-N synthesizer. In “fractional” synthesizers, the output frequency can vary by a fraction of the input reference frequency \cite{21}. This is accomplished by realizing an equivalent “fractional” division ratio, such as $N.f$, where the dot denotes a decimal point and $N$ and $f$ represent the integer and fractional parts of the modulus.

Depicted in figure 2.6, such an synthesizer involves a dual-modulus prescaler, a circuit block that could divide by $N$ or $N + 1$ according to external control. If the prescaler divides by $N$ for $A$ output pulses of the VCO and $N + 1$ for $B$ output pulses, then the equivalent divide ratio is equal to:
\[
\frac{A + B}{A/N + B/((N + 1))}
\] (2.3)

The value of expression 2.3 can vary between \(N\) and \(N + 1\) in fine steps by proper choice of \(A\) and \(B\), which results to the "fractional" division ratio of \(N.f\).

With the help of the "fractional" division, the reference frequency \(f_{REF}\) no longer has to be tied to the channel spacing \(f_{ch}\). With a larger \(f_{REF}\) in the range of tens of megahertz, the loop bandwidth of a fractional-N synthesizer can be as high as a few megahertz, which could yield to a fast lock transient as well as suppressing the VCO close-in phase noise [21]. A larger \(f_{REF}\) also gives a smaller division ratio, which lowers the effect of the reference and Phase Detector Noise in the synthesizer [21].

### 2.2.2 Delta-Sigma Noise Shaping

The fractional-N synthesizer presented in section 2.2.1 is often considered as “bad” because of its poor phase noise performance [10]. There is a critical drawback in this practice of a corny periodic shift between modulus \(N\) and \(N + 1\). Each of the first \(A\) cycles of the divided signal is slightly shorter than the reference period. Consequently, the phase difference between the reference and the feedback signal grows in every period of \(f_{REF}\), until it returns to zero when divide by \(N + 1\) occurs. Eventually the phase detect and the LPF would produce a ramp waveform with a period of \(\frac{1}{(\alpha f_{REF})}\), if the equivalent division ratio is \((N + \alpha)\). Such a waveform would modulate the VCO, creating side bands at \(\alpha f_{REF}\), \(2\alpha f_{REF}\), etc [21]. Such sidebands are called fractional spurs.

Various methods of suppressing the spurs have been devised, such as fractional compensation [21]. Another approach is to randomize the choice of the modulus by
means of a Delta-Sigma modulator. The concept of noise randomization is depicted in figure 2.7.

The scheme is also called “noise shaping”. With the binary modulus control, for example \( b(t) \), generated by a Delta-Sigma modulator and takes the value of 0 or 1, the instantaneous division ratio can be written as \( N + b(t) \) with an average value of \( N + \alpha \). Thus, the bit stream could be seen as an average value \( \alpha \) plus a quantization noise \( q(t) \). It could be proved [21] that the quantization noise in the VCO output signal is well-defined by the spectrum of \( q(t) \), which is decided by the Delta-Sigma Modulator. With different orders and quantization levels in the modulator, the resulting noise spectrum could be ”shaped” such as the noise in the vicinity of the divider carrier is sufficiently small and noise gets concentrated at the higher offset, which is then suppressed by the low-pass filter in the PLL.

Detailed information on Delta-Sigma Modulation could be found in [23, 10, 21, 14].
2.3 Fractional-N Delta-Sigma Frequency Synthesizer for dual-band DVB-H application

In order to cover both European UHF band (470 to 862 MHz) and USA L band (1.670 to 1.675 GHz), the following frequency synthesizer shown in figure 2.8 is proposed [11].

The frequency synthesizer is a Fractional-N 2nd Order Type II Charge Pump PLL. The reference frequency is 40 MHz, and the PLL bandwidth is 35 kHz.

![Figure 2.8: Frequency Synthesizer Architecture for Dual-band DVB-H][11]

<table>
<thead>
<tr>
<th>Output Frequency</th>
<th>Band</th>
<th>VCO frequency</th>
<th>Output Path</th>
</tr>
</thead>
<tbody>
<tr>
<td>470–600 MHz</td>
<td>UHF</td>
<td>1.88–2.4 GHz</td>
<td>VCO → ÷2 → ÷2</td>
</tr>
<tr>
<td>600–825 MHz</td>
<td>UHF</td>
<td>1.8–2.475 GHz</td>
<td>VCO → ÷3</td>
</tr>
<tr>
<td>825–867 MHz</td>
<td>UHF</td>
<td>1.65–1.734 GHz</td>
<td>VCO → ÷2</td>
</tr>
<tr>
<td>1.670–1.675 GHz</td>
<td>USA-L</td>
<td>1.675–1.675 GHz</td>
<td>VCO</td>
</tr>
</tbody>
</table>

Table 2.1: Frequency Planning for European UHF and USA-L band
A single VCO is used to cover the dual band. The frequency is planned as in table 2.1. Output frequency in USA-L band, could be directed directly from VCO output. But the European UHF band needs more planning. But dividing the VCO output by two, three, or a cascade of divide by two, which equals an actual divide by four, the same VCO is used, saving the need for another VCO, which would occupy extra space on the chip and consumes extra power.

In this frequency synthesizer, there is a block called multi-modulus divider. It is basically a block that divides the VCO output frequency by certain modulus decided by the delta-sigma modulator bits. It is a key part in realizing the fractional division, which is unique to fractional-N architecture.

From the frequency synthesizer design, we could determine the range of division ratio of the multi-modulus divider needed. By dividing the VCO frequency by the PLL reference frequency, 40 MHz, we could get the required multi-modulus divider division ratio for each band, as shown in table 2.2.

<table>
<thead>
<tr>
<th>f plan</th>
<th>VCO range</th>
<th>f ref</th>
<th>Division Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>470–600 MHz</td>
<td>1.88–2.4 GHz</td>
<td>40 MHz</td>
<td>47–60</td>
</tr>
<tr>
<td>600–825 MHz</td>
<td>1.8–2.475 GHz</td>
<td>40 MHz</td>
<td>45–61.875</td>
</tr>
<tr>
<td>825–867 MHz</td>
<td>1.65–1.734 GHz</td>
<td>40 MHz</td>
<td>41.25–43.35</td>
</tr>
<tr>
<td>1.670–1.675 GHz</td>
<td>1.670–1.675 GHz</td>
<td>40 MHz</td>
<td>41.75–41.875</td>
</tr>
</tbody>
</table>

Table 2.2: Multi-modulus Divider Division Ratio Range

How to design the multi-modulus divider that fully covers these division range with optimal performance will be demonstrated in the next chapter.
CHAPTER 3

MULTI-MODULUS DIVIDER DESIGN

In the previous chapter of frequency synthesizers, we see the need for frequency dividers, also called prescalers. A frequency divider is employed in the Phase-Locked Loop to reduce the reference frequency and provide necessary programmability of the synthesizer, both in an integer-N or a fractional-N structure [21].

It is worth noticing that a frequency divider is one of the two only blocks in a frequency synthesizer that need to run at full speed. The other is the voltage-controlled oscillator (VCO) [6].

This chapter deals with the design of the multi-modulus divider in the frequency synthesizer proposed in section 2.3. We start with the system level architecture and hierarchy for the multi-modulus divider. Then we discuss the circuit design and implementation, schematic level simulation results, and layout efforts. Finally, we presents a brief comparison of this work with existing designs.

3.1 Divider Architecture and Hierarchy

A crucial aspects of the present-day consumer electronics industry are the short time available for the introduction of new products in the market. Short time-to-market demands architectures providing fast design time, simple layout work, and
easy optimization. Furthermore, from a high re-usability point of view, an architecture with easy adaption of the input frequency range, maximum and minimum division ratios is more desirable. For these reasons, we prefer a generic and fully-programmable architecture.

### 3.1.1 Generic Chain Architecture

The multi-modulus divider system architecture is depicted in fig 3.1. It consists of a chain of divide-by-2/3 dual-modulus prescalers in cascade, connected like a ripple counter [32].

![Multi-modulus Divider architecture](image)

**Figure 3.1: Multi-modulus Divider architecture**

The multi-modulus divider operates as follows. In every division period, the last cell of dual-modulus prescaler in the chain generates signal $mod_{n-1}$. This signal then propagates up the chain. An active $mod$ signal would enable the cell to divide by three once in a division cycle, as long as the programmable input bit $p$ is set to 1. In other word, the dual-modulus divide-by-2/3 cell would divide by three only ONCE in a whole deviation cycle, if it ever gets enabled to do so by having both the
programmability $p$ and the signal mod enabled. For the rest of the division cycle, the cell divide the input by two.

Thus, division-by-three action only adds one extra period of each cell’s input signal to the period of output signal. For example, each divide-by-three action in a cell with an 2.5 GHz (0.4ns period) input would introduce an extra 0.4 ns to the output period. The output period then becomes 1.2ns instead of 0.8 ns.

Applying the principle to the whole chain, the output period can be calculated as in equation 3.1 [32]:

$$T_{out} = 2^n \cdot T_{in} + 2^{n-1} \cdot T_{in} \cdot p_{n-1} + 2^{n-2} \cdot T_{in} \cdot p_{n-2} + \cdots + 2 \cdot T_{in} \cdot p_1 + T_{in} \cdot p_0 = (2^n + 2^{n-1} \cdot p_{n-1} + 2^{n-2} \cdot p_{n-2} + \cdots + 2 \cdot p_1 + p_0) \times T_{in}$$

(3.1)

In 3.1, $T_{in}$ is the period of the input signal, $p_0, \cdots, p_{n-1}$ are the binary programming bits for cell 1 to $n$ respectively. The equation shows that all integer division ratio ranging from $2^n$ to $2^{n+1} - 1$ can be realized. For example, for the former to happen, all $p_n$ should be set to zero, while that latter could be achieved by setting all $p_n$’s to one.

The modular architecture of figure 3.1 can be applied in the realization of programmable frequency dividers for fractional-N synthesizers, including those for dual-band DVB-H applications. As mentioned in chapter 2, a division ratio range of $41.25 \leq N \leq 61.875$ is needed. According to equation 3.1, five divide-by-2/3 cell will be sufficient, which would cover a range from 32 ($32 = 2^4$) to 63 ($63 = 2^5 - 1$). They multi-modulus divider circuit top level architecture is thus shown in figure 3.2 ($n = 5$).
3.1.2 Divider Hierarchy and Logic Implementation

The five cell chain architecture is the top hierarchy of the multi-modulus divider. Each cell in the chain is a divide-by-2/3 dual-modulus prescaler, which forms the next level of hierarchy. This section deals with the implementation of this dual-modulus prescaler cell.

Before we start the discussion on dual-modulus prescaler, it would be helpful to inspect the designs for dividers with constant division ratio.

A divide-by-two only circuit can be realized by two latches in a negative feedback loop [21]. Figure 3.3 shows the circuit configuration. A divide-by-three only circuit could be realized similarly with the aid of an extra AND gate, as shown in figure 3.4 [21].

A divide-by-2/3 circuit would require a control bit, which decides the moduli of the division. For example, the divide-by-three circuit in figure 3.4 could be converted into a dual-modulus divider by interposing an OR gate between the flipflops and before the AND gate, as shown in figure 3.5. The divider is then configured as a ÷2 circuit when $MC$ is high and a ÷3 circuit when $MC$ is low.
Based upon the fundamental structure mentioned above, a dual-modulus divide-by-2/3 prescaler cell could be realized with as in figure 3.6 [32].

The dual-modulus prescaler consists of two functional blocks, the prescaler logic and the end-of-cycle logic [32].

The prescaler logic block divides, upon control by the end-of-cycle logic, the frequency of the input clock by either two or three, and sends the divided output signal to the next cell in the chain. The end-of-cycle logic decides the instantaneous division ratio. The \( \text{mod}_{in} \) signal is active once in a division cycle. The enable signal of
programmability $p$ is checked at the moment $mod_{in}$ is active. Based on its status, the end-of-cycle would send or not send a feedback signal to prescaler logic cell to force it swallow one extra input clock period. It is also worth noticing that regardless of the
The logic implementation of the 2/3 divider cell requires D latches and AND gates. There are many designs for digital latches available, such as the built-in libraries offered by many standard CMOS process. But the multi-modulus divider chain in the frequency synthesizer serves to reduce the output frequency of the VCO to the reference frequency. Thus the input clock frequency for the first dual-modulus cell could be as high as 1.6 GHz to 2.5 GHz. Off the shelf digital blocks do not necessarily work under such high frequency. An appropriate circuit topology should be chosen to meet the high speed requirement.

3.2.1 High-Speed Digital Circuit Topologies

CMOS rail-to-rail logic is by far the most commonly used type of logic circuit [23]. However, standard rail-to-rail CMOS logic is not well suited for high frequency applications. Even though the static power consumption of CMOS is small, the higher operating frequency increases the dynamic power consumption during logic transitions. Thus the power consumption for CMOS goes up with the operating frequency. The large rail-to-rail output swing during logic transitions could also generate huge supply and substrate disturbance [32], making the topology less desirable for high speed circuits.
Current-mode logic (CML) emerged as an alternative approach to high speed digital circuits [1]. Unlike rail-to-rail CMOS, current-mode logic circuits use constant supply current and reduced differential voltage swing, which lead to low noise generation and constant power consumption, which makes it more efficient than rail-to-rail CMOS in high frequency applications.

Current-mode logic is based on a current-steering scheme. The basic MOS current mode logic (MCML) gate structure is shown in figure 3.7.

The current-steering approach works as follows [12]. A constant bias current $I$ is steered to one the circuit branches depending on the inputs to the differential pull down network. The ON branch, to which the current is steered, results in the low output voltage, whereas the OFF branches result in the high outputs. The high output is $V_{DD}$, while the low output is $V_{DD} - \Delta V$. $\Delta V$ is the voltage drop across the resistor $R$ ($\Delta V = I \times R$).
Figure 3.8: Current-mode Logic inverter / buffer circuit [12]

Hence, MCML logic circuits have the following characteristics [12]. First, it has a reduced voltage swing. Instead of switching from one supply rail to the other, MCML needs only a portion of the voltage swing $\Delta V$. The reduced swing leads to higher switching speed. Second, the power consumption of a MCML gate is relatively constant because of the use of a constant tail current in the differential pair. Third, MCML has a high noise immunity due to its differential structure.

Figure 3.8 shows a CML inverter or buffer, figure 3.9 shows a CML D Latch, and figure 3.10 gives some examples of general CML logic gates.

Other high speed digital circuit topologies are also available. For example, True Single-Phase-Clock (TSPC) circuit Techniques were also proposed [34]. Figure 3.11 shows a divider using TSPC scheme. TSPC employs a true single phase clock that
Figure 3.9: Current-mode Logic D Latch [21]

Figure 3.10: Current-mode Logic gates [12]. (a) XOR/XNOR (b) AND/NAND
is the only clock signal needed and never inverted, which avoids the usage of two non-overlapping two phase clocks and thus increase the speed.

Both CML and TSPC have been applied widely in prescaler design. TSPC topology is less complicated than CML and does not require a constant DC biasing current. However, TSPC is essentially a dynamic circuit. Dynamic dividers have undesirable high switching noise [26]. In addition, TSPC prescalers operate difficultly in high frequency due to the effects of charge rearrangement, circuit delay and the requirement of large voltage swing [28]. Therefore, the CML architecture is more suitable to implement high frequency division.

### 3.2.2 Current-mode Logic Circuit Design Parameters

The design of CML circuits involve a number of parameters, such as voltage swing $\Delta V$, Biasing Current $I_{BIAS}$ or $I_{TAIL}$, resistor $R$, total power consumption $P$, as well as the sizing of all the transistors in the circuit.

1. Voltage Swing $\Delta V$
The voltage swing, which is the peak value of the differential output of a CML gate/inverter, is expressed as [1]

\[ \Delta V = I \times R \] (3.2)

\( \Delta V \) is an important parameter. It has a reduced range compared to rail-to-rail CMOS logic. The smaller the swing under the same biasing and parasitic capacitance, the smaller the dynamic switching power the circuit would consume, even though the dynamic power consumption is not the dominant part of the total power consumption.

However, the \( \Delta V \) could not be set arbitrarily small. It should be large enough to full switch the following stage differential input. There is a fundamental input-output voltage-current relationship of a differential pair that decides the minimum swing to fully steer the tail current \( I_{TAIL} \) from one branch to the other. The minimal swing could be expressed as

\[ v_o = \sqrt{\frac{2I_{EE}}{\mu C_{ox}(W/L)}} \] (3.3)

The detailed derivation is presented in appendix A.

2. Biasing Current \( I_{BIAS} \)

The biasing current is closely related to the static power consumption. When steered from one branch to another, it generates voltage drops across the resistors on both branches.

3. Resistor \( R \)
Resistor $R$ in one branch should match the one in the other, just as the rest of corresponding components in the differential pair. There are a number of ways to implement resistors in the circuit. TSMC 0.18 1P6M process has built-it RF resistor module rphpoly_rf using rphpolywo_rf model for low resistance, and module rphripoly_rf using rphpolyri_rf model for relatively high resistance. Resistors generally occupy a much larger area compared to transistors, so it is not desirable to use large resistors in general.

4. Power Consumption $P$

The power consumption of CML circuits consists of two parts, a static portion and a dynamic one. There is a static power consumption regardless of the input because of the use of a constant biasing current. The dynamic power consumption accounts for the charging and discharging of parasitic capacitance, even though it is usually ignorable compared to the former [1] due to a reduced voltage swing.

3.2.3 Schematics and Power Scaling

After considering all the design variables, we start with a nominal voltage swing of 500 mV, which is typical in CML frequency divider [23]. A further increase of the voltage swing is not only a waste of power, but also impractical in an 1.8 V power supply environment. A substantial reduction in voltage swing, however, could lead to an incomplete current steering of the following stage.

In order to achieve the desired voltage swing, the resistor and the bias current should be set accordingly. As mentioned in section 3.2.2, the resistor has an upper limit in its value due to the limitation of the process. In addition, area and noise
considerations also stop us from making large resistors. Thus, even though we want to set the bias current as small as possible, it is usually set above a minimum value.

Another reason why bias currents are kept at a relatively high value is to maintain a high speed of operation. With the same amount of parasitic capacitance, a larger current would be able to charge and discharge the capacitors faster, which could be observed from equation 3.4:

\[ I = C \frac{dV}{dt} \]  

(3.4)

With capacitance C constant, the larger the bias current I is, the larger \( \frac{dV}{dt} \) becomes, which means a faster output waveform change, or a higher maximum operating frequency.

Finally, the bias currents are not set too high to stress the power budget. This is especially important for current mode logic circuits, whose dominant power consumption is the static form \( P_{\text{static}} = V \times I_{\text{BIAS}} \), which is directly related to the bias current value.

Therefore, we have a biasing plan shown in table 3.1. The biasing currents are scaled down from the first to the fifth. This is because the input frequency for each

<table>
<thead>
<tr>
<th>Cell</th>
<th>Norminal ( I_d(\mu A) )</th>
<th>Norminal load ( R(\Omega) )</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.5 GHz</td>
<td>1600</td>
<td>313</td>
</tr>
<tr>
<td>1.25 GHz</td>
<td>800</td>
<td>625</td>
</tr>
<tr>
<td>625 MHz</td>
<td>400</td>
<td>1.25 K</td>
</tr>
<tr>
<td>313 MHz</td>
<td>200</td>
<td>2.5 K</td>
</tr>
<tr>
<td>157 MHz</td>
<td>100</td>
<td>5 K</td>
</tr>
</tbody>
</table>

Table 3.1: Scaling of Currents in the 2/3 divider cells
cell is scaled down by the previous one. As a consequence, the maximum allowed delay increases as we move “down” the chain. Since the delay in a cell is inverse proportional to the cell’s current consumption, the currents in the cell may be scaled down as well to save power [32].

Figure 3.12: Divide-by-2/3 Prescaler Circuit Structure

The logic functions shown in figure 3.6 are implemented using Current-mode Logic (CML) topology presented in figure 3.12. Instead of having seven blocks in total (four D latches and three AND gates) as in figure 3.6, only four blocks exist in the structure.
Figure 3.13: AND_Latch: CML implementation of an AND gate combined with a D latch function

of figure 3.12, three of which are a combination of D latch and the AND gate at the D input. The combined \textit{AND\_Latch} circuit is showing in figure 3.13. The regular D latch implemented in CML without AND gate is shown in figure 3.14.

3.3 Simulation Results

The multi-modulus divider is designed in TSMC 0.18 $\mu m$ 1P6M CMOS process. Transient simulation, noise analysis, corner simulation, and Monte Carlo statistic simulation results are presented in this section.
Figure 3.14: Latch: CML implementation of a D Latch
3.3.1 Transient Simulations

The basic function of the Multi-modulus divider is to divide the input signal by the designated moduli. From equation 3.1 we can infer that in the case of \( n = 5 \), \( p_0, p_1, \ldots, p_4 \) are the binary control bits with \( p_4 \), the modulus control for cell 5, as the MSB and \( p_0 \), the modulus control for cell 1, as the LSB.

The rank of the modulus control bits can also be understood from the input frequency down scale along the chain. With cell 1 facing the highest input frequency, its extra input clock period added to the final output by an active divide-by-three
Figure 3.16: Transient Simulation for divide-by-63 mode at 2.5 GHz
action is the shortest, thus its modulus change should have the least influence on overall frequency division ratio, i.e., \( p_0 \) should be the LSB. On the contrary, cell 5 operates at the lowest frequency. The extra input period added by its divide-by-three action would add a substantially longer time period to the output signal, thus \( p_4 \) is the MSB in the binary modulus control bits.

It is important to notice that a divide-by-three action involves the most time delay [32]. There is a maximum delay between the \( \text{mod}_{in} \) and the clock signal in a given cell that still allows properly timed division by three. Therefore, division ratios that involve divide-by-three actions of the dual-modulus prescalers are the critical testing points. In a five-cascade chain, divide-by-63 is a case when every 2/3 prescaler is enabled for divide-by-three mode once in every division cycle. Therefore transient simulation on divide-by-63 serves as major test point in the multi-modulus testbench. Figure 3.15 is the top level testbench for the multi-modulus divider.

Figure 3.16 shows the output waveform of the first 200 ns under 2.5 GHz input, the highest required operating frequency, as well as every intermedia output waveform for each divide-by-2/3 prescaler cell. It could be seen from the waveform that in a divide-by-63 mode, all the prescalers except the last, which is set to divide by three only, toggle back and forth between divide-by-two and divide-by-three actions.

The output waveform period is measured to be 25.2 ns (25.2ns = 0.4ns \( \times \) 63). Averaging five, ten, or even more successive periods lead to almost identical results.

A full list of output period measurement results at 2.5 GHz input for division ratio from 40 to 63 is shown in table 3.2.
<table>
<thead>
<tr>
<th>Division Ratio</th>
<th>No.Msmt</th>
<th>T(averaged)</th>
<th>T(theoretic)</th>
</tr>
</thead>
<tbody>
<tr>
<td>32</td>
<td>35</td>
<td>12.800 ns</td>
<td>12.8 ns</td>
</tr>
<tr>
<td>33</td>
<td>35</td>
<td>13.200 ns</td>
<td>13.2 ns</td>
</tr>
<tr>
<td>34</td>
<td>35</td>
<td>13.599 ns</td>
<td>13.6 ns</td>
</tr>
<tr>
<td>35</td>
<td>35</td>
<td>14.000 ns</td>
<td>14.0 ns</td>
</tr>
<tr>
<td>36</td>
<td>35</td>
<td>14.400 ns</td>
<td>14.4 ns</td>
</tr>
<tr>
<td>37</td>
<td>30</td>
<td>14.800 ns</td>
<td>14.8 ns</td>
</tr>
<tr>
<td>38</td>
<td>30</td>
<td>15.200 ns</td>
<td>15.2 ns</td>
</tr>
<tr>
<td>39</td>
<td>30</td>
<td>15.600 ns</td>
<td>15.6 ns</td>
</tr>
<tr>
<td>40</td>
<td>30</td>
<td>16.000 ns</td>
<td>16.0 ns</td>
</tr>
<tr>
<td>41</td>
<td>30</td>
<td>16.401 ns</td>
<td>16.4 ns</td>
</tr>
<tr>
<td>42</td>
<td>30</td>
<td>16.800 ns</td>
<td>16.8 ns</td>
</tr>
<tr>
<td>43</td>
<td>30</td>
<td>17.200 ns</td>
<td>17.2 ns</td>
</tr>
<tr>
<td>44</td>
<td>30</td>
<td>17.599 ns</td>
<td>17.6 ns</td>
</tr>
<tr>
<td>45</td>
<td>25</td>
<td>18.000 ns</td>
<td>18.0 ns</td>
</tr>
<tr>
<td>46</td>
<td>25</td>
<td>18.399 ns</td>
<td>18.4 ns</td>
</tr>
<tr>
<td>47</td>
<td>25</td>
<td>18.800 ns</td>
<td>18.8 ns</td>
</tr>
<tr>
<td>48</td>
<td>25</td>
<td>19.200 ns</td>
<td>19.2 ns</td>
</tr>
<tr>
<td>49</td>
<td>25</td>
<td>19.600 ns</td>
<td>19.6 ns</td>
</tr>
<tr>
<td>50</td>
<td>20</td>
<td>20.000 ns</td>
<td>20.0 ns</td>
</tr>
<tr>
<td>51</td>
<td>20</td>
<td>20.400 ns</td>
<td>20.4 ns</td>
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<td>52</td>
<td>20</td>
<td>20.799 ns</td>
<td>20.8 ns</td>
</tr>
<tr>
<td>53</td>
<td>20</td>
<td>21.200 ns</td>
<td>21.2 ns</td>
</tr>
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<td>54</td>
<td>20</td>
<td>21.600 ns</td>
<td>21.6 ns</td>
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<td>20</td>
<td>22.000 ns</td>
<td>22.0 ns</td>
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<td>56</td>
<td>20</td>
<td>22.401 ns</td>
<td>22.4 ns</td>
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<td>57</td>
<td>20</td>
<td>22.800 ns</td>
<td>22.8 ns</td>
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<td>23.200 ns</td>
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<td>20</td>
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<tr>
<td>61</td>
<td>20</td>
<td>24.400 ns</td>
<td>24.4 ns</td>
</tr>
<tr>
<td>62</td>
<td>10</td>
<td>24.799 ns</td>
<td>24.8 ns</td>
</tr>
<tr>
<td>63</td>
<td>10</td>
<td>25.200 ns</td>
<td>25.2 ns</td>
</tr>
</tbody>
</table>

Table 3.2: Frequency Division: Theoretic vs Measured at 2.5 GHz input
3.3.2 Noise Simulation

A major advantage of current mode logic is its relatively low noise compared to other topology. The phase noise generated by the divider can affect the synthesizer noise performance [15].

Two types of simulations in Cadence Analog Design Environment are run: Periodic Steady-State Analysis (PSS) and Periodic Noise Analysis (Pnoise). The PSS analysis computes the periodic steady-state response of a circuit. It determines the circuit’s periodic operating point which is required starting point for Pnoise. Pnoise
analysis then linearizes the circuit around the periodic operating point and computes the resulting noise performance [4].

Figure 3.17 is the testbench for output noise simulation of the multi-modulus divider. Figure 3.18 shows the output phase noise of the divider at 10 kHz to 10 MHz frequency offset. The flicker noise corner is around 1 MHz offset, and the white noise floor is less than or equal to -145 dBC/Hz.
<table>
<thead>
<tr>
<th>Component Models</th>
<th>Voltage Supply</th>
<th>Temperature</th>
<th>Max. Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>FF</td>
<td>1.92 V</td>
<td>-10 °C</td>
<td>≥ 2.5 GHz (100 %)</td>
</tr>
<tr>
<td>TT</td>
<td>1.8 V</td>
<td>27 °C</td>
<td>2.5 GHz (100 %)</td>
</tr>
<tr>
<td>TT</td>
<td>1.8 V</td>
<td>57 °C</td>
<td>2.3 GHz (92 %)</td>
</tr>
<tr>
<td>TT</td>
<td>1.62 V</td>
<td>27 °C</td>
<td>2.3 GHz (92 %)</td>
</tr>
<tr>
<td>SS</td>
<td>1.8 V</td>
<td>27 °C</td>
<td>2.3 GHz (92 %)</td>
</tr>
<tr>
<td>SS</td>
<td>1.62 V</td>
<td>57 °C</td>
<td>1.9 GHz (76 %)</td>
</tr>
</tbody>
</table>

Table 3.3: Maximum Operating Frequency under Different Process Corners

### 3.3.3 Corner Simulation

TSMC 0.18 μm CMOS process CDK contains detailed information about its RF and baseband MOSFET as well as resistor, inductor, capacitor, varactor BSIM3 (V3.24) models. In addition to nominal parameters, which is typical N typical P, Fast N Fast P, Slow N Slow P, Fast N Slow P, and Slow N Fast P corner models are also available for MOSFETs. TT, FF and SS corner models for other circuit components are also included, which gives designers options to simulate circuits in a number of different scenarios.

As mentioned in section 3.3.1, divide-by-63 enables all the divide-by-2/3 cells for divide-by-three action, which involves the most delay in terms of internal transmission delay and contingent block feedbacks. Thus, divide-by-63 mode at 2.5 GHz maximum input frequency is selected for comparison among all corners.

Fast corners and conditions, as well as nominal, or typical circuit parameters all generate correct input output division ratio and frequency relationship. However, slow corners demonstrate different degrees of slow down in speed, as shown in table 3.3. The worst case is when device shifts to slow corner, voltage supply drops and
temperature rises at the same time, in which the multi-modulus divider lose as much as 30% of its nominal operating speed.

### 3.3.4 Statistic Simulations

The manufacturing variations in components, including process variations and mismatches, affect the production yield of any design that includes them. Monte Carlo simulation of Cadence Design System provides a platform to study this influence in details.

Monte Carlo simulation is a statistic simulation that specifies the possible range that device models, process variations and mismatches etc would vary. It runs multiple statistic independent runs with parameters picked from the range randomly with the identical distribution from run to run. TSMC PDK includes Monte-Carlo model files for MOSFET’s that could be used for Monte Carlo simulations. External parameters such as temperature and voltage supply are varied among a list of specific values.

In order to guarantee proper operation across process, voltage supply and temperature variations, a Monte Carlo analysis is performed on both transient and DC operating point simulation. Alterations on both temperature (27 °C, -10 °C, 57 °C) and voltage supply (1.8 V, 1.62 V and 1.98 V) are applied.

Figure 3.19 shows the transient behavior of the Multi-modulus Divider output waveform at maximum moduli (divide-by-63 mode) with a 1.6 GHz sinusoid signal as the input. The start up time of each run differs, but the output period stays the same as 39 ns.
Figure 3.19: Monte Carlo Transient Analysis at 1.6 GHz
Figure 3.20: Monte Carlo Transient Analysis at 2.5 GHz
Figure 3.21: Biasing Current Distribution under temperature variations

<table>
<thead>
<tr>
<th>Temperature</th>
<th>Variations</th>
</tr>
</thead>
<tbody>
<tr>
<td>27°C</td>
<td></td>
</tr>
<tr>
<td>-10°C</td>
<td></td>
</tr>
<tr>
<td>57°C</td>
<td></td>
</tr>
</tbody>
</table>

Statistical Analysis Results: Temperature Sweep

- Tail 1: 1.5359, sd 25.1975, n 20
- Tail 2: 793.269, sd 14.9178, n 70
- Tail 3: 290.075, sd 7.56536, n 70
- Tail 4: 92.852, sd 3.65631, n 70
- Tail 5: 39.801, sd 1.8537, n 70
Figure 3.22: Biasing Current Distribution under voltage supply (1.8 V, 1.62 V and 1.98 V) variations.
Figure 3.20 shows the waveform at maximum moduli (divide-by-63 mode) with 2.5 GHz sinusoid signal input. With process variation, mismatch, voltage, temperature selected randomly in a range, the output waveforms do not all satisfy the design requirement. A few runs have less than expected period due to the missing of divide-by-3 function because of the slowdown of the circuit.

Figure 3.21 shows the distribution of the biasing current of each divide-by-2/3 prescaler under temperature variations. Most of the distributions are in a bell curve, with an exception for dual-modulus prescaler cell five under 1.92 Voltage supply, which shows a slightly off distribution to the lower side. The standard deviation of the biasing current, which is in the order of 30 µA, partly explained the existence of a few transient simulation results that are off. In a current mode logic, the deviation of biasing current high frequency cells directly translates to a variation of voltage swing, which substantially influence the correctness of logic operation of the following stages.

3.4 Layout Efforts and Physical Verification

A complete VLSI design cycle involves efforts in three distinctive domains: behavioral, structural, and physical. So far, we have conducted design in both behavioral and structural domains. In section 3.1, the multi-modulus divider design is done in the behavioral domain, which describes the functions of the divider and how it is partitioned into different units (a chain of dual-modulus divide-by-2/3 prescalers). In section 3.2, the design goes into structural domain where we look at how the functional units are constructed (prescaler logic and end-of-cycle logic), how transistors are used to implement the logic (the choice of MOS Current-mode Logic), and how
the circuit are tailored to emphasize low power (the scaling of bias current in the cells).

However, physical design is indispensable for a complete VLSI design cycle. Physical design describes the layout of the chip [33]. The layout of an integrated circuit defines the geometries that appear on the masks used in fabrication [22]. The geometries include n-well, active, polysilicon, implants, interlayer contacts, and metal layers etc. While device scaling has enhanced the raw speed of transistors, unwanted interaction between different sections in the layout limit the speed and precision of the integrated circuit [22]. So it is important to study these undesirable influences through layout efforts and post-layout simulations.

AMI 0.6 \( \mu m \) CMOS process is one of the many processes available for chip fabrication at the Ohio State University. Since the architecture of the multi-modulus divider described in section 3.1 is generic, and the principles of current-mode logic remain valid regardless of the fabrication process, we migrated the circuit to AMI 0.6 \( \mu m \) CMOS process in order to verify the design methodology and probe the influences caused by layout. For the rest of this chapter, the layout design and simulation results refer to the ones conducted in AMI 0.6 \( \mu m \) process if not specified otherwise.

### 3.4.1 Layout Efforts

AMI Semiconductor 0.50 Micro C5 is a family of mixed-signal foundry process with 3 metal layers, 2 poly layers, and a high resistance layer suitable for 5 volt applications [24]. It is widely used for digital circuits. The process supports both vendor native rules, i.e. rules that are specific to this process, and vendor-independent, MOSIS Scalable CMOS (SCMOS) rules. The SCMOS rules are a common set of
rules widely supported by MOSIS that intend to simplify and unify the layout design and verification process. Circuit geometries are specified in the Mead and Conway’s lambda based methodology [16].

Even though specific vendor’s layers and design rules usually lead to denser layouts, they also yield designs that are less likely to be directly portable to another process. [16] SCMOS rules allow us to work on abstract layer and metric units “lambda”, which is associated to the feature size of the process. The minimum MOSFET channel length is defined to be equal to $2\lambda$. In AMI C5 process family, “lambda” is equal to 0.3 $\mu$m. Therefore, the minimum channel length is 0.6 $\mu$m.

Figure 3.23 shows the layout of the $AND\_Latch$ cell in the first dual-modulus prescaler cell. In addition to the basic design rules imposed by MOSIS, additional layout strategies were applied for better performance of the circuit.

1. Source Sharing. CML circuits primarily consist of differential pairs. A good matching of the MOSFET transistors is very helpful. Therefore, NMOS transistors in all three input differential pairs and the fourth pair in feedback connection share the source terminals through overlapping. This practice reduces the layout area, and it also avoids asymmetries, which would introduce input-referred offsets in fully differential circuits [22].

2. Arrays of Substrate Taps. The n-wells for PMOS transistors need to be connected to $V_{DD}$, the highest voltage in the circuit, while the bodies for NMOS transistors need to connected to $GND$, the lowest voltage potential, which are to ensure the S/D junction diodes remain reverse-biased under all conditions [22].
Figure 3.23: Layout of an AND_Latch in AMI C5N process
Instead of using a single n-well tap or substrate tap, an array of taps are used to reduce the equivalent resistance of the connection, which leads to less undesirable voltage drop from power rails to the actual MOSFET terminals.

3. Metal wiring. AMI C5N process has three layers of metal for all interconnection. In order to use them efficiently, a stick diagram (not included in the thesis) is sketched before the actual layout of any circuit or sub-circuit unit is conducted. In this design, Metal 1 and Metal 2 are used for intra circuit connection, with Metal 1 in the horizontal orientation and Metal 2 in the vertical orientation. Metal 3 is left for inter circuit interconnection and feedbacks.

The layout of a CML D latch is similar to the one shown in figure 3.23 except for the absence of intermediate pitch in AND_Latch, which is required for AND logic but not present in a simple D latch layout.

Finally, it is important to consider the necessary output buffers for a chip in order to properly drive inevitable loads and capacitance associated with measurements and testing. A typical input capacitance of measuring cable is around 40 to 60 pF. Therefore, we designed our output buffer to drive up to 60 pF off chip capacitance.

Figure 3.24 is the output driving stage of the multi-modulus divider. The input operational amplifier converts the differential input signals to a single-ended output signal. The two source followers act as output buffers as well as voltage level shifters. By increasing the sizes of the driving NMOS’s and the biasing currents, the buffer could gain the required driving capability.

Figure 3.25 shows the final layout of a two-bit multi-modulus divider in a Tinychip area (1.5mm × 1.5mm). Hi-ESD (ElectroStatic Discharge) protection pad frame was used for the chip.
3.4.2 Physical Verification

After the layout creation is completed, we start the process of physical verification. Generally, the physical verification procedures can be divided into three parts: the Design Rule Check (DRC), Layout Versus Schematic check (LVS), and paRasitiC eXtraction (RCX) [27]. DRC check makes sure the layout does not violate any design rule. LVS ensures each device in the layout is completely matched to its corresponding component in the original schematic. RXC extracts the parasitic R and C, which is needed for post-layout simulation.
Figure 3.25: Two-bit Multi-modulus Divider Chip in a Tinychip area
Figure 3.26: Extracted View of the same AND_Latch
Figure 3.26 shows the extracted view of the same AND\_Latch cell illustrated in figure 3.23. All the parasitic capacitance values are illustrated between the corresponding terminals. The order of the parasitic capacitance is around several fempto Fara. For example, at node +63 and +70, the gate capacitance is 3.09 fF, which is consistent with the typical process parameters provided by MOSIS, which indicates that Poly and N diffusion overlap capacitance is around 2430 \( aF/\mu m^2 \) in AMI C5 processes, or 2.2 fF in total for a 1.5\( \mu m \) by 0.6\( \mu m \) size NMOS transistor \( (2.43 fF/\mu m^2 \times (1.5 \mu m \cdot 0.6 \mu m) = 2.187 fF) \).

After the paddings and the frame are included, the whole chip is extracted with parasitic capacitance. Simulation is rerun on the extracted file. Figure 3.27 shows the transient simulation of the chip after extraction. The two-bit multi-modulus divider is able to divide by 4, 5, 6, and 7 according to the two control bits \( Ct1 \) and \( Ct2 \).

The main difference between schematic level simulation and post-layout simulation in this case is the difference of their maximum operating frequencies. At schematic level, the multi-modulus divider would be able to run at 250 MHz. After layout extraction, the maximum operating frequency is only 130 MHz. Junction capacitance, interconnection capacitance and resistance all contribute to the extra RC delay that is not included at schematic level simulation. The total chip power consumption also goes up from 4 mW to 14.6 mW after extraction and with off-chip capacitive load, which shows the huge amount of dynamic power consumed in charging and discharging the parasitic capacitance, a significant power burden otherwise unrevealed by the schematic level simulations.

The post layout delay is substantial. One of the reasons could be that AMI C5N process does not provide enough protection for transistors operating in high
Figure 3.27: Post-layout transient simulation of the Multi-modulus Divider Chip at 100 MHz input
frequencies. There is no guard ring around MOSFET, which makes the transistor more susceptible to digital switching noise. The lack of triple well structure also makes MOSFET’s vulnerable to substrate noise coupling. As a result, AMI C5N process is not the first choice for commercial high frequency design or fabrication.

3.5 Comparison with Other Work

Over the years, many dual-modulus and multi-modulus frequency dividers have been proposed in the literature. Table 3.4 include a few of the existing designs of frequency divider that operates at similar frequency or bear similar application purposes.

<table>
<thead>
<tr>
<th></th>
<th>Frequency</th>
<th>Division Ratio</th>
<th>Power</th>
<th>Tech Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>JSSC[6]</td>
<td>1.75 GHz</td>
<td>128/129 dual</td>
<td>24 mW</td>
<td>0.7-µm CMOS</td>
</tr>
<tr>
<td>JSSC[15]</td>
<td>3 GHz</td>
<td>32/33 dual</td>
<td>27 mW</td>
<td>0.35-µm CMOS</td>
</tr>
<tr>
<td>JSSC[32]</td>
<td>1.4–1.8 GHz</td>
<td>511 to 1023</td>
<td>4.4 mW</td>
<td>0.35-µm CMOS</td>
</tr>
<tr>
<td>[28]</td>
<td>2.4 GHz</td>
<td>256 to 271</td>
<td>28 mW</td>
<td>0.35-µm CMOS</td>
</tr>
<tr>
<td>[26]</td>
<td>2.4–2.48 GHz</td>
<td>481 to 496</td>
<td>9 mW</td>
<td>0.18-µm CMOS</td>
</tr>
<tr>
<td>JSSC[8]</td>
<td>20–21 GHz</td>
<td>256 to 263</td>
<td>9 mW</td>
<td>0.13-µm CMOS</td>
</tr>
<tr>
<td>This work</td>
<td>1.6–2.5 GHz</td>
<td>32 to 63</td>
<td>23.3 mW</td>
<td>TSMC 0.18 CMOS</td>
</tr>
</tbody>
</table>

Table 3.4: Comparison with Existing Designs

From table 3.4, we see that our design is comparable with existing literatures, except for a relatively high power consumption compared to designs on similar technologies. This is certainly an area that could be improved in future work.
CHAPTER 4

CONCLUSIONS AND FUTURE WORK

We have successfully shown in Chapter 3 how a Multi-modulus Divider can be designed for a Delta-Sigma Fractional-N frequency synthesizer for dual-band DVB-H receiver. Five divide-by-2/3 dual-modulus prescalers were placed in cascade to cover the division ratio range of 32 to 63. Current mode logic circuit topology was used for high speed division.

Layout efforts of a 2-bit Multi-modulus divider in AMI C5N process were also shown. Post layout simulation confirmed the multi-modulus division functionality as well as the current mode logic circuit principles, though a substantial slowdown in maximum operating speed was detected due to the parasitic effects. Possible reasons for the speed loss were explained.

A lot of work can still be done on this topic, such as further power reduction and physical verification in an RF-friendly triple-well process. These can be pursued in future Ph.D. studies.
APPENDIX A

THE DERIVATION OF MINIMUM VOLTAGE SWING FOR COMPLETE CURRENT STEERING IN CML GATES

This appendix is intended to show the minimum input differential voltage needed to fully steer the tail current from one branch of a current mode differential pair to the other.

![Figure A.1: CMOS differential pair and its current-voltage relationship](image)

\[ V_{1\text{max}} = \frac{2i_{EE}}{\sqrt{\mu COX \left( \frac{W}{L} \right)}} \]

Figure A.1: CMOS differential pair and its current-voltage relationship [23]
The basis for all CML is the differential pair [23]. In figure A.1, the tail current as a function of drain currents can be written as:

\[ I_{EE} = i_D^1 + i_D^2 \] (A.1)

The input voltages can be written as the sum of gate-source voltages:

\[ v_1 = v_{GS1} - v_{GS2} \] (A.2)

The simple square law voltage-current relationship for a CMOS transistor is [22]:

\[ i_D = \frac{\mu C_{ox}}{2} \left( \frac{W}{L} \right)(v_{GS} - v_{TH})^2 \] (A.3)

which can be written as:

\[ v_{GS} = \sqrt{\frac{2}{\mu C_{ox}} \left( \frac{L}{W} \right)} \sqrt{i_D} + v_{TH} \] (A.4)

Therefore, equation A.2 can be written as

\[ v_1 = \sqrt{\frac{2}{\mu C_{ox}} \left( \frac{L}{W} \right)}(\sqrt{i_D^1} - \sqrt{i_D^2}) \] (A.5)

Now, making use of equation A.1,

\[ v_1 = \sqrt{\frac{2}{\mu C_{ox}} \left( \frac{L}{W} \right)}(\sqrt{i_D^1 - I_{EE}}) \] (A.6)

Squaring both sides of A.6, collecting terms, we could get

\[ \frac{16}{(\mu C_{ox})^2} \left( \frac{L}{W} \right)^2 (I_{EE}i_D - i_D^1)^2 = \frac{4}{(\mu C_{ox})^2} \left( \frac{L}{W} \right)^2 I_{EE}^2 - \frac{4}{\mu C_{ox}} \left( \frac{L}{W} \right) I_{EE} v_1^2 + v_1^4 \] (A.7)
This can be solved for $i_{D1}$ [23]:

$$i_{D1} = \frac{I_{EE}}{2} \left[ 1 \pm \sqrt{\frac{2I_{EE}}{\mu C_{ox} \left( \frac{W}{L} \right)}} - \frac{(\mu C_{ox})^2}{4I_{EE}^2} \left( \frac{W}{L} \right)^2 v_1^2 \right]$$

(A.8)

The term inside the brackets will have a peak value of two at some input voltage of $v_{1_{\text{max}}}$. This voltage can be determined by setting the derivative of A.8 to zero, and the result is given by

$$v_{1_{\text{max}}} = \sqrt{\frac{2I_{EE}}{\mu C_{ox} \left( \frac{W}{L} \right)}}$$

(A.9)

Where the input differential voltage reaches $v_{1_{\text{min}}}$, the tail current $I_{EE}$ is completely switched to one branch or the other. For larger differential voltage swing, one branch continues to take all the current and the other side just becomes more firmly off. In real circuits, for larger $v_1$, the source voltage then starts to follow input voltage, limiting the effective differential input as $v_{1_{\text{max}}}$ [23].

As a result, $v_{1_{\text{max}}}$ is the minimum voltage swing for complete current steering. When CML gates are in cascade, the output swing of the previous stage should be larger or equal to this value to ensure the full switching of its following stages.
APPENDIX B

VERILOG HDL SOURCE CODE FOR DUAL-MODULUS PRESCALER

The following is a list of Verilog HDL code used for behavioral simulation of the divide-by-2/3 dual-modulus prescaler.

Module Div23 is the behavioral block for divide-by-2/3 prescaler.

```verilog
module Div23 (modin, fin, modout, fout, P, rst);
    input modin, fin, P, rst;
    inout modout, fout;
    wire d1, qb1, q2, qb2, d3, qb3, d4, q4, qb4;
    wire modout, fout;

    and (d3,q2,modin);
    and (d4,modout, P);
    and (d1,qb2,1'b1);
    latch D1(fout, qb1, d1, fin, rst),
        D2(q2, qb2, fout, ~fin, rst),
        D3(modout, qb3, d3, fin, rst),
        D4(q4, qb4, d4, ~fin, rst);
endmodule
```

Among the submodules called, `latch` is the module for a D Latch.

```verilog
module latch(Q, Qb, D, clk, rst);
    input D, clk, rst;
    output Q, Qb;
    reg Q;
endmodule
```
wire Qb;

always @ (clk or rst or D)
begin
  if(!rst) Q <= 1'b0;
  else if(clk)
    Q <= D;
end
assign Qb = ~Q;
endmodule

A simple test bench is needed to provide the driving clock and output waveforms.

`timescale 100ps / 100ps
'define Tclk 4
'define TMod 112
module test();
  reg fin, modin, rst, P;
  wire fout, modout;
  Div23 cell1( .modin(modin),
    .fin(fin),
    .modout(modout),
    .fout(fout),
    .P(P),
    .rst(rst) );

  initial begin
    fin <= 1'b0;
    rst <= 1'b0;
    modin <= 1'b1;
    P <= 1'b1;
    #5 rst <= 1'b1;
  end
  initial forever
    #Tclk fin <= ~fin;
  initial forever
    #TMod modin <= ~modin;
endmodule
The figure B.1 shows the input output signals of module Div23. During the time when $mod_{in}$ is high, the output stays high for two input clock period and goes low for the next input clock period, generating an equivalent divide by three action, as described in section 3.1.2.
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