CIRCUIT AND SYSTEM DESIGN FOR FULLY INTEGRATED CMOS DIRECT-CONVERSION MULTI-BAND OFDM ULTRA-WIDEBAND RECEIVERS

DISSERTATION

Presented in Partial Fulfillment of the Requirements for the Degree Doctor of Philosophy in the Graduate School of The Ohio State University

By

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* * * * *

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2007
Ultra-WideBand (UWB) technologies are widely accepted as the center piece of ubiquitous wireless interconnects for next generation Wireless Personal Area Networks (WPAN). It finds potential exciting applications in high-connectivity and high-interoperability multimedia consumer products within personal operating space, such as wireless home video distributions systems, and high-speed, high-mobility cable replacement solutions, such as Wireless Universal Serial Bus (W-USB) and wireless IEEE-1394 Firewire. Many active academic and industrial works have been dedicated to the implementation of UWB transceivers, however, a monolithic UWB radio expanding across full 3.1–10.6 GHz UWB spectrum is yet to be accomplished.

Targeting Multi-Band Orthogonal Frequency Division Multiplexing (MB-OFDM) UWB, one of the two major competing industrial UWB standards, this dissertation focuses on system and circuit co-design of a fully integrated CMOS direct-conversion transceiver, with emphasis on architectural issue, frequency planning, and circuit topologies of its RF front-end and frequency synthesizer.

This dissertation extends prior wireless channel analysis on three mandatory frequency bands to full UWB spectrum, and derives general system parameters including sensitivity, system gain, noise figure, IIP$_3$, IIP$_2$, local oscillator (LO) phase noise, and spurious tone rejections for UWB receivers. Subsequent receiver budget analysis
leads to the specifications of each individual functional block along the analog signal receiving chain.

Based upon system-level design, two different RF front-end architectures are implemented using a 0.18-μm 1P6M CMOS technology. The first front-end consists of a single-ended common-gate low-noise amplifier (LNA) with tunable LC-tank load and a class-AB downconversion mixer with an embedded balanced-unbalanced converter (balun). In the second one, a classical inductively-degenerated common-source differential LNA with a bandwidth-expanding feedback loop is followed by a current-injected double-balanced mixer stage. The two structures clearly reflect the trade-offs in UWB RF front-end design.

A novel “two-step” frequency generation scheme and its associated frequency synthesizer architecture are also proposed in this dissertation. This scheme can provide all MB-OFDM UWB bands with only two frequency mixing steps. Analysis on its phase noise and parasitic frequency spur performance justifies its effectiveness.
This dissertation is dedicated to my family and friends.
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CHAPTER 1

INTRODUCTION

1.1 Background and Motivation

The late 20\textsuperscript{th} century and early 21\textsuperscript{st} century witnessed the rapid growth of wireless communication industry. While mobile cellular telephone technologies move progressively from the third generation (3G) towards the fourth generation (4G), many other standard-based wireless technologies spring up aiming at a wider variety of applications. Figure 1.1 shows some well established or emerging wireless communication technologies, such as WLAN, WiMAX/WiBro/Wireless MAN, RFID and UWB. Transmission distance of these representative applications ranges from tens of centimeters (passive RFID transponder ICs) to tens of kilometers (10–66 GHz line-of-sight WiMAX transceivers), and the data rate can be as low as 1.65 kbps (downlink from RFID interrogator to tag at 13.58 MHz) and as high as sub-Gb/s (data exchange between ultra-wideband terminals). Among these technologies, ultra-wideband (UWB) is widely accepted as the key interconnection technique for next-generation wireless personal area networks (WPAN), especially low cost, low power and high data rate applications, such as high-quality multimedia streaming and large digital file transferring.
In order to comply with international regulations and co-exist with other wireless applications such as GPS, UWB systems realize high data rate with a large fractional bandwidth and a low transmission power level. In conventional narrow-band radio designs, the requirement of large bandwidth is in conflict with another important requirement, low power dissipation. This makes the circuit implementation of UWB radio a very interesting and challenging topic for many active state-of-the-art academic and industrial researches.

Meanwhile, low cost and small form factor are crucial for the market success of UWB technologies. As development of advanced microfabrication technologies allows minimum transistor device feature size to shrink down to deep sub-micron and nanometer scales, the increasing level of system integration reduces the cost of silicon
system-on-chip (SOC) continuously. It turns out that off-chip RF components including RF filters, baluns or power amplifiers (PA) become the limiting factor for further cost reduction. Therefore, it is highly desirable to integrate all external components on chip by exploiting system-level architectures and individual RF block topologies.

1.2 Research Objectives and Scope

This dissertation investigates and explores the architectural trade-offs and practical circuit design issues for monolithic UWB receivers on CMOS technology. More specifically, concentrations are devoted to the relations between system-level parameters and CMOS circuit implementation of RF front-ends to minimize off-chip RF components. Frequency synthesizer architectures are also studied to meet the stringent requirements on settling time, phase noise and spur levels.

The first and ultimate objective of this research is to work towards a fully integrated CMOS MB-OFDM UWB receiver. Because the block topologies and specifications are determined by system analysis and design, it is critical to understand how fundamental system issues such as interferers, modulation and multiple access schemes affect receiver architecture and circuit implementations. Therefore, the basic idea of this research is to treat circuit design and system analysis as an integrated design flow so that an optimal architecture can be obtained.

Another important design goal is to enable the entire available UWB bandwidth of 3.1–10.6 GHz to be utilized. This requires an extremely broadband receiver RF front-end capable of amplifying and frequency-translating input signals across 7.5 GHz frequency band, as well as a viable frequency plan and a powerful frequency synthesis scheme to contain the frequency hopping nature of multi-band OFDM UWB system.
Based upon the objectives, this research can be divided into three parts that address UWB receiver system analysis, wideband RF front-end, and frequency synthesizer separately. The first part of this work is dedicated to analyzing UWB radio requirements, selecting receiver architecture, and deriving specifications for individual blocks of the intended UWB receiver. Important system metrics, such as noise figure, $IP_3$, $IP_2$, gain, phase noise, and spurious suppressions, can be derived from wireless link characteristics, receiver sensitivity, BER requirement, out-of-band interferers and OFDM-related considerations. And then, receiver budget analysis leads to detailed block specifications. It is worth mentioning that different system design perspectives may yield different receiver architectures, and hence different circuit implementations. This makes system requirement analysis the cornerstone of all subsequent calculations and designs. The second part deals with circuit design of ultra wideband RF front-ends on the basis of system design. Two versions of RF front-end are tailored to fit in two different architectures which are consequences of distinctive system considerations. Efforts are made in circuit topologies and transistor-level design to meet spectral characteristics, gain and noise requirements specified in system design. The final part of the research concentrates on frequency generation schemes and trade-offs between different synthesizer architectures. Both theoretical analysis and circuit implementations are discussed to demonstrate the big picture of the intertwined system-circuit design flow.

1.3 Thesis Organization

This dissertation is organized as follows.
Chapter 2 goes over the fundamental aspects of MB-OFDM UWB technologies. A brief introduction of general ultra-wideband technologies is given at first, followed by an overview of OFDM technique and related design issues. Then basic properties of MB-OFDM UWB are presented. At the end of this chapter, current state of the arts of UWB radio is summarized as a reference point for UWB system design in later chapters.

Chapter 3 starts with a brief review of two common transceiver architectures, namely, superheterodyne and direct-conversion. Next, general metrics that define the performance of receivers and local oscillators are discussed. Wireless link analysis is performed afterwards, and the impacts of RF blocking profile on receiver sensitivity and selectivity, local oscillator phase noise, spurious suppression, and frequency offset are carefully studied. Following the discussion on blocking profile, design trade-offs in choosing RF front-end structures are presented, because this architecture largely affects receiver budget analysis. In the end, a set of specifications for each individual blocks in direct-conversion receivers derived from budget analysis concludes this chapter.

Chapter 4 focuses on transistor-level circuit implementations of UWB RF front-ends. At first, available circuit topologies for low noise amplifiers, active baluns and downconversion mixers, together with design formulas and guidelines, are discussed. Then design of the two proposed RF front-ends are demonstrated in two separate sections. Circuit simulation results are also provided to show the effectiveness of the design.

Chapter 5 explores the challenge in realizing MB-OFDM UWB frequency synthesizer. The first part of this chapter outlines architectural issues of single-sideband
mixer based frequency synthesis and the origins of frequency spurs in this approach. The second part is devoted to the proposal of a new frequency generation scheme and its corresponded synthesizer architecture. The final part of this chapter describes the preliminary design of giga-hertz voltage-controlled oscillator and the core divide-by-two circuit of the regenerative frequency divider proposed in this work. Simulation results are discussed to show the trade-offs in practical synthesizer design.

Finally, chapter 6 summarizes this dissertation with the contributions of this work and potential improvements along the road.
2.1 UWB Technologies

A UWB transmitter is defined by FCC as “an intentional radiator that, at any point in time, has a fractional bandwidth equal to or greater than 0.20 or has UWB bandwidth equal to or greater than 500 MHz, regardless of the fractional bandwidth”. Fractional bandwidth $B_f$, a quantity relative to center frequency, is expressed as in (2.1)

$$B_f = \frac{B}{f_c} \times 100\% = \frac{2 \times (f_U - f_L)}{(f_U + f_L)} \times 100\% \quad (2.1)$$

Therefore for UWB, the requirement is either $B_f > 0.20$ or $B > 500$ MHz, where $B$ is the absolute frequency bandwidth and $f_c$ is the center frequency of the band of interest.

The booming of UWB is primarily driven by the constantly increasing demands on higher data throughput. Shannon’s channel capacity theorem [3] specifies the maximum achievable bandwidth efficiency in a channel contaminated by additive white Gaussian noise (AWGN):

$$C = B \times \log_2 \left( 1 + \frac{P}{N_0 B} \right) = B \times \log_2 \left( 1 + \frac{S}{N} \right) \quad (2.2)$$
where $C$ is the channel capacity ($b/s$), $B$ is the transmission bandwidth ($Hz$), $P$ is the received signal power ($W$), $N_0$ is single-sided noise power density ($W/Hz$) and $S/N$ is signal-to-noise ratio SNR. Shannon’s theorem reveals an interesting fact that the capacity of a wireless channel shows approximately a logarithmic relation to signal power, while it increases linearly with respect to signal bandwidth.

Intuitively, in narrow band systems, ramping up SNR is more efficient to achieve high data rate than simply utilizing more frequency resource when channel capacity is low. However, following the saturating trend of logarithmic functions, wireless channel capacity eventually gains very little when a large increment of signal power is applied. Alternatively, increasing bandwidth can also provide channel capacity in a more efficient fashion especially when high capacity is desired. Furthermore, the communication can possibly be operated below noise floor, which is a particularly beneficial feature in already crowded modern wireless environments.

With its high data throughput and robustness to multipath fading, UWB is broadly recognized as the key technique for next-generation wireless personal area networks. One important application scenario is to replace current cable-based universal serial busses (USB) with their counterparts in wireless world – *Wireless USB (WUSB)* from the *USB Implementers Forum (USB-IF)* [4]. As shown in Figure 2.1, the fundamental topology in WUSB is a *hub and spoke*. In such a centralized network (referred as a *cluster*), a computer(*host*) initiates all data traffic among the connected devices (*clients*) around it, allotting time slots and data bandwidth to each client. WUSB also supports *dual-role* devices, which can serve as a USB client, and function as a host with limited capabilities at the same time.
Figure 2.1: UWB in wireless USB (WUSB) applications.

Figure 2.2: UWB in wireless home multi-media applications (Wi-Media).
In addition to WUSB, with the growing use of digital multimedia between consumer electronic products (such as digital cameras, camcorders, or TVs), and mobile communication devices (such as PDAs or laptop computers), UWB can serve as a common standard interconnect technology to support the on-going convergence of these mobile multimedia devices. The consumer usage model in Figure 2.2 exemplifies a high-connectivity and high-interoperability streaming media distribution system within personal operating space. The objective for this kind of systems is to enable high quality services and media exchange among the connected devices. For example, HDTVs typically require a data rate of $19 \sim 24$ Mbps, while SDTV/DVDs needs $3 \sim 7$ Mbps. All these applications demand extremely capable media stream deliveries that could be provided by UWB.

FCC authorized a large chunk of frequency (3.1–10.6 GHz) in 2002 for license-free, low emission power, high data throughput, and short-distance wireless devices using UWB technologies. The IEEE 802.15.3a task group (TG3a) took off in January 2003 to investigate UWB technique as the physical layer candidate for next generation wireless personal area networks. Although the endeavor of developing a unified high data rate UWB standard fell apart in January 2006, the two remaining and competing proposals, namely, dual-band direct sequence (DS-CDMA UWB) proposed by Freescale-Xtreme Spectrum and UWB Forum [5], and MB-OFDM UWB system backed up by the WiMedia™ Alliance and Multi-Band OFDM Alliance (MBOA) [1], committed to continue commercializing their individual UWB technologies and growing the UWB market.

Modern UWB technologies originate from early UWB communication, also referred as impulse radio or time-domain communication, which was widely used in
Figure 2.3: Spectral mask of UWB for indoor environments.

radar and military applications around 1960s. The idea is to represent wireless signals using very short-duration pulses that occupy wide spectrum up to several GHz. Transmission data may be modulated using pulse-position modulation and hence no radio frequency carrier is needed.

Similar to conventional impulse radio, DS-CDMA UWB, splits the 7 GHz UWB spectrum into a lower band from 3.1 to 5.15 GHz, and a higher band from 5.825 GHz to 10.6 GHz. M-ary Bi-Orthogonal Keying and a CDMA encoding scheme are used for multiplexing and channelization. In terms of performance, DS-CDMA UWB achieves excellent multipath resolution and bandwidth efficiency. However, DS-CDMA UWB terminal demands a complicated RAKE receiver with much more fingers than in
CDMA cellular phones. This requirement leads to complex detection architectures, higher pressure on DSP processing capabilities, and large power consumption.

Meanwhile, MB-OFDM UWB employs QPSK/OFDM as modulation scheme, and supports data rates of 55, 80, 110, 160, 200, 320 and 480 Mb/s. The typical operation ranges are 10 meters for 110 Mb/s, 4 meters for 200 Mb/s and 2 meters for 480 Mb/s. The desired power consumptions are $<100$ mW for 100 Mb/s and $<250$ mW for 200 Mb/s, while the target packet error rate (PER) is 8%. MB-OFDM UWB system demonstrates less vulnerability to multipath fading, good spectral efficiency, inherent resilience to narrow-band interference, and spectral flexibility to other emerging narrow-band wireless standards and international regulatory rules [6]. Besides the technical advantages, MB-OFDM UWB is officially adopted by USB-IF as radio platform for developing the so-called Certified Wireless USBs. This makes MB-OFDM UWB a competitive and attractive candidate for future wireless broadband applications.

2.2 OFDM Fundamentals

Technically, orthogonal frequency division multiplexing (OFDM) [7] casts profound impacts on MB-UWB radio systems and virtually defines many of their system specifications. Therefore, it is worthwhile to review important properties of OFDM-based systems before moving to MB-OFDM UWBs.

OFDM has gained considerable popularity over the past several years in wireless communication, such as wireless LAN, digital video broadcasting (DVB) and upcoming WiMAX technologies. In contrast to traditional single-carrier technologies, OFDM is generally considered as a wideband multi-carrier scheme, in which a
frequency channel is divided into a bundle of slices (sub-carriers), and data streams from a single source are transmitted in parallel through these sub-carriers. The most pronounced advantage of OFDM is its robustness to multipath fading, which makes it a perfect approach to handle distortions commonly found in contemporary harsh wireless environment. Furthermore, performance and capacity of channels can be improved without the penalty of hardware complexity.

Multipath is a serious challenge in wireless communications. Signals travel through multiple paths and arrive at the same destination with different amplitude, phase shift and time delay. In frequency domain, these frequency components may add up destructively. This leads to signal attenuation and information loss at certain frequencies, which is often referred as fading. From time-domain point of view, multiple copies of signal with different time delays raise the possibilities that different symbols overlap or smear into each other, creating intersymbol interference.

OFDM handles multipath distortions efficiently. Visualized in Figure 2.4, OFDM uses groups of narrow band symbols and inserts guard intervals (also referred as cyclic prefix [7]) between them to counter the time-domain smearing caused by multipath in
Figure 2.5: Block diagram of a complete OFDM transmission and reception path.

wireless environment. OFDM divides desired frequency band $B$ into $M$-subcarriers labeled from 1 through $M$ in Figure 2.4. Each individual subcarrier may use different scheme to modulate. In order to stay away from mutual interfering, frequency spacing between these subcarriers is selected to be the inverse of transmitted symbol duration.

In frequency domain, since the spectrum is split into multiple independent pieces, when multi-path causes fading at certain frequencies, its impact is limited to only a few subcarriers. Therefore, the overall bit error rate (BER) degradation is much less an issue than that in single-carrier scheme. In time domain, a guard interval is added on top of each symbol and its length is set to be longer than any possible smearing. Simply discard the redundant guard intervals, the symbols will be kept intact.
A generic OFDM transmission/reception path is shown in Figure 2.5. On the transmission side, in addition to carrier slicing, error correction coding and interleaving are used to combat weakened subcarriers and error bits. Error correction coding provides redundancy to payload data, while interleaving changes the time order of transmitted bits. When weakened subcarriers lead to a long burst of errors, interleaving allows the long burst to be spread out in time, and results in several shorted bursts of errors. Error correction codes then kick in to recover these short error bursts. After encoding and interleaving, data are fed into digital modulator to generate PSK or QAM signals. The modulated data is then converted into $M$ parallel data streams by a series-to-parallel multiplexer (S/P). The streams are processed by Inverse Fast Fourier Transform (IFFT) block to be modulated onto $M$-subcarriers. The following P/S serializes IFFT output to form a single data stream so as to be modulated by a single carrier. The analog transmitter in the end performs signal amplification, spectrum trimming, frequency upconversion, and finally broadcasting.

The reception path is exactly the reverse of transmission. Received RF signals are processed by analog receiver and converted into digital baseband data prior to being passed to a combination of S/P, FFT and P/S processing units. The resulted data stream is then demodulated, de-interleaved, error corrected and eventually converted into desired payload information.

Despite its big advantages, OFDM-based wireless communication system needs to cope with several design issues, to name a few, frequency offset, phase noise and peak-to-average ratio (PAR). First of all, frequency offset between transmission and reception is a severe challenge for OFDM. In presence of frequency offsets, the subcarriers are no longer orthogonal, resulting in inter-carrier interference (ICI) and
degrading error rate significantly. Phase noise is another challenge. Phase noise introduces reciprocal mixing [8] in wireless communication systems. In OFDM system, due to smaller subcarrier bandwidth, the requirements on phase noise are much more stringent than in conventional modulation schemes. Finally, OFDM signal tends to have a large variation between maximum signal power and average signal power, the so-called PAR, which presents a design challenge to power amplifiers (PAs). The large PAR is because individual OFDM subcarriers virtually have their own independent modulations. There exists a possibility that a data sequence could make all subcarriers add up to each other constructively and form a large peak signal. These design issues and their implications to MB-OFDM UWB systems will be further addressed in later parts of this dissertation.

2.3 Multi-band OFDM UWB

In contrast to impulse radio or “carrier-free” communications, multiband-OFDM UWB is generally regarded as a carrier-based system, similar to GSM, CDMA and DVB. In particular, MB-OFDM UWB is a close relative to wireless local area network (WLAN) systems. MB-OFDM UWB partitions the spectrum from 3.1 to 10.6 GHz into 5 frequency band groups, 14 frequency bands with bandwidth of 528 MHz (Figure 2.6). The band center frequencies $f_B$ are given by [1]:

$$f_B = 2904 + 528 \times n_b \text{ (MHz)}, \quad n_b = 1 \ldots 14 \quad (2.3)$$

where $n_b$ is designated band number. Band group 1 is specified in [1] as mandatory operation mode. Other band groups are reserved for future use.

Each 528 MHz UWB band is divided into 128 sub-carriers with bandwidth of $f_{\text{tone}} = \frac{528}{128} = 4.125 \text{ MHz}$. Out of the 128 sub-carriers, 100 tones carry payload
data, 12 pilot tones facilitate coherent detection against frequency offsets between TX and RX, 10 guard tones relax filter design and the other 6 null tones carry no information at all. The MB-OFDM system adopts a frequency-hopping scheme to provide frequency diversity and multiple access. A guard interval of 9.47 ns is specified as TX/RX switching time, which sets the upper limit of synthesizer settling time between two frequency hops.

MB-OFDM UWB poses a wide variety of new challenges to analog radio design. The large fractional bandwidth complicates the design of RF band-selective networks, such as low-noise amplifier (LNA) input matching and power amplifier (PA) output matching networks. It also makes it tough to realize an analog baseband band-selection low-pass filter (LPF) with both high corner frequency (in excess of 250 MHz when I/Q paths considered) and sufficient attenuations to out-of-band jammers, because classical analog filter topologies may require an op-amp with high DC gain and open-loop unity-gain bandwidth of at least 2.5 GHz (10 times of filter corner frequency to guarantee closed-loop stability). To accommodate the large communication data rate, UWB analog-to-digital converters (ADC) have to resort to power-hungry parallel or time-interleaved architectures, which are undesirable for low-cost and high-mobility applications intended by UWB technologies. In addition,
the frequency hopping nature of MB-OFDM UWB rules out conventional phase-lock loop frequency synthesizers and calls for new frequency generation architectures.

2.4 Previous State of the Art

An abundance of literature has recently been dedicated on realizing full-system MB-OFDM UWB radio implementations [9–11], individual RF/analog building blocks [12–18], and architectural analysis and frequency planning [2,19].

As one of the first published full UWB radio, reference [9] presents a CMOS Mode-1 device using three front-end frequency tuning tanks and three separate PLLs with ring VCOs to reduce die area and avoid undesired frequency spurs. This idea, however, when expanded to 14 bands, may cause bulky synthesizer structure, difficult layout routing, and huge power dissipation. A BiCMOS Mode-1 UWB receiver chain with an agile LO synthesis scheme is demonstrated in reference [10]. Some perspectives on interferer scenario and system linearity requirements are also given in this work. Reference [11] shows a direct-conversion radio covering 3.1–8.2 GHz Mode-2 UWB communications, and provides general guidelines for UWB frequency planning and theoretical analysis on spur propagation along frequency generation path.

To meet the multi-GHz bandwidth needs of UWB LNAs, multi-section LC-ladder band-pass filters can be used in front of classical inductively-degenerated commonsource/emitter LNAs [12,13] to shape LNA input matching spectral characteristics. Resistive feedback topologies can also be adopted [14] to increase bandwidth and maintain gain flatness across multi-GHz range. In [15], the influence of WLAN interferers is emphasized. An extra notch at 5–6 GHz is engineered to reject those
jammers by tweaking the \( LC \) loading network of a voltage-voltage feedback common-gate LNA. Another interesting solution to LNA bandwidth expansion is given in [16], in which the wideband input matching is achieved by applying a dual-loop resistive feedback system and dynamically adjusting the gain ratio between the two loops to equal to desired input impedance.

A popular architecture for MB-OFDM UWB local oscillator is introduced in [6]. Following the similar idea, reference [18] reports a 3-band, Mode-1 synthesizer by using a single-PLL and accompanied single-sideband (SSB) mixing and multiplexing stages. Another viable way to generate UWB band frequencies is to utilize two identical PLLs switching on alternatively to synthesize next hopping frequency, as reported in [17]. This dual-PLL synthesizer has a significant advantage over mixer-based architecture: it avoids using mixers and multiplexers in signal paths and therefore greatly reduces unwanted spectral by-products. But this approach faces a few difficulties as well. For example, to apply to all operation modes, the PLL may occasionally experience large frequency steps and need to settle in a very short time. This poses challenge on PLL loop bandwidth and noise optimization. In addition, to synthesize all 14 UWB frequencies, two PLLs may not be adequate.


Unfortunately, all these representative works reported thus far either could not be expanded to full UWB spectrum or do not address the impacts of RF front-end
topology on system performance and synthesizer characteristics. As will be discussed later in this paper, the choice of RF front-end implementation plays a crucial role in determining receiver specifications, LO phase noise and spurious contents. Therefore a more comprehensive system-level analysis must be performed in order to accomplish an optimally designed UWB receiver.
CHAPTER 3

SYSTEM DESIGN OF DIRECT-CONVERSION UWB RADIOS

In this chapter, requirement analysis, and system-level design for MB-OFDM UWB are discussed. To lay down a foundation for later derivations, this chapter begins with background introduction. Section 3.1 briefly reviews two dominant receiver architectures and their advantages and drawbacks. Important receiver performance parameters are defined in section 3.2. With theoretical framework set up, section 3.4 focuses on MB-OFDM UWB communication system itself, analyzing spectrum characteristics, application scenario, wireless links, and out-of-band blocking profiles, and defining top-level requirements on sensitivity, gain, noise figure, linearity, phase noise and spurious suppression. An important observation in this section leads to the RF front-end design strategies that are adopted in this work. Section 3.5 describes two different versions of receiver structures. In the final section of this chapter, receiver budget analysis is conducted for two receivers separately, and block-level specifications are derived at the end of this chapter.
3.1 Wireless Receiver Architectures

Different mobile application contexts impose different constraints in choosing wireless receiver architectures. For example, the effectiveness of wireless sensor networks heavily relies on the battery life within each sensor node. As a result, power dissipation and cost are the top priorities in selecting receiver architecture and circuit topologies. On the other hand, cellular phone applications must be able to handle hostile urban wireless environments, making sensitivity and selectivity more important considerations than the others. In this section, we focus on two most important and widely used wireless receiver architectures, namely, superheterodyne and direct-conversion (or homodyne/zero-IF). Other architectures such as low-IF [8, 20], RF direct-sampling and software defined radio (SDR) [21] can be found in the references if interested.
3.1.1 Superheterodyne Architecture

Superheterodyne receiver, or simply superhet, is the most widely used architecture in wireless communications for the past a few decades, because of its excellent selectivity and sensitivity. In superhet, RF signals experience multiple frequency translations to be demodulated for processing. Thus superhet architecture usually has more than one intermediate frequency (IF) and more than one IF processing chain. A typical one-IF superhet receiver in IC is shown in Figure 3.1, in which external components are highlighted with light orange color. In terms of operating frequency, the function units in superhet can be categorized as three different sections: RF section, IF section and analog baseband (BB) section.

In RF section, an RF bandpass filter (BPF) immediately after the antenna functions as the pre-select filter suppressing large out-of-band interferers and relaxing dynamic range (DR) requirements on following receiving blocks. This pre-select filter demands high quality factor, and is often realized off the chip. The next stage is a transmitter/receiver (T/R) switch or duplexer. This arrangement allows the antenna and RF BPF to be shared by both transmission and reception, alternatively in time-domain (when T/R switch is used) or in frequency domain (when duplexer is used). It is worth to mention that in reality RF BPF and T/R switch are both passive components that attenuate desired input RF signals. Next to T/R switch, a low noise amplifier (LNA) amplifies the weak RF signals while introducing ideally zero noise. An image-reject filter (IRF) follows LNA in order to minimize the damage from noise or interferer at image frequency. The requirement of high Q-factor on IRF is usually satisfied by using external surface acoustic wave (SAW) or ceramic
filter. The last stage in RF section, downconversion mixer, translates amplified and trimmed RF signals into IF processing pipeline.

Similar to RF section, IF processing chain includes signal amplification (intermediate frequency amplifier, or IFA) and filtering (IF BPF) to remove unwanted frequency mixing products and clean up signals. External filters are often used to provide sufficient selectivity. A pair of mixers at the end of IF section allows in-phase (I) and quadrature (Q) downconversions to analog baseband. After RF signal being transported to analog baseband section, a serial combination of low-pass filters and
variable gain amplifiers (VGA) provides final channel selection, signal conditioning and dynamic range adjustment so that the ADCs can convert analog signals into digital domain with required bit error rate. In addition to the three sections, two local oscillators are needed to enable the two frequency translation steps: \( f_{LO_1} = f_{RF} - f_{IF} \) and \( f_{LO_2} = f_{IF} \). More precisely, \( LO_2 \) should be able to generate I and Q signals with \( 90^\circ \) phase shift.

Superheterodyne receiver offers excellent combined selectivity and sensitivity largely because of the aggressive filtering at RF, IF and analog BB sections. And the evolving maturity throughout the years makes superhet the most reliable solution for digital wireless communications. Despite its obvious advantages, superhet receiver requires a large number of off-chip components, which are often expensive when compared to the fabrication cost of the chip itself. Furthermore, this architecture suffers from the problem of image, and exhibits a trade-off between image rejection and channel selection.

The issue of image is easy to understand. Refer to Figure 3.2(a), in a high-side injection [8] frequency translation scheme, desired signal band is located at \( f_{LO} - f_{IF} \) and LO is presented at \( f_{LO} \). When RF input signals are downconverted to IF band, unfortunately, any noise and interferer at image frequency \( f_{LO} + f_{IF} \) is also transferred into the signal band at \( f_{IF} \), because analog frequency mixing simply fails to discriminate different sidebands. Therefore, as shown in Figure 3.1, an image-reject filter is placed in RF processing section to suppress the corrupting signal from image band. At the same time, an IF channel selection filter is also needed to reject in-band interferers, which are marked in red in Figure 3.2(a).
Here comes the dilemma in choosing $f_{IF}$. Notice the frequency difference between desired signal and image is $2 \times f_{IF}$. If IF frequency is picked up to be high (Figure 3.2(a)), quality factor of IRF can be relaxed. Meanwhile, since the $f_{IF}$ is high, the rejection requirements of channel-selection filter are much more tightened. On the other hand, lowering IF frequency (Figure 3.2(b)) takes burdens from IF filter, but demands a high-$Q$ IFR to suppress image effectively. Since noise or interferer leakage from image band degrades the sensitivity of the receiver, the trade-off between image rejection and channel selection is also regarded as the trade-off between sensitivity and selectivity [8].

In actual superhet receiver design, the trade-off mentioned above needs to be taken care of during initial design stages. More specifically, careful and time-consuming frequency planning is often critical to mitigate the issues associated with images. There are also some specially designed image-reject receiver architectures out there, for example, Harley architecture and Weaver architecture. These techniques are beyond the scope of this dissertation, thus are not further discussed.

3.1.2 Direct-conversion Architecture

The first introduction of direct-conversion receivers dates back to 1930’s, but because of the numerous implementation difficulties associated with it, this type of receivers found few applications until 1980’s. With the development and evolution of integrated circuit technologies, many design issues of direct-conversion receiver have been alleviated, and its simplicity makes it superior to superhet in many situations.

Direct-conversion receivers differ from superheterodyne architecture by placing intermediate frequency at DC, or in other words, eliminating the use of intermediate
frequency. The significance of the so-called “zero-IF” is that the problem of image is completely avoided because image band is in fact located on top of the signal band. As a result, a number of functional units used in superhet can be dropped. The configuration of direct-conversion receivers shown in Figure 3.3 actually looks much simpler than the one in Figure 3.1. Only two processing sections are necessary in this architecture, namely, RF section and analog baseband section.

Same as in superheterodyne receiver, RF BPF acts as the pre-select filter to reject out-of-band blockers, and T/R switch controls signal flows in to or out of transceiver. Low noise amplifier magnifies weak RF input signals and minimizes noise contributions from following stages. I/Q demodulators mix RF signals directly down to DC to be processed by the chain of channel-select LPF, VGA and A/D converter.

Direct downconversion brought forth a few important advantages. The first significant benefit is that since no intermediate frequency is involved in this architecture, RF image-reject filter is no longer a must, and IF processing blocks are completely
dropped off. Only one external component, RF pre-select filter, is necessary, which is much less costly than the three off-chip filters in superhet. Second, removing the IF section reduces the number of building blocks in the receiver, and potentially lowers total power dissipation. In addition, as no image and less spurious frequencies are generated, this architecture can simplify design flow by skipping the time-consuming frequency planning. It is no doubt that direct-conversion architecture is an excellent candidate for low cost, low power applications, at least in principle.

However, the simple structure and resolution of image problem come at the price of a few design challenges: DC offsets, even-order nonlinearity, device flicker noise, and I/Q mismatch. The origins and mechanisms of these issues are well documented in literatures [8,20,22], and only a short overview is given in this dissertation.
DC offsets, even-order nonlinearity and flicker noise  DC offsets, even-order distortion and flicker noise give rise to BER degradation of received signals in a very similar fashion, although they have totally different origins. As will be discussed shortly, the fundamental mechanism behind all three issues is that unwanted low-frequency voltages are generated unintentionally and these voltages fall into and blend with desired signals, corrupting signal fidelity. These low-frequency effects are particularly pronounced for direct-conversion receivers, because no IF stage functioning as a signal buffer exists in this architecture.

DC offsets is primarily caused by *self-mixing*. In IC technologies, due to electromagnetic field effects such as transistor capacitive coupling, substrate permittivity and crosstalk between parallel runners, high frequency signals can feed through between RF ports. For example, in a CMOS Gilbert mixer (Figure 3.4(b)), strong LO signal leaks thru $C_{GS}$ of $M_3$ and $C_{GD}$ of $M_1$ into RF port; the leakage could mix with LO signal generating a DC component (since the leakage frequency equals to LO frequency) at IF port or analog BB port; or the leakage can even propagate back into the output port of the proceeding LNA, (Figure 3.4(a)) and couple through substrate and $C_{GD}$ of $M_1$ into LNA input RF$_{in}$, and then loop back to mixer input port with forward LNA amplification. This leakage is also transferred by mixer resulting in DC offset voltage. Meanwhile, strong interferers could also sneak into local oscillator, mix with itself in mixer, and lead to a small DC voltage. The small DC voltage, amplified by the huge gain provided in baseband amplifiers, could saturate and desensitize the following stages easily and crash entire signal reception. Since RF coupling arises from physical imperfections, DC offset can not be eliminated completely. Hence DC offset cancellation circuits are always required in direct-conversion design.
Even-order nonlinearity is well known to exist in single-ended circuits. Even fully-differential circuits, with the presence of device mismatches especially at radio frequencies, could not cancel out all even-order nonlinearities. While even-order distortions do not introduce concerns to superhet, they prove to be problematic in direct-conversion receivers. Two strong interferers at frequencies $f_i$ and $(f_i + \Delta f)$ respectively can generate a spurious low-frequency component at $\Delta f$, if passed through an even-order nonlinearity. If $\Delta f$ is less than desired channel bandwidth, then the spurious tone falls into signal range at baseband causing BER degradation. More specifically, if the frequency difference term is generated in LNA, it could pass by the mixer into baseband due to any MOS device, load, or LO duty-cycle mismatches in down-conversion mixer. If the even-order distortion happens in mixer, the low-frequency component will be directly contained in desired signals. Therefore in some sensitive applications, special circuit topologies or calibration techniques are needed to satisfy stringent even-order linearity requirements.

Flicker noise is inherently associated with field-effect transistor devices. Roughly speaking, the noise power is inversely proportional to frequency, $\overline{v_n^2} \propto \frac{1}{f}$. Since this noise is more a low-frequency effect than a high-frequency one, it degrades signal BER in the same way as DC offset. From system point of view, the influence of flicker noise can be neutralized by allocating higher gain in the first few RF stages; at device level, large transistor dimensions can be used to lower intrinsic noise power.

In summary, the impacts of DC offset, even-order distortion and flicker noise are all tied to some aspects of actual circuit design. But because the consequence of these issues is similar, they can be treated in similar manners. For example, in reference [23] a couple of low-frequency chopping mixers sandwiched a downconversion RF mixer to
Achieve dynamic device matching in the mixer. As a result, not only the even-order distortion is greatly suppressed, but also DC offsets and flicker noise are noticeably reduced.

**I/Q mismatch** Quadrature mixing is needed in all frequency and phase modulation schemes to recover phase domain information (Figure 3.1 and 3.3). To prevent phase information from being contaminated, quadrature mixing requires local oscillator to generate in-phase and quadrature signals persisting a strict $90^\circ$ phase difference and equal amplitude. In addition, the gain and group delay along $I$ and $Q$ paths need to be identical. In real IC technologies, however, device imperfection, temperature/doping gradient and phase distortion in quadrature LO signals are inevitable. As consequences, gain error and phase imbalance are introduced between I/Q paths, and received signal BER is degraded.

I/Q mismatch exists in both superhet and direct-conversion receivers. But in superhet receiver, I/Q matching requirements are significantly relaxed because of two facts. First, the I/Q mixers operate at low frequency (IF), thus are less sensitive to device mismatch. Second, IF amplifiers preceding mixers provide a large amount of amplification to desired signals, and help them immune from I/Q imbalance. On the contrary, in direct-conversion, I/Q mixing happens at RF while received signals are still weak. This makes I/Q mismatch a tough challenge to deal with.

In conclusion, although it suffers from some design difficulties, direct-conversion architecture inherently allows high integration level and simple signal receiving path, which are highly desirable features for low-cost and compact-size applications. In fact, some properties of MB-OFDM UWB are rather favorable to this architecture.
3.2 Basic Transceiver Performance Metrics

The key parameters of wireless transceivers include receiver sensitivity, noise figure, linearity, adjacent channel and alternate channel selectivity, single-tone desensitization, interference blocking, dynamic range, and automatic gain control range [8,20,24]. Single-tone desensitization is primarily used in CDMA systems and will not be discussed in this dissertation.

3.2.1 Receiver Sensitivity and Noise Figure

Sensitivity and system noise figure are two closely related parameters for a wireless receiver. By definition, receiver sensitivity $S_{\text{min}}$ is the minimum signal strength that a receiver can detect [20], and maintain a target bit error rate (BER). Meanwhile, refer to a two-port analog network in Figure 3.5, Noise factor $F$ is defined as the ratio of input signal-to-noise ratio $SNR_{\text{in}}$ to output signal-to-noise ratio $SNR_{\text{out}}$, reflecting the noise contribution inside the block of interest (typically modeled as a series noise voltage source $V_n^2$ and a parallel noise current source $I_n^2$). Noise figure $NF$ is actually the noise factor in dB, i.e.

$$NF = 10 \times \log_{10}(F) = 10 \times \log_{10}\left(\frac{SNR_{\text{in}}}{SNR_{\text{out}}}\right). \quad (3.1)$$
In wireless communication systems, the quality of reception is determined by desired signal power and integrated thermal noise power within the receiver bandwidth. Therefore, receiver sensitivity can be expressed in dBm as:

\[
S_{\text{min}} \text{ (dBm)} = 10 \cdot \log_{10}(kT_0) + 10 \cdot \log_{10}(B) + NF_{\text{rx}} + SNR_{\text{min}} \tag{3.2}
\]

where \( k = 1.38 \times 10^{-23} \text{ J/}^{\circ}\text{K} \) is Boltzman constant, \( T_0 \) is ambient temperature, \( B \) is signal bandwidth, \( NF_{\text{rx}} \) is total receiver noise figure, and \( SNR_{\text{min}} \) is minimum required signal-to-noise ratio. If \( T_0 = 290^{\circ}K \), then (3.2) can be simplified as

\[
S_{\text{min}} \text{ (dBm)} = -174 + 10 \cdot \log_{10}(BW) + NF_{\text{rx}} + SNR_{\text{min}}. \tag{3.3}
\]

In (3.3), it is clear that sensitivity is a direct indication of receiver noise figure, since required \( SNR_{\text{min}} \) is primarily a pre-defined constant by modem, codec schemes and target data rate.

**Noise figure in cascaded system** Once the system total noise figure requirement is found, it is desirable to determine noise specification of individual blocks that consist of a system. In a system with cascaded stages depicted in Figure 3.6, Friis [25] proved that total noise factor can be expressed in terms of available power gain and noise factor of each block as:

\[
F_{\text{total}} = F_1 + \frac{F_2 - 1}{G_{P,1}} + \frac{F_3 - 1}{G_{P,1}G_{P,2}} + \cdots + \frac{F_N - 1}{G_{P,1}\cdots G_{P,N-1}} \tag{3.4}
\]

where \( F_i \) and \( G_{P,i} \) are the noise factor, available power gain of stage number \( i \), respectively.

Friis equation is particularly useful when an RF receiver is constructed with discrete components whose input and output impedance are designed to be standard.
impedance 50 Ω or 75 Ω. In IC technologies, Friis equation also serves well when the input impedance $Z_{in,i}$ of stage $i$ is complex-conjugate matched to output impedance $Z_{out,i−1}$ of the previous stage $i−1$. Thus no power loss is resulted because of impedance mismatch between stages. In other situations where a receiver is fully integrated and the input/output impedance of the cascaded stages are unknown, impedance mismatch needs to be carefully considered. This concern can be partially resolved during circuit design phase when neighboring circuit blocks are finished designing, then their cascaded effects can be simulated, and corrected parameters can be fed back into system design phase.

Another approach is presented in reference [26] in which input-referred noise voltage rather than SNR, and loaded voltage gain instead of available power gain are used to determine system noise figure. Based on this approach, noise factor of a cascade of LNA, mixer, channel-select filter and AGC is given in [26] as:

$$F_{\text{total}} = 1 + \frac{\mathbf{V}_{n_{i},\text{LNA}}^2}{\mathbf{A}_{\text{LNA}}^2} + \frac{\mathbf{V}_{n_{i},\text{mixer}}^2}{\mathbf{A}_{\text{mixer}}^2} + \frac{\mathbf{V}_{n_{i},\text{filter}}^2}{\mathbf{A}_{\text{filter}}^2} + \cdots$$  

(3.5)

where $\mathbf{V}_{n_{i}}$ and $\mathbf{A}_{vn}$ are the noise voltage source and loaded voltage gain of each stage, respectively.
The advantage of this method is the mismatch-induced power loss in classical RF 2-port network analysis is circumvented, however, it still needs the knowledge of output impedance and load of each stage. In addition, if a more complete 2-port noise model that also includes an equivalent noise current source in parallel (as in Figure 3.5) is used for each building block, the derivation will be rather cumbersome and of little practical value. Therefore, we stick to Friis’s approach in this dissertation.

3.2.2 Receiver Linearity

Nonlinearity affects receiver performance primarily through several different mechanisms, including gain compression, desensitization, cross modulation and intermodulation (IM) [8]. Among them, intermodulation poses serious challenge to RF receivers, thus deserves more discussions. To understand the phenomenon of IM, consider a nonlinear circuit black box with characteristic function of

\[ V_{\text{out}} = \alpha_1 V_{\text{in}} + \alpha_2 V_{\text{in}}^2 + \alpha_3 V_{\text{in}}^3 \]  

(3.6)

when \( V_{\text{in}} = A[\cos(2\pi f_1 t) + \cos(2\pi f_2 t)] \) is passed into the block of (3.6), it can be shown that frequency components appear at \( f_2 \pm f_1 \), \( 2f_2 \pm f_1 \) and \( 2f_1 \pm f_2 \) as:

\[ f_2 \pm f_1 : \alpha_2 A^2 \cos 2\pi (f_2 \pm f_1) t \]  

(3.7)

\[ 2f_1 \pm f_2 : \frac{3\alpha_3 A^3}{4} \cos 2\pi (2f_1 \pm f_2) t \]  

(3.8)

\[ 2f_2 \pm f_1 : \frac{3\alpha_3 A^3}{4} \cos 2\pi (2f_2 \pm f_1) t \]  

(3.9)

These frequency components are called intermodulation products. More specifically, tones at \( f_2 \pm f_1 \) are produced from second order nonlinearity, and tones at \( 2f_2 \pm f_1 \) and \( 2f_1 \pm f_2 \) are generated by third order nonlinearity.
To appreciate the impact of intermodulation, the generation of third order IM product can be graphically explained by referring Figure 3.7. When a desired bandpass signal along with two strong RF interferers are passed through a nonlinear processing block, the third order nonlinearity will generate intermodulation products of the interfering RF signals resulting two spurious tones at \((2f_2 - f_1)\) and \((2f_1 - f_2)\). The IMD tone at \((2f_1 - f_2)\) falls into signal band, affecting data reception [8,20].

The most important nonlinear effects are the second order and third order. In narrow band systems, only IM product at \((2f_1 - f_2)\) or \((2f_2 - f_1)\) induced by third order nonlinearity jumps into signal bandwidth. All other frequency components \((2f_1 + f_2)\) and \((2f_2 + f_1)\) are far away from desired band, thus can be filtered out easily. As to second order nonlinearity, it has notable impact only on direct-conversion receivers, in which IM product at \((f_1 - f_2)\) could influence analog baseband processing, while IM product at \((f_1 + f_2)\) is of little importance. In broad band systems, however, the previously negligible frequency tones tend to be troublesome. This is because not only frequency difference but also frequency summation could happen to fall into the band of interest. This issue will be discussed later within the context of UWB radio specifications.
The linearity of receivers is generally measured by intercept points. The most frequently used are 3rd-order input-referred intercept point ($IIP_3$) and 2nd-order input-referred intercept point ($IIP_2$). When two RF tones with same input power level are delivered into a nonlinear power processing block, $IIP_3$ of the block is defined as the input power level at which the third order IM product reaches the same power level as fundamentals. Similarly, $IIP_2$ is given as the input power level at which the second order IM product has the same power level as the fundamental.

Manipulating the numbers using the plot in Figure 3.8, we have

\[ IIP_m - IM_m = m \cdot (IIP_m - P_{in}). \] (3.10)

Therefore, the general relationship between $m^{th}$-order input-referred intercept point ($IIP_m$), input signal power $P_{in}$ and the IM product $IM_m$ can be expressed as:

\[ IM_m = m \cdot P_{in} - (m - 1) \cdot IIP_m \text{ (dBm)} \] (3.11)
or equivalently

$$IIIP = \frac{m \cdot P_{in} - IM_m}{m - 1} \text{ (dBm)}$$ (3.12)

Using equation (3.12), the linearity requirements of a receiver can be determined. For example, if the minimum required carrier-to-interferer level at the output of analog domain is $(C/I)_{\text{min}}$, desired signal level is $P_{\text{sig}}$, and RF interferer is $P_{\text{int}}$, then $IIIP_3$ needs to satisfy the following relation to guarantee required BER

$$IIIP_3 > \frac{3 \cdot P_{\text{int}} - P_{\text{sig}} + (C/I)_{\text{min}}}{2} \text{ (dBm)}$$ (3.13)

Similarly, second order intercept point is calculated as

$$IIIP_2 > 2 \cdot P_{\text{int}} - P_{\text{sig}} + (C/I)_{\text{min}} \text{ (dBm)}$$ (3.14)

**Linearity in cascaded system** The derivation of intercept points of cascaded stages is a tricky process, since it imagined that phase relations between IM products (IMP) from individual stages should play a role in summing up to total system IM products. However, we can still specify linearity in cascaded stages by two bounding extremities.

The most stringent requirements on individual stages come from the situation when their IMPs add up in phase. In this scenario, $IIIP_3$ in a cascade is given by

$$\frac{1}{IIIP_{3,\text{total}}^2} = \frac{1}{IIIP_{3,1}^2} + \frac{G_{V1}^2}{IIIP_{3,2}^2} + \frac{G_{V1}^2 \cdot G_{V2}^2}{IIIP_{3,3}^2} + \cdots$$ (3.15)

By contrast, the best-case requirement happens when IMP of each stage is completely out of phase. In this case, total $IIIP_3$ is found to be

$$\frac{1}{IIIP_{3,\text{total}}^2} = \frac{1}{IIIP_{3,1}^2} + \frac{G_{V1}^2}{IIIP_{3,2}^2} + \frac{G_{V1} \cdot G_{V2}^2}{IIIP_{3,3}^2} + \cdots$$ (3.16)
In (3.15) and (3.16), $IIP_3$ is specified in voltage rather than in power, and $G_{V,i}$ stands for the voltage gain of stage $i$.

The $IIP_2$ in cascaded stages is derived assuming that IM products are added up in phase. The resulted $IIP_2$ relationship is as follows. Again, $IIP_2$ is a voltage quantity.

\[
\frac{1}{IIP_{2,\text{total}}} = \frac{1}{IIP_{2,1}} + \frac{G_{V,1}}{IIP_{2,2}} + \frac{G_{V,1} \cdot G_{V,2}}{IIP_{2,3}} + \cdots
\]

(3.17)

It is interesting to notice that in these classical linearity expressions (3.15, 3.16, 3.17) in cascaded stages, nonlinearity contribution of latter stages in the cascade may become increasingly more significant. In the derivation above, however, we latently assume that no frequency selectivity of intermediate stage is involved to attenuate interferers. In practical design, interfering signals are progressively suppressed along the receiver chain, hence a frequency selectivity factor $S$, specified as the power attenuation to interferers, needs to be included in linearity analysis. The modified worst-case (in-phase summation) cascaded linearity equations are given as:

\[
\frac{1}{IIP_{3,\text{total}}} = \frac{1}{IIP_{3,1}} + \frac{G_{V,1}^2 \cdot S_1^{3/2}}{IIP_{3,2} \cdot S_1^3} + \frac{G_{V,1}^2 \cdot G_{V,2}^2}{IIP_{3,3} \cdot (S_1 \cdot S_2)^{3/2}} + \cdots
\]

(3.18)

\[
\frac{1}{IIP_{2,\text{total}}} = \frac{1}{IIP_{2,1}} + \frac{G_{V,1}}{IIP_{2,2} \cdot S_1} + \frac{G_{V,1} \cdot G_{V,2}}{IIP_{2,3} \cdot (S_1 \cdot S_2)} + \cdots
\]

(3.19)

### 3.2.3 Other Performance Parameters

In addition to receiver sensitivity, noise figure and linearity metrics, some other parameters are used to define or characterize receiver performance. These parameters include dynamic range, filter attenuations and automatic gain control (AGC) range.

**Dynamic range** Dynamic range is defined as the power range of input signal at antenna port over which a receiver can process and satisfy BER requirements [8, 20].
The lower end of the dynamic range is limited by receiver sensitivity, which is the minimum signal power the receiver can pick up. The higher end of the dynamic range is judged by a receiver’s intermodulation performance, i.e. IM product resulted from large input signals should not exceed receiver noise floor in order to ensure target BER can be satisfied. It is obvious that dynamic range of a receiver is essentially implicated by receiver sensitivity and linearity.

**AGC range**  Automatic gain control in receivers is critical to adjust total receiver gain and accommodate weak and strong input RF signals. The AGC range is closely related to dynamic range, but AGC range is usually wider than required receiver dynamic range to cover gain spreads due to process corners, temperature and supply voltage variations. In direct-conversion receivers, the wide AGC range is normally realized by allocating gain to both step-controlled RF low noise amplifier and baseband variable gain amplifiers (VGA). A general approach is to assign several coarse gain steps to LNA and design a baseband VGA with much finer gain steps.

**Filter attenuations**  As discussed in previous section, multiple filters are employed in wireless radio receivers. In direct-conversion receivers, an RF pre-select filter and an analog baseband channel-select filter are usually needed. The major purpose of these filters is to attenuate RF interferers and maintain required carrier-to-interferer ratio \((C/I)_{\text{min}}\). Therefore, the stop-band attenuation requirements are usually driven by operating frequency and RF blocking profile. Important design specifications for these filters include operating center frequency, corner frequency, pass-band insertion loss, pass-band ripple, stop-band attenuations, and phase transfer characteristics such as group delay.
3.3 Requirements on Local Oscillator in Wireless Receiver

In addition to the aforementioned receiver parameters, another set of critical specifications is tied to local oscillators, which will be the topic of this section. In this section, we focus on establishing a theoretical model and corresponded strategies to derive local oscillator (LO) phase noise and spurious suppression specifications for narrow-band and broad-band wireless receivers.

In frequency domain, an ideal LO is treated as an impulse at $f_{LO}$, while in time domain, it is expressed as a sinusoidal wave (Figure 3.9(a)):

$$V(t) = V_0 \sin(2\pi f_{LO}t)$$  \hspace{1cm} (3.20)

In real local oscillators (Figure 3.9(b)), however, sideband power is distributed around frequency $f_{LO}$. In addition, high-order spurious harmonics are also spreading at $2f_{LO}$, $3f_{LO}$, ... in spectrum. Two different terms contribute to the spectral properties of real-world oscillator: phase noise and spurious tones. Phase noise represents random phase fluctuations that is labeled as $\mathcal{L}(f_m)$ in Figure 3.9(b), while
spurious tones $S(f_m)$ are isolated parasitic frequency components that are unwanted by-products generated in the process of LO synthesis. $f_m$ denotes the offset frequency from center frequency $f_{LO}$.

Phase noise is a measure of noise power in 1 Hz bandwidth at $f_m$ relative to the power of signal, i.e.

$$\mathcal{L}(f_m) = \frac{P_{\text{noise}}(f_m)}{P_{\text{signal}}} \text{ dBc/Hz.} \quad (3.21)$$

Similarly, spurious tone is also defined as power ratio between spur and signal:

$$S(f_m) = \frac{P_{\text{spur}}(f_m)}{P_{\text{signal}}} \text{ dBc} \quad (3.22)$$

Since spur is generally treated as a spectral impulse, no frequency bandwidth is associated with it.

In general, phase noise affects receiver system performance through two mechanisms. First, phase noise transfers in-band and out-of-band blockers into desired signal band through reciprocal mixing. This mechanism particularly bothers narrow-band communication systems. Analysis on blocking profiles, together with the required carrier-to-interferer ratio of system, determines phase noise requirements at different offset frequencies from carrier. Second, phase noise corrupts signal constellation in I/Q plane by shifting constellation points with a common phase error, and smearing the points due to its random noise origin. The consequence is that system BER is degraded. This mechanism is more pronounced in broad-band communications and it is reflected in the requirement of integrated phase noise within the signal bandwidth or maximum tolerable rms phase error. Meanwhile, frequency spurs act very similarly to phase noise. They reciprocal-mix RF interfering signal down into signal bands and contribute distinct additive terms in integrated phase noise.
3.3.1 Phase Noise Model

In order to construct a framework to derive LO phase noise, a phase noise characteristic model is needed. Because free running oscillator is rarely used in practical design, we establish the model with the assumption that a phase-locked loop is used to generate LO frequency. And this assumption is valid in most modern wireless receivers.

A well-known linear phase domain PLL model is depicted in Figure 3.10. Noise contribution from each PLL building blocks is assumed to be additive. $\theta_{REF}$, $\theta_{PFD}$, $\theta_{VCO}$, $\theta_{DIV}$, $I_{n,CP}$, and $V_{n,LF}$ represent noise sources from frequency reference, phase-frequency detector (PFD), VCO, frequency divider, charge pump (CP) and loop filter (LF), respectively. Transfer functions for charge pump, loop filter, VCO and divider are $\frac{I_{CP}}{2\pi}$, $F(s)$, $\frac{2\pi K_{VCO}}{s}$ and $\frac{1}{N}$, respectively.

Without diving into detailed derivations, we can prove that the noise contributions from different components show distinct transfer characteristics at PLL output.
Figure 3.11: Phase noise characteristics of a typical charge-pump PLL.

Noise from reference, CP, divider, PFD demonstrates a low-pass type frequency response, while noise originated from VCO core and VCO tuning line is rejected at low frequencies. Therefore, the phase noise power spectral density of a typical stand-alone charge-pump PLL looks approximately like the one in Figure 3.11, where low-frequency PLL noise floor $L_{PLL,nf}$ is dominated by noise from PFD, CP, reference, and divider, high-frequency phase noise is limited by phase noise from VCO. Another factor that needs to be considered is the noise contribution from post-PLL circuits such as driving buffer stage or duty-cycle correction stage. These blocks usually do not suffer from the noise upconversion in VCO [27], and affect only noise floor of phase noise power spectrum.

Consider both PLL phase noise characteristics and post-PLL processing stages, we model the phase noise spectral characteristics ([11, 28–30]) using a white noise spectral function multiplied by a low-pass filter with 3 dB bandwidth $f_C$ and far-out noise floor, as shown in Figure 3.12. In Figure 3.12, $f_m$ is the offset frequency from LO center frequency, $f_C$ is the corner frequency (a.k.a. loop bandwidth) of the PLL, $f_W$ is the starting frequency when far-out white noise is dominant over oscillator noise,
and $L(f_m)$ is the phase noise power spectral density (PSD) relative to carrier power. $L_{w,nf}$ is the far-out white PLL noise floor, and the transition band of LPF features a $-20\,\text{dB/dec}$ slope that reflects $1/f^2$ regime in Leeson’s classical VCO phase noise model [31]. This model is adopted throughout this dissertation in determining phase noise requirements on local oscillator for general wireless transceivers.

### 3.3.2 Blocker-specified Phase Noise Requirements

The principle of determining phase noise requirements based on blocking profile is illustrated in Figure 3.13. In narrow-band wireless communications, the LO sideband tail often spreads into adjacent channel, alternate channel and even out-of-band frequencies. With the presence of interfering signals in these frequency bands, phase noise reciprocal-mixes with these interferers generating in-channel interferers at IF. For example, blocking signal at $f_{RF} + f_D$ in Figure 3.13 reciprocal-mixes with sideband phase noise at $L(f_D)$, which results in the IF interferer $I$. The interferer at the output of mixer will add to system noise floor $N$, and end up with total unwanted power level $N + I$. Normally, the allowed carrier-to-noise-interferer ratio $C/(N + I)$
Figure 3.13: Principle of determining LO phase noise requirements based on blocking profile.

to ensure required BER is given in radio specifications for a certain wireless standard. If assuming interferer $I$ below system noise floor $N$, allow 3 dB margin, the minimum $C/I$ can be expressed in terms of $C/N$ as [30]

$$(C/I)_{\text{min}} > (C/N)_{\text{min}} + 3 \text{ dB}$$  \hspace{1cm} (3.23)

If the required signal-to-interferer ratio at mixer output, power level of an RF blocker and desired signal bandwidth are known, the corresponding LO phase noise is required to be lower than

$$\mathcal{L}(f_m) = P_S - (C/I)_{\text{min}} - P_B - 10 \cdot \log_{10}(BW) + A_F.$$  \hspace{1cm} (3.24)

where $P_S$ is the power of intended signal, $P_B$ is the power of the blocker, and $BW$ is the signal bandwidth. Without losing generality, an attenuation factor $A_F$ (a negative quantity) is introduced to account for the rejection to blockers due to all RF components including pre-select filter, T/R switch, balun and LNA, prior to
downconversion mixer. An important observation from (3.24) is that the phase noise requirement determined by out-of-band blockers can be relaxed if some interferer suppression can be provided in any stage prior to down-conversion mixing. One possible and popular solution is to use a pre-select filter prior to LNA, and this method is widely adopted in practical radio realizations.

3.3.3 Integrated Phase Noise

Besides reciprocal mixing with RF interferers, phase noise tends to be troublesome in OFDM-based broadband wireless communications. As mentioned above, phase noise in OFDM systems introduces two different effects: common phase error and inter-carrier interference (ICI) [28, 32]. Common phase error leads to rotation of constellation in I/Q diagram for phase modulated signals, while ICI destroys inter-carrier orthogonality smearing signal constellations. Both effects cause signal-to-noise ratio (SNR) degradation of received signals, however, the damage from common phase error can be minimized by introducing pilots tones. In addition, PLL loop bandwidth $f_C$ is usually designed to be large, which is the case in UWB systems in order to cope with fast settling requirements, common phase error becomes less a problem than ICI. Unfortunately, ICI originates from the Gaussian random process characteristics of phase noise, hence its impacts can only be partially offset in practice.

Treat phase noise as a phase modulated single-tone carrier, its PSD can be mathematically written as

$$S_{\phi}(f_m) = S_{\phi W}(f_m) \cdot |H_{LPF}(f_m)|^2$$

(3.25)
where $S_{\phi w}(f_m) = \sigma_w^2$ is the power spectral density of the white Gaussian random noise that is used to modulate LO carrier [28]. The degradation to signal-to-noise-ratio $D_{SNR}$ due to LO phase noise can be expressed as

$$D_{SNR} = 10 \cdot \log_{10} \left( 1 + \frac{\sigma_w^2 E_s}{N_0} \right)$$

where $E_s$ is the symbol energy and $N_0$ is the power spectral density of additive white Gaussian noise.

It is interesting to notice the relationship between $\sigma_w^2$ and phase noise shown in Figure 3.12 [33]:

$$\sigma_w^2 = \int_0^B \mathcal{L}(f_m) df_m$$

$f_0^B \mathcal{L}(f_m) df_m$ is actually the integrated phase noise throughout the signal bandwidth of interest. This way, the LO phase noise characteristics can be derived directly from the minimum allowed SNR degradation during signal reception. MB-OFDM UWB specifies the maximum allowed rms phase error as $\Phi_{rms} = 3.5^\circ$ and it is translated to integrated phase noise by

$$\Phi_{rms} = \frac{180}{\pi} \sqrt{\int_0^B \mathcal{L}(f_m) df_m}$$

and that is to say $\Phi_{rms}$ is in fact equivalent to $\sigma_w$.

### 3.3.4 Spurious Suppression

Similar to the mechanism of phase noise to influence signal reception, unwanted spurious tones in LO may also mix out-of-band blockers down to analog baseband. As shown in Figure 3.14, spur $S(f_D)$ in LO spectrum mixes with an RF interferer at frequency $f_{RF} + f_D$, which produces an interfering signal $I$ at IF. The maximum
allowed $I$ is defined exactly the same as in (3.23). Therefore, starting from out-of-band blocking profile, the maximum allowed spurious tones in LO are determined by

$$S(f_m) = P_S - (C/I)_{\text{min}} - P_B + A_F \text{ (dBc)}.$$  

(3.29)

Similar to (3.24), pre-filtering of out-of-band blockers also help suppress spurious tones.

### 3.4 MB-OFDM UWB System Considerations

With all the principles and models in position, we are ready to pursue the system design of MB-OFDM UWB receivers. In this section, we will utilize those theories within the context of UWB communications.

As shown in Figure 3.15, a fully-integrated direct-conversion receiver is the target of this design. As discussed in previous sections, direct-conversion architecture inherently allows high integration level and simple analog processing chain than other
popular architectures. In fact, some properties of MB-OFDM UWB are rather favorable to zero-IF architecture. For instance, MB-OFDM UWB uses a 4.125 MHz sub-carrier bandwidth and carries no information at frequency zero. As a result, DC offset cancellation schemes can be simplified by inserting a high corner-frequency high-pass filter or a low-order servo loop at baseband with negligible influence on BER.

3.4.1 Wireless Link Analysis

One of the major purposes of performing wireless link analysis is to estimate important system parameters such as total noise figure and sensitivity, and make trade-offs between performance and technical difficulties, based upon the application scenario of intended wireless standards. During this process, both operating frequencies, total emission power, path loss and other important quantities will be determined accordingly [1,6].
The conceptual model used to perform wireless link analysis is depicted in Figure 3.16. To facilitate the derivations of this section, the major steps towards an estimate of receiver sensitivity are summarized here first, and principles behind these steps are given in details later on.

1. Decide operating frequency range $f_L$ and $f_U$;

2. Calculate transmit power $P_{TX}$ based on frequencies and power specifications $EIRP$;

3. Compute wireless path loss $P_{Loss}$ between transmitter and receiver;

4. Determine minimum received power $P_{RX}$ at receiver antenna port;

5. Find out noise power level at receiver antenna $N_{in}$;

6. Estimate RX noise figure $NF_{avg}$, and implementation loss $L$;

7. Determine required receiver sensitivity $S_{min}$ and design margin $M$ based on required $E_b/N_0$. 

Figure 3.16: Conceptual model of performing wireless link analysis.
At first, system operating frequencies should be decided. Recall that the original MB-OFDM proposal allocates band group 2 with 4752–6336 MHz, which overlaps with U-NII band occupied by WLAN devices. When UWB communication happens in this band group, it is very difficult to discriminate desired UWB signals from strong WLAN blockers, thus powerful A/D converters with extremely large dynamic range are required to digitize heavily contaminated waveform to detect UWB signals in digital domain. Realization of these ADCs is actually impractical at present. A feasible resolution is to abandon using band group 2 and only to aim at band groups 1, 3, 4, and 5. And the flexibility of dropping contaminated frequency band is actually one of the advantages of MB-OFDM UWB. Based upon this assumption, only band groups 1, 3, 4, and 5 are considered in this dissertation.

The spectral mask for UWB devices is specified in Figure 2.3. With the knowledge of operating frequencies, total transmission power can be determined by

\[ P_{TX} = \int_{f_L}^{f_U} EIRP(f)df \]  

(3.30)

where \( f_U \) and \( f_D \) are the upper and lower limits of operating frequency band, respectively. Assume flat power spectral density \( EIRP = -41.25 \) dBm/MHz for entire UWB spectrum, then the total transmission power is

\[ P_{TX} = -41.25 + 10 \cdot \log_{10}(11 \times 528) = -3.61 \text{ dBm}. \]  

(3.31)

In order to evaluate the signal power at receiver antenna input, path loss needs to be calculated to account for signal attenuation between transmitter and receiver. A free-space propagation model is used in MB-OFDM UWB. In addition, since RF carrier signal actually jumps around all UWB bands, we assume the hopping follows a randomly distributed pattern. Thus the geometric center frequency of upper and
lower frequency limits is used for calculating average path loss. $f_G$ is expressed as $f_G = \sqrt{f_L \cdot f_U}$. The free-space path loss in dB scale can be written as

$$P_{\text{Loss}} = 20 \cdot \log_{10} \left( \frac{4\pi f_G d}{c} \right)$$

in which $d$ is distance between transmitter and receiver, and $c$ is the speed of light in free space. As an example, for $f_L = 3168$ MHz and $f_U = 10560$ MHz, $f_G \approx 5784$ MHz; consequently, $P_{\text{Loss}}$ is calculated as 67.7 dB at $d = 10$ meters. Therefore, the minimum signal power at the receiving antenna (Plane A in Figure 3.16) can be determined by applying the maximum operating distance for a certain data rate, and taking into consideration of power gains of TX antenna $G_{\text{ant,TX}}$ and RX antenna $G_{\text{ant,RX}}$. Mathematically, $P_{\text{RX}}$ is given as

$$P_{\text{RX}} = P_{\text{TX}} - P_{\text{Loss}} + G_{\text{ant,TX}} + G_{\text{ant,RX}}.$$  \hspace{1cm} (3.33)

Generally, isotropic antennas are assumed for both TX and RX, thus we have $G_{\text{ant,TX}} = G_{\text{ant,RX}} = 0$ dB.

The next step is to compute ambient noise power at RX antenna (Plane A). Given a data rate $R_b$, the corresponding noise power per bit is given as

$$N_{\text{in}} = -10 \cdot \log_{10} (kT_0) + 10 \cdot \log_{10} (R_b) = -174 + 10 \cdot \log_{10} (R_b)$$  \hspace{1cm} (3.34)

here $R_b$ instead of frequency bandwidth $B$ is used.

To calculate the noise power at the input of digital detection and demodulation unit (Plane B in Figure 3.16), a reasonable estimate of total receiver noise figure must be carried on. For UWB Mode 1 operation, a 6.6 dB noise figure is anticipated [1,6]. To target 1-3-4-5 band groups, when circuit noise performance degradation at higher frequencies is taken into consideration, an average noise figure $NF_{\text{avg}} = 8.6$ dB would
Table 3.1: Wireless channel analysis for MB-OFDM UWB band group 1-3-4-5.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Value</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Rate $R_b$ (Mb/s)</td>
<td>110</td>
<td>200</td>
<td>480</td>
</tr>
<tr>
<td>Distance $d$ (m)</td>
<td>10</td>
<td>4</td>
<td>2</td>
</tr>
<tr>
<td>Total TX power $P_{TX}$ (dBm)</td>
<td>-3.61</td>
<td>-3.61</td>
<td>-3.61</td>
</tr>
<tr>
<td>Geometric Center Frequency $f_G$ (MHz)</td>
<td>5784</td>
<td>5784</td>
<td>5784</td>
</tr>
<tr>
<td>TX antenna gain $G_{ant,TX}$ (dBi)</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Path loss @ 1 m (dB)</td>
<td>47.7</td>
<td>47.7</td>
<td>47.7</td>
</tr>
<tr>
<td>Path loss @ $d$ m (dB)</td>
<td>67.7</td>
<td>59.7</td>
<td>53.7</td>
</tr>
<tr>
<td>RX antenna gain $G_{ant,RX}$ (dBi)</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>RX power $P_{RX}$ (dBm)</td>
<td>-71.3</td>
<td>-63.3</td>
<td>-57.3</td>
</tr>
<tr>
<td>Noise per bit at antenna $N_{in}$ (dBm)</td>
<td>-93.6</td>
<td>-91.0</td>
<td>-87.2</td>
</tr>
<tr>
<td>RX noise figure $NF_{avg}$ (dB)</td>
<td>8.6</td>
<td>8.6</td>
<td>8.6</td>
</tr>
<tr>
<td>Noise per bit at digital input $N_b$ (dBm)</td>
<td>-85.0</td>
<td>-82.4</td>
<td>-78.6</td>
</tr>
<tr>
<td>Required $E_b/N_0$ (dB)</td>
<td>4.0</td>
<td>4.7</td>
<td>4.9</td>
</tr>
<tr>
<td>Implementation loss $L$ (dB)</td>
<td>2.5</td>
<td>2.5</td>
<td>2.5</td>
</tr>
<tr>
<td>RX sensitivity $S_{min}$ (dBm)</td>
<td>$-78.5$</td>
<td>-75.2</td>
<td>-71.2</td>
</tr>
<tr>
<td>Link margin $M$ (dB)</td>
<td>7.2</td>
<td>11.9</td>
<td>13.9</td>
</tr>
</tbody>
</table>

be a realistic reference number. Therefore, the noise at Plane B is then

$$N_0 = N_{in} + NF_{avg}.$$ (3.35)

In digital communications, a certain data rate and digital modulation scheme usually correspond to a pre-defined ratio between signal power and noise power floor, namely, $E_b/N_0$, at Plane B. When $N_0$ is known, the minimum required signal power is equivalently known. In actual receiver design, front-end filtering, clipping at DAC, ADC degradation and other non-ideal effects can cause the loss of signal to noise ratio, which is often referred implementation loss [6]. If an implementation loss is assumed to be $L = 2.5$ dB, then the minimum required signal power at Plane A, or the receiver
sensitivity $S_{\text{min}}$, is calculated as

$$S_{\text{min}} = N_0 + \frac{E_b}{N_0} + L \text{ (dBm)}. \quad (3.36)$$

Finally, an additional design margin $M$ is defined as the difference between $S_{\text{min}}$ and actual RX input power $P_{\text{RX}}$. The existence of this margin allows the relaxation of receiver performance requirements in sub-optimal designs. $M$ is expressed mathematically as

$$M = P_{\text{RX}} - S_{\text{min}}. \quad (3.37)$$

It is obvious that the smaller $M$ is, the more demanding the receiver noise requirements are.

As the results of the aforementioned wireless link budget analysis, a worksheet is given in Table 3.1 to calculate receiver sensitivities and design margins for MB-OFDM UWB at different data rates. It is noticed that data transmission with 110 Mb/s at 10 m distance gives most stringent sensitivity requirement and lowest implementation margin.

### 3.4.2 UWB Blocking Profile Analysis

Wireless link analysis essentially provides two important receiver parameters: sensitivity and noise figure. To arrive at other requirements, identifying important RF interferers for UWB systems is crucial. This subsection is exclusively dedicated to this topic.

Unlike narrow-band communication systems, MB-OFDM UWB systems define out-of-band blockers as all interfering signals outside the intended 528 MHz frequency band in which data are transferred. These include both peer UWB signals and other alien RF signals such as WLAN, Bluetooth, Zigbee and cellular phone transmissions.
The spectral profile of most dominant blockers in the United States is depicted in Figure 3.17. Inspect the blocking profile, it is noticeable that 802.11a transmission signals within 5–6 GHz pose the biggest threats. For instance, the power of 802.11a transmission signal at 5125 MHz can be as high as 16 dBm, which is $16 - (-78.5) = 94.5$ dB stronger than UWB RX sensitivity, but only 662 MHz away from the center of Band 3; similarly, WLAN signal at 5850 MHz, which is 750 MHz away from the center of Band 7, can be in excess of 100 dB larger than minimum UWB retrievable signal.

The strong transmission power of these out-of-band interferers introduces more severe challenges to UWB radio than to narrow band wireless applications. These interferers affect four major receiver parameters: LO far-out phase noise floor, unwanted spurious tones in LO, RF front-end linearity, and IF band-selection filter requirements.
<table>
<thead>
<tr>
<th></th>
<th>Minimum Separation (m)</th>
<th>Preselect Filter Attenuation (dB)</th>
<th>Baseband filter Attenuation (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Microwave Oven</td>
<td>0.16</td>
<td>35</td>
<td>35.4</td>
</tr>
<tr>
<td>Bluetooth &amp; 802.15.1</td>
<td>0.02</td>
<td>35</td>
<td>36.9</td>
</tr>
<tr>
<td>802.11b &amp; 802.15.3</td>
<td>0.2</td>
<td>35</td>
<td>36.9</td>
</tr>
<tr>
<td>802.11a</td>
<td>0.2</td>
<td>30</td>
<td>30.7</td>
</tr>
<tr>
<td>802.15.4</td>
<td>0.02</td>
<td>35</td>
<td>35.6</td>
</tr>
</tbody>
</table>

Table 3.2: RF interferers and required attenuations in UWB radio [1].

Fortunately enough, MB-OFDM UWB proposal [1] proposed minimum spatial separations between interfering transmitters and UWB receivers in order to mitigate the detrimental influence of the blocker and ensure proper operation of UWB devices. These distances force propagation path loss of harmful RF signals before reaching UWB devices so as to prevent them from jamming or desensitizing receiver, and render adequate design margins to realistic UWB receiver implementations. The pass loss, combined with suppressions from RF filter and baseband filter of UWB devices, ensures the $E_b/N_0$ requirement can be possibly satisfied. The proposed minimum separations between interferers and UWB devices, and corresponding pre-select filter and baseband filter attenuations are listed in Table 3.2.

Pre-select RF filtering plays an important role in UWB receiver design. Protecting UWB receivers with a certain amount of prefiltering $A_F$ can take away a lot of burden on RF front-end linearity, baseband filtering, and LO phase noise and frequency spurs. Recall that in (3.24, 3.29) phase noise and spurious tone specifications can be relaxed if some interferer rejections $A_F$ can be provided from any stage prior to down-conversion mixing.
Figure 3.18: An ideal pre-select filter for UWB applications.

It is reasonable to anticipate a moderate stopband attenuation $A_F$ provided by RF pre-select filter (20 dB in [10] and 30–35 dB in [1]), but the difficulty is how to realize this pre-select filter. One option is to employ a dynamically tuned filter to protect intended UWB band. But since the operating UWB frequency is constantly leaping between different bands, it is impractical to acquire such a filter that is able to keep pace of the hopping. Another option is to utilize a pre-select filter with fixed spectral characteristics. It is supposed to have low insertion loss in 3.1–4.8 GHz and 6.2–10.6 GHz UWB bands, and good attenuations to otherwise frequencies, as shown in Figure 3.18. It is not surprising that obtaining this filter off-the-shelf is nontrivial.

It is also viable to squeeze some interferer rejection out of LNA (or balun, if used). By choosing its circuit architecture wisely, LNA can provide additional frequency selectivity and in turn ease the design of LO and channel-select filters. But the extra benefit does not come without penalty. Without pre-filtering, LNAs are directly exposed to strong blockers, which tightens its linearity requirements. Furthermore, depending on the spectral selectivity of LNA, relaxation on LO and baseband filter specifications may be quite limited after all.
3.4.3 LO Phase Noise Specifications

Phase noise requirements of MB-OFDM UWB LOs are determined by two factors: out-of-band blockers and integrated phase noise requirement.

At first, we observe that out-of-band blockers are relatively far way from UWB band center frequencies. Referring Figure 3.19, the effect of reciprocal mixing takes place at noise floor regime of local oscillator. Thus the power levels of blockers (denoted as $P_{\text{INT}}$) can only be translated to LO far-out phase noise floor. For each RF blocker, the corresponded upper bound of phase noise floor is calculated and shown in Table 3.3. In Table 3.3, path loss is computed from the minimum spatial separation listed in Table 3.2. It is noticeable that 802.11a interferers at 5725–5850 MHz dictate the LO phase noise floor. Therefore, to ensure negligible reciprocal mixing, $L_{M,nf} < -159$ dBc/Hz.

Secondly, close-in phase noise requirements can be derived on the basis of integrated phase noise requirement, phase noise model in Figure 3.19 and far-out noise floor given above. The corner frequency $f_C$ is assumed to be 100 kHz in order to...
balance PLL settling time and loop stability. Recall that for a single-pole system similar to the one in Figure 3.19, we have [34]

$$\int_0^{f_w} L(f_m)df_m = \int_0^{\frac{\pi}{f_C}} L_{PLL, nf}df_m$$

Therefore, the integrated phase noise within the UWB bandwidth $B$ is dictated by

$$\text{Integrated phase noise power} = \frac{\pi}{2} f_C \cdot 10^{\frac{L_{PLL, nf}}{10}} + B \cdot 10^{\frac{L_{W, nf}}{10}}$$

where $L_{PLL, nf}$ and $L_{W, nf}$ are express in dBc/Hz. Recall from (3.28), the integrated phase noise power normalized to carrier can be expressed in terms of rms phase error, which gives

$$\frac{\pi}{2} f_C \cdot 10^{\frac{L_{PLL, nf}}{10}} + B \cdot 10^{\frac{L_{W, nf}}{10}} = \left( \frac{\pi}{180} \cdot \Phi_{rms} \right)^2. \quad (3.40)$$

Given rms phase error $\Phi_{rms} = 3.5^\circ$, solving (3.40) results in PLL noise floor $L_{PLL, nf} = -76.2$ dBc/Hz and phase noise $L(1 MHz) = -96.2$ dBc/Hz.

Table 3.4 summarizes the fundamental requirements on UWB frequency synthesizer, where the corner frequency $f_C = 100$ kHz. Increasing $f_C$ will put tougher specification to PLL noise floor but relax the phase noise requirement at 1 MHz, which is primarily limited by VCO. For example, if $f_C$ is chosen to be 500 kHz, $L_{PLL, nf}$ becomes $-83.3$ dBc/Hz while $L(1 MHz) = -89.3$ dBc/Hz. This trade-off demands further exploration during actual circuit implementation.

### 3.4.4 LO Frequency Spur Requirements

Unlike the case in narrow-band systems in which high order harmonics in LO are far away from signal band and are easily filtered out, the LO spurious tones in UWB systems are often critical. For example, if UWB device 1 has an LO operating at $f_B = 3432 MHz = 6.5 \times 528 MHz$ on band 1, the LO’s 3$^{rd}$-order harmonics at

$$L_{PLL, nf}$$

and $L_{W, nf}$ are express in dBc/Hz. Recall from (3.28), the integrated phase noise power normalized to carrier can be expressed in terms of rms phase error, which gives

$$\frac{\pi}{2} f_C \cdot 10^{\frac{L_{PLL, nf}}{10}} + B \cdot 10^{\frac{L_{W, nf}}{10}} = \left( \frac{\pi}{180} \cdot \Phi_{rms} \right)^2. \quad (3.40)$$

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<table>
<thead>
<tr>
<th>Parameters</th>
<th>Peer UWB</th>
<th>Bluetooth</th>
<th>802.11b/g</th>
<th>802.11a</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>(a)</td>
<td>(b)</td>
</tr>
<tr>
<td>Lower frequency (MHz)</td>
<td>3128</td>
<td>2400</td>
<td>2400</td>
<td>5150</td>
</tr>
<tr>
<td>Upper frequency (MHz)</td>
<td>10560</td>
<td>2484</td>
<td>2484</td>
<td>5250</td>
</tr>
<tr>
<td>Max power (dBm)</td>
<td>-14.3</td>
<td>0</td>
<td>20</td>
<td>16</td>
</tr>
<tr>
<td>Spatial distance (m)</td>
<td>0</td>
<td>0.02</td>
<td>0.2</td>
<td>0.2</td>
</tr>
<tr>
<td>Closest UWB (MHz)</td>
<td>varies</td>
<td>3432</td>
<td>3432</td>
<td>4488</td>
</tr>
<tr>
<td>Spectral distance (MHz)</td>
<td>264</td>
<td>948</td>
<td>948</td>
<td>662</td>
</tr>
<tr>
<td>Path loss (dB)</td>
<td>8.4*</td>
<td>6.4</td>
<td>26.4</td>
<td>32.7</td>
</tr>
<tr>
<td>Input power (dBm)</td>
<td>-22.6</td>
<td>-6.4</td>
<td>-6.4</td>
<td>-16.7</td>
</tr>
<tr>
<td>$L_{W_{uf}}$ (dBc/Hz)</td>
<td>-141.1</td>
<td>-157.4</td>
<td>-157.4</td>
<td>-147.0</td>
</tr>
<tr>
<td>Spurious rejection (dB)</td>
<td>-53.9</td>
<td>-70.1</td>
<td>-70.1</td>
<td>-59.8</td>
</tr>
<tr>
<td>Spurious rejection (dB) with 30 dB prefiltering</td>
<td>-23.9</td>
<td>-40.1</td>
<td>-40.1</td>
<td>-29.8</td>
</tr>
</tbody>
</table>

* Lowest UWB frequency 3128 MHz is used as the worst-case scenario.

Table 3.3: Worksheet for deriving phase noise and spurious suppression requirements from out-of-band blockers.
2904 + 528 × n_b, n_b = 1–3, 7–14

Switching time (ns) < 9.47

\( \mathcal{L}_{PLL, nf} \) (dBc/Hz) < −76.2
\( \mathcal{L}(1 \text{ MHz}) \) (dBc/Hz) < −96.2
\( \mathcal{L}_{W, nf} \) (dBc/Hz) < −158.9

Out-of-band Spurs (dBc) < −41.7

Table 3.4: Summary of Frequency Synthesizer Requirements.

\( f_B = 10296 \text{ MHz} = 3 \times 6.5 \times 528 \text{ MHz} \) is located at the center of band 14. If a second UWB device happens to transmit data on band 14, all the signals will be mixed down by the harmonics in device 1 LO, corrupting its transmission on band 1. This problem becomes much more serious if SSB-mixer based frequency synthesizers are used, because mismatches, nonlinearities and distortions in SSB-mixer, frequency divider and multiplexer will create a number of harmonic contents and make it very difficult to control their spectral locations and power levels after several stages of frequency mixing.

Following the equation (3.29), spurious suppression requirements can be easily calculated. Table 3.3 summarizes the calculated phase noise and spurious suppression specifications derived from out-of-band blockers. It is worth to notice that even without any pre-filtering, the LO phase noise requirements are fairly generous. However, it will be difficult to meet spurious suppression requirements without the assistance of RF blocks prior to down-conversion mixer.

Table 3.4 summarizes the most important requirements for UWB local oscillator. All phase noise and levels are calculated without considering RF pre-select filter
attenuation, while a 30 dB rejection is expected in determining spur suppression requirements.

3.4.5 System Linearity Requirements

RF front-end linearity is essentially determined by out-of-band interferers [10,11,35]. Once power levels of the interferers are referred to the RF input port of a UWB receiver, their second-order and third-order intermodulation (IM) terms $P_{IM_2}$ and $P_{IM_3}$ due to receiver nonlinearity could be calculated from (3.14) and (3.13):

\[ P_{IM_2}(\text{dBm}) = 2 \times P_{\text{int}}(\text{dBm}) - IIP_2(\text{dBm}) \]  
\[ P_{IM_3}(\text{dBm}) = 3 \times P_{\text{int}}(\text{dBm}) - 2 \times IIP_3(\text{dBm}). \]

In order to make sure that the yielded intermodulation terms do not disturb data detection performance, the maximum $P_{IM}$ is determined as follows. Recall in Table 3.1, average noise power per bit $N_b$ at 110 Mb/s data rate is $-85$ dBm. Since receivers are specified to work with input signal power 6 dB higher than sensitivity $S_{\text{min}} = -78.5$ dBm, a 6 dB margin is allowed to noise power as well. The maximum allowed noise power is then $-79$ dBm. Assume the interferer is required to be 3 dB lower than noise power, then the required intermodulation tone needs to be around the neighborhood of $-82$ dBm.

\[ P_{IM_2} < -82 \text{ dBm} \]
\[ P_{IM_3} < -82 \text{ dBm} \]

In UWB systems, when two distantly spaced RF interferers are passed into second-order and third-order nonlinearity, their frequency sum or difference expressed in (3.7) might fall into intended signal bands. For instance, two RF jamming signals at 2.4
GHz and 5.8 GHz, may create a second-order intermodulation at their frequency sum of 8.2 GHz, within the range of UWB band-10, while the frequency difference at 3.4 GHz falls into UWB band-1. Meanwhile, third-order nonlinearity of receiver front-end could also generate an IMD at $2 \times 5.8 - 2.4 = 9.2$ GHz, which interferes RF transmission in band-12. As another example, second-order nonlinearity on two 2.4 GHz jammers could generate harmful frequency tone near DC and 4.8 GHz tone in band 4; or third-order nonlinearity could produce a tone at $3 \times 2.4 = 7.2$ GHz in band-8.

Inspecting Table 3.3 reveals that 802.11a blockers at 5.8 GHz and 802.11b/g at 2.4 GHz are most threatening, because their powers at antenna input port are the strongest. The worst-case $IIP_2$ comes from the scenario where two 5.8 GHz, $-4.8$ dBm blockers arrive at receiver input. Assuming 30 dB attenuation due to pre-select filter, the required $IIP_2$ is calculated as

$$IIP_2 > 2 \times (-4.8 - 30) - (-82) = 12.4 \text{ dBm}.$$  

Similarly, the worst-case $IIP_3$ requirement is determined by the scenario where one 5.8 GHz, $-4.8$ dBm and one 2.4 GHz, $-6.4$ dBm blockers are fed into a UWB receiver simultaneously. More conservatively, assume the power of the two tones are both at $-4.8$ dBm, and again 30 dB suppression from RF filtering, the $IIP_3$ is calculated as

$$IIP_3 > \frac{3 \times (-4.8 - 30) - (-82)}{2} = -11.2 \text{ dBm}.$$  

It is obvious that the RF pre-select filter is crucial to receiver linearity. Repeat the calculations above without pre-select filter, one can easily find out $IIP_2 > 72.4$ dBm and $IIP_3 > 33.8$ dBm are required, which are almost impossible to achieve in modern CMOS technologies.
Table 3.5: System requirements for MB-OFDM UWB receivers.

<table>
<thead>
<tr>
<th>Requirement</th>
<th>Requirement</th>
</tr>
</thead>
<tbody>
<tr>
<td>Receiver Sensitivity (dBm)</td>
<td>-78.5</td>
</tr>
<tr>
<td>System Noise Figure (dB)</td>
<td>&lt; 8.6</td>
</tr>
<tr>
<td>Pre-select filter attenuations (dB)</td>
<td>30</td>
</tr>
<tr>
<td>$IIP_2$ (dBm)</td>
<td>&gt; 12.4</td>
</tr>
<tr>
<td>$IIP_3$ (dBm)</td>
<td>&gt; −11.2</td>
</tr>
<tr>
<td>$L_{W, nf}$ (dBc/Hz)</td>
<td>&lt; −158.9</td>
</tr>
<tr>
<td>LO Out-of-band Spurs (dBc)</td>
<td>&lt; −41.7</td>
</tr>
</tbody>
</table>

As a summary, Table 3.5 lists basic system-level requirements for MB-OFDM UWB receivers.

### 3.5 Selection of UWB RF Front-end Architectures

#### 3.5.1 Design Objectives

The selection of RF front-end architecture is critical to the successful design of a UWB receiver because of two important factors.

First, LO spur specifications asks for additional filtering provided by RF front-end. Investigating Table 3.3, spur level of $-41.7$ dBc is relatively challenging to achieve [2,36], especially in SSB-mixer based CMOS solutions where device matching at multiple GHz is difficult. Some extra rejection to out-of-band blockers could ease the design UWB synthesizer.

Second, linearity requirements demonstrate a trade-off between front-end components. As a consequence, the architecture needs to be picked before diving into
receiver gain/noise/linearity partitioning and block-level specifications. To appreciate this trade-off, we have to get back to the intermodulation issues in zero-IF UWB receivers.

All direct-conversion receivers suffer from low-frequency components caused by $IMD_2$ when two closely spaced strong blockers fed into receiver nonlinearity. The low-frequency voltage signal leaks into analog baseband chain directly, and saturates following stages. Fortunately, in most cases only second-order nonlinearity in down-conversion mixers really matters, especially when a large AC-coupling capacitor is inserted between LNA and mixer. The propagation of low-frequency $IM_2$ along RF front-end is shown in Figure 3.20, where the large capacitor basically confines low-frequency IM products generated by pre-mixer blocks to these blocks only. Therefore, second-order linearity of mixer is critical, because its $IMD_2$ could sneak into analog baseband directly.
On the other hand, high frequency $IM_2$ components experience different propagating path. Shown in Figure 3.21, since RF $IM_2$ components are located right in-band, they can spread together with intended RF signals all the way into analog baseband without any attenuation. Therefore, not only the $IMD_2$ of mixer demands attention, but also the $IMD_2$ of pre-mixer RF blocks (LNA, Balun and pre-select filter) need to be carefully minimized.

### 3.5.2 LNA Spectral Characteristics

In terms of spectral characteristics, LNA design strategies can be categorized into three different types: single-band LNA, concurrent or double-band LNA(s), and multi-band or multiple LNA(s). Their frequency domain representations are shown graphically in Figure 3.22.

The first possibility in Figure 3.22(a) is to have one LNA simply spanning across 3.1–10.6 GHz range [12, 13, 37]. Despite its simplicity, this solution has one major
drawback – the interfering 802.11a signals are right in the middle of LNA effective gain spectrum. No attenuation to 5-GHz blockers is provided by front-end. In order to achieve extremely broad bandwidth, multiple on-chip passive circuit elements are used, making this implementation relatively die- and cost-inefficient.

Towards another extreme, multiple LNAs or an LNA with multiple (or switchable) band-limiting networks in Figure 3.22(c) can be employed, with one LNA or network dedicated to one UWB band. The obvious advantage is LNA rejects all out-of-band blockers so that LO phase noise and spurious requirements can be relaxed. The price
that needs to be paid is either a large number of on-chip reactive elements or digitally controlled switching when operating band is hopping up and down. The former leads to the occupation of large silicon area, while the latter could inject switching noise to sensitive RF front-end.

Alternately, careful inspection of Table 3.3 reveals that compared with other heterogeneous out-of-band blockers, interferers from peer UWB devices usually are not of significance. This observation leads to the alternative approach in Figure 3.22(b): either a double-LNA structure or a concurrent LNA with dual-band frequency selection can be used to only tackle the most prominent 5 GHz WLAN jammers. By covering the 3.1–4.7 and 6.3–10.6 GHz ranges separately, this method not only provides a certain amount of precious pre-filtering, but also allows relatively simple design.
3.5.3 Targeted Front-End Architectures

In this work, two different versions of UWB RF front-ends shown in Figure 3.23 are designed to prove the concepts we discussed in previous sections.

The architecture of a single-ended input, differential output RF front-end is shown in Figure 3.23(a). One of the important considerations of this RFE is to tackle the difficulty of obtaining off-chip passive ultra-wideband baluns. The single-ended LNA realizes the gain spectrum in Figure 3.22(c) using tunable LC loading tank combined with common-gate gain stage. An active balun is inserted between LNA and mixers. The benefits of active baluns are their compact die size and simple topology. The major challenge is how to achieve extremely wideband amplitude and phase matching between differential signals. The gain and phase errors result in degradation of $IM_2$, hence extensive design effort is devoted to optimize this critical component.

A second RFE features a fully differential architecture. Assuming differential RF input signals fed into LNA, balun is not needed any more. The LNA employed in this RFE implements the gain band in Figure 3.22(b), which is adequate to reject most troublesome 5–6 GHz blockers. In both RFEs, fully differential or pseudo-differential double-balanced mixers are used. Double-balanced mixers are robust to common-mode noise and second-order nonlinearity, which is quite beneficial to direct-conversion receivers.

3.6 Receiver Budget Analysis

To conclude this chapter, theories and observations discussed above are applied to the budget analysis of two direct-conversion UWB receivers. As a result, block-level
<table>
<thead>
<tr>
<th>Specifications</th>
<th>Voltage Gain (dB)</th>
<th>Noise Figure (dB)</th>
<th>$IIP_3$ (dBm)</th>
<th>$IIP_2$ (dBm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>T/R switch</td>
<td>-1.0</td>
<td>1.0</td>
<td>20</td>
<td>200</td>
</tr>
<tr>
<td>Pre-select filter</td>
<td>-0.5</td>
<td>0.5</td>
<td>1000</td>
<td>200</td>
</tr>
<tr>
<td>LNA</td>
<td>12</td>
<td>3.2</td>
<td>0</td>
<td>20</td>
</tr>
<tr>
<td>Balun</td>
<td>0</td>
<td>3</td>
<td>2</td>
<td>40</td>
</tr>
<tr>
<td>Mixer</td>
<td>6</td>
<td>12</td>
<td>8</td>
<td>35</td>
</tr>
<tr>
<td>Baseband LPF</td>
<td>0</td>
<td>15</td>
<td>15</td>
<td>90</td>
</tr>
<tr>
<td>Baseband VGA</td>
<td>36</td>
<td>40</td>
<td>20</td>
<td>90</td>
</tr>
<tr>
<td>A/D Converter</td>
<td>0</td>
<td>30</td>
<td>20</td>
<td>80</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>52.5</strong></td>
<td><strong>7.6</strong></td>
<td><strong>-6.1</strong></td>
<td><strong>13.1</strong></td>
</tr>
<tr>
<td><strong>Requirement</strong></td>
<td><strong>50</strong></td>
<td><strong>8.6</strong></td>
<td><strong>-9.8</strong></td>
<td><strong>12.4</strong></td>
</tr>
</tbody>
</table>

Table 3.6: Block specifications of the balun-embedded UWB receiver.

Specifications are worked out subsequently. Because budget analysis is architecture-dependent, two subsections are dedicated separately to the two targeted receivers with different RFEs described in last section.

### 3.6.1 Receiver with Balun-embedded RFE

The front-end architecture of the balun-embedded receiver is shown in Figure 3.23(a), and Table 3.6 gives specifications of off-chip components T/R switch, pre-select filter, and on-chip blocks including LNA, balun, mixer, analog baseband channel-select filter, variable-gain amplifier and A/D converter. Only the four most critical parameters voltage gain, noise figure, $IIP_3$ and $IIP_2$, are analyzed. Spread sheet approach is adopted because it is simple, straightforward and sufficiently accurate.
<table>
<thead>
<tr>
<th>Offset Frequencies (MHz)</th>
<th>Voltage Gain (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intended UWB</td>
<td>12</td>
</tr>
<tr>
<td>528</td>
<td>8</td>
</tr>
<tr>
<td>750</td>
<td>5</td>
</tr>
<tr>
<td>762</td>
<td>5</td>
</tr>
<tr>
<td>862</td>
<td>3</td>
</tr>
<tr>
<td>948</td>
<td>2</td>
</tr>
</tbody>
</table>

Table 3.7: LNA voltage gain distribution around band center frequency in balun-embedded receiver.

The block-level specifications reflect the balance between system-level metrics, in which $IIP_2$ is the most stringent one and asks for quite an amount of compromise from other requirements. And the values of these specifications are picked by referring most currently published state-of-the-art implementations. Among these pre-determined parameters, $IIP_2$ of CG-LNA and balun are rather challenging due to their single-ended or semi-differential topologies. However, they are necessary to satisfy overall linearity requirement while not over-demanding from other blocks.

To emulate the power level of intended signals and interferers along receiver processing chain, a fifth-order baseband LPF with corner frequency $f_C = 270$ MHz is assumed. The filter order is necessary to attenuate RF blocker so as to satisfy $C/I$ ratio at the onset of digital domain (within A/D converters). In addition, because a switchable multi-band LNA is used in this architecture, we assume reasonably less voltage gain applied to out-of-band blockers than to desired UWB signals. Table 3.7 lists the LNA gain at different offset frequencies with respect to the center of the intended UWB band. The signal strength along the receiver is shown in Figure 3.24.
<table>
<thead>
<tr>
<th>Description</th>
<th>T/R Switch</th>
<th>RF Filter</th>
<th>LNA</th>
<th>Balun</th>
<th>Mixer</th>
<th>LPF</th>
<th>VGA</th>
<th>ADC</th>
<th>Final</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max. Desired Signal</td>
<td>-3.61</td>
<td>-4.61</td>
<td>-5.11</td>
<td>-5.11</td>
<td>-5.11</td>
<td>0.89</td>
<td>0.89</td>
<td>0.89</td>
<td>0.89</td>
</tr>
<tr>
<td>Min. Desired Signal</td>
<td>-72.50</td>
<td>-73.50</td>
<td>-74.00</td>
<td>-62.00</td>
<td>-62.00</td>
<td>-56.00</td>
<td>-56.00</td>
<td>-20.00</td>
<td>-20.00</td>
</tr>
<tr>
<td>802.11a interferer 750MHz away</td>
<td>-4.71</td>
<td>-5.71</td>
<td>-35.71</td>
<td>-30.71</td>
<td>-30.71</td>
<td>-24.71</td>
<td>-69.08</td>
<td>-33.08</td>
<td>-33.08</td>
</tr>
<tr>
<td>802.11a interferer 762MHz away</td>
<td>-16.78</td>
<td>-17.78</td>
<td>-47.78</td>
<td>-42.78</td>
<td>-42.78</td>
<td>-36.78</td>
<td>-81.84</td>
<td>-45.84</td>
<td>-45.84</td>
</tr>
<tr>
<td>802.11a interferer 862MHz away</td>
<td>-9.95</td>
<td>-10.95</td>
<td>-40.95</td>
<td>-37.95</td>
<td>-37.95</td>
<td>-31.95</td>
<td>-82.36</td>
<td>-46.36</td>
<td>-46.36</td>
</tr>
<tr>
<td>BT/802.11b Blocker 948.5MHz away</td>
<td>-6.22</td>
<td>-7.22</td>
<td>-42.22</td>
<td>-40.22</td>
<td>-40.22</td>
<td>-34.22</td>
<td>-88.78</td>
<td>-52.78</td>
<td>-52.78</td>
</tr>
<tr>
<td>Noise Floor (Low gain)</td>
<td>-76.36</td>
<td>-75.86</td>
<td>-75.66</td>
<td>-72.81</td>
<td>-71.23</td>
<td>-60.78</td>
<td>-58.12</td>
<td>-56.48</td>
<td>-45.96</td>
</tr>
<tr>
<td>Noise Floor (High gain)</td>
<td>-76.36</td>
<td>-75.86</td>
<td>-75.66</td>
<td>-66.81</td>
<td>-66.36</td>
<td>-59.41</td>
<td>-57.32</td>
<td>-37.91</td>
<td>-37.33</td>
</tr>
</tbody>
</table>

Figure 3.24: Signal, noise and interferer level in the balun-embedded UWB receiver.
<table>
<thead>
<tr>
<th>Offset Frequencies (MHz)</th>
<th>Voltage Gain (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intended UWB</td>
<td>15</td>
</tr>
<tr>
<td>Peer UWB 528</td>
<td>15</td>
</tr>
<tr>
<td>750</td>
<td>8</td>
</tr>
<tr>
<td>762</td>
<td>8</td>
</tr>
<tr>
<td>862</td>
<td>6</td>
</tr>
<tr>
<td>948</td>
<td>5</td>
</tr>
</tbody>
</table>

Table 3.8: LNA voltage gain distribution around band center frequency in fully-differential receiver.

### 3.6.2 Receiver with Fully-integrated RFE

Similarly, for the fully-differential receiver, block specifications and signal propagation diagram are shown in Table 3.9 and Figure 3.25, respectively. Compared with balun-embedded receiver, fully-differential RFE could potentially achieve higher $IIP_2$. This allows higher gain in RF front-end and larger controllable gain range for the entire receiver. Another benefit is the overall noise figure is lower than balun-embedded receiver.

Table 3.8 gives the gain spectral characteristics of the LNA in this architecture. As discussed in previous section, the LNA only attenuates alien interferers such as WLNA, bluetooth and cellular, but does not suppress any peer UWB signals. Therefore, peer UWB blockers will bear the same amount gain as intended UWB signals.

Figure 3.23(b) illustrates the architecture of a fully-differential RFE.
<table>
<thead>
<tr>
<th></th>
<th>T/R Switch</th>
<th>RF Filter</th>
<th>LNA</th>
<th>Mixer</th>
<th>LPF</th>
<th>VGA</th>
<th>ADC</th>
<th>Final</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Max. Desired Signal</strong></td>
<td>-3.61</td>
<td>-4.61</td>
<td>-5.11</td>
<td>-5.11</td>
<td>5.89</td>
<td>5.89</td>
<td>5.89</td>
<td>5.89</td>
</tr>
<tr>
<td><strong>Min. Desired Signal</strong></td>
<td>-72.50</td>
<td>-73.50</td>
<td>-74.00</td>
<td>-59.00</td>
<td>-48.00</td>
<td>-48.00</td>
<td>-12.00</td>
<td>-12.00</td>
</tr>
<tr>
<td>802.11a interferer 750MHz away</td>
<td>-4.71</td>
<td>-5.71</td>
<td>-35.71</td>
<td>-28.71</td>
<td>-17.71</td>
<td>-62.08</td>
<td>-26.08</td>
<td>-26.08</td>
</tr>
<tr>
<td>802.11a interferer 762MHz away</td>
<td>-16.78</td>
<td>-17.78</td>
<td>-47.78</td>
<td>-40.78</td>
<td>-29.78</td>
<td>-74.84</td>
<td>-38.84</td>
<td>-38.84</td>
</tr>
<tr>
<td>802.11a interferer 862MHz away</td>
<td>-9.95</td>
<td>-10.95</td>
<td>-40.95</td>
<td>-34.95</td>
<td>-23.95</td>
<td>-74.36</td>
<td>-38.36</td>
<td>-38.36</td>
</tr>
<tr>
<td>BT/802.11b Blocker 948.5MHz away</td>
<td>-6.22</td>
<td>-7.22</td>
<td>-42.22</td>
<td>-37.22</td>
<td>-26.22</td>
<td>-80.78</td>
<td>-44.78</td>
<td>-44.78</td>
</tr>
<tr>
<td><strong>Noise Floor (Low gain)</strong></td>
<td>-76.36</td>
<td>-75.86</td>
<td>-75.66</td>
<td>-72.53</td>
<td>-58.49</td>
<td>-50.60</td>
<td>-50.26</td>
<td>-44.88</td>
</tr>
<tr>
<td><strong>Noise Floor (High gain)</strong></td>
<td>-76.36</td>
<td>-75.86</td>
<td>-75.66</td>
<td>-65.03</td>
<td>-56.32</td>
<td>-50.17</td>
<td>-31.86</td>
<td>-31.71</td>
</tr>
</tbody>
</table>

Figure 3.25: Signal, noise and interferer level in the fully-differential UWB receiver.
### Table 3.9: Block specifications of the fully-differential UWB receiver.

<table>
<thead>
<tr>
<th>Specifications</th>
<th>Voltage Gain (dB)</th>
<th>Noise Figure (dB)</th>
<th>$IIP_3$ (dBm)</th>
<th>$IIP_2$ (dBm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>T/R switch</td>
<td>-1.0</td>
<td>1.0</td>
<td>20</td>
<td>200</td>
</tr>
<tr>
<td>Pre-select filter</td>
<td>-0.5</td>
<td>0.5</td>
<td>1000</td>
<td>200</td>
</tr>
<tr>
<td>LNA</td>
<td>15</td>
<td>3.5</td>
<td>-5</td>
<td>30</td>
</tr>
<tr>
<td>Mixer</td>
<td>11</td>
<td>12</td>
<td>5</td>
<td>35</td>
</tr>
<tr>
<td>Baseband LPF</td>
<td>0</td>
<td>25</td>
<td>15</td>
<td>90</td>
</tr>
<tr>
<td>Baseband VGA</td>
<td>36</td>
<td>40</td>
<td>20</td>
<td>90</td>
</tr>
<tr>
<td>A/D Converter</td>
<td>0</td>
<td>30</td>
<td>20</td>
<td>80</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>60.5</strong></td>
<td><strong>7.0</strong></td>
<td><strong>-9.7</strong></td>
<td><strong>13.2</strong></td>
</tr>
<tr>
<td><strong>Requirement</strong></td>
<td><strong>50</strong></td>
<td><strong>8.6</strong></td>
<td><strong>-11.2</strong></td>
<td><strong>12.4</strong></td>
</tr>
</tbody>
</table>
CHAPTER 4

DESIGN OF UWB RF FRONT-ENDS

In this chapter, we concentrate on circuit design of ultra-wideband RF front-end. At first, basic topologies of low noise amplifiers, mixers and baluns are briefly reviewed. Following the introductory parts, the design of balun-embedded front-end and fully-differential front-end are described respectively. Design trade-offs and simulated circuit performance are also given and discussed in details.

4.1 Common Low-Noise Amplifier Topologies

Low noise amplifiers (LNA) in wireless receivers is the first gain stage amplifying weak input RF signals from antenna. It is critical in LNA design to minimize signal power loss and introduce least amount of noise, as well as provide sufficient gain to

<table>
<thead>
<tr>
<th>Design Criteria</th>
<th>Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage Gain</td>
<td>$A_v$ (dB)</td>
</tr>
<tr>
<td>Noise Figure</td>
<td>$NF$ (dB)</td>
</tr>
<tr>
<td>Third-order Intercept Point</td>
<td>$IIP_3$ (dBm)</td>
</tr>
<tr>
<td>Second-order Intercept Point</td>
<td>$IIP_2$ (dBm)</td>
</tr>
</tbody>
</table>

Table 4.1: General LNA design specifications.
suppress noise from later stages. A few most important LNA design specifications are listed in Table 4.1. Return loss \( S_{11} \) reflects the power transferring capability between antenna and LNA. The lower the return loss is, the more power is delivered to LNA. Ideally, the input impedance of LNA \( Z_{\text{in,LNA}} \) needs to be complex-conjugate matched to the output impedance of antenna or RF pre-select filter \( R_s \), to ensure no power loss due to inter-stage impedance mismatch. Because \( R_s \) is always designed to be a standardized 50 Ω, \( Z_{\text{in,LNA}} \) has to be as close to this value as possible.

Two CMOS single transistor amplifier topologies, namely, common-source (CS) and common-gate (CG) topologies, are commonly used in LNA design. Shown in Figure 4.1(a), the classical inductively source-degenerated common-source LNA [22,38] is extensively used in narrow-band wireless communications because of its superior

![Figure 4.1: Two most commonly used LNA topologies.](image)
noise performance, high achievable voltage gain and well developed and standardized
design procedures. Illustrated in Figure 4.1(b), the common-gate LNA also finds exten-
tensive applications due to its wideband capabilities and insensitivity to parasitics.
In this section, both topologies will be briefly discussed. In order to make fair com-
parisons between the two, we will concentrate on input matching characteristics, gain
and noise figure.

4.1.1 Common-Source LNA

In Figure 4.1(a), first ignore the parasitic capacitance between gate and drain
$C_{GD}$, we end up with the input matching section of the amplifier that is redrawn
in Figure 4.2(a). The small-signal equivalent circuit can be simplified as in Figure
4.2(b). It is straightforward to show that $Z_{in}$ equals to

$$Z_{in} = s (L_G + L_S) + \frac{1}{sC_{GS}} + \omega_T \cdot L_S$$

(4.1)
where \( \omega_T = \frac{g_m}{C_{GS}} \) is generally defined as the unity gain bandwidth (GBW) of a given device. In order to match \( Z_{in} \) with \( R_s \), equation (4.1) reduces to

\[
 j\omega_0 (L_G + L_S) + \frac{1}{j\omega_0 C_{GS}} = 0
\]

(4.2)

\[
 R_s = \omega_T \cdot L_S
\]

(4.3)

where \( \omega_0 = \frac{1}{\sqrt{(L_G + L_S)C_{GS}}} \) is seen as the resonance frequency of input matching network, or the operating frequency of CS-LNA. It is instructive to study the relationship concealed in (4.2) and (4.3). First, the 50 \( \Omega \) impedance is indeed synthesized by noiseless components \( L_S \). It is understandable that this topology provides better noise figure than other topologies using resistive matching discussed in [22]. Second, this topology is more suitable for narrow-band systems, because \( L_G, L_S \) and \( C_{GS} \) essentially consist of a band-limiting network that confines optimum power matching within a limited frequency range.

To calculate the gain of CS-LNA, the effective transconductance \( G_m \) is determined first. Intuitively, the equivalent circuit in Figure 4.2(b) is a simple series-\( RLC \) network with quality factor \( Q = \frac{1}{\omega_0 C_{GS}(\omega_T L_S + R_s)} \). Recall that the voltage across capacitor \( C_{GS} \) equals to \( Q \) times of input voltage applied across the entire circuit [8, 22], or mathematically, \( V_{GS} = Q \cdot V_s \). Thus the effective amplifier transconductance \( G_m \) is governed by

\[
 G_m = Q \cdot g_m = \frac{g_m}{\omega_0 C_{GS}(\omega_T L_S + R_s)}.
\]

(4.4)

If the LNA is input-matched \( (\omega_T L_S = R_s) \), (4.4) reduces to

\[
 G_m = \frac{1}{2R_s} \cdot \frac{\omega_T}{\omega_0}
\]

(4.5)

Then the gain of CS-LNA is simply

\[
 A_v = \frac{Z_L}{2R_s} \cdot \frac{\omega_T}{\omega_0}
\]

(4.6)
It is interesting to look at (4.6) and notice LNA gain is actually independent on MOS transconductance $g_m$. When input matching condition and operating frequency are fixed, the gain of matched CS-LNA can only be boosted by tweaking the MOS device to push up its GBW $\omega_T$ or increasing the load $Z_L$.

The derivation of noise figure of CS-LNA is more complicated and time-consuming. Without proof we simply write down the absolute minimum noise figure can be achieved in common-source LNA with source degeneration is given as [22,39]

$$F_{\text{min}} \approx 1 + \frac{2}{\sqrt{5}} \cdot \frac{\omega_0}{\omega_T} \cdot \sqrt{\gamma \delta (1 - |c|^2)}. \quad (4.7)$$

where $\gamma$, $\delta$ and $c$ are device-related parameters. For long-channel devices, $\gamma = 2/3$, $\delta \approx 2 \cdot \gamma$ and $|c| \approx 0.395$.

If the LNA power dissipation is bounded, the power-constrained minimum noise figure is evaluated as

$$F_{\text{min},P} \approx 1 + 2.4 \cdot \frac{\gamma}{\alpha} \cdot \frac{\omega_0}{\omega_T}. \quad (4.8)$$

where $\alpha$ is also a device-related parameter and approximately equals to one. More thorough analysis on LNA noise optimization can be found in reference [39], which proposes an auxiliary capacitor used in parallel with $C_{GS}$ to achieve simultaneous noise optimization and input power matching.

In summary, the most attractive advantages of common-source LNA are its excellent noise performance and relatively large forward power/voltage gain. On the other hand, basic CS-LNA suffers from the Miller effect incurred by $C_{GD}$. The presence of $C_{GD}$ degrades signal isolation between input and output ports. Adding a cascode device would mitigate the impact of $C_{GD}$, but the device generates additional noise. In addition, the noise figure of CS-LNA is extremely sensitive to the quality factor.
of \( L_G \), because the thermal noise from the inductor directly adds to input signals. Finally, the basic CS-LNA discussed above fits well in narrow-band wireless communications. To extend its wideband capabilities, CS-LNA needs to combine with other circuit techniques.

### 4.1.2 Common-Gate LNA

A generic common-gate LNA is shown in Figure 4.1(b). An ideal current source \( I_S \) is placed at the source node of MOSFET \( M_1 \) to prevent AC signal from leaking to ground. In practice, \( I_S \) is occasionally replaced by a large value inductor working as an RF choke to save voltage headroom. DC biasing voltage \( V_b \) provided by auxiliary biasing circuit adjusts the operating point of the active device.

The most significant properties of CG-LNA are its wideband input matching, virtually flat noise figure across large bandwidth, robustness to parasitics, born isolation between input and output, but inferior noise performance, low voltage gain and even worse power gain. Because there is no direct capacitive path between source and drain, the input of CG-LNA is naturally shielded from the reverse signal feedthrough from output [40,41]. It is also noticeable that the current gain of common-gate stage is no larger than one, in contrast to the current gain of \( A_I \approx g_m C_{GS} \) in common-source stages.

To appreciate other properties of CG-LNA, we start from the consideration of input matching. The complex-conjugate matching is satisfied by tuning the transconductance of \( M_1 \) to align to \( R_s \). That is

\[
g_m = \frac{1}{R_s} \tag{4.9}
\]
To calculate the effective transconductance of the given amplifier in Figure 4.1(b), refer to the small-signal equivalent in Figure 4.3.

\[
\begin{align*}
I_{\text{out}} &= -g_m V_{GS} = g_m V_X \\
V_X &= V_s + g_m V_X R_s
\end{align*}
\]

Solving these equations leads to

\[
G_m = \frac{I_{\text{out}}}{V_s} = \frac{g_m}{1 + g_m R_s} = \frac{1}{2 R_s}
\]  
(4.10)

when CG-LNA is input-matched with the relationship in (4.9). Compared with the counterpart of CS-LNA in (4.5), the effective transconductance in CG-LNA is normally lower than CS-LNA. Thus the voltage gain of CG-LNA is calculated as

\[
A_v = \frac{Z_L}{2 R_s}.
\]  
(4.11)

The noise figure of CG-LNA can also be found by using its small-signal equivalent circuit and calculating the noise contributions at LNA output from input \((R_s)\) and from MOS channel noise and gate-induced noise. It is can be shown that under input-matching condition, the CG-LNA noise factor is

\[
F \approx 1 + \frac{\gamma}{\alpha} + \frac{\alpha \delta}{5} \cdot \left(\frac{\omega_0}{\omega_T}\right)^2.
\]  
(4.12)

83
Table 4.2: Important CS-LNA Design Formulas.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Important Formulas</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Impedance</td>
<td>( Z_{in} = s (L_G + L_S) + \frac{1}{sC_{gs}} + \omega_T \cdot L_S )</td>
</tr>
<tr>
<td>Minimum NF</td>
<td>( F_{\text{min}} \approx 1 + \frac{\frac{\gamma}{\alpha} \cdot \frac{\omega_T}{\omega_0} \cdot \sqrt{\gamma \delta (1 -</td>
</tr>
<tr>
<td>Voltage Gain</td>
<td>( A_V = \frac{Z_L}{2R_s} \cdot \frac{\omega_T}{\omega_0} )</td>
</tr>
</tbody>
</table>

Table 4.3: Important CG-LNA Design Formulas.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Important Formulas</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Impedance</td>
<td>( Z_{in} = \frac{1}{g_m} = R_s )</td>
</tr>
<tr>
<td>Minimum NF</td>
<td>( F_{\text{min}} \approx 1 + \frac{\gamma}{\alpha} \approx 2.2 \text{ dB} )</td>
</tr>
<tr>
<td>Voltage Gain</td>
<td>( A_V = \frac{Z_L}{2R_s} )</td>
</tr>
</tbody>
</table>

Interested reader can find the derivation of this expression in Appendix A. In most cases, gate-induced noise is negligible. Therefore, minimum achievable noise figure of common-gate LNA is bounded by [22,38]:

\[
F \geq 1 + \frac{\gamma}{\alpha} \approx 2.2 \text{ dB}
\]  

(4.13)

for long-channel MOS devices in which \( \alpha \approx 1 \) and \( \gamma = \frac{2}{3} \).

In summary, Table 4.2 and 4.3 list a few important design formulas for common-source and common-gate LNAs under the assumption of perfect input matching, respectively.
4.2 Double-balanced Current-commutating Mixers and Active Baluns

Downconversion mixer is an important RF component in wireless transceivers. Downconversion mixers are responsible of translating signal from RF to IF or analog baseband directly. Theoretically, any nonlinear or time-varying elements can serve as frequency translator [22]. Therefore, it is not surprising that many different frequency mixers have been used in state-of-the-art literatures. These mixers can be categorized as active/passive, current-commutating/potentiometric, single-balanced/double-balanced and etc. The common performance metrics of RF mixers are reported in Table 4.4.

4.2.1 Principles of Current-commutating Mixers

In this dissertation, we concentrate on the analysis and design of CMOS double-balanced current-commutating mixer, which is the MOS version of Gilbert cell mixer.
in bipolar technology. This kind of mixer offers combined advantages of high conversion gain, moderate noise performance, and reasonable linearity. Hereby it extensively presents in wireless receivers.

A conventional current-commutating CMOS Gilbert cell mixer is illustrated in Figure 4.4. Differential small RF input signals at $f_{RF}$ are applied to $M_{N1}$ and $M_{N2}$, the fully differential operation of $M_{N1}$ and $M_{N2}$ is guaranteed by adding tail current $I_S$. The two RF input devices act as transconductors to convert voltage into current domain. Matched pairs $M_{N3}$-$M_{N4}$ and $M_{N5}$-$M_{N6}$ work ideally as switches toggling at frequency $f_{LO}$ between $+1$ and $-1$ with 50% duty cycle, and translate RF signal to intermediate frequency $f_{IF}$. The operation principle of MOS Gilbert cell can be better understood by considering the simplified single-balanced mixer depicted in Figure 4.5.
The current flowing through input transconductor $M_{N1}$ equals to $I_{DC} + I_{in}$, where $I_{DC}$ and $I_{in}$ are DC biasing current and small-signal RF input current, respectively. Consider the case in which perfect square wave LO is applied to switching devices $M_{N2}$-$M_{N3}$ so that $M_{N2}$ and $M_{N3}$ are abruptly turned on and off. Applying Fourier expansion to square-wave LO voltage $V_{LO}(t)$, we have

$$V_{LO}(t) = \sum_{n=-\infty}^{\infty} (c_n e^{i\omega_{LO} nt})$$

(4.14)

where $c_{2n+1} = \frac{2}{(2n+1)\pi}$ and $c_{2n} = 0$. (4.15)

Write RF input $V_{RF} = A_{RF} e^{i\omega_{RF} t}$, it can be shown that mixer conversion gain is given as

$$A_v = \frac{V_{out}(f_{IF})}{V_{RF}(f_{RF})} = \frac{2\pi}{g_m R_L}$$

(4.16)
4.2.2 Noise in Current-commutating Mixers

Refer to the CMOS Gilbert cell mixer in Figure 4.4, there are three different noise sources in this mixer:

1. Noise from load resistor $R_L$;

2. Noise from RF transconductors ($M_{N1}$-$M_{N2}$);

3. Noise from switching pairs ($M_{N3}$-$M_{N4}$ and $M_{N5}$-$M_{N6}$);

In term of noise components in MOSFET, unlike in LNAs, flicker noise of mixers in direct-conversion receivers also plays an important role in defining mixer performance. Attention needs to be paid to both thermal noise and flicker noise [42–45].

Flicker noise in MOSFET is modeled empirically [46] as a voltage generator at the gate with power spectral density of

$$\frac{V_{n,1/f}^2}{f} = \frac{K_f}{C_{ox}WL} \cdot \frac{1}{f} \Delta f$$  \hspace{1cm} (4.17)

where $K_f$ is a process dependent flicker noise coefficient, $W$, $L$, $C_{ox}$ are MOSFET gate width, length and gate oxide capacitance, respectively. In addition, flicker noise is experimentally proved to depend on DC biasing current flowing through MOS device. Although the exact relationship is the subject of cutting-edge work, it is widely accepted that

$$\frac{V_{n,1/f}^2}{f} \propto I^\alpha$$  \hspace{1cm} (4.18)

where $\alpha$ is a statistically fitting constant and $I$ is the DC biasing current.

**Thermal Noise** To analyze the contribution of each noise generators in mixers, the single-balanced mixer depicted in Figure 4.6 is used to simplify derivations [42, 44].
Figure 4.6: Noise sources in single-balanced mixer.

Assume the noise sources are independent random processes, noise contribution to the output from each individual generator can be calculated independently. Then superposition is used to sum up these components into the total noise at the output.

Thermal noise from load resistor $R_L$ directly adds into output. Hence the output noise from $R_L$

$$V_{out,RL}^2 = 2R_L^2 \cdot I_{n,RL}^2 = 8kTR_L.$$  \hspace{1cm} (4.19)

Thermal noise from transconductor $M_{N1}$ experiences spectrum folding by LO frequency and its odd harmonics \cite{42,44}, thus the output noise due to $M_{N1}$ is given by

$$V_{out,Gm}^2 = 4kTR_L^2 \gamma g_m.$$  \hspace{1cm} (4.20)

where $g_m$ stands for the value of RF transconductance.
The calculation of thermal noise from switching pairs is a little complicated, because two different mechanisms, namely, direct and indirect mechanisms, are involved to convert noise $V_{n,SW}^2$ into noise voltages at output $V_{out,SW}^2$. Without detailed maths, we directly write down the expression of $V_{out,SW}^2$ as

$$V_{out,SW}^2 = 4kT R_L^2 \gamma I \pi A$$

(4.21)

where $I$ is the DC biasing current flowing through switching devices, while $A$ represents the voltage swing of LO signal. It is interesting to notice the physical meaning behind the relationship between switching pair noise versus LO swing and DC biasing current. As the amplitude of a sinusoidal oscillation grows up, LO is more like a square wave signal, and switching devices act more like ideal switches. In this situation, the noise contribution from switching pair is significantly suppressed, which correlates to our intuition. Meanwhile, while the DC current drops, the noise tends to decrease as well. And this observation serves well to partially explain why passive mixers are superior to active mixers in terms of noise performance.

Summarize the above derivations, we have total thermal noise at single-balanced mixer output written as

$$V_{out,total}^2 = 8kT R_L \left(1 + \gamma \frac{R_L I}{\pi A} + \frac{g_m R_L}{2}\right).$$

(4.22)

In double-balanced Gilbert cell mixers, both switching devices and transconductors are doubled, therefore the noise at mixer output is simply

$$V_{out,total}^2 = 8kT R_L \left(1 + \gamma \frac{2R_L I}{\pi A} + \gamma g_m R_L\right).$$

(4.23)

**Flicker Noise** The analysis of flicker noise in mixer is simpler than thermal noise. At first, as mixer loads are realized by non-poly resistors, no flicker noise presents in
these loads. Secondly, the RF transconductors in first order do not generate flicker noise contribution at mixer output. This is because the low-frequency flicker noise is up-converted to around the $f_{LO}$, following the exact frequency translation mechanism of tail current noise in fully differential VCOs. In practice, flicker noise in RF transconductors could leak into mixer output through any imbalance and mismatch in switching devices. But this direct feed-through can be greatly reduced by careful matching practice and layout optimization.

So the most dominant flicker noise contribution is from switching devices $M_{N3}$-$M_{N6}$. Applying the same model in Figure 4.6, flicker noise from switching devices also goes through the direct and indirect paths as for thermal noise. In most applications, direct mechanism tends to dominate the flicker noise transferring. Thus the flicker noise at mixer output is

$$V_{out,1/f}^2 = \frac{2K_f}{WLC_{ox}} \cdot \left( \frac{2I}{\pi A} \right)^2 \cdot \frac{1}{f}$$ (4.24)

Thus far, we presented a brief overview of noise mechanisms in mixers. In conclusion, we have a few important observations:

- Thermal noise in mixer is dominated by transconductors. $g_m$ can be reduced to minimize mixer noise figure, but at the price of lower conversion gain. This reveals a fundamental trade-off between gain and noise.

- Switching pairs also contribute white noise. But by applying a rail-to-rail swing LO and choosing low quiescent current, white noise from switching pairs can be eliminated effectively.
Flicker noise in mixer is limited by switching pairs. Forcing hard-switching, intentionally using large-channel devices and decreasing DC current can suppress flicker noise. This is especially useful in low data bandwidth applications.

RF transconductor may contribute flicker noise through switching pair mismatch. Thus the way to reduce this leakage is to optimize matching between switching devices.

4.2.3 Linearity of Gilbert Cell Mixers

The third-order linearity of Gilbert cell MOS mixers is primarily determined by the intrinsic device linearity of RF transconductor. This is particularly true when switching pairs respond to quasi-square-wave LO and the harmonic distortion in transconductor is nonetheless dominant. Approaches to improve intrinsic MOSFET
Figure 4.8: Different mixer transconductor topologies.

linearity include adjusting device DC operating point and increasing gate overdrive voltage $V_{ov}$. Simulations are performed on a minimum length NMOS transistor with $\frac{W}{L} = \frac{20 \mu m}{0.18 \mu m}$ in a 0.18-µm CMOS technology. When $V_{DS}$ is fixed, the simulated device intrinsic $IIP_3$ is shown in Figure 4.7. It is apparent that as gate overdrive increases the inherent linearity of NMOS improves as well. Remember the simulated $IIP_3$ here is the maximum attainable for the device under test. In presence of peripheral circuit components, the resulted $IP_3$ will no doubt be degraded.

The second-order linearity of mixer is more interesting to study. One significant mechanism comes from the self-mixing, which is resulted from capacitive coupling
(finite isolation) between RF and LO ports. Besides self-mixing, both RF transconductor and switching pairs introduce even order nonlinearity.

Three different, widely used RF transconductance topologies, fully-differential, pseudo-differential, and LC-tailed, are shown in Figure 4.8. It is well known that fully differential circuits remove even-order distortions effectively [46]. For LC-tailed input transconductors, if the resonance frequency is tuned to be around $2f_{RF}$, then, the second-order nonlinearity can be greatly suppressed, since it acts much like a fully-differential stage at this frequency. Pseudo-differential topology offers worst second-order linearity among the three, because there is no apparent mechanism at any point to guarantee the differentiability of the circuit.

Mismatch and imbalance in switching pair fundamentally limit the maximum attainable second-order linearity. At device level, the mismatch includes threshold voltage $V_{TH}$, process-dependent constant $\mu C_{ox}$, and temperature, doping gradient induced device dimension difference. At signal level, the mismatch refers to LO duty cycle imbalance, and parasitic capacitance loading effects. The $IM_2$ generation mechanism is quite similar to that of flicker noise, because both of these effects can be modeled as slowly varying voltage generators at the gate of switching devices. Mathematical derivations are well-documented in other literatures [23,44,45,47,48], and are not repeated here.

In summary, the $IIP_2$ of mixer depends both on RF input transconductor and switching pairs. When fully-differential topology is used for $g_{m,RF}$, mismatch-induced second-order nonlinearity in switching pair is dominant. If other transconductor topology is used, $g_m$ stage together with current commutating switches dictates mixer second-order linearity performance.
4.2.4 Active Balun Topologies

In principle, balun translates single-ended input into differential output, or vice versa. Ideally, the two outputs demonstrate a 180° phase difference and virtually equal amplitude. In practice, however, parasitic effect and different levels of mismatch degenerate the phase and amplitude relationships between the two outputs. Both passive balun and active balun have been used on chip [49–54]. Although passive
baluns popularly made of microstrip lines have the potential of superior linearity, wideband capabilities and better phase/gain balance, active baluns are much more compact and cost-effective. Thus monolithic active baluns have found more common applications, while passive baluns are primarily used externally. Figure 4.9 shows three commonly used MOS active balun topologies [50]. Although all of the three find applications in modern IC technologies, none of them is a panacea.

Figure 4.9(a) shows a single MOS transistor used as a single-ended to differential converter. Exploiting the signal phase relationship between gate, drain and source, one can notice that voltage out of drain is anti-phase to AC signal applied to gate, while source signal is in-phase to the voltage applied to gate. In ideal case, $V_S$ is $180^\circ$ out of phase to $V_D$, which is the exactly desired property of balun. In practice, however, two pieces of non-ideality limit the applications of this type of balun. First, signal inherently experiences different gate-source gain $A_{v, GS}$ and gate-drain gain $A_{v, GD}$. The transistor needs to be sized and biased carefully to compensate the gain difference. Second, even the gain error is somehow corrected, parasitic capacitance of gate-source $C_{GS}$ and gate-source $C_{GS}$ do not equal to each other. This leads to misalignment between phase transfer function of gate-source and that of gate-drain, resulting in phase imbalance between two outputs. Even worse, the phase difference caused by this is frequency-dependent.

Figure 4.9(b) shows a CMOS differential pair-like balun topology [50,51], in which $M_1$ and $M_2$ are two identical MOS FETs. An AC input is applied at gate of $M_1$, a current source $I_B$ is connected to the common node $X$ of two transistors’ source, and the gate of $M_2$ is grounded. Ideally, AC $V_{out2}$ out of $M_1$ drain is anti-phase to the input $V_{in}$; meanwhile, if $I_B$ is ideal, $V_{out1}$ is in-phase to $V_{in}$, i.e., $|\phi_{out2} - \phi_{out1}| = 180^\circ$. 96
### Design Criteria

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating Frequency</td>
<td>$f_0$ (Hz)</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>$BW$ (Hz)</td>
</tr>
<tr>
<td>Conversion Gain</td>
<td>$A_v$ (dB)</td>
</tr>
<tr>
<td>Noise Figure</td>
<td>$NF$ (dB)</td>
</tr>
<tr>
<td>Gain Mismatch</td>
<td>$\Delta A$</td>
</tr>
<tr>
<td>Phase Error</td>
<td>$\Delta \phi$ (dB)</td>
</tr>
</tbody>
</table>

Table 4.5: Important balun specifications.

The advantage of this topology over the single-MOSFET balun is that it is easy to match signal gain transfer functions through $M_1$ and $M_2$. However, this type of balun suffers its own issues. In practical design, current source $I_B$ is realized by pre-biased MOS transistors (single or cascode), which has an accompanied finite impedance $Z_S$ in parallel with $I_B$. The finite impedance allows signal leakage from node $X$ to ground, generating phase and gain errors between two outputs. In addition, since two different FETs are involved, any mismatches between $M_1$ and $M_2$ will result in gain or phase errors.

In this work, we adopt the common-gate, common-source (CG-CS) balun topology depicted in Figure 4.9(c). The principle behind this design [52–54] is quite similar to the aforementioned two types. It actually can be treated as a variant of the type in Figure 4.9(a), but the outputs are taken from two individual transistors rather than one single transistor. In this topology, $M_1$ works as a common-gate stage, while $M_2$ operates in common-source configuration. The bright side of this balun is that it allows separate generation of anti-phase signals and hence offers more flexibility to
<table>
<thead>
<tr>
<th>Parameters</th>
<th>Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage Gain $A_v$</td>
<td>12 dB</td>
</tr>
<tr>
<td>Noise Figure $NF$</td>
<td>$&lt; 3.2 \text{ dB}$</td>
</tr>
<tr>
<td>$IIP_3$</td>
<td>$&gt; 0 \text{ dBm}$</td>
</tr>
<tr>
<td>$IIP_2$</td>
<td>$&gt; 20 \text{ dBm}$</td>
</tr>
</tbody>
</table>

Table 4.6: Common-gate LNA specifications in balun-embedded RFE.

optimize for accuracy across broader spectrum. The dark side, however, is that since the two arms are totally independent, this balun is more vulnerable to process spreads and common-mode disturbance. Anyhow, this CG-CS balun is used here because of another level of benefit. It will be shown later that this topology can be absorbed into the design of double-balanced mixers, which makes the UWB RFE more compact and simpler.

A few most important balun design specifications are listed in Table 4.5. Gain mismatch and phase error demand special attentions, because they basically determine the input signal balance to following stages. In addition, frequency dependency of these parameters is also of great importance in wideband applications.

### 4.3 Design of A Balun-embedded RF front-end

To verify the design strategies of implementing UWB systems discussed in last chapter, two different versions of UWB RF front-ends have been designed. This section focuses on the design of a single-ended input, fully-differential outputs, and active balun-embedded RFE. The simplified RFE architecture is illustrated in Figure 4.10.
The single-ended common-gate LNA is consisted of one active device $M_1$, DC biasing inductor $L_S$ and loading tank $L_L$ and $C_L$. $L_S$ effectively works as high impedance at intended RF frequencies and as short at DC, which allows the amplifier to work with low supply voltage. DC blocking capacitors $C_{B1}$ and $C_{B2}$ are inserted preceding and following LNA to enable separately biasing of LNA and mixer. $M_2$ and $M_3$ consist of a CG-CS active balun, which is absorbed into a Gilbert Cell mixer as the input transconductors to convert input signals from voltage domain to current domain. The primary purpose of adding $M_4$ and $M_5$ is to achieve better isolation between LO ports and RF port of the mixer. NMOS $M_6$-$M_9$ constitute the switching devices to mix RF down to baseband. Derived from receiver budget analysis in last chapter, the specifications of LNA, balun and mixer are listed in Table 4.6, 4.7 and 4.8, respectively.
### Parameters Specifications

<table>
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<tr>
<td>Voltage Gain $A_v$</td>
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</tr>
<tr>
<td>Noise Figure $NF$</td>
<td>$&lt; 3$ dB</td>
</tr>
<tr>
<td>$IIP_3$</td>
<td>$&gt; 2$ dBm</td>
</tr>
<tr>
<td>$IIP_2$</td>
<td>$&gt; 40$ dBm</td>
</tr>
</tbody>
</table>

Table 4.7: Balun specifications in balun-embedded RFE.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conversion Gain $A_v$</td>
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</tr>
<tr>
<td>Noise Figure $NF$</td>
<td>$&lt; 12$ dB</td>
</tr>
<tr>
<td>$IIP_3$</td>
<td>$&gt; 8$ dBm</td>
</tr>
<tr>
<td>$IIP_2$</td>
<td>$&gt; 35$ dBm</td>
</tr>
</tbody>
</table>

Table 4.8: Mixer specifications in balun-embedded REF.

### 4.3.1 Feedback-enhanced Common-gate LNA

The targeted LNA spectral characteristics is the one shown in Figure 3.22(c). Common-gate topology is adopted due to two major considerations. Firstly, the minimum achievable noise figure for CG-LNA possesses a relatively flat spectrum, while $NF_{\text{min}}$ of CS-LNA tends to grow up as operating frequency increases. Figure 4.11 demonstrates the trend of $NF_{\text{min}}$ versus $\omega_0/\omega_T$, where $f_0 = \omega_0/2\pi$ and $f_T = \omega_T/2\pi$ are LNA operating frequency and intrinsic unity gain bandwidth GBW of MOS device. To provide a reasonable transconductance, minimum size MOSFET is rarely used in LNA, hence $f_T$ often falls in the range of 10–20 GHz for the $0.18\mu m$ CMOS
Minimum achievable noise figure of common-gate and common-source LNAs.

![Minimum Achievable Noise Figure of CS and CG LNAs](image)

Figure 4.11: Minimum achievable noise figure of common-gate and common-source LNAs.

technology used in this work. When employed in UWB receiver to work around 10 GHz, $NF_{\text{min}}$ of CS-LNA is unacceptably high. As a conclusion, CG-LNA is more suitable to 3.1–10.6 GHz UWB applications. Secondly, the gain bandwidth of CG-LNA is exclusively determined by frequency property of loading $LC$-tank. Therefore, common-gate topology fits well in implementing complicated band-switchable architecture.

One design challenge of CG-LNA is to meet the noise figure and gain specifications. As discussed in previous section, we mentioned that the minimum noise figure in common-gate LNA is limited as 2.2 dB. The fundamental reason is the resistive input matching nature of this topology. The requirement of $Z_{\text{in}} = 50$ Ω largely determines
the device size and transconductance of the MOSFET, so the noise figure of CG-LNA is essentially tied up to matching requirement. If this tight relationship can be somehow broken [40, 55], it is possible to achieve lower noise figure than that in (4.13).

Figure 4.12 shows the schematic of a feedback-enhanced CG-LNA and its small-signal equivalent circuit to derive its input impedance. In Figure 4.12(a), a fractional output voltage ($\delta \cdot V_{out}$) is fed back to the gate of MOSFET $M_1$. To derive the input impedance $Z_{in}$ looking into the source of $M_1$, let us consider the circuit in Figure 4.12(b). A test voltage $V_X$ is applied to the source node $S$, if the current flowing into
S is denoted as $I_X$, then $Z_{in} = \frac{V_X}{I_X}$. Write small-signal KVL and KCL, we have

$$
\begin{align*}
V_G &= \delta \cdot V_{out} \\
V_{out} &= Z_L \cdot I_X \\
I_X &= -g_m \cdot V_{GS} = -g_m \cdot (\delta V_{out} - V_X)
\end{align*}
$$

Solve the above equations, we end up with input impedance

$$Z_{in} = \frac{1}{g_m} + \delta Z_L \quad (4.25)$$

Similarly, the closed-loop voltage gain is calculated as

$$A_V = \frac{Z_L}{R_s + \frac{1}{g_m} + \delta Z_L} \quad (4.26)$$

It is noticed that when LNA input impedance $Z_{in}$ matches source impedance $R_s$, equation 4.26 reduces to $A_V = \frac{Z_L}{2R_s}$, which is not different from conventional CG-LNA.

As the input impedance and voltage gain are established, let us take a look at the impact on LNA noise figure of feedback factor $\delta$. A noise transfer function method is used to derive noise figure. The procedures of applying this method is as follows:

1. Identify all noise sources in a circuit;
2. Calculate transfer function from each noise source to output separately;
3. Treat noise sources as independent to each and use superposition to determine total output noise;
4. Find out the power ratio of one noise source to the total output noise;
5. Use the resulted ratio to compute noise figure.
Figure 4.13: Derivation of Noise Figure in Feedback-enhanced CG-LNA.

In feedback-enhanced CG-LNAs, assume feedback loop does not noiseless, two noise sources present in the circuit: thermal noise in voltage source impedance $R_s$:

$$\overline{i^2_{Rs}} = 4kT/R_s$$  \hspace{1cm} (4.27)

and MOS device channel noise:

$$\overline{i^2_D} = 4kT\gamma g_{d0}, \text{ where } g_{d0} = g_m/\alpha.$$  \hspace{1cm} (4.28)

Refer to the small-signal circuits with noise sources in Figure 4.13. In Figure 4.13(a), only noise current $\sqrt{i^2_{Rs}}$ from $R_s$ is considered. Applying KVL and KCL results in following circuit equations:

$$\begin{cases} \sqrt{i^2_{Rs}} + g_mV_{GS} - \frac{V_x}{R_s} = 0 \\ V_{GS} = \delta V_{out} - V_x \\ V_{out} = -g_mV_{GS}Z_L \end{cases}$$
Solve the equations above, we can express the output noise voltage contributed from 
\( \bar{i}_{Rs}^2 \) as

\[
V_{\text{out},Rs} = \frac{g_m Z_L R_s \sqrt{\bar{i}_{Rs}^2}}{1 + g_m (R_s + \delta Z_L)}.
\] (4.29)

The noise contribution from MOS channel noise can be calculated by referring Figure 4.13(b). Circuit equations are written as:

\[
\begin{align*}
\sqrt{i_D^2} + g_m (\delta V_{\text{out}} - V_X) &= \frac{V_X}{R_s} \quad \text{(4.27)} \\
\frac{V_X}{R_s} &= - \frac{V_{\text{out}}}{Z_L}
\end{align*}
\]

Solve the equations above, we can express the output noise voltage contributed from 
\( \bar{i}_D^2 \) as

\[
V_{\text{out},D} = \frac{Z_L \sqrt{\bar{i}_D^2}}{1 + g_m (R_s + \delta Z_L)}.
\] (4.30)

Adding the noise in (4.29) and (4.30) in power together, we have total output noise power as

\[
V_{\text{out, total}}^2 = V_{\text{out, Rs}}^2 + V_{\text{out, D}}^2 = \left( \frac{Z_L}{1 + g_m (R_s + \delta Z_L)} \right)^2 \cdot \left( g_m R_s^2 \cdot \bar{i}_{Rs}^2 + \bar{i}_D^2 \right)
\] (4.31)

Therefore, noise factor of feedback-enhanced CG-LNA is defined as

\[
F = \frac{V_{\text{out, Rs}}^2 + V_{\text{out, D}}^2}{V_{\text{out, Rs}}^2} = 1 + \frac{\sqrt{\bar{i}_D^2}}{\sqrt{\bar{i}_{Rs}^2}}.
\] (4.32)

Substitute (4.27) and (4.28) into (4.32), we have

\[
F = 1 + \frac{4kT \gamma g_m / \alpha}{g_m^2 R_s^2 \cdot 4kT / R_s} = 1 + \frac{\gamma}{\alpha} \cdot \frac{1}{g_m R_s}.
\] (4.33)

If the LNA is designed to be input matched, from (4.25) we have \( Z_{\text{in}} = R_s = \frac{1}{g_m} + \delta Z_L \).

Thus transconductance of \( M_1 \) is determined as \( g_m = \frac{1}{R_s - \delta Z_L} \). LNA noise factor can be rewritten as

\[
F = 1 + \frac{\gamma}{\alpha} \cdot \left( 1 - \frac{\delta Z_L}{R_s} \right).
\] (4.34)
It is interesting to compare (4.34) with (4.13). Adding a feedback factor $\delta$ in fact decouples noise from input matching, and subsequently introduces another level of freedom in optimize LNA noise performance. The lower bound judged by (4.13) is no longer the absolute minimum in presence of the feedback. Theoretically, both $\delta$ and $Z_L$ can be adjusted to lower noise figure. Since LNA voltage gain is actually limited by the ratio of $Z_L R_s$, however, this leaves only $\delta$ as a realistic design variable.

The actual LNA implemented is shown in Figure 4.14, in which no biasing circuit is included for the purpose of clearness. A capacitive divider is used to implement feedback factor $\delta = \frac{C_1}{C_1+C_2}$. $C_1$ is chosen to be small to avoid loading the amplifying device. A 5-bit binary-weighted capacitor bank is employed together with $L_L$ for switching LNA between multiple UWB bands. The capacitor bank is digitally controlled by 5 MOS switches, and each switch is sized to comply with the binary
Figure 4.15: Simulated $S_{11}$, NF and voltage gain of a CG-LNA at Band 3.

Weight of the capacitor the switch controls. The actual width of these MOS switches is designed to balance between parasitic loading when turned off and channel resistance when turned on. Parasitic capacitance of the switch reduces frequency tuning range, while channel resistance degrades the quality factor of the composite LC-tank. The minimum-value capacitor $C_0$ is determined by the frequency separation between UWB bands. Since resonant frequency follows a nonlinear relationship with capacitance/inductance ($\omega = \frac{1}{\sqrt{LC}}$), 5-bit word (32 controlled combinations) is used to compensate the non-uniform distribution of gain center frequencies generated by switchable LC-tank.

The LNA is designed with 1.8 V power supply, and it dissipates 1.4 mA DC current. The simulated insertion loss, noise figure and voltage gain at two representative
Figure 4.16: Simulated $S_{11}$, NF and voltage gain of a CG-LNA at Band 8.

Figure 4.17: Simulated quality factor of inductive load $L_L$. 

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Figure 4.18: Simulated in-band $IIP_3$ at Band 3 for CG-LNA.

<table>
<thead>
<tr>
<th>Band Center Frequencies</th>
<th>4.5 GHz</th>
<th>7.1 GHz</th>
<th>10 GHz</th>
<th>Average</th>
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<tr>
<td>Voltage Gain $A_v$ (dB)</td>
<td>15.2</td>
<td>10.7</td>
<td>8.8</td>
<td>11.57</td>
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<tr>
<td>Noise Figure $NF$ (dB)</td>
<td>2.93</td>
<td>2.85</td>
<td>3.12</td>
<td>2.97</td>
</tr>
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<td>$S_{11}$ (dB)</td>
<td>$&lt;-9.8$</td>
<td>$&lt;-9.5$</td>
<td>$&lt;-9.2$</td>
<td>$&lt;-9.5$</td>
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<tr>
<td>In-Band $IIP_3$ (dBm)</td>
<td>7.92</td>
<td>7.21</td>
<td>7.02</td>
<td>7.38</td>
</tr>
</tbody>
</table>

Table 4.9: Performance of feedback-enhanced common-gate LNA.
bands, Band 3 (4.5 GHz) and Band 8 (7.1 GHz) of the designed CG-LNA are shown in Figure 4.15 and 4.16, respectively. The simulated quality factor of loading inductor $L_L$ is shown in Figure 4.17. And high-$Q$ $LC$-tank is critical to increase LNA gain and lower the noise contribution from the load. Since the LNA spectrum extends to multiple GHz, it is also crucial to choose an inductor with relatively flat peak $Q$ across 3.1–10.6 GHz UWB range. It is seen in Figure 4.17, the peak $Q$ is reached at 13.3 GHz, and $Q$ value is in excess of 7 for entire UWB spectrum. The simulated in-band $IIP_3$ at Band 3 is given in Figure 4.18. The designed LNA possesses a high $IIP_3 = 7.92$ dBm, thanks to the single-transistor topology of the design. This allows the MOSFET to be biased at higher gate overdrive voltage, and thus improves the linearity of active device. The LNA performance is summarized in Table 4.9. It is worth noting that ideally CG-LNA input impedance is independent to loading tank. In this design, however, input matching is actually affected by impedance change of $LC$ loading, since a voltage-voltage feedback is introduced. This is reflected in the curve of $S_{11}$ versus frequency shown in Figure 4.15 and 4.16. In Table 4.9, only the worst-case $S_{11}$ for each intended UWB band is provided.

### 4.3.2 A Balun-embedded Double-balanced Mixer

One important property of active baluns is that they all consume additional power as stand-alone components. In practice, the concept of current-reuse can be applied by combining active balun with the preceding stage LNA [14] or the following mixers. In this work, we adopt the latter to utilize the active balun as voltage-to-current converter of a Gilbert cell mixer. The complete balun-embedded mixer is illustrated in Figure 4.10.
**Linearity Improvement**  The CG arm, consisted of $C_{CG}$, $L_s$, MOSEFTs $M_{N2}$ and $M_{N4}$, along with the CS arm, composed of $C_{CS}$, transistors $M_{N1}$ and $M_{N3}$, constructs a pseudo-differential input stage for the mixer. As discussed in Section 4.2, imbalance in transconductor occupies a large portion of overall mixer even-order nonlinearity. Special attention needs to be paid to minimize the gain and phase errors of the active balun so as to meet the stringent $IIP_2$ specification.

Multiple passive circuit elements contribute to the optimization of the matching between the two arms. Large inductor $L_s$ serves as different roles for the circuit. At DC, it acts as short-circuit taking no voltage headroom so that the stack of transistors within 1.8 V power supply is possible. For RF signal, it works as open-circuit to prevent signal from leaking to ground. The inductance value can be picked up to tune out parasitic capacitance at the source of $M_{N1}$ so that a relatively wideband
gain and phase balance can be achieved. Meanwhile, DC blocking capacitors $C_{\text{CG}}$ and $C_{\text{CS}}$ can be selected to be differently as another level of freedom in matching CG and CS arms. Finally, cascode devices $M_{\text{N3}}$ and $M_{\text{N4}}$ can be involved in tuning the balun as well as provide isolation between RF input port and LO ports. The worst-case (low power supply, high temperature and slow device) gain and phase errors of the balun alone are shown in Figure 4.20. Simulations on balun alone show that from 3.1 to 10.6 GHz, the amplitude deviations vary from -1.73 dB to 0.19 dB, phase differences roughly fall in the range from $179.6^\circ$ to $180.3^\circ$, and total current consumption is 1.8 mA at 1.8 V supply.

**Mixer Gain Considerations**  There exist two levels of conversion gain roll-off associated with UWB mixer design. First, when the mixer tries to downconvert RF signals centered at different UWB bands, it suffers from gain drop at high frequencies due to parasitic capacitance. Second, to contain the large signal bandwidth $BW$ at
baseband, conversion gain of mixer needs to be flat across $0 \sim BW$ range. These issues are better explained with Figure 4.21.

Conversion gain drop at high RF frequency demonstrates the design trade-offs between gain, linearity and power supply. Recall the mixer conversion gain is known as $A_v \approx 2g_{m,RF}R_L/\pi$. To compensate the gain roll-off at the high-end of UWB spectrum, at first $M_{N1}$ is sized to be with minimum transistor length. Secondly, the large $L_s$ can also neutralize the detrimental effect of capacitive parasitics. Finally, a digitally controllable resistor bank is used to make mixer load tunable. This way, the multiplication of $g_m$ and $R_L$ would be roughly constant throughout the UWB spectrum.

The mixer load is selected to be resistive instead of MOS transistor to remove flicker noise in active devices. The price is the voltage headroom taken by load resistor $R_L$. This is challenging in our design because $R_L$, $M_{N5}$, $M_{N3}$ and $M_{N1}$ are
stacked up one on top of another. The more troublesome fact is that to meet the total 9 dB conversion gain of balun-mixer combo towards the high end of UWB spectrum, $R_L$ has to be moderately large. This conflict is resolved by decreasing DC current and simultaneously employing class-AB operation in balun/transconductor.

Recall that in small-signal class-A mode operation, conductance of MOSFET $M_{N1}$ is determined by $g_m = \frac{2I_{DS}}{V_{GS} - V_{TH}}$. The purpose of reducing $I$ is to increase $R_L$, but the increment of $R_L$ is somehow offset by the loss in $g_m$ if class-A operation is assumed. It is possible to make $g_m$ intact by lowering $V_{GS} - V_{TH}$, but it comes with the penalty of reduced $IP_3$. Therefore, to circumvent this dilemma, RF input devices $M_{N1}$ and $M_{N2}$ are DC biased in class-AB regime [56–58]. It is known that class-AB operation allows larger input signal swing towards positive and negative directions, hence handles gain compression much more gracefully and efficiently.
Figure 4.23: Simulated $IIP_3$ of balun-embedded class-AB mixer.

Figure 4.24: Simulated $IIP_2$ of balun-embedded class-AB mixer.
Table 4.10: Simulated results for class-AB balun-embedded mixer.

<table>
<thead>
<tr>
<th>Frequencies</th>
<th>4 GHz</th>
<th>7 GHz</th>
<th>10 GHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conversion Gain $A_v$ (dB)</td>
<td>7.2~6.6</td>
<td>4.9~3.3</td>
<td>2.6~1.4</td>
</tr>
<tr>
<td>Noise Figure $NF$ (dB)</td>
<td>15.7~11.4</td>
<td>18.9~13.2</td>
<td>23.0~17.3</td>
</tr>
<tr>
<td>In-Band $IIP_3$ (dBm)</td>
<td>−2.2</td>
<td>−2.0</td>
<td>−1.7</td>
</tr>
<tr>
<td>In-Band $IIP_2$ (dBm)</td>
<td>34.6</td>
<td>32.3</td>
<td>31.1</td>
</tr>
</tbody>
</table>

The gain roll-off within UWB signal band is interleaved with the considerations of mixer flicker noise performance. The nonflat conversion gain conceptually shown in Figure 4.21 is largely caused by the parasitic capacitance at the IF output nodes. Reducing the dimensions of MOS switching devices $M_{N5} \sim M_{N8}$ could maintain more constant $A_v$. On the other hand, recall from Equation 4.24, large MOS switch size and low DC current could reduce mixer flicker noise. This is particularly important to ensure the flicker noise corner is lower than 4 MHz, so that noise only corrupts the subcarrier around DC, which is indeed not used for carrying data at all. Therefore, the switching devices need to carefully sized to balance between these two criteria.

Figures 4.22 and 4.23 shows the noise figure and conversion gain, $IIP_3$ of the designed balun-mixer combo for input RF signal at 4 GHz, respectively. Figure 4.24 shows the simulated $IIP_2$ at 7 GHz. At higher frequency, conversion gain and noise figure degrade, while linearity is slightly improved. Table 4.10 summarizes the simulated mixer metrics at 4, 7 and 10 GHz. The mixer draws 1.8 mA current from a 1.8 V power supply.

Although efforts have been devoted to maintain gain, noise figure flatness while not sacrificing absolute values of these parameters, simulated results still demonstrate
noticeable variations both across UWB spectrum and within downconverted signal band. In addition, linearity parameters of the mixer fall short to the specifications. This is primarily due to the added cascode devices that take voltage headroom from balun/transconductor thus limit the mixer $IP_3$. Further optimization and system simulations may be needed to balance between parameters and achieve better overall performance.

### 4.4 Design of A Fully Differential RF Front-end

A fully differential RF front-end is described and implemented in this section. The most important assumption is that an off-chip transmission line based wideband balun could convert single-ended RF signal from antenna to fully differential signal. Thus fully differential LNA and mixer can be used to suppress substrate-coupled digital noise and common-mode interferers from power supply lines. High even order linearity can be potentially achieved. The disadvantage of this topology is that the system even-order linearity would heavily depend on the balancing performance of the off-chip balun, which may vary from board to board.
Look at the LNA specifications in Table 4.11, it is observed that the voltage gain and linearity requirements on LNA are relatively moderate. As discussed in previous chapter, this RFE is intended to realize the LNA spectral characteristics depicted in Figure 3.22(b), which only rejects RF blockers below 3.1 GHz and WLAN interferers in 5-6 GHz. Concurrent LNA can be used to construct an RF filter with multiple passbands and a fixed notch [15, 59]. It is also possible to employ a complicated $LC$-filter as LNA’s input matching network, which is in principle similar to the ones in [12, 13]. Due to the complexity of these approaches, however, this work adopts a two-LNA architecture, in which a low-frequency LNA spans from 3.1 to 4.7 GHz while a high-frequency LNA covers 6.3–10.6 GHz frequency range. Because of time limitation, only the low-frequency LNA is designed.

The mixer specifications in Table 4.12 dictates the mixer to achieve both high conversion gain and moderate third-order linearity simultaneously. Unfortunately, it is difficult to meet both requirements with simple CMOS Gilbert cell mixer topology. Therefore, in this dissertation, a current-injection approach is used to boost conversion gain while not degrading $IP_3$ significantly. The principle, design and simulation results of the LNA and mixer are discussed in the following subsections.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conversion Gain $A_v$</td>
<td>11 dB</td>
</tr>
<tr>
<td>Noise Figure $NF$</td>
<td>$&lt; 12$ dB</td>
</tr>
<tr>
<td>$IIP_3$</td>
<td>$&gt; 5$ dBm</td>
</tr>
<tr>
<td>$IIP_2$</td>
<td>$&gt; 35$ dBm</td>
</tr>
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</table>

Table 4.12: Mixer specifications in fully-differential RFE.
4.4.1 A Resistive-feedback Common-source LNA

The principle of resistively shunt-feedback LNA can be explained by referring the simple shunt-series amplifier [22] shown in Figure 4.25. This topology uses resistive feedback $R_f$ to power-match source impedance $R_s$, and potentially offers a wideband real input impedance. The potential issue is the thermal noise contribution from $R_f$. The noise current $I_{2n} = 4kT/R_f$ is directly injected to input-referred node $X$. This noise current can be quite significant compared with other components in the circuit.

However, recall that in presence of Miller effect the impedance across the gate and drain of MOSFET $M_1$ is divided by the Miller effect factor [46]. That is to say actually the equivalent resistance looking from $X$, $R_{eq} = R_f/A$, while $A$ is the forward voltage gain from $X$ to $Y$. Since $R_{eq}$ is forced to be equal to $R_s$, $R_f$ can be very large if $A$ is designed to be large. This way, the noise contribution from $R_f$ could be greatly minimized. This idea leads to the LNA circuit shown in Figure 4.26.
The 3–5 GHz LNA is the simple combination of a classical inductively source-degenerated LNA and resistive shunt-feedback topology in Figure 4.25. Without \( R_f \) and \( C_f \), the LNA reduces to a fully-differential CS-LNA discussed in previous section. \( R_f \) serves as the shunt feedback, while \( C_f \) is simply a DC-decoupling capacitor to separate input and output DC biasing points.

Refer to the single-ended counterpart illustrated in Figure 4.27(a), the analysis of this LNA [60] is as follows. Recall the input matching circuit of conventional common-source LNA in Figure 4.2 without shunt-feedback can be regarded as a series \( RLC \) resonant network. Adding the shunt-feedback resistor \( R_f \) means to introduces a parallel resistance \( R_{f,eq} \) to the small-signal circuit, as shown in Figure 4.27(b). \( R_{f,eq} \) is from \( R_f \) with the modification from Miller effect. It can be expressed as \( R_{f,eq} = \frac{R_f}{1-A_v} \), where \( A_v \) is the LNA open-loop gain. Then the input impedance \( Z_{in} \) can be written
as

\[ Z_{\text{in}} = sL_G + \left( \frac{1}{sC_{GS}} + sL_S + \frac{g_m}{C_{GS}} \right) \parallel R_{f,\text{eq}}. \]  

(4.35)

Solving the right-hand side of equation (4.35) leads to a quite complicated close-form expression of \( Z_{\text{in}} \), which is of little practical value.

Intuitively, the purpose of feedback is to reduce the quality factor of series \( RLC \) network, and equivalently extend the fractional bandwidth of the LNA. In presence of Miller effect, the feedback resistor \( R_f \) can be relatively large, which contributes only a small amount of noise, and only slightly corrupts the LNA noise figure. Without derivation, the quality factor [60] of input matching network with shunt-feedback
resistor $R_f$ is

$$Q_f \approx \frac{1}{\omega_0 \cdot C_{GS} \cdot \left( R_s + \frac{g_m}{C_{GS}} L_S + \frac{\omega_0^2 L_S^2}{R_{fsq}} \right)}. \quad (4.36)$$

For the convenience of comparison, the original common-source LNA [22] has

$$Q = \frac{1}{\omega_0 \cdot C_{GS} \cdot \left( R_s + \frac{g_m}{C_{GS}} L_S \right)}. \quad (4.37)$$

The design procedure of common-source shunt-feedback LNA is rather straightforward.

- Step 1: optimize the design of inductively degenerated CS-LNA as usual;
- Step 2: slightly modify the LNA in Step 1 to reduce input impedance;
- Step 3: add shunt-feedback resistor $R_f$ and re-tune input impedance to match $R_s$;
- Step 4: characterize LNA spectrum and tweak $R_f$ to meet bandwidth, gain, and noise figure requirements.

The linearity of LNA is primarily determined by MOSFET $M_1$. Adjusting its DC biasing point through $V_{b1}$ to larger gate overdrive voltage would improve $IIP_3$ of the designed LNA.

Simulated results of the common-source LNA with shunt-feedback are shown in Figure 4.28 and 4.29. The LNA achieves voltage gain in excess of 23 dB, $-3$ dB bandwidth from 2.87 to 4.9 GHz, noise figure in the range of 2.1–2.82 dB, $S_{11} < -9.5$ dB within desired bandwidth, and in-band $IIP_3$ at $-2.79$ dBm. The LNA takes 8.2 mA current from a 1.8 V power supply. The performance of the LNA is summarized in Table 4.13.
Figure 4.28: Simulated CS-LNA gain, NF and $S_{11}$.

<table>
<thead>
<tr>
<th>PARAMETERS</th>
<th>Simulation Results</th>
<th>Specifications</th>
</tr>
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<td>15</td>
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<td>$-3$ dB bandwidth $BW$ (GHz)</td>
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<td>$3.1 \sim 4.7$</td>
</tr>
<tr>
<td>Noise Figure $NF$ (dB)</td>
<td>$2.1 \sim 2.82$</td>
<td>$&lt; 3.5$</td>
</tr>
<tr>
<td>$S_{11}$ (dB)</td>
<td>$&lt; -9.5$</td>
<td>$&lt; -10$</td>
</tr>
<tr>
<td>In-Band $II P_3$ (dBm)</td>
<td>$-2.79$</td>
<td>$&gt; -5$</td>
</tr>
</tbody>
</table>

Table 4.13: Performance of shunt-feedback CS-LNA.
All the passive components are implemented on-chip from foundry provided library. Metal-insulator-metal (MIM) capacitors are used owing to their low loss (quality factor in excess of 300) and low lateral parasitic capacitance. Polysilicon resistors are adopted because of the large resistance values needed in this design. Thanks to the large number of available inductors, high-Q inductor can be picked up so that low noise figure can be reached. $S_{11}$ of the LNA misses the specification by $-0.5 \text{ dB}$. This can be improved by tuning input matching network, but with a small amount of noise figure and gain. This optimization process is left as future improvement due to the time limitation of this work.

Figure 4.29: Simulated CS-LNA $IIP_3$. 
4.4.2 A current-injected double-balanced mixer

Mentioned in previous section, passive mixers can be highly linear, but fail to provide sufficient gain to suppress noise in preceding blocks. Therefore, in this design a Gilbert cell based double-balanced mixer is used. As revealed in Table 4.12, the most challenging requirement of active mixer is the simultaneous satisfaction of conversion gain \( A_v \approx 11 \text{ dB} \) and odd-order linearity requirements \( IIP_3 > 5 \text{ dBm} \). Previous states of the art show ordinary Gilbert mixer with high linearity \( IIP_3 > 10 \text{ dBm} \) and low conversion gain (0 dB or so) is achievable [43]. But the demands of gain and linearity at the same time are in fact conflicting.

Recall the mixer gain is proportional to input stage transconductance \( g_{m,RF} \), and for MOSFET \( g_m = \frac{2I_{DS}}{V_{GS}-V_{TH}} \). When current is fixed, to increase \( g_m \), gate overdrive voltage \( V_{OD} = V_{GS} - V_{TH} \) has to be decreased. Unfortunately, reducing \( V_{OD} \) would limit the linearity of the mixer. In order to resolve this stalemate, the current-reuse/current-injection approach [45,47,61,62] is borrowed in this design.

Current-reuse approach is modified from the current-injection mixer first introduced in [62]. It found extensive usage in cases when mixer gain boost is needed. The principle of current-injection in mixer is better explained with the assistance of Figure 4.30. The fundamental reasoning behind the current injection is to reduce the DC current flowing thru the load resistors. By injecting fixed current \( I_{inj} \) into current stage, we can keep current flowing into NMOS transconductors \( I_N \) large, while keeping \( I_{SW} \) small. The benefits are two-fold: \( R_L \) can be large with little influence on voltage headroom, and \( g_{m,RF} \) can be increased as well. Therefore, mixer conversion gain can be significantly improved [47]. The current relationship is expressed as \( I_N = I_{inj} + I_{SW} \). Current-injection method is successfully used in older technology.
Figure 4.30: Principle of current-injection in double-balanced mixer.

and higher supply voltage (for example, 0.25-μm CMOS and 3 V supply in [47]), however, the approach adds noise from current source $I_{inj}$, and tends to hurt the linearity performance in low supply applications.

A better solution is to extend the concept of current-injection to current-reuse. The topology of a current-reused double-balanced mixer is illustrated in Figure 4.31. The single-transistor RF transconductor in conventional Gilbert cell is replaced by a push-pull inverter-like input stage composed of $M_{N1}$, $M_{N2}$ and $M_{P1}$, $M_{P2}$, while the switching pairs and resistive loads remain the same. Similar to the current relationship in current-injection mixers, we have $I_N = I_P + I_{SW}$. The advantage of using high $R_L$ to boost $A_v$ due to low $I_{SW}$ is not taken away. Besides, PMOS $M_{P1,2}$ also provides a certain amount of transconductance $g_{m,P}$ in addition to $g_{m,N}$ introduced by NMOS
Figure 4.31: Current-reused double-balanced mixer.

devices. Since signal also propagates through PMOS devices, noise figure is improved when compared with original current-injection topology.

In actual design, $I_N \approx 5 \text{ mA}$, and $I_P \approx 4 \text{ mA}$. This leads to significant increase of conversion gain. The simulated gain, noise figure and $IIP_3$ at 7 GHz are shown in Figure 4.32 and 4.33, respectively. Gain, noise figure, in-band $IIP_3$ and $IIP_2$ at 4, 7, 10 GHz are reported in Table 4.14.
<table>
<thead>
<tr>
<th>Frequencies</th>
<th>4 GHz</th>
<th>7 GHz</th>
<th>10 GHz</th>
<th>Specs</th>
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<td>18.9~14.3</td>
<td>12</td>
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<tr>
<td>In-Band $IIP_3$ (dBm)</td>
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<td>0.06</td>
<td>1.4</td>
<td>5</td>
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<tr>
<td>In-Band $IIP_2$ (dBm)</td>
<td>55.4</td>
<td>52.2</td>
<td>51.1</td>
<td>35</td>
</tr>
</tbody>
</table>

Table 4.14: Simulated results for current-resue double-balanced mixer.

![Double-balanced Mixer with Current Resue](image)

Figure 4.32: Simulated gain and NF of current-reused double-balanced mixer.
Figure 4.33: Simulated $IIP_3$ of Current-reused double-balanced mixer.
CHAPTER 5

SYNTHESIZER FREQUENCY PLANNING AND ARCHITECTURE

In this chapter, we focus on the frequency planning and architecture of UWB frequency synthesizer. Principle of SSB-mixer based synthesis scheme is first introduced. Then spur generation mechanisms in this type of architecture are discussed. Simulation results are provided to justify theoretical analysis. In the end, a new UWB frequency synthesis scheme and corresponded synthesizer architecture are proposed.

5.1 Introduction

MB-OFDM UWB proposal specifies a 9.5 ns TX/RX switching time, which rules out conventional single-PLL based frequency synthesis schemes. As a rough estimate, the PLL loop bandwidth is given as [17]:

\[ f_c = \frac{1}{\tau_{lock} \zeta(\phi_m)} \cdot \ln \left( \frac{f_{\text{step}}}{f_{\text{error}}} \right) \]

where \( \zeta(\phi_m) \) is the effective damping factor, \( f_{\text{error}} \) is the allowable frequency tolerance, \( f_{\text{error}} \) is frequency jump. For the case of 528 MHz jump, in order to settle to 1-kHz frequency tolerance in 9.5 ns, the PLL must have a loop bandwidth of > 260 MHz, which is usually not realistic in current technologies. Even if the loop bandwidth...
Figure 5.1: Principle of SSB-mixer based frequency generation architecture.

is achieved, it will introduce a prohibitively large amount of in-band phase noise and corrupt the received signals. In addition, OFDM is well known for Inter-Carrier Interference (ICI) problems, which often set the integrated phase noise requirement in many wireless standards such as 802.11a/g. In order to overcome this fundamental limitation of PLL, one may have to pursue other novel architectures out of the box.

5.2 SSB-mixer Based Frequency Synthesis

5.2.1 Principles

A widely used LO generation architecture based on single-sideband (SSB) mixing [6, 36, 63–65] is adopted in this work for the frequency synthesizer. Shown in Figure 5.1, the principle of frequency generation using SSB mixer is to employ a fixed-frequency PLL to synthesize $f_{PLL}$, and generate two frequencies $\frac{1}{M} \times f_{PLL}$ and $\frac{1}{N} \times f_{PLL}$ with frequency division, and SSB-mix them to provide desired LO frequency $f_{LO} = (\frac{1}{M} \pm \frac{1}{N}) \times f_{PLL}$. A few similar structures can be grouped together to generate a set of different $f_{LO}$. These frequency components will be fed into a multiplexer (MUX) and digital control logics could select an appropriate LO frequency for transceiver within one nano-second.
In regular mixers, frequency mixing \( \cos(\omega_{RF}t) \cdot \cos(\omega_{LO}t) \) generates both upper- and lower-sideband frequencies \( \frac{1}{2} \cdot [\cos(\omega_{RF} + \omega_{LO})t + \cos(\omega_{RF} - \omega_{LO})t] \). On the contrary, SSB-mixers, also known as image-reject mixers, can greatly suppress the unwanted sideband. The principle of typical SSB-mixing [66] is shown in Figure 5.2. The SSB-mixer structure includes two regular mixers, one 90° phase shifter and one summing stage. If the oscillator is able to provide quadrature signals, the phase shifter can be omitted. In addition, the input RF signals need to contain both in-phase (I) and quadrature (Q) components. Ideally, the phase of RF signal is perfectly aligned with that of oscillator signal. As a result, the output from summing stage will only contain \( \omega_{RF} - \omega_{LO} \) component and eliminate \( \omega_{RF} + \omega_{LO} \). In practice, however, undesired sideband (frequency spur) might not be completely cancelled out due to circuit mismatch and signal imbalance. The existence of spurious sideband brings up an important issue in UWB synthesizer design. This issue is deferred to later section for detailed explanation.
5.2.2 Sources of Frequency Spurs

In SSB-mixer based frequency synthesizers demonstrated in Figure 5.1 and 5.2, sources of frequency spur include PLL, frequency dividers, SSB-mixers and multiplexers. Reference or fractional spurs in charge-pump PLL primarily originate from mismatch between charge-pump pull-up and pull-down currents, and only affect spectrum close to carriers. Thus PLL spurs are of less significance for UWB systems. Multiplexers will also generate frequency spurs, especially in case that isolation between frequency input ports are insufficient. Unwanted frequency component can leak into output port through couplings. Compared to frequency spurs due to SSB-mixing and frequency division, however, spurs from multiplexers are much less dominant [11,18] and hereby skipped in this dissertation.

SSB-mixers The root cause of frequency spur from SSB-mixing is that phase error and gain imbalance between $I$ and $Q$ paths lead to incomplete rejection to unwanted sideband at image frequency. The underlying mechanism is very much like the $I/Q$ mismatch issue in heterodyne receivers. This can be better explained with assistance.
Sideband rejection ratio with phase error and gain imbalance in SSB-mixers.

of Figure 5.3. Without losing generality, the model modified from Figure 5.2 characterizes $I/Q$ gain imbalance as one single gain stage $(1 + \Delta A)$ in $I$-path, and uses $\phi_1$ and $\phi_2$ to represent phase deviations in quadrature RF input and quadrature LO signal, respectively. In presence of the aforementioned gain imbalance and phase error, sideband rejection ratio in SSB-mixers can be expressed as [2]

$$R = 10 \cdot \log_{10} \left[ \frac{1 + (1 + \Delta A)^2 + 2 \cdot (1 + \Delta A) \cdot \cos(\phi_1 - \phi_2)}{1 + (1 + \Delta A)^2 - 2 \cdot (1 + \Delta A) \cdot \cos(\phi_1 + \phi_2)} \right].$$  \hspace{1cm} (5.1)$$

Sideband rejection ratio versus phase error and gain imbalance is plotted in Figure 5.4. Total phase error in degree equals to $\phi_1 + \phi_2$, and gain imbalance $\Delta A$ is represented in terms of percentage of unity gain. That is to say, if $\Delta A = 0$, the gain stage in Figure 5.3 reduces to unity, and no gain imbalance exists between two paths.
Mismatch-induced frequency spur is a serious concern in SSB-mixer. From the plot, it is obvious that ideally when $\Delta A = 0$ and $\phi_1 + \phi_2 = 0$, sideband rejection is maximized to infinity. In presence of mismatch, however, sideband rejection ratio drops drastically. For example, if gain imbalance $\Delta A = 5\%$ or equivalently $\Delta A = 0.46$ dB and total phase error $|\phi_1 + \phi_2| = 5^\circ$, sideband rejection is degraded to 26.02 dB.

To appreciate the design challenge in UWB receivers, let us assume that a 35 dB pre-select filter is anticipated. In order to satisfy the spur requirements in Table 3.3, another 35 dB sideband rejection is needed from SSB-mixer. This translates to $|\phi_1 + \phi_2| < 1.5^\circ$ and $\Delta A < 0.17$ dB, which are very demanding specifications in GHz range.

**Frequency dividers** It is very interesting to look at the role frequency divider plays in SSB-mixer and divider based systems. Consider the divide-by-$N$ block in Figure 5.5, the center frequency, phase noise and frequency spur at offset $f_m$ of input signal are $f_{in}$, $L_{in}(f_m)$ and $S_{in}(f_m)$, respectively. For output signal, those quantities are represented by $f_{in}/N$, $L_{out}(f_m)$ and $S_{out}(f_m)$.
It is well known that frequency division could lower single sideband phase noise of input frequency source [31]. Output phase noise $L_{\text{out}}(f_m)$ can be written in terms of input phase noise $L_{\text{in}}(f_m)$ and division ratio $N$ as

$$L_{\text{out}}(f_m) = L_{\text{in}}(f_m) - 20 \cdot \log_{10} N$$

(5.2)

where $f_m$ is offset frequency from carriers. This is to say, if $f_{\text{out}} = f_{\text{in}}/4$, then the output phase noise at offset frequency $f_m$ is approximately 12 dB lower than input phase noise at same offset frequency.

A similar relationship applies to frequency spur in divider as well. Refer to Figure 5.6, when a single-tone frequency carrier at $f_{\text{in}}$ and an accompanied spur at $f_{\text{in}} + f_m$ are passed through a divide-by-N block, the resulted carrier frequency of interest is located at $f_{\text{in}}/N$. Interestingly, originated from input spur, two sidebands are generated with equal spectral distance $f_m$ from carrier but reduced power level of $S(f_m)/N$. The important observation is that frequency division actually suppresses input spur level by $(20 \cdot \log_{10} N)$ dB.

$$S_{\text{out}}(\pm f_m) = S_{\text{in}}(f_m) - 20 \cdot \log_{10} N.$$  

(5.3)
This phenomenon can be explained by using linear superposition of amplitude modulation (AM) and phase modulation (PM) terms to express input frequency spur. While divider is insensitive to AM components, it does react to PM terms. The combined effect yields the relationship expressed in (5.3). Detailed derivation can be found in Reference [11,67].

5.3 Frequency Planning and Synthesizer Architecture

SSB-mixer based architecture is well known for the advantages of parallel frequency generation, straightforward synthesis scheme, and speedy frequency switching capabilities. On the other hand, the advantages come at the cost of frequency spurs and added noise contributions from post-PLL processing blocks [68]. Hence the major objectives of UWB frequency planning include:

- Maximize frequency coverage (ideally all 14 frequency bands);
- Minimize the appearance and suppress the power level of parasitic frequency components;
- Maintain compact synthesizer structure and low power consumption.

A natural strategy of planning UWB frequencies is to explore the intrinsic mathematical relations between bands and relations between band groups. A quick glance at Figure 2.6 shows that by offsetting the center frequency of band group 3 – 7128 MHz, up or down with 1584 or 3168 MHz respectively, all the band group center frequencies can be reached. Once all these frequencies are handy, simply shifting the band group centers up or down by 528 MHz or directly feeding band group center frequencies to synthesizer output is capable of generating all 14 UWB frequency
bands. So the only question left is how to conveniently make these aforementioned frequencies available.

It is interesting to notice that if \(2904 = 5.5 \times 528\) is absorbed into the equation, (2.3) can be rewritten as

\[
f_B(n_b) = 528 \times n_{\nu'} \text{ (MHz)}, \quad n_{\nu'} = 6.5 \ldots 19.5
\]

where \(n_{\nu'} = n_b + 5.5\). The center frequency of band 8, \(f_B(8) = 7128 = 13.5 \times 528 = 27 \times 264\) and it also can be written as \(f_B(8) = 7128 = \frac{9}{4} \times 3168 = \frac{9}{2} \times 1584\), which happens to include all the important frequencies needed in the discussion above. Based upon this observation, Table 5.1 summarizes the frequency generation schemes for all MB-OFDM UWB band frequencies using one synthesized frequency \(f_0 = 7128\) MHz, and three auxiliary frequencies \(\Delta f_2 = 3168, \Delta f_1 = 1584\) and \(\Delta f = 528\) MHz derived from \(f_0\). The bold numbers represent the centers of five different band groups that are also highlighted in Figure 5.7.

The synthesizer architecture is shown in Figure 5.8. A PLL is employed to generate a fixed frequency \(f_{\text{LO}} = 2 \times 7128 = 14256\) MHz, and a \(\div 2\) circuit is used to generate quadrature signals at \(f_{BG3} = 7128\) MHz. Passing \(f_{BG3}\) through a regenerative divider
<table>
<thead>
<tr>
<th>UWB band frequencies (MHz)</th>
<th>Frequency generation formula</th>
</tr>
</thead>
<tbody>
<tr>
<td>3432</td>
<td>( f_0 - \Delta f_2 - \Delta f )</td>
</tr>
<tr>
<td><strong>3960</strong></td>
<td>( f_0 - \Delta f_2 )</td>
</tr>
<tr>
<td>4488</td>
<td>( f_0 - \Delta f_2 + \Delta f )</td>
</tr>
<tr>
<td>5016</td>
<td>( f_0 - \Delta f_1 - \Delta f )</td>
</tr>
<tr>
<td><strong>5544</strong></td>
<td>( f_0 - \Delta f_1 )</td>
</tr>
<tr>
<td>6072</td>
<td>( f_0 - \Delta f_1 + \Delta f )</td>
</tr>
<tr>
<td>6600</td>
<td>( f_0 - \Delta f )</td>
</tr>
<tr>
<td><strong>7128</strong></td>
<td>( f_0 )</td>
</tr>
<tr>
<td>7656</td>
<td>( f_0 + \Delta f )</td>
</tr>
<tr>
<td>8184</td>
<td>( f_0 + \Delta f_1 - \Delta f )</td>
</tr>
<tr>
<td><strong>8712</strong></td>
<td>( f_0 + \Delta f_1 )</td>
</tr>
<tr>
<td>9240</td>
<td>( f_0 + \Delta f_1 + \Delta f )</td>
</tr>
<tr>
<td>9768</td>
<td>( f_0 + \Delta f_2 - \Delta f )</td>
</tr>
<tr>
<td><strong>10296</strong></td>
<td>( f_0 + \Delta f_2 )</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Frequency components</th>
<th>Values (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>( f_0 )</td>
<td>7128</td>
</tr>
<tr>
<td>( \Delta f )</td>
<td>528</td>
</tr>
<tr>
<td>( \Delta f_1 )</td>
<td>1584</td>
</tr>
<tr>
<td>( \Delta f_2 )</td>
<td>3168</td>
</tr>
</tbody>
</table>

Table 5.1: UWB frequency generation table.
Figure 5.8: Architecture of the proposed mixer-based frequency synthesizer.

[36] creates three output frequencies at $\Delta f = 528$, $\Delta f_1 = 1584$ and $\Delta f_2 = 3158$ MHz that are used in later frequency mixing operations. The selector controls which offset to be used to mix with $f_{BG3}$ using SSB mixer M1 and the second mixer M2 is used to mix the output of M1 with $\Delta f$.

The core of the synthesizer is the regenerative divider, as depicted in Figure 5.9. Originally from dynamic Miller frequency divider and injection-locked divider, the regeneration loop is capable of generating some very interesting and useful frequency components. The output $f_{out}$ of the cascade of three $\div 2$ blocks is fed back and mixed with input frequency $f_{in}$. It can be shown that for $N$ stages of $\div 2$ blocks, the frequency at the output of the $i^{th}$ stage is given by [36]

$$f_i = \frac{2^{N-i}}{2^N + 1} \times f_{in}. \quad (5.5)$$

For $N = 3$ and $f_{in} = 7128$ MHz, the output frequencies of the first and second stage can be calculated as $f_1 = \frac{4}{9} \times 7128 = 3128$ MHz and $f_2 = \frac{2}{9} \times 7128 = 1584$ MHz,
respectively. In addition, passing $f_2 = 1584$ MHz through a $\div 3$ block will end up with desired UWB bandwidth of 528 MHz.

5.3.1 Combining with Bluetooth

An additional advantage of proposed frequency plan is the potential expansion of providing frequency synthesis to 2.4 GHz Bluetooth communication mode.

The mixer-based synthesizer basically has two operation modes: one is UWB mode and the other is Bluetooth mode. In the synthesizer architecture shown in Figure 5.8, the PLL plays different roles in two operation modes. In UWB mode, the PLL serves as a fixed oscillator and provides a critical frequency component for later frequency manipulation. And in Bluetooth mode, the PLL simply works as a
fast-switching fractional-N synthesizer allowing frequency conversions of Bluetooth packets.

The operation in UWB mode has already been discussed in previous parts. In Bluetooth mode, the synthesizer, with all regenerative divider, mixers and multiplexers disabled, is virtually a conventional PLL. In order to share the PLL in both modes, the PLL is designed to be able to synthesize all frequencies between 7100 MHz and 7500 MHz with 1 MHz frequency step. While 7128 MHz used in UWB mode can be directly generated, all 79 Bluetooth channels from 2403 MHz to 2480 MHz can also be obtained by dividing frequencies with an increment of 3 MHz starting from 7209 MHz to 7440 MHz by 3.

Nevertheless, the presented dual-mode architecture is theoretically very promising, but it may suffer from quite a few potential difficulties. First of all, nonlinear operations, such as mixing and multiplexing, will inherently generate a large number of parasitic harmonics. If these harmonics are not suppressed well below a certain level, they will cause severe reciprocal mixing problems and corrupt the received signals. In addition, Bluetooth specifies stringent phase noise, channel frequency offset and settling requirements on PLL. Given the high VCO frequency at 7.3 GHz and large frequency division ratio (≈ 560 for 13 MHz reference frequency), the PLL architecture needs to be carefully selected and some novel calibration techniques need to be employed to meet these specifications. Finally, seemingly a simple arithmetic operator, divide-by-3 is actually another tough component to design especially when it is destined to operate at 7.3 GHz without incurring much phase noise.
CHAPTER 6

CONTRIBUTIONS AND FUTURE WORK

The major target of this work is to design a fully integrated receiver for MB-OFDM UWB system. Towards this objective, contributions of this dissertation can be summarized as follows. First, this work extends the wireless link analysis from 3-band Mode-1 operation to 14-band full UWB spectrum. As consequence, receiver sensitivity, system noise figure and implementation margin are determined based upon the new link analysis. Second, an analytical model is established to derive local oscillator phase noise for OFDM-based UWB systems. This is important to prevent local oscillator from degrading system BER performance. Third, the impacts of RF front-end architecture on local oscillator specifications have been observed. This observation leads to two different versions of front-end structure and circuit implementations. Finally, this dissertation proposed a novel SSB-mixer-based frequency synthesis scheme that is capable of generating all 14 MB-OFDM UWB bands with merely two steps of mixing. The proposed RF front-end and frequency synthesizer architecture show great potentials of being absorbed into a monolithic receiver that provides a highly integrated solution to MB-OFDM UWB system.

Because of the time limitation on this work, the goal of realizing a monolithic receiver is far from being reached. Quite a few optimization process and follow-up
works are left open on the field for future study. To name a few, this dissertation only covers the circuit design of UWB low noise amplifiers and downconversion mixers. To complete a full receiver, post-mixer baseband amplifier, channel-select filter, analog-to-digital converter, and entire frequency synthesizer need to be designed. In addition, the performance of designed UWB RF front-ends in this dissertation needs to be proved by silicon. Furthermore, although the proposed frequency synthesis scheme is very promising, behavioral simulations are required to predict its performance in terms of phase noise, frequency spurs and settling time. All these works are necessary to ensure final circuit implementations to satisfy system-level specifications derived in this thesis.

Nevertheless, this dissertation established a strategy and constructed a framework for the completion of a monolithic UWB receiver. The solid foundation laid down in this work will be very important for the ultimate successfulness in the future.
APPENDIX A

DERIVATION OF NOISE FACTOR IN COMMON-GATE LNA

In basic CG-LNAs, two noise sources present in the circuit, channel noise and gate-induced noise, in addition to thermal noise introduced by source impedance $R_s$:

$$\overline{i^2_{Rs}} = 4kT/R_s\Delta f, \quad (A.1)$$

MOS device channel noise:

$$\overline{i^2_D} = 4kT\gamma g_{d0}\Delta f, \quad \text{where } g_{d0} = g_m/\alpha, \quad (A.2)$$

and MOS gate-induced noise:

$$\overline{i^2_G} = 4kT\delta g_g\Delta f. \quad (A.3)$$

Refer to the small-signal circuits with noise sources in Figure A.1. In Figure A.1(a), only noise current $\overline{i^2_{Rs}}$ from $R_s$ is considered. Applying KVL and KCL results in following circuit equations:

\[
\begin{aligned}
\sqrt{\overline{i^2_{Rs}}} + g_mV_{GS} - \frac{V_X}{R_s} &= 0 \\
V_{GS} &= -V_X \\
V_{out} &= -g_mV_{GS}Z_L
\end{aligned}
\]
Figure A.1: Derivation of Noise Figure in Basic CG-LNA.
Solve the equations above, we can express the output noise voltage contributed from $i^2_{R_s}$ as

$$V_{\text{out},R_s} = \frac{g_m Z_L R_s \sqrt{i^2_{R_s}}}{1 + g_m R_s}.$$  \hspace{1cm} (A.4)

The noise contribution from MOS channel noise can be calculated by referring Figure A.1(b). Circuit equations are written as:

$$\begin{cases} \sqrt{i^2_D} + g_m (-V_X) = \frac{V_X}{R_s} \\ \frac{V_X}{R_s} = -\frac{V_{\text{out}}}{Z_L} \end{cases}$$

Solve the equations above, we can express the output noise voltage contributed from $i^2_D$ as

$$V_{\text{out},D} = \frac{Z_L \sqrt{i^2_D}}{1 + g_m R_s}.$$  \hspace{1cm} (A.5)

The noise contribution from MOS gate-induced noise can be calculated by referring Figure A.1(c). Circuit equations are written as:

$$\begin{cases} -g_m (\sqrt{i^2_G} \cdot sC_{GS} - V_X) \cdot Z_L = V_{\text{out},G} \\ \frac{V_X}{R_s} = g_m (\sqrt{i^2_G} \cdot sC_{GS} - V_X) \end{cases}$$

Solve the equations above, we can express the output noise voltage contributed from $i^2_G$ as

$$V_{\text{out},G} = \frac{g_m \cdot Z_L \sqrt{i^2_G} \cdot sC_{GS}}{1 + g_m R_s}.$$  \hspace{1cm} (A.6)

Therefore, noise factor of basic CG-LNA is defined as

$$F = \frac{V^2_{\text{out},R_s} + V^2_{\text{out},D} + V^2_{\text{out},G}}{V^2_{\text{out},R_s}} = 1 + \frac{i^2_D}{g_m R_s^2 \cdot i^2_{R_s}} + \frac{i^2_G}{g_m R_s^2 \cdot i^2_{R_s}}.$$  \hspace{1cm} (A.7)

Substitute (4.27) and (4.28) into (A.7), we have

$$F = 1 + \frac{4kT \gamma g_m}{g_m R_s^2 \cdot 4kT / R_s} = 1 + \frac{\gamma}{\alpha} \cdot \frac{1}{g_m R_s}.$$  \hspace{1cm} (A.8)
If the LNA is designed to be input matched, from (4.25) we have $Z_{\text{in}} = R_s = \frac{1}{g_m}$.

LNA noise factor can be rewritten as

$$F = 1 + \frac{\gamma}{\alpha} + \frac{\alpha \delta}{5} \cdot \left( \frac{\omega_0}{\omega_T} \right)^2.$$  \hspace{1cm} (A.9)
BIBLIOGRAPHY


