THE ROLE OF DEFECTS ON SCHOTTKY AND OHMIC CONTACT
CHARACTERISTICS FOR GAN AND
ALGAN/GAN HIGH-ELECTRON MOBILITY TRANSISTORS

DISSERTATION

Presented in Partial Fulfillment of the Requirements for the Degree Doctor of Philosophy
in the Graduate School of The Ohio State University

By
Dennis Eugene Walker, Jr., B.S., M.S.

**************************

The Ohio State University
2006

Dissertation Committee:

Dr. Leonard J. Brillson, Adviser
Dr. Steven A. Ringel
Dr. George J. Valco

Approved by

Adviser

Graduate Program in
Electrical and Computer Engineering
Copyright by
Dennis Eugene Walker, Jr.
2006
ABSTRACT

The AlGaN/GaN material system is ideally suited for both UV detectors and light sources as well as high performance, high power transistors. Devices built on AlGaN/GaN can be incorporated into either high power amplifier transmitters or low-noise receiver amplifier systems. Unfortunately, the III-N material system lacks an ideal lattice-matched substrate and high defect levels create current collapse and dispersion that adversely affects the high performance and stability the material system is capable of. Through a deeper understanding of the physics and device properties affected by these defects, engineered solutions will allow the realization and utilization of the full potential of AlGaN/GaN device properties. Auger Electron Spectroscopy (AES) and the associated secondary electron threshold (SET) techniques allow the characterization of the band bending and work function at the surface of semiconductors. Using these techniques in conjunction with ultra-high vacuum (UHV) sample cleaving and metal deposition, the underlying physical processes involved in Schottky barrier formation to non-polar GaN was investigated revealing cases of both ideal band-bending and Fermi level pinning. Cathodoluminescence spectroscopy (CL) allows the investigation of luminescent defect levels with depth-resolving capability by controlling the incident beam voltage and associated electron beam penetration into the sample. High electron mobility transistors (HEMTs) exhibiting current collapse were investigated using CL and CL mapping and specific defects were found in the GaN channel and buffer regions that
may help explain the current collapse phenomena. Coupling a novel gate mask into a typical HEMT fabrication sequence and utilizing three, independent UHV sample cleaning techniques including thermal desorption of contaminants, Ga-reflux, and N2 ion sputtering, and metallization of the gates on AlGaN/GaN HEMTs, correlations in defect levels, surface cleaning technique, and finished device performance were found. In analyzing the CL data for this sample, however, a specific feature located just below the GaN near-band edge was observed to accumulate near the Ohmic contacts prompting a further investigation of both the effects of the RIE etch used in producing the UHV-compatible mask as well as four different Ohmic contact structures on both defect levels determined by CL and on final device performance. Finally, a bulk GaN sample was processed with Ohmic contacts to determine the correlation of the AlGaN device layer in the formation of this defect level associated with the Ohmic contacts and the role of the mesa RIE etch, if any, on the same defect. Through these investigations, progress in the underlying physics of Schottky barrier formation on GaN and the important role of defects on device performance using AES, SET, and CL have been demonstrated.
Dedicated to my parents, Dennis and Fujie, 
and to my wife, Erika.
ACKNOWLEDGEMENTS

I would like to thank Dr. Leonard Brillson, my adviser, for his patience and encouragement over the years. He has supported and guided me throughout my studies at The Ohio State University and provided much needed and valuable guidance in my research.

I would like to thank my committee members, Dr. Ringel and Dr. Valco, as well as Dr. Bibyk, for the patience they have shown and for their help through the discussions I have had with each of them.

All of my fellow group members, past and present, have helped me in many ways and have made my experience in the lab unique, enjoyable, and memorable. In particular, I would like to thank Dr. Gregg Jessen, Dr. Shawn Bradley, Dr. Min Gao, and Brad White for everything they have done for me.

I would also like to acknowledge the AFRL Sensors Directorate at Wright Patterson Air Force Base. I have learned a lot about semiconductor device processing, especially from Bob Fitch, Jim Gillespie, Paul Cassity, and Joe Breedlove. Thank you for all your support, patience, and guidance in processing HEMT devices. In addition, I would like to thank Dr. Steve Binari and Dr. Jeff Mittereder at NRL for providing sample support and discussions on current collapse. I would also like to thank Daniel Ewing at Carnegie Mellon University for providing insight into thermionic emission in devices exhibiting dual-Schottky barriers.
Finally, I would like to thank God and my family for all their love and guidance. I want to thank my wonderful and caring parents who encouraged me to begin on this path to graduate school and my loving wife, Erika, whose patience and support helped me finish this long journey.
VITA

December 25, 1975 ................................................ Born – Havelock, North Carolina, USA

1999..............................................................................................B.S. Engineering Physics, Wright State University

2001...........................................................................................M.S. Electrical Engineering The Ohio State University

1999-2006 ...............................................................................Graduate Research Associate The Ohio State University

PUBLICATIONS


FIELDS OF STUDY

Major Field:   Electrical Engineering
               Physical Electronics
               Circuits

vii
# TABLE OF CONTENTS

<table>
<thead>
<tr>
<th>Chapter 1. INTRODUCTION AND BACKGROUND</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.1 ALGAN AND GAN</td>
<td>6</td>
</tr>
<tr>
<td>1.2 SCHOTTKY DIODE FUNDAMENTALS</td>
<td>8</td>
</tr>
<tr>
<td>1.3 ALGAN/GAN HEMTs</td>
<td>11</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Chapter 2. EQUIPMENT AND TECHNIQUES</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.1 EQUIPMENT OVERVIEW</td>
<td>16</td>
</tr>
<tr>
<td>2.1.1 Cleanroom</td>
<td>16</td>
</tr>
<tr>
<td>2.1.2 Ultra-High Vacuum (UHV) Systems</td>
<td>17</td>
</tr>
<tr>
<td>2.2 FABRICATION AND PROCESSING TECHNIQUES</td>
<td>18</td>
</tr>
<tr>
<td>2.2.1 Photoresist and Mask Alignment</td>
<td>19</td>
</tr>
<tr>
<td>2.2.2 Annealing</td>
<td>20</td>
</tr>
<tr>
<td>2.2.3 Metallization</td>
<td>21</td>
</tr>
<tr>
<td>2.2.4 Ion Sputtering</td>
<td>23</td>
</tr>
<tr>
<td>2.2.5 RIE Etching</td>
<td>24</td>
</tr>
<tr>
<td>2.2.6 Dual Layer Mask</td>
<td>25</td>
</tr>
<tr>
<td>2.2.7 Sample Cleaving</td>
<td>27</td>
</tr>
<tr>
<td>2.3 ANALYSIS TECHNIQUES</td>
<td>28</td>
</tr>
<tr>
<td>2.3.1 Auger Electron Spectroscopy (AES)</td>
<td>28</td>
</tr>
<tr>
<td>2.3.2 SET/Work Function Measurements</td>
<td>29</td>
</tr>
<tr>
<td>2.3.3 Electron Backscattering Pattern (EBSP)</td>
<td>30</td>
</tr>
<tr>
<td>2.3.4 Cathodoluminescence (CL)</td>
<td>31</td>
</tr>
<tr>
<td>2.3.5 DC Electrical Measurements</td>
<td>36</td>
</tr>
<tr>
<td>2.3.6 RF Electrical Measurements</td>
<td>42</td>
</tr>
<tr>
<td>2.4 SAMPLE UNIFORMITY</td>
<td>42</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Chapter 3. SCHOTTKY BARRIER FORMATION ON CLEAVED, NON-POLAR GAN</th>
<th>Page</th>
</tr>
</thead>
</table>

viii
3.1 INTRODUCTION ................................................................. 45
3.2 EXPERIMENTAL METHODS .................................................. 46
3.3 RESULTS ........................................................................... 50
3.4 DISCUSSION ..................................................................... 55
3.5 CONCLUSIONS ............................................................... 59

CHAPTER 4. DEFECTS AND CURRENT COLLAPSE IN ALGAN/GAN HEMT DEVICES .......................................................... 61
4.1 INTRODUCTION ................................................................. 61
4.2 EXPERIMENTAL ................................................................ 62
4.3 INITIAL RESULTS (COMPARING BOTH DEVICES INDIVIDUALLY) .................................................. 63
4.4 FURTHER RESULTS (COMPARING PRE- AND POST-STRESS DATA) .................................................. 65
4.5 CONCLUSIONS ............................................................... 70
4.6 DEVICE FABRICATION AND DEFECT ANALYSIS EXPERIMENTS .................................................. 71

CHAPTER 5. ALGAN/GAN/SIC HEMT DEVICE SURFACE TREATMENT OF SCHOTTKY CONTACT GATE REGIONS .................................................. 73
5.1 INTRODUCTION ................................................................. 73
5.2 EXPERIMENTAL ............................................................... 74
5.2.1 Double-layer Mask Details and Importance .................................................. 74
5.2.2 Sample C11B – Initial Results ...................................................... 79
5.2.3 Sample C11C – Effects of Various UHV Surface Treatments on Device Performance .................................................. 83
5.3 RESULTS AND CORRELATIONS ............................................. 106
5.3.1 Electrical Measurements and Response .................................................. 106
5.3.2 Low-temperature Ohmic metal investigation ........................................ 143
5.4 CONCLUSION ............................................................... 149

CHAPTER 6. ALGAN/GAN/SIC HEMT DEVICE OHMIC CONTACT INVESTIGATION AND EFFECT OF RIE ON DEVICE PERFORMANCE .............. 151
6.1 DEVICE FABRICATION ....................................................... 152
6.2 INITIAL CL ANALYSIS ........................................................ 154
6.3 ELECTRICAL RESPONSE FOR SAMPLE F01 ........................................ 166
6.4 DC AND RF ELECTRICAL RESULTS FOR SAMPLE F01 .................................................. 170
6.5 OHMIC INVESTIGATION OF SAMPLE F01 ........................................ 179

CHAPTER 7. OHMIC CONTACT INVESTIGATION AND EFFECT OF RIE ON BULK GAN .................................................. 185
7.1 POST-OHMIC ANNEAL ........................................................ 188
7.2 RESULTS OF ALGAN LAYER IMPORTANCE VS. GAN ONLY .................................................. 194

CHAPTER 8. CONCLUSIONS AND FUTURE WORK .................................................. 196

APPENDIX INTERCHANGEABLE EVAPORATOR DESIGN DIAGRAMS .......... 201
LIST OF REFERENCES ........................................................................ 209
LIST OF FIGURES

Figure 1 - Schottky diode band diagram (after [12]). ......................................................... 9

Figure 2 – (A) Basic HEMT structure with layer thicknesses not to scale and (B) sample HEMT band diagram. ............................................................................... 12

Figure 3 - Typical wafer fabrication process flowchart used to fabricate the HEMT devices. ..................................................................................................... 19

Figure 4 - EBSP pattern of GaN sample H01 used to determine crystal orientation. ....... 31

Figure 5 - Room temperature CL of sample C11 through the dual-layer mask. A 5 keV electron beam at 0.5 mA was used to examine the sample. ......................... 34

Figure 6 - Time-dependent electron beam effects on near band edge (NBE) and yellow luminescence (YL) with fitted curves shown in red. Upon turning off the e-beam during the 175 second period shown, the intensities remained at the same level.................................................................................... 35

Figure 7 – Forward-current diode curve variations in ideality factor, n, for different current transport mechanisms (After [52]). ...................................................... 39

Figure 8 - Analysis positions for MOCVD grown AlGaN samples. ................................. 43

Figure 9 - Low-temperature CL scans of bulk AlGaN at locations shown in Figure 8 demonstrating variability of the AlGaN NBE from one analysis point to another ......................................................................................................................... 44

Figure 10 - Representative Ga-LMM and N-KLL spectra used to determine Fermi level position relative to the band edges. Ga L_{3,4.5}M_{4.5} peak energies and the average of the two deconvolved N-KLL peak energies were used in Figure 12 and Figure 13 [69]. ................................................................. 48

Figure 11 - Representative work function determinations from secondary electron threshold with -10 V sample bias. All measurements are relative to the freshly cleaved surface offset to 0 eV. The SET threshold moves to higher energy as the Au overlayer becomes thicker. These threshold curves also
change shape as the surface becomes more metallic and uniform in potential [69].

Figure 12 - Representative N-KLL and Ga-L$_{3}$M$_{4,5}$M$_{4,5}$ intensity decreases with metal deposition (data points) and determination of electron scattering lengths [69].

Figure 13 - Ga-AES energy position relative to the initial position of "good" Cleave A. The average final energy positions for all curves is 1053.06±0.04 eV [69].

Figure 14 - N-AES energy position relative to the initial position of "good" Cleave A. The average energy position for the "rough" cleaves was 375.81±0.19 eV [69].

Figure 15 - SET work function shifts for each cleave. All curves are offset to the origin [69].

Figure 16 - Band diagram demonstrating band-bending measurements as determined by rigid core level shifts [69].

Figure 17 - Band diagram showing change in work function due to band bending, $qV_B$, vs. electron affinity, $\chi$ [69].

Figure 18 - Monte Carlo simulation of electron beam penetration in sample B10. The 2 keV electron beam samples the upper AlGaN layer while the 25 keV electron beam will penetrate into the SiC substrate.

Figure 19 - Low-temperature CL scans of sample B10 prior to electrical stressing. Each curve was taken at a magnification of 20,000x at a location exhibiting strong luminescence at the indicated wavelength.

Figure 20 - Low-temperature CL scans of B10 on a device after electrical stressing similar to Figure 19.

Figure 21 - Sample B10 low-temperature CL image maps at set energies pre- and post-electrical stress. The SEM image is at the same location as each of the image maps. The increased luminescence in the GaN NBE image post-stress is due to electron beam effects. Note that the Y4 and Y7 defects that appear in the pre-stress images also appear at the same locations post-stressing along with possible new defect locations as seen in the lower left portions of the Y4 and Y7 post-stress images.

Figure 22 - Sample B10 depth-dependent CL maps at the same location as in Figure 21 showing the Y4 and Y7 defect levels have the highest intensity at 10 kV excitation.
Figure 23 - SEM images of undercut for variations in dual-mask structure with F-14 etch times of (A) 5 minutes, (B) 8 minutes, and (C) 12 minutes..................... 76

Figure 24 - SEM images of undercut for final 23.5 minute F-14 etch. As seen, a final 800 nm of undercut was measured on structure A while 700 nm was measured on sample B, a 2 µm alignment bar that has been almost entirely undercut................................................................................................................. 77

Figure 25 - Dual-layer mask of the HEMT device structure with a cutaway view of the actual gate region for a 13.5 minute F-14 etch. ........................................ 78

Figure 26 - RF performance of AlGaN/GaN HEMT devices for sample C11B. Solid-colored die indicate devices resulting in RF performance. Other die indicate either unusable devices due to poor lift-off (green X’s) or no indication of RF performance (shaded die). ......................................................... 80

Figure 27 - IPE results for Ni/Au Schottky contacts on the device layer of sample C11B consisting of AlGaN with different processing. ......................................................... 82

Figure 28 – CASINO Monte Carlo predicted electron beam penetration into sample C11............................................................................................................ 83

Figure 29 – CASINO Monte Carlo simulated electron beam penetration and signal contribution in each layer of sample C11..................................................... 84

Figure 30 - Sample C11 wafer map diagram showing the right, center, and left orientations for each processed piece as determined during the sample processing and the process method used on each piece........................................ 86

Figure 31 - AES spectra from the center of sample C11-1 showing the elements detected on the surface prior to and after the UHV anneal. A slight reduction in C and O intensity post-anneal and an increase in N intensity suggest an improved surface post annealing......................................................... 87

Figure 32 - CL from center portion of Sample C11-1. The black curves indicate the sample condition prior to processing and the red curves post-annealing. Notice the increased blue luminescence (BL) at all sampling depths post-annealing......................................................... 88

Figure 33 - CL from the left portion of sample C11-1. The reduced GaN NBE near the surface and increased BL throughout the sample indicate damage in the sample with annealing. The reduced YL may, however, indicate a reduction of deep recombination centers......................................................... 89

Figure 34 - CL for sample C11-1 on the right portion of the sample pre- and post-annealing. The increased AlGaN NBE intensity reveals this portion of the sample was significantly improved by the anneal. ......................................................... 90
Figure 35 – 2 keV AES spectra of the center of Sample C11-2 showing the effects of the Ga-reflux cleaning and post-anneal on surface contaminants. Note the increased N AES signature and reduced C and O................................. 93

Figure 36 - Stainless-steel sample used in Ga-deposition testing to determine uniformity and appropriate sample positioning of the sample holder .......... 94

Figure 37 - CL analysis of center region of sample C11-2. The black curves show typical C11 signature pre-processing, red curves reveal damage post-Ga-reflux, and green curves show the sample condition post-anneal. Notice the band of new defect luminescence surrounding the GaN NBE at the surface layers both post-Ga deposition and annealing................................. 96

Figure 38 - AES from center region of C11-3 showing effects of N$_2$ ion sputtering on sample surface chemistry. The asterisk (*) indicates the N peak spreading with sputtering................................................................. 99

Figure 39 - AES spectra for the right portion of ion-sputter treated sample C11-3. Notice the decrease in C contamination, but persistence of O as well as the nearly identical level of N pre- and post-sputter and anneal. ......................... 100

Figure 40 - CL analysis of the center piece of sample C11-3. N$_2$ ion sputtering, shown in red, completely destroys the GaN bandedge and disrupts the YL in the upper layers of the sample to a depth of ~10 nm. Annealing, shown in green, returns the GaN bandedge, BL, and YL to nearly pre-treated sample conditions................................................................. 101

Figure 41 - CL spectra for the right portion of sample C11-3. N$_2$ ion sputter damage is localized to the upper ~5 nm of the sample surface (red curve) and is restored with annealing (green curve). ........................................ 104

Figure 42 - Contamination removal from sample C11 as determined by AES measurements of the center of each piece. The initial point of each scan has been normalized to 1 for comparison. (A) Carbon, (B) Nitrogen, (C) Oxygen. Overall, N$_2$ ion sputter cleaning was the most effective method to remove C and O while increasing N................................................. 105

Figure 43 - $f_T @ g_m$ peak in GHz for sample C11 showing all HEMT devices measured demonstrating the improved performance of the annealed sample and the poor performance of the N$_2$ sputter and Ga-reflux treated samples. The standard process sample performed consistently well........... 107

Figure 44 - $F_{Max} [\text{MAG}] @ g_m$ peak in GHz for sample C11 showing all HEMT devices measured. As in the $f_T$ measurements, the standard process had the highest yield and uniform response while the N$_2$ sputter and Ga reflux samples appear to have poor performance....................................................... 109
Figure 45 - Annealed portion of sample C11 demonstrating the results of transistor tests analyzed to determine the final contribution to the cut-off frequency average. Red blocks indicate good Igs-Vgs response, green blocks indicate good Ids-Vds FET family of curves with pinch-off, dark blue blocks indicate good transconductance performance, gm, and yellow blocks indicate good current gain |h21|^2 curves. The final devices passing three of the four tests are shown in the right in light blue.

Figure 46 - Sample C11 showing final resulting devices passing three of the four tests in color and the assumed approximate position of the sputter and Ga beam used during processing.

Figure 47 - Cut-off frequency values for sample C11 using only the devices determined as passing three of the four tests discussed previously. The processed samples consistently performed with higher fT than the standard process sample. In addition, the N2 ion sputter cleaned sample performs better at the outer edge as shown by the red arrow indicating possible damage due to sputtering too intensively in the inner portions of the sample destroying the AlGaN device layer and 2-DEG.

Figure 48 - Forward Vgs for Igs = 2mA/mm of sample C11. The RIE-exposed portions of the sample fabricated using the dual-layer mask exhibit lower Vgs at this current.

Figure 49 - Igs-Vgs Schottky diode curves for samples C11-1, C11-2, and C11-3. The Ga-reflux treated sample exhibits significantly higher reverse currents and a possible second Schottky barrier compared to devices processed with an anneal and N2 ion sputter.

Figure 50 - Comparison of Schottky gate response for sample C11 with processing. The Ga-reflux sample exhibits higher reverse currents and a second Schottky barrier as shown in Figure 49.

Figure 51 - Norde F(V) plots demonstrating parameter extraction for sample C11.

Figure 52 - Norde-extracted Schottky Barrier Heights (SBH) for sample C11.

Figure 53 - Norde-extracted Series Resistance, R_s, in Ohms for sample C11. The Ga-reflux and N2 sputtered samples exhibit abnormally high R_s corresponding to devices with poor performance.

Figure 54 - Diode I-V curve for device 0515 of the annealed sample C11-1 showing the linear region for parameter extraction.
Figure 55 - Schottky Barrier Height (SBH) determined using I-V curve data for sample C11. The general trends agree with the values obtained using the Norde analysis as shown in Figure 52. ............................................................... 122

Figure 56 - Ideality factors for Schottky diodes of sample C11 obtained using I-V curve analysis. Ideality factors near 1 indicating thermionic emission are preferred............................................................... 123

Figure 57 – Photo of Device 0615 from the Ga-reflux treated sample after DC-RF testing. The catastrophic failure destroyed the drain contact and may be due to excess current conduction through the device. ........................................ 124

Figure 58 - Norde analysis using Equation 6 showing a comparison between the annealed and Ga-reflux C11 samples. Note the two distinct minima in the Ga-reflux device as indicated.............................................................................. 125

Figure 59 - Schottky diode I-V curve from device 0615 with and without the calculated bias dependence.............................................................................................................. 126

Figure 60 - Series resistance modeling of device 0615 from sample C11................. 127

Figure 61 - I-V curve difference of experimental and theoretical data with lower barrier removed. The linear region and linear fit parameters are shown for the second Schottky barrier height............................................................... 128

Figure 62 - Double-barrier model plotted simultaneously with the actual data for diode 0615........................................................................................................... 128

Figure 63 - Theoretical I-V and actual data comparison with and without Norde-determined series resistance................................................................................ 129

Figure 64 - $I_{ds}$-$V_{ds}$ FET family of curves for Device 0515 of the annealed sample C11-1................................................................................................................ 133

Figure 65 - $I_{ds}$-$V_{ds}$ FET family of curves showing increased series resistance for device 0610 of the Ga-reflux treated sample C11-2. ................................................. 134

Figure 66 - $V_{th}$ map of sample C11. Threshold voltage values were higher in the $N_{2}$ ion sputtered sample in devices that did not exhibit high frequency response........................................................................................................... 135

Figure 67 - Comparison of $I_{ds}$-$V_{gs}$ data for HEMT devices across three processing methods on sample C11...................................................................................... 136

Figure 68 - Device 0715 transconductance, $g_{m}$, and drain-source current, $J_{d}$ for the Ga-reflux treated sample............................................................................. 137
Figure 69 - Maximum transconductance, $g_{m\text{-peak}}$, for sample C11. The majority of the devices subjected to the N$_2$ sputter treatment have an extremely low $g_{m\text{-peak}}$ corresponding to the non-functioning HEMTs. .............................................. 139

Figure 70 - FET family of curves with corresponding reverse gate leakage current for device 0512 from the annealed portion of sample C11-1. ......................... 140

Figure 71 - Gate leakage current at gate bias = -4 V for sample C11............................... 141

Figure 72 - Reverse gate current vs. drain-source voltage for typical devices on sample C11 ............................................................................................................. 142

Figure 73 - Low-temperature surface-sensitive CL of Ohmic and mesa regions both on and off the mesa normalized to the GaN NBE for comparison of the defect shoulder luminescence. A 600 V electron beam was used at 1x10$^{-9}$A. .............................................................................................................. 144

Figure 74 - CL maps of sample C11 showing (A) SEM of Ohmic alignment mark on AlGaN/GaN mesa, (B) 3.45 eV GaN NBE, and (C) 3.40 eV shoulder localized around the Ohmic metal. ............................................................................................................... 145

Figure 75 - CL maps off the AlGaN/GaN mesa on sample C11 showing (A) SEM of Ohmic alignment mark, (B) 3.45 eV GaN NBE, and (C) the lack of the 3.40 eV shoulder. ............................................................................................................. 146

Figure 76 - CL maps of the 3.40 eV defect luminescence with varying electron beam penetration voltages on sample C11.......................................................... 147

Figure 77 - Sample C11 with both Ohmic and gate metal on mesa AlGaN. The 3.40 eV shoulder defect luminescence only appears for the Ohmic metal with no defect luminescence from the gate metal edges................................. 148

Figure 78 – Sample F01 CASINO Monte Carlo simulation of electron penetration depth for varying electron beam energies.......................................................... 152

Figure 79 - Sample F01 map showing regions of processing for RIE and demonstrating the basic layout of the Ohmic contacts on the sample. The inset illustrates the concept of four subreticles with four Ohmic contact metal schemes contained within each die. .......................................................... 153

Figure 80 – Low-temperature CL analysis of sample F01 prior to processing at beam voltages of 500 eV, 1 keV, and 5 keV. ............................................................... 155

Figure 81 - GaN NBE CL intensity maps for sample F01 both pre-Ohmic and post-gate processing. The Ti/Al/Ni/Au Ohmic contacts have a higher intensity of GaN NBE most likely due to an increased low-energy shoulder resulting from Y2 defect luminescence for these contacts.................... 159
Figure 82 - GaN low-energy shoulder (Y2-defect) CL intensity maps for sample F01 both pre-Ohmic and post-gate processing. The Ti/Al/Ni/Au Ohmic contacts exhibit intense Y2 defect luminescence post-processing. Ir- and Pt-based Ohmic contacts also appear to exhibit a lower intensity of this same defect.......................................................................................................... 161

Figure 83 – Blue Luminescence (BL) CL intensity maps for sample F01 both pre-Ohmic and post-gate processing. The RIE damage increases the amount of BL exhibited by the sample in the top layers of the device as clearly demonstrated by the maps at 600 eV and 2 keV post-processing.......................... 163

Figure 84 - Yellow luminescence (YL) CL intensity maps for sample F01 both pre-Ohmic and post-gate processing. The Ohmic composition appears to result in increased intensity of the YL while RIE processing does not affect the formation of YL. ................................................................................. 165

Figure 85 - Contact resistance (Ohm-mm) for sample F01. Notice that Ohmic B, Ir, has an overall higher contact resistance than the other three metals............. 167

Figure 86 - Sheet resistance beneath the Ohmic contacts in Ohms/square for sample F01.......................................................................................................... 168

Figure 87 - Specific contact resistance for sample F01 in ohm-cm². Notice that Ohmic B, Ir, has a much higher specific contact resistance than the other three metal contacts................................................................. 169

Figure 88 - Vgs for Igs = 2mA/mm for sample F01. Notice the Ohmic A, Ni, exhibits higher values for this test due to the lower contact resistance for this metal................................................................. 171

Figure 89 - Igs-Vgs characteristics of the Schottky contacts for the four subreticles of die position [14,17] located in the non-RIE exposed region of sample F01................................................................. 172

Figure 90 - Igs-Vgs characteristics with respect to the RIE exposure for devices 14,18A and 14,19A of sample F01. The RIE-exposed curve, 14,19A, reaches the upper current limit before the final bias voltage is reached......... 173

Figure 91 – Peak transconductance, gm-peak, for sample F01. The RIE etch does not appear to affect the gm-peak performance, although the Ohmic contact composition and the related quality of Ohmic contact does have an effect. For example, the Ir Ohmic contact, Ohmic B, which was shown to exhibit poorer contact resistance also exhibits a consistently lower gm-peak than the other Ohmic contact subreticles................................................................. 174
Figure 92 - $V_{th}$ wafer map of sample F01 showing a definite increase in $V_{th}$ due to the RIE etch process applied to the upper portion compared to the non-RIE exposed region. ................................................................. 175

Figure 93 - FET family of curves for devices 14,18, non-RIE exposed, and 14,19, RIE exposed, demonstrating the difference in I-V characteristics caused by the RIE etch effect on $V_{th}$. Curves with square symbols represent I-V measurements from device 14,18A while triangle symbols represent device 14,19A. ................................................................. 176

Figure 94 - $f_t$ at $g_{m-peak}$ for sample F01. Overall, the performance on the RIE etched portion of the sample is poorer than on the non-RIE exposed portion. ................................................................. 177

Figure 95 - Summary of average $f_t$ values in GHz for sample F01 by RIE region and Ohmic metal type. ................................................................................................................. 178

Figure 96 - $F_{max}$ (MAG) at $g_{m-peak}$ for sample F01........................................................................ 179

Figure 97 – Low-temperature CL of F01 Ohmic alignment marks prior to Ohmic alloy annealing for all four Ohmic metals. The marked higher-intensity luminescence in the Ohmic A Y2 defect map may be an indication of Y2 defect formation prior to Ohmic contact anneal. A 1 keV, 1x10$^{-9}$ A electron beam was used with a magnification of 1,000x. ............................................ 181

Figure 98 - Sample F01 post-Ohmic anneal. CL maps reveal some amount of Y2 defect luminescence for all metals, although metal A, Ni, produces the highest concentration of this defect emission. Also note the Ohmic metal off mesa does not exhibit strong Y2 defect luminescence. A 2 keV, 5x10$^{-10}$ A electron beam was used with a magnification of 1,000x. ........................................... 183

Figure 99 - Low-temperature (12 K) CL scans of bulk GaN sample G01 on RIE etched and unetched surfaces with a 2 keV, 5x10$^{-10}$ A electron beam. ................. 186

Figure 100 – CASINO Monte Carlo simulation of GaN sample G01 illustrating the sampling depth with electron beam energy.................................................. 187

Figure 101 - Low-temperature CL analysis of sample G01 showing depth-dependence of the RIE damage with electron penetration depth. The damage extends to a total depth of between 100 and 1000 nm. ......................... 188

Figure 102 - Low-temperature CL analysis of sample G01 post-Ohmic anneal for an electron beam of 2 keV at 1x10$^{-9}$ A. .............................................................. 189

Figure 103 - CL maps of GaN sample G01 revealing RIE etch damage for a 2 keV electron beam at 5x10$^{-10}$ A and a magnification of 10,000x........................................ 190
Figure 104 - Post-Ohmic contact deposition CL maps of sample G01 with an electron beam of 2 keV, 1x10^-9 A at 3,000x. ................................................................. 191

Figure 105 - Sample G01 CL maps post Ohmic anneal showing no visible accumulation of Y2 defects at the Ohmic contact edge for either RIE etched or unetched surfaces. A 2 keV, 1x10^-9 A electron beam was used at a magnification of 3,000x. .................................................................................. 192

Figure 106 - Low-temperature CL of sample G01 post-anneal in the unetched region. The circles and labels indicate points of interest mapped in Figure 107....................................................................................................................... 193

Figure 107 – Low-temperature CL mapping of Sample G01 at a slow raster rate. A 7,500x magnification, 2 keV, 1x10^-9 A electron beam was used to collect the images. ........................................................................................................... 194
LIST OF TABLES

Table 1 - Basic semiconductor properties and Combined Figure of Merit (CFOM) illustrating the advantages of using GaN in high power, high temperature, and high frequency devices [3].............................................................................. 8

Table 2 - Sample identification and descriptions.............................................................. 15

Table 3 - Dual-mask RIE etch process detailing the overall time, power, and DC bias for each step................................................................................................... 76

Table 4 – Range, range straggle, and sputter yield for varying N ion beam energies as calculated using TRIM simulations for an incident ion beam at 45° to the sample surface, the approximate angle of incidence for the ion beam on sample C11........................................................................................... 102

Table 5 - Least square fitting results of diodes in row 6 using two methods: fitting to the series resistances and fitting to the material resistance and fractional part with calculated series resistances. The highlighted rs2 values indicate necessary refinements in the model are necessary to accurately extract the series resistance from the curve fits.................................................................... 130

Table 6 - Average values for the saturation currents, ideality factors, and Schottky barrier heights using the series resistance fit and material resistance/fractional part of the area curve fitting methods......................... 131

Table 7 - Sample F01 Ohmic metal structures and thicknesses...................................... 153

Table 8 - Energy regions of integration of CL line scans used to produce CL wafer maps.................................................................................................................. 157

Table 9 - Normalized statistical analysis of CL intensity data shown in Figure 81. It is clear that Ohmic metal A consistently exhibits higher GaN NBE compared to the other metals while the RIE etch does not affect the GaN NBE luminescence........................................................................................................... 159
Table 10 - Normalized statistical analysis of CL intensity data shown in Figure 82. Ohmic contact A, Ti/Al/Ni/Au, exhibits nearly twice the integrated intensity of Y2 luminescence compared to the other Ohmic contacts............. 161

Table 11 - Normalized statistical analysis of CL intensity data shown in Figure 83. The surface of all Ohmic contacts post-processing with RIE exhibit nearly 4x the integrated intensity of BL compared to the non-RIE post-processing Ohmic contacts. The BL is most intense in the 600 eV and 2 keV upper layers with nearly no change detected at 5 keV................................. 163

Table 12 - Normalized statistical analysis of CL intensity data shown in Figure 84. The YL intensity is nearly 3x higher at the surface region for all metals post-processing with only a slight correlation to the Ohmic metal used. Ni-based contacts appear to have an increased amount of YL followed by Pt, Ir, and Mo................................................................. 165
CHAPTER 1.

INTRODUCTION AND BACKGROUND

Demand for ever-increasing performance in the speed and reliability of technology by modern society requires constant advances in our understanding of both the underlying physics of semiconductor behavior and devices as well as advances in the properties of materials. To that end, GaN and AlGaN have allowed the development of both optoelectronics with output and detection capabilities extending into the ultraviolet regime as well as high-frequency, high-power transistors. In the advancing field of optoelectronics, UV capabilities afforded by GaN and other similar wide-band gap semiconductor systems have increased the available storage capacity of optical data systems and allowed the development of true white-light sources and full-color display systems. Transistor development utilizes the particular advantages of AlGaN/GaN including the high saturation velocity and breakdown characteristics of the material itself. High-electron mobility transistor (HEMT) development is most advanced in the AlGaN/GaN system and has led the way in high-power device and low-noise amplifier design for high-frequency transmitters and receivers.

Despite these advances, however, defects limit the performance of AlGaN/GaN-based transistors by adversely affecting the high-frequency characteristics and stability as seen in dispersion and current droop in recent studies. The solution to this dilemma is the
use of characterization techniques capable of detecting differences on a nanometer-scale and correlating these results with the performance differences due to fabrication techniques and surface conditions of the device layer. Various nanometer-scale techniques were utilized in this thesis to analyze such differences, including low-energy cathodoluminescence (CL) spectral analysis and image mapping, Auger electron spectroscopy (AES) for surface contamination studies and core-level shifts, and secondary electron threshold (SET) measurements capable of determining work-function all on a nm-scale. Using the information collected from these techniques, one can establish correlations between both the epitaxial growth and surface condition and the resulting device performance. These increase our understanding of the relationships between the physical semiconductor properties and the final engineered devices.

My thesis is concerned specifically with the use of advanced nm-scale surface-sensitive analysis techniques and the technology and state-of-the-art processing of HEMT structures. The thesis has been organized as follows. First, the techniques that were utilized, including CL, AES, and SET measurements, will be discussed and the capabilities and nuances of each will be explained to allow a thorough understanding of the results obtained. Next to be discussed will be the processing techniques used to make the devices as well as variations in these techniques to unique properties not typically encountered in normal device fabrication.

Following this necessary background information, I will present in Chapter 3 the results of a study determining the basic physical mechanisms behind Au and Ag Schottky barrier formation on cleaved, non-polar cross-sections of GaN epilayers as determined by AES and SET measurements. These samples exhibit two basic types of behavior:
unpinned, near-ideal classical behavior and pinned, non-ideal dipole formation at the surface. The quality of the cleaved surface layer determined the behavior of the associated sample with flat cleaves resulting in near-ideal behavior and poor cleaves, as determined from SEM images, resulting in pinned surfaces.

Understanding the behavior of Schottky barrier formation on GaN is essential to the fabrication of devices for this material system. In addition, typical AlGaN/GaN HEMT transistors have been plagued by current-droop in which stressing of the device electrically can result in reduced, long-term changes in the HEMT performance that is not well-understood. To further understand this detrimental behavior exhibited by some HEMT devices, Chapter 4 details the results of an examination into a sample known to exhibit this current collapse both pre- and post-stressing. Two specific defects termed Y4 and Y7 defect levels found within the device layers reveal a possible cause of this current-collapse. Monochromatic CL maps indicate concentrations of these defects believed to accumulate around dislocations that allow an alternative current path within the device.

As already indicated in studying Schottky formation on cleaved GaN, the quality of the surface layer can greatly affect the resulting Schottky contact with observed behavior ranging from near-ideal band-bending and Schottky formation to non-ideal pinned Fermi level behavior. However, in fabricating HEMT devices, ideal, cleaved surface layers are not possible and the actual surface quality is not typically controlled beyond a chemical oxide removal or oxygen plasma ash step prior to metallization.

Many detailed studies have been performed on GaN to determine the most appropriate method of surface cleaning. Some of the techniques attempted include
thermal desorption, Ga-reflux cleaning, ion sputtering, and various chemical cleanings, including NH$_3$ and various acid solutions. While a clean surface can result from all these situations, the suitability for actual device fabrication is unclear. I conducted an investigation into the effects of some of these surface cleaning techniques commonly employed in working with GaN and AlGaN using a special mask designed for an ultra-high vacuum (UHV) environment. Chapter 5 presents the results for AlGaN/GaN HEMTs fabricated from the same wafer where the surface conditions were varied prior to gate deposition. The correlation of the surface condition as determined by surface sensitive AES with electronic states measured by depth-dependent CL reveals the role of defects within the AlGaN and GaN band gaps on final device performance. These studies showed that, while N$_2$ ion sputtering was most effective at removing surface contaminants, annealing was most successful at creating devices with performance comparable to standard processing. Final cutoff frequency results following a careful examination of the electrical performance for each device revealed the HEMTs fabricated using the dual-layer mask process with cleaning performed with up to twice the cutoff frequency of the standard process devices. From such results, it is clear that surface states and defects play a role in final device performance.

In utilizing the special gate mask to investigate the role of defects on AlGaN/GaN HEMTs, a specific defect located at ~50 meV below the GaN near band edge was determined to originate from around the Ohmic contacts on the unetched, mesa regions of the sample. To investigate the role of this defect on Ohmic contact formation and to determine the effect of the RIE etch used in forming the dual-layer gate mask, I carried out an Ohmic contact and RIE damage study using AlGaN/GaN HEMT devices. Chapter
6 describes this work in detail. A mask set was used that allowed the creation of four different Ohmic contacts within each die. This enabled the correlation of these different Ohmic contact compositions between the CL spectral response as well as the final performance of the devices. In addition, half of the sample was subjected to an RIE etch used in forming the dual-layer mask. For contacts consisting of Ti/Al/metal/Au, it was found that the ~50 meV defect level accumulating around the Ohmic contacts formed most strongly in Ni-based Ohmic contacts. Some evidence of this defect also appeared in Ir- and Pt-based contacts. In addition, the RIE etch directly increased the intensity of a second defect at deeper trap energies (blue luminescence) and affected the threshold voltage of the gates.

Throughout the final two HEMT studies, a correlation of the defect level ~50 meV below the GaN near band edge was made to Ohmic contacts formed on AlGaN that was not subjected to mesa etching as observed via CL mapping techniques. In both these studies, however, it was unclear whether the defect luminescence was a result of the Ohmic contacts to AlGaN or whether this same defect level would form on GaN not subjected to RIE. Chapter 7 addresses the role of both the AlGaN layer and the RIE etch on this defect formation. Here, bulk, undoped GaN was processed with Ti/Al/Ni/Au Ohmic contacts in which half of the sample was subjected to a typical RIE mesa etch. The results show that the AlGaN layer was essential in forming this defect level and that the RIE etch caused changes within the band gap of the semiconductor as determined by CL to a depth of ~100-1000 nm.

Through these studies, a better understanding has been made of the important and detrimental effects of defects on final device performance. In addition, a novel use of
AES and SET measurement techniques helped advance our understanding of the initial formation of Schottky barriers on GaN. Overall, this work emphasizes the importance of localized defects near surfaces, interfaces, and specific regions of active device structures on a nanometer scale. It also underscores the value of nanometer-scale chemical and electronic techniques that can analyze defect properties on this same scale.

1.1 AlGaN and GaN

Modern electronics rely heavily on silicon-based technologies. In both the digital and analog device realms, silicon has become the dominant material for making integrated circuits. Due to silicon’s indirect and narrow bandgap, however, optoelectronic, high frequency, and high-power devices have all required the use of other compound semiconductor material systems including III-nitrides. Of these new semiconductor materials, gallium nitride (GaN) and its relatives, indium gallium nitride (InGaN) and aluminum gallium nitride (AlGaN), have risen to the task of providing a wide, direct band gap material system for semiconductor devices operating at the upper limits of current device technology.

GaN was one of the first materials successfully used to produce blue LEDs and laser diodes [1]. With the advent of this technology, the entire visible color spectrum was suddenly available for full-color display units and higher density optical data storage. Similar to III-V technology, band gap engineering with the incorporation of aluminum or indium in the crystal lattice allowed microwave transistor devices based on the two-
dimensional electron gas (2-DEG) known as high-electron mobility transistors, or HEMTs, to be developed with operating frequencies well into the GHz range [2-4].

GaN can be grown in different crystalline forms including cubic and wurtzite. In device fabrication, the wurtzite form is preferred. Substrates used to grow GaN include sapphire, silicon carbide (SiC), and more recently silicon [5]. Although advances have been made in the area of GaN growth, the crystal quality continues to remain markedly poorer and more difficult to grow than the crystal quality attainable for the more mature silicon industry resulting in smaller wafers with less usable device area. Reasons for this include the difficulty of finding a substrate for epitaxial growth with a lattice constant matching that of GaN [5, 6]. Ideally, GaN epitaxy would be performed on GaN substrates, but while advances continue to be made in this field, it remains difficult to grow bulk GaN substrates. In high power applications, SiC substrates are preferred due to the higher thermal conductivity as seen in Table 1 below [7].

The key properties important in high power, high frequency device applications are listed along with values for other common semiconductors in Table 1. As can be seen in the combined figure of merit (CFOM), the properties of GaN are superior to all the other semiconductors listed. With proper device fabrication, GaN-based semiconductor devices outperform most other material systems.
<table>
<thead>
<tr>
<th>Property</th>
<th>GaN</th>
<th>4H-SiC</th>
<th>GaAs</th>
<th>Si</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandgap $E_g$ (eV)</td>
<td>3.40</td>
<td>3.25</td>
<td>1.42</td>
<td>1.12</td>
</tr>
<tr>
<td>Breakdown field $E_B$ (MV/cm)</td>
<td>4.0</td>
<td>3.0</td>
<td>0.4</td>
<td>0.25</td>
</tr>
<tr>
<td>Electron mobility $\mu$ (cm$^2$/V s)</td>
<td>1300</td>
<td>800</td>
<td>6000</td>
<td>1350</td>
</tr>
<tr>
<td>Maximum velocity $v_g$ ($10^7$ cm/s)</td>
<td>3.0</td>
<td>2.0</td>
<td>2.0</td>
<td>1.0</td>
</tr>
<tr>
<td>Thermal conductivity $\chi$ (W/cm K)</td>
<td>1.3</td>
<td>4.9</td>
<td>0.5</td>
<td>1.5</td>
</tr>
<tr>
<td>Dielectric constant $\varepsilon$</td>
<td>9.0</td>
<td>9.7</td>
<td>12.8</td>
<td>11.8</td>
</tr>
<tr>
<td>CFOM = $\chi\mu v_g E_B^2 / (\chi\mu v_g E_B^2)_{Si}$</td>
<td>489</td>
<td>458</td>
<td>8</td>
<td>1</td>
</tr>
</tbody>
</table>

Table 1 - Basic semiconductor properties and Combined Figure of Merit (CFOM) illustrating the advantages of using GaN in high power, high temperature, and high frequency devices [3].

Another important aspect of GaN is its ionicity of bonding, calculated to be about 39% [8], which should lead to a Schottky barrier moderately dependent on the metal work function [9]. The importance of this will become evident later and depends on the amount of Fermi level pinning at the metal contact that has been observed to depend on the ionicity of the crystal [10].

1.2 Schottky Diode Fundamentals

Schottky diodes are based on the Schottky barrier theory developed simultaneously by Schottky and Mott in 1939. The basic premise of the device is shown in Figure 1A. When a semiconductor and metal are brought together, the Fermi levels align and the conduction band (for an n-type semiconductor) will bend upward as electrons are depleted from the semiconductor forming a potential barrier [11]. Under the influence of a forward bias as depicted by $V_F$ in Figure 1B, electrons can more easily flow from the semiconductor into the metal since the barrier to the electrons within the
semiconductor is decreased to \( q(V_r-V_f) \) while the barrier to the electrons within the metal remains nearly constant. During reverse bias, the electrons experience a larger barrier height from the semiconductor to the metal.

Figure 1 - Schottky diode band diagram (after [12]).

In the ideal Schottky contact, current transport occurs solely by thermionic emission over the Schottky barrier. Unfortunately, the majority of Schottky contacts exhibit non-idealities. Although the theory proposed by Schottky and Mott should result in Schottky barrier height dependence on metal work function, researchers realized that data taken in the laboratory for many material systems revealed the barrier height to remain nearly constant regardless of the metal used to make the contact. Based on these observations, theories of Fermi level pinning were developed that explained how interface states could trap charge and force the Fermi level to remain relatively constant,
or “pinned”, at the semiconductor-metal interface [13, 14]. While many mechanisms can be used to explain this behavior including the ionicity of the bonds, a common requirement is that states must be created within the forbidden region of the band gap. Such states were first studied by Tamm and were later identified as localized states [15]. The basic idea behind Fermi level pinning involves the charge neutrality layer located at $\Phi_o$ in Figure 1B and localized states at the interface that force the Fermi level to a certain position in the band gap [16].

At the surface of the semiconductor, many types of states can form including intrinsic surface states, interfacial relaxation induced states, metal induced gap states (MIGS), vacancy, anti-site, or defect related states, and exchange reaction doping [12]. The role of these localized states within the band gap is significant as previously mentioned and ultimately, many factors influence the final Schottky barrier height. The semiconductor surface itself is composed of intrinsic surface states since the atoms at the surface have dangling bonds that are highly reactive [17]. Atmosphere-exposed surfaces immediately develop a contamination layer that separates the metal layer from the semiconductor as indicated by $\delta$ in Figure 1B. Although this layer is typically thin and electrons can tunnel through the barrier, this contamination layer ultimately affects the quality of the Schottky barrier. The metal atoms can also diffuse into the semiconductor or semiconductor atoms can diffuse into the metal forming localized states even at room temperature [18].

While ideal Schottky contacts are preferred, it has been pointed out that when a cleaved surface is utilized as a Schottky contact, the entire system must be analyzed differently than for air-exposed semiconductor surfaces used as Schottky contacts. This
is because the interface layer indicated by $\delta$ in Figure 1B disappears and the metal is in intimate contact with the semiconductor [12]. Results obtained under such circumstances can be extremely useful in determining the role of interface and localized states on the resultant Fermi level and Schottky barrier height without the influence of the states [17]. The Schottky barrier behavior is determined during the critical initial stages of barrier formation and these phenomena on GaN have been studied using various techniques and with various surface treatments [19].

1.3 AlGaN/GaN HEMTs

Schottky contacts are versatile, rectifying devices which have been used by device engineers as the gate contact of high-electron mobility transistors (HEMTs) capable of operating at microwave frequencies. HEMTs are important in modern technology due to the need for devices to operate at higher frequencies than the lower mobility of silicon allows. Also, power densities from GaN-based HEMTs are over ten times higher than that from GaAs HEMTs [7]. Typical needs for higher frequency devices are spurred by the demand for ever-increasing communication system speeds [20].

The basic structure of a GaN based HEMT is illustrated in Figure 2A with a dual-layer mask to be discussed in Section 2.2.6. A sample band diagram is shown in Figure 2B. The operation of a HEMT is similar to that of a field-effect transistor and relies on the high mobility of the semiconductor and the ability to vary the band gap and doping to cause a two-dimensional electron gas (2-DEG) to form at the interface of two epitaxial layers. This 2-DEG acts as a channel for charge flow between the source and drain. A
potential applied to a gate contact allows control of the amount of conduction through this channel. In the case of a HEMT, the gate is formed by a Schottky contact between the source and drain. Ideally, no current will flow through the gate. Also, current flow through the HEMT can be stopped with an adequately applied gate voltage in a condition known as pinch-off.

![Figure 2 – (A) Basic HEMT structure with layer thicknesses not to scale and (B) sample HEMT band diagram.](image)

Many fabrication issues can affect the operation of HEMT devices. In modern HEMT preparation, the semiconductor surface is exposed to multiple phases of photoresist deposition, annealing, etching, cleaning, and finally expected to be free of localized defects during the final Schottky contact gate deposition. HEMT fabrication research to date has centered on obtaining the highest frequency devices with the best operating characteristics while maintaining the minimum number of steps during processing. The resulting devices have been highly successful considering the amount of damage inflicted on the surface of the semiconductor during processing and the quality of
the substrates. The localized states affecting the Schottky gate contacts degrade the performance of HEMTs and studies are being done to understand these phenomena [21, 22].
CHAPTER 2.

EQUIPMENT AND TECHNIQUES

A variety of AlGaN and GaN samples were used in the following experiments. Experiments involving the fundamental examination of Schottky barrier formation were performed on thicker layers of GaN, both grown by MBE and MOCVD. Device work was performed on samples designed with a 2-DEG incorporated into the growth for final HEMT device fabrication. The substrates used include both sapphire and SiC. These samples consist of the highest quality material for making state-of-the-art devices at the time of the sample growth. The samples are outlined in Table 2. For simplification in comparison and discussion, sample ID numbers are used throughout the text to indicate the specific wafer the results originate from as detailed in the table below.
<table>
<thead>
<tr>
<th>Sample ID</th>
<th>Substrate</th>
<th>Structure (From Top Layer Down)</th>
</tr>
</thead>
<tbody>
<tr>
<td>F01B</td>
<td>6H-SiC</td>
<td>AlGaN Contact Layer (190 Å), UID, x=0.28 GaN Channel/Buffer Layer, (1.51µm), UID</td>
</tr>
<tr>
<td>C11B, C</td>
<td>4H-SiC</td>
<td>AlGaN Contact Layer (120 Å), UID, x=0.21 AlGaN Donor Layer (80 Å), Si 2e18, x=0.21 AlGaN Spacer Layer (30 Å), UID, x=0.21 GaN Channel Layer (200 nm) AlN Buffer Layer</td>
</tr>
<tr>
<td>B10</td>
<td>SiC</td>
<td>AlGaN (250 Å), x=0.25 GaN (1000 nm) AlN</td>
</tr>
<tr>
<td>G01</td>
<td>Sapphire</td>
<td>GaN (3 µm), undoped</td>
</tr>
<tr>
<td>H01</td>
<td>Sapphire</td>
<td>GaN (700 nm), Si 2e18 cm⁻³ GaN (300 nm), UID AlN (20 nm)</td>
</tr>
</tbody>
</table>

Table 2 - Sample identification and descriptions.

The many techniques utilized in performing the experiments in my thesis can be categorized into two main groups: sample processing techniques and sample analysis techniques. The processing techniques include both standard device fabrication processing necessary to build HEMT devices as well as various surface preparation and modification techniques. Sample analysis techniques determine the condition of the sample surface and bulk properties throughout fabrication and determine the effects of surface processing on sample characteristics. The various techniques will be described in detail as they fall under these categories following a discussion of the major equipment used.
2.1 Equipment Overview

The experiments were performed at both The Ohio State University (OSU) in the Electronic Materials and Nanostructures Laboratory (EMNLAB) and Wright-Patterson Air Force Base (WPAFB) in the cleanroom of the Air Force Research Laboratory. All ultra-high vacuum (UHV) work was performed at OSU and all processing requiring the use of a cleanroom was performed at WPAFB. In many experiments, samples were repeatedly transported from the cleanroom to OSU and back for continuous processing and sample analysis steps.

2.1.1 Cleanroom

Device processing and photolithography was performed in a state-of-the-art class 10/100 cleanroom facility. The cleanroom is equipped with wafer spinners, mask aligners, UV lamps, digitally-controlled hot plates, a thickness profilometer, optical microscopes, a scanning electron microscope (SEM) with focused ion beam (FIB) capabilities, reactive ion etching (RIE), DC and RF electrical test equipment, an electron-beam metallization chamber, and a plasma enhanced chemical vapor deposition (PECVD) SiO$_2$ and Si$_3$N$_4$ deposition system. Constant humidity and temperature monitoring maintain the stable environment necessary for reproducible device fabrication.
2.1.2 Ultra-High Vacuum (UHV) Systems

Ultra-high vacuum is necessary to analyze samples where maintaining a clean sample surface is required. Within the UHV environment, one of the greatest sources of contamination and damage is from the incident electron beam focused on the sample surface [23, 24]. Carbon deposition can occur, although this can be kept at a minimum if simple cleaning procedures are followed. Maintaining a clean surface is extremely important when studying cleaved samples and the UHV systems were baked out after venting for maintenance so that the background pressures could be kept at a minimum. Two UHV chambers at OSU were used for sample analysis: an SEM chamber and a metallization and analysis chamber.

2.1.2.1 SEM Chamber

The SEM utilized for these experiments was a JAMP-7800F manufactured by JEOL. The microscope was modified in-house to include a multi-function processing chamber capable of Au and Ag metallization, sample cleaving, and sample heating. The SEM microscope can achieve a 5 nm beam spot size under appropriate electron beam conditions and includes a high-resolution electron analyzer with 50 meV resolution. Finally, a monochromator/photomultiplier tube (PMT) combination, UHV liquid helium cryo stage, and data collection system attachment from Oxford allows cathodoluminescence (CL) sample analysis at liquid helium temperatures. Due to the collection angle of the electron analyzer with the sample mount and the restrictions based
on the collection mirror required for CL analysis, different stages must be employed depending on whether electron or photon collection is desired.

2.1.2.2 Metallization and Analysis Chamber

A UHV chamber was utilized for both metallization and sample analysis of certain HEMT devices to investigate the effects of gate channel modifications on overall device performance. This UHV chamber achieves an ultimate base pressure of ~8x10^{-11} Torr and includes metallization capabilities using an interchangeable Ti or Pt source as well as independent Ni, Al, Au, and Ga evaporators. Auger electron analysis of the sample is performed using a single-pass electron analyzer with a coaxially-mounted electron gun. An ion sputter gun can also gently clean the sample or etch rapidly for depth profile surveys. Through specially-designed sample mounts, samples can be heated to temperatures in excess of 800°C for specific annealing or cleaning steps. Finally, room-temperature CL analysis is possible using a fiber-optic cable brought to the sample surface with spectrum analysis using an Oriel monochromator and CCD setup.

2.2 Fabrication and Processing Techniques

HEMT devices were processed using standard fabrication techniques. A simplified fabrication process flowchart is shown in Figure 3. Many fabrication techniques were required to complete fabrication of HEMT devices in the cleanroom and these will be discussed in the following sections.
2.2.1 Photoresist and Mask Alignment

Each stage of processing requires the precise alignment of masks used to transfer device features to the photoresist and eventually to the sample. Two types of mask
aligners were used: a Karl Suss MJB-3 and a Karl Suss MA-6 aligner. Both systems are used in contact photolithography and utilize high-pressure mercury arc UV lamps as the primary light source. The MA-6 is capable of handling up to 6” wafers with 7” masks while the MJB-3 can handle samples as large as 3” in diameter. With careful sample alignment, odd-shaped pieces of varying thicknesses can also be aligned with both of these systems.

Photoresists appropriate to the process step were chosen. In most cases, the Ohmic and gate contacts required lift-off steps following metal deposition [25]. For these purposes, two-layer masks consisting of SF-11 and Shipley 1805 photoresist with two-step developing was used.

The processing of sample C11 required a special dual-layer mask composed of Si$_3$N$_4$ and SiO$_2$ as originally explored by Dr. Gregg Jessen, currently a staff scientist at the Air Force Research Laboratory, Wright Patterson Air Force Base, Dayton, OH [26]. This mask allows the processing of the sample prior to gate metallization within a UHV environment where standard organic masks would begin to decompose, outgas, and contaminate the chamber. Details of the mask formation are in a separate section below.

2.2.2 Annealing

Annealing is important in the processing of semiconductors. Many reactions require a minimum heat of formation or reaction temperature. When these reactions are desired, it is necessary to supply the necessary kinetic energy to allow the reaction to occur. On the other hand, the halting of the reaction through an appropriate cooling of
the sample can prevent unwanted decomposition or further reaction and damage that can destroy the devices. In such situations, a controlled rapid thermal anneal (RTA) provides the necessary temperature and timing as well as an appropriate ambient gas flow to reduce oxidizing agents and to cool the sample to quench the reaction.

For Ohmic processing, a dry nitrogen purge followed by an RTA of 800°C for 30 seconds in flowing dry nitrogen allowed reactions to occur at the metal-semiconductor interface for the formation of a low-resistance Ohmic contact. The typical metal stack used on the AlGaN/GaN device structures involved Ti/Al/Ni/Au. A computer-controlled Steag SHS100 RTA system was used for these process steps.

During gate processing of sample C11, various annealing steps were necessary prior to gate deposition to allow damage caused to the surface through the ion sputter or Ga reflux method surface cleanings to be partially repaired. It is crucial that the gate region of the sample have the least amount of subsurface damage for well-behaved Schottky contacts to form. These anneals were performed in the metallization and analysis chamber through the use of resistively heated coils embedded in the molybdenum sample block. The sample temperature was monitored using a pyrometer through a 6-inch quartz viewport.

2.2.3 Metallization

Controlled evaporation and deposition of metals was necessary in nearly every stage of device fabrication. A variety of metal evaporators provided pure metal depositions ranging from fractions of a monolayer to hundreds of nanometers in thickness.
depending on the process step involved. Metal thickness monitoring was accomplished using quartz crystal oscillators (QCOs) calibrated to both the density and z-ratio of the specific metal as well as the deposition geometry dictated by the chamber incorporated into the measurement through a tooling factor.

The simplest metallization was performed in the cleanroom using a commercial, computer-controlled electron-beam metallization system. A rotating turret mount ensured uniform coverage of each metal and computer monitoring of the entire process maintained appropriate pressures and deposition rates. Although the chamber pressures were typically in the mid-10⁻⁷ Torr during deposition, excellent device performance results were obtained for all contacts deposited using this system. Pre-metal dips of diluted HCl and other chemicals were employed to remove any surface oxides and contaminants prior to metallization.

The metallization and sample analysis chamber also allowed for a variety of metals to be deposited within an UHV environment as mentioned previously. Independent dual-metal sources mounted on different ports with shielding between the two sources ensured minimal cross-contamination of the metals. A rod-source electron-beam evaporator was used for Ni deposition while resistively-heated baskets containing alumina crucibles were used for Ga and Au deposition. Calibrations were performed on two QCOs positioned for optimal metal thickness measurements using thicknesses of metal deposited on Si samples with a wire grid placed over the surface. The gaps were then measured using a Tencor profilometer and the corresponding tooling factor was determined.
In this particular chamber, accurate sample placement is also necessary and was achieved using an oversized stainless blank as shown in Figure 36 for Ga upon which the deposition pattern was determined for specific, reproducible placements of the sample mount during actual metal deposition as determined from the various micrometers and angle measurements available on the sample manipulator. During the evaporation of Au and Ga from the thermal sources which have a known, non-uniform resulting deposition pattern, the sample mount was repeatedly shifted from side to side \(~5\) mm to promote an even coverage of metal on the sample surface.

The JEOL SEM was equipped with a metallization system for depositing Au on GaN in the study of the formation of Schottky barriers to GaN. While original work was performed using a crucible heater similar to that described previously, a deposition system implementing coil heaters was later incorporated into the sample transfer system to allow for the changing of the metal sources without breaking UHV in the process chamber. This was necessary to allow for rapid source refilling as well as the changing of source material from Au to Ag without the otherwise tedious and time-consuming process of baking out the chamber [27]. Details of the designed system are included in the Appendix.

2.2.4 Ion Sputtering

Ion sputtering involves the bombarding of a surface by ions generated within an attached ion gun. The energy of the ions determines the amount of damage the impact produces and this control allows the technique to be used in a variety of tasks. In general,
a low-power ion beam can be used for charge compensation during electron-beam bombardment of insulating samples, although this is not usually effective, while a higher-power ion beam will create greater damage and actual sputtering of the surface which is useful for depth profiling [28]. In processing sample C11, a lower beam energy was used in order to clean the surface of the sample despite difficult beam alignment. To make the ion beam barely visible on the sample surface and allow for the proper placement of the beam, the beam energy was increased to a maximum of 3.5 keV. In addition, nitrogen ions have been shown to give the best results in cleaning GaN due to the nature of the material [29]. Typically, nitrogen vacancies (V_N) form at the GaN surface and to avoid these, a nitrogen ion beam tends to force nitrogen into the lattice replacing some of the lost nitrogen maintaining a better surface than noble gas ion beams.

2.2.5 RIE Etching

Dry etching techniques have become critically important in fabricating devices from robust materials such as GaN and AlGaN. While GaN can be etched using wet chemicals, the etch rates are extremely slow. For this reason, many techniques have been investigated in an attempt to increase the speed of the etching, including photo-assisted electrochemical etching and dry etching. Typically, dry etching consisting of RIE or inductively-coupled plasma (ICP) etching is utilized because of the fast and satisfactory results obtained for mesa isolation etches [2]. In my work, RIE plasma etching [30] was used both in mesa isolation and in dual-layer mask etching.
The largest hurdle in using such dry etching techniques is that the plasma causes both localized heating of the material being etched and the high-energy particles that contact the surface can impose damage many monolayers to a typical depth of 400-600Å into the surface creating a variety of detrimental localized states that can severely degrade device performance. Anneals can be performed to attempt to repair the surface of the sample, but the damage is typically extensive and not entirely reversible [3, 31]. For GaN mesa isolation etching, the damage is usually an acceptable trade-off because of the difficulty in utilizing other etching methods. In our study, however, it was important to maintain the lowest possible amount of etch damage because the surface being etched in developing the SiO₂/Si₃N₄ mask was the Schottky gate contact region, one of the most sensitive regions of the HEMT device. To minimize this damage, the lowest possible power and bias voltage were used that still gave a satisfactory profile and etch rate for the dual-layer lift-off mask.

Reactive ion etching (RIE) of the sample surface is necessary during standard processing for mesa isolation of each transistor structure. The different chemistries used to achieve the undercut etch will be discussed in the relevant section of sample C11.

2.2.6 Dual Layer Mask

Plasma-enhanced CVD (PECVD) deposition of the mask layers produce uniform films free of pinholes and other anomalies with thicknesses of 4000Å Si₃N₄ and 2000Å SiO₂. This was followed by a dual SF11/1805 photoresist spin-on for transferring of the mask to the underlying Si₃N₄/SiO₂ mask material. After the necessary photolithography,
the 1805 photoresist was removed and the SF-11 mask was used in a dual process RIE etch discussed in a following section for final mask preparation.

The Si$_3$N$_4$/SiO$_2$ mask was required to allow for UHV surface treatments and preparation prior to gate metal deposition with minimal outgassing. Typical lift-off masks are developed using a combination of PMMA and standard photoresist. While these compounds produce the desired dual-layer mask necessary for clean lift-off while minimally affecting the surface, they are both organic-based and outgas when introduced in a UHV environment. SiO$_2$ and Si$_3$N$_4$ were chosen because of the availability of these compounds to be grown using a PECVD system due to their typical use in passivating the AlGaN surface after device fabrication and for their UHV compatibility and the ability to withstand higher temperature anneals. While the Si$_3$N$_4$/SiO$_2$ mask used in this research was developed independently, a variation was later discovered to have been developed using a final acid etch of a bottom SiO$_2$ layer by another group [32].

In developing the mask, many hurdles had to be overcome. Deposition of the films was relatively simple because of the typical depositions made for device passivation as mentioned earlier. Etching the dual-layer structure was difficult and many attempts were made on test samples before a satisfactory etch recipe was developed. RIE plasma etching was utilized as the etching could be adjusted based on the composition of the gases used and the platen such that the sidewalls of the SiO$_2$ could be made to etch in an anisotropic manner while the underlying Si$_3$N$_4$ could be etched in an isotropic manner to form the necessary undercut.

Lift-off of the Ni/Au gate metal layer deposited on this mask had to be modified from the standard “adhesive tape” technique typically employed. An acetic acid/NH$_4$F
etch was used to undercut the mask prior to lift-off due to the strong adhesion of the metal layer on the mask itself. With the addition of this step, it was found that successful lift-offs could be performed reproducibly without damaging the exposed Ohmic contacts. This will be discussed more fully in the C11 sample processing section.

2.2.7 Sample Cleaving

As mentioned earlier, the study of contact formation requires that the surface be as free from localized states prior to metal deposition as possible. For this reason, many researchers have studied contacts made to semiconductor surfaces cleaned by various surface preparation techniques and qualified using either low-energy electron diffraction (LEED) patterns or AES. While this is a useful approach to studying samples that will be processed in air, it is difficult to study the actual contact formation mechanism in this manner because the cleaning, no matter how gentle the approach, inevitably modifies the sample surface [33]. To study the underlying fundamental mechanism of contact formation, an ideal, atomically-flat surface is needed and this can be acquired through the use of sample cleaving in UHV [18].

Many techniques have been developed to cleave samples in UHV. The method used throughout the majority of my studies has involved cutting the backside sapphire substrate of the sample with a diamond saw along an expected cleavage plane to a depth of about 0.25 of the total thickness of the sample. This is necessary because sapphire, or corundum, is not known to cleave, but rather exhibits parting [34]. The sample is then mounted on a cross-sectional sample mount that holds the sample vertically in UHV. A
wobble stick constrained in a railing mechanism to only allow one degree of freedom is used to strike the sample in a corner such that the sample in tension will cleave. Depending on the sample, this is important to ensure that the epilayer under investigation is not crushed during the cleavage process.

2.3 Analysis Techniques

Throughout the sample fabrication process, a variety of analysis techniques allow monitoring of the physical characteristics and continual evaluation of the sample quality. As discussed below, these techniques range from elaborate experiments involving the SEM to simple setups in the metallization and analysis chamber. Following the fabrication, the samples were subjected to electrical characterization in a probe station where device performance could be recorded and analyzed.

2.3.1 Auger Electron Spectroscopy (AES)

Auger electron spectroscopy (AES) is a powerful technique used to analyze the chemical nature of surfaces [23, 35, 36]. It is often combined with an ion sputter gun to perform depth profiles of the sample or to allow for sputter cleaning of the sample surface prior to analysis. AES is a surface sensitive technique since any Auger electrons originating deeper than the top few monolayers will lose too much kinetic energy colliding with the crystal lattice and will become part of the background signal. This escape depth is given most simply by the following expression [37]:

$$\lambda_r(\varepsilon) = \varepsilon / [a(\ln \varepsilon + b)] \text{ (Å)}$$

(1)
A table must be consulted in the reference for the variables a and b which are constants related to the sample material and \( \varepsilon \) is the incident electron beam energy in eV. The fundamental physical processes that occur to generate an Auger electron are three-fold. An incident electron has a predetermined energy and upon colliding with an atom in the lattice, a portion of the energy removes an electron from a core level creating a hole. A second electron from an outer level relaxes and shifts to the newly formed hole releasing its energy to a third electron in an outer level. This third electron then has enough energy to leave the atom and is termed the Auger electron which is subsequently collected by an electron analyzer and detected by an electron multiplier [38].

Although the technique is typically used to determine the presence or absence of particular elements, with a high enough energy resolution and sensitive electron multipliers, it can be used to study shifts in the core levels at the surface layers. This is because as a thin metal overlayer is applied to the surface, the bands will bend as previously mentioned during contact formation. With this band-bending, the core levels of the semiconductor will also shift and this will be detectable by observing the shift in the AES signal prior to and after deposition.

2.3.2 SET/Work Function Measurements

An extension of the AES method, secondary electron threshold, or work function, measurements provide information on the sample surface conditions on a micron scale. In the typical grounded sample situation of AES, the lowest-energy secondary electrons leaving the sample cannot be collected by the electron analyzer because of the higher
work function of the analyzer itself. Through an appropriate negative biasing of the sample, the secondary electron onset or threshold can be measured when the bias is increased above the analyzer work function [39]. This is a particularly useful technique to employ when investigating contacts between two layers since the relative work functions can be compared and the change in work function can possibly give insight into the processes involved in the formation of the contact.

2.3.3 Electron Backscattering Pattern (EBSP)

In studying cleaved epilayers of GaN, it is necessary to know the exact orientation of the sample and to identify the surface being analyzed. A typical SEM image cannot be used to determine this information. Through the use of an EBSP setup in another SEM, the exact crystal orientation was determined. The use of EBSP to analyze GaN is relatively recent as outlined by Trager-Cowan et. al. [40], while similar crystal structure analysis has been performed for other materials [41]. EBSP analysis I obtained from samples used in studying Schottky barrier formation in Chapter 3 from sample H01 is shown in Figure 4 with the necessary crystal directions and planes indicated. Through the amount of offset in the crystal with the camera and knowledge of the cleave plane direction, sample cleaving can be performed obtaining the desired GaN surface for Schottky barrier formation studies.
2.3.4 Cathodoluminescence (CL)

CL analysis is performed in UHV using an electron gun to create electron-hole pairs in the semiconductor. A monochromator is used externally along with either a CCD array or a photomultiplier tube (PMT) to collect the photons that are emitted from the sample when the electron-hole pairs recombine [42, 43]. The light collection can be performed in a variety of ways. In a standard setup, a fiber optic is placed near the sample surface and light is collected through this mechanism because a tight control of the electron beam is not critical. In the SEM, however, the light is collected using a parabolic mirror that is designed to collect ~75% of the incident light emitted from the sample. The aluminum mirror has a 1 mm aperture that allows for the electron beam to pass through [44] while minimizing the distortion to the scanned beam that would be

Figure 4 - EBSP pattern of GaN sample H01 used to determine crystal orientation.
possible if a fiber optic capable of charging were to be placed near the path of the electron beam.

An interesting aspect of CL utilized in many setups can be explored by varying the voltage of the incident electron beam. Due to the penetration depth of the resulting electrons, a depth dependent study can be performed of the sample. By varying the voltage in a manner that maintains low voltages, it is possible to probe the sample from the surface to the bulk in plan view. Various methods have been proposed to calculate the resulting depth in the semiconductor that is being probed by the incident electrons. One such method was explored by Everhart and Hoff [45]. In that work, a relationship between the kinetic energy of the incident beam and the maximum depth of penetration was termed the Bohr-Bethe range. This was later expanded by Kanaya and Okayama to include a better fit to more elements as given below [46]:

$$R_v = \left(\frac{0.0276A}{\rho Z^{0.889}}\right)E_b^{1.67} (\mu m)$$  \hspace{1cm} (2)$$

In this equation, $E_b$ is the electron beam energy in keV, $A$ is the atomic weight in g/mol, $\rho$ is the density in g/cm$^3$, and $Z$ is the atomic number. Another approach is to use a Monte-Carlo simulation and calculate from this the statistical average of the depth of penetration. One popular program used for this is CASINO [47].

It is important to note that CL analysis is a powerful technique for analyzing samples since the UHV environment can maintain the surface chemical and electronic conditions resulting from the given surface treatment. For example, the samples fabricated into working HEMT devices can be analyzed prior to surface treatments, after a treatment to ensure the sample has been modified as expected and to record the effects of the treatment on the sample just prior to metal deposition, and also after the metal
deposition has taken place. It has been shown that CL can be used to investigate localized states in semiconductors [48]. These results can be used to monitor the localized states that are luminescent and to determine exactly what states are forming or being removed by the surface treatment with minimal damage to the sample surface.

In the SEM setup, light collected from the sample using a parabolic mirror is dispersed by a 1200 rules mm\(^{-1}\) grating in an Oxford MonoCL monochromator. The photons are then detected using a high-sensitivity Hamamatsu R943-02 photomultiplier tube in a Peltier-cooled housing.

When recording CL spectra, several variables must be considered and controlled in order to obtain reproducible results. System settings, i.e. beam voltage, current, and multiplier settings, must be maintained at the same values for comparisons taken between scans from different days. Also, sample behavior during electron beam bombardment must be considered since some samples are damaged or changed by exposure to the electron beam [24]. Sample C11, for example, exhibits typical CL spectra for GaN at room temperature as shown in Figure 5 with electron-beam effects for an incident electron beam with energy of 5 keV at 0.5 mA over a period of 26 minutes as shown. Due to the dual-layer gate mask covering the surface and the analog control of the beam spot size, an exact measurement of the incident beam area is unknown. The defect luminescence centered at ~2.19 eV increases in intensity with exposure while the near band edge luminescence decreases.
Figure 5 - Room temperature CL of sample C11 through the dual-layer mask. A 5 keV electron beam at 0.5 mA was used to examine the sample.

The defect yellow luminescence (YL) was summed from 1.89-2.43 eV and the near band edge (NBE) was summed from 3.34-3.43 eV and plotted as a function of time in Figure 6. Additionally, the NBE:YL ratio is plotted revealing two regions with different rates of change between the NBE and defect emission. The NBE decreases at a decaying exponential rate from its initial stable value. The YL rapidly increases during the first ~1.5 minutes and then stabilizes. The subsequent decrease and increase in YL may be due to a shift of the beam on the sample with charging and heating of the sample surface. The electron beam was turned off at the time indicated to determine the
permanent nature of the intensity changes. Despite a 175 second interval of the electron beam being off, the intensities remained at the same level afterward.

Figure 6 - Time-dependent electron beam effects on near band edge (NBE) and yellow luminescence (YL) with fitted curves shown in red. Upon turning off the e-beam during the 175 second period shown, the intensities remained at the same level.

Possible reasons for such changes in intensity include a filling of states and local temperature increases with electron beam exposure [42]. The shifting of rates away from saturated recombination pathways can result in decreases in luminescence intensity. In addition, localized heating can lead to other non-radiative recombination. Finally, sample contamination from carbon deposited during irradiation can also reduce intensity with prolonged scans [49]. To minimize such effects during sample analysis, low beam
currents were used and scans were taken as quickly as possible after alignment was complete.

2.3.5 DC Electrical Measurements

The various fabricated devices were tested for standard current-voltage (I-V) characteristics. A current applied to the Ohmic contacts, Schottky contacts, and various device structures results in a recorded voltage drop across the contact. The results reveal details about the quality of the contact and the semiconductor. I-V curves were recorded using either an automatic probe station setup or a manual probe station depending on both the device and sample fabrication stage of the sample being analyzed. The manual probe station with an HP4145B analyzer was used to measure individual contacts and devices when more extensive, specialized analysis was required, such as in analyzing failed devices.

Various techniques may be used to record I-V data. The simplest method is to use a two-probe technique where a current source and a voltmeter are used to analyze the junction by placing one probe on each of two contacts and forcing a current to flow between the two contacts. The voltage required to generate this current is then recorded. Alternatively, the voltage can be ramped and the current monitored, however this requires careful monitoring of the current to limit the supply should the contacts begin to rapidly conduct electricity which could possibly cause damage during the measurement process.

Another technique often used is to place four probes on two pads and to use one pair of probes for each of the voltage and current. With this setup, a calculation can be
performed to eliminate the contact resistance between the probe and the contact pad resulting in a more accurate measurement of the actual contact resistance of interest between the contact pad and the semiconductor.

Automatic probe station measurements of the Ohmic contacts and related process control structures were recorded using a Keithley 450 system. The associated probe station was an Electroglas model and provided precise movement and placement of the sample during measurements.

To explain differences in Schottky barrier heights, it is necessary to understand the underlying mechanism responsible for the Schottky behavior and the corresponding analysis to obtain Schottky barrier heights from the I-V curves [11-13, 50]. Ideally, thermionic emission over the Schottky barrier will dominate the current transport as given in Equations 3 and 4 with the Richardson constant as given in Equation 5 [11].

\[
J = J_0 \{\exp(qV/kT) - 1\} \\
\text{with} \\
J_0 = A* T^2 \exp(-q\phi_b / kT) \\
\text{and} \\
A* = 4\pi m^* q k^2 / h^3
\]

Before performing an analysis of the Schottky diodes, it is necessary to determine the Richardson constant as given in Equation 5. The typical method of extracting the Richardson constant is through a plot of a modified Norde equation given in Equation 6 [50]. When curves are taken for varying temperatures, A* can be found along with the Schottky barrier height. A* varies depending on many factors and in the absence of an
experimentally determined Richardson constant, the published or theoretical value must be used.

\[ F_1 = \left( \frac{qV}{2kT} \right) - \ln\left( \frac{I}{T^2} \right) \]  

(6)

Incorporating image force lowering in the form of an ideality factor, \( n \), into the standard thermionic emission equation results in a more complete description of thermionic emission as shown in Equation 7 after [11]. This equation incorporates a bias dependence on the overall current transport mechanism. The addition of \( n_2 \) demonstrates two ways that various authors have dealt with the inclusion of the ideality factor. The equation can simply take the form of Equation 3 where \( n_2 = n_1 \) or \( n_2 \) can be chosen as ideal \( n_2 = 1 \). In the dual-Schottky barrier work of Chapter 5, it was found that \( n_2 = 1 \) produced the best fits to the data following the work of Skromme et. al. [51] and was chosen as the functional form describing the dual Schottky barriers.

\[ J = J_0 \exp\left( \frac{qV}{n_1 kT} \right) \left[ 1 - \exp\left( \frac{qV}{n_2 kT} \right) \right] \]  

(7)

Of particular interest is the concept of the ideality factor. As shown in Figure 7, the ideality factor can vary from \( n = 1 \) in three distinct regions for a single barrier. First, in the low-current regime, recombination in the depletion region can dominate and the value for \( n \) can approach 2. Second, with a higher applied voltage, high-level injection can dominate. Finally, series resistance dominates in the highest current levels and this term causes the I-V curve to deviate from a linear relationship on an ln(I)-V plot of the Schottky diode current as mentioned previously and seen in Figure 50.
Figure 7 – Forward-current diode curve variations in ideality factor, n, for different current transport mechanisms (After [52]).

To analyze the diode curves, two different techniques were combined: analysis using standard modeling from Equations 3 - 7 with parameter extraction from forward I-V plots and analysis using a variation originally proposed by Norde using modified forward I-V plots with high series resistance taken into account. The problem of samples exhibiting high series resistance becomes apparent when analysis is attempted on a standard I-V plot due to the rapid onset of the series resistance region and extremely small thermionic emission region for Schottky barrier height extraction. To circumvent this problem, Norde proposed plotting the I-V curve using a modified function given in Equation 8 [53].
\[ F(V) = \frac{V}{2} - \frac{1}{\beta} \ln \left( \frac{I}{AA^{*}T^{2}} \right) \] (8)

For well-behaved Schottky diodes, the function produces a curve with two distinct regions of slopes \(-1/2\) and \(+1/2\). At the minimum point, a series of equations can be solved that yield both the series resistance and the Schottky barrier height for the diode as given in Equation 9. As mentioned previously, the Richardson constant can vary from sample to sample, but since this uncertain variable is in the \(\ln\)-term of Equation 8, the effect of an error in \(A^{*}\) is reduced [50].

\[ \phi_{b} = F(V_{0}) + \frac{V_{0}}{2} - \frac{kT}{q} \] (9)

In addition, inhomogeneous Schottky barriers may display two distinct Schottky barrier heights that can be modeled independently. Early work in silicide contacts on Si where the parallel Schottky barriers could be formed resulted in clear double-Schottky barriers that could be modeled in this manner [54, 55]. A lower Schottky barrier patch in parallel with a higher Schottky barrier patch will produce a total current as shown in Equation 10 [51]. The saturated current equation is given in Equation 11 and depends again on the Richardson constant, \(A^{**}\). The linear extrapolation of the Richardson constant for AlGaN was used, although a determination of this constant can be made using temperature-dependent data analysis.

\[ I = \left( I_{sat,1} \exp \left[ \frac{q(V - I^{*}r_{S_{1}})}{n_{1} kT} \right] + I_{sat,2} \exp \left[ \frac{q(V - I^{*}r_{S_{2}})}{n_{2} kT} \right] \right) \left( 1 - \exp \left[ -\frac{qV}{kT} \right] \right) \] (10)

where

\[ I_{sat,1,2} = SA^{**}T^{2} \exp \left[ -\frac{q\phi_{b}}{kT} \right] \] (11)
An appropriate fitting of Equation 10 to data that clearly demonstrates a dual-Schottky barrier can be performed and the two saturation currents $I_{sat,1}$ and $I_{sat,2}$, series resistances $r_{s1}$ and $r_{s2}$, and ideality factors $n_1$ and $n_2$ can be extracted. Care must be taken in fitting this equation, however, since the equation is recursive. An iterative approach was used in this analysis. Once these values have been determined, the final Schottky barrier heights can be extracted using Equation 11. This calculation depends on the area of the contact where the sum of the areas for each Schottky barrier height should be used. Unfortunately, when the individual areas are not known, two approaches can be used to extract the Schottky barrier heights: using the total area or half of the area as an approximation or calculating the area from the material resistance. The first approach leads to an error due to the area. The second approach can be fit using a modified Equation 10. Setting $R_{s1} = R_{mat}/(S*fp)$ and $R_{s2} = R_{mat}/(S*(1-fp))$ [56] allows the fit to constrain the area to the total area using a best-fit material resistance, $R_{mat}$, and fractional part, $fp$, of the area for the lower Schottky barrier region where $S$ is the total diode area.

Although the model utilizing the two Schottky barrier height patches has been found to produce a reasonable fit to the actual data, further refinements of the model are necessary to incorporate actual physical effects due to parallel Schottky barriers. For example, when two Schottky barrier patches are modeled using Equation 10, the interface between the patches is assumed to be abrupt. Physically, the interface region must transition over a finite distance and the lower Schottky barrier height region will pinch-off depending on the higher Schottky barrier height region and the actual size and geometry of the lower barrier height patch [57-59]. The complicated models that correctly account for these effects are difficult to fit and will not be used in the analysis.
of dual Schottky barriers in Chapter 5. In addition, interface states and other effects are not accounted for in the dual Schottky barrier model which would need to be included to fully model current transport across the Schottky barrier.

2.3.6 RF Electrical Measurements

High frequency devices such as HEMTs require the use of specialized testing methods to determine the characteristics of the device. Typically, a network analyzer is used to extract the s-parameters of the device by applying high frequency test signals and observing the behavior of the reflected and transmitted portions of the test signal. From this data, the computer is able to calculate the frequency response and output the gain, frequency, and breakdown voltage characteristics of the devices. Using this data along with data collected from other techniques, the device performance characteristics at the high frequency, small-signal level can be determined. The equipment used for these measurements was located in the cleanroom at AFRL and included an HP 8510C network analyzer and HP 8517A S-parameter test setup used to measure the high frequency performance of the HEMT devices. HP also manufactured the associated sweep generators and voltage sources.

2.4 Sample Uniformity

Throughout the experiments, the problem of sample non-uniformity often surfaced and required an initial investigation of the sample to ensure an appropriate baseline of the sample condition was established prior to further processing or analysis.
An example of the importance of this aspect was investigated in high Al alloy composition AlGaN. The original samples are shown in Figure 8 with the analysis positions labeled as shown. The samples were taken from the same wafer.

Figure 8 - Analysis positions for MOCVD grown AlGaN samples.

CL scans were acquired at the locations shown by red dots and the initial scans from these locations are shown below in Figure 9. As can be seen in this figure, the AlGaN near-band edge (NBE) signature varies from 4.66 to 4.86 eV. Assuming a bowing parameter of 1.0 and using Equation 12 [60, 61], this corresponds to an Al alloy composition of $x = 0.54$ to 0.60.

$$E_g(x) = (1-x)E_g(GaN) + xE_g(AlN) - bx(1-x)$$  \hspace{1cm} (12)
This amount of variability in the bandgap for a particular sample can make determinations of the effects of sample processing on emission behavior difficult to determine. It is important, therefore, to determine pre-scans of the sample condition prior to processing which serves two purposes. First, the sample uniformity and suitability for the experiment can be determined and new samples acquired if necessary. Second, a baseline is set by which further processing and analysis changes can be compared. This is especially important in samples that will be subjected to rigorous processing and where comparisons of the final sample condition will be made across large areas.
CHAPTER 3.

SCHOTTKY BARRIER FORMATION ON CLEAVED, NON-POLAR GaN

3.1 Introduction

Understanding Schottky barrier formation and operation is essential to the engineering of many modern semiconductor devices. In particular, the physical properties of GaN and related III-N semiconductors are highly suitable for high-frequency device performance and engineering. In light of this, it is important to understand and engineer Schottky barriers on GaN to fully optimize devices on these materials. Unfortunately, studies to understand the nature of Schottky barrier formation at metal-GaN interfaces are complicated by two factors. First, GaN is available almost exclusively in epitaxial form, unlike most conventional semiconductors, so that large area cleavage surfaces are unavailable for studying clean, ordered surfaces macroscopically. Up to now, the majority of band bending studies have been performed using photoelectron spectroscopy (PES) in which the incident excitation beam could not be confined to the nanometer scale. Second, the only macroscopic surfaces available are polar, giving rise to pronounced piezoelectric effects that introduce potential changes in addition to those associated with the surface band bending. In order to obtain clean, atomically-ordered surfaces of GaN (0001), researchers have employed a variety of
methods, including ion sputter cleaning and annealing, thermal desorption, various chemical etches, and a Ga-reflux method [29, 62-64]. Many studies have shown that such cleaning techniques can introduce surface or sub-surface defects that can affect the semiconductor’s Fermi level, \( E_F \), position before and after metal contact formation. See, for example, references [13, 29, 33, 65-68].

A new approach for studying the interface formation of Schottky barriers to GaN that avoids these adverse effects and allows the study of both the relative band-bending and relative work function variations with metal deposition on the scale of a scanning electron microscope (SEM) beam diameter is demonstrated. In addition, cleaving a (0001) face wafer to reveal a non-polar face eliminates the piezoelectric effect and associated polarization charges normal to the cleaved surface. A further advantage of the focused electron beam size is that the ultra-high vacuum (UHV)-cleaved surface can be imaged to select microscopic areas that are relatively free of steps or other morphological artifacts. The work contained in this chapter is currently in press [69].

3.2 Experimental Methods

MBE-grown GaN samples were cleaved and analyzed under UHV conditions in a JEOL-7800F SEM equipped with a 50 meV resolution hemispherical electron energy analyzer. The (-12-10) family a-plane and (01-10) family m-plane cleavage planes were determined by electron backscattering pattern (EBSP) analysis in another SEM. A slot was cut on the backside of the sample along the respective cleave plane to promote a flat, cleaved surface. Gold and silver metal films were deposited in an attached UHV
processing chamber with film thicknesses determined by a quartz crystal oscillator thickness measurement system. The cleaved surface was analyzed iteratively before and after each metal deposition on a monolayer scale in order to monitor the initial stages of GaN contact formation.

The structure of sample H01 used in this experiment is given in Table 2. Analysis positions were reproducibly located following each metal deposition through the use of the SEM imaging capability. The analysis positions chosen were contained within the top Si-doped epilayer where the Fermi level in the bulk was calculated to be <0.005 eV below the conduction band.

The SEM was used to collect two types of data: Auger electron spectroscopy (AES) and secondary electron threshold (SET) measurements. The AES spectra analysis consists of monitoring the rigid shifts of undifferentiated Auger peak features that, in analogy to PES core level measurements [70-72], indicate the change in band bending with metal deposition. Since all three core levels involved in the Auger transition shift rigidly (assuming no chemical shifts), the net change in peak energy of the emitted Auger electron is equivalent to the rigid shift of all core levels and hence the band bending. We assume that the interaction energy between the two final state holes and the relaxation energy of the final state are independent of the surface configurations during metallization. High-resolution, undifferentiated spectra were recorded using a 3 kV, 4-5x10^-9 A electron beam and a linear background subtraction performed based on the ~10 eV region following the peaks of interest. Two Ga-LMM peaks were analyzed and the sharper of the two, the Ga L3M4,5M4,5 peak, was monitored with an energy resolution of between 0.05 to 0.20 eV to determine the peak energy shift for the Ga-core level as
shown in Figure 10. A deconvolution of the N-KLL peak reveals two overlapped peaks and the energy positions for both peaks were used to determine the energy shift in the N-AES core level at each point.

![Figure 10 - Representative Ga-LMM and N-KLL spectra used to determine Fermi level position relative to the band edges. Ga L_{3,4,5}M_{4,5} peak energies and the average of the two deconvolved N-KLL peak energies were used in Figure 12 and Figure 13 [69].](image)

SET measurements allow a determination of the work function of the sample. A –10 V bias applied to the sample insured that secondary electrons from a 3 kV, 4-5x10^{-10} A incident electron beam could overcome the work function of the analyzer and be collected [39, 73]. Figure 11 shows how the intercept of a line fit to the onset with the secondary electron baseline is used to determine the relative work function of the sample.
In some instances, multiple thresholds due to surface potential inhomogeneities were observed and the first significant threshold was chosen as the primary sample work function. This SET data combined with the AES-measured band bending permits one to monitor both the band bending and associated work function behavior of the GaN surface during metal deposition and Schottky barrier formation. Both techniques are highly surface sensitive with Auger electron escape depths of 10.4 Å for N-KLL and 17.5 Å for Ga-L₃M₄,5M₄,5 electrons as found using the curves and fit parameters for elements as reported by Seah and Dench [74].

![Graph showing representative work function determinations from secondary electron threshold with -10 V sample bias. All measurements are relative to the freshly cleaved surface offset to 0 eV. The SET threshold moves to higher energy as the Au overlayer becomes thicker. These threshold curves also change shape as the surface becomes more metallic and uniform in potential [69].](image)

Figure 11 - Representative work function determinations from secondary electron threshold with -10 V sample bias. All measurements are relative to the freshly cleaved surface offset to 0 eV. The SET threshold moves to higher energy as the Au overlayer becomes thicker. These threshold curves also change shape as the surface becomes more metallic and uniform in potential [69].
3.3 Results

Cleaving of GaN epilayer films grown on sapphire is difficult, although the two common cleavage planes for GaN are the (-12-10) a-plane and (01-10) m-plane [75, 76]. Kamler et al. reported that the m-plane could be more easily cleaved than the a-plane [75]. We also observed the overall cleaves to be poorer for the (-12-10) family a-plane surface, although more usable regions of high cleave quality were found on this face than on the (01-10) family m-plane surface.

In order to determine the overlayer uniformity, the peak height intensity of the N-AES signal versus metal deposition thickness was plotted. Figure 12 shows that N and Ga Auger electrons are attenuated exponentially with equivalent escape depths calculated from the curves’ slopes of 11.1 Å and 16.1 Å for N-KLL and Ga-LMM, respectively. These values are in good agreement with escape depths of 10.4 Å and 17.5 Å for 372 eV and 1053 eV electrons passing through a uniform Au film as mentioned previously [74]. This behavior indicates that the first few monolayers attenuate the escaping electrons as a uniform film coating the surface.
The Ga LMM and N KLL AES peak energies shift rigidly with GaN band bending at the cleaved surface. Their positions are shown in Figure 13 and Figure 14. In Figure 13, the Ga AES peak position is plotted for each metal overlayer coverage with the minimum starting value of 1051.35 ± 0.01 eV measured for (-12-10) Cleave A. The N peaks are unresolved and were analyzed by averaging their deconvolved peak values. Error bar increases with metal coverage reflect the lower signal-to-noise in measuring attenuated peak energies.
Figure 13 - Ga-AES energy position relative to the initial position of "good" Cleave A. The average final energy positions for all curves is 1053.06±0.04 eV [69].

Figure 14 - N-AES energy position relative to the initial position of "good" Cleave A. The average energy position for the "rough" cleaves was 375.81±0.19 eV [69].
In three “good” cleaves on the (-12-10) surface, as determined by the lack of visible features in the SEM image after the final gold deposition, the bands were observed to shift upward in energy for both the N-KLL and Ga-LMM peaks. The maximum shift in the Ga AES features was $1.71 \pm 0.05$ eV as shown in Figure 13, based on the sharper Ga L$_3$M$_{4,5}$M$_{4,5}$ peak. The N-KLL features shift rigidly with the Ga-LMM features for the first few Å and continue to increase, albeit with larger error bars due to the deconvolution and broader peaks.

The “rough” cleaves on the (01-10) surface, whose surface features were usually noticeable in SEM images only after the final metal deposition, were also investigated. Atomic force microscope images taken at a random location along the “rough” cleave after Au-deposition and removal from the UHV system revealed an RMS roughness of ~9.8 nm and feature heights of ~6.3 nm. Figure 13 and Figure 14 show that, in the “rough” cleave case, the AES peak positions for both the Ga and N peaks were already displaced by $1.71 \pm 0.05 - 1.83 \pm 0.24$ eV prior to metallization. This result indicates that the GaN (01-10) surface bands were bent prior to metal deposition and pinned initially at the same energy as the final energy for the “good” cleaves. For these surfaces, the initial band bending changed only slightly with metallization.

Figure 13 and Figure 14 also include preliminary results for Ag deposition on GaN, albeit only for a “rough” cleave on the (01-10) surface. The observed behavior is very similar to the case of Au on “rough” cleaved GaN. The AES peak features again are initially at the 1.7 eV final energy position of the “good” cleave case and remain at this position in the band gap regardless of metal deposition.
Figure 15 illustrates SET work function, based on the movement of the largest onset energy with increasing metal deposition. SET measurements followed each AES peak position determination. The measurements are shown with the initial point of each curve set to zero to allow for relative comparisons eliminating complications due to the applied bias and electron analyzer work function. Preliminary SET values for (-12-10) cleaves displayed large work function changes consistent with increased band bending, but absolute values were complicated by a detector overload. The cleaves on the (01-10) face, however, reveal an increase in the work function from initial cleaved state to final metal state of $0.95 \pm 0.02$ eV in the case of Ag and $1.56 \pm 0.03$ eV for Au. The initial behavior for the Ag work function was observed to have a reproducible $\sim 0.1$ eV decrease with the initial 1 Å metal deposition before increasing to the final value as shown in Figure 15.

Figure 15 - SET work function shifts for each cleave. All curves are offset to the origin [69].
3.4 Discussion

From these observations, it is clear that a variety of behavior can occur during the formation of a Schottky barrier depending on the surface conditions present at the time of contact formation. Figure 16 shows how these results can be interpreted in terms of band bending and electron affinity changes. The Fermi levels for the sample and the analyzer are connected. In the freshly cleaved, ideal situation, the bands would be flat and the Fermi level would be within 0.005 eV of the conduction band as mentioned earlier. As metal is applied and the core levels shift, the associated Schottky barrier height will increase as shown.

Figure 16 - Band diagram demonstrating band-bending measurements as determined by rigid core level shifts [69].
A classical Schottky barrier approach can be used for the ideal surface cleaves. Simple calculations in which the metal work functions are 5.1 eV for Au and 4.3 eV for Ag [77], and UHV-clean and atomically-ordered GaN is assumed to have an electron affinity of 3.5 eV [78] yield values for the expected band bending as $qV_B = \Phi_M - \chi_{\text{GaN}} - (E_C - E_F)_{\text{bulk}} = 1.6$ eV for Au and 0.8 eV for Ag. This value for the electron affinity may include an intrinsic dipolar contribution due to the determination of $\chi$ from the polar (0001) face that may not be present in the electron affinity for the non-polar faces, although we are not aware of such a determination to date. The maximum observed band bending of 1.7 eV for Au was determined by the change in the Ga L$_{3}$M$_{4.5}$M$_{4.5}$ peak energy from its initial to its final average value for a “good” cleave. See Figure 13. This assumes that the bands are initially flat, a condition routinely achieved in III-V compound semiconductors for clean, well-cleaved surfaces in UHV [79]. Thus, the value observed for Au is within 0.1 eV of that expected from the calculations for a classical Schottky barrier.

At the present time, reliable work function measurements are available only for the “rough” (01-10) cleaved surfaces, where the Fermi level appeared to be pinned at a final value independent of metal coverage. The work function was observed to change from the freshly cleaved surface to the metallized surface of $1.56 \pm 0.03$ eV and $0.95 \pm 0.02$ eV for Au and Ag, respectively. The relative work function difference of 0.61 eV observed at these ~20 Å coverages is roughly consistent with the 5.1-4.3 eV = 0.8 eV difference for bulk metal coverages. The decrease in work function within the first monolayer of Ag deposition shown in Figure 15 may be an indication of dipole formation at the Ag-GaN interface.
The band bending measurements obtained on “good” cleave surfaces coupled with the work function measurements provide additional information about surface dipoles. Figure 17 shows that the metal work function $\Phi_M$ must equal band bending $qV_B + (E_C-E_F)_{bulk} + \Delta \Phi + \chi'$, where $\Delta \Phi$ is the work function increase measured via SET where the lowest-energy onset was assumed to determine the secondary electron threshold and $\chi'$ is the electron affinity of the “rough” cleaved surface. For $\Phi_M = 5.1$ eV, $qV_B = 1.71$ eV, and $\Delta \Phi = 1.56$ eV, $\chi' = 1.83$ eV. Since $\chi$ for GaN (0001) is 3.5 eV [78], pinned (01-10) surface must produce a surface dipole that decreases $\chi$ by 1.67 eV. This is consistent with the Ag overlayer as well, given that the measured work functions for Au and Ag on these surfaces differ by almost the same amount as the difference in their work functions (see above).

\begin{figure}[h]
\centering
\includegraphics[width=0.5\textwidth]{band_diagram.png}
\caption{Band diagram showing change in work function due to band bending, $qV_B$, vs. electron affinity, $\chi$ [69].}
\end{figure}
For both ideal and rough cleaves, the AES peak energies stabilized at approximately the same value, regardless of the initial value of the Fermi level. The Fermi level pinning observed for rough (01-10) surfaces suggests the presence of states within the GaN band gap. Other groups have calculated states within the GaN bandgap at similar energies. For example, recent density-functional theory calculations [80] predict the existence of an occupied state at 1.8 eV above the valence band in non-polar GaN, i.e., 3.39-1.8=1.59 eV below the conduction band for a 3.39 eV band gap [81]. This surface state occurs in a specific reconstruction involving one or two monolayers of Ga on the surface [80]. Thus, our preliminary studies showing a pinning level at ~1.7 eV on non-polar GaN are in good agreement with the values obtained theoretically. The presence of such mid-gap states at sufficiently high concentrations could restrict $E_F$ movement for metals with higher work function than Au.

The band bending at flat and rough GaN non-polar surfaces differs significantly from previous GaN(0001) polar GaN studies. Density functional theory indicates that a Ga bilayer can form, pinning the Fermi level at ~1.8 eV above the valence band in polar GaN [80]. Barrier height studies on polar surfaces show a wide range of behavior, depending on surface preparation conditions. For example, Wu and Kahn utilized XPS to measure the Fermi energy position and band bending with gold deposition of GaN(0001) prepared by sputtering and annealing in UHV, finding that the $E_F$ shifted downward 0.5 eV from its initial position ~2.6 eV above the valence band maximum (VBM) [78]. This results in a final $E_F$ position ~2.1 eV above the VBM and ~1.3 eV n-type Schottky barrier height. For chemically-etched and air-exposed GaN(0001), Sporken et. al. used XPS to
determine a Schottky barrier height of 1.15 eV for Au on GaN [71]. Other groups report typical values ranging from 0.8-1.2 eV for various surface treatments and contact formation [19, 82], although one study utilizing low-temperature deposition and I-V measurements reported a Schottky barrier height of 1.88 eV [83]. This range of barriers for Au on GaN(0001) underscore the importance of surface preparation for these polar surfaces and the value of cleaved surface studies. With a known electron affinity for the non-polar face and analyzer work function, a determination of the Fermi level position would yield absolute measurements of the band-bending and work functions. In the future, this cross-sectional micro-AES technique may be used to study a full set of metals on GaN as well as AlGaN. Here the changes in electron affinity versus Al content can be used to identify pinning levels in III-N semiconductors.

3.5 Conclusions

Observations of Schottky barrier formation on non-polar face GaN were measured using both AES measurements of the rigid core level shifts as well as secondary electron threshold measurements of the work function change with metal deposition. Cross-sectional epilayer Schottky barrier studies were performed in UHV to investigate the nature of Schottky barrier formation on GaN. Well-defined band bending for non-polar surfaces was observed revealing Schottky barrier heights for Au on GaN near the maximum for polar surfaces as reported by other groups. Fermi level pinning was also observed at an energy level ~1.7 eV above the valence band maximum. Although the Schottky barrier differences between these non-polar and the previous polar face
measurements could be due either to orientation or cleaved vs. chemical surface treatment, the results shown here demonstrate the usefulness of the micro-AES band bending approach to studying contact formation.
CHAPTER 4.

DEFECTS AND CURRENT COLLAPSE IN ALGaN/GaN HEMT DEVICES

4.1 Introduction

Devices fabricated using GaN have been found to exhibit current droop when subjected to electrical stress. The underlying physical reactions involved in forming Schottky contacts as shown in the previous chapter can be affected greatly by the presence of defects. In particular, defect formation at the interface of the metal and semiconductor may drastically impede the performance of the barrier by creating a lower resistance path for current conduction through the contact in the form of a trap within the band gap or altering the Schottky barrier height through pinning of the Fermi level as seen previously. Fortunately, determinations of these effects can typically be made using electrical measurements, CL measurements, and other analysis techniques sensitive to trap and defect formation.

Current collapse in HEMT devices is not entirely understood. Two main theories have been developed to explain the observed phenomena [84]. First, it is possible that defects formed within the bulk GaN channel region of HEMT devices may be responsible for the trapping of charge and eventual current collapse in the device. Alternatively, defects and traps at the interface can have the same effect on the device. Passivation
tends to neutralize the current collapse and UV light has been shown to successfully depopulate the traps temporarily allowing the I-V characteristics to be restored to near the original level.

This current collapse was investigated in HEMTs grown by the Naval Research Laboratory. These devices exhibited clear current collapse and were stressed at NRL to ensure consistent UV light detrapping and electrical stressing as described in [22]. The devices were analyzed using CL prior to stressing and following stressing. Defects were found to be localized within the GaN channel region at two different energies within the bandgap.

4.2 Experimental

Devices that were known to exhibit current collapse were analyzed in an attempt to determine the cause of the current collapse. Initially, two adjacent devices on sample B10, one stressed and one unstressed, were analyzed. It was found that the differences in the uniformity of the wafer required that the same device be used prior to and post-stressing. Low-temperature CL line scans and monochromatic CL imaging was used to determine the location of particular defects. Electrical stressing was then performed and current collapse was verified to determine the devices did exhibit the typical collapse as seen in other devices. Finally, the devices were examined post-stressing and images were compared to the pre-stress data for the same device. Figure 18 shows a CASINO Monte Carlo simulation for the electron beam excitation vs. depth for devices on sample B10.
4.3 Initial Results (Comparing both devices individually)

The initial results showed differences that seemed to arise from an inconsistency in the sample itself. As shown in Figure 19, the low-temperature CL taken from five different positions in the gate region with a magnification of 20,000x revealed differences in the spectra that varied dramatically with position. The spectra were taken by searching for positions in the drain-gate and gate-source regions where the particular wavelength appeared to have an increase in intensity. For example, the green curve was recorded at a position where the 370 nm, Y4 luminescence appeared to have a maximum intensity.
Due to the thick gate metal, no luminescence was observed directly over the gate contact itself.

Figure 19 - Low-temperature CL scans of sample B10 prior to electrical stressing. Each curve was taken at a magnification of 20,000x at a location exhibiting strong luminescence at the indicated wavelength.

Upon examining the gate region of an unstressed device, similar scans were recorded for a stressed device located adjacent to the previous unstressed device. A similar set of scans as the previous figure is shown in Figure 20 for this adjacent stressed device. Differences in the two devices are difficult to discern due to the variations in the signal levels across the sample. Despite these difficulties, the CL image maps were recorded both pre- and post-stress for the same device at each of the energy peaks resolved in the original scans.
4.4 Further Results (Comparing Pre- and Post-Stress Data)

The results from the pre- and post-stress image mapping are shown in Figure 21. The results for the image maps reveal subtle, yet possibly significant changes between the pre- and post-stress images. Overall, there may be slight increases in the intensity of the individual defect levels and perhaps some new defect centers forming, although no significant changes were detected for any particular energy investigated at 2 keV. The AlGaN NBE consists of a nearly uniform brightness throughout the entire mesa region not covered by either Ohmic or gate contacts. The GaN NBE, on the other hand, appears to increase in intensity on the left side of the image. This was investigated further,
however, and determined to be a result of the electron beam placement on the sample surface for extended periods of time. During various portions of the analysis, the electron beam was focused at particular locations which enhanced the GaN NBE. Thus, these changes in the GaN NBE intensity cannot be used to determine the effects of the electrical stress and current collapse on the overall device luminescence.

Two defect levels were determined to be present in the sample and were studied in detail using the CL image mapping technique. Other groups using photoluminescence (PL), a technique similar to CL where an incident photon beam is used to excite electron-hole pairs, have studied the Y4 and Y7 defect levels. These groups have observed these Y4 and Y7 luminescence features in GaN under various circumstances, but have also not concluded the exact nature of the defects. For example, the Y4 defect luminescence does not occur in samples with stacking faults and only occurs in samples with strong Y7 luminescence [85]. In sample B10, the Y4 defect luminescence appeared strongly at spots in both the pre- and post-stressed device. In addition, new defect formation spots appear to be apparent in the post-stressed sample, for example in the lower left portion of the gate region. The Y7 defect, while appearing in each location pre- and post-stress, does not appear to change as clearly as the Y4 defect level. Also, the defects post-stressing are possibly of higher intensity than the levels pre-stressing and may indicate the enhancement of the defect with stressing. Unfortunately, the instrument conditions may have changed due to the elapsed time period between the pre- and post-stress images resulting in an uncertainty in the absolute levels of luminescence intensity.
Figure 21 - Sample B10 low-temperature CL image maps at set energies pre- and post-electrical stress. The SEM image is at the same location as each of the image maps. The increased luminescence in the GaN NBE image post-stress is due to electron beam effects. Note that the Y4 and Y7 defects that appear in the pre-stress images also appear at the same locations post-stressing along with possible new defect locations as seen in the lower left portions of the Y4 and Y7 post-stress images.
Although the image mapping for the energies studied pre- and post-stressing indicates the possible increase in the number of defect locations as well as stability of the defect in locations that were determined to have a high intensity of luminescence with electrical stressing, it is important to understand the actual location of the defects within the device structure. Depth-dependent CL maps were collected by varying the electron beam voltage to excite luminescence at depths as shown in Figure 18. These maps are shown below in Figure 22. The Y4 defect level on the left and the Y7 defect level on the right both appear to peak in intensity at 10 kV corresponding to a sample depth of approximately 200 nm. This is well into the GaN channel and buffer layer. Only the highest intensity peaks and peaks that are located in the upper regions of the GaN buffer are seen in the 2 kV scans shown in Figure 21. It is important, therefore, to understand the actual cause of the defect levels Y4 and Y7 since it is established that the origins of the luminescence are in the GaN layer and not the surface region.

The Y4 luminescence is thought to be caused by excitons “bound to some point defects trapped by the edge threading dislocations” while the Y7 defect “arises from recombination of an exciton bound to some point defect that is in turn trapped by the stress field of the threading-edge dislocation” [85]. These assignments are possible in the situation of sample B10, although the dislocation density is known to be ~200x higher than the approximate dislocation density as suggested by the appearance of Y4 and Y7 defect luminescence. This can be explained by considering that the point defects are being held by specific threading dislocations and not every dislocation will lead to the accumulation of Y4 and Y7 defects. It is clear, however, from the image maps collected on sample B10 that if the defects are associated with dislocations, the defects responsible
for Y4 luminescence accumulate around different dislocations than the defects responsible for Y7 luminescence.

**Y4 Defect**  
370 nm  
3.35 eV

**Y7 Defect**  
386 nm  
3.21 eV

Figure 22 - Sample B10 depth-dependent CL maps at the same location as in Figure 21 showing the Y4 and Y7 defect levels have the highest intensity at 10 kV excitation.
4.5 Conclusions

The appearance of defects Y4 and Y7 throughout the gate region of sample B10 indicates a possible role of these defects in the current collapse exhibited by this sample with electrical stressing. Previous research by other groups and this study have revealed the two defects appear to be related in some way because of the simultaneous appearance of the Y4 and Y7 defect luminescence, however the CL maps recorded during this investigation show the defects do not accumulate at the same dislocations. The exact role of the defect in the current collapse phenomena is unclear, however it is possible the defect may be trapping charge in the buffer layer and reducing the amount of current transfer with accumulated charge. The depopulating of these traps and subsequent return of the current-handling capability by the device would support this scenario. It is possible the reason the traps do not appear to change significantly with electrical stress is simply that the e-beam penetration into the exact location of the traps efficiently charges them regardless of the prior state of the trap. To conclusively correlate these defects with current collapse, further investigations of devices that do not exhibit current collapse in search of similar Y4 and Y7 defect luminescence or further stressing experiments are necessary. An understanding of the correlation of these traps with sample growth conditions may isolate the exact nature of these traps and the role they play in this or other phenomena.
4.6 Device Fabrication and Defect Analysis Experiments

Knowledge of surface chemistry effects on final device performance is essential to device and process engineers. The role various defects have on device characteristics allows for both appropriate controls of surface conditions to assure high yield and also provides a better understanding of how to successfully develop novel device processing procedures.

To extend our understanding of these basic relationships in the context of HEMT devices, a novel UHV mask was developed and qualified on Si, GaAs, and sapphire to allow for novel processing within a clean, UHV environment where surface cleaning and preparation could be performed without typical contamination issues when processing at atmosphere. Sample C11, an AlGaN/GaN HEMT structure grown on SiC, was processed with this mask and HEMT devices have been demonstrated that yield high frequency performance as well as variations in this performance with the processing methods chosen. In processing and analyzing this sample, however, it was noticed that the Ohmic contacts used, Ti/Al/Ni/Au, resulted in a specific localization of a particular defect around the Ohmic contacts as determined by CL analysis. To investigate this effect isolating the specific cause of the luminescence as well as to gain insight into the effect of the RIE etch on device performance, a new AlGaN/GaN on SiC sample, named sample F01, was processed with four different Ohmic metal types including Ti/Al/Ni/Au. A standard process without the new dual-layer mask was utilized and half of the sample was subjected to an RIE etch to reproduce the etch conditions of sample C11. Correlations with final HEMT and Ohmic device performance were found which will be discussed in Chapter 6. Finally, a bulk GaN sample, name sample G01, was processed with
Ti/Al/Ni/Au Ohmic contacts to determine the role of the substrate, i.e. AlGaN/GaN HEMT structures vs. bulk GaN, on the appearance of this particular defect as detected by CL.
CHAPTER 5.

ALGAN/GAN/SIC HEMT DEVICE SURFACE TREATMENT OF SCHOTTKY CONTACT GATE REGIONS

5.1 Introduction

Many experiments have been performed to determine the best way to produce clean GaN and AlGaN. Many procedures produce clean surfaces as determined by various surface analysis techniques, but only limited experiments have attempted to determine the effects of surface processing on final device performance. An understanding of the correlations between surface treatments, AES measurements, CL spectra, and electrical measurements is extremely powerful in creating state-of-the-art devices. Through an understanding of the underlying physical processes involved in improving or degrading the device performance, optimizations can be made to engineer better performing and more reliable devices.

Through the use of a dual-layer mask, HEMT devices were fabricated that could be processed in UHV, an extremely clean environment where normal surface contamination problems are minimized. Immediately after processing, the gates were deposited in UHV to eliminate any air exposure of the clean gate region.

Four samples were investigated in detail. The three types of cleaning procedures performed were a simple thermal anneal, a Ga-reflux method shown to result in clean.
GaN surfaces, and N\textsubscript{2} ion sputtering to remove contamination. Having worked out the gate metal lift-off using test samples, I fabricated the devices accordingly. The processing was found to result in lower device yield despite good surface quality as determined by AES and CL measurements and the improved cutoff frequency after a careful examination of the electrical characteristics to determine which devices functioned properly throughout device testing.

5.2 Experimental

5.2.1 Double-layer Mask Details and Importance

To study the effects of various surface treatments on device performance, a mask capable of being placed in vacuum without compromising the delicate UHV environment needed to be developed. Dr. Gregg Jessen outlined the basic design principles and his work at developing a mask for this purpose as outlined in his thesis under Chapter 8, “AT06 AlGaN/GaN HEMTs for Attempted RF Characterization” [26]. The basic design presented in [26] was used with significant optimizations made in the undercut profile and a series of experiments designed to qualify the mask for actual device fabrication. Through these tests, I determined that the Si\textsubscript{3}N\textsubscript{4}/SiO\textsubscript{2} mask alone would not allow good lift-off of the standard Ni/Au gate metal even with 800 nm undercut verifying the similar result found by Dr. Gregg Jessen. Eventually, I developed a solution to the problem by wet chemical pre-etching the SiO\textsubscript{2} prior to lift-off to promote good lift-off of the metal overlayers.
The final bottom layer thickness of Si₃N₄ chosen for the dual-layer mask was 4000 Å, more than twice the final thickness of any metal deposition that would be evaporated on the samples. This ensures that two design criteria will be maintained: the metal that is deposited will not come into contact with the sidewalls of the upper mask layer preventing lift-off and the metal layer will adhere to the underlying semiconductor with a minimal amount of adhesive from the tape contacting the surface in large, open areas of metal.

The upper layer thickness of SiO₂ chosen in my mask design was 2000 Å. This allows for the stability necessary with up to 800 nm undercut while still allowing the mask formation to be performed in a reasonable length of time.

5.2.1.1 Etching Design

The mask is fabricated in two steps to allow for good feature formation in the upper mask layer with the anisotropic F-23 etch while allowing the lower layer to be undercut with the F-14 isotropic etch. In addition to the chemistry and nature of the etching chosen in the two steps, the DC bias and power are reduced to the minimal levels during the second stage of etching to ensure the RIE etch necessary to create the sample mask imparts minimal damage to the underlying surface while the etch is in contact with the sample surface. During etching, the DC bias recorded was 75 V and the etch power was stable at 24 W, significantly lower than the 100 W used in the initial upper layer mask etching. The final etch characteristics are shown in Table 3.
<table>
<thead>
<tr>
<th>Etch Step</th>
<th>Chemistry</th>
<th>Characteristic</th>
<th>Power/DC Bias</th>
<th>Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>F-23</td>
<td>Anisotropic – Straight Sidewalls</td>
<td>100 W/ 227 V</td>
<td>35 minutes</td>
</tr>
<tr>
<td>2</td>
<td>F-14</td>
<td>Isotropic – Undercut</td>
<td>24 W/ 77 V</td>
<td>23.5 minutes</td>
</tr>
</tbody>
</table>

Table 3 - Dual-mask RIE etch process detailing the overall time, power, and DC bias for each step.

5.2.1.2 Pictures of Etching Variations

A series of experiments was developed and variations in the power and length of time for the two etch process steps were made until a suitable mask was designed and shown to work properly. To test each step, an SEM with FIB capabilities was utilized to analyze the sample after each etch variation.

Figure 23 - SEM images of undercut for variations in dual-mask structure with F-14 etch times of (A) 5 minutes, (B) 8 minutes, and (C) 12 minutes.

In Figure 23, three variations of the undercut etch were tested. The initial F-23 etch was determined to etch through the upper layer completely and stop short of contacting the actual AlGaN gate layer for the time shown in Table 3. The F-14 isotropic etch, however, was varied for 5, 8, and 12 minutes and the resulting masks resulted in
160, 260 and 480 nm of undercut respectively. While each of these would work as a lift-off mask, it was decided that with the stability afforded by the upper SiO₂ layer, a deeper undercut and resulting aspect ratio could be achieved with a longer etch time.

Figure 24 - SEM images of undercut for final 23.5 minute F-14 etch. As seen, a final 800 nm of undercut was measured on structure A while 700 nm was measured on sample B, a 2 µm alignment bar that has been almost entirely undercut.

In Figure 24, the results for the final 23.5 minute F-14 etch are shown. The structure seen on the surface is residual SF-11 that was left on the test sample during the etch. Figure 24A shows a typical structure with 800 nm undercut revealing the overall profile of the mask. With this mask, even an extremely abnormal evaporation with significant overspray will not wick up the sidewalls and create poor lift-off as long as the metal thickness is kept to less than 4000 Å, the thickness of the lower layer. Figure 24B shows a 2 µm bar that has been nearly completely undercut and demonstrates the structural support of the mask.
Finally, in Figure 25, an actual HEMT device structure is shown with the source, drain, and gate regions composed of the dual-layer mask. The gate region is the most critical component and the insets show both a close-up view of the gate and a cutaway view achieved using a FIB demonstrating the actual profile of the 13.5 minute etch. In the final version of the mask, a 23.5 minute etch was utilized which provides even more undercut than is shown in this figure.
5.2.1.3 Lift-Off Etch Solution

Although the overall design of the mask and the etch details were eventually designed to provide the necessary undercut for metal lift-off, there remained one important aspect of the mask to test: actual lift-off of the metal. Prior to running the actual sample, test samples prepared on GaAs wafers were metallized and lift-off was attempted without success. Inspection of the wafer revealed the metal adhered to the surface of the mask and did not release as expected.

To overcome this obstacle, an etch was used that could undercut the SiO₂ overlayer of the dual-layer mask and allow the gate metallization to lift-off cleanly. Unfortunately, most SiO₂ etches also attack one of the four Ohmic metals in the existing Ohmic pads: Ti, Al, Ni, or Au, with Al being the most easily etched and damaged metal. For example, buffered oxide etch, or BOE, consists typically of about 6:1 NH₄F (40%):HF. This etch is used as a standard etch for SiO₂, but it will attack both Al and Ti and is not suitable for use with a sample having exposed Ohmic contact pads. An alternative suggested by J.J. Gajda of IBM System Products Division utilizes BOE with an additional amount of glycerol substituted for the water [86]. Although this may work well, I did not test this etchant. My approach utilized a (2:1) acetic acid : ammonium fluoride solution.

5.2.2 Sample C11B – Initial Results

After the HEMT devices were fabricated on a test sample C11B and lift-off was performed, the devices were found to give satisfactory RF results. Unfortunately, the lift-
off on the annealed sample was not complete and many devices were not usable. The UHV deposited sample without a pre-anneal did not yield performing devices overall. This result indicates the sample behaved differently when the evaporation was performed in a UHV environment as opposed to a standard HV environment.

Figure 26 - RF performance of AlGaN/GaN HEMT devices for sample C11B. Solid-colored die indicate devices resulting in RF performance. Other die indicate either unusable devices due to poor lift-off (green X’s) or no indication of RF performance (shaded die).

An overview of the RF results is shown in Figure 26. Each solid-colored rectangular region represents a portion of the sample with devices exhibiting RF performance. The shaded die are devices that failed to exhibit RF performance. The marked out regions represent devices that failed because of the lift-off technique and not because of faulty Schottky gate contacts. Considering the processing performed on the samples prior to gate metallization with the RIE damage during the dual mask
fabrication, it is important to note the devices performed in such a manner. The devices metallized in UHV, however, gave results only on the annealed sample and one particular transistor on the unannealed sample. This led to further investigations of the unannealed sample in an attempt to determine the cause of this general failure in device performance.

The different samples were subjected to internal photoemission (IPE) analysis, a technique that allows the determination of the Schottky barrier height, following RF performance testing in an attempt to determine the cause of the difference between the metallizations. These results are shown in Figure 27 below. The Schottky barrier height was found to be higher in the piece that was metallized using a standard metallization chamber. This is consistent with the fact that the devices exhibited RF performance considering a higher Schottky barrier height is an indication of higher Schottky contact quality. From this determination, it is apparent the sample that was metallized in UHV had different surface characteristics. One possible explanation of this is that the surface is more reactive due to the metallization in UHV after the pre-metal HCl etch used in this particular sample. Localized states may have formed at the interface that remained during metallization because a contamination layer could not form during contact deposition when the first monolayers of Ni took form on the surface.
Figure 27 - IPE results for Ni/Au Schottky contacts on the device layer of sample C11B consisting of AlGaN with different processing.

In summary, the initial trial using the modified dual-layer mask are shown in Figure 26 and Figure 27. The portion of the sample deposited using standard metallization techniques resulted in devices with a higher Schottky barrier height than either of the UHV deposition methods and the devices exhibited RF performance. The UHV-deposited portion of the sample without additional annealing resulted in lower gate Schottky barrier heights with the majority of the final devices failing to exhibit RF performance. The UHV annealed and UHV-deposited gates resulted in working devices where the Schottky barrier height of the gates were comparable to the standard process portion. Most importantly, the dual-layer mask was shown to successfully allow gate lift-off resulting in working HEMT devices.
5.2.3 Sample C11C – Effects of Various UHV Surface Treatments on Device Performance

Sample C11C (referred to as sample C11) has the sample structure as indicated in Table 2. CASINO Monte Carlo simulations of the predicted electron penetration depth with varying beam voltage are shown in Figure 28. The actual expected signal contribution reveal that with a maximum electron beam voltage of 5 keV, the entire structure can be analyzed as shown in Figure 29. The sample was initially quartered and three quarters were processed simultaneously through the Ohmic metallization. Two of these three pieces were then processed using the dual-layer mask developed for UHV processing and analysis of the gates with the results of sample C11B discussed in the previous section.

![Figure 28 – CASINO Monte Carlo predicted electron beam penetration into sample C11.](image-url)
Figure 29 – CASINO Monte Carlo simulated electron beam penetration and signal contribution in each layer of sample C11.

As noted previously in Chapter 2, C11 also exhibited time effects with e-beam exposure. In particular, two different processes with different rates occurs. The GaN NBE decreases in intensity with time to a value of nearly $\frac{1}{2}$ the original intensity over a period of 26 minutes. The defect level YL increases in intensity rapidly at first and appears to saturate unlike the GaN NBE. Curve fits to the data revealed an increase in intensity of the GaN NBE with a time constant of 358 seconds. The saturation of the YL, on the other hand, took place with a time constant of 21.7 seconds. Effects from the slowly decaying GaN NBE can be avoided by taking measurements quickly with a minimal amount of setup time. The faster response of the YL, however, is difficult to avoid and should be kept in mind throughout the following data analysis. Most likely,
this will also be partially responsible for scatter in the data since the effects are localized to the electron beam placement and are highly sensitive to the time taken in aligning the electron beam and preparing to record a scan.

The first quarter wafer that was processed, sample C11B, demonstrated the dual-layer process could be used to successfully fabricate working devices. The piece was quartered again after the gate mask development and the three usable pieces were processed using a standard metallization in a typical metal deposition, a standard metallization in the UHV system, and a simple anneal and metallization in UHV. The sample that was processed in a typical metal deposition system resulted in a number of working devices showing the viability of the technique. The UHV-processed samples, however, resulted in an extremely low yield and these processing methods, including the pre-gate metal HCl dip, were not used in subsequent processing.

A second quarter wafer of C11 was processed with an identical dual-layer mask. During one of the analysis steps prior to depositing the Si₃N₄/SiO₂ gate mask, however, a small portion of the sample fractured in the SEM chamber. The remaining piece was cut into three pieces and processed using different surface treatments in UHV: a simple anneal, a Ga-reflux cleaning procedure and anneal, and a N₂ ion beam sputter followed by an anneal. The fourth piece was later retrieved from the SEM and processed using standard photoresist techniques and these device results were compared with the dual-layer mask processing device results.
Figure 30 - Sample C11 wafer map diagram showing the right, center, and left orientations for each processed piece as determined during the sample processing and the process method used on each piece.

Four pieces of sample C11 were processed as shown in Figure 30. The left and right portions of the sample were named during sample mounting in the UHV sample holder and this terminology is reflected throughout the following discussion of results. Finally, the four sample names and associated cleaning procedures are indicated in the figure.

5.2.3.1 Anneal

Annealing is a technique often used to remove contaminants, to repair damage in samples, and to cause reactions to occur including Ohmic contact formation to AlGaN/GaN samples. Sample C11-1 was subjected to a typical 1 minute, ~850°C anneal in UHV prior to metallization.
Figure 31 - AES spectra from the center of sample C11-1 showing the elements detected on the surface prior to and after the UHV anneal. A slight reduction in C and O intensity post-anneal and an increase in N intensity suggest an improved surface post annealing.

As seen in Figure 31, AES spectra of the sample surface reveals a small decrease in C and O with annealing. The N signal intensity increases and the small decrease in other contaminants indicates the anneal modified the sample surface resulting in a slightly improved surface quality. The purpose of the anneal was to remove damage from the RIE mask etch while desorbing contaminants from the surface. The AES of the right and left regions of the sample reveal similar effects, although problems with the AES system resulted in extraneous noise spikes in these spectra. Finally, the upper Au layer is highly visible in the final scan taken after metallization of the gates.
Figure 32 - CL from center portion of Sample C11-1. The black curves indicate the sample condition prior to processing and the red curves post-annealing. Notice the increased blue luminescence (BL) at all sampling depths post-annealing.

As seen in Figure 32, the CL analysis reveals typical GaN NBE at ~3.39 eV, blue luminescence (BL) between 2.6 and 3.1 eV, and YL from 1.4 to 2.6 eV for the sample at room temperature. The origin of the YL band is still uncertain, and researchers have debated many views on the cause of this deep trap defect level [85]. The BL band is
assumed to be due to Zn contamination and transitions from the conduction band or shallow donors to the Zn-related acceptor [85]. The annealing, however, creates an increase in the BL intensity for all sampling depths of the sample. This would indicate the anneal did not improve the sample quality or repair damage from the RIE etching, but rather created additional damage. The low-energy shoulder of the GaN NBE is reduced at all sampling depths, indicating lower impurity exciton emission.

Figure 33 - CL from the left portion of sample C11-1. The reduced GaN NBE near the surface and increased BL throughout the sample indicate damage in the sample with annealing. The reduced YL may, however, indicate a reduction of deep recombination centers.
Figure 33 shows the left portion of sample C11-1. The GaN NBE is reduced in the regions nearest the sample surface indicating possible damage by the anneal. The BL increases similar to the behavior seen in the center portion of the sample and discussed previously. The YL decreases, however, indicating that certain defects within the sample can be repaired through a simple anneal.

Figure 34 - CL for sample C11-1 on the right portion of the sample pre- and post-annealing. The increased AlGaN NBE intensity reveals this portion of the sample was significantly improved by the anneal.
Figure 34 shows similar CL scans taken on the right portion of the sample. These scans indicate two important aspects of the anneal. First, the annealing step dramatically improved this portion of the sample due to the increased AlGaN NBE luminescence intensity. In fact, this is the only time the AlGaN signature was recorded with such intensity on sample C11. At other locations on the sample, the AlGaN NBE recombination was significantly less perhaps as carriers either recombined non-radiatively or were immediately swept out of the region. The GaN NBE, however, is reduced slightly in most of the scans.

A possible explanation for the improved AlGaN signature with this particular anneal is a nonuniformity in the heating provided by the sample block. An investigation of the annealing uniformity revealed a variation between 800-1000°C depending on the portion of the sample block being observed. On C11-2, the pyrometer, using an assumed emissivity, $\varepsilon$, of the sample surface of 0.15, detected a temperature of 860°C on the left, 787°C in the center, and 803°C on the right portions of the sample. The decreased GaN NBE in the left portion of the sample may be due to a possible decomposition of the sample with annealing, particularly if the value of emissivity used results in an observed temperature less than the actual sample temperature. The right portion of the sample exhibited a vast improvement in the AlGaN signature that can be correlated to a lower anneal temperature.

These results demonstrate that a properly adapted and optimized anneal can be used to improve the condition of the sample surface. On the other hand, an anneal that is too high in temperature can damage the sample as seen by CL. The AES spectra revealed an improvement in all cases with the anneal, but the CL is sensitive to the defects within
the sample and can be used to gauge the actual damage regardless of the elemental composition and reduced contamination of the surface layer.

5.2.3.2 Ga Reflux with Combined Anneal

The Ga-reflux method has been shown to be an effective method of cleaning the surfaces of GaN [29, 87]. This technique involves the simultaneous deposition of Ga onto the sample surface held at 800-900°C. The Ga strikes the surface, bonds with some of the contaminants, and leaves the sample surface removing the contaminants in the process. In addition, it is possible the Ga, being a component of GaN and AlGaN, can be incorporated into the lattice and repair some defects, such as Ga vacancies near the sample surface. The anneal allows the Ga to be mobile and all excess Ga should be removed during the processing. In processing the second piece of sample C11, the Ga-reflux method was chosen as an experimental surface treatment for the gate region of the HEMT processing. The Ga flux during this treatment was maintained at ~0.2 Å/sec yielding a total deposition of ~16 Å/min over a total elapsed time of 5 minutes.

To ensure all excess Ga had been thermally desorbed, an additional anneal following the Ga exposure step was performed for 2 minutes at ~900°C. Following each of these anneals, the sample cooled for about one hour prior to performing any CL or AES analysis due to the long cooling time and insulating nature of the heating sample block.

Analysis during the processing within the UHV chamber consisted of combined analysis by CL and AES prior to any processing, post-Ga-reflux, post-additional anneal,
and finally AES after metallization. This analysis leads to variations across the sample that were detected in the final device DC and RF performance and is important to the final understanding of the effects of the Ga-reflux on the sample behavior.

![Graph showing AES spectra of the center of Sample C11-2](image)

**Figure 35** – 2 keV AES spectra of the center of Sample C11-2 showing the effects of the Ga-reflux cleaning and post-anneal on surface contaminants. Note the increased N AES signature and reduced C and O.

Figure 35 shows the AES analysis at each stage of sample processing with Ga-reflux at the center of sample C11-2. As seen in the comparison of the black curve to the other spectra, the Ga-reflux technique decreased the level of C and O while increasing the amount of N at the sample surface. Unfortunately, the single-pass CMA is not extremely sensitive in the higher energy range and the lack of large, open analysis positions due to the gate mask did not allow for significant detection of Ga. With the top layer of the
mask composed of SiO₂ on the surface, the oxygen is not expected to be completely removed. The left region of the sample resulted in similar AES measurements. On the right portion of the sample, however, the Ga-reflux did not appear to affect the sample surface in the same way. As seen in Figure 36, the Ga evaporator did not coat the right-most portions of the sample with as thick a layer as on the center and left. The increase in N and reduction in C and O in the AES spectra is indicative of a cleaner sample surface and following the final anneal, the Ni/Au Schottky contact was deposited.

Figure 36 - Stainless-steel sample used in Ga-deposition testing to determine uniformity and appropriate sample positioning of the sample holder

CL analysis of the Ga-reflux sample during processing shown in Figure 37 revealed an initial typical GaN response with BL and YL as seen in the other C11 samples. Following the Ga-reflux sample cleaning, however, a drastic change in luminescence is observed with an increase in BL to the maximum depth observable. The lower voltage scans to a depth of 1 keV corresponding to the upper AlGaN surface layer reveal a dramatic decrease in luminescence intensity of the GaN NBE. This decrease is
most likely due to damage induced by the Ga-reflux method as well as a masking of GaN signature by possible excess Ga on the surface. The subsequent anneal attempt to remove excess Ga was successful at restoring the GaN NBE to pre-Ga-reflux levels. The anneal, however, allowed the incorporation of the Ga into the sample as evident in the green CL curves. A large band of defect luminescence surrounding the GaN NBE from ~3.0 to 3.94 eV increases in intensity after the anneal corresponding to the Ga introduction into the upper surface layers. This is assumed to originate from both an incorporation of the Al in the AlGaN layer resulting in the defects above the GaN bandedge and a collection of defects due to the incorporation of excess Ga during the anneal into the sample. In addition, the BL clearly increases in intensity throughout the depths of the sample.
Figure 37 - CL analysis of center region of sample C11-2. The black curves show typical C11 signature pre-processing, red curves reveal damage post-Ga-reflux, and green curves show the sample condition post-anneal. Notice the band of new defect luminescence surrounding the GaN NBE at the surface layers both post-Ga deposition and annealing.

Although the CL reveals dramatic changes with Ga-reflux and annealing, the AES measurements do not indicate an incorporation or deposition of contaminants into the surface layers. Following the anneal, the AES indicates similar levels of C, O, and N as were recorded post-Ga-reflux indicating the sample was not further contaminated with the processing. In addition, the Ga signature appears similar in both post-Ga-reflux and
post-anneal AES signifying little change in the amount of Ga on the surface with anneal. Finally, the increase in N AES indicates the Ga-reflux improved the quality of the surface layer since AES is surface sensitive and N Auger electrons originate from the top ~10 Å of the sample as discussed in Chapter 3.

Although the right portion of the sample appeared to result in a similar clean surface chemistry as determined by AES after processing, CL results indicate this portion of the sample was affected least by the Ga-reflux cleaning method. The decrease in GaN NBE intensity was seen throughout the sample depth. In addition, the intensity of YL remains constant despite the processing which may be an indication of the lower amount of Ga exposure expected on this portion of the sample.

Unfortunately, the thickness of the top Au layer of gate metal deposited on this sample was slightly thinner than in the other pieces due to a lack of Au in the crucible during evaporation. The final value of Au deposited was 750 Å compared to the 1000 Å deposited on C11C-1 and C11C-3. This may be a possible explanation in the device failures that will be discussed later.

5.2.3.3 N₂ Ion Sputter and Anneal

The third piece of sample C11 was treated using a N₂ ion sputter cleaning followed by an anneal. The ion sputter sequence used on the sample was somewhat rigorous due to the alignment of the ion beam with the sample block and difficulty in observing the irradiated area. A total time of 22 minutes of ion beam exposure was used to clean the sample over a range of ion beam energies from 1 keV to 3.5 keV. AES
measurements were made on the sample at various intervals to determine the effectiveness of the sputtering at removing C contamination which was used to determine the total time of exposure. Although this amount of aggressive ion sputtering would not be utilized in normal processing of a sample, it is advantageous in that it emphasizes the effects of the ion beam and anneal in both AES and CL results as well as final device performance.

The results of the AES analysis on the center portion of the sample are shown in Figure 38. As can be seen in this figure, the sputter cleaning removed significantly more C and O than either the anneal alone or the Ga-reflux method. The N signature is greatly improved, although prior to annealing the N appears to be split between the lattice-bound N and ion-beam incorporated N as seen by the increased width of the N signature. After annealing, the broadening of the N peak disappears and the intensity of the N peak increases as the excess implanted N is incorporated into the lattice.
Figure 38 - AES from center region of C11-3 showing effects of N$_2$ ion sputtering on sample surface chemistry. The asterisk (*) indicates the N peak spreading with sputtering.

The left portion of the sample shows similar behavior as the center region, although the spreading of the N peak is minimal. The C and O contamination is again reduced and the N intensity increases dramatically. The right portion of the sample appears to be affected much less than the other two portions, however. The AES shown in Figure 39 reveals a similar decrease in C as the left and center portions of the sample. The level of N and O, however, remains nearly the same before and after the annealing and there is no discernable change in the N lineshape. The cause for the ringing associated with the O peak is unclear, although it appears the N-sputtered sample
experienced more charging due to the ion bombardment and implantation in post-sputtering scans.

Figure 39 - AES spectra for the right portion of ion-sputter treated sample C11-3. Notice the decrease in C contamination, but persistence of O as well as the nearly identical level of N pre- and post-sputter and anneal.

CL analysis of the sample reveals changes in the spectra with ion sputter processing. Figure 40 shows the center portion of sample C11-3. Ion sputtering produces a dramatic decrease in the GaN NBE signal for all levels and completely disrupts all radiative recombination processes to a depth of ~10 nm, including the upper AlGaN layers as shown in Figure 29. It is important to note that this disruption in luminescence does not appear to affect the BL which actually increases at the surface while all other luminescence is quenched. Annealing restores the GaN NBE to near pre-
sputtered levels for all depths. It appears the sputter treatment incorporates a large amount of nitrogen from the sputter beam into the sample and thoroughly disrupts the lattice. Annealing the sample restores order to the crystal indicated by the return of the GaN NBE and YL.

Figure 40 - CL analysis of the center piece of sample C11-3. N₂ ion sputtering, shown in red, completely destroys the GaN bandedge and disrupts the YL in the upper layers of the sample to a depth of ~10 nm. Annealing, shown in green, returns the GaN bandedge, BL, and YL to nearly pre-treated sample conditions.
In Figure 41, the right portion of the sample is shown. This region of the sample is significant and warrants discussion due to the nature of the final device performance in which this region of the sample resulted in working HEMT devices. As previously mentioned regarding the AES analysis of the right portion of the sample, the ion sputtering did not appear to affect the N or O levels as drastically as in the other portions. The C was removed and, therefore, the ion beam did strike the surface, but not to the same extent as the left and center. In the right portion of the sample, there is also evidence for disruption of the upper layers of the sample to a depth of ~5 nm unlike the left and center portions of the sample shown previously which were damaged to a depth of ~10 nm. Again, in the ion-damaged region of the sample, the BL increases while the YL decreases. The anneal restores the YL and GaN NBE, however, and increases the BL emission at all energies indicating the mechanism for BL emission is present throughout the sample structure and is triggered by annealing. There is a possibility that Si from the upper mask layers is also being deposited on the sample surface or even driven into the sample by the ion sputter beam and further disrupting or doping the lattice. The AES analysis did not reveal a significant change in Si concentration and the CL analysis did not reveal any particular luminescence that might be correlated to such a phenomena, however.

<table>
<thead>
<tr>
<th>Ion Beam Energy (kV)</th>
<th>Range (Å)</th>
<th>Range Straggle (Å)</th>
<th>Sputter Yield (atoms/ion)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>25</td>
<td>15</td>
<td>3.29</td>
</tr>
<tr>
<td>2</td>
<td>40</td>
<td>25</td>
<td>4.01</td>
</tr>
<tr>
<td>3.5</td>
<td>62</td>
<td>37</td>
<td>4.31</td>
</tr>
</tbody>
</table>

Table 4 – Range, range straggle, and sputter yield for varying N ion beam energies as calculated using TRIM simulations for an incident ion beam at 45° to the sample surface, the approximate angle of incidence for the ion beam on sample C11.
In the CL spectra, evidence for the disruption of the upper layers of the sample to a depth of \(~10\) nm is supported by the lack of GaN NBE emission. As seen in Table 4, TRIM calculations [88, 89] predict the maximum range of the ions on sample C11-3 to be 62 Å with 37 Å straggle. The simulation included a 45° ion beam angle of incidence since this is the approximate angle of incidence for the ion gun column to the sample. The damage as indicated by CL agrees with this simulation result well since it is localized to this approximate upper layer. By the Monte Carlo simulations of the electron penetration depth discussed previously, the peak of the penetration curve for a 2 kV electron beam, the depth of damage in the center and left portions of the sample, occurs at \(~75\) Å.

In summary, some plots of the three major elements found at the surface of sample C11 are shown in Figure 42. The assumption that the amount of contamination prior to processing is the same in all three samples allows the initial point to be normalized to 1. The values were determined from the center analysis position of each sample where the difference in the peak-to-valley was used without any further corrections by sensitivity factors since direct comparison reveals the effectiveness of each cleaning process. The process step shown in all three process methods are as follows:

Anneal: 1. Pre-scan, 2. Post anneal


Ion-sputter: 1. Pre-scan, 2. Post ion sputter, 3. Post anneal
Figure 41 - CL spectra for the right portion of sample C11-3. N$_2$ ion sputter damage is localized to the upper ~5 nm of the sample surface (red curve) and is restored with annealing (green curve).
Figure 42 - Contamination removal from sample C11 as determined by AES measurements of the center of each piece. The initial point of each scan has been normalized to 1 for comparison. (A) Carbon, (B) Nitrogen, (C) Oxygen. Overall, N$_2$ ion sputter cleaning was the most effective method to remove C and O while increasing N.
As seen in the previous figure, the amount of contamination by C is most effectively removed through the ion sputter cleaning method although both the simple anneal and Ga-reflux with anneal result in some amount of contamination removal. The amount of increase in N as detected by AES, assumed to reflect the quality of the AlGaN surface, is similar in both the Ga-reflux and ion sputter treated samples. The simple anneal does not appear to improve the quality of the sample surface to the level of the other two techniques. Finally, the amount of oxygen detected on the sample surface, which includes the SiO₂ mask, is reduced to a similar level for both the Ga-reflux and ion sputtered samples. Overall, the N₂ ion sputtered sample with anneal appears to be the most improved and would be expected to result in the best performing devices as determined by AES.

5.3 Results and Correlations

5.3.1 Electrical Measurements and Response

To fully understand the effects of the different processing methods on the final device performance, a thorough investigation was made of the electrical responses from the four pieces. DC and RF measurements were recorded and the analysis indicates fundamental changes in the device characteristics with processing. In particular, the PECVD deposition of the mask and subsequent RIE etching of the gate region affected the Schottky barrier formation and gate leakage characteristics, although the cut-off
frequency and maximum frequency of oscillation would still be maintained to a level nearing that observed using standard processing techniques.

5.3.1.1 Frequency Response $f_T$ and $f_{max}$

The ultimate goal of cleaning the surface layers of the C11 devices was to fabricate high-speed devices with improved electrical performance compared to standard process devices. To this end, the data shown in Figure 43 is a plot of the cut-off frequency or average unity current gain frequency as given by Equation 13 [90, 91].

![Figure 43 - $f_T$ @ $g_{m_{peak}}$ in GHz for sample C11 showing all HEMT devices measured demonstrating the improved performance of the annealed sample and the poor performance of the N$_2$ sputter and Ga-reflux treated samples. The standard process sample performed consistently well.](image)
The figure shows that a number of the HEMT devices did operate at frequencies above 3 GHz. The devices processed using standard gate fabrication techniques, i.e. SF-11/1805 resist and standard e-beam metal evaporation, showed overall better response with an average $f_T=4.15\pm0.84$ GHz. The annealed sample had a frequency response of $4.02\pm1.17$ GHz showing the nearly identical performance of the annealed sample with the standard process sample. The ion-beam sputtered and annealed sample gave a response of $1.55\pm0.77$ GHz, significantly lower than the other two samples, mostly due to the poor response of the majority of devices. The Ga-reflux and annealed sample had an $f_T$ of $2.07\pm1.24$ GHz. This sample, however, only had two significant, working devices that pulled the average up for the sample which will be discussed later.

A similar measurement of the maximum oscillation frequency is shown in Figure 44 below. The equation defining $f_{\text{max}}$ is given in Equation 14 [92]. It is clear that the $f_{\text{max}}$ is dependent on both the cut-off frequency, $f_T$, discussed previously and the parasitic gate resistance and gate-drain capacitance. To increase the maximum frequency of oscillation, it is necessary to either increase the $f_T$ of the device or to decrease the gate resistance and capacitance, for example by reducing the gate width. As can be seen in this figure, the majority of devices perform at less than 1 GHz due to a variety of reasons. In particular, devices near the edge of the wafer did not perform well because of non-uniformities in the developing of the 1800-series mask resulting in a majority of devices failing to develop entirely when subjected to the RIE mask etch. This is particularly true on the right and left edges, namely columns 2 and 7.
Figure 44 - F_{\text{Max}} [MAG] @ g_{m-peak} in GHz for sample C11 showing all HEMT devices measured. As in the ft measurements, the standard process had the highest yield and uniform response while the N\textsubscript{2} sputter and Ga reflux samples appear to have poor performance.

\[
f_{\text{max}} = \frac{f_t}{\sqrt{8\pi R_C C_{gds,t}}}
\]  

(14)

The particular f_{\text{max}} plotted in Figure 44 refers to the maximum available gain at the peak g_{m}. This ensures an appropriate bias is applied to the transistor and that the stability of the device in operation is obtained [93]. The standard process devices considering all working devices showed f_{\text{max}} values of 5.89±1.15 GHz. The annealed sample performed nearly as well with f_{\text{max}} of 5.38±1.63 GHz followed by the ion
annealed sample of 4.36±1.44 GHz. Finally, the Ga-reflux sample exhibited the lowest 
$f_{\text{max}}$ value of 3.34±1.81 GHz.

In evaluating the frequency performance, some of the devices were found to 
respond poorly in certain DC tests as will be discussed in further detail later. To 
eliminate error in the above calculations of the average frequency response, the devices 
were analyzed using four tests and when only devices that were able to perform well in 
three of the four tests were considered, consistent results revealing the effects of the 
cleaning processes on cutoff frequency were obtained as will be discussed further below. 
Figure 45 shows the annealed portion of sample C11 where the four test results are 
shown in the left map. In the right map, the devices that passed three of the four tests are 
shown which demonstrates the resulting devices contributing to the final average cut-off 
frequency value for the annealed portion of the sample.

Figure 45 - Annealed portion of sample C11 demonstrating the results of transistor tests 
analyzed to determine the final contribution to the cut-off frequency average. Red blocks 
indicate good $I_{gs}$-$V_{gs}$ response, green blocks indicate good $I_{ds}$-$V_{ds}$ FET family of curves 
with pinch-off, dark blue blocks indicate good transconductance performance, $g_m$, and 
yellow blocks indicate good current gain $|h_{21}|^2$ curves. The final devices passing three of 
the four tests are shown in the right in light blue.
The final devices contributing to the frequency performance calculations for the entire sample are shown in Figure 46. The standard process devices were only tested for three of the characteristics since \( I_{gs} - V_{gs} \) Schottky gate curves were not recorded. These devices were still required to pass three tests, however, and it was found that the devices near 0407 failed to exhibit pinch-off resulting in those devices being removed from consideration.

![Figure 46](image)

Figure 46 - Sample C11 showing final resulting devices passing three of the four tests in color and the assumed approximate position of the sputter and Ga beam used during processing.

The final values for the cut-off frequency shown in Figure 47 indicate specific trends not seen in Figure 43. For example, after removing devices not passing three of the four tests, it becomes clear that the Si\(_3\)N\(_4\)/SiO\(_2\) mask processing devices actually performed better than the standard process devices despite being exposed to an additional RIE etch. The N\(_2\) ion sputtered sample exhibited a range of values from 2.2 to 9.2 GHz.
with the highest frequency transistors located the farthest from the sputtered region. This indicates the sputter cleaning as well as the Ga-reflux sample may produce the best devices with a full process optimization. The right portion of the annealed sample which indicated an AlGaN NBE in Figure 34 shows good yield, although the cutoff frequency for these devices is slightly lower than the average for the piece. This could indicate that the other portions of the sample rapidly sweep carriers out of the AlGaN layer explaining why the GaN NBE is intense while the AlGaN NBE is extremely weak in most of the CL spectra recorded for sample C11.

Figure 47 - Cut-off frequency values for sample C11 using only the devices determined as passing three of the four tests discussed previously. The processed samples consistently performed with higher $f_T$ than the standard process sample. In addition, the N$_2$ ion sputter cleaned sample performs better at the outer edge as shown by the red arrow indicating possible damage due to sputtering too intensively in the inner portions of the sample destroying the AlGaN device layer and 2-DEG.
Through analyzing the frequency response of the devices, it becomes clear that the devices are capable of operating as HEMT transistors through all four types of processing situations. The standard process and the annealed samples show the most promise for high yields of working high-speed transistors. The significance of these results is apparent when a consideration of the actual processing steps employed is taken into account. The standard process devices were expected to perform well since the processing techniques used have been shown to produce devices on other material capable of frequency responses in excess of 10x the response obtained using substrate C11 [90, 94, 95]. The results from the dual-layer mask processed samples are promising, however. With a simple anneal, the devices can be made to perform on average with a 3% reduction in $f_T$ or 9% reduction in the $f_{max}$ when all devices are considered and actually perform with an increase of ~50% in $f_T$ when devices not performing properly are removed from consideration as shown in Figure 47. Additional processing steps employed appeared to have resulted in damaged devices and low yield, although these initial results indicate the potential for using the dual-layer mask in future processing remains a viable and promising area of research with appropriate optimizations.

5.3.1.2 Schottky Diode Analysis

An investigation into the actual device performance with respect to the Schottky gate formation will aid in the understanding of these high frequency results. Figure 48 shows an overview of the Schottky performance of sample C11. The map clearly demonstrates differences in the gate-source voltage, $V_{gs}$, to achieve a gate-source current,
I_{gs}, of 2 mA/mm depending on the processing performed to each piece. The standard process sample required the highest V_{gs}, on average 1.46±0.15 V, to conduct the required amount of current. All the other samples were at least 0.4 V lower than this standard with the annealed sample showing an average of 1.09±0.26 V. The N\textsubscript{2} ion sputtered sample resulted in an average of 1.26±0.25 V and the Ga-reflux sample had the lowest value of 1.06±0.29 V. This demonstrates the sample damage caused in processing the gate mask and a possible variation in the Schottky behavior due to the position of the device on the wafer.

![Diagram showing V_{gs} values for different samples and die positions](image)

Figure 48 - Forward V_{gs} for I_{gs} = 2mA/mm of sample C11. The RIE-exposed portions of the sample fabricated using the dual-layer mask exhibit lower V_{gs} at this current.
The forward $V_{gs}$ data shows the standard process sample produces Schottky diodes requiring a higher applied bias for the same current flow compared to all the dual-layer mask samples. This indicates poorer Schottky contact behavior in the latter samples since identical Ohmic contacts were used throughout the wafer. To understand the underlying process behind such a response, it is necessary to examine the actual I-V characteristics for the Schottky diodes.

In Figure 49, the diode curves for all the devices recorded are shown. Some devices near the periphery of the samples did not result in working diodes for various reasons and do not exhibit diode behavior. The N$_2$ ion sputtered sample performed erratically possibly indicating a premature failure of some devices during testing. Most notable, however, is the behavior of the Ga-reflux sample shown by the green curves. The reverse current through the diode is nearly 100x greater than in the other processes and most likely accounts for the catastrophic failure of nearly all the devices tested. This will be discussed in further detail in the following section.
Figure 49 - $I_{gs}$-$V_{gs}$ Schottky diode curves for samples C11-1, C11-2, and C11-3. The Ga-reflux treated sample exhibits significantly higher reverse currents and a possible second Schottky barrier compared to devices processed with an anneal and N$_2$ ion sputter.

Figure 50 shows typical $I_{gs}$-$V_{gs}$ curves for the various devices across the three dual-layer processed samples. From these curves, the values in Figure 48 can be obtained by observing the gate voltage necessary to achieve a gate-source current of 2 mA/mm. Immediately noticeable is the different shape of the curves and the corresponding difference in response based on this shape. In particular, all three curves appear to have a series resistance onset region at ~0.5 V that can be attributed to a series resistance dominating the current flow. This onset of the series resistance dominant current flow appears essentially the same for devices processed using a pre-gate anneal and for the N$_2$-ion sputter cleaning technique, but appears different in the case of the Ga-reflux device.
For my particular sample, the theoretical value of $A^*$ required to analyze the Schottky barrier heights was calculated in a manner described by Qiao et. al [96]. A linear interpolation of the effective mass based on $m^* = 0.20\ m_0$ for GaN and $m^* = 0.40\ m_0$ for AlN [81] was performed and the Al concentration of sample C11 is $x = 21\%$ resulting in a final value of $A^* = 29.08\ \text{A cm}^{-2}\ \text{K}^{-2}$.

As can be seen in Figure 51, the typical Norde plot results in a clear minimum from which a simple polynomial fit can be made and the necessary values of the minimum current, $I_0$, minimum voltage, $V_0$, and $F(V_0)$ can be found. In some cases, such as devices 0515 and 0516 shown, a second minimum appeared to form. The first
minimum was used in the initial evaluation and was interpreted as the dominant feature of the curve.

Figure 51 - Norde F(V) plots demonstrating parameter extraction for sample C11.

Plots of the Norde-extracted Schottky barrier heights are shown in Figure 52. The annealed and the N$_2$ ion sputtered samples both exhibit similar Schottky barrier heights of 0.732±0.006 and 0.739±0.015 eV, respectively. The Ga-reflux sample, however, was significantly lower with an extracted Schottky barrier height of 0.573±0.007 eV.
Simultaneously, the series resistance, $R_s$, was extracted from the data and is shown in Figure 53. In observing the ion sputtered sample, a clear degradation in the series resistance is observed from the outer edge of the sample, device 0317, to the inner region of the sample, device 0313. This degradation most likely correlates with the non-uniform ion beam coverage experienced by the sample during processing. Due to the geometry of the ion gun in the metallization and analysis chamber, it is assumed that the majority of the ions would strike the surface near to device 0211. In these circumstances, more damage would occur in this region with the possibility of a complete sputtering of the device layers. This is consistent with the results shown in Figure 43, for example, since the devices in this region did not exhibit typical frequency response. Also, the Ga-
reflux sample does not appear to exhibit typical series resistance values for working devices such as found in the annealed sample.

![Diagram showing series resistance values](image)

Figure 53 - Norde-extracted Series Resistance, $R_s$, in Ohms for sample C11. The Ga-reflux and N$_2$ sputtered samples exhibit abnormally high $R_s$ corresponding to devices with poor performance.

An alternate method of finding the series resistance and ideality factor from the I-V curves is to use the equations discussed previously in Chapter 2 in conjunction with a plot of ln(I/(1-exp(-qV/kT))) vs. V. In such a situation, the ideality factor can be calculated from the slope of the resulting line. The Schottky barrier height can be found using Equation 4 by solving for $\Phi_b$ at $J_0$ where $J_0$ is the y-intercept at V=0 V. An example of this is shown in Figure 54. The diode I-V curve is also well-behaved even...
through the reverse bias region of the plot indicating the equations accurately model the Schottky barrier until series resistance dominates the I-V curve.

![Graph showing diode I-V curve with linear region and parameters](image)

Figure 54 - Diode I-V curve for device 0515 of the annealed sample C11-1 showing the linear region for parameter extraction.

A summary of the Schottky barrier heights obtained using the diode I-V curves is shown in Figure 55. The Schottky barrier heights obtained using this technique were consistently ~0.6 eV lower than the values obtained using the modified Norde technique, although the analysis does not take into account series resistance that also affects the curves. The annealed sample gave Schottky barrier heights on average of 0.658±0.006 eV while the ion-sputtered sample had comparable Schottky barriers of 0.653±0.009 eV. Finally, the Ga-reflux sample Schottky barrier heights were consistently lower with an
average value of 0.544±0.006 eV. The overall quality of the Ga-reflux Schottky contacts consistently perform poorer than the Schottky contacts for the other two processing methods.

Figure 55 - Schottky Barrier Height (SBH) determined using I-V curve data for sample C11. The general trends agree with the values obtained using the Norde analysis as shown in Figure 52.

Finally, the extracted ideality factors for sample C11 are shown in Figure 56. Values near 1 are preferred since this indicates Schottky diodes exhibiting thermionic emission as discussed previously. The annealed sample and the ion-sputtered sample both exhibit reasonable ideality factors of 1.235±0.012 and 1.306±0.029, respectively. The Ga-reflux method again demonstrates poor diode behavior with an ideality factor on average of 2.834±0.140. Such a large ideality factor is suspicious since it is expected that
a diode will result in ideality factors between 1 and 2 under normal situations of current transport as discussed previously.

Figure 56 - Ideality factors for Schottky diodes of sample C11 obtained using I-V curve analysis. Ideality factors near 1 indicating thermionic emission are preferred.

As previously noted, the Ga-reflux sample behaves in a different manner from the other two cleaning procedures and appears to have no “good” Schottky barriers or low series resistances as indicated by column 6 in the previous four sample characteristic maps. During testing, this sample also behaved differently with nearly every device catastrophically failing during the DC-RF measurements. An example of this is shown in Figure 57 for device 0615 from the Ga-reflux treated sample.
Figure 57 – Photo of Device 0615 from the Ga-reflux treated sample after DC-RF testing. The catastrophic failure destroyed the drain contact and may be due to excess current conduction through the device.

To understand the cause of both the catastrophic failure of the device and the poor performance of the Ga-reflux sample, a closer examination will need to be made of the $I_{gs}$-$V_{gs}$ curves presented in Figure 49 and Figure 50. As discussed previously, the Norde analysis revealed extremely high apparent series resistance in the Schottky gates from this sample. Figure 58 shows the Norde plots for samples 0515 and 0615 on the annealed and Ga-reflux samples. Although it appears there may be a second peak at about 0.8 V bias in the annealed sample, there are clearly two minima in the Ga-reflux situation. Calculating the series resistance of the 1st analysis point reveals an extremely high value of $\sim 1.5 \, \text{M} \Omega$. The Schottky barrier height from this minimum, however, is extremely low at $\sim 0.568 \, \text{eV}$ or $0.545 \, \text{eV}$ from direct I-V plot analysis. The 2nd analysis point indicated
on the Norde plot reveals an extremely low series resistance of 34.0 Ω and a Schottky barrier height of 0.801 eV by Norde analysis.

![Norde analysis plot](image)

Figure 58 - Norde analysis using Equation 8 showing a comparison between the annealed and Ga-reflux C11 samples. Note the two distinct minima in the Ga-reflux device as indicated.

5.3.1.3 Double-Schottky Barrier Analysis

From the Norde data analysis and I-V curve shape, a dual Schottky barrier was detected in this particular sample, but only an in-depth analysis of the I-V curves can accurately determine the parameters of both Schottky barriers in the diode. Figure 59 shows the actual data from device 0615 in black. The red curve is a calculated current based on the equation $I = I_0 \exp(qV/nkT)$ where $n=2.705$ from the previous I-V analysis and the I-V data determined Schottky barrier height of 0.545 eV was used. To correctly
model the low-voltage, bias-dependent portion of the curve, it was necessary to incorporate \((1 - \exp(-qV/nkT))\) as indicated by the green curve.

![Schottky diode I-V curve from device 0615 with and without the calculated bias dependence.](image)

Figure 59 - Schottky diode I-V curve from device 0615 with and without the calculated bias dependence.

After modeling the first barrier height, the difference between the actual data and the theoretical curve allows for a determination of the second barrier. The series dependence, however, determines the deviation of the first curve from a linear plot at high currents and must be included in the model as well. The Norde predicted value of \(1.5 \text{ M} \Omega\) was initially used as a starting point, but it was clear the value was unphysical and did not model the diode correctly. A value of \(5 \text{k} \Omega\) was chosen and this is shown in Figure 60.
Assuming the theoretical Schottky barrier model determined in the previous steps, the resulting difference of the experimental data and the theoretical curve result in a linear region where a second Schottky barrier can be calculated. This difference curve is shown in Figure 61. A resulting Schottky barrier height of 0.713 eV was determined and an ideality factor of 1.18 was calculated along with a series resistance of 34.0 Ω as determined from the previous Norde analysis.
Figure 61 - I-V curve difference of experimental and theoretical data with lower barrier removed. The linear region and linear fit parameters are shown for the second Schottky barrier height.

The resulting combined data is shown in Figure 62. It is clear that the model predicts two, independent Schottky barriers in the Ga-reflux treated sample.

Figure 62 - Double-barrier model plotted simultaneously with the actual data for diode 0615.
As seen in Figure 63 using Equation 10, it is clear that the series resistance determined by the Norde analysis of 1.5 MΩ clearly results in a poor fit of the actual data due to the early onset of the high series resistance of the current and the chosen 5 kΩ series resistance is a more reasonable value. The occurrence of the Norde minimum at low bias voltages makes the Norde series resistance extraction for the lower Schottky barrier difficult. The second minimum in the Norde plot does appear to correctly predict the series resistance for the second barrier, however. Based on this investigation, it appears the Ga-reflux samples exhibit two Schottky barriers: a higher barrier similar to
the annealed and ion-sputtered samples at about 0.7 eV with a lower ideality factor of 1.2 and a lower barrier at 0.545 eV with a high ideality factor of 2.7.

As an alternative investigation, the I-V curves for all the diodes shown in row 6 in blue on Figure 55 were curve fit using a least-squares fitting routine of Equation 10 to extract the values of the parameters. It was found that fitting to the series resistance produced values of series resistance ~10x higher for the first barrier compared to the second. When constraining the series resistance to the fractional part of the area and the material resistance, the fractional part was found to be modeled most closely with equal areas and approximately equal series resistances.

<table>
<thead>
<tr>
<th></th>
<th>Device 0610</th>
<th>Device 0611</th>
<th>Device 0612</th>
<th>Device 0613</th>
<th>Device 0614</th>
<th>Device 0615</th>
<th>Device 0616</th>
</tr>
</thead>
<tbody>
<tr>
<td>rs1 (fit)</td>
<td>362.7</td>
<td>74.5</td>
<td>285.9</td>
<td>227.7</td>
<td>268.0</td>
<td>292.6</td>
<td>345.4</td>
</tr>
<tr>
<td>rs2 (fit)</td>
<td>126.6</td>
<td>228.9</td>
<td>61.6</td>
<td>41.0</td>
<td>32.6</td>
<td>28.2</td>
<td>72.7</td>
</tr>
<tr>
<td>fp</td>
<td>0.79</td>
<td>0.63</td>
<td>0.50</td>
<td>0.49</td>
<td>0.51</td>
<td>0.49</td>
<td>0.50</td>
</tr>
<tr>
<td>rs1 (calc)</td>
<td>36.6</td>
<td>114.6</td>
<td>70.3</td>
<td>54.7</td>
<td>31.5</td>
<td>29.1</td>
<td>72.4</td>
</tr>
<tr>
<td>rs2 (calc)</td>
<td>138.8</td>
<td>196.2</td>
<td>70.4</td>
<td>51.9</td>
<td>32.5</td>
<td>27.7</td>
<td>71.8</td>
</tr>
</tbody>
</table>

Table 5 - Least square fitting results of diodes in row 6 using two methods: fitting to the series resistances and fitting to the material resistance and fractional part with calculated series resistances. The highlighted rs2 values indicate necessary refinements in the model are necessary to accurately extract the series resistance from the curve fits.

In all cases, constraining the series resistance to the fractional part and material resistance results in rs2 matching the value of the unconstrained rs2 while rs1 is forced to an unusually low value of series resistance which becomes evident at higher currents where the lower barrier becomes dominant. This indicates the need for a more advanced model or the consideration of interface charges not taken into account using a simplified double-Schottky barrier model.
The average saturation currents, average ideality factors, and average Schottky barrier heights for the two curve fit techniques are shown in Table 6. Although the series resistances used in both methods varies and the area used in the calculation of the series resistance fit curves is the total area for each Schottky barrier portion, the final results agree in that the lower Schottky barrier height is ~0.5 eV with an ideality factor of ~2.7 and the higher Schottky barrier height is ~0.7 eV with an ideality factor ~1.2. This higher Schottky barrier region models the expected thermionic emission due to the deposited Ni/Au gate contacts and shown in Figure 55 for the other two process methods.

<table>
<thead>
<tr>
<th></th>
<th>Series resistance fit curves</th>
<th>Material resistance and fractional part fit curves</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{sat,1}$</td>
<td>$5.98 \times 10^{-9} \pm 1.03 \times 10^{-9}$ A</td>
<td>$5.82 \times 10^{-9} \pm 0.96 \times 10^{-9}$ A</td>
</tr>
<tr>
<td>$I_{sat,2}$</td>
<td>$7.31 \times 10^{-12} \pm 4.46 \times 10^{-12}$ A</td>
<td>$2.80 \times 10^{-12} \pm 1.58 \times 10^{-12}$ A</td>
</tr>
<tr>
<td>$n_1$</td>
<td>$2.69 \pm 0.11$</td>
<td>$2.67 \pm 0.13$</td>
</tr>
<tr>
<td>$n_2$</td>
<td>$1.20 \pm 0.01$</td>
<td>$1.17 \pm 0.05$</td>
</tr>
<tr>
<td>SBH$_1$</td>
<td>$0.546 \pm 0.006$ eV</td>
<td>$0.531 \pm 0.006$ eV</td>
</tr>
<tr>
<td>SBH$_2$</td>
<td>$0.747 \pm 0.018$ eV</td>
<td>$0.742 \pm 0.014$ eV</td>
</tr>
</tbody>
</table>

Table 6 - Average values for the saturation currents, ideality factors, and Schottky barrier heights using the series resistance fit and material resistance/fractional part of the area curve fitting methods.

The typical association of low-current behavior with an ideality factor of 2 to generation-recombination should also be considered. First, the ratio of recombination current to thermionic emission can be written as Equation 15 [12]. This equation indicates that the recombination current will increase with increasing depletion width, W, common in lightly doped semiconductors. The Ga interstitial in GaN is known to behave as a donor [85]. Considering this along with the behavior of the other diodes and the temperature of the measurements, it is not likely that this lower barrier is due to
recombination. However, if the minority carrier lifetime in the depletion region is decreased significantly, it is possible a contribution could be detected. To fully understand the role of recombination in the Ga-reflux sample, temperature-dependent I-V data would need to be collected and analyzed.

$$\frac{I_{r0}}{I_0} = \frac{q\eta_r}{A'T^2} \left( \frac{W}{2\tau_0} \right) \text{Exp} \left[ \frac{\phi_m}{kT} \right]$$  \hspace{1cm} (15)

The lower Schottky barrier exhibited only in the Ga-reflux treated sample indicates a difficulty in using this treatment to clean the surface of AlGaN samples in device fabrication. Although the surface treatment may effectively remove contamination, the unreconstructed surface is another indication of the poor crystal quality resulting from this particular cleaning method [29, 87]. The CL results discussed previously indicate the surface region is damaged and contains many defects including a degradation of the top AlGaN layer. The Ga most likely creates patches of lower Schottky barrier contact between the Ni/Au and AlGaN resulting in a poor Schottky barrier with excess current flow both in forward and reverse bias conditions. This most likely explains the resulting catastrophic failure of the devices at the source contact region during the higher biasing necessary for frequency response RF measurements due to the higher power levels compared to the current flow in the annealed and ion-treated samples.

5.3.1.4 FET Family of Curves

An important consideration in the final device performance of any FET transistor is the $I_{ds}$-$V_{ds}$ response with varying gate voltage. From this curve, the biasing points
necessary for amplification and other characteristics can be determined. As seen in Figure 64, the typical, well-behaved I-V family of curves results in complete pinch-off of the device at a fairly low gate voltage.

In many cases, the transistors were found not to exhibit pinch-off. Optical microscope images taken of the devices post-processing revealed microscopic breaks in the gate fingers that account for this behavior in some devices. On three devices in the Ga-reflux sample (0613, 0614, and 0615), the initial $V_g=1$ V curve began as expected and then suddenly the current through the device went to 0. Most likely, catastrophic failure mentioned previously and shown in Figure 57 occurred during the measurement due to the higher power flowing through the device and associated heat generation.

![Figure 64 - $I_{ds}$-$V_{ds}$ FET family of curves for Device 0515 of the annealed sample C11-1.](image)

133
In Figure 65, device 0610 from the Ga-reflux treated sample is shown where the threshold voltage is nearly the same as the threshold voltage shown in Figure 64. Device 0610 has a $V_{th}=-1.88$ V and device 0515 has a $V_{th}=-1.92$ V. The general curve shape, however, is different and reflects the higher series resistance evident in the Schottky barrier diodes with the low barrier detected in the I-V curves of the gate contacts. The second Schottky barrier in the Ga-reflux treated sample may also be creating a sharper knee voltage and well-defined threshold voltage. It is expected that the high series resistance will affect the transconductance as well [97]. Clearly, the Ga-reflux method causes fundamental changes in the gate properties and the resulting device characteristics.

Figure 65 - $I_{ds}$-$V_{ds}$ FET family of curves showing increased series resistance for device 0610 of the Ga-reflux treated sample C11-2.
In Figure 66 below, the threshold voltage is shown for the various devices on sample C11. The threshold voltage is defined as the gate voltage necessary to deplete the channel of free carriers [91]. In looking at the two figures, it appears the Ga-reflux method and annealed samples had lower threshold voltages than the standard process device, although this is most likely a result of the RIE mask etch. The average threshold voltage for the standard process sample was -2.74±0.45 V. For the annealed sample, an average value of -3.36±0.53 V was found while the ion sputtered sample had an average value of -2.07±0.79 V. Finally, the Ga-reflux sample displayed an average threshold voltage of -2.79±0.61 V.

Figure 66 - $V_{th}$ map of sample C11. Threshold voltage values were higher in the $N_2$ ion sputtered sample in devices that did not exhibit high frequency response.
Figure 67 shows the variation in the threshold voltage at the level of the drain-source voltage vs. gate bias. As expected, the threshold voltage is located around -2 V for all samples. The ion-beam treated sample, however, appeared in most of the die to have an unclear threshold upon examining the $I_{ds}$-$V_{gs}$ curves. Closer examination of the FET family of curves for the same sample showed that none of the families of curves were recorded in complete form. The threshold voltages do not reveal this problem with the FET family of curves because the devices themselves are working, in most cases, as expected with regard to the Schottky barrier and Ohmic source and drain contacts. They simply do not pinch-off as is necessary for proper operation.

![Graph showing comparison of $I_{ds}$-$V_{gs}$ data for HEMT devices across three processing methods on sample C11.](image)

Figure 67 - Comparison of $I_{ds}$-$V_{gs}$ data for HEMT devices across three processing methods on sample C11.
As seen in Figure 68, the transconductance follows the expected form for a device with series resistance included. The particular curve shown is from device 0715 on the Ga-reflux treated sample that has resulted in poor overall device performance. Again, it is most likely a result of this portion of the sample having been exposed to a different amount of Ga flux during the cleaning cycle.

![Figure 68 - Device 0715 transconductance, $g_m$, and drain-source current, $J_d$ for the Ga-reflux treated sample.](image)

The transconductance of the HEMT, as in other transistors, determines the amount of current gain the device is capable of delivering for the input gate voltage. It is determined directly from the slope of the drain-source current as given in Figure 68. To obtain the most amplification, the peak of the $g_m$ curve is often set as the bias point. The
peak $g_m$ is shown in the form of a map for all the devices on sample C11 in Figure 69. Unexpectedly, the devices on the Ga-reflux treated sample appear to perform nearly as well as the devices on the annealed sample. The average of the peak transconductance for the standard process was determined to be $171.7\pm21.4$ mS/mm. For the annealed sample, the average $g_m$-peak is lower at $136.5\pm16.1$ mS/mm. The ion sputtered sample showed a value of $262.5\pm218.3$ mS/mm on average with device 0211 included. Upon manually examining the I-V curve, however, it was found that this device did not function properly, resulting in an unphysical $g_m$. Upon removing it from the data set, a more reasonable average of $45.4\pm25.9$ mS/mm was obtained indicating the entire set of transistors was essentially non-functioning. Finally, the Ga-reflux sample resulted in an average $g_m$-peak of $216.4\pm73.4$ mS/mm. Again, the artificially high device 0616 was removed resulting in a more reasonable average $g_m$-peak of $148.2\pm30.5$ mS/mm, comparable to the value found in the annealed sample.
Figure 69 - Maximum transconductance, $g_m$-peak, for sample C11. The majority of the devices subjected to the N$_2$ sputter treatment have an extremely low $g_m$-peak corresponding to the non-functioning HEMTs.

Finally, the reverse gate current was investigated and found to correspond to the onsets of saturation as shown in Figure 70. The significance of this measurement is in the possible contribution of the gate leakage current in the destructive failure of the devices during operation.
Figure 70 - FET family of curves with corresponding reverse gate leakage current for device 0512 from the annealed portion of sample C11-1.

As can be seen in Figure 71, the reverse gate leakage currents as determined from the $I_g$-$V_{gs}$ characteristics are correlated with the processing. The lowest leakage currents are seen on the standard process sample which was not subjected to a damaging RIE etch. The annealed and ion sputtered samples both appear to have significantly more leakage current. The Ga-reflux sample consistently performs with extremely high gate leakage.
This also explains the catastrophic failures noted during device testing due to the poor Schottky barriers as noted previously.

Figure 71 - Gate leakage current at gate bias = -4 V for sample C11.

A plot of the $I_d$-$V_{gs}$ curves for typical devices across C11 is shown in Figure 72. Clearly, the device from the Ga-reflux sample is conducting over 4 orders of magnitude more reverse current through the gate than the standard process device. Consistently, this sample performs poorly and nearly all measurements indicate the process is unsuitable as a cleaning procedure for HEMT fabrication, although the two devices which worked properly gave unusually high cutoff frequency responses. Proper optimization of the Ga-reflux method would be necessary and may result in higher yields and an improved frequency response over standard processing. Ion sputtering, however, is promising and
with an appropriate optimization of the sputter conditions, may be beneficial to the sample gate region. The RIE in general damages the Schottky barrier as indicated perhaps most clearly in the reverse gate leakage map and $I_d$-$V_{gs}$ curves, but the RF device performance is still impressive despite this disadvantage.

![Diagram showing negative gate current vs. drain-source voltage for typical devices on sample C11.]

Figure 72 - Reverse gate current vs. drain-source voltage for typical devices on sample C11.

Overall, the surface treatments resulted in specific changes in the electrical characteristics of the devices as exhibited by the FET family of curves and related gate leakage, threshold voltage, and transconductance values. The FET family of curves for the Ga-reflux sample indicated the high series resistance in the overall response as expected from the prior Schottky gate analysis. The threshold voltage and maximum
transconductance were clearly poorer in the N$_2$ sputtered devices due to the damage as indicated in the CL analysis. The leakage current, on the other hand, was best for the standard process devices, followed by the annealed, the Ga-reflux treated, and the N$_2$ ion sputtered devices. These results show the importance of not only surface cleanliness, but also the defect levels within the device on the final device performance characteristics.

5.3.2 Low-temperature Ohmic metal investigation

During preliminary investigations of sample C11, low-temperature CL mapping was performed to determine the origin within the sample of particular defect features. As shown in Figure 73, a difference in the line scan spectra was observed for the Ohmic contacts on and off the AlGaN mesa. The low-energy shoulder of the GaN NBE at ~3.40 eV increases for the Ohmic contacts on-mesa indicating a possible correlation of this defect with Ti/Al/Ni/Au placement on an AlGaN surface vs. GaN.
Figure 73 - Low-temperature surface-sensitive CL of Ohmic and mesa regions both on and off the mesa normalized to the GaN NBE for comparison of the defect shoulder luminescence. A 600 V electron beam was used at 1x10^{-9}A.

To determine the origin of this luminescence, CL mapping was utilized. Figure 74A shows a typical Ohmic contact alignment mark placed on the AlGaN/GaN mesa. In Figure 74B, the dominant 3.45 eV GaN NBE luminescence is uniformly distributed throughout the mesa region. Figure 74C clearly shows the localization of the 3.40 eV defect as seen in the line scan spectra to the edges of the Ohmic contact region. The Ohmic contact is in some way causing a new defect level to form in the interaction of the metal layers with the AlGaN surface post-annealing.
Figure 74 - CL maps of sample C11 showing (A) SEM of Ohmic alignment mark on AlGaN/GaN mesa, (B) 3.45 eV GaN NBE, and (C) 3.40 eV shoulder localized around the Ohmic metal.

Similar maps are shown in Figure 75 for a similar Ohmic contact alignment cross placed off the mesa region on the GaN buffer layer. As seen in the figure, the 3.45 eV GaN NBE is dramatically reduced. This is expected from previous line scan measurements that revealed a reduction in intensity on the order of 10x for the entire spectra off mesa. The RIE damage and the lower quality of the underlying buffer layer result in this reduced luminescence. Of particular importance, however, is Figure 75C, in which rather than localized bright regions of 3.40 eV defect luminescence surrounding the entire Ohmic metal region, the spectra indicate a complete lack of this defect. The mesa region includes an upper layer of AlGaN as described in Table 2. The off-mesa regions consist of pure GaN. Clearly, the ~50 meV defect level is only formed on-mesa where Al is present or where there is no damage due to the RIE mesa etch.
Once the Ohmic-related luminescence was determined to originate from the mesa regions, similar maps were recorded with varying electron beam energies to determine the depth at which the defects are most concentrated. Figure 76 shows the same defect luminescence on a different Ohmic contact and reveals the highest concentration appears at a depth of 5 keV. This result identifies the deeper layers of the device to be participating and contributing to this defect. The Ohmic contact after annealing is expected to make a low-resistance contact to the 2-DEG layer at the AlGaN/GaN interface. The increase of this defect emission at 5 and 10 keV shows that the defects are originating from well within the GaN channel layer below ~230 Å.
Figure 76 - CL maps of the 3.40 eV defect luminescence with varying electron beam penetration voltages on sample C11.

Because this luminescence was observed for Ohmic contacts on GaN, an investigation was made into other Ohmic metal compositions to determine if this was specific to the Ohmic contacts themselves or whether it was a common characteristic of metal on AlGaN/GaN. A different quarter of sample C11 on which standard gates had been processed without the use of the dual-layer gate mask allowed the investigation of this defect formation as shown in Figure 77 with the Ni/Au gate metal. It was quickly apparent that the defect luminescence only appears to accumulate around the edges of the
Ti/Al/Ni/Au Ohmic contacts since the gate metal regions consisting of Ni/Au do not exhibit this defect luminescence, even on the AlGaN mesa.

![Ohmic SEM](image1)

![Gate SEM](image2)

Figure 77 - Sample C11 with both Ohmic and gate metal on mesa AlGaN. The 3.40 eV shoulder defect luminescence only appears for the Ohmic metal with no defect luminescence from the gate metal edges.

The Ohmic metal layers consist of Ti/Al/Ni/Au that has been annealed at 850°C to create the low-resistance contact to the device layer at the GaN/AlGaN interface. From the CL investigations discussed, this process also creates a defect level that occurs ~0.05 eV below the GaN NBE and extends to a depth well into the GaN channel layer below the 2-DEG. The gate metal regions do not exhibit such luminescence and are therefore not a participant in the defect formation. The best identification of this defect
level based upon the energy of the luminescence is as the Y2-luminescence line occurring at \( \sim 50 \text{ meV} \) below the DBE, or GaN NBE. Research to date assigns this defect luminescence to structural defects and in particular, to excitons bound to surface defects and not dislocations [85]. If this is true, the yet unidentified surface defects may be caused by the incorporation and disruption of the lattice by some aspect of the Ohmic metal. The Ohmic contact consists of the metals Ti, Al, Ni, and Au while the gate metal consists of the latter two metals, Ni and Au. In addition, the AlGaN surface contains Al, possibly a necessary component in the defect formation. The RIE etched region in which the AlGaN has been removed and GaN is the exposed surface did not exhibit such luminescence, however, further supporting the idea that AlGaN may be essential in producing this particular defect and that perhaps this defect is essential in producing low-resistance Ohmic contacts by providing a low-barrier path for current flow through the GaN.

5.4 Conclusion

As seen in the frequency characteristics of HEMTs fabricated using the dual-layer mask process, responses comparable to that found in standard process devices can be obtained. Appropriate optimization should decrease the differences between the two processing methods allowing the use of the dual-layer technique as a replacement mask to traditional organic photoresists. The advantages to this are great when opportunities are considered such as more detailed study of device processing in UHV and the use of UHV analysis techniques during processing steps to understand in greater detail the
formation mechanisms of the gate Schottky contact. Additionally, and perhaps more important for the device engineer, is the opportunity to use more difficult metal schemes for the gate than available with standard photoresist. Examples include exotic refractory metals with various work functions that can be evaporated onto the more durable Si$_3$N$_4$/SiO$_2$ mask as well as metallizations only available using sputter sources. It is expected that with minimal modifications, the mask would be suitable for lift-off of sputtered metals.
CHAPTER 6.

ALGAN/GAN/SIC HEMT DEVICE OHMIC CONTACT INVESTIGATION AND EFFECT OF RIE ON DEVICE PERFORMANCE

Upon discovering variations in both the device performance with processing and in Ohmic contact defect formation on mesa regions, an experiment was designed to pursue the causes and correlations of the phenomena with regard to the nature of the Ohmic contacts. The composition of sample F01 is given in Table 2. The channel and buffer layers are combined into one 1.51 µm GaN layer. This entire structure has been grown on a 6H-SiC substrate.

A CASINO Monte Carlo simulation of the electron beam penetration with beam voltage reveals that for electron beams less than 2 keV, the excitation will occur mainly in the upper AlGaN layer. For electron beams of energy greater than 2 keV, the majority of excitation occurs in the underlying GaN channel and buffer. Most of the analysis was performed at an electron beam energy of 600 eV to analyze the effects of the RIE damage on the upper surface layers, although depth-dependent information can be acquired through the careful adjustment of the beam characteristics in CL analysis as discussed previously.
Figure 78 – Sample F01 CASINO Monte Carlo simulation of electron penetration depth for varying electron beam energies.

6.1 Device Fabrication

The devices were fabricated using a mask set that includes structures for Ohmic contact characterization, also known as process control structures. The aspect of this mask that differs from the mask used in C11 is that four different Ohmic layer compositions can be used and compared with four independent subreticles per die. For sample F01, this aspect of the mask allowed a comparison of four different Ohmic variations on the device characteristics. Also, these four types of Ohmic metal could be investigated to determine the role of the Ohmic composition on the Y2-defect formation that occurs surrounding the Ohmic contact metal as seen in sample C11. Finally, the
sample was masked after the Ohmic contacts were deposited and half of the device gate regions were subjected to an RIE etch similar to the etch subjected to the surface of sample C11 during the dual-layer mask development to determine the effect of this etch on final device performance. The general layout of the wafer is shown in Figure 79 with the RIE regions clearly marked and the unprocessed portions of the wafer shown.

![Figure 79 - Sample F01 map showing regions of processing for RIE and demonstrating the basic layout of the Ohmic contacts on the sample. The inset illustrates the concept of four subreticles with four Ohmic contact metal schemes contained within each die.](image)

The exact thicknesses of the Ohmic metals used are given in Table 7. The metals were evaporated in a standard e-beam metal evaporator under HV conditions following a 30 second 1:1 HCl:DI pre-metal dip.

<table>
<thead>
<tr>
<th>Ohmic</th>
<th>Metal Structure</th>
<th>Thicknesses (Å)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>Ti/Al/Ni/Au</td>
<td>350/2333/500/200</td>
</tr>
<tr>
<td>B</td>
<td>Ti/Al/Ir/Au</td>
<td>200/1000/500/200</td>
</tr>
<tr>
<td>C</td>
<td>Ti/Al/Mo/Au</td>
<td>150/600/350/500</td>
</tr>
<tr>
<td>D</td>
<td>Ti/Al/Pt/Au</td>
<td>350/2333/500/200</td>
</tr>
</tbody>
</table>

Table 7 - Sample F01 Ohmic metal structures and thicknesses.
The gate metal used was 200/2800 Å Ni/Au. Although a pre-metal dip similar to that described for the Ohmic contacts can be used prior to the gate evaporation, this was not performed for sample F01. This was done in the interest of preserving the seven different metals exposed in the four Ohmic contacts from any possible interactions with the acid mixture used as a pre-metal dip.

6.2 Initial CL Analysis

Initial CL scans as shown in Figure 80 revealed well-behaved spectra with an AlGaN NBE visible at depths of 5 and 10 keV electron beam penetration. The AlGaN band edge was located at 3.96 eV in this location and at 3.99 eV in a location toward the center of the quarter wafer corresponding to Al mole fractions of 0.26 and 0.277 for a bowing parameter of 1.0 in good agreement with the expected x=0.28 as given by the grower. The amount of 2.55-3.25 eV BL at this location is minimal, although as the sample is excited nearer to the AlGaN/GaN 2-DEG interface, the intensity of this defect luminescence increases.
Figure 80 – Low-temperature CL analysis of sample F01 prior to processing at beam voltages of 500 eV, 1 keV, and 5 keV.

CL spectra was recorded at each die location on the wafer both after the mesa etch prior to the Ohmic anneal and after the devices, including the gate metal deposition, were completed. The CL scans at 600 eV used an electron beam current of $5 \times 10^{-9} \text{A}$. The pre-scans were taken on open mesa regions with a 10,000x magnification while the post-scans were taken on the processed gates with 1,000x magnification to excite the maximum open gate region since the Ohmic and gate contacts mask the large majority of signal contribution area after processing. The additional scans for depth-dependent studies were recorded with incident electron beam conditions of 2 and 5 keV at $2.5 \times 10^{-9} \text{A}$ and 1,000x magnification to include the entire device structure gate region. Due to these varying analysis conditions, each line scan was normalized to the GaN NBE prior to further analysis eliminating differences in signal intensity due to the available excitation.
regions. Integrations of the same energy regions were performed for each map as shown in Table 8. The initial scans were recorded with a slit width of 0.5 mm, but due to the decrease in signal intensity after processing, 1 mm slit widths were used. This leads to an unfortunate difficulty in comparing the two scans due to dispersion and associated curve broadening. The pre-scans were recorded at twice the step size of the post-scans and the monochromator has dispersion as shown in Equation 16 where the grating used contains 1200 lines/mm. A summation of the same energy range for both sets of curves can be compared for general trends with these normalizations and assumptions as stated. Finally, the scale of each sample set shown below has been set with the same minimum and maximum to allow for cross-comparisons in the image maps.
Table 8 - Energy regions of integration of CL line scans used to produce CL wafer maps.

<table>
<thead>
<tr>
<th>Energy Region Name</th>
<th>Energy Range of Integration (Summation)</th>
</tr>
</thead>
<tbody>
<tr>
<td>GaN NBE</td>
<td>3.43-3.55 eV</td>
</tr>
<tr>
<td>1st Shoulder (Y2 Defect Luminescence)</td>
<td>3.43-3.40 eV</td>
</tr>
<tr>
<td>Blue Luminescence (BL)</td>
<td>2.55-3.25 eV</td>
</tr>
<tr>
<td>Yellow Luminescence (YL)</td>
<td>2.07-2.54 eV</td>
</tr>
</tbody>
</table>

\[
Dispersion = \frac{1.8 \times 1800}{(\text{lines/mm}) \times \text{slitwidth}}
\]  

(16)

As seen in Figure 81 below, the sample is fairly uniform in the pre-scans with a relatively high GaN NBE luminescence indicating high levels of radiant recombination in the sample at the near band edge. This would result from a sample with a low concentration of additional defects and lower energy recombination pathways available and corresponding high crystal quality. After processing, however, the sample luminescence intensity decreases dramatically as shown in the post-processing map at 600 eV.

Additional details about the effects of processing and the role of the Ohmic metal on CL intensities can be determined by looking at the statistics of each subreticle, or individual Ohmic metal portion of each die as shown in Figure 79, compared to the initial condition of the sample. The subreticles exhibiting no RF response were removed from the dataset as bad devices. Details of this analysis are shown in Table 9. The intensity was reduced by \(\sim\)9\% for Ohmic A at 600 V while the intensity was reduced by \(\sim\)16\% for the other Ohmic metals. Most likely, this difference between the Ohmic contacts is a direct result of the range of energies used in calculating the CL intensities for the GaN
due to the overlap of the Y2 defect luminescence with the GaN NBE energy range. In addition, there is a significant increase in Y2 luminescence intensity for Ohmic A, Ti/Al/Ni/Au, as will be discussed below. It must also be remembered that the values for the maps and statistics were derived from CL spectra normalized to the GaN NBE intensity. This should result in a flat map for these scans unless the peak broadens and results in a higher intensity for the integrated or summed results. The overall trend in the GaN NBE data, however, is a decrease in post-processing luminescence. There is no effect of the RIE etch damage on the GaN NBE as observed in the CL maps and statistics. It appears the GaN NBE, originating from a buried layer beneath the AlGaN, is not affected by this low-voltage etch as investigated from the near-surface to a depth of ~100 nm. This is a promising result for further investigations of both the use of the dual-layer mask in future mask designs as well as the use of low-power RIE in other types of processing.
Figure 81 - GaN NBE CL intensity maps for sample F01 both pre-Ohmic and post-gate processing. The Ti/Al/Ni/Au Ohmic contacts have a higher intensity of GaN NBE most likely due to an increased low-energy shoulder resulting from Y2 defect luminescence for these contacts.

<table>
<thead>
<tr>
<th>Description</th>
<th>RIE?</th>
<th>Ohmic A</th>
<th>Ohmic B</th>
<th>Ohmic C</th>
<th>Ohmic D</th>
</tr>
</thead>
<tbody>
<tr>
<td>Composition</td>
<td></td>
<td>Ti/Al/Ni/Au</td>
<td>Ti/Al/Ir/Au</td>
<td>Ti/Al/Mo/Au</td>
<td>Ti/Al/Pt/Au</td>
</tr>
<tr>
<td>600 eV Pre</td>
<td></td>
<td>3.82±0.05</td>
<td>3.59±0.02</td>
<td>3.50±0.03</td>
<td>3.56±0.04</td>
</tr>
<tr>
<td>600 eV Post</td>
<td>No</td>
<td>3.85±0.09</td>
<td>3.53±0.03</td>
<td>3.47±0.02</td>
<td>3.62±0.02</td>
</tr>
<tr>
<td>2 keV Post</td>
<td>No</td>
<td>3.86±0.03</td>
<td>3.61±0.03</td>
<td>3.53±0.01</td>
<td>3.57±0.05</td>
</tr>
<tr>
<td>5 keV Post</td>
<td>No</td>
<td>3.66±0.09</td>
<td>3.48±0.08</td>
<td>3.50±0.06</td>
<td>3.49±0.08</td>
</tr>
<tr>
<td>600 eV Post</td>
<td>Yes</td>
<td>3.82±0.03</td>
<td>3.54±0.04</td>
<td>3.45±0.02</td>
<td>3.57±0.03</td>
</tr>
<tr>
<td>2 keV Post</td>
<td>Yes</td>
<td>3.83±0.03</td>
<td>3.60±0.02</td>
<td>3.50±0.03</td>
<td>3.59±0.03</td>
</tr>
<tr>
<td>5 keV Post</td>
<td>Yes</td>
<td>4.10±0.04</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 9 - Normalized statistical analysis of CL intensity data shown in Figure 81. It is clear that Ohmic metal A consistently exhibits higher GaN NBE compared to the other metals while the RIE etch does not affect the GaN NBE luminescence.
The second CL feature of interest is the Y2 defect that was first seen and discussed in sample C11. This shoulder of the GaN NBE in sample C11 appeared only in the case of the Ti/Al/Ni/Au Ohmic contact structure and only surrounding the Ohmic metallization on AlGaN/GaN mesa regions of the sample. In the wafer maps in Figure 82, there is an increase in the amount of Y2 luminescence for all four different metallization studied. However, there is clearly a stronger correlation of Y2 defect luminescence intensity increase after gate processing with the Ti/Al/Ni/Au Ohmic metal structure compared to the other metals used. This indicates the defect is associated most strongly with some aspect of the Ni variation of Ohmic contact and may be due to structural defects formed during the incorporation of the Ni metal in the AlGaN/GaN layers. This would also strongly indicate the Y2 defect is related to a surface defect, perhaps one that can form at the interface between the AlGaN or GaN and the metal islands that form within the Ohmic contact during annealing and diffusion of the metal into the semiconductor. An additional observation is that the Ohmic C metal, Mo, does not appear to exhibit as intense Y2 luminescence as the other metals and may be a result of the way Mo reacts with AlGaN and GaN compared to the other metals investigated.

The Y2 luminescence does not appear to be affected by the RIE etch. The data indicates that, like the GaN NBE, this particular luminescence is not intensified by the damage from the etch. Rather, it is correlated to the particular metal used in the Ohmic contact. In addition, the depth dependence data shows a distribution of the Y2 defect throughout the sample to a depth of at least 70 nm where the luminescence intensity does not appear to decay even for the highest electron beam energy used.
Figure 82 - GaN low-energy shoulder (Y2-defect) CL intensity maps for sample F01 both pre-Ohmic and post-gate processing. The Ti/Al/Ni/Au Ohmic contacts exhibit intense Y2 defect luminescence post-processing. Ir- and Pt-based Ohmic contacts also appear to exhibit a lower intensity of this same defect.

<table>
<thead>
<tr>
<th>Description</th>
<th>RIE?</th>
<th>Ohmic A</th>
<th>Ohmic B</th>
<th>Ohmic C</th>
<th>Ohmic D</th>
</tr>
</thead>
<tbody>
<tr>
<td>Composition</td>
<td></td>
<td>Ti/Al/Ni/Au</td>
<td>Ti/Al/Ir/Au</td>
<td>Ti/Al/Mo/Au</td>
<td>Ti/Al/Pt/Au</td>
</tr>
<tr>
<td>600 eV Pre</td>
<td>No</td>
<td>0.076±0.002</td>
<td>0.084±0.006</td>
<td>0.104±0.007</td>
<td></td>
</tr>
<tr>
<td>600 eV Post</td>
<td>No</td>
<td>0.17±0.01</td>
<td>0.066±0.002</td>
<td>0.088±0.007</td>
<td></td>
</tr>
<tr>
<td>2 keV Post</td>
<td>No</td>
<td>0.089±0.006</td>
<td>0.103±0.004</td>
<td>0.110±0.005</td>
<td></td>
</tr>
<tr>
<td>5 keV Post</td>
<td>No</td>
<td>0.18±0.02</td>
<td>0.084±0.014</td>
<td>0.100±0.023</td>
<td></td>
</tr>
<tr>
<td>600 eV Post</td>
<td>Yes</td>
<td>0.082±0.010</td>
<td>0.084±0.014</td>
<td>0.100±0.023</td>
<td></td>
</tr>
<tr>
<td>2 keV Post</td>
<td>Yes</td>
<td>0.081±0.005</td>
<td>0.071±0.003</td>
<td>0.078±0.002</td>
<td></td>
</tr>
<tr>
<td>5 keV Post</td>
<td>Yes</td>
<td>0.15±0.01</td>
<td>0.099±0.006</td>
<td>0.080±0.002</td>
<td>0.102±0.003</td>
</tr>
</tbody>
</table>

Table 10 - Normalized statistical analysis of CL intensity data shown in Figure 82. Ohmic contact A, Ti/Al/Ni/Au, exhibits nearly twice the integrated intensity of Y2 luminescence compared to the other Ohmic contacts.
The third feature of the CL spectra, the blue luminescence (BL), has been shown to increase with annealing in sample C11. This particular luminescence is also prominent in the F01 sample post-processing. Wafer maps of the BL are shown in Figure 83 below. Initially, the amount of BL appears very low in intensity and uniform throughout the wafer. Post Ohmic processing, however, the intensity is nearly doubled in the portion not subjected to an RIE etch. From previous experience, the Ohmic contact RTA alloying anneal most likely caused this increase in BL intensity. In sample C11, as discussed previously, an increase in the BL was noted in every process step following an anneal, regardless of the change in BL that may have been seen prior to the anneal due to processing.

Of particular interest is the strong correlation of this BL with the RIE etch. In the etched portions of the sample, the BL increases by over a factor of 10. This increase in intensity does not correlate with any particular Ohmic metal and is uniformly distributed throughout the RIE treated sample. At an electron beam voltage of 2 keV, the BL is ~5x more intense in the RIE-treated portion of the sample compared to the non-RIE treated portion. As seen in Figure 78, this corresponds to an electron penetration depth of ~20 nm, or distributed mainly at the AlGaN/GaN interface. Finally, using the 5 keV electron beam, the distribution again appears to be the same on either portion of the sample regardless of the RIE etch. Therefore, the intense BL increase in sample F01 is isolated to the upper AlGaN layer and the depth of damage by the particular RIE etch used in the dual-layer gate mask processing extends to a depth of approximately the top AlGaN device layer, i.e. 190 Å.
Figure 83 – Blue Luminescence (BL) CL intensity maps for sample F01 both pre-Ohmic and post-gate processing. The RIE damage increases the amount of BL exhibited by the sample in the top layers of the device as clearly demonstrated by the maps at 600 eV and 2 keV post-processing.

<table>
<thead>
<tr>
<th>Description</th>
<th>RIE?</th>
<th>Ohmic A</th>
<th>Ohmic B</th>
<th>Ohmic C</th>
<th>Ohmic D</th>
</tr>
</thead>
<tbody>
<tr>
<td>Composition</td>
<td></td>
<td>Ti/Al/Ni/Au</td>
<td>Ti/Al/Ir/Au</td>
<td>Ti/Al/Mo/Au</td>
<td>Ti/Al/Pt/Au</td>
</tr>
<tr>
<td>600 eV Pre</td>
<td></td>
<td>0.39±0.13</td>
<td>0.35±0.08</td>
<td>0.33±0.07</td>
<td>0.35±0.09</td>
</tr>
<tr>
<td>600 eV Post</td>
<td>No</td>
<td>0.39±0.13</td>
<td>0.35±0.08</td>
<td>0.33±0.07</td>
<td>0.35±0.09</td>
</tr>
<tr>
<td>2 keV Post</td>
<td>No</td>
<td>0.30±0.11</td>
<td>0.30±0.10</td>
<td>0.48±0.07</td>
<td>0.29±0.07</td>
</tr>
<tr>
<td>5 keV Post</td>
<td>No</td>
<td>0.23±0.11</td>
<td>0.27±0.14</td>
<td>0.30±0.07</td>
<td>0.24±0.08</td>
</tr>
<tr>
<td>600 eV Post</td>
<td>Yes</td>
<td>1.71±0.40</td>
<td>1.46±0.25</td>
<td>1.51±0.35</td>
<td>1.69±0.35</td>
</tr>
<tr>
<td>2 keV Post</td>
<td>Yes</td>
<td>0.69±0.12</td>
<td>0.66±0.15</td>
<td>0.72±0.15</td>
<td>0.76±0.14</td>
</tr>
<tr>
<td>5 keV Post</td>
<td>Yes</td>
<td>0.33±0.06</td>
<td>0.27±0.04</td>
<td>0.32±0.03</td>
<td>0.28±0.03</td>
</tr>
</tbody>
</table>

Table 11 - Normalized statistical analysis of CL intensity data shown in Figure 83. The surface of all Ohmic contacts post-processing with RIE exhibit nearly 4x the integrated intensity of BL compared to the non-RIE post-processing Ohmic contacts. The BL is most intense in the 600 eV and 2 keV upper layers with nearly no change detected at 5 keV.
The final defect feature of the CL spectra is the yellow luminescence (YL) observed in both C11 and F01. The cause of this luminescence is unclear, although many models and theories have been proposed to explain it. The integrated YL intensities for sample F01 are shown in Figure 84 below. The initial scans have a low concentration of YL defect emission across the entire sample. After Ohmic processing, however, the YL increases by a factor of nearly 10 across the entire sample. This increase is not due to the RIE etch since the RIE portion has nearly the same intensity as the non-RIE portion of the wafer.

The YL appears to be uniform throughout the entire depth of the sample. In analyzing both the wafer maps and statistics presented in Table 12, the Ohmic metal composition appears to affect the YL intensity. The A and D Ohmic metals, or Ni and Pt, have a higher concentration of YL regardless of the depth of excitation. The B and C Ohmic metals, or Ir and Mo, on the other hand, exhibit lower concentrations of YL overall. In processing and analyzing sample C11, the surface cleaning techniques attempted were not observed to change the overall concentration of YL to any significant extent. This may be due to the fact that the YL was stabilized prior to surface processing due to the fabrication methods used in forming the mesas, Ohmic contacts, or gate mask. The YL in sample F01 at the surface, however, appears to be dramatically increased by the fabrication in general.
Figure 84 - Yellow luminescence (YL) CL intensity maps for sample F01 both pre-Ohmic and post-gate processing. The Ohmic composition appears to result in increased intensity of the YL while RIE processing does not affect the formation of YL.

Table 12 - Normalized statistical analysis of CL intensity data shown in Figure 84. The YL intensity is nearly 3x higher at the surface region for all metals post-processing with only a slight correlation to the Ohmic metal used. Ni-based contacts appear to have an increased amount of YL followed by Pt, Ir, and Mo.
6.3 Electrical Response for Sample F01

As discussed previously, sample F01 was fabricated to test both the effect of the RIE etch on the devices and also to investigate the role of the Ohmic metal contacts on performance. To effectively address this, it is necessary to correlate the electrical performance with the CL response as well as Ohmic data to RF response.

The Ohmic contact characteristics will be discussed to lay a foundation for the RF characteristics as well as for correlations to be made between the two. The contact resistance in ohm-mm is shown in Figure 85. It should be remembered that the Ohmic metals were deposited and analyzed prior to the RIE etch, so averages for the entire wafer are valid for these data sets. The Ti/Al/Ir/Au contacts had significantly higher contact resistances than the other devices with an average of 2.52±0.19 ohm-mm vs. 0.36±0.02 for Ni, 0.46±0.10 for Mo, and 0.49±0.03 ohm-mm for Pt. It is expected that device performance will be best for Ni contacts and that Ir contacts will result in poor performance overall.
Figure 85 - Contact resistance (Ohm-mm) for sample F01. Notice that Ohmic B, Ir, has an overall higher contact resistance than the other three metals.

The sheet resistance under the Ohmic contacts is shown in Figure 86. There is a slight trend across the sample decreasing from right to left. This is not contact metal dependent and is a result of the quality of the wafer itself. The average sheet resistance for the sample is 420.6 ohms/square.
The specific contact resistance is a good determination of the nature of the Ohmic contact and can be used to compare different contacts. Of the four metals used in the Ti/Al/metal/Au contact structure for sample F01, it was found that the best contacts were made using Ni with an average specific contact resistance of $3.26\pm0.5\times10^{-6}$ Ohms-cm$^2$. Pt followed this at $5.75\pm0.63\times10^{-6}$ Ohms-cm$^2$, Mo with $9.39\pm6.22\times10^{-6}$ Ohms-cm$^2$, and finally Ir with the largest specific contact resistance of $1.65\pm0.26\times10^{-4}$ Ohms-cm$^2$.

Overall, the Ni, Pt, and Mo-based Ohmic contacts exhibit similar behavior while the Ir performed poorly. These results are comparable to specific contact resistivities obtained for state-of-the-art Ohmic contacts [98]. It has been shown that Ir-based Ohmic contacts can perform as well as or better than Ni-based Ohmic contacts. Ir is particularly robust at
higher temperature operation [90, 94, 99]. The most likely cause for Ir-based Ohmic contacts on F01 to perform poorly compared to the other Ohmic contacts is the metal thicknesses as given in Table 7. For example, in the study described by Fitch et. al., the Ir-based Ohmic contact was reported to have a specific contact resistance of $4.6 \times 10^{-5}$ Ohms-cm$^2$. This is significantly lower than the values recorded on sample F01. However, the thickness used to achieve this was 300/2000/500/200 Å Ti/Al/Ir/Au compared to 200/1000/500/200 Å used in sample F01. Further investigation into optimizing the metal thickness for sample F01 are necessary to determine the full potential of Ir-based contacts on this sample.

![Figure 87 - Specific contact resistance for sample F01 in ohm-cm$^2$. Notice that Ohmic B, Ir, has a much higher specific contact resistance than the other three metal contacts.](image)

169
The Ohmic data demonstrates that the contacts were of a high quality in three of the four cases. The poorer performance of the Ir contact does not appear to correlate to the changes in CL emission, however. Only the Ni contacts exhibited a difference in the Y2 defect luminescence as discussed previously. From these results, the CL intensities when considering the Y2, BL, and YL defect luminescence appear to correlate to the sample quality and to the specific contact resistance only when all defects are considered and not in direct relation to any specific defect. Therefore, it is difficult to predict the quality of the resulting Ohmic contact due to the multiple variables, i.e. defects, sample quality and uniformity, metals, metal thicknesses, anneal temperatures, etc., encountered in processing the contacts.

6.4 DC and RF Electrical Results for Sample F01

As discussed in sample C11, the forward $V_{gs}$ for $I_{gs} = 2mA/mm$ is a good indication of the quality of the Schottky barrier. Shown in Figure 88 are the values for this test where there is a correlation between Ohmic metal A and the Schottky diode behavior. The gate metal used for the entire sample was 200/2800 Å Ni/Au. The Ohmic contact, as expected, affects the electrical behavior of the Schottky contact. Since the test parameter requires that the current through the device be a constant for each test position, when a lower resistance Ohmic contact is used on a device, the voltage required to pass the same amount of current will increase assuming the same Schottky barrier height. This correlation is due in part to the better Ohmic contacts that result from using Ni and is another indication of device quality and expected device performance.
Figure 88 - $V_{gs}$ for $I_{gs} = 2mA/mm$ for sample F01. Notice the Ohmic A, Ni, exhibits higher values for this test due to the lower contact resistance for this metal.

Figure 88 illustrates how the Ohmic contact quality can affect the gate test values obtained in the previous discussion. In addition, the Schottky diode I-V curves are shown in Figure 89 and Figure 90. The lower contact resistance results in a better device performance due to lower losses even after series resistance effects have begun to dominate. Also, the I-V curve demonstrates a different reverse bias behavior than was found in C11 as a result of the better device performance achieved with this wafer and process method. The best performing Schottky diodes are those associated with the best performing Ohmic contacts due to the effect of the improved Ohmic contacts lowering the series resistance on Schottky diode performance.
Figure 89 - $I_{gs}$-$V_{gs}$ characteristics of the Schottky contacts for the four subreticles of die position [14,17] located in the non-RIE exposed region of sample F01.

In addition to the various Ohmic contact effects on the Schottky diodes, the RIE etch also changes the general characteristics as shown in Figure 90 for a single Ohmic contact A, Ni, in both the RIE-exposed and non-RIE exposed portions of sample F01. Although the non-RIE exposed sample exhibits a higher reverse bias leakage current, the forward characteristics are better than in the RIE exposed sample.
Figure 90 - $I_{gs}$-$V_{gs}$ characteristics with respect to the RIE exposure for devices 14,18A and 14,19A of sample F01. The RIE-exposed curve, 14,19A, reaches the upper current limit before the final bias voltage is reached.

The peak in the transconductance, $g_{m}$-peak, is another indication of the overall gain available in the device and determines a resulting bias point for further RF testing. As shown in Figure 91, the RIE etch does not appear to correlate with the $g_{m}$-peak data, although the poorer Ir Ohmic contacts do result in a slightly lower value and poorer device compared to the other three metals. These results should translate into the final frequency performance of the device.
The threshold voltage of the HEMT transistor is shown below in Figure 92. The RIE etch has a definite impact on the threshold voltage most likely due to the damage caused during the etch process. This degradation in the threshold voltage is possibly a result of the increase in the BL and additional current leakage paths in the device gate region. As seen in Figure 93, this change in the threshold voltage shifts the transistor load line, knee voltage, and bias parameters thereby causing the device performance to suffer.
Figure 92 - $V_{th}$ wafer map of sample F01 showing a definite increase in $V_{th}$ due to the RIE etch process applied to the upper portion compared to the non-RIE exposed region.
Figure 93 - FET family of curves for devices 14,18, non-RIE exposed, and 14,19, RIE exposed, demonstrating the difference in I-V characteristics caused by the RIE etch effect on $V_{th}$. Curves with square symbols represent I-V measurements from device 14,18A while triangle symbols represent device 14,19A.

As seen in Figure 94 and Figure 96, the cutoff frequency, $f_T$, at $g_{m\text{-peak}}$ and the maximum frequency of oscillation, $f_{\text{max}}$, at maximum available gain and $g_{m\text{-peak}}$ reveal subtle differences as expected from the CL and previous electrical measurements. For clarity, Figure 95 presents the average values of $f_T$ for sample F01. Ohmic metals B and C, Ir and Mo, perform with lower $f_T$ and $f_{\text{max}}$ response than Ohmic metals A and D, Ni and Pt. These contacts appear to be less susceptible to large variations in cut-off frequency performance due to RIE processing. For example, the decrease in cut-off frequency for the Ir and Mo contacts was ~16% from non-RIE to RIE etched sample while the Ni and Pt contacts exhibited ~45-55% decrease in performance due to the RIE.
The Ir contacts, Ohmic B, were expected to result in poorer devices due to the resistive losses in the Ohmic contacts themselves. Metal variation D, however, exhibited a slightly higher level of YL in the CL spectra and a slightly higher contact resistance and specific contact resistance. This most likely explains the slight loss in frequency performance overall.

Figure 94 - \( F_1 \) at \( g_{\text{m-peak}} \) for sample F01. Overall, the performance on the RIE etched portion of the sample is poorer than on the non-RIE exposed portion.
Figure 95 - Summary of average $f_T$ values in GHz for sample F01 by RIE region and Ohmic metal type.

The frequency response of these devices does not appear to correlate to the Y2 defect luminescence apparent in the Ni-based Ohmic contacts. The BL luminescence, however, is an indicator of the final quality of the devices as demonstrated by the BL increase due to the RIE processing and corresponding increase in threshold voltage and decrease in overall frequency response.
Figure 96 - $F_{\text{max}}$ (MAG) at $g_{\text{m-peak}}$ for sample F01.

6.5 Ohmic Investigation of Sample F01

In addition to the electrical CL comparisons for each device and the correlations to final device performance, the Ohmic contacts were also investigated as in sample C11 for the appearance of Y2 luminescence. Previously, it was found that the Ohmic contacts on AlGaN mesa region produced luminescence at $\sim$50 meV below the GaN NBE in confined regions directly surrounding the Ohmic contacts on sample C11. To determine whether the defect formed with the anneal or if this was a characteristic that appeared just after metallization, pre-scans of sample F01 were taken prior to the Ohmic RTA anneal as shown in Figure 97.
The Ohmic alignment marks prior to annealing appear similar in the SEM images with extremely uniform surfaces. GaN NBE appears to be uniform throughout the mesa region as expected. At ~50 meV below the GaN NBE, however, it appears that there is little if any defect luminescence in any Ohmic contact metal for the 1 keV beam sampling near the surface in the upper AlGaN layer as shown in Figure 78. The marked location in Ohmic metal A indicates a possible indication of the formation of Y2 luminescence even prior to anneal. The intensity is extremely weak, however, despite the high incident beam currents and the luminescence is exhibited clearly in only one location of the map. This indicates the formation of the Y2 defect luminescence is due to a surface defect and that even with simple metal placement on the surface without an anneal, the defect can begin to form. The Ohmic metal was deposited in an e-beam metallization system and the kinetic energy of the metal atoms as they strike the surface may be enough to begin diffusion and disruption of the lattice at the surface.
Figure 97 – Low-temperature CL of F01 Ohmic alignment marks prior to Ohmic alloy annealing for all four Ohmic metals. The marked higher-intensity luminescence in the Ohmic A Y2 defect map may be an indication of Y2 defect formation prior to Ohmic contact anneal. A 1 keV, 1x10^{-9} A electron beam was used with a magnification of 1,000x.
In Figure 98, the Ohmic metal regions were investigated after the RTA. The same Y2 luminescence at ~50 meV below the GaN NBE is observed for metal A indicating the anneal provides the necessary energy for defect formation even at lower beam currents and deeper in the sample near the AlGaN/GaN interface. The Ohmic contacts appear differently post-anneal as seen in the figure. The final surface morphology varies greatly depending on the metal used and may be an indication of the uniformity of the metal islands diffused into the semiconductor, although studies on this were not done for these samples. Ohmic B, the Ir contact that behaved poorly in Ohmic contact tests, appears to have the smoothest morphology with small patches of rough morphology spaced at distant intervals. The other contacts appear rough with features in the surface at short intervals. AFM results indicate that Ohmic A has small features ~150 nm tall and ~250 nm across throughout the surface. Ohmic B consists of large dips and valleys in the rough portions that are ~340 nm tall and microns across as well as small surface features ~100 nm tall and ~500 nm across interspersed throughout the contact region. Ohmic C consists of a variety of features including large undulations ~150 nm tall extending from peak to valley across ~1.8 μm as well as smaller features ~80 nm in height and ~1 μm across. Finally, Ohmic D consists of tall features similar to those found in Ohmic A which are ~250 - 400 nm tall and ~1 μm across. The resulting RMS roughnesses are as follows: Ohmic A = 34.4 nm over a 5 μm x 5 μm square, Ohmic B = 69.1 nm, Ohmic C = 27.9 nm, and Ohmic D = 87.7 nm. When compared to the $f_T$ and $f_{\text{max}}$ for the devices, it appears the rougher contacts tend to produce poorer performing results over the contacts with a smoother surface roughness.
Figure 98 - Sample F01 post-Ohmic anneal. CL maps reveal some amount of Y2 defect luminescence for all metals, although metal A, Ni, produces the highest concentration of this defect emission. Also note the Ohmic metal off mesa does not exhibit strong Y2 defect luminescence. A 2 keV, 5x10^{-10} A electron beam was used with a magnification of 1,000x.
As expected, however, the Ohmic contacts containing Ni have the highest intensity Y2 defect luminescence concentrated around the Ohmic metal and only on the AlGaN device layer mesa. Ohmic B, Ir, and Ohmic D, Pt, also exhibit a similar Y2 luminescence, however, as seen in Figure 98. Interestingly, the GaN NBE intensity was extremely low in Ohmic D in the region shown in Figure 98 compared to the GaN NBE for the other Ohmic metals. In observing the samples post-RIE etch and gate fabrication, however, the Y2 defect luminescence appeared to be quenched.
CHAPTER 7.

OHMIC CONTACT INVESTIGATION AND EFFECT OF RIE ON BULK GaN

To further investigate the formation and characteristic of the Y2 defect and RIE etching on luminescence, GaN sample G01 was processed using typical 350/2333/500/200 Å Ti/Al/Ni/Au Ohmic contacts annealed at 850°C for 30 seconds in flowing nitrogen. A typical RIE mesa etch of half of the sample prior to processing allowed the comparison of the etched surface with the unetched, as-received surface luminescence. The pre-Ohmic CL shown in Figure 99 clearly demonstrates the effect of the RIE etch on the GaN surface quality. These scans were not normalized and the resulting CL shows a minor decrease in the GaN NBE with etching. As observed for the low-power etch of sample F01, the BL again increases. The YL, however, is greatly increased by the RIE processing, unlike the observations made for the low-power RIE of sample F01.
Figure 99 - Low-temperature (12 K) CL scans of bulk GaN sample G01 on RIE etched and unetched surfaces with a 2 keV, $5 \times 10^{-10}$ A electron beam.

Figure 100 shows the CASINO Monte Carlo simulation prediction of the electron beam penetration depth for GaN. The majority of scans recorded and shown were for a 2 keV electron beam whose peak luminescence would be acquired from a depth of ~20 nm. Scans were recorded, however, to the maximum of 25 keV as will be shown in the next figure.
Figure 100 – CASINO Monte Carlo simulation of GaN sample G01 illustrating the sampling depth with electron beam energy.

Figure 101 shows the sample spectra as a function of depth due to the sampling of the electron beam penetration. In the surface region of the sample at lower voltages, the region between the YL and BL increases in intensity up to 2 keV, or 20 nm. Also, the features that appear below the GaN NBE are more intense throughout the majority of the sample, with the spectra being nearly identical in the RIE and non-RIE regions only at a sample depth of between 200 and 1000 nm. This places the RIE damage region extent in the same range.
Figure 101 - Low-temperature CL analysis of sample G01 showing depth-dependence of the RIE damage with electron penetration depth. The damage extends to a total depth of between 100 and 1000 nm.

7.1 Post-Ohmic Anneal

Following the typical Ohmic anneal consisting of 850°C for 30 seconds in flowing nitrogen, the sample appears as shown in Figure 102. This particular set of curves has been normalized due to a difference in intensity from masking by the Ohmic contacts. As seen in this figure, the majority of the spectra has been restored to the previous sample conditions, including the GaN NBE, the features between the NBE and
BL, and the YL. The BL intensity, however, increases in the RIE exposed region post-anneal, as has been observed in samples C11 and F01 discussed previously.

Figure 102 - Low-temperature CL analysis of sample G01 post-Ohmic anneal for an electron beam of 2 keV at 1x10^-9 A.

CL maps of the various features shown in the CL line scan are shown in Figure 103. The GaN NBE at 3.48 eV is most intense at the edges of the visible defects. The centers of the defects do not show any luminiscence at any of the wavelengths and appear to be inactive, possibly due to a dislocation or inversion domain core causing non-radiative recombination. Finally, there does not appear to be any Y2-luminescence in either the CL line scan or the maps. A similar situation was found in both samples C11 and F01 prior to Ohmic processing.
After the Ohmic contacts were deposited, similar maps were produced at the edge of the Ohmic contacts to isolate any concentration of the Y2 luminescence to the Ohmic contact edge as shown in Figure 104. Similar to the previous scans, the GaN NBE is
slightly lower on the RIE etched sample while there is no indication of the Y2 defect luminescence prior to the Ohmic contact anneal.

Figure 104 - Post-Ohmic contact deposition CL maps of sample G01 with an electron beam of 2 keV, 1x10^-9 A at 3,000x.

Following the Ohmic contact anneal, image maps were taken to determine the presence of the Y2 luminescence as shown in Figure 105. It was found that the sample did not exhibit any luminescence accumulated at the edges of the Ohmic contacts. This is the same result as seen in both C11 and F01 on the RIE etched off-mesa GaN regions. In sample G01, however, the unetched regions were not affected by a potentially damaging RIE etch indicating the necessary role of AlGaN in forming this particular defect.

As mentioned previously, the RIE etch consisted of a standard mesa etch. This was composed of Cl₂, Ar, and He with a power setting of ~40 W and 145 V DC bias.
Due to the bias and energy of the ions, some of the constituents of the etch are likely to have been driven into the sample. The gas constituents, however, are not known to produce luminescence as impurities within GaN.

Figure 105 - Sample G01 CL maps post Ohmic anneal showing no visible accumulation of Y2 defects at the Ohmic contact edge for either RIE etched or unetched surfaces. A 2 keV, 1x10^-9 A electron beam was used at a magnification of 3,000x.

CL analysis of the unetched portion of sample G01 post-anneal is shown in Figure 106. The labels on the spectra indicate the regions analyzed in Figure 107. Particular
attention is made to the BL and features just below the GaN NBE in energy. These features display a clear spatial dependence in the image maps.

Figure 106 - Low-temperature CL of sample G01 post-anneal in the unetched region. The circles and labels indicate points of interest mapped in Figure 107.

Figure 107 shows slow-scan spectra maps taken in the unetched region of the sample post-anneal. The GaN NBE appears with higher intensity in the faceted regions surrounding the dislocation cores or inversion domains. This is most likely due to a higher GaN crystal quality in these regions as the dislocation core removes impurities and defects in the strain field surrounding the dislocation. In addition, the 3.44 eV luminescence intensity is increased in association with selected defects which are not seen in images utilizing a faster electron beam raster rate. The post-anneal BL band
appears blurred when compared to the pre-anneal case. This is most likely due to the anneal causing the defects responsible for BL to spread throughout adjacent sample regions at elevated temperatures.

![SEM images with CL spectra at different wavelengths](image)

Figure 107 – Low-temperature CL mapping of Sample G01 at a slow raster rate. A 7,500x magnification, 2 keV, 1x10⁻⁹ A electron beam was used to collect the images.

7.2 Results of AlGaN Layer Importance vs. GaN Only

The observation of the defect at ~50 meV lower than the GaN NBE is an indication of a possible mechanism of Ohmic contact formation. It is possible that an accumulation of defects aid in allowing charge to transfer through the device layers to the 2-DEG. This effect is not seen in the GaN G01 sample processed with Ti/Al/Ni/Au
Ohmic contacts. The AlGaN appears to play an important role in the formation of the defect level. This is possibly a result of the Al content itself or the interface between the AlGaN epilayer and the underlying GaN channel layer and the associated strain.
CHAPTER 8.

CONCLUSIONS AND FUTURE WORK

Au and Ag deposition on the non-polar cleaved GaN epilayers reveal the underlying physics of Schottky barrier formation on clean GaN surfaces. The technique of using core level shifts and secondary electron threshold measurements was shown to allow a means of monitoring both band-bending and work function during Schottky barrier formation. Similar experiments using additional metals as well as variations of the semiconductor surface would reveal further details of Schottky barrier formation physics. For example, non-polar, off-axis grown GaN epilayers could be cleaved to reveal the standard (0001) c-axis device layer upon which a similar study could be performed to determine the effects of the sample polarization on Schottky barrier formation in typical devices. Also, Ohmic metal deposition would reveal the underlying differences, on a nanometer-scale, of Ohmic contact formation which may provide insight into the existence of low work function patches and variations in the contact layer.

An investigation was made into the possible mechanism underlying current collapse as seen in devices fabricated on AlGaN/GaN. CL mapping studies revealed the existence of two defects, Y4 and Y7, that appear to be scattered throughout the GaN channel and buffer layers. Although it appears there is a slight increase in the defect luminescence with electrical stressing, it is still unclear if these particular defects are
playing a definite role in current collapse. Additional studies should be made to
determine the role of these defects, if any, in the actual current collapse as well as to
determine the source and mechanism of this luminescence in the devices.

The results from the C11 sample analysis reveal the correlation between surface
processing and final device characteristics. The sample processed by standard methods
resulted in consistent overall results. The annealed sample showed promising CL
signatures and moderate cleaning by AES, and the final devices performed well. The N₂
ion sputtered sample was effectively cleaned as determined by AES analysis, although
CL revealed extensive damage of the surface. The final anneal corrected much of this
damage as revealed by further CL analysis. The resulting devices were mostly non-
functioning with respect to f₁ and fₘₐₓ performance, but the less-sputtered regions show
promising results. Finally, the Ga-reflux sample produced poor results overall due to an
additional current leakage path and possible dual-Schottky barrier or low Schottky barrier
patches. Unfortunately, the thinner Au overlayer on the Schottky gate contacts cannot be
ruled out as a possible cause for the device failures during testing. Final device
performance for the two working devices revealed promise for this technique as well with
appropriate optimization.

My research has shown the possible effectiveness of various UHV surface
cleaning techniques on device performance. Varying the parameters of both the dual-
mask developing and sample cleaning techniques would allow further insight into the
optimum method to prepare GaN samples. For example, the ion sputter energy and time
correlation to final device processing should be investigated since the particular
parameters used in this study are simply a first trial. The amount of time used in making
the undercut of the dual-layer mask and resulting damage to the sample can be varied since for normal lift-off metal evaporation, a smaller undercut would suffice and the minimal damage may improve device response overall. The amount of Ga deposited during the Ga-reflux cleaning may greatly affect the sample surface quality and minimize the damage produced, although from my results, it appears the technique may be difficult to adapt to actual device processing due to the excessive leakage currents. Finally, the anneal temperatures and times should be investigated since it is expected the anneal should repair some of the damage in the crystal lattice and the CL results consistently show an increase in BL post-anneal.

Sample F01 demonstrated the effect of various Ohmic contact processing and RIE etch damage on device performance. In particular, the Ti/Al/Ni/Au Ohmic contact scheme typically used in AlGaN/GaN HEMT processing produced the best results in terms of specific contact resistance as well as final device performance overall. The RIE damage, however, affected the BL intensity the greatest causing an increase in this defect, even with the low power and DC bias used to etch the gate mask. Through electrical characterization, it was determined that the damage by the RIE yielded devices with poorer Schottky contacts as determined by the \( V_{th} \) of the final HEMTs, the gate I-V characteristics, and the FET family of curves for the devices.

A further investigation of RIE damage on GaN with sample G01 revealed that the mesa etch reduces the GaN NBE and increases defect luminescence in both the BL and YL bands. This is consistent with the results seen throughout processing F01 and C11. An interesting future study would involve identifying the structures found throughout the
sample surface and associating the defects or dislocations to the various changes in luminescence as observed in the low-temperature CL maps.

The Ohmic contact processing was determined to cause an increase in defect emission on the low-energy shoulder of the GaN NBE ~50 meV below the peak of the GaN NBE for samples C11 and F01. This defect luminescence has been referred to as Y2 luminescence and is believed to be associated with excitons bound to surface defects. The appearance of this particular defect most strongly in the Ni-based Ohmic contacts reveals the participation of Ni in the reaction forming this luminescence. Finally, two of the other three Ohmic contacts also weakly exhibited signs of the same defect formation surrounding the contact pads, revealing that the luminescence may be associated with the actual metal incorporation into the lattice and disruption of the lattice during the Ohmic alloy anneal. A possible future study would involve removing a portion of the Ohmic metal that is currently masking the underlying semiconductor surface to reveal the distribution of the defect under the contact. Using a focused ion beam (FIB) to etch to a particular depth just thin enough to allow photons to exit was considered, although etching too far would damage the contact and create new defects complicating the analysis. A wet chemical etch would most likely cause damage as well and the experiment requires further planning.

Studies on GaN sample G01 have revealed the role of the AlGaN layer in the ~50 meV Y2 defect level seen in samples F01 and C11. No observation was made of the defect on either the pre- or post-annealed surface which indicates that the epitaxial layer may be necessary for the formation of this defect as well. A similar study on bulk AlGaN
would determine the role of an epitaxial film and the associated strain and other characteristics as opposed to the AlGaN itself.

The C11 UHV surface preparation and cleaning study relied on a dual-layer mask consisting of Si₃N₄/SiO₂ etched using two different RIE etches to achieve an appropriate lift-off undercut. Although the initial idea for the mask was developed previously [26], the entire process was carefully studied and optimized to minimize the damage to the sample surface using extremely low power RIE etching in the final isotropic etch step while achieving the appropriate amount of undercut for the mask. The problem of the deposited metal adhering to the surface of the mask not allowing for good lift-off was solved with a wet-chemical etch utilizing acetic acid and ammonium fluoride. It is clear from the results obtained on both C11 and F01 that the mask etching produces damage detrimental to device performance, and a study to determine the optimum undercut etch that will clear the mask entirely while minimizing exposure time of the surface to the damaging ions should be studied prior to incorporating the etch into future projects.

As has been demonstrated through each sample analyzed, defects play an important role in the operation of devices. As emphasized throughout each chapter, the importance of localized defects near the surface, interfaces, and in specific regions of active devices has been shown to have important effects on final device performance. Nanometer-scale techniques capable of analyzing such defects are essential to the advancing of both future device processing as well as our understanding of the underlying physics of semiconductor devices.
APPENDIX

INTERCHANGEABLE EVAPORATOR DESIGN DIAGRAMS
As mentioned in Chapter 2, the details of an interchangeable source metal evaporation system similar to that described by Drummond et. al. [27] were essential to the investigation of Schottky contact formation on GaN. The following drawings detail the construction of the device which also utilized an off-the-shelf UHV bellows and two-conductor feed-through for electrical contact to the evaporator. The two halves of the evaporator are held together using 0-80 bolts insulated with alumina ceramic spacers. After thorough cleaning, each new mount is carefully outgassed in a separate UHV chamber prior to loading with the chosen metal. Au and Ag, used in my experiments, were slowly heated on the tungsten filaments to ensure wicking and retention of the source material. The completed, assembled Au evaporator as well as the mating transfer assembly that attaches to the transfer rod are shown in the three photos following the CAD drawings.
QTY: 2
MATERIAL: STAINLESS STEEL
ADVISOR: DR. BRILLSON

TAPPED 0-80(x2)

TAPPED 4-40

TAPPED 2-56(x2), DEPTH 0.10
VENT HOLE DIA 0.05

ø1.20

0.33

0.39

0.08

1.20

0.26

ø0.08

ø0.126

0.15

0.10

0.08

0.20

0.34

0.50

30°
QTY: 2
MATERIAL: HIGH PURITY LOW-OXYGEN COPPER
ADVISOR: DR. BRILLSON

SLIP FIT TO 0.25" COPPER ROD
QTY: 2
MATERIAL: STAINLESS STEEL
ADVISOR: DR. BRILLSON

TAPPED 4-40(X12)

Φ0.45
Φ0.25

0.06
0.10
0.28
0.10
0.30
0.10
0.48
0.20
QTY: 1
MATERIAL: STAINLESS STEEL
ADVISOR: DR. BRILLSON

TAPPED 4-40(X8)

END OF TWIST-LOCK GROOVE MAY BE ROUNDED

TWIST-LOCK GROOVES TO ALIGN TO BASE UNIT’S 4 2-56 POSTS

OSU/EMNLAB PART: EVAPORATOR TRANSFER COUPLER
NAME: WALKER, DENNIS

DRAWING NO.
LIST OF REFERENCES


