ADAPTIVE DIGITAL CALIBRATION TECHNIQUES FOR
HIGH SPEED, HIGH RESOLUTION SIGMA DELTA ADCS
FOR BROADBAND WIRELESS APPLICATIONS

DISSERTATION

Presented in Partial Fulfillment of the Requirements for

the Degree Doctor of Philosophy in the Graduate

School of The Ohio State University

By

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ABSTRACT

Analog to digital converters are the interface between the analog world and the digital domain where information is extracted from the signal, is processed and then interpreted. The performance of all electrical devices depends on this interface. As the electronic devices are evolving to more complex designs, requirements on A/D converters are becoming more stringent consequently. This thesis is focused on the design of high performance analog to digital converters for broadband wireless applications. In these systems A/D is a part of the receiver chain which its requirements are defined together with all other blocks of the receiver through system design. System designs for two future generations of mobile systems are done in this work. Convergence of WiMAX/WLAN is the first example that is studied in this thesis and is a multi-mode system that can revolutionize internet access inside metropolitan areas. 4th generation of mobile phones is the second system that is studied and includes the convergence of 3rd generation with WLAN systems.
These designs shed a light on the trade-offs in the design of a multi-standard broadband receivers. They also clarify how dynamic range and resolution of A/D trade-offs with the complexity of filtering and amplification blocks that precedes it in the receiver. Two designs of sigma delta A/D converters suitable for the above mentioned wireless systems are presented in this work. The two designs are given from the main categories of sigma delta ADCs i.e. single-loop and MASH architectures. Designs are done in TSMC 0.18um technology using 1.8 V supply. As the submicron technologies are unable to provide high performance analog designs without sacrificing power consumption, high performance analog to digital converters need a sort of calibration to achieve their required speed and accuracy. Although these calibration techniques can be done off-line during the start-up or the idle time of converter, e.g. the transmission time in TDD systems, background schemes are more desirable. In this thesis, different adaptive calibration techniques for sigma delta modulators are studied. Most of the previous work in this field is limited to the MASH type of sigma delta ADCs. A new adaptive technique is proposed that can be used for single-loop as well as MASH sigma delta converters. The proposed method is a fully-digital solution and does not add any complexity to the analog circuitry. Adaptive compensation of analog imperfections can be also applied to other types of analog to digital converters. Pipeline ADCs, for example, are the competitors of sigma delta converters in wireless applications. In pipeline ADCs, non-idealities present in the interstage gains can degrade the converter performance significantly. This thesis also presents a new technique for nonlinear calibration of pipeline ADCs.
To my dear parents Farideh, and Ali and my beloved husband Behrooz.
ACKNOWLEDGMENTS

My first thanks go to my advisor Professor Mohammed Ismail for all of his great support during my Ph.D. program, for letting me be a part of his VLSI group and for giving me guidance and helping me to build my future career. This research could not be completed without his support and encouragements.

I would like to thank Professor Steven Bibyk and Professor Oscar Takeshita to accept serving in my dissertation committee and for their helpful comments.

I wish to express my gratitude to Doug Garrity, my supervisor at Freescale Semiconductor where I spent a six-month internship. My internship was not only added up to my knowledge in the design of analog to digital converters, but it also provided me with insights and ideas for my future research.

I also wish to thank my fellow colleagues in Analog VLSI Lab of the Ohio State University for their friendships and their spiritual and technical support.

Part of this research was supported by Semiconductor Research Center (SRC) and I would like to thank them for sponsoring this research.

And finally, my deepest thanks belong to my husband, Behrooz for his incredible love and support.
VITA

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CHAPTER 1

INTRODUCTION

1.1. Motivation

Wireless communication systems have evolved tremendously during the last few years. They provide more services, higher quality of service and have larger coverage area than ever. Development in analog to digital converters has a significant impact on these systems. Idea of software radio where signal picked up by antenna is directly converted to digital using analog to digital converter is still further away in future. However, the technology trend is moving toward that direction where most of signal processing can be done in digital domain.

This trend pushes analog to digital converters to provide more resolution at higher speed and with lower power consumption. Among different types of Analog to Digital Converters (ADCs), sigma delta ADCs are especially attractive for wireless communication systems due to their lower power consumption which is due to the fact
that these converters are less sensitive to analog circuit imperfections and hence relaxed analog designs can be used that help to save power. This characteristic of sigma delta ADCs makes them very suitable for submicron technologies where high performance analog is hard to achieve. Insensitivity to analog imperfections is originated from a technique used in these ADCs called “noise shaping” which is used to push the quantization noise out of signal bandwidth. The same process also shapes the errors caused by the analog circuit non-idealities and hence makes the converter more robust to analog imperfections.

There are two approaches to implement sigma delta converters: switched-capacitor and continuous time. Although continuous time sigma delta modulators have become very popular recently for high speed applications, but the switched-capacitor ones are still dominant for low to medium speed applications. This thesis is focused on switched-capacitor implementation of sigma delta analog to digital converters.

However, as the wireless systems provide more broadband services, practical oversampling ratio in sigma delta ADCs becomes smaller and therefore noise-shaping can not be done very effectively. Therefore, analog circuit imperfections in broadband sigma delta ADCs can cause significant degradation in resolution. High performance ADCs need to use a calibration scheme to compensate for analog errors.

This research is focusing on calibration techniques for sigma delta converters with application in wireless communication systems.
1.2. Thesis Organization

The thesis is organized as follow: chapter 2 provides an introduction to wireless communication systems and their physical layer designs. Different design trade-offs in the system level are discussed here and the procedure for derivation of block specifications from the overall requirement of system is explained. Chapter 3 performs system design for two future generations of mobile system, WiMAX/ WLAN and 3G/WLAN. The requirements derived for analog to digital converter here are used in the following sections. An overview of the sigma delta ADC fundamentals and also different architectures for these converters are the subject of chapter 4. Material presented in this chapter will serve as the required background for chapter 5. Two different designs of sigma delta modulator for the multi-band 3G/WLAN systems are given in chapter 5. Designs are based on single-loop and MASH sigma delta ADCs and both are done in TSMC0.18 um technology. Pros and cons of each design are also presented in this chapter. Chapter 6 is dedicated to calibration techniques for sigma delta modulators. Different foreground and background as well as adaptive techniques are discussed in this chapter. A modification to an existing on-line correlation –based adaptive technique is presented. An innovative technique is also proposed based on active noise cancellation technique that can be used to remove the in-band quantization noise, thermal noise and any other additive noise from the output of sigma delta modulator. Adaptive techniques can be also used in other types of ADCs to compensate for analog circuits non-idealities. Chapter 7 of this thesis presents a new technique for calibration of pipeline converters. Thesis is concluded in chapter 8.
1.3. Research Contributions

The original contributions made by the author in this thesis are:

1. System design for the convergence of WiMAX and WLAN systems.

2. System design for the convergence of 3G (GSM/WCDMA) with WLAN systems.

3. Design of a single-loop multi-standard sigma delta modulator based on biquad filters for the 3G/WLAN applications.

4. Design of a MASH sigma delta modulators with optimized power consumption and additional digital calibration block for 3G/WLAN applications.

5. Propose a modification to the on-line correlation-based adaptive calibration techniques for sigma delta MASH ADCs.

6. Propose a new calibration method based on adaptive noise cancellation technique that can be used with any type of sigma delta converter.
CHAPTER 2

DESIGN OF MULTI-STANDARD WIRELESS RECEIVERS

2.1. Introduction

With the boom of communication systems starting in twentieth century, wireless systems and specifically handheld cell phones have enormously evolved in a short period of time. Excited with a huge available market, the wireless industry has been growing enormously and offers increasingly more services with lower prices to its customers. Demand for global roaming and having different services all in one compact handheld are feeding this huge market and also asking for multiple-standard wireless solutions.

Figure 2.1 shows an abstract scheme of the evolution of wireless systems. It starts with the first digital mobile phones that use GSM and EDGE standards. Although they outperform the first generation analog phones (not shown in the figure) but still are suitable for voice calls only. The increase demand for higher data rates and providing
more features rather than voice, result in the development of the latest generation of mobile networks which is CDMA system, also known as third generation (3G). These systems offer much higher data rate and capacity which make them suitable for high speed data applications. Along with the developments in mobile phones, wireless systems have another market to grow and that is Wireless Local Area Networks (WLAN) which provides computer users with wireless high speed data transfer.

3G mobile systems cover a wide range of several miles around their base stations and are part of Wireless Wide Area Networks (WWAN) that provide their users with access across cities, states and even entire country. WLAN access points, on the other hand, cover a range of 50-100 feet but with much higher data rates.

![Figure 2.1. Evolution of multi-standard wireless systems.](image-url)
Convergence of these two systems is especially attractive for notebook users who like to have the wide-area broadband access while away from their offices. In this thesis, fourth generation of wireless systems refers to converge of 3G and WLAN. Figure 2.1 also shows the WiMAX systems that will be covered in more detail in chapter 3 and are designed to provide broadband high speed access within the metropolitan areas.

In general, the basic motivations behind the development of different generations of wireless systems are to increase the data rate, expand the coverage area and to accommodate more features on the same device. In addition to offering different services, wireless transceivers are required to have little power consumption and smaller form factor to make them suitable for portable devices. Designing a multi-standard wireless system needs knowledge in both system and block level. Several factors need to be accounted for to make a compact, low power, and high performance solution for the specific wireless application.

This chapter discusses the important parameters of a transceiver and different steps in designing a multi-standard wireless system. The material covered in this chapter is generally applied for any architecture, however, a zero-IF transceiver is considered as an example since it has become the most popular solution for the new generation of highly integrated multi-standard systems.

2.2. System Design

The term “system design” is used to describe the derivation of the specifications for each block in the receiver and transmitter chain such that the whole transceiver complies with the country’s regulatory body (e.g. Federal Communications
Commission, FCC, inside the U.S.). Standards usually give the overall requirements such as range of frequency, sensitivity level for receiver and transmission mask for the transmitter and system design maps these specifications to the gain, noise and linearity requirements of different blocks as well as frequency planning for the frequency synthesizer. Efficient distribution of these specifications in the receiver or transmitter chain guarantees a low power, high performance and compact design.

2.3. Sensitivity

Sensitivity is the key parameter of a receiver and is defined as the minimum signal level in dBm that can be detected by the receiver with an acceptable signal-to-noise ratio. Standard specifies the required sensitivity for the receiver as well as either NF or the maximum allowable Bit Error Rate (BER). In either case the following equation gives the SNR or NF (depends on which one is not specified explicitly) [1]:

\[ P_{in,\text{min}} = -174 dBm/Hz + NF + 10 \log B + SNR_{\text{min}} \]  

(2.1)

![Figure 2.2. Block diagram of a zero-IF receiver (I-path only).](image)
The total receiver noise figure defined in equation (2.1) is made of the cascaded effect of the noise figures of different blocks in the receiver. Figure 2.2 shows a block diagram of the I-path in a general zero-IF receiver. As the figure shows seven different stages are cascaded from antenna to the final ADC.

Total NF is calculated from each block noise figure and gain according to Friis equation [1]:

\[
NF_{Total} = NF_{RF-SW} + \frac{NF_{RF-Filter} - 1}{G_{RF-SW}} + \frac{NF_{LNA} - 1}{G_{RF-SW}G_{RF-Filter}} + \ldots + \frac{NF_{ADC} - 1}{G_{RF-SW} \ldots G_{LP-Filter}}
\]  

(2.2)

where \( G \) is the available power gain.

SNR calculated from equation (2.1) should be treated as the Carrier to Noise plus Distortion Ratio (CNDR) at the backend of the receiver and needs to be large enough to keep the BER below a maximum value given by the standard. Important sources of noise and distortion are device noises, which are measured by block NF or block input referred noise, inter-modulation products between the blockers that are produced due to the block nonlinearities and PLL phase noise. Different components of noise and distortion that make the final value of CNDR are shown in figure 2.3. Each of these factors is analyzed in the next sections.

2.4. Noise Calculation

Each block contributes to the total noise because of the thermal noise of the resistors and thermal and flicker noise of the transistors. This noise is usually measured in terms of NF or the input referred noise of the block. NF is the ratio of SNR at the input of the block to the SNR at the output of the block and can be expressed as [2]:

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\[ NF = 10 \times \log \left( \frac{R_{in} + R_{eq}}{R_{in}} \right) \]  \hspace{1cm} (2.3) \\

where \( R_{in} \) is the source resistance or the output resistance of the preceding block in the receiver chain and \( R_{eq} \) is the equivalent thermal resistance. \( R_{eq} \) is then related to input referred noise with the following equation:

\[ R_{eq} = \frac{V_{n}^2}{4KTB} \]  \hspace{1cm} (2.4) \\

\( V_{n}^2 \) is the mean squared noise voltage in \( \text{V}^2/\text{Hz} \) and \( B \) is the bandwidth.

The problem with calculating NF using equation (2.3) is that it uses power gain instead of voltage gain. Baseband designers usually define voltage gain instead of power gain and converting the voltage gain to power gain needs the knowledge of input and output impedances of the component as shown in the following equation:

\[ V_{in} = \frac{R_{in}V_s}{R_{in} + R_s} \]  \hspace{1cm} (2.5) \\

\[ V_{out} = \frac{R_L}{R_L + R_{out}} \]  \hspace{1cm} (2.6) \\

\[ P_{in} = \frac{R_{in}V_s^2}{(R_{in} + R_s)^2} \]  \hspace{1cm} (2.7) \\

\[ P_{out} = \frac{R_LV_{out}^2}{(R_L + R_{out})^2} \]  \hspace{1cm} (2.8) \\

\[ G = \frac{P_{out}}{P_{in}} = A_v^2 \frac{R_L}{R_{in}} \left( \frac{R_{in} + R_s}{R_L + R_{out}} \right)^2 \]  \hspace{1cm} (2.9)
In above equations, $A_v$ is the voltage gain and values of voltages and impedances are shown in figure 2.4.

Power gain can be calculated easily for discrete components where they are usually matched to 50 ohm. For integrated components, however, the input and output impedances are not known a priori (in fact they are not usually matched impedances so that the design can have more flexibility to be optimized for power, noise and linearity).

For the above reasons, calculation of noise in this thesis is done based on input referred voltage noise of the blocks, equation (2-4), instead of noise figure, equation (2-3).
Figure 2.3. Components of noise and distortion in a wireless transceiver.

Figure 2.4. Power gain and voltage gain for a two port network.
2.5. Nonlinearity

In-band and out-of-band blockers generate inter-modulation products due to block nonlinearities. The inter-modulation products that lie inside the signal bandwidth raise the noise floor and can be seen as a noise source (refer to figure 2.3). Among all of these terms, second order and third order inter-modulation terms are usually the dominant ones and therefore specific parameters are defined to measure them.

Every two interfere terms with adjacent frequencies can generate a low frequency second order products that lies inside the signal bandwidth. Therefore to calculate the total second order product, every blocker needs to be considered. The magnitude of this inter-modulation term at the output of each block is calculated as [1]:

\[
V_{\text{2nd-order}}^{\text{rd-order}} = \frac{V_{\text{block}}^2}{\text{VIP2}} \times \text{Gain}
\]  \hspace{1cm} (2.5)

where \( \text{Gain} \) is the block gain, \( \text{VIP2} \) is the input referred IIP2 of the block and \( V_{\text{block}} \) is the magnitude of the in-band or out-of-band blocker.

If the two interferes are located at \( \omega_1 \) and \( \omega_2 \) then the third order inter-modulation products would be at \( 2\omega_1 - \omega_2 \) and \( 2\omega_2 - \omega_1 \). Only if these terms are inside the signal bandwidth, their contribution to the total noise and distortion would be important. Third order inter-modulation product is then calculated from the following equation [1]:

\[
V_{\text{3rd-order}}^{\text{rd-order}} = \frac{V_{\text{block}}^3}{\text{VIP3}^2} \times \text{Gain}
\]  \hspace{1cm} (2.6)
2.6. PLL Phase Noise

The other contribution to the total noise and distortion comes from PLL phase noise as it is shown in figure 2.3. This noise is due to the fact that in practice, frequency synthesizer does not generate a pure sinusoidal or cosine waveform for frequency translation of the signal. The fact that frequency synthesizer output has a phase uncertainty (phase noise) will produce noise in system through two different mechanism, reciprocal mixing and residual FM which are discussed in the following sections.

2.6.1 Reciprocal Mixing

PLL like other blocks in the receiver is susceptible to noise. Noise coming from different blocks in the PLL loop will change the amplitude and the frequency of the LO signal. The random variation in frequency due to the noise makes the LO output to deviate from a pure sinusoidal wave [1]. Instead of a single tone, the spectrum of LO output signal will show a skirt of frequencies around the fundamental component. At the mixer, desired signal and all the blockers (interferers) are down converted by the LO and due to this extra tail, their spectrum will overlap. Figure 2.4 illustrates this phenomenon.

The overlap causes a part of blocker to mix with the signal and hence the signal is corrupted with phase noise of the LO. This effect is called “reciprocal mixing”. When calculating the total receiver noise, in order to take the phase noise into account, the phase profile of the PLL should be known.
The following equation can be used to calculate the total noise due to “reciprocal mixing”:

\[
V_{PNRM} = S_{\text{blocker}} + PN(\Delta f_c) + 10 \times \log BW
\]  \hspace{1cm} (2.7)

During the system design, the phase profile of the PLL needs to be specified by using the above equation. The design starts with an assumption on \(PN(@1MHz)\), which is the phase noise in dBc/Hz measured at 1MHz offset. Based on this value, phase noise will be calculated at any frequency offset where the blockers are located and the resulting noise voltage \(V_{PNRM}\) will be calculated using equation (2-7).
2.6.2. Residual FM (In-Band Phase Noise)

Phase noise of the PLL also changes the phase of the carrier signal and cause phase error. The effect of in-band phase noise can be seen in the constellation diagram of the modulated signal. Figure 2.6 shows the constellation diagram of a QPSK system in the presence of the PLL phase noise. The deviation between the ideal vector and the real one on the constellation diagram can be modeled as a random signal with Gaussian distribution. The standard deviation of this random signal is equal to the RMS phase error of the PLL. If the RMS value of the phase error is large, it causes the signal to be detected erroneously and hence increases the BER. The phase noise specification would be tighter for higher order modulations (e.g. 16QAM, 64QAM,....) which have more compact constellation diagrams. The in-band phase noise is calculated as follow [3]:

\[
V_{PN IB} (dBV) = S_{bl ocker} (dBm) - 20 \cdot \log \frac{BW}{\sqrt{2} \sigma_f} 
\]

In the above equation \( \sigma_f \) is called the residual FM and is equal to:

\[
\sigma_f = \sqrt{2a(f_2 - f_1)} 
\]

for a PLL with the phase profile of: \( L_\phi(f) = \frac{a}{f^2} \)
2.7. Calculating Total SNDR

All the noise and distortion terms discussed in sections 2.4 to 2.6 are used to calculate the total SNDR (signal to noise plus distortion ratio) as follow:

\[
SNDR(dB) = 10 \times \log \left( \frac{S_{\text{signal}}}{V_{\text{Thermal}}^2 + V_{2n-\text{order}}^2 + V_{3rd-\text{order}}^2 + V_{\text{PNRM}}^2 + V_{\text{PNIB}}^2 + \ldots} \right)
\]

In addition to the major noise sources that discussed above, flicker noise and aliasing noise due to the low pass filtering at the baseband are also present. SNDR can be calculated at any block in the receiver chain. At the output of ADC, however, the value of SNDR should be more than the minimum value required for the maximum BER specified by the standard.
2.8. Selectivity

In addition to sensitivity, selectivity is another important parameter of any receiver. It is defined in the standard as the required carrier to interfere rejection ratio during the interference test. Due to the nonlinearity of the blocks, interferes will translate into the desired channel bandwidth and will be added up to the total noise. Hence, selectivity can be also considered in terms of its effect on sensitivity. In a zero-IF receiver, analog filtering is only done in RF (that filters out-of-band blockers) and at the Baseband. Filtering can be also done partially in digital domain. That eases the requirements on the analog filters. Pushing all the filtering to be done after ADC requires larger dynamic range in all the baseband blocks which in turn increases power consumption in these blocks.

2.9. Receiver Building Blocks

2.9.1. Low Noise Amplifier

Low noise amplifier is the first integrated block in RF front end. LNA needs to amplify a signal that can be as weak as few micro volts in the presence of strong interfere. At this stage, although the out of band interferers have been suppressed by the off-chip band-selection RF filter but the in-band interferers and adjacent channels are still strong. Therefore the linearity of LNA needs to be very good. Noise figure of LNA is also a critical parameter for the receiver. Since LNA is the first stage in the cascade of stages in the receiver chain, the noise figure of LNA is directly added to the noise figure of the whole receiver without being attenuated by any preceding gain stage. Hence, noise, linearity and gain will have a tough trade-off in the design of low
noise amplifier. In order to see how this trade-off is handled in the state-of-the-art designs, table 2.1 lists some of the work reported in the recent publications.

### 2.9.2. Mixer

Frequency translation of signal from RF to Baseband is done at mixer. In a zero-IF architecture since the problem of image does not exist, signal is transferred from RF to DC right after the LNA (figure 2.2). Mixer is therefore the second block in the receiver chain and should be designed with high linearity, low noise and based on the system design might need some conversion gain. Noise figure of mixer still plays an important role in the receiver NF since the only gain stage preceding it is LNA with a typical noise of 10~20 dB. Table 2.2 summarizes some of the state-of-the-art designs of mixer reported in ISSCC and CICC in the recent years.

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<td>2.4 (5.5)</td>
<td>0.18</td>
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<td>9.4</td>
<td>7.6</td>
<td>5.8</td>
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Table 2.1. State-of-the-art designs of low noise amplifiers.

19
Design of a mixer in zero-IF receivers is also critical for another reason and that is DC offset. DC offset is generated at the output of the mixer due to the finite isolation between the RF and LO ports. Because of this finite isolation, the LO signal can leak to the RF port and mixes with itself, the result would be a DC offset that corrupts the signal. In another scenario, a strong interfere from the RF port can also leak to the LO port of mixer, mixes with the original signal and make a large low frequency term at the output of mixer. The mentioned scenarios make static (constant) DC offset, however, dynamic DC offset is also possible. The LO signal that has leaked to the RF port can find its way to the antenna, get radiated from antenna and subsequently reflected from other moving objects, received by the antenna again and hence makes a time varying DC offset term as shown in figure 2.5.

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<td>13.9</td>
<td>11.9</td>
<td>-3</td>
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</table>

Table 2.2. State-of-the-art designs of CMOS mixers.
DC offset problem makes the isolation between the LO and RF ports of a mixer, an important design parameter. In addition to provide a large isolation between LO and RF port of the mixer, DC offset still needs to be treated using a specific technique. In broadband applications such as WLAN, little data is transferred near DC; therefore a DC notch (high pass) filter can be used to remove the DC offset. Digital cancellation of DC offset is also becoming popular where the DC term is extracted after the A/D and is subtracted from the mixer output using auxiliary D/A.

2.9.3. Frequency synthesizers

Frequency synthesizers are used to transfer the signal from one frequency to another. In zero-IF receivers frequency translation is from RF to DC. Complicated design of frequency synthesizers can generate a very clean output sinusoidal signal with a programmable frequency that can be a rational multiple of a fixed frequency. From the system design point of view, the important parameter of a PLL is its phase noise that shows how clean the generated sinusoidal signal is. Phase noise cause a frequency tail around the LO frequency that translates a part of interferes inside the signal band at the output of the mixer. Phase noise also generates an inaccuracy in the phase of the modulated signal that causes blurring in the constellation diagram and increases the bit error rate.

2.9.4. Variable Gain Amplifier (VGA)

 Receivers need to have some gain variability distributed through their RF and baseband blocks. This gain variability provides enough gain for the sensitivity
requirement of the receiver and at the same time avoids saturation of the receiver blocks.

![DC offset generation due to: (a) LO leakage, (b) interferer leakage, (c) radiation form antenna.](image)

Figure 2.7. DC offset generation due to: (a) LO leakage, (b) interferer leakage, (c) radiation from antenna.
when a strong signal is present. In the RF section, LNA has usually low and high gain modes that provides up to 20 or 30 dB gain variation.

The rest of the gain variation is provided by variable gain amplifier (VGA) blocks that are distributed through the baseband chain. In order to compute the required gain variation, dynamic range of the receiver is calculated as follow:

\[
DR_{RX} = P_{in,max} - P_{in,min} - KTBF + SNR_{min} + m_{arg in}
\]

where \( DR_{RX} \) is the dynamic range of the total receiver, \( P_{in,max} \) is the sensitivity level of receiver (minimum signal level at antenna), \( P_{in,min} \) is the maximum signal level at antenna, \( KTBF \) is the noise floor, \( SNR_{min} \) is the minimum required signal to noise ratio at the output of ADC and finally \( m_{arg in} \) is few dB margin (e.g. 6dB) to account for fading, DC offset, Baseband gain step error,…….

The minimum baseband gain control required is calculated as the total receiver dynamic range excluding the dynamic range of ADC and the amount of gain variability that is provided by the RF part, mainly LNA:

\[
VGA_{min, var} = DR_{RX} - DR_{ADC} - (G_{LNA,max} - G_{LNA, min})
\]

2.9.5. Filters

Filters are used to reject interferes and improve selectivity of the receiver. Filtering also relaxes the linearity and dynamic range requirement of the succeeding stages. In zero-IF receivers, part of the filtering can be done in digital domain and by decimation filters (providing a sigma delta ADC is used for analog to digital conversion). Postponing filtering until after ADC increases the required dynamic range and linearity of ADC. This issue is studied in next section.
2.9.6. Analog to digital converter

Analog to digital converter is the last block in the analog part of the receiver. The most important specifications for ADC are dynamic range, sampling frequency, and linearity that will be discussed here.

Linearity of the ADC is the limiting factor for the total receiver linearity since its IIP3 is divided by the gain of all its preceding stages. IIP3 of cascaded stages is determined from the IIP3 and gain of each individual stage as follow:

\[
\frac{1}{\text{IIP}_3^2} = \frac{1}{\text{IIP}_{3,1}^2} + \frac{G_1^2}{\text{IIP}_{3,2}^2} + \frac{G_1^2G_2^2}{\text{IIP}_{3,3}^2} + \ldots
\]  \hspace{2cm} (2.13)

Equation (2.13) shows that IIP3 of each stage is divided by the gain of its preceding stages and contributes to the total IIP3 and it can be easily shown that total IIP3 would be smaller than each of these scaled IIP3 contribution from each stage. For the last stage, IIP3 is divided by the gain of the whole receiver chain and therefore would result in the minimum term in determining the total IIP3. Since the nonlinearity causes the inter-modulation products and adds to the total distortion, filtering stages before ADC can relax its linearity requirement by attenuating interferes and hence minimizing the intermodulation products. IIP3 of ADC can be defined along with IIP3 of other stages as explained in section 2.5.

Another way of estimating the required IIP3 of ADC that is common in industry is depicted in figure 2.8 [15]. This figure plots the output third order intermodulation product and fundamental product versus input power. Shown on the x-axis is the channel signal level at the antenna which gets added by \( G_{RX} \), total gain of the receiver chain, to make the channel signal level at the input of ADC. Interferer level at antenna
is also added by $G_{RX}$ but is also subtracted from $L_{RX}$, which is the total attenuations imposed by the filters, to make the interferer level at the input of the ADC. Assuming that the minimum required SNR at the output of the ADC is only limited by the third order intermodulation products caused by this interferer, point A on the plot should be SNR dB above point B. It can be easily shown that IIP3 needs to satisfy the following inequality:

$$IIP_3 - P_{in} - G_{RX} + SNR_{\text{min}} \leq 3(IIP_3 - P_{in} - G_{RX} + L_{RX}) \tag{2.14}$$

where $P_{in}$ is the channel signal level at antenna, $G_{RX}$ is the total receiver gain, $SNR_{\text{min}}$ is the minimum required SNR at the output of ADC, $P_{in}$ is the highest interferer signal at antenna and $L_{RX}$ is the total attenuation of interferer due to filtering in the receiver chain.

Another important parameter of the ADC that should be determined during the system design is the sampling frequency. Choosing the sampling frequency of the ADC is a matter of trade-off between the complexity of the analog anti-aliasing filter and power consumption of the ADC. When the analog signal with bandwidth $f_b$ is sampled at ADC with sampling frequency of $f_s$, all the interferers elements present within the range of $f_b$ around multiples of $f_s$ are aliased back inside the signal bandwidth. The higher the sampling frequency the weaker these interference would be since they have already experienced large attenuations from analog filters. On the other hand, higher sampling frequency equals to more power consumption in analog to digital converter. Usually 4~8 oversampling ratio is the minimum value for the oversampling of the signal.
In addition to linearity, ADC needs to have enough dynamic range to pass all the signal and interferers present in its input without being saturated. Dynamic range of the ADC is then defined as the difference between the maximum and minimum signal strength at its input. More filtering of interferer will be done in the digital domain after the signal is converted by ADC.

Figure 2.8. Calculating the ADC required IIP3 [15].
Figure 2.9 shows different steps in calculating the dynamic range of ADC. It starts with defining the channel signal level at antenna which is given by standard. Adding the total gain of the receiver chain to this value, results in the signal level at the input of the ADC (shown by step 2 in figure 2.9).

In calculating the receiver gain, maximum gain of the variable gain stages should be considered. Noise level at the input of the ADC would be below this signal level by SNR. The value of SNR is the minimum value of signal to noise ratio that results in maximum BER specified in standard. Step 3 in figure 2.9 shows this procedure. ADC is supposed to have a quantization noise level well below the noise calculated in step 3 so that it does not degrade the signal to noise ratio of the receiver significantly.

The total noise of ADC (including its thermal noise and quantization noise) are set at least 10~20 dB below this level (shown in figure 2.9 as step 4). Noise level of ADC that is determined in step 4 shows the minimum signal that should be handled by ADC. The maximum signal level present at the input of ADC is due to the remaining interferes and is calculated by finding the peak value of the channel signal level present at ADC and adding the residual dynamic range to it.

Residual dynamic range is the difference between the channel signal and interferer after interferer gets attenuated by the filters. 6~10 dB headroom is also added to this value to account for the DC offset, Baseband gain step error, fading,……. Dynamic range is then determined as the difference between the full scale and the channel noise of ADC (step 4).
Figure 2.9. Calculating the ADC dynamic range [12].
CHAPTER 3

DESIGN EXAMPLES OF MULTI-STANDARD WIRELESS SYSTEMS

3.1 Introduction

This chapter is dedicated to two system design examples of multi-standard wireless systems. The material covered in chapter 2 is used here to design multi-standard receivers for future generation of mobile applications. Examples include convergence of WiMAX and WLAN as well as 3G and WLAN.

3.2 WiMAX/WLAN Convergence

3.2.1 Convergence of LAN\(^1\) and MAN\(^2\) Systems

Wireless systems and their corresponding standards can be categorized based on their range of applications and coverage area. As Figure 3.1 shows two of these systems that lie next to each other are local area networks that provide wireless internet access inside homes and offices and MAN systems (Metropolitan Area

\(^1\) Local Area Network
\(^2\) Metropolitan Network
Networks) that covers the wide range of a metropolitan area. Convergence of these two standards provides more flexibility for customers who can maintain their internet connection as they move in or out of their offices inside the cities. IEEE802.16 or as it is known in industry, WiMAX stands for “Worldwide Interoperability Microwave Access”, is introduced to provide broadband wireless access inside the metropolitan areas. WiMax can replace cables and DSLs to bring the internet to homes and offices and also can be used to backhaul the internet connections in rural areas [16].

Another important application of WiMax is introduced by IEEE802.16e that gives portability and mobility to this service. IEEE 802.16e fills the gap between very high data rate of Wireless Local Area Networks (WLAN) and high mobility of cellular systems. As the user roams between the WiFi hotspots, the WiMAX system can still maintain the internet connectivity. Another powerful feature of this standard is the scalability and configurability of the WiMax systems that provide just enough bandwidth for the users to satisfy their demands [17].

WiMax/WLAN systems need to work in the hostile environment of cellular phones and hence have tough blocker requirements similar to GSM systems while need to provide the quality of service which even exceeds that of WLAN (IEEE802.11a/g) [18]. Combination of these factors will put stringent requirements on system and block level. Since the mobile version of WiMAX is limited to licensed band, transmitted power in these bands can be increased to reach further distance than what WLAN can cover. Therefore instead of covering few hundred feet which is almost the diameter of a WLAN hotspot, WiMAX towers can transfer the signal as far
as 50 miles. Convergence of WiMAX and WLAN can also facilitate interoperability of services provided by different vendors.

![Global wireless standards categorized based on range of coverage](image)

**Figure 3.1** Global wireless standards categorized based on range of coverage [19].

### 3.2.2 Frequency Bands

Figure 3.2 shows the available RF bands that can be used for WiMAX applications [20]. Although both licensed and unlicensed bands are considered for WiMAX, IEEE802.16e has specified only the licensed bands for mobile application of WiMAX. In order to design a multi-standard receiver that covers WLAN (IEEE 802.11b/g) and WiMAX, the best choice for WiMAX frequency bands would be MMDS (2.5-2.69 GHz).
GHz, 2.7-2.9 GHz) and 3.4-3.6 GHz which are relatively close to the WLAN bands and hence this choice enables sharing between RF and baseband blocks in the multi-standard transceiver.

![Available frequency bands for WiMax systems](image)

Figure 3.2 Available frequency bands for WiMax systems [20].

3.2.3 Modulation and System Specifications

WiMAX uses OFDM (Orthogonal Frequency Division Multiplexing). OFDM has been used for DAB (Digital Audio Broadcasting) since 1960. It has been recently become popular for high speed bi-directional wireless data communication as a very bandwidth efficient method of transferring high data rate information. OFDM has
been used in Asymmetric Digital Subscriber Line (ADSL) as well as wireless systems such as IEEE 802.11a/g and WiMAX. OFDM can be seen as a special version of Frequency Division Multiplexing (FDM), as shown in Figure 3.3 [21], where different signals are transferred on different frequency bands, called subcarriers. Subcarriers are separated from each other by guard bands. OFDM uses the available bandwidth more efficiently by letting the subcarriers to overlap. In order to avoid overlap between the data carried by these subcarriers, the frequencies are chosen to be perpendicular in mathematical sense (Figure 3.3 (b)). The different subcarriers are then demodulated by Discrete Fourier Transform (DFT) in receiver.

![Figure 3.3](image.png)

(a) FDM with 6 subcarriers

(b) OFDM with 6 subcarriers

Figure 3.3 (a) FDM with 6 subcarriers using filters and (b) OFDM with 6 orthogonal subcarriers overlapped in frequency domain.
In WiMax, signal bandwidth can be any multiple of 125 KHz between 1.25MHz and 20 MHz. Number of subcarriers, however, is fixed and is equal to 256. Subcarrier symbol time therefore will decrease as the signal bandwidth increases and makes the system more sensitive to the phase noise of the oscillator [22].

Data transferred on each subcarrier is also modulated. In WiMax, signal modulation can adaptively change among BPSK, QPSK, 16QAM and 64QAM to optimize the data rate. When the link quality is good enough, the more complex modulations are used to increase the data rate. For the WiMax/ WLAN system designed here, a 20 MHz bandwidth is chosen so that both of standards have the same signal bandwidth. Table 3.1 shows some of the key system parameters of WiMAX system.

As specified by the standard, BER (Bit Error Rate) should be less than $10^{-6}$ which corresponds to 18dB SNR for 64QAM signal. NF (Noise Figure) is also specified by the standard to be 7dB and therefore sensitivity of the receiver can be calculated using the following equation [22]:

$$P_{in,min} = -102 + SNR_{RX} + 10 \times \log(f_s \frac{N_{used}}{N_{FFT}} \frac{N_{subchannels}}{16})$$

(3.1)

where, $SNR_{RX}$ is the receiver SNR specified in the standard and depends on the modulation scheme and coding rate, $f_s$ is the sampling frequency in MHz, $N_{used}$ is the number of subcarriers that are used to carry the information and $N_{FFT}$ is the total
number of subcarriers. \( N_{\text{subchannel}} \) is the number of subchannels used in OFDMA systems.

Sampling frequency is calculated as:

\[
f_s = \text{floor} \left( \frac{nBW}{8000} \right)
\]

In the above equation, \( n \) is a constant depends on the bandwidth. For bandwidths which are a multiple of 2MHz the value of \( \frac{57}{50} \) is given by standard. The calculated values for sensitivity are given in Table 3.1.

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<td>256</td>
<td>200</td>
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Table 3.1 Key system parameters of WiMAX system.

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3 Orthogonal Frequency Multiplexing Access (OFDMA) is a multiple access technique where different subcarriers are assigned to different users.
3.2.4 Blocking Profile

Every standard specifies the hostile environment where the receiver is supposed to work in by specifying a set of tests called interfere tests. In these tests, the receiver needs to provide a minimum BER in presence of other interferes which their strengths are also mentioned in standard. IEEE802.16 standard specifies the receiver adjacent and alternate channel rejection requirements. These requirements are more stringent for a 64QAM with 3/4 coding ration; hence, only this case is considered in this design.

Adjacent channel and alternate channel rejection should be measured under minimum and maximum signal strengths. The interference tests are depicted in Figure 3.4 where three scenarios are shown: a weak signal with weak interferer (a), strong signal with strong interferer (b) and finally weak signal and strong interferer (c). Among them (c) imposes the hardest trade-off between noise and linearity. The required carrier to noise ratio (CNR) given in table 3.1 should be satisfied under all interferes tests. The blocker profile for IEEE 802.11b/g is shown in Figure 3.5. As it has been illustrated in this figure, the difference between the strength of signal and interferer in WLAN is more than WiMAX however the requirement of BER is more relaxed (10^-3 compared to 10^-6 in WiMAX). That makes the overall requirement on both systems close to each other and helps to achieve a multi-standard WiMAX/WLAN receiver with maximum hardware share.
Figure 3.4 Adjacent and alternate channel interferer tests in IEEE802.16.

Figure 3.5 IEEE802.11b/g blockers profile
3.2.5 Receiver Architecture

Among the different architectures for receivers, zero-IF has been the most popular one in multi-standard designs due to its high level of integration and low power consumption. Zero-IF architecture removes the need for image rejection filters which need to be implemented off-chip. However, problems of zero-IF architecture, i.e. DC offset and sensitivity to I/Q mismatch shall be addressed carefully. A summary of the system specifications in WiMAX and WLAN (IEEE 802.11b) are given in Table 3.2. Based on system requirements, link budget design was done using Excel spread sheets and specifications for individual block in the receiver chain were derived. Excel sheets for this system design is given in Appendix A.

<table>
<thead>
<tr>
<th>Standard</th>
<th>IEEE 802.11b/g</th>
<th>IEEE 802.16</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency Bands</td>
<td>2.4~2.4835 GHz</td>
<td>2.5<del>2.69, 2.7</del>2.9, 3.4~3.6</td>
</tr>
<tr>
<td>Channel Bandwidth</td>
<td>22 MHz</td>
<td>20 MHz</td>
</tr>
<tr>
<td>Modulation scheme</td>
<td>DBPSK, DQPSK, QPSK</td>
<td>BPSK, QPSK, 16QAM, 64QAM</td>
</tr>
<tr>
<td>Multiple Access</td>
<td>DSSS, CCK</td>
<td>OFDM</td>
</tr>
<tr>
<td>QoS</td>
<td>FER&lt;8*10^{-2} (BER&lt;10^{-3})</td>
<td>BER&lt;10^{-6}</td>
</tr>
</tbody>
</table>

Table 3.2 System specifications of WLAN and WiMAX
Figure 3.6 shows a block diagram of the proposed zero-IF transceiver. A multimode RF switch is placed right after the antenna to choose among the different standards and also between reception and transmission mode for TDD. According to IEEE802.16, WiMAX systems can use TDD or FDD duplexing method. An RF filter is also used to extract the relevant RF band. Two different LNAs are used for WLAN and WiMAX so that the relatively narrowband design of LNA leave room for optimization for noise and linearity. Mixers as well as whole baseband chain are shared between the two standards. Two filters are used before and after VGA to increase the selectivity of the receiver and relax the linearity requirements of VGA as well as ADC. Block specifications are driven based on the method described in chapter 2 and the results are summarized in Table 3.3. Figure 3.7 and 3.8 show different signal levels at the output of each block in the receiver chain for WiMAX and WLAN case respectively.

<table>
<thead>
<tr>
<th></th>
<th>RF-Filter</th>
<th>LNA</th>
<th>Mixer</th>
<th>Filter</th>
<th>VGA</th>
<th>Filter</th>
<th>ADC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain high/low [dB]</td>
<td>-1.5</td>
<td>18/0</td>
<td>10/5</td>
<td>-3</td>
<td>50/20</td>
<td>-3</td>
<td>0</td>
</tr>
<tr>
<td>IIP3 [dBm]</td>
<td>53</td>
<td>-7</td>
<td>8.6</td>
<td>12</td>
<td>12</td>
<td>12</td>
<td>22.5</td>
</tr>
<tr>
<td>IIP2 [dBm]</td>
<td>80</td>
<td>29.9</td>
<td>64.5</td>
<td>64.5</td>
<td>64.5</td>
<td>64.5</td>
<td>75</td>
</tr>
<tr>
<td>Block Noise [v/Hz^0.5]</td>
<td>4.5E-10</td>
<td>3.50E-10</td>
<td>1.00E-9</td>
<td>1.00E-9</td>
<td>1.00E-9</td>
<td>1.00E-9</td>
<td>1.00E-9</td>
</tr>
<tr>
<td>ADC Dynamic Range [dB]</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>55</td>
</tr>
</tbody>
</table>

Table 3.3 Block requirements for zero-IF WiMAX/WLAN receiver.
Figure 3.6 Block diagram of the proposed zero-IF transceiver for WiMAX/WLAN.

Figure 3.7 Different signal levels in proposed zero-IF receiver for WiMAX system.
Figure 3.8 Different signal levels in proposed zero-IF receiver for WLAN system.

### 3.2.6 DC Offset Cancellation in WiMAX

DC Offset is one of the important challenges in zero-IF architecture. Usually DC offset is removed by high pass filtering the signal. This method can be easily used for WLAN where the information at DC is not significant. In IEEE 802.11b, the 22 MHz channel bandwidth is fully used to carry the information, but if the corner frequency of the Notch filter is \(0.1\) of the data rate, the increase in BER would be insignificant [23].

In WiMAX, however, using 256FFT OFDM makes a small subcarrier spacing (90 KHz for a 20 MHz bandwidth). Such a small cut-off frequency results in a long
settling time during the transients (e.g. TX/RX switching or switching between different modes). The cut-off frequency can be selected higher during the preamble for fast settling time. Another problem is that the drift of filter center frequency with respect to the LO frequency will result in undesired filtering of the near-zero subcarriers which degrade the BER significantly. This problem can be removed by using a mixed mode AFC (Automatic Frequency Correction) [24].

Analog calibration method can be also used to tune the cut-off frequency of the Notch filter that is responsible for removing DC offset. In [25], a GmC filter is used to extract the DC offset and subtract it from the output of the mixer. The diagram of the DC extractor is shown in Figure 3.9. The cut-off frequency of the filter is tuned by changing the resistor or capacitor of the filter. This method is used for Bluetooth and 802.11b and could provide as low as 1KHz cut-off frequency for Bluetooth application.

![Figure 3.9 DC Offset Cancellation](image)

Figure 3.9 DC Offset Cancellation [25]
Figure 3.10 shows the OFDM channel in WiMAX. It uses 256 subcarriers from which 192 carry the data. If all the 192 available data carriers are used, the carrier spacing of 90 KHz for a 20 MHz bandwidth is resulted that would force very stringent requirements on PLL phase noise and also need a high Q high pass filter for DC offset cancellation. On the other hand, using a part of subcarriers and not all will ease the requirements on PLL phase noise and DC cancellation at the price of lower data rate. Using 192 data carriers with 64QAM modulation can provide data rate of 100Msps which is almost twice the maximum data rate available in WLAN (54Msps). Therefore, there is a trade-off between number of used subcarriers and data rate.

Figure 3.10. 256-FFT OFDM symbols in WiMAX shown in frequency domain.
3.3 Fourth Generation of Cellular Phones (4G)

3.3.1 Introduction

First generation of phones (1G) was analog devices which were based on a large number of similar but non-compatible technologies. They offered a limited range of services mainly voice and were based on those of fixed telephone networks.

Second generation (2G), which includes GSM standard and its improved versions of that, employs digital modulation and offers higher data rates and better quality of service but still are used for transferring voice and little extra services were added to the newer versions of them.

Cellular phones more evolved to third generation (3G) which is the latest development in mobile systems. 3G includes WCDMA systems that outperform the previous GSM standards in terms of data rates and also variability of services. WCDMA systems are more spectrum efficient than 2G systems. In addition to increased capacity they also have advantages in terms of signal quality, security, provision of real data services, and international roaming.

The intent of fourth generation (4G) terminals is to provide seamless global mobility as well as global compatibility with chosen access technologies such as wireless local area networks, cellular, and satellite systems. One technical challenge to the advent of seamless global-terminal mobility is the difficulty in achieving a common global-frequency plan. In every world region, at least part of the necessary spectrum is already allocated for other radio services. Hence the 4G is possible through the communication systems that can support different frequency bands under
different standards. The flexibility and adjustability are the key features of these multi-standard systems and system design is playing an important role in achieving these.

This section is dedicated to the system design of a 4G cellular system that supports GSM, WCDMA and WLAN standards. This multi-standard system provides its users with wireless telephony as well as internet connection whenever the user enters a WLAN hot spot zone. The specification derived here for the analog to digital converter will be used later on in chapter 5 to illustrate two design of sigma delta modulator.

### 3.3.2 System Specifications

Figure 3.11 below shows the frequency bands dedicated to these standards and table 3.4 summarizes the key system parameters. Sensitivity levels and blocking profiles are shown in figures 3.12 through 3.14 for GSM, WCDMA, and IEEE 802.11b respectively.

![Figure 3.11 Frequency bands for 3G and WLAN standards.](image)

45
<table>
<thead>
<tr>
<th>Standard</th>
<th>Multiple Access Method</th>
<th>Duplex Method</th>
<th>Modulation</th>
<th>Channel Bit Rate</th>
<th>Channel Bandwidth</th>
<th>Channel Spacing</th>
</tr>
</thead>
<tbody>
<tr>
<td>GSM(^4)</td>
<td>TDMA/FDM</td>
<td>FDD</td>
<td>GMSK</td>
<td>270 kbps</td>
<td>200 KHz</td>
<td>200 KHz</td>
</tr>
<tr>
<td>WCDMA</td>
<td>CDMA/FDM</td>
<td>FDD</td>
<td>QPSK/OQPSK</td>
<td>1.22 Mbps</td>
<td>3.84 MHz</td>
<td>5 MHz</td>
</tr>
<tr>
<td>IEEE 802.11b</td>
<td>CSMA/CA(^5)</td>
<td>TDD</td>
<td>DBPSK, DQPSK, CCK(^6)</td>
<td>1,2,5.5,11</td>
<td>20 MHz</td>
<td>25MHz</td>
</tr>
</tbody>
</table>

Table 3.4 Key system parameters for 3G and WLAN standards.

---

4 From different GSM standard, PCS1900 which covers 1930-1990MHz is considered here.
5 Carrier Sense Multiple Access with Collision Avoidance
6 Complementary Code Keying

Figure 3.12 Blocking profile for GSM 900 [2].
Figure 3.13 Blocking profile for WCDMA standard [3].

Figure 3.14 Blocking profile for IEEE 802.11b [3].
3.3.3 Receiver Architecture

As it has been discussed in the previous section for a WiMAX/WLAN system, zero-IF architecture is the best choice for a fully integrated compact multi-standard radio. However, due to the relatively low bandwidth of channel in GSM, 200 KHz, any kind of DC offset cancellation would take out a considerable amount of information too. Therefore, a low-IF receiver would be a better option for GSM. Although low-IF architectures do not have the problem of DC offset and flicker noise of zero-IF receivers but image rejection would be very challenging especially when very low IF frequency is applied. Figure 3.15 illustrates the problem of image and image rejection in low-IF receiver. Figure 3.15 (a) shows that image is any interferer present at $2\omega_{IF}$ of the desired channel. This interferer is then translated into the signal band after down-conversion as it is shown in figure 3.15 (b). Figure 3.15 (c) depicts the filtering that is necessary before down conversion to remove the image signal.

Choosing the IF frequency imposes a design trade-off between the difficulty of the image rejection and simplicity of the circuit after the down-conversion. If a very low-IF is chosen then the signal is almost translated to DC and the circuit after the down-conversion can be considered as a baseband chain with low pass filters to remove remaining interferers and low pass analog to digital converter, however very low IF needs a very sharp image rejection filter since the distance between the desired channel and image ($2\omega_{IF}$) is now very small.

A very low-IF is definitely our desired choice for the multi-standard receiver since then GSM can share the baseband with WCDMA and WLAN that use zero-IF
architecture. By choosing $\omega_{IF}$ equal to 100 KHz, the problem of image rejection is also solved thanks to the “spurious free response” of the GSM. As the blocking profile of GSM drawn in figure 3.12 shows, there is no blocker present at 200 KHz which makes a very relaxed requirement on image rejection at this frequency.

In order to extract the signal after the down-conversion in GSM, polyphase filters can be used to select the signal and reject the image. Polyphase filters have asymmetric frequency response that can be seen as the frequency response of a low pass filter shifted by a constant value. Therefore, they can be used to pass the desired channel which is now located between 0 to 200 KHz.

A zero-IF/Low-IF configurable receiver is chosen for the 4G radio with low-IF mode working for GSM and WCDMA and zero-IF structure for WLAN. Figure 3.16 depicts the proposed architecture for the multi-standard receiver. The Excel sheet used for system calculation of this receiver is brought in Appendix B. Table 3.5 and 3.6 summarizes the specification of different blocks as well as detailed requirements of ADC in the proposed 4G system respectively.
Figure 3.15 Problem of image and image rejection in low-IF receivers.
Figure 3.16 Multi-standard receiver architecture for GSM/WCDMA/WLAN.
Table 3.5 Block specifications for multi-standard GSM/WCDMA/WLAN receiver.

<table>
<thead>
<tr>
<th>Standard</th>
<th>Channel Bandwidth</th>
<th>Clock Frequency</th>
<th>Oversampling Ratio</th>
<th>Required Dynamic Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>WCDMA</td>
<td>3.84 MHz</td>
<td>30.72 MHz</td>
<td>8</td>
<td>52 dB</td>
</tr>
<tr>
<td>GSM</td>
<td>200 KHz</td>
<td>51.2 MHz</td>
<td>128</td>
<td>70 dB</td>
</tr>
<tr>
<td>WLAN (11.b)</td>
<td>22 MHz</td>
<td>88 MHz</td>
<td>4</td>
<td>51 dB</td>
</tr>
</tbody>
</table>

Table 3.6 Specifications for analog to digital converter in the proposed GSM/WCDMA/WLAN receiver.
CHAPTER 4

HIGH SPEED HIGH RESOLUTION SIGMA DELTA ADCs

4.1 Introduction

Analog to digital converters are the interface between the real world which is analog and the digital world where the information buried in signal is extracted, processed, and interpreted. As the electronic systems become more complicated, they impose more stringent requirements on analog to digital converters. In wireless communication systems for example having variety of services (i.e. voice, video, internet,...) on a single handheld cell phone requires large signal bandwidth to transfer higher data rates and providing these services inside a hostile metropolitan area means higher resolution(dynamic range) for ADCs. Analog to digital converters, therefore, are becoming more demanding in resolution and speed. As the battery life time for the portable devices is also a crucial factor, all of these should be achieved with low power consumption. Among different techniques of analog to digital
conversion, oversampling sigma-delta ADCs have found their place in many applications. Although these converters are originally used for high resolution low to medium speed applications such as audio and sensors, but many work has been done in recent years to improve their performance for higher speed applications. Wireless communication systems are particularly interested in sigma delta ADCs that can accomplish analog to digital conversion with much lower power compared to Nyquist rate ADCs such as pipeline.

Figure 4.1 illustrates the resolution-bandwidth requirements for analog to digital converters in different wireless standards. Graph also shows the range of sigma delta application.
4.2. Fundamentals of Sigma Delta ADC

Sigma delta ADCs use oversampling and noise shaping to get more resolution out of a coarse quantizer. Both of these techniques can reduce the sensitivity of the total ADC to the nonidealities of the analog circuitry. Unlike the Nyquist rate ADCs where the accuracy of the total converter is directly determined by the accuracy of the analog circuitry, noise shaping and oversampling can reduce this dependency and relax the requirements on analog part which in turn helps to reduce the power consumption of the converter significantly.

Any analog to digital conversion consists of sampling and quantization where continuous signal first is quantized in time by a sampling circuit and then becomes discrete in amplitude by a quantizer. This process is illustrated in figure (4.2). Although an ideal sampling process does not generate any error, quantization inherently adds some error due to the fact that infinite possible values of amplitude are mapped to a finite number of quantization levels.

When the input signal is fairly dynamic, this error resembles a uniformly distributed white noise with its amplitude changing randomly between +/-\(\Delta/2\) (\(\Delta\) is called the quantization level). Therefore, quantization noise has a flat spectrum spreading from zero to the sampling frequency. Figure (4.3) shows the probability density function and the power spectral density of this noise. For a sinusoidal input to the quantizer, the ratio between signal power and this quantization noise is given by:

\[
SNR = 1.76 + 6.02B
\]  
(4.1)
From figure 4.3 (b) the total quantization noise can be calculated as the integral of the power spectral density:

\[
e_q^2 = \frac{f_s}{2} \int_{-f_s/2}^{f_s/2} S_q(f) df = \frac{\Delta^2}{12}
\]  

(4.2)

Equation (4.2) shows that the total power of quantization noise is constant and only depends on the quantization level which itself is determined by the full-scale voltage of the quantizer and its resolution.

Figure 4.2 Sampling and quantization in a general analog to digital converter.
Figure 4.3 Probability density function (a) and power spectral density (b) of the quantization noise.

**Oversampling**: Nyquist theorem requires that the sampling frequency be at least twice the signal bandwidth to prevent the aliasing errors. As it is shown in equation (4.2), total power of the quantization noise of a quantizer is constant and depends only on the quantization level. If the signal is then sampled with a high sampling frequency (much larger than the minimum required by the Nyquist theorem), the constant power of quantization noise will spread over a wider range and hence the amount of the noise that lies inside the signal bandwidth would be decreased proportional to the sampling frequency. This technique is called oversampling. Oversampling increases the signal
to quantization ratio by 3dB for each doubling of sampling frequency and is expressed in the following equations:

\[ f_N = 2f_b \]  
(4.3)

\[ OSR = \frac{f_s}{f_N} \]  
(4.4)

\[ SNR = 1.76 + 6.02B + 10\log(OSR) \text{ [dB]} \]  
(4.5)

**Noise-shaping:** Although oversampling can decrease the quantization noise, but only few dB improvement is achieved with the price of doubling the sampling frequency which almost doubles the power consumption too. Quantization noise can be decreased more effectively by using noise shaping. Noise shaping uses analog filters to high pass the quantization noise and push it outside the signal bandwidth. This is done through using a feedback loop around the quantizer and also an analog filter inside the loop which is designed to reject the quantization noise inside the signal bandwidth while maintaining minimum distortion to the signal.

General block diagram of a sigma delta ADC is shown in figure (4.4). Due to the use of noise-shaping and oversampling, sigma delta ADCs also need post-processing stages which include low pass filtering and decimation. In addition to the sigma delta modulator, this figure also includes the anti-aliasing filter and the low pass filtering and decimation. Design of a sigma delta ADC is therefore an example of a mixed signal design. It is a fairly complex system that needs to be modeled at different stages of the design with different levels of abstraction.

Loop filter, H(z), in its simplest way, can be an integrator with transfer function:
\[ H(z) = \frac{z^{-1}}{1 - z^{-1}} \]  \hspace{1cm} (4.6)

Figure 4.4 Block diagram of a sigma delta ADC.

Quantization noise transfer function would be:

\[ NTF(z) = \frac{Y(z)}{Q(z)} = 1 - z^{-1} \]  \hspace{1cm} (4.7)

and the signal transfer function:

\[ STF(z) = \frac{Y(z)}{X(z)} = z^{-1} \]  \hspace{1cm} (4.8)

Therefore, the modulator high passes the quantization noise while only delays the signal by one sample. In order to suppress the quantization noise even more a higher
order loop filter can be used in the loop. In an \( n \)th order modulator signal and noise transfer functions can be calculated as:

\[
STF(z) = z^{-n}
\]

(4.9)

\[
NTF(z) = (1 - z^{-1})^n
\]

(4.10)

The peak signal to quantization noise for an \( n \)th order sigma delta modulator is given by:

\[
SNR_p = \frac{3\pi}{2} (2^B - 1)^2 (2n + 1) \left(\frac{OSR}{\pi}\right)^{2n+1}
\]

(4.11)

where \( B \) is the quantizer resolution in bits, \( n \) is the order of the filter and \( OSR \) is the oversampling ratio as defined by equation (4.4). Figure (4.5) plots SNR as a function of oversampling ratio and filter order. Oversampling ratio is chosen within the range of 4 to 64 which is the reasonable value for a broadband application. Plot is drawn for \( B=1 \) which means a single-bit or two level quantizer. This is the common case although not necessarily true for most of MASH structure which will be covered in more detail in next section. Filter order is chosen between 1 and 6. Plot clearly shows the fact that SNR is increased more significantly with filter order when OSR is high. For lower OSR increasing the filter order results in a very gradual increase in SNR. As Figure (4.5) illustrates the general case for MASH sigma delta ADCs, it can be concluded that without a high enough oversampling ratio, increasing the filter order does not improve SNR that much and it only leads to larger die size and more power consumption.

Figure (4.6) plots the SNR as a function of oversampling ratio and quantizer resolution. SNR values are calculated for a second order filter. This case represents the
single loop sigma delta modulators where a second order filter is usually used for stability.

The graph shows that increasing quantizer resolution leads to a considerable improvement in signal to noise ratio for all possible oversampling ratios. Using more bits in quantizer also helps to stabilize the feedback loop and let more aggressive noise shaping be used without sacrificing stability. Advantages of multi-bit modulators are discussed in more detail in next section.

Figure 4.5 SNR as a function of oversampling ratio and filter order for a one bit quantizer (B=1)
4.3. Decimation in Sigma Delta ADCs

As it was explained in previous section, a sigma delta modulator uses oversampling and noise shaping to get a high resolution digital output word by using a coarse quantizer. The output of a sigma delta modulator is then a short length digital word (equal to the resolution of the coarse quantizer, probably few bits) but sampled at a much higher frequency than the Nyquist rate. It also contains quantization noise which is shaped out of signal bandwidth and hence has large value in higher frequencies.

![SNR as a function of oversampling ratio and quantizer resolution for a 2nd order modulator](image)

Figure 4.6 SNR as a function of oversampling ratio and quantizer resolution for a 2\textsuperscript{nd} order modulator (n=2)
Hence, the output of the sigma delta modulator needs to be low pass filtered and decimated down to the Nyquist rate. Decimation should increase the length of the digital word while maintaining the resolution. It was shown by Candy [26] that sinc filters with response of \( \sin c^k(f) \) are suitable for decimating the sigma delta output down to four times the Nyquist rate. Further reduction of the sampling frequency is better done with filters that have sharper roll-off at the edge of Baseband. If the decimation filters does not have a sharp transition, the amount of the quantization noise that lies from the edge of signal bandwidth to the filter stop-band will alias back inside the signal bandwidth and ruin the signal to noise ratio.

A \( k^{\text{th}} \) order sinc filter has the frequency response:

\[
H(f) = \left( \frac{\sin c(Nf / f_s)}{\sin c(f / f_s)} \right)^K
\]

(4-12)

where \( N \) is the decimation factor, and \( K \) is the filter order.

Candy [26] showed that if \( K = l \) (where \( l \) is the modulator order), then decimation increases the noise power by \( N \) times but if \( K = l + 1 \) (filter order is at least one more than the modulator order), then the increase in base-band noise is below 0.25 dB.

### 4.4. Single Loop vs. MASH Sigma Delta

As the equation (4.11) shows, signal to noise ratio of a sigma delta modulator can be increased by increasing the order of the loop filter. If the order of the filter is increased by just cascading integrators inside the modulator loop, then a single loop ADC is achieved as shown in figure (4.7)-(a). Single loop ADCs usually needs feedback paths to the output of each integrator to maintain the stability. It can be
shown that in general, if feedforward coefficients $a_1, a_2, \ldots$ are increased then signal to noise ratio is increased and if the coefficients in feedback path are increased then the stability of the loop is improved but the signal to noise ratio would be decreased. Stability and resolution are then trade-off in a single loop modulator.

In order to ease the trade-off between resolution and stability, MASH sigma delta ADCs cascade the low order stable modulators of order one or two to make higher order modulators. Figure (4.6)-(b) shows the block diagram of a MASH ADC composed of two second order modulators. Chapter 5 presents two ADCs design for the same application one with single loop and the other with MASH structure. The comparison of the two designs, brought in chapter 5, shows the cons and pros of each approach.

4.5. Feedforward Architecture

It was mentioned before that one of the advantages of sigma delta ADCs to nyquist rate converters is the fact the formers are less sensitive to analog circuit imperfections. That it due to the fact the nonidealities of Opamp are also noise shaped by the filtering function of the modulator and are high passed from the signal bandwidth. In broadband application, however, oversampling ratio is relatively low (4~16 are the common values) and hence this filtering of non-idealities is not very effective anymore. As a result, distortion terms appear in the output due to the analog circuit nonlinearities and degrade the modulator performance and resolution significantly. Feedforward sigma delta modulators are designed to decrease this distortion. Figure (4.8)-(a) shows a second order conventional sigma delta modulator.
In ideal case the output of this modulator has a delayed version of the input and a second order high passed of quantization noise. Input to the integrators then is the error signal which has a high passed term of the input as follow:

\[ Y_1(z) = (1 - z^{-2})X(z) \]  \hspace{1cm} (4-13)
Because of the finite gain, slew rate, voltage dependant gain of Opamp and other source of errors harmonics of input signal will be generated in the outputs of integrator. They will be digitized by the quantizer and finally will appear in the output. From this discussion, it can be concluded that in order to prevent this problem, output of the integrators should become independent of the input signal. Figure (4.8)-(b) shows a possible architecture of modulator that does this. From this figure, $Y_1(z)$ and $Y_2(z)$ can be written as:

$$ Y_1(z) = \frac{H_1(z)Q(z)}{1 + H_1(z)(2 + H_2(z))} \quad (4-14) $$

$$ Y_2(z) = \frac{H_1(z)H_2(z)Q(z)}{1 + H_1(z)(2 + H_2(z))} \quad (4-15) $$

The above equations show that output of integrators are completely independent of the input signal and are only functions of the quantization noise and the analog filters transfer functions used in the modulator ($H_1(z), H_2(z)$). The complete cancellation of input signal at the output of integrators requires perfect matching between the different paths (feedforward and feedback) of the modulator. However, the incomplete cancellation in practical case causes a small portion of the input signal to appear at the output of the integrators with a small amount of distortion. In any case the amount of distortion would be less significant compared to a conventional modulator.

Feedforward technique was first introduced in [27] for a second order sigma delta modulator and then used in multi-bit single loop [28] as well as cascade (MASH) modulators in [29], [30].
4.6. Leslie-Singh Architecture

As it was discussed in the previous section, single loop modulators have some advantages over MASH type of sigma delta ADCs as they are less sensitive to analog circuit imperfections. It was also seen that single loop ADCs have stability problems and to make the loop more stable, it is better to use multi-bit quantizer inside the loop. Multi-bit loop, however, needs multi-bit DAC which its linearity will limit the accuracy of the whole ADC. Leslie and Singh [31] proposed a multi-bit sigma delta modulator that has only a single-bit DAC in its feedback loop and since the single-bit DAC is inherently linear it would not limit the accuracy of the ADC. Figure (4.9) shows a block diagram of this modulator. As it can be seen from this figure, the multi-bit quantizer is put outside of the modulator loop and the digital filters $H_1(z), H_2(z)$ are designed to cancel the quantization noise of the single-bit quantizer at the output.

The only noise present at the output of the modulator will be the high-passed quantization noise of the multi-bit quantizer. In theory, the modulator has a performance of a multi-bit modulator but with a single bit DAC in its feedback loop. In practice, however, two factors will limit the performance and degrade the performance of this architecture compared to a true multi-bit solution. The first one is the mismatch between the analog filters inside the modulator loop and the digital filters $H_1(z), H_2(z)$ which causes a leakage of quantization noise of the single-bit quantizer appear at the output.
The other factor is the signal scaling. As figure (4.9) shows, the modulator loop is in fact a single-bit loop and hence the integrator coefficients can not be increased to boost the SNR as much as it can be done in a real multi-bit modulator. It has been already discussed in section 4.1 that using a multi-bit quantizer inside the loop will decrease the signals swings and helps to improve the loop stability, hence the integrator coefficients \( a_1 \) and \( a_2 \) can be increased which in turn increases the signal to noise ratio. In Leslie-Singh architecture, the sigma delta modulator is still single bit and hence dose not benefit from this SNR improvement. Therefore, the performance
of this architecture would be better than a single-bit modulator but worse than a true multi-bit sigma delta ADC. Optimizing the coefficients to get the maximum performance is discussed in [32].

![Leslie-Singh architecture with multi-bit noise shaping and single-bit DAC.](image)

Figure 4.9 Leslie-Singh architecture with multi-bit noise shaping and single-bit DAC.

### 4.7. Mixed Pipeline-Sigma Delta ADCs

The idea of Leslie-Singh architecture can be extended to mixed sigma delta-pipeline ADCs where a medium to high resolution pipeline ADC is used as the multi-bit quantizer. This method is used in [33], [34] to cascade a second order 5-bits sigma delta modulator with a 4-stage 12-bits pipeline ADC. The whole converter provides
more than 14 bits (SNR=89 dB) with a low oversampling ratio of 8. This architecture is particularly attractive for broadband applications and will be further discussed in the next section.

4.8. Reduced Sample-Rate Sigma Delta ADCs

The single-bit and multi-bit quantizers in Leslie-Singh architecture (refer to figure 4.9) are both work at the high oversampled frequency. Significant amount of power can be saved if the multi-bit quantizer which is usually implemented using a flash or pipeline ADC can be sampled at a lower frequency. This is in fact possible and is the basis of the so called “reduced data-rate sigma delta ADCs”. Figure (4.10) shows the evolution of a conventional Leslie-Singh modulator to a reduced sample-rate one. As it was discussed in section 4.2, the oversampled output of a sigma delta modulator can be decimated using sinc filters. Sinc filters are usually used to reduce the sampling frequency down to four times the Nyquist rate and extra decimation is then provided with a narrow band sharp filter. Figure (4.10)-(a) shows a conventional Leslie-Singh sigma delta modulator with kth order decimation filter. In order to cancel the quantization noise of the single-bit quantizer, digital filter $H_2(z)$ needs to be:

$$H_2(z) = \frac{(1-z^{-1})^2}{a_1a_2}$$  \hspace{1cm} (4-16)

Since the decimation filter is linear it can be moved to the left side of summation. The numerator of $H_2(z)$ is cancelled with denominator of the decimation filter and the result will be an FIR filter which is a function of $z^{-N}$ as shown in figure (4.10)-(b). Down-sampling can be moved before the filtering and multi-bit quantizer by replacing
\(z^{-N}\) with \(z^{-1}\) in the transfer function of the filter. The result is shown in figure (4.10)-(c).

Reduced sample-rate ADCs are reported in several papers [35]-[38]. It is particularly attractive for broadband applications where oversampling ratio is usually low (4-16). This minimum oversampling ratio is usually required even if a Nyquist rate ADC such as pipeline is going to be used. The reason for that is to relax the requirement of the anti-aliasing filter that precedes the ADC. Since oversampling is used, it is better to get advantage of that by using a sigma delta loop that can shape the noise. The pipeline or other Nyquist rate ADC can be then used in a Leslie-Singh architecture. The input signal is sampled with a frequency four to sixteen times above the Nyquist rate but the pipeline ADC can work at a lower frequency. That saves the power and eases the design of the pipeline converter.

**4.9. Parallel Sigma Delta ADCs**

Similar to the time-interleaved ADCs that use parallel SAR, Flash or pipeline ADCs in parallel to increase the conversion rate, sigma delta ADCs can be also connected in parallel to increase the conversion bandwidth. Parallel sigma delta ADCs are categorized in two groups: frequency-band-decomposition and modulation-based sigma delta ADCs.

In a frequency-band decomposition A/D, each channel converts part of the total bandwidth as it is shown in figure (4.11).

Figures show how the reduced sample-rate is derived from the conventional Leslie-Singh architecture [37].
The quantization noise power at the output of A/D is calculated as:

\[ e_n^2 = \frac{\Delta^2}{12} k^2 \frac{\pi^L}{(L+1)(M-1)^L} \frac{1}{2^{L+1}} \]  

(4-17)

where \( M \) is the number of channels and \( L \) is the order of band pass filters which is also twice the order of low pass and high pass filters. Quantization noise of each sigma delta modulator is assumed to be a white noise with uniform distribution between \([-2\Delta, 2\Delta]\).

Equation (4-17) shows that doubling the number of channels increases the resolution by \( L \) bits. Doubling the number of channels also halves the conversion bandwidth of each modulator. Frequency-band-decomposition A/Ds have the highest design complexity among parallel converters since each channel requires a unique sigma delta modulator design. However, this architecture is the most robust one to the channel mismatch errors.
Figure 4.10. Leslie-Singh architecture with reduced sample-rate.
Frequency-band-decomposition technique resembles FDM (Frequency Division Multiplexing) method in wireless communication systems where different users send their data over a part of bandwidth and channels are separated from each other by a bank of filters. If frequency-band-decomposition technique can be compared with FDM then modulation-based parallel sigma delta ADCs can be seen as CDMA or OFDM techniques where signals in different channels are coded using orthogonal sequences or frequencies.

Figure (4.12) shows the general block diagram of a modulation-based parallel sigma delta A/D. Input signal is first modulated in each channel and after passing through the sigma delta modulator and digital filter is demodulated and combined to generate the total output. The modulation has also the effect of decoupling the signal and quantization noise.

Different modulation-based parallel methods are proposed in literatures based on the modulation matrix which is used. Modulation matrix is a matrix with a number of rows that is equal to the number of channels and each column of it corresponds to a particular time instance. Discrete Fourier transform, identity matrix and Hadamard matrix are different options for modulation matrix. The modulation-based parallel sigma delta ADCs are sensitive to mismatch between different channels and high resolution requires calibration for these errors [39]. The source of channel mismatch includes different input referred offset, signal independent charge injection, signal dependant charge injection, and differences in gain and phase of sigma delta
modulators in different channels. These errors cause distortions and tones in the output of converter.

Figure 4.11. Frequency-band-decomposition sigma-delta A/D converters [39].
4.10. Design of a Sigma Delta Modulator

4.10.1. Behavioral Modeling

Sigma delta modulator is a complex design that needs to be done in different steps with different levels of abstraction. Before the circuit implementation, behavioral modeling can be done to prove that the design can provide the specifications at least in the system level. In this thesis, Matlab/Simulink has been used to perform the behavioral modeling of sigma delta modulators. Behavioral modeling of sigma delta
ADCs has been discussed in several papers [40]-[43]. The following non-idealities have more effect in signal to noise degradation and therefore needed to be modeled:

*Opamp finite gain:*

Finite gain of the Opamp cause a gain and a pole error in the transfer function of an ideal integrator. The output of the integrator can be then written as [43]:

\[
V_o(z) = \frac{C_s}{C_i} \rho_2 \frac{z^{-1}V_i(z) - z^{-1/2}V_{fb}(z)}{1 - \frac{\rho_2}{\rho_1} z^{-1}}
\]  
(4.18)

where

\[
\rho_1 = \frac{A_{f_{dc1}}}{1 + A_{f_{dc1}}}
\]  
(4.19)

\[
\rho_2 = \frac{A_{f_{dc2}}}{1 + A_{f_{dc2}}}
\]  
(4.20)

\[
f_{dc1} = 1
\]  
(4.21)

\[
f_{dc2} = \frac{C_i}{C_s + C_i} = \frac{1}{1 + a_i}
\]  
(4.22)

Parasitic capacitors have been neglected in the above equations; otherwise they should be included in the feedback factor equations (4.21) and (4.22). Figure (4.13) plots the signal to noise degradation of a 2-2 MASH sigma delta modulator versus finite gain of the Opamp. The modulator will be used in chapter 5 and plot shows that a minimum gain of 50 dB is required so that SNR degradation due to finite gain remains below few dB.
Figure 4.13. Effect of Opamp finite gain on the SNR of a 2-2 MASH $\Sigma\Delta$

*Opamp finite bandwidth:*

Opamp finite bandwidth causes the output of integrator to settle to its final value in an exponential manner. Similar to Opamp DC gain, finite bandwidth introduces gain and pole error. It can be shown that the output of integrator at the end of sampling phase would be:

$$V_o(z) = \frac{C_s}{C_I} \frac{\rho_2 (1-\delta_2)[z^{-1}V_i(z) - z^{-1/2}V_{fb}(z)]}{1 - \rho_2 \rho_1 (1 + \delta_2 (\rho_1 \rho_2 ^{-1}))z^{-1}}$$

(4.23)

where $\rho_1$ and $\rho_2$ are given by equations (4.19) and (4.20) and $\delta_2$ is:
\[ \delta_2 = \exp\left(-\frac{g_m \tau_2}{C_s \rho_2}\right) \]  

(4.24)

\(\tau_2\) is the available time during the integration phase. For a single pole Opamp \(\frac{g_m}{C}\) represents the open loop bandwidth and hence equation (4.23) shows that open loop bandwidth of Opamp cause gain and pole error that adds to the errors already caused by finite gain of Opamp. Figure (4.14) shows the signal to noise ratio of the 2-2 MASH modulator used in section 3-8 as a function of Opamp bandwidth. A minimum bandwidth of 250 MHz is required for this specific case to achieve more than 65 dB SNR.

*Switch resistance:*

In above analysis, the switch resistance is assumed to be zero. Nonzero resistance of the switches together with the capacitances of the switched capacitor circuit makes an RC time constant that affect the settling behavior of the Opamp during the sampling time.
The output of the integrator at the end of sampling phase would be:

\[
V_o(z) = \frac{C_s}{C_I} \rho_2 \left(1 - \delta_2\right)[(1 - \delta_1)z^{-1}V_i(z) - (1 - \delta_1z^{-1})z^{-1/2}V_{fb}(z)] \\
\quad \quad \quad \quad \quad \quad \quad \quad \frac{z^{-2} - \rho_2}{\rho_1}(1 + (\delta_1 + \delta_2)(\frac{\rho_1}{\rho_2} - 1) + \delta_1\delta_2)z^{-1} + \delta_1\delta_2
\] (4.25)

where

\[
\delta_1 = \exp\left(-\frac{\tau_1}{R_1 C_s}\right)
\] (4.26)

\[
\delta_2 = \exp\left(-\frac{g_m}{C_s \rho_2 (1 + \lambda)}\right)
\] (4.27)
In the above equations, \( R_1 \) and \( R_2 \) are the equivalent resistance of the switches in the sampling phase and integration phase respectively.

Comparing equation (4.25) with (4.23) which only accounts for finite gain and finite bandwidth of Opamp shows that resistance of switches introduces an extra pole to the transfer function of integrator. The pole and gain error are also intensified by including the nonzero resistance of switches and moreover, the gain error in the feedback path is no longer the same as the gain error in the signal path. All of these effects lead to more degradation of signal to noise ratio of the \( \Sigma\Delta \) modulator with respect to its ideal value.

Simulations was done for the same 2-2 MASH modulator used in chapter 5 to specify maximum allowable switch resistance that does not degrade the signal to noise ratio more than a few dB. Figure (4.15) shows the result of this simulation, it turns out that switch resistance should be below 200\( \Omega \). On the other hand, choosing small value for switch resistance has an undesirable effect and that is increasing the charge injection. Following equation shows that the small on-resistance for an NMOS switch can be obtained by choosing a large device (increasing \( \frac{W}{L} \)).

\[
R_{on} = \frac{1}{\mu_{n}C_{ox} \frac{W}{L} (V_{GS} - V_{th} - V_{DS})} \quad (4.29)
\]

Large switches, on the other hand, have larger charge injection which is evident from the equation below:
\[ Q_{\text{Charge}_{\text{-injection}}} = -WLC_{ox}(V_{DD} - V_{in} - V_{th}) \] (4.30)

Therefore choosing the right size for switches is a matter of trade-off between speed of the switched capacitor circuit (how small the RC time constant will be) and its accuracy (amount of charge injection). The effect of charge injection on the accuracy of the circuit, however, can be decreased significantly by using early clocks which turn off the switches near the virtual ground first and hence limit the charge injection problem to only those early switches.

Figure 4.15. Effect of Opamp non-zero switch resistance on the SNR of a 2-2 MASH \( \Sigma \Delta \).
Other sources of error:

In addition to the above mentioned errors, there are other non-idealities in the analog circuit of ΣΔ modulator that can be included in behavioral modeling of the ADC. Among them are: finite slew rate of Opamp, non-linear Opamp gain (variation of Opamp gain with its output voltage or gain compression effect), non-linear switch resistances, nonlinear capacitances (voltage dependant capacitors), non-idealities of DAC, and finally non-idealities of the quantizer including offset and hysteresis.

4.10.2 Optimal Coefficients for Sigma Delta Converters

Figure (4.16) shows a single loop 2\textsuperscript{nd} order sigma delta modulator with feed forward path coefficients of \( a_1 \) and \( a_2 \). Writing the z-transform function of output of modulator gives:

\[
Y(z) = \frac{a_1 a_2 z^{-2}}{(1 + a_1 a_2 - a_2) z^{-2} + (a_2 - 2) z^{-1} + 1} X(z) + \frac{(1 - z^{-1})^2}{(1 + a_1 a_2 - a_2) z^{-2} + (a_2 - 2) z^{-1} + 1} Q(z)
\]

(4.31)

which gives signal and noise transfer function as following:

\[
STF = \frac{a_1 a_2 z^{-2}}{(1 + a_1 a_2 - a_2) z^{-2} + (a_2 - 2) z^{-1} + 1}
\]

(4.32)

\[
NTF = \frac{(1 - z^{-1})^2}{(1 + a_1 a_2 - a_2) z^{-2} + (a_2 - 2) z^{-1} + 1}
\]

(4.33)

In order to make equation (4.32) equal to (4.9) which represents STF of an ideal \( n \)\textsuperscript{th} order modulator, and the same way making (4.33) equal to (4.10), \( a_1 \) and \( a_2 \) need to be equal to 0.5 and 2 respectively. Simulation results of the sigma delta modulator with these coefficients show that the voltage swing at the output of the first and second
integrator would be 1.08 and 1.6 volts peak-to-peak respectively. In a technology with 1.8v power supply, Opamp swing of 1.6 volts is not desirable since the process and voltage supply variations may cause the Opamp output voltage to be clipped which in turn produces significant distortion. Therefore \( a_1 \) and \( a_2 \) gains need to be chosen different from ideal values which but that causes the signal to noise ratio achievable form this modulator to be less than ideal value.

Voltage swings of all integrators except the last one can be changed without changing the performance of modulator. This is possible by introducing gains in feedback paths. Figure (4.16)-(b) shows how extra gains can be added to the feedback path to decrease the output swing of first integrator from 1.08v to 0.86v. Output swing of the last stage, however, can not be change without affecting the modulator performance. Opamp swing limitation results in non-optimal gain values and degrades signal to noise ratio of modulator.

In addition to the internal nodes voltage swings, modulator coefficients have impacts on stability of the modulator loop. Larger coefficients result in more aggressive noise shaping and hence increase the signal to noise ratio, but on the other hand jeopardize the stability of the loop. Increasing gain coefficients does not increase signal to noise ratio unbounded and signal swings are limited by the supply voltages. Figure (4.17) plots the achieved peak signal to noise ratio for the 2nd order modulator of figure (4.16) with \( a_2 = 2 \) while \( a_1 \) changes from 0.02 to 1.4. At the beginning, increasing gain of \( a_1 \) increases the signal to noise ratio but after some point \( (a_1 = 0.8) \), SNR shows a huge drop. This drop is because of the instability of the loop.
Measuring OL (Overload Level) shows that it has dropped from -6 dBm (for $a_1 = 0.5$) to OL=-14 dBm for $a_1 = 1.4$. Since the loop saturates for smaller value of input signal, peak of SNR happens at smaller input level and hence the value of $\text{SNR}_{\text{peak}}$ is also decreased.

Using multi-bit quantizer inside the loop improves the stability and increases the OL of modulator. Therefore the signal to noise ratio of the modulator increases not only because of the increase resolution added by multi-bit quantizer but also due to the fact that more aggressive noise shaping is now possible without making the feedback loop unstable.

Power consumption is another factor that is affected by the coefficients in the modulator. Larger coefficients result in smaller feedback factor that in turn increases the required Opamp bandwidth and hence increases the power consumption.
Figure 4.16 (a), (b) Using scaling coefficients to change internal node voltage swings in a modulator, (a) without feedback path gains, (b) introducing gain scales to decrease output swing of first integrator.

Figure 4.17. Signal to noise ratio of the 2\textsuperscript{nd} order ΣΔ modulator versus a\textsubscript{1} coefficient.
5.1. Design a Single Loop Sigma Delta ADC for WCDMA Application

This section describes the design of a single loop filter-based sigma delta ADC for WCDMA application. Specifications for this ADC are as follows:

\[
BW = 3.84 \text{ MHz} \quad (5.1)
\]

\[
f_s = 30.72 \text{ Msps} \quad (5.2)
\]

\[
DR = 62 \text{ dB} \quad (5.3)
\]

Given the values for signal BW and clock frequency, oversampling ratio is calculated to be 8. The required dynamic range is almost equal to 12 bit resolution. Using the procedure described in section 4.9.1, Opamp specifications can be derived as:

\[
A_{dc} = 100 \text{ dB} \quad (5.4)
\]

\[
SR = 577 \text{ v/μs} \quad (5.5)
\]
SNR of a sigma delta ADC was given in chapter 4 and is repeated here:

\[
\text{SNR}_p = \frac{3\pi}{2} (2^b - 1)^2 (2n + 1)(\frac{\text{OSR}}{\pi})^{2n+1}
\]  (5.7)

Using this equation a 4th order MASH sigma delta modulator with 17 level quantizer provides 64 dB signal to noise ratio which barely meets the specification. Instead, we decided to use a single loop sigma delta modulator. As explained previously, single loop sigma delta modulators are less sensitive to analog circuit nonidealities, which is more attractive in submicron technology. In order to provide a broadband attenuation for noise transfer function, it was decided to locate two poles of NTF at origin and optimize the location of two other poles inside the signal bandwidth. In order to keep the coefficients of the filter loop real, the two zeros should be complex conjugate.

Noise transfer function can be written as:

\[
\text{NTF} = (1 - z^{-1})^2 (z^{-2} - \alpha z^{-1} + 1)
\]  (5.8)

Using this noise transfer function, loop filter can be calculated as:

\[
H(z) = \frac{-z^{-1}(z^{-3} - (2 + \alpha)z^{-2} + (2 + \alpha)z^{-1} - (2 + \alpha))}{(1 - z^{-1})^2 (z^{-2} - \alpha z^{-1} + 1)}
\]  (5.9)

The transfer function given in equation (5.9) can be decomposed into two second order terms and implemented using switched capacitor biquad filters.

\[
H(z) = \frac{A z^{-2} + B z^{-1} + C}{z^{-2} - \alpha z^{-1} + 1} \ast \frac{D z^{-2} + E z^{-1} + F}{z^{-2} - 2 z^{-1} + 1}
\]  (5.10)

Equating the two above equations, gives the followings relationships for the parameters A to F:
\[ AD = -1 \]  \hspace{1cm} (5.11)

\[ AE + BD = 2 + \alpha \]  \hspace{1cm} (5.12)

\[ AF + BE + CD = -2(\alpha + 1) \]  \hspace{1cm} (5.13)

\[ BF + CE = 2 + \alpha \]  \hspace{1cm} (5.14)

\[ CF = 0 \]  \hspace{1cm} (5.15)

There are six variables (A,B,..F) that should be determined from the above five equation, therefore, there is one degree of freedom. \( \alpha \) can be selected to maximize the signal to noise ratio. Above parameters can be also calculated using the Sigma Delta Matlab toolbox of Shreier [44]. This toolbox synthesizes the loop transfer function based on the filter order, oversampling ratio and \( H_{inf} \). Where \( H_{inf} \) is the limit on the value of the noise transfer function as frequency goes to \(-\pi\) or \(\pi\). By fixing the two zeros of noise transfer function at DC, \( \alpha \) can be determined to locate the two other zeros such that it maximizes the signal to noise ratio. There is a trade-off between the amount of noise shaping and loop stability. Increasing \( H_{inf} \) leads to more attenuation of the quantization noise inside the signal bandwidth which in turn increases the signal to noise ratio. However, high \( H_{inf} \) makes the feedback loop more prone to instability.

Figure (5.1) and (5.2) illustrate this fact by comparing the root loci of the two loop transfer function with \( H_{inf} = 4 \) and \( H_{inf} = 6 \). For the case where \( H_{inf} = 4 \), the range of loop gain for which the closed loop system is stable would be:

\[ 0.668 < k < 1.33 \]  \hspace{1cm} (5.16)

for \( H_{inf} = 6 \), this range is limited to:

\[ 0.725 < k < 1.2 \]  \hspace{1cm} (5.17)
Figure 5.1. Root Locus of the 4\textsuperscript{th} order loop filter designed with $H_{\infty}=6$

Figure 5.2. Root Locus of the 4\textsuperscript{th} order loop filter designed with $H_{\infty}=4$
Variation in loop gain can be caused by parameter variation in analog design and can be predicted to some degree of accuracy. As a good trade-off between the required signal to noise ratio and stability, $H_{\text{inf}} = 6$ is chosen for this design. The noise and loop filter transfer functions would be:

$$NTF_{H_{\text{inf}}=6} = \frac{(z-1)^2(z^2-1.891z+1)}{(z^2-0.4434z+0.0629)(z^2-0.0863z+0.2025)}$$ (5.18)

$$H_{H_{\text{inf}}=6} = \frac{3.0403(z-0.5703)}{(z-1)^2} \frac{(z^2-1.154z+0.5623)}{(z^2-1.891z+1)}$$ (5.19)

Figure (5.3) shows the signal and transfer function for the loop filter calculated using sigma-delta toolbox for oversampling ratio of 8 and $H_{\text{inf}} = 6$.

Figure 5.3. Signal and noise transfer function of the single loop sigma delta ADC
Figure (5.4) zooms into the signal bandwidth and it is evident that signal transfer function is fairly resembles a band-pass function inside the signal bandwidth.

Figure 5.4. Signal and noise transfer function of the single loop sigma delta ADC, zoomed into the signal bandwidth

Behavioral simulations as described in chapter 4, section 4.9.1 was done and the results show a dynamic range of 85 dB and a peak signal to noise ratio of 72 dB which both are well above the requirements for this design. Some of the important parameters of the design are summarized in table 5.1.
Table 5.1. Design parameters and performance for single loop sigma delta ADC

The filter transfer function given in equation (5.19) is implemented using two switched capacitor circuits. H is decomposed to two second order terms, each resembles a biquad filter:

\[ H_1 = \frac{3.0403(z - 0.5703)}{(z - 1)^3} \]  

(5.20)
$$H_2 = \frac{(z^2 - 1.154z + 0.5623)}{(z^2 - 1.891z + 1)} \quad (5.21)$$

Figures (5.5) and (5.6) show the switched capacitor implementation of $H_1$ and $H_2$ respectively.

---

**Figure 5.5.** Switched capacitor implementation of $H_1$
Figure 5.6. Switched capacitor implementation of H2

Simulation results of this modulator are brought in figures (5.7) and (5.8). Modulator dynamic range is 85 dB and its peak signal to noise ratio is 72.8 dB. The overload input occurs at 0dBm and a single tone test with a low frequency sinusoidal input shows 82 dB spurious free dynamic range.

5.1.2. Remarks and Conclusions for Single Loop Design

High order single loop sigma delta ADCs can provide higher signal to noise ratio than a MASH sigma delta of the same order. Higher resolution, however, comes with the price of stability. Unlike to the first and second order loop filters which are always stable, loop filters of order three and higher results in modulators that are conditionally
stable. This means that if the gain loop exceeds a certain range, loop becomes unstable and saturates the quantizer and it can not be recovered from this instability condition unless the outputs of integrators are being reset. Figures (5.1) and (5.2) for example, show these regions of stability for two 4th order filters. If the loop gain exit this region and system becomes unstable, amplitude of the signals inside the loop keep growing. The signals however do not grow to infinity and their values are limited to the amount of supply voltage in the circuit. The output signals of the Opamps, therefore, will be clipped and the internal quantizer is saturated. This causes the loop filter to drop. If decreasing the loop gain cause the system to move inside the stable region, the instability has been solved without any further problem. This is not the case for high order single loop modulators. As figure (5.1) shows, value of k needs to be larger than 0.752 for stability. Saturation of the quantizer will drop the loop gain below this value and the result is that the modulator remains in instable region. For this reason, high order single loop modulators usually use extra circuitry to reset the outputs of the Opamps in case that instability happens.
Figure 5.7. Resolution and dynamic range performance of the single-loop ΣΔ ADC.

Figure 5.8. Output spectrum for a single tone test of the single-loop ΣΔ ADC.
5.2. Design Example of a MASH Multi-bit ADC

As it was seen in the previous section, the resolution and stability trade-off in single loop modulators which makes the practical application of these modulators limited. Unlike the single loop modulators, MASH sigma delta uses the unconditionally stable first and second order modulators and cascade them to achieve the required resolution. This section explains the design and implementation of a MASH sigma delta ADC for 4th generation of cellular phones that cover GSM/WCDMA/WLAN receiver. The ADC specifications derived from system study (refer to chapter 2) and are listed in Table 5.2. Table 5.2 also includes the requirements of ADC in Bluetooth system, since the same design can satisfies the requirements of a Bluetooth system, it is mentioned here. A two stage 4th order MASH sigma delta ADC is chosen for this design. Block diagram of this modulator is shown in figure (5.9). The first stage is enough to digitize Bluetooth and GSM signal and the whole 4th order modulator is required for WCDMA signal. It will be shown in Chapter 6 that using ANC (Adaptive Noise Cancellation) can boost the performance of the 4th order modulator to provide enough resolution for WLAN. In this section, we concentrate on the design of the modulator for GSM, WCDMA and Bluetooth and WLAN will be covered in next chapter.

Table 5.2 also shows the clock frequency and oversampling ratio in each standard which are determined in system level from the anti-aliasing filter requirements.
<table>
<thead>
<tr>
<th>Standard</th>
<th>Channel Bandwidth</th>
<th>Clock Frequency</th>
<th>Oversampling Ratio</th>
<th>Required Dynamic Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>WCDMA</td>
<td>3.84 MHz</td>
<td>30.72 MHz</td>
<td>8</td>
<td>50 dB</td>
</tr>
<tr>
<td>GSM</td>
<td>200 KHz</td>
<td>51.2 MHz</td>
<td>128</td>
<td>70 dB</td>
</tr>
<tr>
<td>WLAN (11.b)</td>
<td>22 MHz</td>
<td>88 MHz</td>
<td>4</td>
<td>52 dB</td>
</tr>
<tr>
<td>Bluetooth</td>
<td>1.5 MHz</td>
<td>48 MHz</td>
<td>32</td>
<td>51 dB</td>
</tr>
</tbody>
</table>

Table 5.2. ADC specifications in the multi-standard GSM/WCDMA/WLAN along with the ADC requirements in a Bluetooth system.

![GSM, Bluetooth](image)

Figure 5.9. Block diagram of the multi-standard sigma delta modulator
5.2.1. Circuit Implementation

This section explains the circuit implementation of the multi-standard sigma delta ADC depicted in figure 5.9. A fully differential switched capacitor circuit is used to remove DC offset and common mode errors. Circuit diagram of the switched capacitor circuit is given in Figure 5.10. Two non-overlapping phases are used for sampling and integration phases. Delayed clocks are used to decrease the effect of voltage dependent charge injection of witches. More details on clock generation block is given in the next section. A flash ADC is used inside the loop as the quantizer due to its fast operation that minimizes the loop delay. Switched capacitor DAC is used to feedback the output of modulator to the input of the integrators.

Figure 5.10. Switched capacitor circuit used to implement each stage of the multi-standard sigma delta converter with the block diagram given in Figure 5.9.
5.2.2 Clock Generator

Clock generator needs to generate two non-overlapping clocks $\phi_1$ and $\phi_2$ and the delayed version of each $\phi_{1d}$ and $\phi_{2d}$ which are used for the switches that are connected to signal. Figure 5.11 shows a scheme of the clock generator circuit with more details of the design is given in figure 5.12.

![Figure 5.11. Block diagram of the clock generator circuit](image1)

![Figure 5.12. Clock generator circuit](image2)
5.2.3. Opamp Design

Simulating the 4\textsuperscript{th} order sigma delta modulator in Matlab/Simulink with 88MHz clock frequency gives the following specifications for the Opamp, which needs for enough signal to noise ratio required for all standards listed in table 5.2.

<table>
<thead>
<tr>
<th>Opamp parameter</th>
<th>Min. Required value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$A_{\text{DC}}$</td>
<td>60 dB</td>
</tr>
<tr>
<td>GBW</td>
<td>250 MHz</td>
</tr>
<tr>
<td>Output Swing</td>
<td>1 V</td>
</tr>
<tr>
<td>SR</td>
<td>150 V/$\mu$s</td>
</tr>
</tbody>
</table>

Table 5.3. Opamp required parameters in multi-standard sigma delta design

It is very difficult to provide high gain and large output swing in low supply voltage using a single stage Opamp. Hence, a two stage Opamp seems to be the best choice. In order to provide enough gain, first stage is usually folded cascode or telescopic and in order to have high output swing a simple common source is used in the second stage.
Two or more stage Opamps need a compensation technique to split their dominant pole from non-dominant pole and to improve their stability. The most common technique is the Miller compensation where a compensated capacitor is placed between the outputs of the two stages. However, this technique introduces a right-half-plane zero which can degrade the phase margin significantly. In order to compensate for this zero, a resistor is connected in series with the compensation capacitor.

Miller compensation makes the PSR (Power supply rejection) of the amplifier degrade in high frequency. This is due to the fact that the miller capacitance is connected between drain and gate of the output transistor. In high frequencies, this capacitor is almost short circuited and the device would be diode connected and conducts the noise on the supply rails directly to the output. Another drawback of the miller compensation is that the compensation capacitor should be larger than the load capacitor and the transconductance of the output transistor should be large enough to push the non-dominant farther away. Since compensation capacitor directly affects the power consumption, larger Cc means more power consumption.

Another technique for compensating a two stage Opamp was first introduced by Ahuja [45] and is called cascode compensation. In cascode compensation, the compensation capacitance is connected between source of the cascode device in first stage and the output of second stage. Figure (5.13) compares the configuration of miller with cascode compensation.

In a sigma delta modulator, Opamps which are used in integrators are needed to settle to the final value within some accuracy during the integration time. Therefore,
settling behavior of the Opamp in closed loop configuration is the most important factor. Feldman has derived the cascode compensated Opamp voltage transfer function connected in a feedback configuration as follows [46]:

\[
\frac{V_o(s)}{V_i(s)} = \frac{1}{f \left(1 + s / \alpha \zeta \omega_n \right) \left(1 + 2 \zeta s / \omega_n + s^2 / \omega_n^2 \right)}
\]

(5.22)

where \( f \) is the feedback factor of the amplifier during the integration phase and is equal to:

\[
f = \frac{C_F}{C_s + C_F + C_p}
\]

(5.23)

\( (C_F, C_s \text{ and } C_p \text{ are the integrator, sampling and parasitic capacitors respectively}) \).

Equation (5.22) shows that the closed loop Opamp has two real zeros one at the right-half-plane and the other on the opposite location at the left-half-plane which compensate each other. Closed loop Opamp also has a real left-half-plane pole and two complex conjugate poles where their exact locations are specified by \( \alpha \), \( \zeta \), and \( \omega_n \) as are depicted in figure (5.14).

Location of poles and zeros of this Opamp are related to the Opamp parameters through the following equation:

\[
\frac{g_{mi}}{C_c} = \frac{1}{f} \frac{\alpha \zeta}{1 + 2 \alpha \zeta^2} \omega_n
\]

(5.24)

\[
\alpha \zeta \omega_n^3 = \frac{f g_{mi} g_{me} g_{ma}}{C_s C_F^2}
\]

(5.25)

\[
\omega_n (2 + \alpha) \zeta = \frac{g_{me} (C_{load} + C_c) - f g_{mi} C_c}{C_T^2}
\]

(5.26)
where $g_{mi}$, $g_{mc}$, and $g_{ma}$ are the transconductance of input, cascode and output transistors respectively and:

$$C_T^2 = C_{load} C_c + C_{load} C_1 + C_1 C_c$$

(5.27)

$C_1$ is the total parasitic capacitor at the source of the cascode transistor.

Figure 5.13. (a) Miller and (b) Cascode compensation

Figure 5.14. Zero and pole locations for a closed loop cascode compensated Opamp
Equations (5.24)-(5.27) show that the poles and zeros of a cascode compensated Opamp are complicated functions of the circuit parameters, namely transconductance of the transistors in signal path. Since the settling behavior of the Opamp during the integration phase is the critical characteristic in sigma delta modulator, the Opamp should be designed to have the required settling behavior. From equation (5.22), the settling error can be calculated as:

$$e_{ss} = \frac{s(\infty) - s(t_s)}{s(\infty)}$$

(5.28)

where $s(\infty)$ and $s(t_s)$ are the step response of closed loop Opamp and hence the settling error in terms of zeros and poles positions would be:

$$e_{ss} = \frac{1}{1-2\alpha^2 + \alpha^2 \zeta^2} \exp(-\alpha \zeta \omega t_s) + \frac{\alpha \zeta \exp(-\zeta \omega t_s)}{(1-2\alpha^2 + \alpha^2 \zeta^2)} \left[\left[\left(1-2\zeta^2 + \alpha \zeta \right) \cos(\omega t_s \sqrt{1-\zeta^2}) + \frac{1-2\alpha^2 + \alpha \zeta}{\sqrt{1-\zeta^2}} \sin(\omega t_s \sqrt{1-\zeta^2})\right]\right]$$

(5.29)

As the above equation shows, settling error is a function of $\alpha$, $\zeta$, and $\omega_n t_s$. These relationships are depicted in figure (5.15). This figure plots settling error as a function of $\omega_n t_s$ for different values of $\zeta$ and for $\alpha = 1$. Considering the minimum required settling error, figure (5.16) gives different $\omega_n t_s$ based on the value of $\zeta$. The value of $\zeta$ which leads to minimum $\omega_n t_s$ will be desired since it minimizes the required bandwidth for the Opamp and hence reduces the power consumption.

Another factor to determine is $\alpha$. Figure (5.16) shows the same graph for $\alpha = 0.9$. This figure shows less variability of settling error with respect to different values of
\( \zeta \). This leads to a more robust design since \( \zeta \) might change from its designed value due to the parameter variations in real circuit.

Figure 5.15. Steady state error of the cascode compensated Opamp for \( \alpha = 1 \)

Figure 5.16. Steady state error of the cascode compensated Opamp for \( \alpha = 0.9 \)
Smaller value of $\alpha$, however, requires more $\omega_n t_s$ for the same value of settling error that means more bandwidth and increased power consumption. Therefore, designer sees a trade-off between robustness and power consumption.

Choosing the values of $\alpha$, $\zeta$ and $\omega_n t_s$, $g_m$ of transistors can be calculated using equations (5.24)- (5.26).

As the above discussion shows, settling behavior of a cascode compensated Opamp is a function of transconductance of input, cascode and output transistors. In order to have a better control on these parameters, a folded cascode configuration was chosen for the first stage. By choosing different currents for the input and cascode branches, $g_m$ of input and cascode transistors can be set independently and hence provide more flexibility to achieve required settling behavior. The Opamp circuit is depicted in figure (5.17).

The Opamp is designed to meet the specifications listed in Table 5.3. Some of the performance parameters of this design are listed in Table 5.4.

5.2.4. Quantizer and Internal DAC

A 5 level Flash ADC was used as the quantizer to minimize the delay in the feedback path. Internal DAC was implemented by a switched capacitor circuit which was added to the integrator. The reference voltages were generated by an R-ladder.
Figure 5.17. Two stage cascode compensated Opamp

TSMC0.18µm, $V_{dd}=1.8$ V

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$A_{DC}$</td>
<td>75 dB</td>
</tr>
<tr>
<td>$BW$</td>
<td>284 MHz</td>
</tr>
<tr>
<td>$PM$</td>
<td>77</td>
</tr>
<tr>
<td>CMRR</td>
<td>115 dB</td>
</tr>
<tr>
<td>PSRR</td>
<td>95 dB</td>
</tr>
<tr>
<td>$SR$</td>
<td>175 V/µs</td>
</tr>
<tr>
<td>$OS$</td>
<td>1.2 V</td>
</tr>
</tbody>
</table>

Table 5.4. Performance parameters of the designed Opamp
5.2.5. Modulator Performance

The two stage 4\textsuperscript{th} order modulator of figure (5.9) was implemented in TSMC 0.18\textmu m technology using a 1.8 V supply voltage. Figure (5-18) shows the layout of this design. Single tone tests with sinusoidal inputs are done for the three standards Bluetooth, GSM, and WCDMA. The results are given in figures (5-19) to (5-21). Table 5.5 summarizes the modulator performance. The only standard missing in this table is WLAN which will be discussed in Chapter 6. In fact, in order to provide enough resolution for WLAN, a 6\textsuperscript{th} order (2-2-2) sigma delta modulator is needed. Higher order MASH modulators have leakage problems due to the analog circuit non-idealities that degrade their performance significantly and hence not much improvement will gain with increasing the number of stages and it only costs more area and power. Chapter 6 introduces a new technique to boost the signal to noise ratio of modulator without need to increase the cascaded stages. The technique is implemented all in digital and hence will not add to analog complexity. The two stage 4\textsuperscript{th} order modulator with this extra digital block will be able to provide enough resolution for WLAN.
Figure 5.18. Layout of the 2 stage 4th order ΣΔ modulator in TSMC 0.18μm Technology.
Figure 5.19. Output spectrum of the one stage 2\textsuperscript{nd} order modulator tested for Bluetooth signal

Figure 5.20. Output spectrum of the one stage 2\textsuperscript{nd} order modulator tested for GSM signal
Figure 5.21. Output spectrum of the two stage 4\textsuperscript{th} order modulator tested for WCDMA signal

<table>
<thead>
<tr>
<th>Standard</th>
<th>ΣΔ modulator</th>
<th>( f_s ) [MHz]</th>
<th>SNDR(^*)(_{\text{max}}) [dB]</th>
<th>SND(_{\text{Required}}) [dB]</th>
<th>Power [mw]</th>
</tr>
</thead>
<tbody>
<tr>
<td>WCDMA</td>
<td>2-2</td>
<td>30.72</td>
<td>56</td>
<td>52</td>
<td>11</td>
</tr>
<tr>
<td>GSM</td>
<td>2</td>
<td>51.2</td>
<td>72</td>
<td>70</td>
<td>6</td>
</tr>
<tr>
<td>Bluetooth</td>
<td>2</td>
<td>48</td>
<td>60</td>
<td>51</td>
<td>5</td>
</tr>
</tbody>
</table>

Table 5.5. Performance parameters of the multi-standard ΣΔ modulator

\(^*\) SNDR is calculated using 1024-point FFT.
Chapter 6

Calibration of Sigma Delta ADCs

6.1. Introduction

Sigma delta modulators are well-known to be less sensitive to analog circuit imperfections compared to nyquist rate ADCs which need very accurate analog circuitry. This is due to the fact that all analog circuit non-idealities except the ones in first integrator are noise shaped by the loop filter. Based on the location of these errors inside the sigma delta modulator they experience some amount of filtering. As the demand for broadband wireless applications is increasing, oversampling ratio of the sigma delta ADCs designed for such applications is limited to the maximum available clock frequency. Therefore noise shaping can not effectively filter out all the errors caused by imperfections of analog circuit. On the other hand, in submicron technology, design of high performance analog circuits is getting more difficult adding
to the above mentioned problems. Hence, high resolution, high speed sigma delta ADCs require some form of calibration.

Calibration techniques for sigma delta ADCs are discussed in many papers. These techniques can be categorized based on:

- Analog or Digital calibration
- Background or Foreground techniques
- Type of error that is corrected

The most usual analog calibration is trimming where the matching requirements of the DAC elements are improved by laser trimming of the DAC components. An analog calibration technique is proposed in [47] to cancel the pole error introduced by the finite gain of Opamps. An extra ADC is used in [48], [49] to correct for the nonlinearity and improve the INL (Integral Nonlinearity) of analog to digital converter. Unlike the analog calibration techniques that need an extra analog circuitry for monitoring and correcting the errors, digital techniques compensate for the errors after the signal is converted to the digital domain. Digital calibration techniques are becoming more popular because of the advances in digital signal processing and the fact that power and area are effectively scale down in digital designs. Digital calibration techniques are the main focus of this chapter.

Calibration techniques can be also classified into foreground and background methods. Foreground calibration is the most common way of compensating for the static (inherent) errors of ADCs. A calibration routine can be done at startup by applying a known test signal to the input of the ADC. In the most common way of
foreground calibration, a lookup table is built with the measured values of ADC output for possible values of input. This table is then used during the normal operation of the ADC to correct the erroneous output of converter [50]. This method does not account for the continuous variation of supply voltage, temperature and parameters due to the aging. Foreground calibration can be also done periodically during the idle time of the ADC, however, many applications do not allow for such interruptions. Background calibration techniques are then developed to overcome these problems and provide continuous monitoring and correcting of the errors in sigma delta ADCs.

Calibration techniques are also categorized based on the type of error that they tackle. Most of the calibration techniques proposed in literatures target either DAC nonlinearities or leakage noise problem in MASH sigma delta architectures. For the multi-bit single loop sigma delta ADCs, DAC nonlinearity is the most important source of error. It has been discussed in chapter 4 that multi-bit modulators help to stabilize the loop and let more aggressive noise shaping, however they also need highly linear DAC inside the loop. In fact, the non-linearity of this DAC is added directly to the input signal and hence it is not high passed by the loop filter. Section 6.2 gives a brief review of these techniques.

Due to stability issues with high order single loop modulators, MASH ADCs become the most popular architecture for sigma delta analog to digital converters. MASH ADCs use a cascade of stable first and second order modulators to make a higher order one. The converter also uses digital filters to combine the output of each
stage and makes the final output. Digital filters are designed such that the quantization noise of all stages except the last stage is cancelled.

MASH ADCs however are suffering from noise leakage problem which is caused due to the mismatch between loop analog filters and correction logic digital filters. Noise leakage problem is discussed in more detail in next section. Adaptive calibration techniques are introduced to address this problem.

This chapter is focused on adaptive techniques to compensate the non-idealities in sigma delta modulators. Due to its popularities, a brief overview of compensation techniques for DAC nonlinearities is given in section 6.2. Section 6.3 is dedicated to the adaptive techniques starting with techniques to remove noise leakage problem in section 6.3.1. Foreground calibration techniques are brought in section 6.3.2 and background techniques in section 6.3.3. A new background adaptive technique based on active noise cancellation is proposed in section 6.3.4.

### 6.2. Compensation of Internal DAC Non-linearity

The use of multi-bit quantizer instead of single bit quantizer in ΣΔ modulators has several advantages such as increasing the signal to noise ratio, improving stability and relaxing Opamp specification. However, many designers have been reluctant to use the multi-bit quantizer because of the non-linearity of the internal DAC. Since the errors of the internal DAC add up directly to the input signal, the linearity of the internal DAC should be at least as good as that of the overall ADC. Various techniques have been proposed to improve the DAC linearity including the analog and digital techniques.
Trimming techniques are used in many SAR ADCs as well as other high resolution converters. Thin film resistors are laser-trimmed to achieve required accuracy and linearity. Using highly focused laser beam, the width of resistor can be changed and hence its resistance value is changed. Laser trimming can provide up to 16 bits accuracy. However, the process is very expensive and requires the integration of thin film and patterning. The laser equipments that provide tightly focused beam are also expensive. Laser trimming can not take care of any shift due to packaging that might happen due to mechanical stresses [52].

Other forms of analog techniques are also used to provide required matching in digital to analog converters. If switched capacitor DAC is used then small unit capacitors can be used in parallel with the main capacitors. These small capacitors can then be switched in and out by an auto-calibration routine to achieve required accuracy [51].

Digital calibration techniques are also very common in relaxing the matching requirement of DAC components. A family of these techniques is called DEM (Dynamic Element Matching). Unlike other calibration techniques which rely on the absolute value of the components to provide the required matching, DEM only cancels for the variation in components but does not remove that.

Figure 6.1 shows the basic idea behind this technique. In a conventional sigma delta ADC design, output of quantizer is a B-bit thermometer code where each bit of this code controls one element of the DAC (i.e. if the DAC composed of N current sources, each bit controls one of these current sources). In DEM, this one-to-one
correspondence is broken and is controlled by an element selection block. In the simplest approach, element selection logic selects the unit elements randomly and therefore mismatch between the elements do not cause a fix error in some specific codes anymore but the error will be averaged out over all the codes.

Randomization was the first approach to use DEM and it converted the error caused by mismatch to white noise hence raising the noise floor in the DAC. CLA or Clocked averaging is another form of DEM where the element selection is done at each clock cycle according to a periodic sequence. A barrel shifter is used and is shifted by one position after each clock cycle. Therefore, after $2^{B-1}$ clock cycles, the sequence is repeated. Although CLA does not increase the noise floor, it suffers from in-band tones. Due to the repetition of the element selection sequence every $2^{B-1}$ clock cycles, all the tones and distortions are translated by this frequency and if fall inside the signal band, cause the in-band tones. For example $m^{th}$ order harmonics of input signal generates tones around:

$$n \frac{f_s}{2^B-1} + mf_{in}$$

$n,m$ are integers, and $f_s,f_{in}$ are the clock and input frequencies respectively.

If these generated tones fall inside the signal bandwidth, signal to noise ratio will be degraded significantly. Other versions of DEM are also exist that try to mitigate this problem such as ILA (Individual Level averaging), DWA (Data Weighted Averaging) and Noise-shaped DEM. A complete list of these techniques can be found in [53].
6.3. Adaptive Calibration Techniques

As the interest in using digital solutions to analog problems is increasing, digital calibration techniques are becoming more popular in designing high resolution analog to digital converters. Instead of removing the errors caused by non-idealities in analog circuit, digital calibration techniques correct and compensate for these errors based on the information which is buried in the digital output word. The rest of this chapter is dedicated to adaptive digital calibration techniques.

Adaptive refers to the techniques where a digital correction/calibration block corrects for the analog circuit non-idealities. Due to the uncertainties in of the analog circuits’ world (e.g. parameter variation, aging, temperature and supply voltage drift...), the digital correction block is also adaptively changes itself to achieve true compensation in any case. These adaptive calibrations are divided in two groups of
foreground and background techniques. Since all the adaptive techniques proposed in literature are dealing with the noise leakage in MASH sigma delta modulators, this problem is first discussed in section 6.3.1, followed by foreground and background techniques in sections 6.3.2 and 6.2.3 respectively.

6.3.1 Noise Leakage in MASH Sigma Delta ADCs

MASH sigma delta ADCs are commonly used to provide a high order sigma delta modulator by cascading lower order stable modulators. Quantization noise of each stage is used as the input to the next stage except the first stage which is supplied by the original input signal. Outputs of these stages are combined through digital filters together which are designed such that the quantization noise of all stages except the last one are cancelled out. The only quantization noise present at the output would be the quantization noise of the last stage which is filtered by a high pass filter of the order equal to the sum of order of all stages. Theoretically, the more stage cascading together, the more resolution is achieved. In practice, however, the perfect cancellation of quantization noises require perfect matching between the analog loop filters and digital correction filters which is not possible. This results in a leakage of the quantization noise to the output of the modulator that degrades the performance of the ADC. Figure 6.2 pictures this issue for a two stage MASH modulator.
6.3.2. Adaptive Foreground Calibration

The leakage noise problem depicted in figure 6.2 can be removed by using tunable digital correction filters which their coefficients can be tuned during an off-line calibration period. Static and systematic errors can be removed by a foreground calibration, during which a test signal is applied to the input of the modulator,

Coefficients of the adaptive digital correction filter can be tuned to provide the lowest distortion at the output of the modulator as proposed in [54]. In this method, a
calibration signal is applied to the input of the modulator and the output of each stage is measured through some test points. Output of the modulator is also measured which is a function of the output of each stage through the FIR filters as expressed in the following equation:

\[ Y_{TOTAL} = (a_{01} + a_{11} + \ldots + a_{N1})Y_1 + (a_{02} + a_{12} + \ldots + a_{N2})Y_2 + \ldots \]  

(6.1)

where \( Y_{TOTAL} \) is the output of the modulator, \( Y_i \) is the output of the \( i^{th} \) stage and \( a_{ij} \) is the \( i^{th} \) coefficient of the \( j^{th} \) FIR filter.

The most effective off-line method is proposed in [55], [56]. As shown in figure 6.3, a well-defined pseudo-random analog signal is chosen as the calibration signal and is applied to the input of 2-2 modulator. Both of the FIR filters at the output of the modulator are tuned to minimize the following goal function:

\[ E(F_1, F_2) = \sum_{k=1}^{N} (L_y(k) - L_x^{cal}(k - 4))^2 \]  

(6.2)

L is the transfer function of a low pass filter that is designed to separate the signal part from the out of band quantization noise at the output of modulator. The error signal is chosen as the filtered output minus the filtered delay of the input signal. The filter cut-off frequency should be near the signal Nyquist frequency and needs to roll off faster than the rising rate of noise spectrum (e.g. \( \omega^{-5} \)). This calibration technique is used for the two stage 4th order sigma delta modulator of figure (6.3). Results are shown in figures (6-4) and (6-5). Figure (6-4) plots the filter coefficients of FIR adaptive filter versus the adaptive iterations. Figure (6-5) depicts the mean squared error. Simulation shows that signal to noise ratio is improved by 6 dB.
Figure 6.3. Adaptive off-line calibration technique for a MASH sigma delta modulator

Figure 6.4. Convergence of filter coefficients for adaptive off-line calibration
6.3.3. Adaptive Background Calibration

Although effective but the off-line methods interrupt the normal operation of the \( \Sigma \Delta \) converter to apply the calibration signal. Pseudo on-line method is proposed in [53] where at least two converters are working in parallel. One is converting the input signal to digital while the other is being calibrated. The overhead for a two-converter case is 100% but it would decrease when many converters are working in parallel for instance in time interleaved ADCs [57].

Figure 6.5. Adaptive off-line calibration technique for a MASH sigma delta modulator
Another interesting method for background calibration of the $\Sigma\Delta$ ADCs injects a test signal at some point in the ADC feedback loop and uses the correlation between the output and the injected signal as the error signal to tune the FIR filter coefficients. Different approaches to this method are shown in figure (6-6). In Fig. (6-6)-(a), the power of the test signal is measured at the output of the modulator and used as the error signal to modify the coefficients of the digital cancellation filters in both stages of a 2-2 MASH modulator [58]. Test signal is applied to the input of the first stage quantizer and so it goes through the same path to the output as the first stage quantization noise does and hence minimizing the test signal at the output would have the same effect of minimizing the quantization noise of the first stage at the output.

Figure (6-6)-(b) shows another version of this technique, where, again the test signal is injected to the input of the first stage quantizer. The error signal; however, is calculated by calculating the correlation between the output signal and the known test signal [58], [59].

Both methods look attractive, although, both of them have some practical difficulties. In the method described in figure (6-6)-(a), the test signal is chosen to be out of signal band so that the power of the signal does not affect the measurements, but then the measurements is influenced by the quantization noise which is quite high out of signal band and that produces uncertainty in the results. It is evident that in order to prevent extremely difficult requirements for the test signal measurements, the adaptation step size should be variant and change according to the values of the mismatches (e.g. big step size for high value of mismatches and reduced step size for
lower value of mismatches. However, the mismatch values are not known a priori. Method depicted in figure (6-6)-(b) seems to work better but the measurement of the correlation between the test signal and output takes a long time. Simulation results of using this technique in a Leslie-Sing ΣΔ modulator is brought in [59] and it shows that $2^{16}$ points are required to calculate the correlation. The coefficients converge after about 6000 iterations and the coefficients should be stored with at least 16 bits resolutions.

Figure (6-7) shows the correlation-based on0line calibration method for a two stage MASH sigma delta modulator. Similar to the idea of reduced bit-rate sigma delta ADCs, the decimation filters can be placed before the FIR adaptive filters to relax their speed requirements. Moreover, the injected signal can be applied after the quantizer and hence removes the need for the analog summation circuit. The result is shown in figure (6-8) which is a modified correlation-based calibration technique. The two stage MASH sigma delta ADC is simulated with this calibration technique. Output spectrum of the modulator is shown in figure (6-9). It shows that calibration technique was able to decrease the noise leakage terms in the output significantly. Signal to noise ratio is improved by more than 12 dB.
Figure 6.6. (a) On-line compensation using the injected test signal and power measurement

Figure 6.6(b) On-line compensation using the injected test signal and correlation measurement
Figure 6.7 Correlation-based on-line calibration technique for a two stage 4th order sigma delta modulator

Figure 6.8 Modified on-line compensation using the injected test signal and correlation measurement
Figure 6.9 Simulation results for on-line calibration technique depicted in figure 6.8.

6.3.4. Adaptive Technique Using Noise Cancellation

As it was seen in the previous section, adaptive on-line calibration techniques reported in papers are all applied to MASH sigma delta ADCs and are based on correlation between the output signal and a known pseudo-random sequence. This section introduces a novel technique to adaptively calibrate the sigma delta ADC without the need for a calibration signal. The method can be used for MASH as well as single-loop ADCs and is fully-digital, hence, does not add any complexity to the analog circuitry. Section 6.3.4.1 explains the fundamentals of adaptive noise cancellation technique which is a common technique in voice processing to remove
Section 6.3.4.2 proposes the application of this technique to the sigma delta analog to digital converters. Mathematical derivation for the transfer function of this system is also given in this section. Simulation results of applying this technique to a two-stage 4th order sigma delta modulator are given in section 6.3.4.3. In section 6.3.4.4 the performance of this technique with modulated signal inputs are investigated. Some remarks and conclusions are given in section 6.3.5.

6.3.4.1. Adaptive Noise Cancellation

This section describes the fundamentals of ANC (Adaptive Noise Cancellation) technique. Figure 6.10 shows a block diagram of this system. ANC is a common technique in voice processing to remove the sinusoidal interferer from the desired voice signal. As figure 6.10 shows, a microphone is used to collect the voice signal; however, due to the presence of a noise source in the environment, microphone will receive a mix of signal and noise. If the noise source is reachable through a sensor, e.g. another microphone, then a sample of the noise signal can be picked by this sensor. An adaptive FIR filter can be used to generate a replica of the noise signal from the measured noise. The main microphone will receive the corrupted signal and output of the FIR filter and if the filter has generated an exact replica then the noise elements will cancel each other at the main microphone.

In order to use this technique to remove the quantization noise and all other additive noise from the output of ADC, ANC block should be connected to the output of the sigma delta modulator. In the case of a sigma delta modulator, however, noise
source is not available and therefore a modified version of AND, called ALE (Adaptive Line Enhancer) need to be used. Figure 6.11 shows a block diagram of ALE system. As this figure shows in this system, the input to the FIR filter is taken from a delayed version of the original signal and hence no noise sensor is required.

Figure 6.10 Application of adaptive noise canceller in voice processing.

Figure 6.11 Block diagram of ALE (Adaptive Line Enhancer).
When ALE block is connected to the output of a sigma delta modulator, its input will be the sum of desired signal and high passed filtered quantization noise.

\[ x(k) = s(k) + n(k) \]  \hspace{1cm} (6-3)

A delayed version of this signal is then fed to an adaptive filter. The error signal is defined as:

\[ e(k) = d(k) - y(k) \]  \hspace{1cm} (6-4)

where the input signal is chosen as the desired output for the filter:

\[ d(k) = x(k) \]  \hspace{1cm} (6-5)

Using equations (6-3)-(6-5), the following expression for error signal is obtained:

\[ e(k) = s(k) + n(k) - y(k) \]  \hspace{1cm} (6-6)

Least Mean-Squared algorithm (LMS) tunes the filter weights to minimize the above error signal in the mean squared sense.

Taking expectation from both sides of equation (6-6) gives:

\[ E[e^2] = E[(s - y)^2] + E[n^2] + 2E[n(s - y)] \]  \hspace{1cm} (6-7)

Assuming that filter output is independent from noise, the third term in above equation would be zero. The second term \( E[n^2] \) is constant and is equal to the noise variance \( \sigma_n^2 \). Therefore, in order to minimize the expectation of error filter, output \( y \) should be a close estimate of signal \( s \). The assumption that filter output is independent of noise is true only if noise is a wideband random noise and the delay
block in Figure (6-11) is long enough to make the delayed samples of noise completely uncorrelated.

In conclusion, the filter output in ANC provides the best estimate of the signal in mean squared sense providing that the noise is wideband compared to the signal and it is delayed enough to make its samples completely uncorrelated from each other. This fact is illustrated in figure (6-12) and is mathematically proved in the next section.

Figure 6.12 ALE separates the broadband noise from narrowband desired signal.

6.3.4.2. Using ANC in Sigma Delta Converters

The adaptive noise cancellation technique shown in figure (6.11) can be used to improve the signal to noise ratio at the output of sigma delta modulator before the signal goes through low pass and decimation filtering. ANC can improve signal to noise ratio significantly without adding any complexity to the analog circuit. It relaxes
the requirements on the following low pass filter, which usually needs to be implemented by a long FIR filter and based on the application; it may even remove the need for such filtering completely. The most advantage of ANC is its adaptability. Contrary to the fixed coefficient low pass/decimation filters, ANC adapts its coefficients based on its input signal. Figure 6.13 shows how ANC can be a part of digital signal post-processing of a sigma delta modulator.

![Fig 6.13](image)

Figure 6.13.Block Diagram of a sigma delta ADC including Adaptive Noise Cancellation.

In this section, the transfer function of the above system is derived with the assumption that the coefficients of adaptive filter have been already converged to their optimum values given by the Wiener solution. Under this assumption, ANC can be seen as a linear discrete time system and the transfer function is defined as:

\[
H(z) = \frac{Y(z)}{D(z)}
\]  

(6-8)
$Y(z)$ and $D(z)$ are the z-transforms of filter output and desired signal respectively.

Filter output can be written as:

$$y(k) = \sum_{i=0}^{L-1} w_i(k)x(k-i)$$  \hspace{1cm} (6-9)

Since input to the filter, $x(k)$ is the delayed version of the desired signal $d(k)$, equation (6-9) can be re-written as:

$$y(k) = \sum_{i=0}^{L-1} w_i(k)d(k-i-\delta)$$  \hspace{1cm} (6-10)

Using equations (6-8) and (6-10), transfer function of ANC system would be:

$$H(e^{j\omega}) = \sum_{i=0}^{L-1} w_i e^{-j\omega(i+\delta)} \quad -\pi \leq \omega \leq \pi$$  \hspace{1cm} (6-11)

where $w_i$ is the $i$th coefficient of the filter and $\delta$ is the delay line shown in Figure (6.11).

At steady state, LMS algorithm has tuned the filter coefficients to the optimum Wiener solution, which is given by the following equation:

$$w = R_{xx}^{-1}P$$  \hspace{1cm} (6-12)

In equation (6-12), $R_{xx}$ is the auto-correlation matrix of input signal and $P$ is the cross-correlation vector between the filter input and desired signal of the filter.

Following steps show the derivation for these two matrices.

**Calculate Auto-correlation matrix $R_{xx}$**

Input of the adaptive filter, $x$, is composed of the sinusoidal signal and the quantization noise shaped by the sigma delta modulator. Since signal and noise are
uncorrelated, the auto-correlation of the input data would be sum of auto-correlation of
the signal and auto-correlation of the quantization noise:
\[ R_{xx} = R_{ss} + R_{nn} \]  
(6-13)

First, we calculate the auto-correlation of signal. Considering a sinusoidal signal:
\[ s(k) = c \cos(\omega_0 * k + \phi) \]  
(6-14)

\( \phi \) is a random phase uniformly distributed on \([- \pi \quad \pi]\).

The auto-correlation is calculated as:
\[ r_{ss}(l) = E\{s(k)s(k-l)\} = \frac{c^2}{2}\cos^2(\omega_0 l) \]  
(6-15)

Auto-correlation matrix \( R_{xx} \) is a \( L \times L \) symmetric matrix with each component
calculated as in equation (6-15).
\[
R_{ss} = \frac{c^2}{2} \begin{pmatrix}
1 & \cos(\omega_0) & \cos(2\omega_0) & \ldots & \cos(L-1)\omega_0 \\
\cos(\omega_0) & 1 & - & \ldots & - \\
\cos(2\omega_0) & - & 1 & \ldots & - \\
& \ldots & \ldots & \ldots & \ldots \\
& - & \ldots & - & 1
\end{pmatrix}
\]  
(6-16)

In order to calculate auto-correlation of noise, it should be noted that in this case noise
is the shaped quantization noise. Assuming a white uniformly distributed quantization
noise, power spectral density of the quantization noise is:
\[ S_{quantization}^2(w) = \frac{\Delta^2}{12f_s} \]  
(6-17)

After being shaped by the noise transfer function of the \( N \)th order sigma delta
modulator, the power spectral density would be:
\[ S_n^2(w) = \frac{\Delta^2}{12f_s} \left| 1 - z^{-1} \right|^{2N} \]  
\[ (6-18) \]

Substituting \( z = e^{j2\pi \frac{f}{f_s}} \) in above equation results in:

\[ S_n^2(w) = \frac{\Delta^2}{12f_s} \omega^{2N} \]  
\[ (6-19) \]

Auto-correlation function and power spectral density of a stationary stochastic process form a Fourier transform pair; hence, knowing the power spectral density of noise, auto-correlation is found as:

\[ r_{nn}(l) = \frac{1}{2\pi} \int_{-\pi}^{\pi} S_n^2(\omega)e^{j\omega l} \, d\omega \]  
\[ (6-20) \]

However, different samples of noise are uncorrelated and hence equation (6-20) is zero for all non-zero values of \( l \) and auto-correlation matrix of noise will be:

\[ R_{nn} = A I_{L \times L} \]  
\[ (6-21) \]

where:

\[ A = \frac{\Delta^2 \omega^{2N}}{12(2N+1)f_s^{2N+1}} \]  
\[ (6-22) \]

Finally, auto-correlation matrix of filter input data \( R_{xx} \) can be written using equations (6-13), (6-16) and (6-21):
Equation (6-12) needs the inverse of matrix \( R_{xx} \). In order to write a simple closed form expression for \( R_{xx}^{-1} \), matrix \( \Gamma_{L^*2} \) is defined as:

\[
\Gamma = \frac{1}{2} C \begin{bmatrix}
1 & 1 \\
\frac{e^{-j \omega_0}}{e^{j \omega_0}} & \frac{e^{j \omega_0}}{e^{-j \omega_0}} & \frac{e^{j \omega_0}}{e^{-j \omega_0}} & \cdots & \frac{e^{j (L-1) \omega_0}}{e^{-j (L-1) \omega_0}} \\
\end{bmatrix}
\]  

(6-24)

Complex conjugate (Hermitian) of this matrix would be:

\[
\Gamma = \frac{1}{2} C \begin{bmatrix}
1 & 1 \\
\frac{e^{j \omega_0}}{e^{-j \omega_0}} & \frac{e^{-j \omega_0}}{e^{j \omega_0}} & \frac{e^{-j \omega_0}}{e^{j \omega_0}} & \cdots & \frac{e^{-j (L-1) \omega_0}}{e^{j (L-1) \omega_0}} \\
\end{bmatrix}
\]  

(6-25)

It can be easily shown that \( R_{xx} \) can be written as:

\[
R_{xx} = \Gamma \Gamma^H + R_{nn}
\]  

(6-26)

where \( R_{nn} \) is the auto-correlation of the noise matrix defined in equation (6-21).

Now, the matrix inversion lemma can be used to find the inverse of \( R_{xx} \). Matrix inversion lemma declares that if Matrix \( A \) is a positive definite matrix and can be written as:
\[ A = B^{-1} + CD^{-1}C^H \]  
(6-27)

then the inverse of this matrix would be:

\[ A^{-1} = B - BC(D + C^HBC)^{-1}C^HB \]  
(6-28)

Using this lemma and equation (6-26), inverse of auto-correlation matrix \( R_{xx} \) can be written as:

\[ R_{xx} = R_{nn}^{-1} - R_{nn}^{-1}(I + \Gamma^H R_{nn}^{-1}\Gamma)^{-1}\Gamma^H R_{nn}^{-1} \]  
(6-29)

**Calculate Cross-correlation vector \( P \)**

Cross-correlation vector is calculated as the correlation between the desired signal and the input signal, which is the delayed version of desired signal by \( \delta \) samples. Since noise components are uncorrelated from each other, only signal components will appear in cross-correlation vector:

\[ P_{L\times1}(i) = E[s(k - \delta - i)s(k)] = \frac{c^2}{2} \cos \omega_0 (\delta + i) \quad i = 0, 1, \ldots, L - 1 \]  
(6-30)

\( P \) can be written in terms of \( \Gamma \) as follow:

\[ P = \Gamma v_D \]  
(6-31)

where \( v_D \) is a vector defined as:

\[ v_D = \frac{C}{2} \begin{bmatrix} e^{-j\omega_0 \delta} \\ e^{j\omega_0 \delta} \end{bmatrix} \]  
(6-32)

Using equations (6-12), (6-26) and (6-30), wiener coefficient of noise canceller adaptive filter in steady state can be written as:
\[ w = (R_{nn}^{-1} - R_{nn}^{-1} \Gamma (I + \Gamma^H R_{nn}^{-1} \Gamma)^{-1} \Gamma^H R_{nn}^{-1}) \Gamma v_D \] (6-33)

Substituting equation (6-33) in (6-11) and after some mathematical manipulation, transfer function of the ANC system is calculated as:

\[ H(e^{j\omega}) = \frac{c^2}{4A\Delta_R} (\alpha(\omega)e^{-j\omega_0\delta} + \beta(\omega)e^{j\omega_0\delta})e^{-j\omega\delta} \] (6-34)

where:

\[ \alpha(\omega) = \left( \frac{c^2}{4A} + 1 \right) \sum_{i=0}^{L-1} e^{-j(\omega-\omega_0)i} - \frac{c^2}{4A} \sum_{i=0}^{L-1} e^{j2\omega_0iL} \sum_{i=0}^{L-1} e^{-j(\omega+\omega_0)i} \] (6-35)

\[ \beta(\omega) = \alpha^*(-\omega) \] (6-36)

\[ \Delta_R = \det(I + \Gamma^H R_{nn}^{-1} \Gamma)^{-1} = \left( \frac{c^2}{4A} + 1 \right) - \frac{c^4}{16A^2} \sum_{i=0}^{L-1} e^{j2\omega_0iL} \sum_{i=0}^{L-1} e^{-j2\omega_0i} \] (6-37)

In order to better understand the performance of ANC, equation (6-34) is plotted in Figure (6-14) for a 40th order FIR filter. The simulation is done for a second order sigma delta modulator with 7-level internal quantizer. The result shows that the performance of ANC resembles a bandpass filter. The center frequency of this filter locates at the frequency of the sinusoidal input. As we move away from the input signal frequency, filter provides significant attenuation to the noise. Although the filter does not work that efficiently in lower frequencies, its response can be improved by increasing the filter order. Transfer function of this filter for L=40 also shows a considerable ripples out of filter band which is also decreased significantly as the filter order is increased.
6.3.4.3. Simulation Results

In this section the adaptive noise cancellation technique is applied to the same 4\textsuperscript{th} order sigma delta modulator designed in chapter 5 (refer to figure 5.9). As it was discussed in chapter 5, the conventional 4\textsuperscript{th} order sigma delta modulator can satisfy the requirements of GSM and WCDMA standards, however, it is not able to provide enough resolution for WLAN system as listed in table 5.5. Simulation results brought in this section show that the performance of this sigma delta modulator can be boosted using active noise cancellation technique so that it can be used for WLAN system as
well. Block diagram of this modulator is repeated here in figure (6-15) with the noise canceller block added to its output. For all the simulations done in this section, a 20\textsuperscript{th} order IIR filter is used as the adaptive filter and the length of delay line is chosen as \( \delta = 6 \). Least mean square algorithm is used with the adaptation size of \( \mu = 1e^{-4} \) to tune the coefficients of the IIR adaptive filter using “Output Error Method” as explained in [60]. The transfer function of the IIR filter can be written as:

\[
H(z) = \frac{\sum_{i=0}^{N} a_i z^{-i}}{1 - \sum_{i=1}^{N} b_i z^{-i}} \tag{6-35}
\]

where \( N \) is the order of the filter and is chosen as 20 for these simulations and \( a_i \)s and \( b_i \)s are the tunable coefficients.

ADC performance is studied for a single tone sinusoidal input. The fourth order modulator is designed for WLAN standard with 20MHz channel bandwidth and 10MHz signal bandwidth. Signal to noise ratio is 43 dB before applying the ANC block which will be improved to 58 dB after the noise canceller. A block diagram of the whole system is given in Figure (6-15). Figure (6-16) shows the signal to noise ratio improvement before and after ANC. In these simulations, the thermal noise has been ignored. As it was explained in the previous section, the extraction of signal from the quantization noise is done by ANC due to the fact that quantization noise and signal are independent and quantization noise samples are uncorrelated from each other. The same statement is also true for the input referred thermal noise of the ADC and one expects that ANC can also decrease the amount of thermal noise at the output.
of the converter. In order to show that, Figure (6-17) depicts the SNR performance of the same 4\textsuperscript{th} order modulator in presence of 6\(\mu\)v/Hz input referred thermal noise.

**Figure 6.15.** Block diagram of the sigma delta modulator with active noise cancellation.

Figure (6.18) illustrates the SNR performance after using noise cancellation technique. The attenuation of thermal noise is significant and is equal to 100dB. The high passed shaped noise in this figure is due to the quantization noise of the 4\textsuperscript{th} order sigma delta modulator. As the figure shows, after using noise cancellation, the level of quantization noise and thermal noise will be brought down even below the initial noise floor.
Figure 6.16. SNR performance after and before using ANC block for a sinusoidal input.

Figure 6.17. ANC performance in presence of thermal noise.
Figure 6.18. Thermal noise shaped by the 4\textsuperscript{th} order modulator and ANC block.

Figure 6-18 also emphasizes the fact that the more dynamic the noise is, the more improvement can be achieved by using ANC technique. Using higher resolution quantizer inside the sigma delta modulator makes the quantization noise a better example of a uniformly distributed random noise and hence similar to thermal noise it will experience a more significant attenuation using this technique.

6.3.4.4. Effect of Noise Canceller on Modulated Signals

In the previous section, noise cancellation technique was tested with a pure sinusoidal signal and also in the presence of thermal noise. Mathematical derivation of ANC transfer function given in section 6.3.4.2 was for a sinusoidal input too. ANC, however, can perform as effectively with a modulated signal. In order to investigate that, the sigma delta modulator is fed with a BPSK modulated signal. Figures (6.19)
and (6.20) show the eye diagram of the output of the modulator with and without using noise cancellation. Figure (6-20) clearly illustrates a wider eye (less noise) than Figure (6-19). BPSK, QPSK and QAM family of modulations, are combinations of orthogonal sinusoidal signals, however, it is interesting to see how ANC works for a non-sinusoidal modulation such as MSK (Minimum Shift Keying). Figures (6-21) and (6-22) bring the results for a MSK modulated signal. Again the quantization noise is reduced after noise cancellation which is evident from a wider eye diagram.

6.3.4.5. Remarks and Conclusions on Adaptive Noise Cancellation

A simple Adaptive Noise Cancellation technique is proposed in this section that can be used to boost the signal to noise ratio of sigma delta modulators. Mathematical derivation of the system shows that ANC uses the statistical difference between the signal and noise and the fact that noise samples are uncorrelated from each other whereas signal samples have a much stronger correlation. Simulation results for different modulated and non-modulated signals show that ANC can effectively remove the in-band as well as remaining out of band quantization noise and also reduce the thermal noise of the sigma delta modulator significantly. Another advantage of the proposed technique is that it is all implemented in digital and hence brings no complexity to the analog circuitry.
Figure 6.19. Eye diagram for the BPSK modulated signal at the output of Sigma Delta modulator.

Figure 6.20. Eye diagram for the BPSK modulated signal after noise cancellation.
Figure 6.21. Eye diagram for the MSK modulated signal at the output of Sigma Delta modulator.

Figure 6.22. Eye diagram for the MSK modulated signal after noise cancellation.
CHAPTER 7

ADAPTIVE TECHNIQUES FOR CALIBRATION OF PIPELINE ADCS

7.1. Introduction

The idea of using adaptive techniques for compensation of analog imperfections in sigma delta ADCs can be generalized to other types of data converters as well. Pipeline ADCs for example are competitors of sigma delta modulators when it comes to wireless applications. Pipeline ADCs can work in higher speeds thanks to the pipelining nature of these converters. Higher resolution, however, comes with large power consumption since these converters need highly accurate analog circuitry. Calibration techniques can be used to compensate for analog imperfections and hence relax the requirements on the analog part by using more complex digital post-processing methods. This chapter briefly reviews some of the calibration techniques used in pipeline ADCs and proposes an adaptive scheme that can be used to compensate for linear as well as nonlinear errors in pipeline stages. A review of the fundamentals of pipeline ADCs are covered in section 7.2. Section 7.3 discusses the
calibration techniques proposed in recent literatures and section 7.4 brings the proposed scheme.

7.2. Fundamental of pipeline ADC

In a pipeline analog to digital converter the required resolution is achieved through a number of stages that each resolves a part of the final digital output. All stages of pipeline ADC are working concurrently on different samples of the input signals therefore the throughput is increased.

Figure 7.1 depicts the general block diagram of a pipeline ADC. It is composed of different stages where each stage is working on the residue of its previous stage. Each stage consists of an analog to digital sub-converter (ADCS), digital to analog sub-converter (DACS), analog summation and a gain stage. Analog non-idealities present in each of these blocks can degrade the resolution of the converter.

Figure 7.1 Block diagram of a pipeline ADC.
The most familiar compensation technique which is used in pipeline ADCs is the Redundant Sign Digit (RSD) coding which is used to relax the requirement on the ADSC comparators offset. In order to see how the ADSC offset can cause error in the output of converter figure (7.2) shows the residue plot of a single bit per stage pipeline versus the input signal. As the input signal changes within \( -v_{\text{ref}} \) and \( v_{\text{ref}} \), the residue is confined inside the \([-v_{\text{ref}}, v_{\text{ref}}]\), however if the comparator has an offset, figure (7.3) shows that the residue signal can go out of the range. The overflow causes an error in the resolved code by the next stage and all the stages down the pipeline chain. Overflow can be prevented by adding some redundant bits to each stage which also adds some margin for the comparator offset. Figure (7.4) shows the same pipeline stage with added one bit of redundancy. This configuration is known as 1.5\text{bits/stage} since only two comparators (one less than a full 2-bit ADSC) is needed. It can be seen from the figure that offsets as large as \( v_{\text{ref}}/4 \) can be tolerated without overflow.

Figure 7.2 Residue plot of a single bit/stage pipeline ADC.
Figure 7.3 Residue plot of a single bit/stage pipeline ADC with comparator offset.

Figure 7.4 Residue plot of a 1.5 bits/stage pipeline ADC ideal case and with comparator offset.

7.3. Calibration techniques for pipeline ADC

Redundant Sign Digit (RSD) coding solves the comparator offset problem however; there are other sources of errors that limit the achievable resolution in pipeline converters.
Component mismatches rise to DAC error that degrade the accuracy of conversion. A digital on-line cancellation technique has been proposed in [61] that can solve this problem. It is also shown in [62] that the errors in the DAC can be lumped into the gain errors of interstage gain and be cancelled through the techniques used for interstage gain calibration as shown in figure (7.5). The problem of calibrating the pipeline ADC is therefore narrowed down to compensating for the errors in this equivalent interstage gain.

Most of the calibration techniques proposed in literatures compensate for the linear gain error in pipeline stages. Calibration techniques that account for nonlinearities [62]-[64] are based on the correlation between an injected random test signal and the converter uncalibrated output code. Correlation based methods have the following drawback:

**Modeled-based**

Techniques discussed in [62]-[64] are assuming a third order nonlinear model for the gain stage. Generalization of these techniques to the case where the gain stage model includes higher order terms is not trivial and would be very complicated if not impossible.

**Slow convergence**

These methods are based on the fact that the injected random signal is completely uncorrelated from the input signal. Correlation measurement, however, needs many data points so that the input signal is averaged out in the calculations. It usually needs millions of data to correctly estimate the coefficients of the gain stage model [62].
Add analog complexity

Test signal can be injected before ADSC, after ADSC or after DASC. Each option adds some complexity to the rest of the circuit.

If added before ADSC, test signal needs to have an accurate analog value. Therefore, another DAC is usually used to generate the accurate and controlled test signal. Adding a random signal before ADSC has an effect similar to changing the comparator trip points randomly, therefore, the allowable range for comparator offsets is reduced by the value of the test signal.

Adding the test signal after DASC is the most common way proposed in literatures. The benefit is that injected signal is digital which its value can be controlled very accurately and hence no extra DAC is needed. It turns out that injection of a signal after ADSC will decrease the input signal range (assuming that input to all stages are intended to kept the same and between +/-Vref). In order to prevent the decrease in the input signal range, the resolution of ADSC needs to be increased. Number of levels in the DASC also needs to be increased since injected random signal adds to the number of possible inputs to the DASC [65].

Test signal can be also injected after DASC which then has the same problem as when it is injected before ADSC and that is the injected signal needs to have an accurate analog level. Therefore an extra DAC is needed [66].
7.4. Proposed adaptive nonlinear correction

An adaptive calibration scheme is proposed here that solves many problems with the existence correlation-based methods. The proposed technique is an online calibration scheme and does not need any test signal, hence, unlike the methods suggested by [62], [63] it does not need extra resolution in the internal ADSC and...
DASC to accommodate for an injected signal. It is completely a post-processing method and hence no modification to the analog circuitry is required.

A block diagram of the system is shown in figure 7.6. Pipeline ADC is divided into two parts: the stage under calibration and the rest of pipeline stages to the right which is called backend. Similar to correlation-based calibration signals, the accuracy of calibration depends on the accuracy of the backend stage. Hence, in the following calculations, the residue signal $y$ is considered equal to its digitized value by the backend stage. $y$ is labeled as uncalibrated digital output in the figure. Errors are due to the non-ideal gain stage which its transfer function is shown as a general function $f(\cdot)$ in this figure. In the following calculation, non-ideal gain stage is modeled by a polynomial of an arbitrary order. This non-ideal gain stage limits the accuracy of $y$, input to the backend, which in ideal case should be as accurate as the resolution of the total ADC minus the effective number of bits resolved by the first stage. For example in a pipeline ADC with two effective bits in the first stage, 14bits total accuracy can not be achieved unless $y$ is accurate to at least 12bits. In a conventional design usually redundancy is added to get enough resolution, for example to get 14bits total accuracy a 16 bit pipeline ADC is used and the total digits are truncated to 12. Adding redundant stages to the backend, however, is not an efficient solution in terms of power and area.
Calibration method shown in figure (7.6) calculates an accurate estimate of residue signal $x$ called $\hat{x}$. $\hat{x}$ can be used to regenerate a digital estimate of the input signal $\hat{V}_{\text{in}}$. This calibration scheme works as follow:

Although $x$ and $y$ are related by a nonlinear transfer function. At each instant of time and for each specific value of $x$, a linear gain can be defined that relates $x$ and $y$ as follow:

$$m_i = \frac{y}{x}$$  \hspace{1cm} (7-1)

This gain however is variable as shown in figure 7.7 and also unknown since the nonlinear interstage gain function $f(.)$ is unknown. As shown in figure 7.6, by knowing this gain an estimate of $x$ can be calculated from backend digital output $y$. In order to provide an error (reference) signal to continuously adapt this gain, an estimate of $y$ is generated by using a nonlinear function $g(.)$. A tangent hyperbolic function is used in this analysis since it resembles the nonlinearity present in interstage gains very well. It has a fairly linear behavior near zero and shows a gain compression effect for larger input values. $g(.)$ resembles the unknown function $f(.)$ since it relates the same variables $x$ and $y$ together. Therefore, $g(.)$ also needs a tunable parameter to generate the same mapping between $x$ and $y$ as $f(.)$ does for each instant of time. The instant equality of $f(.)$ and $g(.)$ are shown in figure 7.8.

Estimates of $x$ and $y$ are related as follow:

$$\hat{x} = \frac{y}{m_i}$$  \hspace{1cm} (7-2)

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\[
\hat{y} = \frac{1 - e^{-\beta \hat{x}}}{1 + e^{-\beta \hat{x}}}
\]  

(7-3)

Since \( g(.) \) generates an estimate of \( y \) in its output, an error signal can be defined as follow to tune the value of the \( m_i \) as well as \( \beta \):

\[
e = y - \hat{y}
\]  

(7-4)

Objective function is chosen to be a quadrature function of this error as:

\[
J = \frac{1}{2} E(e^2)
\]  

(7-5)

The steepest gradient method is used to update \( m_i \) and \( \beta \) such that the above objective function is minimized. The formula for updating \( m_i \) is derived as:

\[
m_i[k + 1] = m_i[k] - \mu m_i \nabla J_{m_i}
\]  

(7-6)

In the above equation \( m_i[k] \) is the value of \( m_i \) at instant \( k \) and \( \mu m_i \) is the adaptation step size. \( \nabla J_{m_i} \) is calculated as:

\[
\nabla J_{m_i} = e \frac{de}{dm_i} = -(y - \hat{y}) \frac{d\hat{y}}{dm_i}
\]  

(7-7)

\[
\hat{y} = \frac{1 - e^{-\frac{y}{m_i}}}{1 + e^{-\frac{y}{m_i}}}
\]  

(7-8)

\[
\frac{d\hat{y}}{dm_i} = -2\beta y e^{-\frac{y}{m_i}} \left( \frac{-\beta \frac{y}{m_i}}{(1 + e^{-\frac{y}{m_i}})^2} \right)
\]  

(7-9)

and finally the equation for updating \( m_i \) can be written as:
\[ m_i[k+1] = m_i[k] + \mu_{m_i} \frac{2\beta y}{m_i^2} \frac{-\beta \frac{y}{m_i}}{e^{\frac{-\beta \frac{y}{m_i}}{(1+e^{-\beta \frac{y}{m_i}})^2}}} \quad (7-10) \]

The equation for updating \( \beta \) is also calculated in a similar way as:

\[ \beta[k+1] = \beta[k] - \mu_{\beta} \nabla J_{\beta} \quad (7-11) \]

\[ \nabla J_{\beta} = e \frac{de}{d\beta} = -(y - \hat{y}) \frac{d\hat{y}}{d\beta} \quad (7-12) \]

\[ \frac{d\hat{y}}{d\beta} = 2y \frac{e^{-\beta \frac{y}{m_i}}}{m_i} \frac{1}{(1+e^{-\beta \frac{y}{m_i}})^2} \quad (7-13) \]

\[ \beta[k+1] = \beta[k] + \mu_{\beta} \frac{2y}{m_i} \frac{e^{-\beta \frac{y}{m_i}}}{(1+e^{-\beta \frac{y}{m_i}})^2} \quad (7-14) \]

The proposed method is simulated for a 14 bit pipeline ADC with 3 effective bits at the first stage. The nonlinear interstage gain at first stage is modeled with a 5th order polynomial as:

\[ y = 7.99x - 0.05x^3 - 0.01x^5 \]

Adaptation step sizes are chosen as:

\[ \mu_{m_i} = 0.8 \]

\[ \mu_{\beta} = 0.2 \]

Results are shown in figures (7-9)-(7-11) for convergence of \( m_i \), \( \beta \) and error \( e \) respectively.
Figure 7.6 Block diagram of the proposed scheme.

Figure 7.7 Variable gain $m_i$ that relates instant values of $x$ and $y$. 

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Figure 7.8 Variable gain $\beta$ that generates equality between $g(.)$ and $f(.)$ (the blue dotted line is $f(.)$ and red and purple lines are two $g(.)$ that generate the same mapping between $x$ and $y$ for the two shown samples).

Figure 7.9 Convergence of $\beta$ coefficient for a constant input signal $V_{in} = 0.5714V_{ref}$. 
Figure 7.10 Convergence of $m_i$ coefficient for a constant input signal $V_{in} = 0.5714V_{ref}$.

Figure 7.11 Error signal defined as $e = y - \hat{y}$ for a constant input signal $V_{in} = 0.5714V_{ref}$. 
CHAPTER 8

CONCLUSION

In this dissertation, design of high performance sigma delta converters for wireless communication applications were studied in a top-down approach. It started from the study and design of the multi-standard wireless systems. It was shown that system design can be seen as budget analysis for noise and nonlinearity of each block in the receiver chain such that the overall carrier to noise plus distortion ratio was better than the value specified by standard. During these system designs it became evident that the ADC specifications trade-off with the complexity of the baseband blocks that precede the converter. Variable gain amplifier relaxes the ADC dynamic range and filters ease the requirement on ADC linearity. It was also shown that even if a nyquist rate ADC is used in receiver, few orders of oversampling ratio are required to relax the requirement on anti-aliasing filter. Therefore, sigma-delta ADCs are an excellent candidate for these applications since they can exploit this oversampling ratio to
provide higher resolution at lower power consumption compared to nyquist rate converters.

Two special cases were considered: WiMAX/WLAN and 4th generation of cell phones. The specifications derived for the analog to digital converter in 4th generation cell phones were used throughout the thesis to explore different designs of sigma delta ADCs. These specifications are repeated in table 7.1.

<table>
<thead>
<tr>
<th>Standard</th>
<th>Channel Bandwidth</th>
<th>Clock Frequency</th>
<th>Oversampling Ratio</th>
<th>Required Dynamic Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>WCDMA</td>
<td>3.84 MHz</td>
<td>30.72 MHz</td>
<td>8</td>
<td>52 dB</td>
</tr>
<tr>
<td>GSM</td>
<td>200 KHz</td>
<td>51.2 MHz</td>
<td>128</td>
<td>70 dB</td>
</tr>
<tr>
<td>WLAN (11.b)</td>
<td>22 MHz</td>
<td>88 MHz</td>
<td>4</td>
<td>51 dB</td>
</tr>
</tbody>
</table>

Table 8.1. Specification for analog to digital converter in the proposed GSM/WCDMA/WLAN receiver.

The thesis then presented two designs for sigma delta modulator based on single loop and MASH structures. The single loop design was a 4th order modulator that used optimum location for zeros of noise transfer function to maximize the signal to noise ratio. The optimal filter transfer function was then synthesized using two biquad filters. It was shown that although the single loop modulator used a very aggressive
noise shaping that outperform the conventional MASH designs, it had stability issues. Higher order single loop designs have irrecoverable instability cycles which mean that if they become unstable they can not be recovered unless the modulator is being reset. MASH modulators, however, cascade the first or 2\textsuperscript{nd} order stable stages to make a high order modulator without compromising stability.

A two stage 4\textsuperscript{th} order MASH modulator was designed that could be used to digitize GSM and WCDMA systems. It turned out that this modulator can not provide enough resolution for the broadband signal in WLAN standard. The conventional solution is to add another 2\textsuperscript{nd} order stage but that costs more power consumption and considerable increase in die size. Moreover, higher order MASH modulators also have another problem known as noise leakage which stems from the mismatch between the analog filters and digital ones and cause an incomplete cancellation of quantization noises at the output of the modulator. In deep submicron technology that design of high performance analog is becoming more difficult, the noise leakage is also more prominent.

In order to provide enough resolution for WLAN, a new method is then proposed based on active noise cancellation technique. The proposed technique uses a well-known method in speech processing that extracts the voice signal from a corrupting noise. Using the noise canceller block at the output of the sigma delta modulator can help to extract the desired signal form the quantization noise.

Mathematical derivation of the system shows that ANC uses the statistical difference between the signal and noise and the fact that noise samples are
uncorrelated from each other whereas signal samples have a much stronger correlation. Simulation results for different modulated and non-modulated signals show that ANC can effectively remove the in-band as well as remaining out of band quantization noise and also reduce the thermal noise of the sigma delta modulator significantly. The advantage of this technique to the other ways of increasing SNR is that it is completely a digital post-processing technique that is implemented in the digital domain. Therefore no complexity is added to the analog circuitry. The two stage 4th order MASH sigma delta modulator equipped with this noise canceller block is then the solution to 4G system. The achieved results are summarized in table 7.2.

<table>
<thead>
<tr>
<th>Structure of MASH Modulator</th>
<th>Clock Frequency</th>
<th>Required Dynamic Range</th>
<th>Achieved Dynamic Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>WCDMA 2-2</td>
<td>30.72 MHz</td>
<td>52 dB</td>
<td>56 dB</td>
</tr>
<tr>
<td>GSM 2</td>
<td>51.2 MHz</td>
<td>70 dB</td>
<td>72 dB</td>
</tr>
<tr>
<td>WLAN (11.b) 2-2 with ANC</td>
<td>88 MHz</td>
<td>51 dB</td>
<td>58 dB</td>
</tr>
</tbody>
</table>

Table 8.2. Achieved performance for the two stage 4th order sigma delta modulator designed for GSM/WCDMA/WLAN receiver.
**Future Work**

As it was shown in chapter 6, the quality factor of the adaptive noise cancellation filter is increased with the order of the filter. Higher order FIR filters with large number of taps consume power and take large die size. IIR filters decrease the required filter order considerably but with the expense of stability. Frequency domain implementation of adaptive filters is also another interesting solution that is especially attractive for OFDM based systems. In this approach, the adaptive tuning of the filter coefficients are done in frequency domain, therefore FFT and IFFT are required to transfer the filter input signal to frequency domain and to convert the output of the filter back to time domain. OFDM systems are equipped with FFT and IFFT functions and hence these facilities can be used for the noise cancellation purpose as well.

Another interesting project is to explore the effectiveness of the noise canceller in presence of tones at the output of the modulator. Single bit modulators are especially attractive due to the fact that they need a single bit, inherently linear DAC. These modulators, however, suffer from a large mount of tones at their output spectrum. Presence of tones indicates that the quantization noise is no longer uncorrelated with the signal. This fact can degrade the effectiveness of the proposed noise cancellation technique which assumes the signal and quantization noise are completely uncorrelated.
BIBLIOGRAPHY


[21] -., “Orthogonal frequency division multiplexing”,

[22] IEEE802.16 standard.


[52] \url{http://www.analog.com/en/content/0,2886,759\%255F%255F7017,00.html}


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APPENDIX A

SYSTEM DESIGN EXCEL SHEETS FOR WIMAX/WLAN
<table>
<thead>
<tr>
<th>Gain</th>
<th>Antenna</th>
<th>RF-Filter</th>
<th>I.F. Switch</th>
<th>LNA</th>
<th>Mixer</th>
<th>VGA</th>
<th>Filter</th>
<th>VGA1</th>
<th>Filter</th>
<th>ADC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum Gain AV dB</td>
<td>0</td>
<td>1.5</td>
<td>1.5</td>
<td>23</td>
<td>5</td>
<td>0</td>
<td>3</td>
<td>50</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Maximum Gain AV dB</td>
<td>1</td>
<td>0.8414</td>
<td>0.841395</td>
<td>14.43</td>
<td>1.770</td>
<td>1</td>
<td>0.7079</td>
<td>316.23</td>
<td>0.71</td>
<td>1</td>
</tr>
<tr>
<td>11b Maximum Gain AV dB</td>
<td>1</td>
<td>0.8414</td>
<td>0.841395</td>
<td>1.770</td>
<td>1.770</td>
<td>1</td>
<td>0.7079</td>
<td>316.23</td>
<td>0.71</td>
<td>1</td>
</tr>
<tr>
<td>Minimum Gain AV dB</td>
<td>0</td>
<td>1.5</td>
<td>1.5</td>
<td>0</td>
<td>5</td>
<td>0</td>
<td>3</td>
<td>33</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>11b Max. Gain AV dB</td>
<td>0</td>
<td>1.5</td>
<td>1.5</td>
<td>5</td>
<td>5</td>
<td>0</td>
<td>3</td>
<td>30</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>11b Minimum Gain AV dB</td>
<td>0</td>
<td>1.5</td>
<td>1.5</td>
<td>5</td>
<td>5</td>
<td>0</td>
<td>3</td>
<td>30</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Gain for Test1 adjacent channel dB</td>
<td>0</td>
<td>1.5</td>
<td>1.5</td>
<td>0</td>
<td>10</td>
<td>0</td>
<td>3</td>
<td>10</td>
<td>3</td>
<td>0</td>
</tr>
<tr>
<td>Gain for Test1 alternate channel dB</td>
<td>0</td>
<td>1.5</td>
<td>1.5</td>
<td>0</td>
<td>5</td>
<td>0</td>
<td>3</td>
<td>0</td>
<td>3</td>
<td>0</td>
</tr>
<tr>
<td>Gain for Test2 adjacent channel dB</td>
<td>0</td>
<td>1.5</td>
<td>1.5</td>
<td>0</td>
<td>10</td>
<td>0</td>
<td>3</td>
<td>10</td>
<td>3</td>
<td>0</td>
</tr>
<tr>
<td>Gain for Test2 alternate channel dB</td>
<td>0</td>
<td>1.5</td>
<td>1.5</td>
<td>0</td>
<td>10</td>
<td>0</td>
<td>3</td>
<td>0</td>
<td>3</td>
<td>0</td>
</tr>
<tr>
<td>80.11b Gain for Interferer Test dB</td>
<td>0</td>
<td>1.5</td>
<td>1.5</td>
<td>0</td>
<td>10</td>
<td>0</td>
<td>3</td>
<td>20</td>
<td>3</td>
<td>0</td>
</tr>
<tr>
<td>Maximum Signal Level dBv</td>
<td>-43</td>
<td>-44.5</td>
<td>-46</td>
<td>-46</td>
<td>-41</td>
<td>-41</td>
<td>-44</td>
<td>-11</td>
<td>-14</td>
<td>-11</td>
</tr>
<tr>
<td>Minimum Signal Level dBv</td>
<td>-78</td>
<td>-79.5</td>
<td>-81</td>
<td>-58</td>
<td>-53</td>
<td>-53</td>
<td>-56</td>
<td>-6</td>
<td>-9</td>
<td>-9</td>
</tr>
<tr>
<td>Min. Signal for Interferer Tests 1 dBv</td>
<td>-75</td>
<td>-76.5</td>
<td>-78</td>
<td>-78</td>
<td>-68</td>
<td>-68</td>
<td>-71</td>
<td>-61</td>
<td>-64</td>
<td>-61</td>
</tr>
<tr>
<td>Signal for Inter. Tests 1 for alternate channel[dBv]</td>
<td>-75</td>
<td>-76.5</td>
<td>-78</td>
<td>-78</td>
<td>-73</td>
<td>-73</td>
<td>-76</td>
<td>76</td>
<td>-79</td>
<td>-79</td>
</tr>
<tr>
<td>Signal Level for Interferer Tests 2 for alternate channel[dBm]</td>
<td>-53</td>
<td>-54.5</td>
<td>-56</td>
<td>-56</td>
<td>-46</td>
<td>-46</td>
<td>-49</td>
<td>-49</td>
<td>-52</td>
<td>-52</td>
</tr>
<tr>
<td>11b Max. Signal Level [dBm]</td>
<td>-10</td>
<td>-11.5</td>
<td>-13</td>
<td>-13</td>
<td>-8</td>
<td>-8</td>
<td>-11</td>
<td>-11</td>
<td>-14</td>
<td>-14</td>
</tr>
</tbody>
</table>

Figure A.1 Gain distributions in the WiMAX/WLAN receiver chain.
### Signal Levels

<table>
<thead>
<tr>
<th></th>
<th>Antenna</th>
<th>RF-Filter</th>
<th>R/T Switch</th>
<th>LNA</th>
<th>Mixer</th>
<th>VGA</th>
<th>Filter</th>
<th>VGA1</th>
<th>Filter</th>
<th>ADC</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Maximum Signal Level [mV]: -37 dBv</strong></td>
<td>7.07946</td>
<td>5.95682</td>
<td>5.0148723</td>
<td>5.012</td>
<td>5.0125</td>
<td>5.0125</td>
<td>6.3995734</td>
<td>261.838</td>
<td>190.526</td>
<td>190.526</td>
</tr>
<tr>
<td><strong>Minimum Signal Level [mV]: -1.72 dBv</strong></td>
<td>0.12599</td>
<td>0.10593</td>
<td>0.0891251</td>
<td>1.259</td>
<td>2.2387</td>
<td>2.2387</td>
<td>1.5840932</td>
<td>501.187</td>
<td>354.813</td>
<td>354.813</td>
</tr>
<tr>
<td><strong>Minimum Signal Level for Interferer Tests1 [mV]: -49 dBv</strong></td>
<td>0.17783</td>
<td>0.14982</td>
<td>0.1258925</td>
<td>0.4126</td>
<td>0.3981</td>
<td>0.3981</td>
<td>0.2818383</td>
<td>0.89125</td>
<td>0.63096</td>
<td>0.63096</td>
</tr>
<tr>
<td><strong>Signal for Interferer Tests2 for adjacent channel [mV]: -34 dBm</strong></td>
<td>4.46604</td>
<td>7.40984</td>
<td>6.3995734</td>
<td>6.31</td>
<td>19.953</td>
<td>19.953</td>
<td>14.125375</td>
<td>44.6684</td>
<td>31.6228</td>
<td>31.6228</td>
</tr>
<tr>
<td><strong>Signal for Interferer Tests2 for alternate channel [mV]: -53 dBm</strong></td>
<td>0.90119</td>
<td>0.84111</td>
<td>0.7079458</td>
<td>0.708</td>
<td>2.2387</td>
<td>2.2387</td>
<td>1.5840932</td>
<td>1.58489</td>
<td>1.12202</td>
<td>1.12202</td>
</tr>
<tr>
<td><strong>adjacent Channel (Test1 with Pmax= -62 dBm) [mV]</strong></td>
<td>0.28184</td>
<td>0.23714</td>
<td>0.1995262</td>
<td>0.2</td>
<td>0.631</td>
<td>0.631</td>
<td>0.6308957</td>
<td>0.19953</td>
<td>0.01995</td>
<td>0.01995</td>
</tr>
<tr>
<td><strong>alternate Channel (Test1 with Pmax= -62 dBm) [mV]</strong></td>
<td>2.54109</td>
<td>2.41349</td>
<td>1.77872704</td>
<td>1.778</td>
<td>3.1623</td>
<td>3.1623</td>
<td>0.3162228</td>
<td>0.31622</td>
<td>0.00032</td>
<td>0.00032</td>
</tr>
<tr>
<td><strong>adjacent Channel (Test2 with P1r= -34 dBm) [mV]</strong></td>
<td>7.07946</td>
<td>5.95682</td>
<td>5.0148723</td>
<td>5.012</td>
<td>15.849</td>
<td>15.849</td>
<td>1.5840932</td>
<td>5.01187</td>
<td>0.50119</td>
<td>0.50119</td>
</tr>
<tr>
<td><strong>alternate Channel (Test2 with Pmax= -53 dBm) [mV]</strong></td>
<td>7.07946</td>
<td>5.95682</td>
<td>5.0148723</td>
<td>5.012</td>
<td>15.849</td>
<td>15.849</td>
<td>1.5840932</td>
<td>0.1584893</td>
<td>0.00158</td>
<td>0.00158</td>
</tr>
</tbody>
</table>

### Blockers

<table>
<thead>
<tr>
<th></th>
<th>Antenna</th>
<th>RF-Filter</th>
<th>R/T Switch</th>
<th>LNA</th>
<th>Mixer</th>
<th>VGA</th>
<th>Filter</th>
<th>VGA1</th>
<th>Filter</th>
<th>ADC</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>adjacent Channel (Test1 with Pmax= -62) [dBm]</strong></td>
<td>-58.9</td>
<td>-61</td>
<td>-61</td>
<td>-51</td>
<td>-51</td>
<td>-71</td>
<td>-61</td>
<td>-81</td>
<td>-81</td>
<td>-81</td>
</tr>
<tr>
<td><strong>alternate Channel (Test1 with Pmax= -62) [dBm]</strong></td>
<td>-40.5</td>
<td>-42</td>
<td>-42</td>
<td>-37</td>
<td>-37</td>
<td>-77</td>
<td>-77</td>
<td>-117</td>
<td>-117</td>
<td>-117</td>
</tr>
<tr>
<td><strong>adjacent Channel (Test2 with P1r= -34) [dBm]</strong></td>
<td>-30.5</td>
<td>-33</td>
<td>-33</td>
<td>-23</td>
<td>-23</td>
<td>-43</td>
<td>-43</td>
<td>-53</td>
<td>-53</td>
<td>-53</td>
</tr>
<tr>
<td><strong>alternate Channel (Test2 with Pmax= -53) [dBm]</strong></td>
<td>-30.5</td>
<td>-33</td>
<td>-33</td>
<td>-23</td>
<td>-23</td>
<td>-63</td>
<td>-63</td>
<td>-103</td>
<td>-103</td>
<td>-103</td>
</tr>
<tr>
<td><strong>11th First Out of Band Blocker [dBm]</strong></td>
<td>-23</td>
<td>-24.5</td>
<td>-64.5</td>
<td>-64.5</td>
<td>-54.5</td>
<td>-54.5</td>
<td>-94.5</td>
<td>-74.5</td>
<td>-114.5</td>
<td>-114.5</td>
</tr>
<tr>
<td><strong>11th Second Out of Band Blocker [dBm]</strong></td>
<td>-30</td>
<td>-11.5</td>
<td>-91.5</td>
<td>-91.5</td>
<td>-91.5</td>
<td>-161.5</td>
<td>-141.5</td>
<td>-221.5</td>
<td>-221.5</td>
<td>-221.5</td>
</tr>
</tbody>
</table>

Figure A.2 Signal and blocker strengths in the WiMAX/WLAN receiver chain.
<table>
<thead>
<tr>
<th>Block Input</th>
<th>Antenna</th>
<th>RF Filter</th>
<th>R/F Switch</th>
<th>LNA</th>
<th>Mixer</th>
<th>VGA</th>
<th>Filter</th>
<th>VGA1</th>
<th>Filter</th>
<th>ADC</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td>100</td>
<td>100</td>
<td>0.1</td>
<td>0.6</td>
<td>1</td>
<td>0.9</td>
<td>0.9</td>
<td>0.9</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>Each Block Contribution to total VIP3 (test1, adjacent)</td>
<td>0.0001</td>
<td>0.0001</td>
<td>5.01E-05</td>
<td>0</td>
<td>0.6977</td>
<td>0</td>
<td>3.1010944</td>
<td>1.55423</td>
<td>15.5423</td>
<td>0.70406</td>
</tr>
<tr>
<td>Each Block Contribution to total VIP3 (test1, alternate)</td>
<td>0.0001</td>
<td>0.0001</td>
<td>5.01E-05</td>
<td>0</td>
<td>0.6977</td>
<td>0</td>
<td>0.9806521</td>
<td>0.49149</td>
<td>0.02247</td>
<td></td>
</tr>
<tr>
<td>Each Block Contribution to total VIP3 (test2, adjacent)</td>
<td>0.0001</td>
<td>0.0001</td>
<td>5.01E-05</td>
<td>0</td>
<td>0.6977</td>
<td>0</td>
<td>3.1010944</td>
<td>1.55423</td>
<td>15.5423</td>
<td>0.70406</td>
</tr>
<tr>
<td>Each Block Contribution to total VIP3 (test2, alternate)</td>
<td>0.0001</td>
<td>0.0001</td>
<td>5.01E-05</td>
<td>0</td>
<td>0.6977</td>
<td>0</td>
<td>3.1010944</td>
<td>1.55423</td>
<td>0.70406</td>
<td></td>
</tr>
<tr>
<td>1.1b Inband Blocker [Vp2rms]</td>
<td>0.0001</td>
<td>0.0001</td>
<td>5.01E-05</td>
<td>0</td>
<td>0.6977</td>
<td>0</td>
<td>3.1010944</td>
<td>0.33101</td>
<td>0.00981</td>
<td>0.00279</td>
</tr>
<tr>
<td>1.1b First Out of Band Blocker [Vp2rms]</td>
<td>0.0001</td>
<td>0.0001</td>
<td>5.01E-05</td>
<td>0</td>
<td>0.0E-08</td>
<td>0</td>
<td>6.187E-08</td>
<td>6.3E-12</td>
<td>2E-12</td>
<td>5.6E-15</td>
</tr>
<tr>
<td>1.1b Second Out of Band Blocker [Vp2rms]</td>
<td>0.0001</td>
<td>0.0001</td>
<td>5.01E-05</td>
<td>0</td>
<td>0.0E-16</td>
<td>0</td>
<td>6.187E-16</td>
<td>6.3E-24</td>
<td>2E-12</td>
<td>5.6E-31</td>
</tr>
</tbody>
</table>

**Figure A.3 Requirements on linearity (IIP2, IIP3) for different blocks in WiMAX/WLAN receiver chain.**
Figure A.4 Phase noise of the PLL and its contribution to the total noise floor in WiMAX/WLAN receiver chain.
<table>
<thead>
<tr>
<th>Thermal Noise</th>
<th>Antenna</th>
<th>RF Filter</th>
<th>IF Switch</th>
<th>LNA</th>
<th>Mixer</th>
<th>VGA</th>
<th>Filter</th>
<th>VGA1</th>
<th>Filter</th>
<th>ADC</th>
</tr>
</thead>
<tbody>
<tr>
<td>KTR Noise</td>
<td>1.9E-04</td>
<td>1.8E-04</td>
<td>1.8E-04</td>
<td>6E-04</td>
<td>5E-04</td>
<td>1E-04</td>
<td>1E-04</td>
<td>1E-04</td>
<td>1E-04</td>
<td>1E-04</td>
</tr>
<tr>
<td>Block input referred noise V/m^2</td>
<td>4.55E-12</td>
<td>4.55E-12</td>
<td>4.55E-12</td>
<td>5E-08</td>
<td>1E-08</td>
<td>1E-08</td>
<td>1E-08</td>
<td>1E-08</td>
<td>1E-08</td>
<td>1E-08</td>
</tr>
<tr>
<td>NF (dB)</td>
<td>4.4E-01</td>
<td>4.4E-01</td>
<td>4.4E-01</td>
<td>0E-01</td>
<td>0E-01</td>
<td>0E-01</td>
<td>0E-01</td>
<td>0E-01</td>
<td>0E-01</td>
<td>0E-01</td>
</tr>
<tr>
<td>Block input referred noise over BW [V/m]</td>
<td>4.55E-12</td>
<td>4.55E-12</td>
<td>4.55E-12</td>
<td>5E-08</td>
<td>1E-08</td>
<td>1E-08</td>
<td>1E-08</td>
<td>1E-08</td>
<td>1E-08</td>
<td>1E-08</td>
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<tr>
<td>11b Block input referred noise over BW [V/m]</td>
<td>2.03E-06</td>
<td>2.03E-06</td>
<td>2.03E-06</td>
<td>6E-06</td>
<td>6E-06</td>
<td>6E-06</td>
<td>6E-06</td>
<td>6E-06</td>
<td>6E-06</td>
<td>6E-06</td>
</tr>
<tr>
<td>Cascaded output referred noise over BW [V/m]</td>
<td>2.03E-06</td>
<td>2.03E-06</td>
<td>2.03E-06</td>
<td>6E-06</td>
<td>6E-06</td>
<td>6E-06</td>
<td>6E-06</td>
<td>6E-06</td>
<td>6E-06</td>
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<tr>
<td>Cascaded output referred noise over BW [V/m]</td>
<td>2.03E-06</td>
<td>2.03E-06</td>
<td>2.03E-06</td>
<td>6E-06</td>
<td>6E-06</td>
<td>6E-06</td>
<td>6E-06</td>
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<table>
<thead>
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<th>Final CSR</th>
<th>Antenna</th>
<th>RF Filter</th>
<th>IF Switch</th>
<th>LNA</th>
<th>Mixer</th>
<th>VGA</th>
<th>Filter</th>
<th>VGA1</th>
<th>Filter</th>
<th>ADC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Carrier (MHz) for adjacent Ch hear1</td>
<td>30.398089</td>
<td>30.398089</td>
<td>30.398089</td>
<td>30.398089</td>
<td>30.398089</td>
<td>30.398089</td>
<td>30.398089</td>
<td>30.398089</td>
<td>30.398089</td>
<td>30.398089</td>
</tr>
<tr>
<td>Carrier (MHz) for alternate Ch hear1</td>
<td>43.009580</td>
<td>43.009580</td>
<td>43.009580</td>
<td>43.009580</td>
<td>43.009580</td>
<td>43.009580</td>
<td>43.009580</td>
<td>43.009580</td>
<td>43.009580</td>
<td>43.009580</td>
</tr>
<tr>
<td>Carrier (MHz) for adjacent Ch hear2</td>
<td>51.333333</td>
<td>51.333333</td>
<td>51.333333</td>
<td>51.333333</td>
<td>51.333333</td>
<td>51.333333</td>
<td>51.333333</td>
<td>51.333333</td>
<td>51.333333</td>
<td>51.333333</td>
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</table>

ADC Resolution & Dynamic Range
- ADC Dynamic Range (dB) | 55
- 11b ADC Dynamic Range (dB) | 35

ADC Resolution (bits)
- 9.25E+00
- 9.77E+00

Figure A.5 Thermal noise requirements, final carrier to noise and distortion ratio and dynamic range of data converter in WiMAX/WLAN receiver.
APPENDIX B

SYSTEM DESIGN EXCEL SHEETS FOR 3G/WLAN
<table>
<thead>
<tr>
<th>Gain</th>
<th>Antenna</th>
<th>RF Filter</th>
<th>R/T switch</th>
<th>LNA</th>
<th>Mixer</th>
<th>VGA</th>
<th>Filter</th>
<th>VGA</th>
<th>Filter</th>
<th>ADC</th>
</tr>
</thead>
<tbody>
<tr>
<td>GSM, Min. Gain for Interferer [dB]</td>
<td>0</td>
<td>-1.5</td>
<td>-1.5</td>
<td>5</td>
<td>10</td>
<td>0</td>
<td>.3</td>
<td>20</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>WCDMA, Min. Gain for Interferer [dB]</td>
<td>0</td>
<td>-1.5</td>
<td>-1.5</td>
<td>5</td>
<td>10</td>
<td>0</td>
<td>.3</td>
<td>20</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>11a, Min. Gain for Interferer [dB]</td>
<td>0</td>
<td>-1.5</td>
<td>-1.5</td>
<td>5</td>
<td>10</td>
<td>0</td>
<td>.3</td>
<td>20</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>11b, Min. Gain for Interferer [dB]</td>
<td>0</td>
<td>-1.5</td>
<td>-1.5</td>
<td>5</td>
<td>10</td>
<td>0</td>
<td>.3</td>
<td>20</td>
<td>0</td>
<td>0</td>
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<tr>
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<td>-1.5</td>
<td>-1.5</td>
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<td>10</td>
<td>0</td>
<td>.3</td>
<td>30</td>
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<td>0</td>
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<tr>
<td>WCDMA, Maximum Gain AV [dB]</td>
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<td>-1.5</td>
<td>-1.5</td>
<td>15</td>
<td>10</td>
<td>0</td>
<td>.3</td>
<td>50</td>
<td>0</td>
<td>0</td>
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<tr>
<td>WCDMA, Minimum Gain- AV [dB]</td>
<td>0</td>
<td>-1.5</td>
<td>-1.5</td>
<td>5</td>
<td>10</td>
<td>0</td>
<td>.3</td>
<td>16</td>
<td>0</td>
<td>0</td>
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<tr>
<td>11a, Maximum Gain AV [dB]</td>
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<td>-1.5</td>
<td>-1.5</td>
<td>15</td>
<td>10</td>
<td>0</td>
<td>.3</td>
<td>50</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>11b, Maximum Gain AV [dB]</td>
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<td>-1.5</td>
<td>-1.5</td>
<td>15</td>
<td>10</td>
<td>0</td>
<td>.3</td>
<td>50</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>11b, Minimum Gain AV [dB]</td>
<td>0</td>
<td>-1.5</td>
<td>-1.5</td>
<td>5</td>
<td>10</td>
<td>0</td>
<td>.3</td>
<td>16</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Figure B.1 Gain distributions in the 4G receiver chain.
### Table

#### Signal Levels in [dBm]

<table>
<thead>
<tr>
<th></th>
<th>Antenna</th>
<th>RF Filter</th>
<th>R/T switch</th>
<th>LNA</th>
<th>Mixer</th>
<th>VGA</th>
<th>Filter</th>
<th>VGA1</th>
<th>Filter</th>
<th>ADC</th>
</tr>
</thead>
<tbody>
<tr>
<td>GSM, Maximum Signal Level [dBm]</td>
<td>-28</td>
<td>-29.5</td>
<td>-31</td>
<td>-26</td>
<td>-16</td>
<td>-16</td>
<td>-14</td>
<td>11</td>
<td>11</td>
<td>11</td>
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<tr>
<td>GSM, Minimum Signal Level [dBm]</td>
<td>-117</td>
<td>-110.5</td>
<td>-120</td>
<td>-105</td>
<td>-95</td>
<td>-95</td>
<td>-98</td>
<td>30</td>
<td>38</td>
<td>38</td>
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<tr>
<td>WCDMA, Maximum Signal Level [dBm]</td>
<td>-38</td>
<td>-39.5</td>
<td>-41</td>
<td>-36</td>
<td>26</td>
<td>26</td>
<td>29</td>
<td>13</td>
<td>13</td>
<td>13</td>
</tr>
<tr>
<td>WCDMA, Minimum Signal Level [dBm]</td>
<td>-119</td>
<td>-120.5</td>
<td>-122</td>
<td>-107</td>
<td>-87</td>
<td>-87</td>
<td>-100</td>
<td>50</td>
<td>50</td>
<td>50</td>
</tr>
<tr>
<td>11a, Maximum Signal Level [dBm]</td>
<td>-33</td>
<td>-34.5</td>
<td>-36</td>
<td>-31</td>
<td>-21</td>
<td>-21</td>
<td>-24</td>
<td>-8</td>
<td>-8</td>
<td>-8</td>
</tr>
<tr>
<td>11a, Minimum Signal Level [dBm]</td>
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<td>-96.5</td>
<td>-98</td>
<td>-93</td>
<td>-73</td>
<td>-73</td>
<td>-76</td>
<td>-26</td>
<td>-26</td>
<td>-26</td>
</tr>
<tr>
<td>11b, Maximum Signal Level [dBm]</td>
<td>-23</td>
<td>-24.5</td>
<td>-26</td>
<td>-21</td>
<td>-11</td>
<td>-11</td>
<td>-14</td>
<td>-4</td>
<td>-4</td>
<td>-4</td>
</tr>
<tr>
<td>11b, Minimum Signal Level [dBm]</td>
<td>-89</td>
<td>-90.5</td>
<td>-92</td>
<td>-77</td>
<td>-67</td>
<td>-67</td>
<td>-70</td>
<td>-20</td>
<td>-20</td>
<td>-20</td>
</tr>
<tr>
<td>GSM, signal level for adjacent Channel Blocker [dBm]</td>
<td>-56</td>
<td>-57.5</td>
<td>-59</td>
<td>-54</td>
<td>-44</td>
<td>-44</td>
<td>-44</td>
<td>-4</td>
<td>-4</td>
<td>-4</td>
</tr>
<tr>
<td>WCDMA, signal level for Highest In-Band Blocker [dBm]</td>
<td>-57</td>
<td>-58.5</td>
<td>-60</td>
<td>-55</td>
<td>-45</td>
<td>-45</td>
<td>-45</td>
<td>-85</td>
<td>-85</td>
<td>-85</td>
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<tr>
<td>11a, signal level for Highest In-Band Blocker [dBm]</td>
<td>-52</td>
<td>-53.5</td>
<td>-55</td>
<td>-50</td>
<td>-40</td>
<td>-40</td>
<td>-40</td>
<td>-60</td>
<td>-60</td>
<td>-60</td>
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<tr>
<td>11b, signal level for adjacent Channel Blocker [dBm]</td>
<td>-48</td>
<td>-49.5</td>
<td>-51</td>
<td>-46</td>
<td>-36</td>
<td>-36</td>
<td>-36</td>
<td>-56</td>
<td>-56</td>
<td>-56</td>
</tr>
<tr>
<td>11b, signal level for Highest In-Band Blocker [dBm]</td>
<td>-48</td>
<td>-49.5</td>
<td>-51</td>
<td>-46</td>
<td>-36</td>
<td>-36</td>
<td>-36</td>
<td>-56</td>
<td>-56</td>
<td>-56</td>
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</tbody>
</table>

### Table

#### Signal Levels in [mW]

<table>
<thead>
<tr>
<th></th>
<th>Antenna</th>
<th>RF Filter</th>
<th>R/T switch</th>
<th>LNA</th>
<th>Mixer</th>
<th>VGA</th>
<th>Filter</th>
<th>VGA1</th>
<th>Filter</th>
<th>ADC</th>
</tr>
</thead>
<tbody>
<tr>
<td>GSM, Maximum Signal Level [mW]</td>
<td>0.112602</td>
<td>0.094743</td>
<td>0.0797459</td>
<td>0.1418</td>
<td>0.44828</td>
<td>0.44828</td>
<td>0.31735</td>
<td>10.036</td>
<td>10.0356</td>
<td>10.0356</td>
</tr>
<tr>
<td>GSM, Minimum Signal Level [mW]</td>
<td>4E 06</td>
<td>3.36E 06</td>
<td>2.92E 06</td>
<td>2E 05</td>
<td>5E 05</td>
<td>5E 05</td>
<td>3.6E 05</td>
<td>0.0356</td>
<td>0.03561</td>
<td>0.03561</td>
</tr>
<tr>
<td>GSM, signal level for adjacent Channel Blocker [mW]</td>
<td>0.004483</td>
<td>0.003772</td>
<td>0.001735</td>
<td>0.0056</td>
<td>0.01785</td>
<td>0.01785</td>
<td>0.001785</td>
<td>0.01785</td>
<td>0.01785</td>
<td>0.01785</td>
</tr>
<tr>
<td>GSM, signal level for Highest In-Band Blocker [mW]</td>
<td>0.03735</td>
<td>0.026702</td>
<td>0.022467</td>
<td>0.04</td>
<td>0.12634</td>
<td>0.12634</td>
<td>0.00126</td>
<td>0.01263</td>
<td>0.01263</td>
<td>0.01263</td>
</tr>
<tr>
<td>GSM, Cascaded output referred to reference Channel Blocker [mW]</td>
<td>0.035608</td>
<td>0.02996</td>
<td>0.0252084</td>
<td>0.01418</td>
<td>0.14176</td>
<td>0.14176</td>
<td>0.10063</td>
<td>0.63321</td>
<td>0.63321</td>
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<tr>
<td>GSM, Minimum Signal Level [mW]</td>
<td>3.17E 06</td>
<td>2.07E 06</td>
<td>2.24E 06</td>
<td>1E 05</td>
<td>4E 05</td>
<td>4E 05</td>
<td>2.8E 05</td>
<td>0.0089</td>
<td>0.00894</td>
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<td>WCDMA, Maximum Signal Level [mW]</td>
<td>0.004591</td>
<td>0.001338</td>
<td>0.001126</td>
<td>0.002</td>
<td>0.00633</td>
<td>0.00633</td>
<td>0.00633</td>
<td>0.00633</td>
<td>0.00633</td>
<td>0.00633</td>
</tr>
<tr>
<td>WCDMA, signal level for adjacent Channel Blocker [mW]</td>
<td>0.003995</td>
<td>0.003362</td>
<td>0.0022804</td>
<td>0.005</td>
<td>0.01591</td>
<td>0.01591</td>
<td>0.00016</td>
<td>0.0016</td>
<td>0.00159</td>
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</tr>
</tbody>
</table>

Figure B.2 Signal and blocker levels in 4G receiver.
Figure B.3 Blocker levels, and linearity requirements of different blocks in 4G receiver.

<table>
<thead>
<tr>
<th>Blockers</th>
<th>Antenna</th>
<th>RF Filter</th>
<th>R/T switch</th>
<th>LNA</th>
<th>Mloor</th>
<th>VGA</th>
<th>Filter</th>
<th>VGA1</th>
<th>Filter</th>
<th>ADC</th>
</tr>
</thead>
<tbody>
<tr>
<td>GSM, adjacent Channel Blocker [dBm]</td>
<td>-41</td>
<td>-44.5</td>
<td>-46</td>
<td>-41</td>
<td>-31</td>
<td>-51</td>
<td>-31</td>
<td>-31</td>
<td>-31</td>
<td></td>
</tr>
<tr>
<td>GSM, Highest In-Band Blocker [dBm]</td>
<td>-36</td>
<td>-27.5</td>
<td>-29</td>
<td>-24</td>
<td>-14</td>
<td>-14</td>
<td>-54</td>
<td>-34</td>
<td>-34</td>
<td>-34</td>
</tr>
<tr>
<td>WCDMA, Highest In-Band Blocker [dBm]</td>
<td>-44</td>
<td>-45.5</td>
<td>-47</td>
<td>-42</td>
<td>-32</td>
<td>-32</td>
<td>-72</td>
<td>-52</td>
<td>-52</td>
<td>-52</td>
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<tr>
<td>11b, adjacent Channel Blocker [dBm]</td>
<td>-35</td>
<td>-36.5</td>
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<td>-23</td>
<td>-43</td>
<td>-23</td>
<td>-23</td>
<td>-23</td>
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<tr>
<td>11b, Highest In-Band Blocker [dBm]</td>
<td>-35</td>
<td>-36.5</td>
<td>-38</td>
<td>-33</td>
<td>-23</td>
<td>-23</td>
<td>-43</td>
<td>-23</td>
<td>-23</td>
<td>-23</td>
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<table>
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<th>VIP3</th>
<th>Antenna</th>
<th>RF Filter</th>
<th>R/T switch</th>
<th>LNA</th>
<th>Mloor</th>
<th>VGA</th>
<th>Filter</th>
<th>VGA1</th>
<th>Filter</th>
<th>ADC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Block Input Referred Ip3 [Vrms]</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>6.4</td>
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<td>1</td>
<td>0.9</td>
<td>0.9</td>
<td>0.9</td>
<td>3</td>
</tr>
<tr>
<td>GSM, Each Block Contribution to total VIP3</td>
<td>0.0001</td>
<td>0.0001</td>
<td>5.012E-05</td>
<td>156.99</td>
<td>2.20647</td>
<td>0</td>
<td>9.88652</td>
<td>4.91149</td>
<td>0.00</td>
<td>44231</td>
</tr>
<tr>
<td>WCDMA, Each Block Contribution to total VIP3</td>
<td>0.0001</td>
<td>0.0001</td>
<td>5.012E-05</td>
<td>156.99</td>
<td>2.20647</td>
<td>0</td>
<td>9.88652</td>
<td>4.91149</td>
<td>0.00</td>
<td>44231</td>
</tr>
<tr>
<td>11a, Each Block Contribution to total VIP3</td>
<td>0.0001</td>
<td>0.0001</td>
<td>5.012E-05</td>
<td>156.99</td>
<td>2.20647</td>
<td>0</td>
<td>9.88652</td>
<td>4.91149</td>
<td>0.00</td>
<td>44231</td>
</tr>
<tr>
<td>11b, Each Block Contribution to total VIP3</td>
<td>0.0001</td>
<td>0.0001</td>
<td>5.012E-05</td>
<td>156.99</td>
<td>2.20647</td>
<td>0</td>
<td>9.88652</td>
<td>4.91149</td>
<td>0.00</td>
<td>44231</td>
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</table>

<table>
<thead>
<tr>
<th>VIP2</th>
<th>Antenna</th>
<th>RF Filter</th>
<th>R/T switch</th>
<th>LNA</th>
<th>Mloor</th>
<th>VGA</th>
<th>Filter</th>
<th>VGA1</th>
<th>Filter</th>
<th>ADC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input referred Vip2 (per block)[mW]</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>6.6</td>
<td>6</td>
<td>70</td>
<td>40</td>
<td>40</td>
<td>40</td>
<td>50</td>
</tr>
<tr>
<td>GSM, Each Block Contribution to total VIP2</td>
<td>0.01</td>
<td>0.01</td>
<td>0.0070795</td>
<td>0.3353</td>
<td>0.14854</td>
<td>0</td>
<td>0.07046</td>
<td>0.0499</td>
<td>0</td>
<td>0.39985</td>
</tr>
<tr>
<td>WCDMA, Each Block Contribution to total VIP2</td>
<td>0.01</td>
<td>0.01</td>
<td>0.0070795</td>
<td>0.3353</td>
<td>0.14854</td>
<td>0</td>
<td>0.07046</td>
<td>0.0499</td>
<td>0</td>
<td>0.39985</td>
</tr>
<tr>
<td>11a, Each Block Contribution to total VIP2</td>
<td>0.01</td>
<td>0.01</td>
<td>0.0070795</td>
<td>0.3353</td>
<td>0.14854</td>
<td>0</td>
<td>0.07046</td>
<td>0.0499</td>
<td>0</td>
<td>0.39985</td>
</tr>
<tr>
<td>11b, Each Block Contribution to total VIP2</td>
<td>0.01</td>
<td>0.01</td>
<td>0.0070795</td>
<td>0.3353</td>
<td>0.14854</td>
<td>0</td>
<td>0.07046</td>
<td>0.0499</td>
<td>0</td>
<td>0.39985</td>
</tr>
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</table>
### Figure B.4 Signal bandwidths, LO phase noise requirement in 4G receiver.

<table>
<thead>
<tr>
<th></th>
<th>GSM, Bandwidth</th>
<th>WCDMA, Bandwidth</th>
<th>11a, Bandwidth</th>
<th>11b, Bandwidth</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>200000</td>
<td>200000</td>
<td>200000</td>
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</tr>
<tr>
<td></td>
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<td>200000</td>
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</table>

<table>
<thead>
<tr>
<th>Reciprocal Mixing</th>
<th>Antenna</th>
<th>RF Filter</th>
<th>R/F switch</th>
<th>LNA</th>
<th>Mixer</th>
<th>VGA</th>
<th>Filter</th>
<th>VGA1</th>
<th>Filter</th>
<th>ADC</th>
</tr>
</thead>
<tbody>
<tr>
<td>LO Phase Noise (1 MHz) [dBc/Hz]</td>
<td>-100</td>
<td>-105,563</td>
<td>-109,548</td>
<td>-113,908</td>
<td>-123,529</td>
<td>-127,960</td>
<td>-133,908</td>
<td>-127,960</td>
<td></td>
<td></td>
</tr>
<tr>
<td>GSM, LO Phase Noise (blocker: 43 dBm @ 600 MHz) [dBc/Hz]</td>
<td>-100</td>
<td>-105,563</td>
<td>-109,548</td>
<td>-113,908</td>
<td>-123,529</td>
<td>-127,960</td>
<td>-133,908</td>
<td>-127,960</td>
<td></td>
<td></td>
</tr>
<tr>
<td>WCDMA, LO Phase Noise (blocker: -26 dBm @ 3 MHz) [dBc/Hz]</td>
<td>-105,563</td>
<td>-109,548</td>
<td>-113,908</td>
<td>-123,529</td>
<td>-127,960</td>
<td>-133,908</td>
<td>-127,960</td>
<td>-133,908</td>
<td></td>
<td></td>
</tr>
<tr>
<td>11a, LO Phase Noise (blocker: 52 dBm @ 5 MHz) [dBc/Hz]</td>
<td>-123,529</td>
<td>-127,960</td>
<td>-133,908</td>
<td>-127,960</td>
<td>-133,908</td>
<td>-127,960</td>
<td>-133,908</td>
<td>-127,960</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>GSM, V_{ref} from blocker: 43 dBm (V^2/2ms)</th>
<th>2.2E-11</th>
<th>2.2E-11</th>
<th>2.2E-11</th>
<th>2.2E-11</th>
<th>2.2E-11</th>
<th>2.2E-11</th>
<th>2.2E-11</th>
<th>2.2E-11</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>GSM, V_{ref} from blocker: 26 dBm (V^2/2ms)</td>
<td>4.4E-09</td>
<td>4.4E-09</td>
<td>4.4E-09</td>
<td>4.4E-09</td>
<td>4.4E-09</td>
<td>4.4E-09</td>
<td>4.4E-09</td>
<td>4.4E-09</td>
</tr>
<tr>
<td>WCDMA, V_{ref} from blocker: 52 dBm (V^2/2ms)</td>
<td>2E-10</td>
<td>2E-10</td>
<td>2E-10</td>
<td>2E-10</td>
<td>2E-10</td>
<td>2E-10</td>
<td>2E-10</td>
<td>2E-10</td>
<td></td>
</tr>
<tr>
<td>WCDMA, V_{ref} from blocker: -44 dBm (V^2/2ms)</td>
<td>2E-11</td>
<td>2E-11</td>
<td>2E-11</td>
<td>2E-11</td>
<td>2E-11</td>
<td>2E-11</td>
<td>2E-11</td>
<td>2E-11</td>
<td></td>
</tr>
<tr>
<td>11a, V_{ref} from blocker: 58 dBm (V^2/2ms)</td>
<td>4E-12</td>
<td>4E-12</td>
<td>4E-12</td>
<td>4E-12</td>
<td>4E-12</td>
<td>4E-12</td>
<td>4E-12</td>
<td>4E-12</td>
<td></td>
</tr>
<tr>
<td>11b, V_{ref} from blocker: -39 dBm (V^2/2ms)</td>
<td>8E-11</td>
<td>8E-11</td>
<td>8E-11</td>
<td>8E-11</td>
<td>8E-11</td>
<td>8E-11</td>
<td>8E-11</td>
<td>8E-11</td>
<td></td>
</tr>
<tr>
<td>11b, V_{ref} from blocker: -35 dBm (V^2/2ms)</td>
<td>9.8E-12</td>
<td>9.8E-12</td>
<td>9.8E-12</td>
<td>9.8E-12</td>
<td>9.8E-12</td>
<td>9.8E-12</td>
<td>9.8E-12</td>
<td>9.8E-12</td>
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</table>
Figure B.5 Residual FM derivation for 4G receiver.
<table>
<thead>
<tr>
<th>Thermal Noise</th>
<th>Antenna</th>
<th>RF Filter</th>
<th>IF switch</th>
<th>LNA</th>
<th>Mixer</th>
<th>VGA</th>
<th>Filter</th>
<th>VGA1</th>
<th>Filter</th>
<th>ADC</th>
</tr>
</thead>
<tbody>
<tr>
<td>VTR Noise</td>
<td>2.6E-12</td>
<td>2.6E-12</td>
<td>2.6E-12</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Block input referred noise Vsqrt(Hz)</td>
<td>4.5E-10</td>
<td>4.5E-10</td>
<td>4.5E-10</td>
<td>6.0E-08</td>
<td>7.0E-08</td>
<td>7.0E-08</td>
<td>3.0E-08</td>
<td>4.5E-08</td>
<td>1.0E+00</td>
<td></td>
</tr>
<tr>
<td>Req</td>
<td>3.0E+01</td>
<td>2.4E+07</td>
<td>6.1E+03</td>
<td>2.4E+04</td>
<td>5.4E+04</td>
<td>1.2E+05</td>
<td>6.4E+07</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NF (dB)</td>
<td>6.1E+00</td>
<td>1.3E+01</td>
<td>2.6E+01</td>
<td>3.2E+01</td>
<td>3.6E+01</td>
<td>3.0E+01</td>
<td>6.6E+01</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GSM, Block input referred noise over Bandwidth [Vrms]</td>
<td>4.9E-14</td>
<td>4.9E-14</td>
<td>4.9E-14</td>
<td>1.9E-13</td>
<td>9.8E-13</td>
<td>8.0E-11</td>
<td>1.8E+10</td>
<td>4.9E+10</td>
<td>2.9E+07</td>
<td></td>
</tr>
<tr>
<td>WCDMA, Block input referred noise over Bandwidth [Vrms]</td>
<td>1.0E+12</td>
<td>1.0E+12</td>
<td>1.0E+12</td>
<td>3.2E+12</td>
<td>2.1E+10</td>
<td>5.8E+09</td>
<td>2.0E+09</td>
<td>4.5E+09</td>
<td>1.6E+09</td>
<td>9.6E+05</td>
</tr>
<tr>
<td>11a, Block input referred noise over Bandwidth [Vrms]</td>
<td>4.5E-12</td>
<td>4.5E-12</td>
<td>4.5E-12</td>
<td>1.2E-11</td>
<td>6.8E-11</td>
<td>1.4E-09</td>
<td>4.6E-09</td>
<td>9.6E-09</td>
<td>2.6E+00</td>
<td>6.6E+04</td>
</tr>
<tr>
<td>11b, Block input referred noise over Bandwidth [Vrms]</td>
<td>4.5E-12</td>
<td>4.5E-12</td>
<td>4.5E-12</td>
<td>1.2E-11</td>
<td>6.8E-11</td>
<td>1.4E-09</td>
<td>4.6E-09</td>
<td>9.6E-09</td>
<td>2.6E+00</td>
<td>6.6E+04</td>
</tr>
<tr>
<td>GSM, Cascaded output referred noise over Bandwidth [Vrms]</td>
<td>2.5E-07</td>
<td>2.5E-07</td>
<td>2.5E-07</td>
<td>1.2E-06</td>
<td>1.2E-06</td>
<td>9.8E-06</td>
<td>1.4E+04</td>
<td>1.4E+04</td>
<td>1.4E+04</td>
<td>1.4E+04</td>
</tr>
<tr>
<td>WCDMA, Cascaded output referred noise over Bandwidth [Vrms]</td>
<td>1.0E+06</td>
<td>1.0E+06</td>
<td>1.0E+06</td>
<td>2.0E+06</td>
<td>2.0E+06</td>
<td>3.9E+05</td>
<td>7.0E+05</td>
<td>7.0E+05</td>
<td>7.0E+05</td>
<td>7.0E+05</td>
</tr>
<tr>
<td>11a, Cascaded output referred noise over Bandwidth [Vrms]</td>
<td>2.5E-06</td>
<td>2.5E-06</td>
<td>2.5E-06</td>
<td>1.2E-06</td>
<td>1.2E-06</td>
<td>9.8E-06</td>
<td>1.4E+04</td>
<td>1.4E+04</td>
<td>1.4E+04</td>
<td>1.4E+04</td>
</tr>
<tr>
<td>11b, Cascaded output referred noise over Bandwidth [Vrms]</td>
<td>2.5E-06</td>
<td>2.5E-06</td>
<td>2.5E-06</td>
<td>1.2E-06</td>
<td>1.2E-06</td>
<td>9.8E-06</td>
<td>1.4E+04</td>
<td>1.4E+04</td>
<td>1.4E+04</td>
<td>1.4E+04</td>
</tr>
<tr>
<td>Noise Floor (dB)</td>
<td>-133.8</td>
<td>-133.8</td>
<td>-133.8</td>
<td>-128.9</td>
<td>-128.9</td>
<td>-106.0</td>
<td>-105.9</td>
<td>97.147</td>
<td>93.923</td>
<td>66.09</td>
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</tbody>
</table>

Figure B.6 Thermal noise calculations in 4G receiver.
<table>
<thead>
<tr>
<th>Final CDR</th>
<th>Antenna</th>
<th>RF Filter</th>
<th>R/T switch</th>
<th>LNA</th>
<th>Mixer</th>
<th>VgA</th>
<th>Filter</th>
<th>VgA1</th>
<th>Filter</th>
<th>ADC</th>
</tr>
</thead>
<tbody>
<tr>
<td>GSM, Carrier (N+D)</td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>19.7420712</td>
</tr>
<tr>
<td>WCDMA, Carrier (N+D)</td>
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<td></td>
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<td>32.7472184</td>
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<tr>
<td>11a, Carrier (N+D)</td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>50.8808221</td>
</tr>
<tr>
<td>11b, Carrier (N+D)</td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>-41.8392587</td>
</tr>
</tbody>
</table>

**ADC Resolution & Dynamic Range**

| GSM, ADC Dynamic Range [dB] | 70 |
| WCDMA, ADC Dynamic Range [dB] | 52 |
| 11a, ADC Dynamic Range [dB]  | 62 |
| 11b, ADC Dynamic Range [dB]  | 52 |
| GSM, ADC Resolution [bits]  | 9.33E+00 |
| WCDMA, ADC Resolution [bits] | 7.01E+00 |
| 11a ADC Resolution [bits]   | 6.51E+00 |
| 11b ADC Resolution [bits]   | 6.44E+00 |

Figure B.7 Carrier to noise and distortion ratio and ADC requirements in 4G receiver.