STUDIES ON FIELD EFFECT TRANSISTORS WITH CONJUGATED POLYMER AND HIGH PERMITTIVITY GATE DIELECTRICS USING PULSED PLASMA POLYMERIZATION

DISsertation

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* * * * *

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ABSTRACT

The aim of this Ph.D. project is to explore the operating mechanism of polymer field effect transistors (PFETs) to improve their performance. Polymer semiconductors are composed of π-conjugated polymers and have the advantage of easy processing. Their solution processibility at room temperature makes them an attractive candidate for light-weight, large-area, flexible electronics. However, the performance of PFETs is currently limited by low carrier mobility and high driving voltages. This dissertation presents thin film insulators as new gate dielectric materials to relax the requirement for driving voltages and illustrates some unique features of field dependent mobility in PFETs. Light responsive PFETs based on new polymer semiconductors are also demonstrated as a potential application of PFETs.

Pulsed plasma deposited polymer insulating films were investigated for their potential application as the gate dielectric in PFETs. The work on pulsed plasma polymerized (PPP) thin film insulators put emphasis on improving the dielectric constant of the thin polymer films. The driving voltage of a PFET can be reduced by using gate insulators with a high dielectric constants. Early work on PPP allylamine films indicated that the chamber temperature during pulsed plasma polymerization has an effect on the dielectric constant. PPP allylamine films were employed as the insulating layers and tested as metal-insulator-semiconductor (MIS) capacitors. The insulating polymer films
were deposited at plasma reactor temperatures of 25°C and 100°C. Multiple frequency capacitance-voltage (C-V) measurements indicated that an *in-situ* heat treatment during film deposition increased the insulator dielectric constant. The dielectric constant, calculated from the C-V data, rose from 3.03 for samples with no heat treatment to 3.55 for samples with an *in-situ* heat treatment. For both sample sets, the I-V data demonstrates a low leakage current value (<0.65 pA/mm²) up to 100V.

Later work on PPP insulators took advantage of engineering ability of the dielectric constant of the polymer film by the judicious selection of a monomer possessing a high polarizability. Polymerized dichlorotetramethylidisiloxane (DCTMDS) films deposited by radio frequency pulsed plasma polymerization (PPP) demonstrated very high dielectric constants for an organic-based system, in the range of 7 to 10. The high dielectric constants of PPP DCTMDS films are due to the high polarizability of the DCTMDS monomer. The pulsed plasma duty cycle (ON/OFF) was varied resulting in slightly higher dielectric constant DCTMDS films for higher duty cycles. The variation of dielectric constants does not show any trend with varying film thicknesses, indicating that the thickness of the deposited films is not significant for controlling permittivity. Post-deposition annealing over a certain temperature range improves the electrical integrity of PPP DCTMDS films, but temperatures that are too high induce an even higher leakage than the samples with no heat treatment. An optimal annealing temperature was identified to be in the range of 150 ℃ to 200 ℃. Samples annealed within this temperature window have low leakage current densities below 0.1 pA/μm² at 10 V for film thicknesses about 100 nm. Poly(3-hexythiophene) (P3HT) polymer field effect transistors (PFETs) using PPP DCTMDS gate dielectric films were fabricated and
tested. Due to the high dielectric constants of PPP DCTMDS, these PFETs possess high gate capacitance and operate at low voltage.

The field dependent mobility was demonstrated in polythiophene (PT) FETs by varying the gate length. The field effect mobility in polythiophene polymer field effect transistors (PFETs) increases with reduced channel lengths for high driving forces across the source and drain, which is contradictory to the decrease in mobility caused by short channel effects in amorphous Si thin film transistors (TFTs). The longitudinal electric field (across source and drain) dependence of the field effect mobility is believed to create the rise in mobility once the longitudinal electric field exceeds a critical value of $10^5$ V/cm. The high longitudinal electric field also modulates the influence of the gate bias upon the field effect mobility in PT PFETs. With increased longitudinal electric field, the correlation between field effect mobility and gate bias is largely enhanced.

The photoresponse of polymer field effect transistors (PFET) based on the 2,5-bis(dibutylaminostyryl)-1,4-phenylene-b-alkyne-b-1,4-bis(2-ethylhexyl)benzene terpolymer (BAS-PPE) was also investigated. BAS-PPE is a photoluminescent conducting polymer with a bandgap of 2.25 eV. The BAS-PPE PFETs were fabricated using an open coplanar configuration and light is illuminated onto the top side of the PFETs with no shadowing present. A sweep of $V_{DS}$ demonstrates that $I_{DS}$ saturation is suppressed during illumination, which suggests that pinch-off can not be reached since the injected photo-generated carriers continue unabated. Also, with incident light, the channel can not be turned off, even at high positive gate biases, due to the accumulation of photo-generated carriers. A sweep of $V_{DS}$ shows that BAS-PPE can act as a p-type polymer and favors hole injection and transport. A sweep of $V_{GS}$ shows an increase in $I_{DS}$
with different light intensities. The $I_{\text{light}}/I_{\text{dark}}$ ratio reaches as high as about 6000 at an incident light intensity of 0.8 mW/mm$^2$ and a photoresponsivity of 5 mA/W is calculated.

Overall, this dissertation studied features of PFETs and suggested techniques to improve their performance, which hopefully will contribute to future progress of polymer electronics.
This is dedicated to my late father
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LIST OF ACRONYMS

FET – field effect transistor
MOSFET – metal oxide semiconductor field effect transistor
MISFET – metal insulator semiconductor field effect transistor
PFET – polymer field effect transistor
TFT – thin film transistor
HOMO – highest occupied molecular orbital
LUMO – lowest unoccupied molecular orbital
6T – sexithiophene
PT – polythiophene
P3HT – poly(3-hexylthiophene)
PPP – pulsed plasma polymerization
PA – polymerized allylamine
DCTMDS – dichlorotetramethyldisilane
PPE – polyphenyleneethynylene
PPV – polyphenylenevinylene
BASPPE – 2,5-bis(dibutylaminostyryl)-1,4-phenylene-b-alkyne-b-1,4-bis(2-ethylhexyl)benzene
CHAPTER 1

INTRODUCTION

The aim of this Ph.D. dissertation is the technological development of polymer field effect transistors (PFET), or also sometimes called polymer thin film transistors (PTFT). In PFETs, the active channel materials are composed of conjugated polymer semiconductors. In the distant past, polymers were only considered to be insulating, but this all changed since the discovery of conductive halogen treated polyacetylene in 1977 [1]. Later, in 1990 electroluminescence from poly(p-phenylene vinylene) was reported [2], which generated a tremendous level of interest to harness these materials for electronic and optoelectronic devices.

Conjugated polymers can be conductive and semiconductive due to the presence of alternately single and double bonds between the carbon atoms, namely conjugated double bonds, in their backbone. Every double bond contains a strong $\sigma$ bond and a weaker $\pi$ bond. If a polymer contains only $\sigma$ bonds, it will be an insulator because of the large bandgap between the highest occupied molecular orbital (HOMO) and the lowest un-occupied molecular orbital (LUMO). HOMO and LUMO are analogous to the valence band edge and conduction band edge, respectively, in inorganic semiconductors. Polymers containing conjugated $\pi$ bonds have a lower bandgap and can act as
semiconductors. Doping creates ions and cations in the conjugated polymer and improves its conductivity [1]. Conductive polymers are useful as electromagnetic shielding or antistatic coatings, while high purity polymer semiconductors are under intensive study as polymer light emitting diodes (PLEDs) [2-27] and polymer field effect transistors (PFET).

Despite their low mobility, PFETs are still studied extensively as a potential for electronics with reduced cost due to the simplicity of solution processed films. The fabrication costs for polymer electronic circuits can be greatly reduced from standard silicon device processing by fabricating devices from solution at low temperature. Also, their compatibility with flexible substrates provides the potential for new applications. In addition to their technological interest, PFETs are also one of the most reliable means to study charge transport in polymer semiconductors. The main body of this Ph.D. dissertation is to explore the working mechanism of PFETs and develop pulsed plasma polymerized high dielectric constant thin film insulators for applications as the gate dielectric material in PFETs. Efforts were also used to develop a polyphenyleneethynylene derivative based PFETs for light detection application.

The remainder of this dissertation is organized as follows:

Chapter 2 will briefly introduce the basics of polymer semiconductors and Si MOSFET device physics. The theory of various aspects of organic FET operation, including mobility in PFETs, new gate dielectric materials for OFETs operating at low voltages, and potential applications of PFETs will be described. This chapter will also summarize the current status of PFET performance.
Next, Chapter 3 will present studies of pulsed plasma polymerized thin dielectric films. PPP dielectric thin films with high dielectric constants were pursued as the gate dielectric in PFETs to ease the requirement for a high voltage power supply for PFET operation. Chapter 4 will present studies of short channel PFETs with channel lengths varying from 7 µm down to 1 µm. The mobility in short channel devices is demonstrated to increase once the longitudinal electric field exceeds a critical value of $10^5$ V/cm. In chapter 5, PFETs suitable as light detectors are presented. The output current of these light sensitive PFETs increased 3-fold with incident visible light.

Chapter 6 summarizes the conclusions of the experimental findings, and provides suggestions for future research.
CHAPTER 2

POLYMER FIELD EFFECT TRANSISTORS

This chapter provides an introduction to PFET device physics and topology. To assist in the understanding of PFETs, publications on oligomer and macromolecule based FETs are also referenced. FETs based on oligomers or macromolecules are classified as other types of organic FETs (OFETs) slightly distinct from PFETs. These three categories of organic FETs are different on many levels, but all three organic semiconductors share in common a π-conjugated systems. Some properties discovered in FETs based on oligomers and macromolecules also apply to PFETs. Where applicable, publications on FETs based on oligomers and macromolecules will be used to illustrate phenomenon in PFETs.

Before diving into the details of studies on PFETs, the basics of carrier transport and the conduction mechanism in polymer semiconductors will be discussed. The basic operation of traditional Si MOSFETs will also be presented as a reference to assist in the understanding of basic PFET operation later.
2.1 Basics of conjugated polymers as semiconductors [28, 29]

2.1.1 Formation of energy bands in polymer semiconductors

The concept of orbitals is essential to the understanding of bonding in molecules. The orbitals in an atom can be obtained by solving Schrödinger’s equation, and molecular orbitals can also be acquired by solving the Schrödinger equation for an interacting system. It was found that the composite two-electron wave functions are approximately linear combinations of the individual atomic orbitals (Fig. 2.1). The possible combinations of the atomic orbitals $\chi_A$ and $\chi_B$ on an two-atom molecule are:

$$\psi_1 = \chi_A + \chi_B$$

and

$$\psi_2 = \chi_A - \chi_B$$

Figure 2.1 Linear combinations of atomic orbitals (LCAO): when 2 atoms are brought together leads to 2 distinct “normal” modes – a higher energy anti-bonding orbital, and a lower energy bonding orbital (Adopted from Ref. [28]).
The electron density in these orbitals is the square of the wave function and must be the same by symmetry for each atom. The electron probability density is high in the region between the ion cores for $\psi_1$, leading to a lowering of the bonding energy level (Fig. 2.2). $\psi_2$ is the antibonding orbital having an energy higher than that of the isolated atoms. The anti-bonding states are less localized and can therefore contribute to carrier conduction as long as there are electrons in those states. If $N$ atoms are brought together, there will be $N$ distinct LCAO, and $N$ closely-spaced energy levels in a band.

Figure 2.2 Electron distributions and energies of molecular orbitals in $H_2$ (Adopted from Ref.[29]).
The type of interatomic bond, such as covalent, ionic, mixed, etc., determines how far the binding and anti-binding levels are separated in energies. A regular covalent bond, typically known as a $\sigma$ bond (Fig. 2.3 (a)), will have a huge separation in energy levels between binding and anti-binding states. Hence very few electrons will gain enough energy to reach the anti-binding levels, which explains why most organic molecules are insulators. With the addition of a $\pi$ bond (Fig. 2.3 (b)) to the $\sigma$ bond, a much weaker double bond is formed. Molecules containing double bonds (Fig. 2.3 (c)) have much closer binding and anti-binding energies than ones containing only $\sigma$ bonds.

![Figure 2.3 Illustration of the formation (a) a $\sigma$ bond, (b) a $\pi$ bond, and (c) a double bond.](image)
Conjugated polymers contain alternating single and double bond, and the number of successive bonds in a row in an alternating pattern of single and double bonds is called the “conjugation length”. By bringing together more and more atoms into one molecule, the energy levels will split, but they will stay closer in energy. A chain of more and more
atoms will render more levels by splitting further into bonding and anti-bonding levels. Besides more available energy levels, the levels also pack closer together. Supposing that the number of successive atoms in the chain approaches infinity, the energy levels will eventually overlap and a band structure will be created with a forbidden energy gap between the HOMO and LUMO levels (Fig. 2.4). As mentioned before, if the molecule contains only $\sigma$ bonds, the bandgap will be large, in the range of 6 to 8 eV. Since conjugated molecules contain $\pi$ bonds, their bandgaps are much narrower and encompass the visible light energies.

![Figure 2.4 Orbital energies of (a) atom, (b) small molecule, (c) large molecule, and (d) polymer (Adopted from Ref. [29]).](image)

The most common organic semiconductors include oligomers and polymers. They are both composed of repeated monomer units. The repetition number determines if the molecule is an oligomer or a polymer, but the line drawn between an oligomer and a polymer is not well defined. Very often a molecule with more than 15 repetition units is
considered a polymer, but it is not uncommon to see that 10 repetition units are used as the boundary between oligomers and polymers. One important difference between an oligomer and a polymer resides with polymers that are assumed to have a full band structure because the states in polymers are closely packed, whereas oligomers still have distinct energy levels. It also has to be pointed out that in polymers, the energy levels are actually separated by small amount of energies, but these are blurred at room temperature.

2.1.2 Charge formation and transport in polymer semiconductors

It was observed that carrier mobility in metals and inorganic semiconductors decreases at higher temperatures, while the mobility in polymer semiconductors has an opposite behavior. The difference in their behavior is rooted from the fundamentally different mechanisms of charge transport in the two material systems. Charge transport in metals and inorganic semiconductors is limited by the scattering of the carriers by lattice vibrations, or phonons. Therefore, at increased temperature the charge transport is impeded further due to the higher density of phonons at higher temperatures. Polymer semiconductors either are amorphous or contain disordered portions, so their energy states may be localized. With charge transport taking the form of tunneling between localized states, the mobility is thermally activated. Phonons in this case assist charge transport, so the mobility in polymer semiconductors actually rises when the temperature increases.

Conjugated polymer semiconductors are perceived as a one-dimensional lattice because they consist of the repetition of small monomeric units along the chain direction.
A conjugated polymer is characterized by a regular alternation of single and double carbon-carbon bonds, and consequently the electron energy levels are distributed into bands. Due to its low dimensionality, a polymer chain undertakes a profound conformational change in its geometrical structure adjacent to the charge added to the system by photo- or electro- injection. Here the coupling between the charge and the local deformation of the chemical structure is called a polaron. The natural transport mechanism of polarons is hopping because polarons are localized species. The polaron is characterized by the reversal of the bond alternation, as shown in polythiophene below (Fig. 2.5).

![Figure 2.5 The molecular scheme of polaron formation in polyphenylene.](image)

If two electrons are removed from a polymer chain, either a second independent polaron is created, or they combine into a bipolaron. A bipolaron can only be generated when the second removed electron is the unpaired electron of the first polaron and the two positive charges of the bipolaron move as a pair instead of independently.
2.2 Basic Si MOSFET operation [30]

The metal-oxide-semiconductor field effect transistor (MOSFET) is a key component of present-day microelectronics, and closely follows PFET operation. Therefore a review of its basic operation will be illustrative as a starting point for discussing PFETs. Conventional MOSFETs have a planar structure with a thermally grown SiO$_2$ gate insulator, a surface-inversion channel, and localized regions of heavily doped with the doping type opposite to the substrate (Fig. 2.6). These heavily doped regions adjacent to the channel act as the source and drain. In field effect devices, the conductivity of the channel is modulated by an electric field applied normal to the surface of the semiconductor. The MOSFETs work on the principle that a voltage applied to the gate modulates the current flowing between source and drain as a result of the conductance modulation in the semiconductor by the vertical electric field. To discuss the fundamentals of the MOSFETs, a MOS capacitor or MOS-C is first introduced because a basic MOSFET is essentially a MOS-C with two pn junctions adjacent to the region of the semiconductor under the gate.

![Thin Gate Insulator](image)

Figure 2.6 The basic MOSFET structure.
As the simplest MOS device, a two-terminal MOS-C structure is typically composed of a thin SiO$_2$ layer sandwiched between a silicon substrate and a metallic gate plate. The electric contact to the Si substrate is provided by a second metallic layer on the back or bottom side of the substrate. The bias applied to the gate electrode causes the MOS structure to be in an accumulation, depletion, or inversion state. Energy band diagrams are used to describe the static state for the MOS-C. Using an n-type semiconductor as an example, the energy band diagrams are shown in Fig. 2.7.

For an ideal n-type MOS structure, the MOS-C should be in a flat band energy state (Fig. 2.7(a)) when no gate bias is applied. As shown in Fig. 2.7, the Fermi level of the metal should line up with the Fermi level of the semiconductor. With the application of a positive gate bias, the Fermi level in the metal is lowered relative to the Fermi level, $E_F$, in the semiconductor, causing the formation of a positive slope for the energy bands in both the insulator and semiconductor. Negatively charged electrons are drawn toward the semiconductor/insulator interface to maintain the charge balance. That the majority carrier concentration is greater near the oxide/semiconductor interface than in the bulk characterizes accumulation.

The application of a small negative gate voltage slightly raises $E_F$ in the metal above that in the semiconductor and a small negative sloping of the energy bands is formed in both the insulator and semiconductor. The concentration of majority carrier electrons are depleted in the vicinity of the oxide/semiconductor interface as the negative voltage repels electrons from the interface and forms a space region.
Figure 2.7 Energy band diagrams describing the static state in an ideal n-type MOS-C: (a) flat band; (b) accumulation; (c) depletion and (d) inversion.

When a large negative bias is applied to the MOS-C gate, the bands at the semiconductor surface will bend upwards further and the surface region eventually changes from n-type to p-type. The hole concentration at the surface increases from less than the intrinsic carrier concentration, $n_i$, to greater than $n_i$ when the midgap energy at insulator/semiconductor interface $E_{iS}$ exceeds the Fermi level $E_F$. Under these
circumstances, the surface of the semiconductor is commonly referred to as being in the inversion region.

The p-type MOS-C also has three physical distinct biasing regions – accumulation, depletion, and inversion. It is important to pay attention that the bias voltages in a p-type device are essentially reversed in polarity from an n-type device. The band diagrams of a p-type MOS-C are shown in Fig. 2.8. The bias conditions are (a) $V_G = 0$; (b) $V_G < 0$; (c) $V_T > V_G > 0$; and (d) $V_G > V_T$. The quantity $V_T$ is called the threshold voltage. For the special applied bias $V_G = V_T$, the surface minority carrier concentration, in this case electron concentration, equals the bulk majority hole concentration. At $V_G = V_T$, the MOS-C enters strong inversion.

With the basic operation of a MOS-C introduced, the channel formation in MOSFETs will now be easy to understand. In a MOSFET, a current will flow parallel to the semiconductor/insulator interface once a conduction channel is formed between the source and drain. This current is normally called the drain current because charge carriers always enter the structure through the source and leave through the drain, subject to the control of the gate. An inverting gate bias induces a source-to-drain channel and significantly raises the conductance of the channel. To examine the effect of gate bias on the conductance of the channel, the source-to-drain voltage is set at 0 V, using an n-channel MOSFET as the illustration. The gated region between the source and drain islands is just a MOS-C. Under accumulation or depletion bias, the gated region contains very few electrons and the $n^+$ islands of source and drain are electrically isolated. When $V_G$ exceeds $V_T$, an inversion channel is formed adjacent to the Si surface. The induced n-type channel connects the source with the drain and is ready to conduct a current once a
non-zero $V_{DS}$ is applied. The conductance of the inversion channel would be greater at a greater inversion bias due to a greater concentration of electrons induced at the Si surface.

Figure 2.8 Energy band diagram for a p-type MOS-C: (a) flat band; (b) accumulation; (c) depletion and (d) inversion.
Now with the inversion channel created at a bias of $V_G > V_T$, when $V_{DS}$ increases to a small positive voltage, a drain current proportional to $V_{DS}$ begins to flow into the drain terminal. However, the surface channel acts like a simple resistor only over a very small range of $V_{DS}$. As $V_{DS}$ increases above a few tenths of a volt, the slope of $I_D$-$V_{DS}$ starts to reduce. The reduction in the $I_D$-$V_{DS}$ slope occurs because the number of inversion layer carriers decreases as $V_{DS}$ increases. A further increase in $V_{DS}$ causes a progressive reduction in the channel carrier concentration. Eventually the inversion layer completely vanishes at the drain end, which is referred to as pinch-off. The slope of $I_D$-$V_{DS}$ becomes approximately zero after $V_{DS}$ exceeds the voltage where pinch-off occurs, $V_{Dsat}$, and the device is operating in the saturation region. The pinched-off portion in the channel grows wider towards the source end as $V_{DS}$ increasing further, and the drain current $I_D$ remains approximately constant for long channel devices in the pinch-off region (Fig. 2.9).

The drain current in the linear region can be expressed by the equation

$$I_D = \frac{Z_\mu C_o}{L} \left[ (V_G - V_T) V_D - \frac{V_D^2}{2} \right]$$

for $0 \leq V_D \leq V_{Dsat}$ and $V_G \geq V_T$. In the saturation region, the drain current is described differently as

$$I_{Dsat} = \frac{Z_\mu C_o}{2L} (V_G - V_T)^2$$
In the previous equations, $I_D$ stands for source-drain current, $Z$ as the channel width, $L$ as the channel length, $\mu$ as carrier mobility, $C_o$ as the capacitance of the gate dielectric, $V_G$ as gate bias, $V_T$ as threshold voltage, and $V_D$ source-drain voltage.

Figure 2.9 Visualization of various phases of MOSFET operation after inversion channel formation. (a) $V_{DS} = 0$; (b) Moderate $V_{DS}$; (c) pinch-off; and (d) post-pinch-off (Adopted from Ref.[30]).
The general form of the $I_D$-$V_{DS}$ characteristic is illustrated in Fig. 2.10. Moreover, $V_{DSat}$ increases with increasing $V_G$ because a greater number of inversion layer carriers are present at higher $V_G$. In addition, the slope in the linear region of the $I_D$-$V_{DS}$ characteristic is higher with increasing $V_G$ due to the greater conductance of the channel at higher $V_G$.

Figure 2.10 General form of the $I_D$ – $V_{DS}$ characteristics expected from a long channel MOSFET (Adopted from Ref.[30]).

2.3 Features of PFETs

Studies on PFETs appeared in publications frequently since the late 1980’s [31-33]. Generally PFETs take on a similar configuration to that of inorganic thin film transistors (TFTs). The basic structure of a TFT was developed using low conductivity materials such as polycrystalline and amorphous inorganic semiconductors for active matrix liquid crystal displays on a glass substrate. All organic semiconductors are characterized by low mobilities, and their deposition, either by vacuum sublimation or
solution processing, is very similar to the structure of TFTs. The structure of a polythiophene FET is shown in Fig. 2.11.

![Schematic cross-sectional view of a polythiophene FET](image)

Figure 2.11 Schematic cross-sectional view of a polythiophene FET (adopted from Ref. [32]).

The operation of a PFET differs from that of a conventional metal-insulator-semiconductor field effect transistor (MISFET) in that conventional MISFETs operate through a minority carrier channel that forms in the strong inversion regime, while the current flows in a PFET through majority carrier injection in an accumulation channel. The threshold voltage in MISFETs is defined at the onset voltage for strong inversion and there is an isolating depletion layer formed between the channel and the substrate. The definition of threshold voltage of MISFETs can not be applied to PFETs because they do not have an inversion channel. Organic semiconductors are compared more with amorphous inorganic materials rather than conventional crystalline semiconductors because of their similar low mobilities that limit the charge carrier transport. Mobility
values have been improved from the range of $10^{-8} \sim 10^{-5}$ cm$^2$/Vs to 0.1 cm$^2$/Vs for polymers and the order of 1 cm$^2$/Vs for organic small module single crystals over the last twenty years.

2.4 Modeling of organic FETs

The operation of organic FETs has been studied using both analytical models and two-dimensional simulations. Modeling has covered the topics of $I_D$-$V_{DS}$ characteristics, $I_D$-$V_G$ characteristics, trap distributions, short channel effects, electric field dependent mobilities, subthreshold behaviors, and the effect of source-drain contact barriers.

2.4.1 Analytical models of organic FETs

2.4.1.1 The effect of interface traps on organic FET operation

To describe the behavior of OFET operation, Horowitz et al. developed a series of analytical models to fit the experimental data [34-35]. The structure of an organic FET used in this study is shown in Fig. 2.12. One analytical model was developed to describe the operation of OFETs in the accumulation mode. Accumulation mode organic FETs are expected to be already in an ON state at zero gate bias because the channel for current flow already exists due to bulk charges. However, it was observed that a gate bias was needed to reach a threshold voltage to turn the device ON in many real OFETs. Since no gate bias is required to form the channel, the low conductivity in the channel before the gate voltage reached the threshold voltage was attributed to a gate-bias-dependent mobility. To elaborate the origin of the observed threshold voltage, the output
characteristics of two dihexylsexithiophene FETs were analyzed as examples in this study.

![Figure 2.12 Schematic view of an organic field-effect transistor (Adopted from Ref. [34]).](image)

The first device, doped with oxygen by leaving it in air, behaved just as expected. A substantial current flowed at zero bias proving that it did not need any gate voltage to be turned ON. The square root of the saturation current versus gate voltage aligned along a nice straight line. However, the second device measured in vacuum exhibited a different behavior where the square root of its saturation current bent upwards at low gate voltages. A threshold voltage could be derived from this output characteristic and this threshold voltage corresponded to a free carrier density that did not agree with the low conductivity measured. It implied that the low mobility at gate biases below the threshold voltage should account for the discrepancy between the measured data and expected result. The extracted mobility showed an initial linear increase with gate bias but then saturated at a value close to that obtained at high gate voltages.
Horowitz and Delannoy developed another analytical model that took account of a trap distribution in OFETs [35]. It was suggested that organic semiconductors had narrow trap distributions because molecules in an organic compound are weakly bound by van der Waals forces and the traps mainly locate between the valence band edge and the Fermi level. The model was able to predict the behavior of actual alpha-conjugated sexithienyl (α6T) FETs (Fig. 2.13) and the parameters extracted from the model were compared to those obtained from temperature dependent current-voltage measurements of Au/α6T/Au sandwich structures. It was shown that the behavior of the OFET can be divided into low gate voltage regions and high gate voltage regions. At low gate biases, a major portion of free carriers are trapped and the saturation current density varies as the squared gate voltage. At higher gate biases where all traps are filled, the saturated current density varies as $(V_g - V_t)^2$, in which $V_t$ corresponds to the gate voltage where the free-carrier density equals the trap density. The effective mobility at low gate biases is lower than the microscopic mobility by a factor of the ratio of free-to-trap carrier densities, whereas at high gate biases the mobility is equal to the microscopic mobility of the semiconductor. Here the microscopic mobility means the mobility is independent of the gate voltage. Though the extracted mobility in the OFET is much lower, the energy of the shallow trap level determined from the model is very close to those obtained from the Au/α6T/Au sandwich structures. The lower mobility in an OFET can be explained by the factor that charge transport in FETs is greatly influenced by the insulator-semiconductor interface.
Figure 2.13 $I_d^{1/2}$ vs $V_g$ plot for a $\alpha$6T FET. The dashed line indicates the corresponding numerically computed saturation current (Adopted from Ref. [35]).

2.4.1.2 Temperature and gate-voltage dependent mobility in OFETs

Horowitz et al. also developed a multiple trapping and release (MTR) model and a grain boundary model to analyze the behavior of polycrystalline OFETs [36]. The field effect mobility of sexithiophene (6T) FETs was derived from their I-V characteristics by the transconductance equation for low drain voltages

$$g_d = \frac{\partial I_d}{\partial V_d} \approx \frac{Z \mu C_{i} (V_g - V_o)}{L}.$$
The zero voltage $V_0$ in the transconductance equation is defined as

$$V_0 = \pm \frac{q n_0 d_s}{C_i} + V_{FB}$$

where $n_0$ is the density of free carriers in the bulk, $d_s$ is the thickness of the semiconductor, and $V_{FB}$ is the flatband voltage. This equation is adopted for the mobility extraction because it is valid even for the case of a nonconstant mobility as long as the drain voltage is much lower than the gate bias. It was found that the extracted mobility has a linear relationship with applied gate bias once the effect of the contact resistance is corrected (Fig. 2.14).

The field-effect-mobility dependence on temperature can be divided into three regions, (1) a high temperature region, (2) a low temperature region, and (3) an intermediate region [36]. The mobility is thermally activated in the high temperature region of $T > 100$ K, and it is practically independent of temperature in the low temperature range of less than 25 K. At the intermediate temperatures, charge transport occurs via thermally activated tunneling, but the activation energy is substantially reduced compared to that of the high temperature region. Both the MTR and grain boundary models are based on a trapping mechanism that most of the injected carriers are trapped in states localized in the forbidden gap. In the MTR model, the traps were assumed uniformly distributed in the semiconductor film and analytical equations were derived to estimate the energy distribution of traps. It turned out that the MTR model cannot account for the temperature independent mobility at temperatures lower than 25 K.
Figure 2.14 Variation of the hole mobility of a sexithiophene evaporated polycrystalline film as a function of gate bias. Closed circles correspond to uncorrected data, and open circles to data corrected for the contact series resistance (Adopted from Ref. [36]).

Instead of the uniformly distributed traps of the MTR model, the traps are assumed to be mainly located at the grain boundaries in the grain boundary model. One crucial condition for the grain boundary model to be differentiated from the MTR model is that the size of the grains has to be larger than the Debye length \( L_D = \sqrt{\frac{ekT}{q^2N}} \), otherwise the grain boundary model will converge towards the MTR model. Charge transport is determined by the mechanism of transfer through grain boundaries in the grain boundary model. The mobility calculated using the grain boundary model qualitatively follows the
temperature dependence of mobility at high, intermediate, and low temperatures, but the calculated mobility is three to four orders of magnitude higher than the mobility extracted from experimental data. The discrepancy between model and experimental results could be due to the absence of possible temperature and gate voltage dependence on the potential barrier and the concentration of trapped charges at the grain boundaries.

Vissenberg and Matters derived a theory for the field effect mobility in amorphous OFETs based on the hopping mechanism of charge transport between localized states [37]. Instead of activating carriers to a transport level, hopping is a thermally activated tunneling of carriers between localized states. An analytic expression was obtained for the field effect mobility as a function of temperature and gate voltage. The field effect mobility has an Arrhenius-like temperature dependence \( \mu \sim \exp[-E_a/(k_BT)] \), where \( E_a \) is the activation energy. The activation energy, \( E_a \), is a function of gate voltage in that it decreases with increasing gate bias (Fig. 2.15). Charges accumulate at the semiconductor/insulator interface with the presence of gate bias and fill the energy states starting from lower-lying energy sites [37]. Additional charge carriers brought down by higher gate voltage will occupy states at higher energies, so less activation energy is required for these charges to hop to neighboring sites. Assuming the relative dielectric constant to be about 3, which is appropriate for most organic solids for both pentacene and polythienylene vinylene (PTV), the field effect mobility was calculated. The agreement between theoretical calculation and experimental data was quite good. The activation energy for PTV is about twice that for pentacene, and the field effect mobility is more than two orders of magnitude lower than that in pentacene.
Figure 2.15 Activation energy $E_a$ for the field-effect mobility in a pentacene and a polythienylene vinylene (PTV) thin-film transistor as a function of the gate voltage $V_G$. The experimental data is shown with square symbols and the solid lines are calculated (Adopted from Ref [37]).

The difference was mainly attributed to the structural order of the organic films. Pentacene has better stacking properties than PTV, which results in a larger area of overlap of the electronic wave functions and higher tunneling probability between different sites. The overlap parameter in the theoretical expression reflected the influence of morphology of the organic films on the field effect mobility. A more recent study on the mobility in pentacene FETs by Fritz et al. [38] showed that the mobility is strongly
dependent on crystallinity, defects within the crystal structure, grain boundaries, and surface effects.

2.4.1.3 Short channel effects in OFETs

Short channel effects in sexithiophene (6T) FETs (Fig. 2.16) were studied analytically by Torsi et al. [39]. In short channel devices, the potential distribution in the channel region and the electric field become two dimensional and the gradual channel approximation is not valid any more. Channel shortening and parasitic resistance have been taken into account in short channel device modeling. Parasitic resistance influences the extracted field-effect mobility through its effect on the apparent threshold voltage. A comparison between the parasitic resistance extracted from the model and the total device resistance measured as the ratio between $V_{DS}$ and $I_D$ in saturation region showed that the parasitic resistance was more than ten times lower than the total resistance of the device. This low value of parasitic resistance can be explained the large overlap between the source/drain and the un-patterned gate, based on the experimental observation that parasitic resistance decreases with larger source/drain to gate overlap in TFTs [40]. The calculated threshold voltage had a value of 20 V and it in turn yielded a residual doping concentration of $7 \times 10^{16}$ cm$^3$ in 6T. An average gate length shortening of 2 µm was calculated for 25 µm devices and about 1 µm for 4 µm devices. The mobility increase with applied gate voltage was explained by two reasons: the parasitic resistance becomes smaller with higher gate bias and a decrease occurs in the percentage of trapped charges at higher gate bias.
Figure 2.16 Families of normalized $I_D$ at different gate fields as a function of the longitudinal field ($E_{DS} = V_{DS}/L$) (Adopted from Ref. [39]).

The drain current normalized by the corresponding channel length should be identical when gate field is the same, but the experimental results showed increased normalized current when the channel length decreased even at the same gate electric field. To justify the increase in the normalized current, the longitudinal electric field dependence of mobility observed above electric field of $10^5$ V/cm must be included in the model (Fig. 2.17). The mobility dependence on longitudinal electric field could be due to a larger tunneling probability between the polycrystalline grains in 6T. The calculated electrical characteristics agree with the experimental data only when a longitudinal field dependence of the mobility was included in the model.
2.4.2 Two-dimensional numerical simulations of organic FETs

Though analytical models are valuable for quick estimation of device parameters, two-dimensional numerical simulations can overcome the approximations and simplifications in analytical equations and provide a more accurate evaluation for the device operation.
2.4.2.1 Numerical simulation of organic FET I-V characteristics

A two dimensional simulation of OFETs was performed by Alam et al. [41] based on sexithiophene (6T) FETs. In this simulation, an effective density of states was defined as a single energy level at the band edge to equate the gaussian distribution of states in 6T. The standard drift-diffusion equations were used to simulate the electrical characteristics of OFETs. The field mobility was expressed as

$$\mu(E,T) = \mu(0,T) \sqrt{1 - \frac{2qaE_b}{E_{\text{t}}} \exp \left( \frac{4qaE_b \tanh \left( \frac{\hbar \omega}{4kT} \right)}{\hbar \omega} \right)}$$

which is dependent on the polaron binding energy $E_b$, hopping distance $a$, electric field $E_{\text{t}}$, phonon energy $\hbar \omega$ that assists in the hopping transport, and temperature $T$. In most organic materials, the electric field as well as temperature can increase the carrier mobility by lowering the potential barrier for hopping transport, which is opposite to the effect these processes have in inorganic crystalline materials. The contacts were assumed to be ohmic in the modeling. The simulation results showed that the potential profile of 6T FETs is mostly one-dimensional, except near the drain. This result explains why the experimentally measured electrical characteristics of alpha sexithiophene FETs could be reproduced well using a 1-D analytical model (Fig. 2.18).
Figure 2.18 The 2-D constant potential profile of a 1.5 µm transistor (Adopted from Ref. [41]).

Another observation of the simulation results is that the I-V characteristics are relatively insensitive to the thickness of the conducting film because most of the charges remain confined within 50 Å of the surface under a wide range of drain and gate voltages [42]. This observation is contradictory to some other studies of polymer FETs and oligomer FETs [32, 33], which found that there is an optimum film thickness for PFETs. For thicknesses thinner or thicker than this thickness range, the gate bias has less modulation on the charge transport. In addition to the channel portion near the polymer semiconductor film at the semiconductor/insulator interface, the bulk region of the organic film acts as a resistance and conducts a leakage current under $V_{DS}$ bias. The measured drain current is actually composed of two components, which are the channel current and the leakage current through the bulk of the polymer layer due to its intrinsic conductivity. Unlike the channel current, this leakage current is independent of gate bias, but proportional to $V_{DS}$. As presented by Tsumura et al. [32], PFETs with thick polymer
layers did not saturate. However, if the polymer semiconductor film is un-doped, PFETs with even thicker film can saturate at high $V_{DS}$ values. This observation proved that the lack of saturation in thicker samples with relatively high doping concentrations was caused by the uncontrollable leakage current through the bulk of the organic semiconductor film. In thinner films, the leakage body current is reduced, but the channel conductivity is also lowered due to the thickness-dependent free-carrier-density per unit surface area in the polymer semiconductor layer. Mobility can also be lower in thin films due to surface scattering if the thickness is comparable to the surface roughness.

2.4.2.2 Top versus bottom source/drain contacted organic FETs

Tessler et al. performed a two-dimensional simulation for top source/drain contact PFETs [45], but PFETs can take either top contact (staggered) or bottom contact (coplanar) configuration [46], as shown in Fig. 2.19. In a top contact configuration, the source and drain contacts are deposited on the top surface of the organic material. Charge carriers injected by the source contact vertically traverse the organic layer before they reach the organic/insulator interface and form a channel there. In a bottom-contacted configuration, the source and drain contacts are formed directly onto the gate insulator before the organic active layer is deposited. Here injected charge carriers will arrive at the organic/insulator interface without traveling vertically in the organic film.

Though most publications claimed that top contact PFETs had higher output current than their bottom contact counterpart, bottom contact devices are still in favor due to their ease in fabrication. The deposition of the functional polymer is the final process step for a bottom-contacted PFET, so all the previous fabrication steps can be
completed in ambient air even if the polymer semiconductor is sensitive to oxygen and water vapor. As the last layer added to the bottom contact structure, the polymer semiconductor film is also protected from any contamination during the previous fabrication steps.

![Illustration of top source-drain contacts and bottom source-drain contacts configurations](image)

Figure 2.19 Illustration of top source-drain contacts and bottom source-drain contacts configurations (Adopted from Ref. [46]).

The operation of a top contact PFET modeled by Tessler et al. [45] was calculated by solving the Poisson equation. The mobility was assumed to be at a constant value of $5 \times 10^{-3}$ cm$^2$V$^{-1}$s$^{-1}$ and the injection barrier was first set to be 0.2 eV for the two dimensional simulation. The organic layer was treated as an undoped wide bandgap
semiconductor and the only source for mobile charge were the metal electrodes. The simulated carrier density profile showed that the region underneath the source/drain contacts became charged after the application of the gate voltage. The potential distribution inside a PFET showed that a negligible voltage drop occurs across the polymer film and the gate bias drops almost entirely across the insulator only. This explains in many cases why the I-V characteristics of top contact PFETs are similar to those of bottom contact PFETs. It is observed from the charge density distribution that the channel is formed by the charges injected from both the source and drain contacts, but the source injection is more effective because the bias between the drain and gate is lower than that of the source-gate bias. There is also charge accumulation outside the active device area due to charge carrier diffusion. It was also noticed that the entire source-drain bias dropped across the channel with no voltage drop vertically across the active layer. Nevertheless, as the value of the injection barrier increased from 0.2 eV to 0.5 eV, there would be a vertical voltage drop across the polymer film. The barrier at the metal/polymer interface will reduce the effective magnitude of gate bias thus causing the threshold voltage to increase, which produces a bias dependent mobility. Another observation to the simulation result is that only a fraction of the contact area, called the effective contact area, is used to inject charge carriers. According to the simulated current density distribution in the FET, the effective contact area grows with the height of the charge injection barrier, as shown in Fig.2.20.
Figure 2.20 Calculated steady state current distribution just underneath the contact plane. The dashed line was calculated for contact barrier of 0.2 eV and the solid line was calculated for contact barrier of 0.5 eV. Note that for this figure calculation the contact width was increased from 1 to 5 mm while keeping the channel length constant (Adopted from Ref. [45]).

Li et al. [47] carried out a two dimensional simulation focused on a theoretical investigation of the surface potential in bottom contact using P3HT FETs. The model was built by solving the two dimensional current continuity equation involving drift and diffusion currents together with Poisson’s equation. The hole mobility was assumed to be $5 \times 10^{-3}$ cm$^2$V$^{-1}$s$^{-1}$, the same as used in the top contact PFET simulations. The injection
barrier for the metal/organic contacts was modeled as Schottky barriers with various barrier heights. The parasitic resistance was found to play an important role in the simulation. It was generally assumed that the injection and extraction of charge carriers take place in the very small regions along the vertical faces of the source and drain contacts directly adjacent to the channel, so there should be no parasitic resistance for bottom contact devices. However, if a parasitic resistance was not considered for the injection and extraction of charge carriers into and out of the channel, the simulation results poorly reproduced the experimental results of P3HT FETs. Without a parasitic resistance included, the simulated surface potential will drop above the edge of the source contact if the injection barrier is sufficiently high, but this drop will not happen at the drain contact even with a high contact barrier of about 0.5 eV. The explanation of this simulation result is that the source/channel junction is reverse biased, while the channel/drain junction is forward biased. However, this simulation result disagrees with the experimental measurements obtained by scanning Kelvin probe microscopy. A significant potential drop of comparable magnitude was observed above both the source/channel and channel/drain junctions. To reconcile the discrepancy between the simulation and experimental results, modifications were made to the ideal bottom contact PFET structure by including parasitic resistances in the model. The parasitic resistances in the modified model arises from the proposed situation that charge carriers are injected at the source contact and collected at the drain contact predominantly through the top surfaces instead of the vertical face of the contacts (Fig. 2.21).
Figure 2.21 Schematic representation of a P3HT FET structure. The material along the edges of the contacts may be structurally disordered with low mobility and high concentration of traps, which forces charge injection from the top surface of the S/D contacts instead of the lateral surface (Adopted from Ref. [47]).

Charge injection and extraction through the top surfaces of contacts could occur when the regions immediately adjacent to the vertical contact faces are covered with disordered material with negligible mobility or high concentration of traps. The structure of the polymer layer along the edges of the contacts is usually disrupted during the deposition, so carrier transport through the vertical contact faces is likely to be hindered by disordered low conductance regions in real PFETs. In this case, the charge carriers have to move along the paths in the polymer layer between the top surfaces of the two contacts, where the carrier concentration is significantly lower than in the channel and results in relatively high resistance. For the modified model significant voltage drops appear in both regions of the drain and source contacts, and the voltage drops are in
comparable in magnitude when the operation is in the triode regime. When the contact barrier is high enough, the source resistance appears to be greater than the drain resistance.

2.4.2.3 The effect of contact barrier and electric field dependent mobility on output characteristics of organic FETs

Bolognesi et al. [48] addressed the influence of carrier mobility and contact barrier height on the operation of OFETs using two dimensional simulations. The field dependence of mobility is expressed as

$$\mu = \mu_0 \exp \left( \frac{E}{E_0} \right)$$

where $\mu_0$ is the low field mobility and $E_0$ is a critical field. A low field mobility of $5.4 \times 10^{-3}$ cm$^2$V$^{-1}$s$^{-1}$ was used in their simulation and the critical field calculated from Monte Carlo simulation was $3 \times 10^5$ V/cm. The different injection efficiency of the contacts was accounted for by using assumed barrier heights of 0.1 eV for one simulation and 0.4 eV for another simulation. The I-V characteristics calculated with field dependent mobility are quite distinct from those calculated using a constant mobility in the low V$_{DS}$ region where V$_{DS}$ is less than 30 V. The drain current increases linearly with V$_{DS}$ in the constant mobility model, while a superlinear behavior was calculated with the field dependent mobility model. The superlinear effect reduces at lower barrier heights.

According to the simple analytical expression for channel conductance

$$g_{d} = \frac{\mu C_{ox} Z(V_{GS} - V_{T} - V_{DS})}{L}$$
the value of $g_d$ should decrease linearly with higher $V_{DS}$. However, the channel conductance did not change monotonically with $V_{DS}$, instead it increased initially followed by a subsequent nonlinear reduction. Again the lower barrier heights effectively reduced the nonlinear effect. The calculated square root of the saturation drain current as a function of the gate voltage showed a good linear behavior if low barrier contacts were used in the simulation. With high barrier contacts, the curve is slightly nonlinear close to the threshold voltage. The non-ideality caused by the high barrier contacts can cause errors in the evaluation of channel mobility.

The effect of a contact barrier at the source/drain contacts and the effect of an electric field dependent mobility have also been studied by Cherian et al. [49]. A two dimensional model was based on solving the continuity equation, drift-diffusion current and Poisson’s equations. Simulations for two dimensional models were performed for four cases: (1) a constant mobility and ohmic contact, (2) constant mobility and contact barriers, (3) field dependent mobility and ohmic contacts, and (4) field dependent mobility and contact barriers. The field effect mobility was modeled as

$$\mu = \mu_0 e^{\gamma \sqrt{E}}$$

when mobility variations with gate bias was considered in the simulation of cases (3) and (4). For cases (2) and (4), contact barriers were included to account for the high resistance caused by the injection barrier at the source electrode in organic FETs [50-51]. Temperature dependence was neglected in this model since the measurement temperature was controlled at a constant value. The simulation results were compared to the output characteristics of phthalocyanine OFETs. The modeling using the last case matched the experimental data the closest, which indicates in real device operation both contact
barriers and field dependent mobility influence the transfer characteristics of OFETs (Fig. 2.22).

(a)

(b)

Figure 2.22 Numerical fit to the IV curves using (a) a constant mobility and ohmic contacts; (b) a constant mobility and a contact barrier of 0.4 eV; (c) an electric field dependent mobility and ohmic contacts; and (d) a field dependent mobility and a contact barrier of 0.415 eV (Adopted from Ref. [49]).

(Continued)
2.4.2.4 Subthreshold behavior simulation

The two dimensional simulation by Scheinert et al. [52] of poly(3-dodecylthiophene) (P3DDT) PFETs with a poly(4-vinylphenol) (P4VP) gate dielectric found that the high inverse subthreshold slope (S) and the drain voltage dependent subthreshold current are due to trap states either at the semiconductor/insulator interface
or in the bulk. The standard drift-diffusion model was used to implement the two-dimensional simulation. The bandgap of P3DDT is 2 eV, and its electron affinity is 3 eV. The dielectric constants determined from optical measurements were 2.56 for P4VP and 3.24 for P3DDT. The mobility used in their simulation was on the order of $10^{-3} \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$.

A few doping concentrations in the range of $10^{15} \text{ cm}^{-3}$ up to a few times $10^{17} \text{ cm}^{-3}$ were tested in the simulation. It was found that the simulated inverse subthreshold slope is always too low compared to the experimental measurements no matter what doping concentration was used. To imitate the subthreshold transfer characteristics, the model was modified to include interface or bulk traps with energy states in the band gap. The traps can be modeled as either acceptor-like or donor-like, depending on the doping concentration. Acceptor-like interface traps were assumed for the doping concentration of $10^{16} \text{ cm}^{-3}$ because only acceptor-like traps at this doping concentration will push the threshold voltage to a positive value. If the doping concentration of $10^{17} \text{ cm}^{-3}$ instead of $10^{16} \text{ cm}^{-3}$ was assumed in the model, a fixed positive interface charge of $3 \times 10^{11} \text{ cm}^{-2}$ and donor-like interface traps are needed to fit the simulated curves with the measured ones above threshold. The simulation with donor-like interface traps was partially successful, but the acceptor-like interface traps were more effective in reproducing the experimental data (Fig. 2.23). The same approach applied to bulk traps and again the acceptor-like assumption works better than the donor-like assumption [52-53].
Figure 2.23 Experimental transfer characteristics and simulated ones with (a) acceptor-like traps and (b) donor-like traps (Adopted from Ref.[53])
The simulation adopting acceptor-like traps found that the subthreshold current would increase with higher densities of traps at a constant energy, or it would increase with the reduction of the separation between the trap and valence band energies at a constant interface trap density. Inclusion of the traps at the interface or in the bulk also enabled the numerical model to mimic the drain voltage dependence of the subthreshold drain current in PFETs, which contradicts the ideal long channel behavior that the drain voltage has little influence on the drain current once the drain voltage exceeds a few kT/q. To identify whether it is interface traps or bulk traps responsible for the peculiar subthreshold behavior in P3DDT FETs, the subthreshold swing of P3DDT FETs with P4VP dielectric was compared to P3DDT FETs with a SiO$_2$ gate dielectric. If bulk traps were responsible for the peculiar subthreshold behavior, with the same bulk structure of P3DDT, the subthreshold swing of PFETs with SiO$_2$ gate dielectric should have the same high value as that of PFETs with P4VP gate dielectric. However, PFETs with a SiO$_2$ gate dielectric has a subthreshold swing 30 times lower than that of PFETs with P4VP dielectric. Based on the analysis above, it seems that the interface traps are the major contributor to the high subthreshold swing, but analyzing only current characteristics of transistors is hardly sufficient to draw a definitive conclusion. More information on the devices has to be obtained from additional measurements to distinguish between the influence of interface traps and that of bulk traps.
2.5 Mobility of PFETs

Mobility is the central figure-of-merit for transistors. It has been a source of comparison since the first PFET was fabricated electrochemically in 1986 [31]. Since polymer semiconductors have low mobility by nature, ways to improve the mobility in PFETs significantly has been intensely pursued. It is a goal of researchers to match or exceed the mobility and the ON-OFF ratio for Si thin film transistors, so that PFETs can be used in large area active displays as driving devices. In contrast to Sect. 2.4, which discussed the electric field dependence of mobility in PFETs using modeling, this section introduces more experimental efforts to improve the mobility in PFETs. Early efforts to improve mobility in PFETs were in their trial stage, so they were less directed. One of the early works by Holland et al. explored the possibility of higher mobility in more ordered polymer films [54], but this study failed to demonstrate the beneficial effects of ordered polymer systems. Fortunately with accumulated experience and growing wisdom, the ordering in polymer semiconductors was effectively improved later and the mobility of PFETs finally caught up with amorphous Si TFTs.

2.5.1 Early research on mobility of PFETs

The early PFETs had a very low value of mobility, in the range of $10^{-5}$ cm$^2$V$^{-1}$s$^{-1}$ [31]. The polythiophene (PT) FETs reported by Tsumuru et al. [31] in 1986, probably the first PFET work published, was fabricated using a bottom contact configuration, where the polythiophene film was deposited electrochemically. The field effect was only observed when the PT film was electrochemically undoped. The bandgap was electrochemically determined to be 2 eV. Though polymer films deposited from solutions
are a far more popular method for PFET fabrication nowadays, Tsumuru et al. set a valid example that the mobility of polymer semiconductors can be extracted from the PFETs transfer characteristics.

Another early paper on P3HT FETs published by Assadi et al. in 1988 used spin-coating to deposit the P3HT film from a chloroform solution [42]. The mobility was found to be sensitive to the film thickness. The calculated mobility in a film with a thickness less than 500 Å could be two orders of magnitude lower than that for thicker samples. Other than its sensitivity to film thickness, Assadi et al. also observed a decrease in mobility with increased temperature in the range of 300 to 350 K. Due to the low mobility of polymer semiconductors, hopping was speculated as the likely mechanism for charge carrier transport in polymer semiconductors, but the decrease in mobility with elevated temperature is not consistent with a hopping model. Optical spectra of the polymer film suggested conformation defects in the polymer chain, and the formation of defects can explain the decrease in mobility at higher temperatures.

The mobility of 3[2(S2-methyl-butoxy)ethyl]-polythiophene (PMBET) FETs spun from different solvent mixtures were evaluated by Holland et al. [54] to investigate the effect of morphology on polymer channel mobility. Unfortunately this work did not reveal the advantage of ordering for mobility improvement due to the ineffective experimental approach. In this study, various morphologies of PMBET were attained by adding “bad solvent” methanol to the PMBET solution in THF. The addition of a poor solvent caused aggregation and finally precipitation when the ratio of methanol:THF exceeded 4:10. The mobility dropped drastically as the content of methanol increased.
The low mobility was explained by the reduced hopping probability with increased interchain separation as the polymer chains become rigid at the presence of methanol.

The mobility of polythienylenevinylene (PTV) FETs was determined to be $0.22 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ by Fuchigami et al. [55]. The mobility was extracted from the plot of the square root of the drain current against the gate voltage for a device with interconnected gate-drain electrodes. It was found that the mobility increased linearly with the conversion ratio of the reaction from the precursor to PTV. The conversion, which transforms the precursor to a $\pi$-conjugated polymer (Fig. 2.24), occurs in the presence of heat and HCl.

![Chemical Structures](image)

**Figure 2.24** The chemical structures of the precursor polymer and PTV after conversion (Adopted from Ref. [55]).
The effective $\pi$-conjugation length is enlarged as the conversion ratio increases, so the enhancement in mobility was considered largely dependent on the $\pi$-conjugation length of PTV.

2.5.2 Improved mobility in ordered polymer films

To improve mobility in PFETs, the most popular method is to introduce structural ordering into the polymer films. Charge transfer along the polymer chain is much faster than interchain transport, but interchain transport is unavoidable in a three-dimensional polymer system. The efficiency of interchain transport depends on the separation distances between polymer chains, so better packing of polymer chains will enhance transfer rates. The most often seen techniques to create oriented polymer films are: mechanical rubbing, the addition of an alignment layer, or self-organization [56-64].

2.5.2.1 Mechanical rubbing

The improvement in channel mobility in an aligned functional polymer layer generated by mechanical rubbing was investigated for P3HT FETs by Heil et al. [56]. Small layer thicknesses in the range of 20 nm down to 6 nm were used to ensure the orientation of the P3HT layer was quite close to the gate insulator. The substrates were cleaned and HMDS treated before the deposition of the functional layers. Samples were rubbed at $100^\circ$C with a piece of velvet. Elevated temperatures increase the flexibility and allow repositioning of the polymer chains, but a temperature higher than $100^\circ$C leads to a strong decrease in the mobility in OFETs. Test results showed that rubbing ten times was enough to induce a considerable difference in the polymer orientation. Instead of
relaxation, the aligned polymer chains tend to orient further when the rubbed samples were heated a second time at 100°C due to chain to chain interactions. The mobility of the samples rubbed perpendicular to the charge transport direction dropped by a factor of 17 compared to the control samples, whose mobility was on the order of $10^{-4}$ cm$^2$V$^{-1}$s$^{-1}$.

On the other hand, the mobility increased 4 times in the PFETs rubbed for the direction of charge transport. It was further improved by a factor of more than 2 after annealing.

Another method to generate aligned PFETs by mechanical rubbing is called the friction-transfer technique developed by Tanigahi et al. [57]. An oriented thin film will be formed on the clean surface of a substrate by rubbing a piece of solid polymer against the substrate. Solid polymer pellets are formed from a polymer powder by compression. The film preparation setup is as shown in Fig. 2.25.

Figure 2.25 Schematic picture of the equipment for polymer film preparation by the friction-transfer technique (Adopted from Ref.[57]).
The preparation temperature is critical to the properties of the polymer thin films. The temperature has to be high enough to ensure uniform films, otherwise the film will be discontinuous. On the other hand, the temperature should not be so high that it will cause thermal decomposition of the polymer. The friction-transfer technique opened a door for the application of polymer semiconductors that can not be dissolved in organic solvents. P3HT and poly(3-dodecylthiophene) (P3DDT) FETs were fabricated by the friction-transfer technique [58]. Polarized optical absorption spectra proved that the polymer chains were strongly aligned parallel to the friction direction. The test results of those two types of PFETs showed that a high mobility was obtained if the current flow is parallel to the polymer chain alignment direction. For P3HT FETs, $\mu_{\text{parallel}} (\text{P3HT}) > \mu_{\text{amorphous}} (\text{P3HT}) > \mu_{\text{orthogonal}} (\text{P3HT})$, where $\mu_{\text{parallel}}$ was 2 to 5 times $\mu_{\text{amorphous}}$ and 10 to 20 times that of $\mu_{\text{orthogonal}}$. The situation is different in P3DDT FETs, where $\mu_{\text{parallel}} (\text{P3DDT}) > \mu_{\text{orthogonal}} (\text{P3DDT}) > \mu_{\text{amorphous}} (\text{P3DDT})$ and enhancement values as high as 20 to 70 were observed. The results suggest faster charge carrier transport occurs along the main chain than transport between chains separated by alkyl side chains.

2.5.2.2 Alignment sublayer

Several groups have also fabricated aligned poly(9,9-dioctylfluorene-co-bithiophene) (F8T2) FETs using a thin polyimide layer as the alignment layer to induce long range ordering in the overlaying F8T2 film [59-60]. F8T2 was chosen because its thermotropic liquid crystallinity above 265°C allows better packing of the F8T2 chains via self-assembly. F8T2 is also relatively stable in air and soluble in a wide range of
solvents. A mechanically rubbed polyimide sublayer allows F8T2 to align parallel to the rubbing direction after a post-rubbing heat treatment.

Sirringhaus et al. [59] used a top-gate configuration in their F8T2 PFETs (Fig. 2.26).

![Figure 2.26 Top gate F8T2 FETs with a polyimide alignment layer (Adopted from Ref. [59]).](image)

The F8T2 film was first heated at 275 to 285°C for 3 to 15 min to align the polymer chains in its nematic liquid crystalline (LC) phase along the underlying polyimide, followed by a quenching at room temperature to preserve the polymer chain alignment but prevent its crystallization. Polarized optical absorption spectra was employed to examine the degree of alignment. No dissolution nor swelling was observed in F8T2 films after the gate dielectric poly(vinylphenol) (PVP) was spin-coated from its solution
in alcohol solvents such as isopropanol. An abrupt interface formed between the two 
solution-deposited semiconductor and insulator layers. Parallel mobility of F8T2 FETs 
was in the range of 0.009 to 0.02 cm²V⁻¹s⁻¹, while the perpendicular mobility was in a 
much lower range of 0.001 to 0.002 cm²V⁻¹s⁻¹. It was found that the anisotropy 
\( \frac{\mu_{\text{parallel}}}{\mu_{\text{perpendicular}}} \) only weakly depended on temperature variations. The sizes of the LC 
domain estimated from optical micrographs were on the order of 0.1 to 1 μm, so each 
FET channel length likely contained several domain boundaries. According to the fact 
that LC F8T2 FETs had significantly higher mobility than as-spun samples, it was 
postulated that the LC domain boundaries had less interference to the charge carrier 
transfer in the channel than the crystalline grain boundaries in as-spun F8T2 films. Since 
the straight chain segment is much smaller than the FET channel length, the rate-limiting 
step was concluded to still be the interchain hopping process in aligned F8T2 films even 
though the charge transport direction was parallel to the channel length. Therefore, the 
mobility anisotropy should be interpreted as the average distance that the charge carriers 
travel along the chain between two interchain hopping events is larger in parallel devices 
than in perpendicular devices.

In another report on F8T2 FETs by Kinder et al. [60], the polyimide sublayer was 
spin-coated from its diluted solution and hand-rubbed with a rayon cloth after curing. The 
rubbed polyimide layer had a thickness of about 40 nm, and it was atop 200 nm of 
thermal SiO₂ which together acted as the gate dielectric material (Fig. 2.27). The F8T2 
film on top of the rubbed polyimide received a heat treatment after its deposition. The 
heat treatment in a nitrogen ambient brought the F8T2 into a mesophase for self-
alignment along the grooves in the rubbed polyimide layer. The channel mobility
calculated in the saturation ranged from $2 \times 10^{-3}$ to $1 \times 10^{-2}$ cm$^2$V$^{-1}$s$^{-1}$ for F8T2 FETs whose current flow was in parallel with the polymer backbone. The anisotropy ratio, defined as $\mu_{\text{parallel}}/\mu_{\text{perpendicular}}$, had values of 3.5 to 6.5.

![Diagram of F8T2 FET structure](image)

Figure 2.27 Bottom gate F8T2 FETs using polyimide as both alignment layer and a second gate dielectric (Adopted from Ref.[60]).

2.5.2.3 Self-organization

High mobilities were also demonstrated using a self-oriented process with regioregular poly(3-alkylthiophene) (P3AT) FETs [61-64]. An alkyl group can be incorporated into the polythiophene backbone in the form of head-to-tail (HT) or head-to-
head (HH) configuration. If P3AT contains both HT and HH in a random pattern, it is said to be regiorandom. Regioregular P3AT has either the configuration HT or the configuration HH, but never both (Fig. 2.28).

![Chemical structures of head-to-tail and head-to-head P3AT](image)

Figure 2.28 Chemical structures of head-to-tail and head-to-head P3AT (Adopted from Ref.[61]).

The P3HT used for these studies of self-organized PFETs was the HT configuration, and its properties are different from regiorandom P3HT. Regioregular P3AT has a smaller band gap and better ordering and crystallinity than regiorandom P3AT. The mobility in
regioregular P3HT FETs processed from a chloroform solution has been reported as high as 0.1 cm$^2$V$^{-1}$s$^{-1}$ [64]. The high mobility was attributed to the ordering in the polymer films due to the preferred orientation of regioregular P3HT chains. It was postulated based upon the reflection x-ray geometry that the backbone of regioregular P3HT was parallel to the substrate while the hexyl side chains might be normal to the substrate. This preferred orientation of regioregular P3HT would place the carrier transport direction parallel to the substrate, which allows high mobility in this direction.

The mobility of regioregular P3HT also depends on solvent volatility and how the film was deposited. The mobility could be as low as $\sim 10^{-5}$ cm$^2$V$^{-1}$s$^{-1}$ if the regioregular P3HT was dissolved in p-xylene and spin-coated. Higher mobility was achieved with tetrachloroethane and chloroform solvents, while THF, p-xylene and toluene showed lower relative mobilities for regioregular P3HT. The quality of the films can be quite distinct, because the degree of film discontinuity and particularly agglomeration might vary with the solubility of the polymer in a solvent and the evaporation rate of the solvent. The coating process of the P3HT deposition from a solution also influences the channel mobility in P3HT FETs. It was found that regioregular P3HT FETs prepared by spin-coating generally had lower mobility than drop-cast samples. Drop-cast polymer films have better ordering than spin deposited films due to the slower evaporation of the solvent from the drop-cast polymer films which allows more time for the polymer chains to orient. However, the off current in drop-cast FETs is higher than spin-coated samples, which could be due to the larger bulk leakage current between the source and drain in thicker drop-cast films. The off current could be reduced by heating the sample in nitrogen at 100$^\circ$C for 5 min, but too high an annealing temperature leads to dramatically
lower mobility [61]. Further research on regioregular P3HT FETs quantitatively proved that P3HT FETs prepared by dip coating yield higher mobilities, compared to the samples prepared by spin coating or drop casting [62]. Dip-coated bottom contact P3HT FETs were fabricated by dipping an SiO$_2$/Si substrate into a P3HT solution after a hexamethyldisilazane (HMDS) treatment and subsequently being removed at a speed of 0.2 to 0.5 mm/s. The film thickness was in the range of 20 to 40 Å. The dip-coated P3HT FETs with 25 µm gate length showed saturation, but samples with a 5 µm gate length barely saturated. The mobility extracted from 25 µm gate length FETs was 0.12 cm$^2$V$^{-1}$s$^{-1}$, while 5 µm gate length was higher at 0.18 cm$^2$V$^{-1}$s$^{-1}$. The higher mobility in dip-coated PFETs implied improved structural order of the polymer film near the polymer-insulator interface. This assumption of structural order was supported by the UV absorption spectra.

With reports of the mobility of regioregular P3HT FETs improved up to 0.1 cm$^2$V$^{-1}$s$^{-1}$ with ON/OFF ratios greater than 10$^6$, which is comparable to inorganic amorphous Si TFTs, the fabrication of a monolithically integrated optoelectronic circuits was accomplished using P3HT FETs as a current supply for poly[2-methoxy-5-(2’-ethyl-hexyloxy)-p-phenylene-vinylene] (MEH-PPV) LEDs on the same substrate by Sirringhaus et al. [63]. The integrated active pixel clearly demonstrated that PFETs have sufficient driving power to switch PLEDs of similar sizes. The process of P3HT FETs was optimized by reducing unintentional doping and promoting self-organization to improve the ON-OFF ratio and the mobility. The conductivity of P3HT films increases drastically upon exposure to air, but a layer of thermally deposited SiO$_x$ (x < 2) on the polymer film surface restores the low conductivity. The mobility was improved in FETs.
whose SiO$_2$ surface was treated with the silylating agent hexamethyldisilazane (HMDS) before P3HT deposition. It was believed that HMDS promoted phase segregation of the polymer at the interface by replacing the natural hydroxyl groups on the SiO$_2$ surface with apolar methyl groups. A flat surface was also advantageous for P3HT self-organization compared to a substrate with prefabricated source-drain contacts. X-ray diffraction showed local scale ordering of regioregular P3HT with a lamellar phase-segregated structure. As sketched in Fig. 2.29, the P3HT film has alternating layers of conjugated backbones with interdigitated side chains parallel to the substrate. The relatively long conjugation lengths along P3HT chains and $\pi$-$\pi$ stacking of adjacent chains were believed to account for the formation of local ordering.

![Figure 2.29 The lamellar structure of the regioregular P3HT on SiO$_2$ substrate (Adopted from Ref.[63]).](image)

A schematic of the integrated pixel with a P3HT FET driving an MEH-PPV LED is shown in Fig. 2.30. The integrated circuit was vertically layered. On top of the source-drain contacts of the P3HT FET, SiO$_x$ was thermally evaporated through a mechanically
aligned shadow mask to define the active LED area. The Au drain electrode for the FET acts also as the hole-injection anode of the LED. The light emitting polymer MEH-PPV was spin-coated and the device was completed by evaporating a semitransparent Ca-Ag cathode [63-64].

Later work on P3HT FETs by the same research group [64] improved the ON-OFF ratio further to the order of $10^8$ measured between turn-on voltage (about 2.5 V) and $V_g = -70$ V. Sirringhaus et al. [64] again pointed out that the alkyl group provided by the HMDS treatment changed the hydrophilic surface of natural SiO$_2$ and thus attracted the hexyl chains of the P3HT towards the interface. The SiO$_x$ was thought to passivate the active dopants in P3HT or attract mobile dopants out of the bulk of the film because it is a

Figure 2.30 Cross section of the integrated P3HT FET and MEH-PPV LED (Adopted from Ref.[63]).
reducing agent. A similar improvement was obtained by immersing the as-deposited FETs into a strong reducing agent of hydrazine. Dedoping of P3HT by the reducing effect was directly observed by photothermal deflection spectroscopy. One interesting comment on the integrated optoelectronic pixel was that the integration succeeded using underlying spin-coated PFETs, but failed with buried FETs based on vacuum sublimated oligomers. The subsequent deposition of PLEDs degraded the oligomer FETs, but P3HT FETs were robust enough to resist the degradation caused by the subsequent deposition of light-emitting polymers in different solvents.

2.6 Gate dielectric materials for OFETs operating at low voltages

The most important parameters to describe the performance of PFETs are carrier mobility, on/off ratio, and the operational voltage range. As briefed in Section 2.5, elevating the mobility attracted tremendous attention over the last two decades and was the dominant topic for most PFET studies. The on/off ratio was also improved and now rivals Si TFTs. PFET operational voltages, however, often reach as high as 40 to 100 V, which is too high for practical usage. To reduce PFET driving voltages while maintaining a usable current level, a high gate capacitance is required. The current flowing in PFETs is proportional to the number of field-induced carriers per unit area in the channel, while the number of carriers in the channel is proportional to the capacitance of the gate dielectric. A high gate capacitance can be achieved by using materials with a high dielectric constant, or by shrinking the gate dielectric thickness. High dielectric constant insulators explored in OFETs are typically inorganic metal oxides, which are common to the Si CMOS industry. However, these materials are rigid and often incompatible with
flexible substrates. Gate insulators as thin as a few nanometers can be realized using self-assembled monolayer (SAM) of silane-based molecular dielectrics formed directly on surfaces containing hydroxyl (OH) groups.

The following is a summary of various studies on OFETs operating at low voltages either by using high dielectric constant insulators or reducing the thickness of the gate insulator.

2.6.1 High-dielectric constant gate insulators

Inorganic metal oxides such as barium zirconate titanate (BZT), tantalum pentoxide (Ta$_2$O$_5$), and SrBi$_2$Ta$_2$O$_9$ (SBT), with very high dielectric constants were used in OFETs to reduce their operational voltages. The output current of these FETs with high dielectric constant gate dielectrics reached a few microamps at driving voltages less than 10 V, while the $I_{DS}$-$V_{DS}$ curves exhibited sufficient saturation.

Pentacene FETs using a BZT gate insulator by Dimitrakopoulos et al. [65] demonstrated low operating voltages. Pentacene FETs with a BZT gate dielectric were fabricated to investigate whether it was a concentration of accumulated carriers in the channel region (N) or the gate field (E) contributing to the dependence of mobility on gate bias. The question was raised from the observation that in pentacene FETs on Si/SiO$_2$ substrate, the mobility was higher in OFETs with thinner SiO$_2$ gate insulators. Both N and E are substantially higher in devices with reduced insulator thickness. Since N depends on both gate dielectric constant and its thickness, while E depends only on the thickness, the effects of these two parameters can be separated. By keeping the thickness of the gate insulators comparable, a higher mobility should be achieved with devices
incorporating a higher dielectric constant than in FETs with SiO$_2$. This experimental design essentially kept the gate field the same in the two FETs with only the dielectric constant varied. The metal oxide film BZT was used in the comparison device as the gate insulator with a high dielectric constant of 17.3. It was deposited by radio frequency magnetron sputtering from a sintered powder target in an Ar/O$_2$ gas mixture at room temperature. Test results proved that higher mobilities were achieved at lower operating voltages in devices with a BZT gate dielectric. Therefore, a higher concentration of the charge carriers accumulated in the channel was identified to be responsible for the gate-voltage-dependence of mobility in pentacene FETs. Based on this conclusion, Dimitrakapoulos et al. [65] thought that the multiple trapping and release model was the mechanism to explain the gate-voltage-dependence of mobility. The multiple trapping and release model assumes that a large concentration of localized states exists in the forbidden gap, which can inject trapped holes by releasing them at a rate dependent upon the thermal energy. The initial linear increase of mobility with gate voltage indicates that most of the injected holes are trapped in the localized states at low biases. At a sufficiently high bias, all of the trap states are now filled and the mobility saturates above this gate bias as a consequence of the traps not participating. Any subsequently injected carriers are free to move in the channel with a saturated mobility. Higher dielectric constant insulators allow the traps to be filled at much lower gate voltages, which explains the higher mobility observed in BZT based devices at low voltages compared with SiO$_2$ based devices.

Tantalum pentoxide (Ta$_2$O$_5$) has also attracted a lot of attention as an insulating material due to its high dielectric constant in the range of 20 to 35 [66]. It attracted a lot
of attention for research with Si based MOSFETs, and was studied by Bartic et al. [66] with P3HT FETs. Top-gate and bottom-gate P3HT FETs were fabricated, with the Ta$_2$O$_5$ e-beam evaporated for both configurations. In the top-gate structure, Ta$_2$O$_5$ was evaporated directly on the P3HT film and proved that P3HT film could withstand the hot evaporation of a high melting temperature dielectric layer. The e-beam evaporated Ta$_2$O$_5$ films exhibited a breakdown strength exceeding 1 MV/cm, with a gate leakage of $10^{-8}$ A/cm$^2$ for bottom-gate devices and $10^{-7}$ A/cm$^2$ for top-gate devices. Both top-gate and bottom-gate FETs with Ta$_2$O$_5$ had operational voltages lower than 3 V. The low operating voltage was attributed to the high dielectric constant of Ta$_2$O$_5$, which induced a high charge density at much lower voltages compared to a SiO$_2$ gate dielectric. It was observed that top-gate devices had a more severe leakage in their output current than bottom-gate devices. The high leakage current in top-gate devices was due to the oxygen doping of the P3HT film during the evaporation of Ta$_2$O$_5$ and led to a poor on/off current ratios. The source of the oxygen could be outgassing from the Ta$_2$O$_5$ target during the dielectric deposition.

The high dielectric constant SrBi$_2$Ta$_2$O$_9$ (SBT) was also tested as a gate dielectric in P3HT FETs by Han et al. [67] operating at low voltages of about 10 V. The dielectric constant of SBT was determined to be about 50 from capacitance-voltage measurements. High-quality SBT films were prepared on a Si substrate with a thin underlying silicon nitride (SiN) buffer layer (Fig. 2.31). The SiN buffer layer grown directly on a Si wafer before SBT deposition was kept sufficiently thin so that it would not cause a significant voltage drop across itself. The SBT film was spin-coated atop the SiN buffer from a presynthesized solution, followed by annealing at 900$^\circ$C for an hour. The SBT based
P3HT FETs had a fair mobility of $7.47 \times 10^{-3}$ cm$^2$/Vs, but a very good on/off ratio as high as $10^4$ with a gate bias sweep of only -4 V to 4 V. The strong gate effect in P3HT devices using a SBT gate insulator was the result of the high gate dielectric capacitance provided by the high dielectric constant of SBT films.

Figure 2.31 Schematic diagram of the polymer field effect transistor with high-dielectric SBT films as the gate dielectric (Adopted from Ref. [67]).

Using the high dielectric constant insulator TiO$_2$ in P3HT FETs, Wang et al. showed devices which operate at low drive voltages of -5 V or less [68]. TiO$_2$ films formed by a pulsed dc linear scanning magnetron physical vapor deposition process have a dielectric constant of about 41. Since the output current of a FET is proportional to the
product of the number of carriers per unit area in the channel (N) times the carrier mobility (μ), where N depends linearly on the dielectric constant of the gate insulator, the use of high dielectric constant materials can partially compensate for the relatively low mobility of polymer semiconductors. The ON/OFF ratio in TiO$_2$ based P3HT FETs was limited by the relatively large gate leakage current through the TiO$_2$ gate dielectric. To reduce the leakage current through the gate insulator, a thin layer of SiO$_2$ was added on top of the TiO$_2$ by plasma enhanced chemical vapor deposition (PECVD) to improve the device performance (Fig. 2.32).

Figure 2.32 Schematic diagrams of the FET configuration (a) with and (b) without the SiO$_2$ overlayer on the high dielectric constant gate insulator (Adopted from Ref. [68]).
The SiO$_2$ overlayer smoothed out the surface of the gate dielectric and resulted in a significantly improved mobility and ON/OFF ratio even though the effective dielectric constant of the gate dielectric was lowered due to the weighted average with a relatively low SiO$_2$ dielectric constant. The hysteresis observed earlier in the $I_{DS}$ vs $V_{GS}$ scans was also reduced with the addition of a thin SiO$_2$ passivation layer. A rough surface of TiO$_2$ can cause strong variations in the formation of carrier traps, which is the origin of the hysteresis in drain current during gate voltage sweep. It takes a longer time for trapped carriers to follow the bias voltage and escape from the traps, so there is a “memory” effect during gate voltage sweeps which appears as a hysteretic behavior in the output current. The density of traps is significantly lower on a smoother SiO$_2$ surface, which explains the reduced magnitude of hysteresis in the bilayer SiO$_2$/TiO$_2$ gate dielectric structure.

2.6.2 SAM gate dielectrics

It was demonstrated by Collet et al. that a thin layer of densely packed self-assembled monolayer (SAM) of alkyltrichlorosilanes as the gate insulator can efficiently reduce the operating voltage of organic FETs [69]. A SAM insulator with a thickness of only about 2 nm was tested using sexithiophene (6T) FETs. The saturation current of these sexithiophene FETs reached as high as 8 nA with a driving voltage of 2 V. The formation of the SAM gate insulator started with the precursor SAM tetradecylenyltrichlorosilane (TETS) SiCl$_3$-(CH$_2$)$_n$CH=CH$_2$. The vinyl endgroups (-CH=CH$_2$) were oxidized into carboxylic endgroups (-COOH) in an aqueous solution of KMnO$_4$/NaIO$_4$/K$_2$CO$_3$. It was necessary to transform the vinyl endgroups into carboxylic
endgroups for the subsequent patterning process of the 6T film. The 6T FETs with this 2 nm SAM insulator had a gate leakage current density lower than $10^{-6}$ A/cm$^2$, but the leakage current density measured without a 6T film deposited atop was much lower, ranging about $10^{-8}$ to $10^{-7}$ A/cm$^2$.

Later work by Halik et al. [70] proposed an explanation for the increase of the leakage current through the SAM insulator upon the deposition of the organic semiconductor. They suggested that the higher leakage was due to the reduced effective thickness of the SAM dielectric caused by the partial penetration of the subsequently deposited organic semiconductor molecules into the SAM. Alkyltrichlorosilane was then specifically synthesized with an aromatic endgroup, (18- phenoxyoctadecyl)trichlorosilane (PhO-OTS) (Fig. 2.33), to resist the molecular penetration from the contacting organic semiconductor layer. Compared to other alkyltrichlorosilanes with linear endgroups, the SAM of PhO-OTS should have a more closely packed surface because the $\pi$-$\pi$ interaction between the phenoxy endgroups of adjacent molecules will create an intermolecular top-link. The PhO-OTS SAM formed on hydroxylized Si surface had a thickness of about 2.5 nm and a dielectric constant of 2.5. Pentacene FETs using the PhO-OTS SAM insulator had an output current of 1 $\mu$A at a 2.5 V driving voltage. The gate leakage current density was as low as $10^{-9}$ A/cm$^2$ at 1 V gate bias and the breakdown field of the PhO-OTS SAM was about 14 MV/cm, comparable to that of SiO$_2$ with a similar thickness. This work again proved that the operating voltage and power dissipation of organic devices can be dramatically reduced by exploiting thin gate dielectrics with very thin thicknesses.
Figure 2.33 Chemical structures of organic materials and cross-section of a TFT with molecular SAM gate dielectric: (a) Structure of PhO-OTS; (b) Structure of pentacene; and (c) Cross-section of a pentacene TFT with SAM dielectric and source/drain contact deposited through a shadow mask (Adapted from Ref. [70]).

2.6.3 Hydroscopic gate insulator

Sandberg et al. [71] reported on the low voltage operation of P3HT FETs using a dielectric material, which can neither be categorized as a high dielectric constant nor be described as a small thickness. This study used a hydroscopic insulator polyvinylphenol (PVP) in P3HT FETs and these hydroscopic insulator field-effect transistors (HIFETs) could take advantage of moisture in the air to show superior gate modulation in the presence of moisture than in N<sub>2</sub> atmosphere. This phenomenon was thought to be due to an enhancement of the gate field by an ionic process in the moisturized gate dielectric. This discovery widened the scope of searching for methods to reduce the operational voltage of PFETs, but its generality has yet to be proved.
2.7 Applications of PFETs

2.7.1 Flexible electronics and displays

PFETs are ideal candidates for large area flexible electronics because of their low temperature processing and full compatibility with plastic substrates. Their solution processibility could be incorporated into high-speed roll-to-roll processes widely used in the plastics industry. Applications of PFETs in flat-panel displays gathered great interest over the last decade. FETs based on vacuum-deposited oligomers [72-95] are strong competitors of PFETs, but the solution processed films for PFETs are favored for their low cost processing. Researchers are making great progress in many aspects of PFETs towards the final goal of their commercialization. Charge injection can be improved by engineering the HOMO and LUMO levels of polymer semiconductors by chemical synthesis to better match the metal work functions [96]. The effects of various solvents and film formation methods on the performance of PFETs were investigated [97]. PFETs of new configurations, such as vertical-channel structure devices, were also explored by Stutzmann et al. [98]. The stability and lifetime of PFETs in ambient air conditions are now beginning to be tested [99-100]. Novel sub-micrometer PFETs were fabricated using photolithographic techniques [101-102]. The output current of these small feature-sized devices reached the order of micro-amps at operating voltages of less than 5 V. The patterning techniques developed to date for PFETs and polymer ICs fabrication include inkjet printing [103-104], pad printing [105], carbon-plot [106], line patterning [107-108] and reactive ion etching [109]. PFETs have been developed on plastic substrates by Lee et al. [110] as a pre-test for flexible display applications. Finally, the demonstration of
active-matrix displays driven by solution processed PFETs took us one step closer towards polymer displays [111].

2.7.2 PFET sensors

One area researchers have put more efforts into recently is sensors based on PFETs. PFETs have been implemented as light sensors, chemical sensors, and even biosensors.

2.7.2.1 Light sensors

PFET light sensors were first reported in 2001 by Narayan and Kumar [112]. It was first reported that the behavior of poly(3-octylthiophene-2,5-diyl) (P3OT) FETs was modified upon photoexcitation with a large increase in the output current depending on the intensity of light. Polymer FETs are ideal for low-light level optical detection by nature of their high optoelectronic responses [112-113]. As in most polymer semiconductors, hole transport is favored in P3OT while electron transport is hindered. Therefore the spatial separation of photo-generated electron-hole pairs is enhanced due to the unipolar transport of charge carriers across the polymer semiconductor to yield large changes in the drain current. Electron-hole pairs are generated in the channel region, as well as in the bulk upon illumination. Under negative gate bias, the holes from the bulk drift towards the channel, while the electrons are repelled away from the channel or remain in the bulk. Thus, a vertical spatial electron-hole separation forms which biases the channel for a larger drain current. The decay of photoinduced carriers can be described as a fast initial recombination process (in seconds) followed by a second slow-
relaxation process (in hours) upon switching the photoexcitation off. The slower process is due to the spatial separation of the photogenerated negative and positive carriers.

A study of F8T2 phototransistors by Hamilton et al. [114] observed that the drain current in the off-state was significantly increased by several orders of magnitude under illumination, but the effect of illumination was milder in the strong accumulation region. The smaller effect of illumination on the drain current can be explained by the overwhelming effect of the gate voltage on the concentration of accumulated carriers in the channel. The off-state drain current showed a strong dependence on the level of illumination. The threshold voltage of the devices was reduced with the contribution of trapped photogenerated electrons in positively charged states. The unaffected field-effect mobility in these phototransistors indicated that the electronic structure of the polymer semiconductor was not affected by the illumination. It was also speculated from the unaffected mobility that the illumination induced negligible temperature change in the device, otherwise a temperature increase would result in higher mobility in conjugated polymer semiconductors. The subthreshold swing was similar regardless of whether the device was in darkness or illuminated, so the density of states in the polymer must not have been significantly changed by the illumination either.

2.7.2.2 Gas sensors

It was suggested as early as 1988 by Assadi et al. [42] that organic field effect transistors can be used as gas sensors by taking advantage of the chemical modification in the organic semiconductor layer. The conductivity of \( \pi \)-conjugated polymer films can be interrupted by exposing them to gases. Later the correlation between the morphology and
the vapor responses was investigated, and the role side-chains play was explored [115-118]. Organic vapor sensors based on alkoxy-substituted polyterthiophenes were also presented [117-118]. The sensitivities of these PFET gas sensors reached the part per million (ppm) range.

The basic structure of a gas sensor based on OFETs is a regular PFET configuration with bottom gate and top source/drain electrodes. The organic semiconductor functions simultaneously as both transistor channel material and vapor-sensing layer during exposure to the atmosphere being analyzed. The source-drain current is measured to evaluate the sensor response. Gas sensors based on PFETs operate by the mechanism that the conductivity of the organic semiconductor changes in the presence of the analytes due to chemical degradation.

Though intended to study the stability of P3HT PFETs in ammonia gas, the decrease in current upon exposure to ammonia exhibited P3HT FETs were sensitive to ammonia gas and this property could be exploited for applications as gas sensors [42]. The output current was measured every 10 min during ammonia exposure to characterize the deterioration of the P3HT. To serve as control data, the same measurement was also performed in the media without ammonia gas. The effect of gaseous ammonia on P3HT was shown by the decrease in conductivity of the P3HT film. The process is reversible for short exposure periods to NH₃, but became irreversible after a certain threshold exposure time. For a total exposure time of less than 20 min, the conductivity decrease was reversible. The mobility of the device could return to its original value when it was removed from the gas for 10 min. For exposure periods longer than 20 min, the process became irreversible. If the exposure time exceeded 100 min, the mobility would drop two
to three orders of magnitude. It was found that the decrease in mobility was of the same order as the corresponding decrease in conductivity. This observation indicated that the changes in output current should be attributed to the mobility variations rather than variations in doping concentration. Though no detailed analysis was presented in this study, the output current drop in the presence of an analyte gas was explained based on the assumption that the mobility decrease was related to the hopping conditions for charge transfer between polymer chains. A later report by Torsi et al. [115] on gas sensors based on substituents of polythiophene provided the explanation that in polycrystalline organic semiconductor films, the mass up-take due to physi-sorption at the grains led to an enhancement of the barriers between the grains, which in turn caused the current intensity to decrease.

The effect of polycrystalline grain boundaries was demonstrated from the magnitude of the response in polymer semiconductor films with different grain sizes [115-118]. The polycrystalline morphology of the active layer may be a disadvantage for high-mobility PFET application, but it is ideal for sensing applications. The experimental observation suggested smaller grain size and larger porosity increases sensor response. This observation implied that the response of the OFET sensors to alcohols depends on interaction at grain boundaries, which may supply a passage for alcohol vapors to penetrate the thin film and bind near the channel. Further investigations suggested that for sensor applications alkoxy substituted polythiophenes are superior to alkyl substituted polythiophenes [117-118], even though it is preferable the other way for high mobility OFETs. Compared to alkyl-substituted regioregular polythiophenes, alkoxy-substituted polyterthiophenes have smaller polycrystalline grains with more grain boundaries.
It was discovered that the side-chains play an important role in gas sensing. The change in device current of a series of polycrystalline PFETs exposed to several primary alcohols showed that the degree of response increases with the length of the semiconductor hydrocarbon end groups. The responses of the alkyl-substituted functionalized poly-(3,3’-didodecyl-2,2’:5’,2’’-terthiophene) (Poly-DDT) (Fig. 2.34) regioregular thin films increased linearly with the length of the alkyl chain-bearing analytes. However, the correlation with the alkyl chain length was not seen for alkoxy-substituted poly(3,3’’-dipentoxy-2,2’:5’,2’’-terthiophene) (Poly-DPOT) (Fig. 2.34). The responses of Poly-DPOT showed a linear correlation with the analytes’ associated dipole moment. On the other hand, no clear trend was observed for the responses of Poly-DDT to the analyte dipole moment. These results could be explained by the fact that the alkoxy chain enhanced the dipole moments associated with Poly-DPOT. More evidence to support the explanation is that only Poly-DPOT responded to ethanol when both Poly-DT and Poly-DPOT were exposed to 1-hexanol and ethanol atmospheres. Since Poly-DPOT bears a much stronger dipole moment than Poly-DDT, polar-type interactions dominate in Poly-DPOT sensors making them more sensitive to polar substances, whereas dispersion-type interactions prevail in Poly-DT devices. Therefore, Poly-DPOT could detect the shorter and more polar molecules such as ethanol, but Poly-DT is completely insensitive to ethanol. At the same time, Poly-DPOT can sense hexanol because it has a quite long linear alkyl chain, which interacts with the long chain alcohols. It was also shown that the magnitude of the response was gate bias dependent in that with a lower gate bias, resulting in a smaller response. This gate modulated response envisaged such devices as sensing switches.
2.7.2.3 Biosensors

Other than gas sensors, PFETs also functioned as bio-chemical sensors in aqueous solutions, such as glucose sensors using PEDOT:PSS FETs [119] or P3HT FETs [120-121]. The plastic-substrate-compatibility and bio-compatibility of organic semiconductors may lead to low cost single-use and disposable biosensors for health related applications based on OFETs fabricated with a very simple technological process.
Based on the previous studies, it seems that the conductivity in PFET gas sensors is changed due to an alteration in charge transport in the presence of analytes. The OFET sensors for aqueous analytes introduced in this section, though, respond to the change of the conductivity caused by the variation of charge concentration in the organic semiconductor films.

For applications of detecting analytes in aqueous solutions, modifications were performed to the structure of PFETs to suit the application in aqueous solutions. The polymer semiconductor film was either directly in contact with the analyte solution [119] or isolated from the solution by a gate insulator film [120-121]. The device configuration of a PEDOT:PSS sensor is shown in Fig. 2.35 [119].

![Figure 2.35 The test setup of a PEDOT:PSS glucose sensor (Adopted from Ref.[119]).](image)
In this sensor structure, the test solution is in direct contact with the conductive polymer PEDOT:PSS. A phosphate buffer saline (PBS) solution with a pH of 7.14 was confined by a well formed of an elastomeric material called poly(dimethyl siloxane) (PDMS) on top of the PEDOT:PSS film. Biases were applied to both the PEDOT:PSS and PBS and current through the PEDOT:PSS at a certain bias was monitored to trace the appearance of glucose. The bias to the PBS was provided by a Pt wire electrode immersed in the PBS.

In contrast to PEDOT:PSS sensors, P3HT glucose sensors put the sensitive area and the electrical contacts on opposite sides of the supporting substrate [120-121]. The organic semiconductor layer was protected from the aqueous solution by encapsulation in epoxy. The measurement set-up is shown in Fig. 2.36. The PFET structure in this study is different from the traditional PFETs where its metallic gate is omitted for the purpose to provide an exposure pathway to the analyte sensitive gate dielectric silicon nitride directly to the test solution. The sensing device was immersed in a volume of analyte solution during the measurement. The electrochemical potential developed at the solution/dielectric interface modulates the current flow in the transistor. To reduce the operational voltage for OFETs and improve the pH sensitivity, insulators with high dielectric constant such as Ta$_2$O$_5$ need to used as the gate dielectric [121].

The sensing capability of PEDOT:PSS FETs to glucose was demonstrated by Zhu et al. [119]. The output current of the device changed dramatically when both glucose and an enzyme were present in the buffer solution. Since the modulation of output current was measured in PBS, it ruled out the possibility that the pH in the solution was the reason of the sensor response to glucose. Instead, it was found that H$_2$O$_2$ is generated
during the reaction of glucose with the enzyme, which is then oxidized at the Pt electrode.

Figure 2.36 (a) Schematic representation of the device structure; (b) The measurement setup of a pH sensor in glucose solution (Adopted from Ref [121]).

The oxidation of $\text{H}_2\text{O}_2$ either caused the reduction of pre-existing PEDOT$^+$ (due to PSS doping) in the film to maintain the charge balance in the analyte solution, or led to a redistribution of the potential at the PBS/PEDOT:PSS interface. In either case, the conductivity of the polymer film decreased and was reflected in the lower output current.
of the PEDOT:PSS FETs. It was shown that the change in current responded even at concentrations as low as 0.1 mM of glucose, but reaches saturation above 1 mM. However, these values were subject to change depending on parameters such as the amount of enzyme and the thickness of the PEDOT:PSS film, and the reproducibility of the sensing results are not reported. The gating effect in this glucose sensor was implemented by applying a voltage to the Pt electrode. The modulation of the gate voltage was shown to increase the sensing response with a more positive voltage at the electrode.

Unlike the PEDOT:PSS glucose sensors, the sensing response of P3HT FETs was induced due to the pH change caused by the reaction of glucose with an enzyme named glucose oxidase. The decrease of the drain current of P3HT FETs reflected the formation of gluconic acid due to the glucose-enzyme reaction when the glucose is added to the test solution. Since the drain current increases with a pH for P3HT sensors, the increased acid concentration in the test solution caused a current lowering. The pH change was detected at the proton sensitive gate dielectric, which is usually an oxide or a nitride possessing proton binding sites on their surfaces [120-121]. The potential drop at the solution/dielectric interface was controlled by the protonation/deprotonation process at the surface of the gate dielectric. This pH-dependent potential determined the concentration of accumulated charge in the P3HT film and consequently the output current of the P3HT FETs. pH sensors using silicon nitride were demonstrated, but it required operating voltages up to 10 V. Once the gate dielectric was replaced by the high dielectric constant insulator Ta$_2$O$_5$, the operating voltage dropped to as low as 1 V. The
pH response of these sensors is reversible after successive immersions in buffer solutions with different pH value, but their reproducibility in glucose solution was not reported.

2.7.3 Other applications

Other possible niche applications based on the flexibility of polymer electronics include packaging, luggage tags, smart labels, and computerized clothing. The long history of polymers, the wide variety of material choices, and the maturity of polymer manufacturing will facilitate the future commercialization of polymer electronics based on PFETs.
CHAPTER 3

RADIO FREQUENCY (RF) PULSED PLASMA
POLYMERIZED (PPP) DIELECTRIC FILMS

3.1 Motivation for exploring PPP dielectric films

Polymer electronics are gaining considerable attention, but more effort is needed to reach a satisfactory solution for an all-polymer field effect transistor (FET). Replacing the traditional silicon dioxide gate dielectric with a suitable polymer dielectric would enable flexible electronics and displays.

Synergistically, the Si CMOS community is also seeking both alternative high dielectric gate insulators to replace the traditional thermally grown SiO$_2$ as well as, new low dielectric constant materials for interconnect technology. Thermally grown SiO$_2$ and nitrided SiO$_2$ has been the most popular gate dielectric for Si metal-oxide-semiconductor FETs (MOSFET), but it cannot satisfy the long term needs as MOSFET critical dimensions shrink below the 130 nm node. Substitute dielectrics are needed to relax the gate dielectric thickness (high permittivity) and to reduce the parasitic capacitive coupling overlap created by multiple interconnect levels (low permittivity).

Polymer FETs (PFET) have been available for more than ten years, and most work on PFETs has focused on polymer semiconductors for the active component, often
neglecting the gate dielectric material. These prior PFET investigations often adopted SiO$_2$ as the gate insulator due to its maturity and convenience. However, to reflect the most attractive advantage of polymeric devices, the ultimate aim is to find a flexible gate insulator. Unfortunately, most effort towards alternative gate dielectrics has been driven by the Si CMOS community and focuses on advanced inorganic gate dielectrics using high-permittivity materials. These materials include Al$_2$O$_3$, Ta$_2$O$_5$, HfO$_2$, ZrO$_2$, Zr silicate, and Hf silicate [122-124]. It is clear that, whereas these high-k dielectrics may be suitable for Si CMOS applications, in view of their rigidity they are unsuitable for flexible devices.

Polymeric gate dielectrics are a natural choice for the flexible insulators. A few groups reported results on PFETs using polymer insulators. Garnier et al. used a sheet of commercially available polyester film polyethylene terephthalate. The film was 1.5 µm thick, and its flatness was achieved by fixing it to a frame. This method is inspiring for an all-polymer PFET, though its reliability needs to be improved [125]. Drury et al., Sirringhaus et al., and Kawase et al. all used spin-coated polyvinylphenol (PVP) from either isopropanol or isopropanol:xylene solutions as the gate dielectric [126-127]. Narayan et al. used polyvinyl alcohol (PVA) cast from an aqueous solution [112]. Solution processed polymer insulators have obtained reasonable and controllable thicknesses for very large PFETs, but it will be challenging to achieve the ultra-thin thickness and uniformity for scaled PFETs.

Attention must also be paid to the possible intermixing of polymer dielectrics and polymer semiconductors that are solution based. It is quite possible that these two polymers would dissolve each other when deposited as an overlayer. Also, the type and
amount of impurities contained in solution are difficult to control, so it is hard to predict what charges and traps will exist at/near the PFET insulator/semiconductor interface. This brings another concern to PFET performance. To produce repeatable and predictable PFETs, detailed information on the gate insulator is necessary. High homogeneity and good dielectric properties are essential in obtaining high performance devices. However, to date, no electrical characterization of the polymer insulator or interface has been cited except its overall thickness.

Plasma processing in general, and plasma polymerization in particular, has gained increasing interest for its ability to engineer compositions of thin film materials in one relatively simple step. A wide variety of monomers are available as precursors, and the composition and structure of the deposited polymer layer can be tailored by adjusting the plasma deposition parameters, such as input power, discharge pressure, composition of the gas feeds, and the deposition temperature [128-129]. A comprehensive introduction to all major aspects of plasma polymerizations has been provided by Yasuda [130]. In the present studies, an RF powdered plasma discharge, operated at a frequency of 13.56 MHz, was employed. Metal electrodes, located externally to the glass reactor to avoid metal atom contamination of the polymeric films, were used to deliver the RF power. A pulsed plasma discharge was employed in lieu of the more conventional continuous-wave operational mode. The pulsed mode was employed to provide enhanced control of film chemistry during the deposition process [131].

Dielectric constant and breakdown electric field are the two most important electrical parameters for characterizing a dielectric material. Dielectric constants are determined from the measured capacitance data and known device dimensions. Leakage
current measurements indicate the electrical integrity of the insulator. This information can be used to compute the breakdown electric field provided the insulator thickness is known. Since the insulator in the MIS structure essentially blocks the dc current flow between the two electrode plates (except small leakage currents), the major diagnostic technique to characterize MIS capacitors is C-V analysis. During a C-V measurement, both a dc voltage and an ac signal are necessary for the C-V measurement. A dc voltage is applied to the device to determine the base bias condition. A small-signal ac voltage is superimposed on the base bias and its modulation gives rise to the variation in measured charges by modifying the semiconductor depletion layer. The charge variation results in a detectable capacitance [132].

In the course of exploring a new material as gate insulator, capacitance characterization is of practical importance and C-V characterization has typically been monitored. Measured C-V data and parameters extracted from the new polymer MIS structure are presented and compared to those of traditional Si MOS. As discussed below, these parameters provide quantitative measures of the advantages and disadvantages of these new materials or techniques under consideration. Note that the polymer MIS structure is built on a traditional Si wafer so that the channel occurs at the Si surface. This will facilitate comparison to known Si MOS structures by substituting only the dielectric. The measured data can also be compared with the theoretical data to identify deviations from the ideal in both the insulator and the semiconductor.

The application of C-V characterization has already been extended into PFET research. Scheinert et al [133] inspected the C-V characteristic of arylamino-PPV MIS capacitors to study the field effect in organic devices. In accumulation, the insulator
capacitance is only found for low frequencies. At positive gate voltages, PFET inversion has not been observed. The low mobility causes a high relaxation time. The measured characteristics show a large hysteresis for different sweep directions and a shift of the curves for repeated measurements. This work shows that C-V characterization can be of great help to demonstrate the field effect in PFETs.

The main reason to look for a polymer replacement for SiO\textsubscript{2} in polymer devices is because of its rigidity, which contradicts the desired flexibility for PFETs. Plasma polymerization has gained large attention in new material development and treatment, but it is still new in the field of microelectronics study. Since it can be employed to deposit films on large substrates, the plasma polymer approach should be favorable towards large area polymer circuitry as long as the electrical properties of these films satisfy the requirements of gate insulators. This study presents recent progress made using RF (radio frequency) pulsed-plasma polymerization (PPP) to create suitable gate dielectrics. Capacitance-voltage (C-V) and current-voltage (I-V) measurements were employed to characterize the RF pulsed-plasma deposited dielectric films.

3.2 PPP allylamine dielectric films

3.2.1 Fabrication and test of capacitors using PPP allylamine dielectric films

This work explores this possibility by evaluation of pulsed RF plasma deposited polyallylamine insulator films via detailed C-V and I-V characterizations. Two types of polyallylamine films deposited on Si wafers by radio-frequency (RF) pulsed plasma polymerization were employed as the dielectric in a metal-polyallylamine-Si metal-insulator-semiconductor (MIS) structure. All insulator film thickness employed were
approximately 2000 Å. They were deposited with the same monomer but under two different reactor conditions. Samples PA1 were deposited at room temperature, while samples PA2 underwent an *in-situ* heat treatment at 100 °C during deposition.

A fairly detailed general description of the pulsed plasma polymerization technique has been presented previously [134]. However, a significant modification in the present study was the use of a bell-shaped reactor in lieu of the cylindrical reactors employed previously.

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**Figure 3.1** A schematic of the plasma reactor system and associated electronic components used in this study.
The bell-shaped reactor, located inside a temperature controlled oven enclosure, provided more uniform film thickness on the silicon substrates. A wire mesh, symmetrically placed around the top of the bell-jar, served as the ground electrode. A metal plate, located under the bottom glass plate of the reactor served as the hot electrode. Figure 3.1 provides an illustration of the reaction system plus associated electrical components employed in this study. Further details on the operation of this system have been provided by Sanchez-Estrada [135]. Pulsed plasma deposition provides better control over the quality of the deposited films. During plasma on periods, reactive species are generated from the monomer. These reactive species settle on substrate and form a low damage film during plasma off periods.

In the present work, plasma on and off times of 3 and 10 ms, respectively, were employed during polymerization of the allylamine monomer. A peak power input of 36 W was employed during the plasma on periods. The monomer was introduced at a flow rate of 3.5 cm³(STP)/min and the reactor pressure was adjusted to 190 mTorr. After deposition of the PPP film, MIS capacitors were fashioned by evaporating metal contacts through a wire mesh to define 180×170 μm² Ti/Au rectangles (Fig. 3.2). Backside electrical contacts were made by e-beam evaporation of Ti/Au onto the back of the Si wafer. The specified resistivity for the Si substrate from the manufacturer was 1-10 Ω-cm. By checking known data of resistivity vs. n-type doping concentration for uniformly doped silicon wafers, the doping concentration of the substrate should be between 4×10¹⁴ and 4×10¹⁵ cm⁻³. The Ti/Au metal thickness was 150 Å /1000 Å. Ti adheres to Si better than Au, so a thin Ti layer is added to promote adhesion.
Figure 3.2 (a) A photomicrograph of the Ti/Au quadrangles evaporated atop the PPP film; and (b) a side view of the entire PPP allylamine MIS capacitors used in this study.
Capacitance and conductance measurements have been carried out with an Agilent 4284A LCR meter coupled with MDC (Material Development Corporation) CSM/Win analysis software [136]. A family of C-V curves were measured at five different frequencies between 100 Hz and 1 MHz. Leakage current (I-V) curves were measured with an Agilent 4156 parameter analyzer. Measurements were performed under ambient room light.

3.2.2 The effect of *in-situ* heating on the dielectric constant of PPP allylamine

Figure 3.3 shows C-V responses for PA1 and PA2. For both PA1 and PA2, the capacitance tends to shift to higher values when decreasing the ac voltage frequency. The phenomenon of higher accumulation capacitance at lower ac frequency had also been reported in other polymers. It was stated in Simpson *et al.* [137] that the variation in dielectric constant is attributed to the frequency dependence of the polarizable units in a polymer to orient quickly enough with respect to the applied ac signal.

The dielectric constants determined from measured C-V characteristics at 1 MHz were 3.03 for PA1 and 3.55 for PA2. Sample PA2, which was deposited with an *in-situ* heat treatment, exhibited a higher dielectric constant, presumably due to densification of the film. The dielectric constant is calculated based on the capacitance formula for a parallel plate capacitor,

$$k_i = \frac{Ct}{\varepsilon_0 A}, \quad (3.1)$$
where $k_i$ is the relative dielectric constant of the insulator, $\varepsilon_0$ is the permittivity of vacuum, $A$ is the area of the MIS device, $C$ is the measured accumulation capacitance and $t$ is the insulator thickness.

Figure 3.3 Multiple-frequency C-V plots for RF pulse plasma deposited polyallylamine films (a) PA1: sample deposited at room temperature (b) PA2: sample deposited at 100 °C.
Leakage current versus gate voltage measurements determine the amount of current able to conduct vertically through the MIS capacitor. A small leakage current implies the polymer layers contain few electrically active defect centers and virtually no pinholes.

![Graph showing leakage current density versus voltage](image)

**Figure 3.4** The vertical leakage current density of PPP allylamine capacitors.

Both samples showed leakage currents below 20 fA up to 100 V bias, resulting in a leakage current density of only $6 \times 10^{-11}$ A/cm$^2$ at an electric field strength of 5 MV/cm for a 200 nm thick film (Fig. 3.4). The leakage current density of thermally grown SiO$_2$ at 5 MV is about $10^{-9}$ A/cm$^2$ for a 100 nm thick oxide [138], which is more than ten times higher than that of RF pulsed plasma polyallylamine. This is an extremely small leakage current and clearly shows the electrical integrity of PPP polyallylamine films. No
electrical breakdown in either PA1 or PA2 was observed up to the measurement limitation of a 100 V applied gate voltage. This data indicates that the breakdown electric field must exceed 5 MV/cm.

3.3 High-k dielectric films

3.3.1 Method to improve the dielectric constant of PPP dielectric films

Recent PFETs are rivaling amorphous silicon TFTs and poly-Si TFTs, but are generally more limited in output power than single crystal MOSFETs due to the lower mobility of the active semiconducting organic layer. Reducing the gate dielectric thickness is an effective way to decrease the voltage required to turn on a transistor and drive it into the saturation region. Therefore, a thinner gate dielectric is highly desired to effectively increase output power, but highly challenging if seeking flexibility simultaneously.

The magnitude of the dielectric constant depends on the polarizability of the polymer constituents. The dielectric constant of materials can be predicted from its molecular dielectric polarizability and molar volume. Polarizability is the ability of the polarizable units, namely electronic, atomic and dipolar, in an insulator to orient quickly enough to keep up with the oscillations of an alternating electric field. A higher dielectric constant is demonstrated by materials with high polarizability. Prediction of molecular polarizability involves tedious calculations. A simple estimation of polarizability is to sum tabulated polarizabilities of the molecule under consideration [139-143]. This method can be used to predict the molecular polarizability of monomers.
Molar volume also has an effect on the dielectric constant since the introduction of free volume decreases the number of polarizable groups per unit volume. Dense chain packing in polymers limits free volume. For high-k materials, factors which prevent efficient chain packing, like pendant groups, flexible bridging units, and bulky groups, must be minimized [140-143]. The PPP approach offers a viable route to minimizing free volume in a polymer via the appropriate choice of monomer and plasma deposition conditions. A good starting point will be a single variable experimental design on the pulse duty cycle to create polymer conformation differences.

Plasma polymerization has the advantage of a wide selection of monomers. Therefore, our high-k dielectric studies start with a monomer containing atoms of high polarizability.

3.3.2 High-k PPP DCTMDS dielectric films

Our most recent work started with a monomer containing atoms of high polarizability. The monomer dichlorotetramethyldisiloxane (DCTMDS) contains a –Cl functional group in its structure, which has a high tabulated polarizability and therefore should improve the dielectric constant of the polymer insulator.

The study of PPP DCTMDS dielectric films was divided into two parts. Part one examined how the duty cycle affects the permittivity of polymerized DCTMDS dielectric films. Two duty cycles, 10ms/90ms and 10ms/30ms, were used to deposit DCTMDS dielectric films. For each duty cycle, two deposition durations were used to generate a thin sample and a thick sample. Therefore, this step also tested if the permittivity changes
with overall film thickness or deposition time. The deposition parameters and testing results are listed in Table 3.1.

The permittivity was evaluated by two methods, indirectly by measuring the refractive index by ellipsometry and more directly by calculating the dielectric constant from an analysis of the capacitance-voltage relationship of the Au/PPP DCTMDS/Si MIS structure (Fig. 3.5).

Figure 3.5 A photograph of a quarter of a 2-inch Si wafer with the PPP DCTMDS dielectric deposited atop and 0.6 mm Au dots shadowmask evaporated atop the PPP film forming the MIS capacitor.
All the dielectric constants are derived using C-V characteristics at a 1 MHz frequency. Five measurements were taken on each sample to check the consistency of testing results. The refractive index measurement was performed using a Rudolph AutoEL III ellipsometry and the C-V characterization used an Agilent 4284A LCR meter coupled with Material Development Corporation CSM/Win analysis software. The results listed in Table 3.1 and 3.2 are the averages and standard deviations calculated from the five measurements for each sample.

Part two of this study identified the optimal temperature window for post-deposition annealing to reduce the leakage current through the dielectric. Six samples were prepared for this study. One of the six samples did not receive post-deposition annealing and was kept as the experimental control. The other five samples were annealed for 3 hours in air at 150, 200, 250, 300, and 350 °C respectively.

The capacitance of samples DCTMDSI1 through DCTMDSI4 were normalized by area and thickness by $A/t$ and plotted against gate voltage as shown in Fig. 3.6. With the vertical axis being $Ct/A$ in Fig. 3.6, the data in the accumulation region actually is representative of the relative dielectric constant of the polymerized DCTMDS films. The effects of the duty cycle and thickness are listed in Table 3.1, which shows that high duty cycles generate samples with slightly higher relative dielectric constants. For low duty cycle samples, thicker samples have higher relative dielectric constants, but this phenomenon did not happen with high duty cycle samples. Therefore it seems that the thickness of the deposited films is not a significant factor for controlling permittivity.
Figure 3.6 Capacitance-voltage characteristics of MIS capacitors using PPP DCTMDS dielectric films at 1 MHz.

The calculated dielectric constants are in the range of 7 to 10, which is remarkable result since it is a relatively high number for an organic system. The most commonly used polymers, like polyethylene and Teflon, have dielectric constants only slightly higher than 2. The few reports of flexible polymer dielectric films used as gate insulators in PFETs [59, 112, 125-127], such as polyvinylphenol or polyimide, generally have dielectric constants ranging from 3 to 3.5. Thus, these results compare very favorably to the more common choice for PFETs of rigid thermally grown SiO$_2$ which has a dielectric constant of 3.9.
<table>
<thead>
<tr>
<th></th>
<th>Duty cycle</th>
<th>Deposition time (min)</th>
<th>Thickness (Å)</th>
<th>Relative dielectric constant</th>
</tr>
</thead>
<tbody>
<tr>
<td>DCTMDSI1</td>
<td>10/90</td>
<td>12</td>
<td>600</td>
<td>7.3±0.15</td>
</tr>
<tr>
<td>DCTMDSI2</td>
<td>10/90</td>
<td>24</td>
<td>1300</td>
<td>9.2±0.24</td>
</tr>
<tr>
<td>DCTMDSI3</td>
<td>10/30</td>
<td>22</td>
<td>790</td>
<td>10.4±0.32</td>
</tr>
<tr>
<td>DCTMDSI4</td>
<td>10/30</td>
<td>37</td>
<td>1450</td>
<td>10.5±0.73</td>
</tr>
</tbody>
</table>

Table 3.1 The effect of duty cycle and thickness on the dielectric constant of PPP DCTMDS films.

Testing results also show that high duty cycles generate samples with higher dielectric constants. For low duty cycle samples, the thicker samples have a higher refractive index and dielectric constant, but this phenomenon does not occur with high duty cycle samples. Therefore, there is no clear trend based upon this data set that the thickness of the deposited films is a significant factor for controlling permittivity.

One drawback with samples DCTMDSI1 to DCTMDSI4 is that they exhibit a large leakage current density. To solve this problem, post-deposition annealing was employed. Annealing improves the material integrity and possibly densifies the film. A set of six samples was prepared for an annealing study. Since a 10ms/30ms duty cycle was identified as producing a higher permittivity than a 10ms/90ms duty cycle according to the results of DCTMDSI1 through DCTMDSI4, the duty cycle of 10ms/30ms was selected for the subsequent annealing study. The annealing temperatures and testing results are listed in Table 3.2. It is clear that all the annealed samples have lower dielectric constants than the as-deposited samples.
The thickness of the samples DCTMDSII1 through DCTMDSII6 before annealing was about 1150 Å. The thickness of DCTMDSII2 retained its thickness after annealing, but for the rest of the samples, it is observed that the thickness of the films shrinks with heat treatment and that higher annealing temperatures reduce the thickness more substantially. The refractive index measured by ellipsometer also decreases with rising annealing temperature, which also indicates that the permittivity of the films is reduced due to heat treatment.

<table>
<thead>
<tr>
<th>Annealing temperature (°C)</th>
<th>Thickness (Å)</th>
<th>Relative Dielectric constant</th>
<th>Refractive index</th>
<th>Leakage current density (pA/µm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DCTMDSII1</td>
<td>N/A</td>
<td>1130</td>
<td>8.8 ± 0.11</td>
<td>1.572 ± 0</td>
</tr>
<tr>
<td>DCTMDSII2</td>
<td>150</td>
<td>1140</td>
<td>8.1 ± 0.52</td>
<td>1.568 ± 0.0008</td>
</tr>
<tr>
<td>DCTMDSII3</td>
<td>200</td>
<td>1050</td>
<td>7.4 ± 0.15</td>
<td>1.554 ± 0.0011</td>
</tr>
<tr>
<td>DCTMDSII4</td>
<td>250</td>
<td>1010</td>
<td>8.7 ± 0.05</td>
<td>1.540 ± 0.0011</td>
</tr>
<tr>
<td>DCTMDSII5</td>
<td>300</td>
<td>860</td>
<td>4.9 ± 0.13</td>
<td>1.518 ± 0.0016</td>
</tr>
<tr>
<td>DCTMDSII6</td>
<td>350</td>
<td>800</td>
<td>6.1 ± 0.11</td>
<td>1.509 ± 0.0048</td>
</tr>
</tbody>
</table>

Table 3.2 The effect of post-deposition annealing on the properties of PPP DCTMDS dielectric films.

Table 3.2 also shows that the dielectric constants calculated from C-V measurements are not necessarily proportional to the square root of the refractive index. The trend for dielectric constants changing with annealing temperature according to C-V is not as clear as for the changes in refractive index. This could be because the capacitance measurement is affected by factors such as leakage current and series resistance that cause the MIS diode to have a low phase angle. These factors may cause the measured capacitance to deviate from the real capacitance, which in turn alters the
calculated dielectric constants. The disturbance of these non-ideal factors is usually illustrated in the phase angle during the measurement. The ideal phase angle for a C-V measurement should be 90°. The smaller the phase angle, the bigger effect these non-ideal factors have on the measurement. The phase angle for DCTMDSII1 and DCTMDSII4 was about 70°, for DCTMDSII2 and DCTMDSII3 was about 80°, and for DCTMDSII5 and DCTMDSII6 was about 40°.

Figure 3.7 shows smoother C-V curves for DCTMDSII2 and DCTMDSII3 and figure 3.8 shows that DCTMDSII2 and DCTMDSII3 also have the lowest leakage current density. The leakage current density of these samples is at least an order of magnitude smaller than the un-annealed sample (Fig. 3.8(b)). If the annealing temperature is too high, the samples can have even higher leakage than the un-annealed DCTMDSII1. It is observed that the optimum annealing temperature range for polymerized DCTMDS is between 150 to 200 °C. When the annealing temperature is less than or equal to 200 °C, the leakage current is reduced with increasing temperature. However, once the annealing temperature surpasses about 250 °C, the leakage current is elevated. It is suspected that the samples annealed at the highest temperatures, DCTMDSII5 and DCTMDSII6, are damaged probably due to the volatizing of low molecular weight oligomers and eventually leading to breakage of relatively weak chemical bonds in the polymer.
Figure 3.7 Multi-frequency C-V characteristics of DCTMDSII1 through DCTMDSII6 annealed at different temperatures: (a) No anneal; (b) 150 °C; (c) 200 °C; (d) 250 °C; (e) 300 °C; and (f) 350 °C.

(Continued)
Figure 3.7 continued

(c)

(d)
Figure 3.7 continued

(e) Annealing temp. 300 °C

(f) Annealing temp. 350 °C

Voltage (V)

Capacitance (pF)

Frequency
- 1 MHz
- 100 kHz
- 10 kHz
- 1 kHz
- 100 Hz
- 100 Hz
Figure 3.8 Leakage current density versus voltage of PPP DCTMDS (a) leakage current density of samples DCTMDSII1 through DCTMDSII6 (b) expanded view of the leakage current density of samples DCTMDSII2 and DCTMDSII3.
The absorption bands were also measured for the monomer, a polymer film using a 10/30 on/off ratio before annealing and the same polymer film after after annealing are plotted in Fig. 3.9. The absorption for the monomer is much sharper than those of the polymers because it is a liquid. The bands are always much sharper for liquids. This simply reflects the fact that some motions are restricted in the solidified polymer films. The absorptions at wavenumbers 1260, 1060 and 800 are assigned to C-Si, Si-O and Si-Cl stretching vibrations, respectively. The Si-C suffers the largest loss during the PPP process while the Si-O signal was retained well. Annealing causes further loss of Si-Cl bonds, which could explain the reduced permittivity in annealed samples. Nevertheless, DCTMDSII2 and DCTMDSII3 PPP films still have dielectric constants that are twice that of SiO₂.

Figure 3.9 FTIR spectra of DCTMDS monomer, polymerized DCTMDS before annealing and polymerized DCTMDS after annealing.
Finally, it was shown that the PPP DCTMDS films are resistant to immersion in typical chemical solvents encountered during PFET fabrication, such as acetone, methanol, and isopropynol. They are even robust enough to withstand conventional photolithographic processing with no observable film shrinkage, warping or peeling (Fig. 3.10).

(a)

(b)

Figure 3.10 (a) A photomicrograph of the PPP DCTMDS film before photolithography and (b) after photolithography showing the photoresist covering some regions. Note, the square is an opening through the photoresist. No observable change to the PPP film is noted.
Since working P3HT FETs on PPP DCTMDS films were demonstrated, it at least shows that the films are also resistant to xylene, one of the most widely used solvents for electroactive polymers. Film adhesion was also excellent and PPP films withstood the scotch tape test (Fig. 3.11).

Figure 3.11 A photograph of a portion of the Si wafer coated with a PPP DCTMDS film and then with Au dots selectively shadowmask evaporated. Here Scotch tape is used to test film adhesion.
3.3.3 PFETs using high-k PPP DCTMDS as gate dielectric

The best quality PPP DCTMDS film was chosen as the gate dielectric for a bottom contact (coplanar) regioregular poly(3-hexylthiophene) (P3HT) PFETs (Fig. 3.12). The thickness of the gate dielectric was about 850 Å, and it was annealed at 200 °C for 3 hr in air.

![Diagram of P3HT PFETs](image)

Figure 3.12 The structure of P3HT PFETs using PPP DCTMDS as gate dielectric.

The gate was a boron-doped Si substrate with a resistivity of 0.05 to 0.1 Ω-cm. The source and drain contacts are 0.5×0.5 mm² Au pads made by shadow mask evaporation. P3HT was applied in solution by spin-coating. The P3HT PFETs were tested in a nitrogen atmosphere using Alessi probes and a Keithley 4200 semiconductor parameter analyzer.
The electrical characteristics of P3HT PFETs using PPP DCTMDS as their gate dielectric are shown in Fig. 3.13. It is demonstrated that PPP DCTMDS films possess good qualities as PFET gate dielectrics.

Figure 3.13 The $I_{DS}$ versus $V_{DS}$ characteristic of P3HT PFETs using PPP DCTMDS as gate dielectric under (a) accumulation and (b) depletion modes.
Compared to published PFET literature to date [54-64], these PFETs operate at relatively low supply voltages because of the high PPP DCTMDS capacitance attributed to the high permittivity. The threshold voltage extrapolated from $I_{DS}^{1/2}$ versus $V_G$ plot is only about 3 V. With such a low threshold voltage, PFETs with PPP DCTMDS gate dielectrics achieve saturation at relatively low $V_{DS}$. However, the drain current shifts at low source-drain biases implying a leakage pathway through the gate dielectric. Figure 3.13(b) shows that these transistors are turned off at positive gate bias instead of zero gate bias, which indicates that a positive voltage is needed to deplete the charges from the dielectric/semiconductor interface.

As expected, more negative gate bias accumulates more charges to the channel, so the transconductance of these PFETs increases with more negative gate bias (Fig. 3.14). There is a leakage $I_{DS}$ of 3 nA in the off state at a gate bias of 8 V. The ON/OFF ratio of these P3HT FETs between $V_G = 8$ V and $V_G = -8$ V was only about 20 at $V_{DS} = -5$ V, however. The subthreshold current is 1.6 nA (3.2 nA/mm gate width). Leakage through the PPP gate dielectric partially accounts for the high subthreshold current and poor ON/OFF ratio. Un-intentional doping in P3HT may also contribute to the high leakage in the devices. At the same time, the low ON current due to low mobility in these devices is another factor leading to the low ON/OFF ratio.
The high leakage current and low ON current in these devices also resulted in a high subthreshold swing of about 6 V/decade. The subthreshold swing was calculated as

$$S = \frac{\Delta V_G}{\log(\Delta I_{DS})}$$

in the subthreshold region, as shown in Fig. 3.15. In these experiments, no seed layer was used to promote ordering in the P3HT overlayer and therefore the mobility was limited. The low mobility on the order of $10^{-4}$ cm$^2$/V·s accounts for the poor ON current in these P3HT FETs.

The observed performance of P3HT FETs using PPP DCTMDS gate dielectrics suggested that the performance of PFETs needs to be improved by reducing the leakage current through the gate dielectric further, and also improving mobility in the channel at
the P3HT/gate-dielectric interface. However, the demonstration of polymerized DCTMDS films in working PFETs proved its potential to be the high-k gate insulator for flexible polymer circuits.

Figure 3.15 The linear portion of the $I_{DS}$ versus $V_G$ was used for the derivation of the subthreshold swing.

3.3.4 Low leak PPP DCTMDS

3.3.4.1 PPP DCTMDS films with a slow initial sublayer

By post-deposition annealing, the leakage current through PPP DCTMDS was decreased, but only one order of magnitude. The transfer characteristics of P3HT FETs using PPP DCTMDS as gate insulator illustrated that the ON/OFF ratio and subthreshold
swing need to be improved by limiting the leakage current further through the PPP DCTMDS gate dielectric.

With a respectably high dielectric constant for the PPP DCTMDS films demonstrated in the previous part of study, a Au/PPP-DCTMDS/Au test structure is now used to evaluate the leakage current more carefully. PPP DCTMDS films were deposited under three conditions. One was continuous wave (CW) plasma, conventional pulsed plasma, and pulsed plasma with a slow initiation layer of 1-ms/30-ms on/off ratio for the initial ~500 Å sublayer followed by 10-ms/30ms ratio to complete the total thickness. The detailed deposition parameters are listed in Table 3.3.

<table>
<thead>
<tr>
<th></th>
<th>CW</th>
<th>P</th>
<th>SIP</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>sublayer</td>
<td>upperlayer</td>
<td></td>
</tr>
<tr>
<td>Power (W)</td>
<td>20</td>
<td>75</td>
<td>75</td>
</tr>
<tr>
<td>On(ms)/off(ms)</td>
<td>N/A</td>
<td>10/30</td>
<td>1/30</td>
</tr>
<tr>
<td>ratio</td>
<td></td>
<td></td>
<td>10/30</td>
</tr>
<tr>
<td>Growth time (min)</td>
<td>25</td>
<td>40</td>
<td>11</td>
</tr>
<tr>
<td>Target thickness (Å)</td>
<td>2000</td>
<td>2000</td>
<td>500</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1500</td>
</tr>
</tbody>
</table>

Table 3.3 films formed with continuous wave plasma, pulsed plasma and slow initial pulsed plasma.

The power (20 W) used for CW sample deposition is close to the average power with 10ms-0n/30ms-off duty cycle (10/(10+30)×75 =18.7W). The deposited films were annealed at 200°C for 3 hr.

From the FTIR spectra shown in Fig. 3.16, it is clear that the film deposited under the 1/30 duty cycle has retained the largest Si-Cl absorption and the CW sample the least,
based on the relative intensity of the peak at 800 wavenumbers. The 10/30 film is intermediate between the 1/30 and the CW in terms of Si-Cl retention. Additionally, the composite film generated from an initial 1/30 followed by 10/30 is intermediate between the pure 1/30 and pure 10/30, as one might expect. Thus lowering the duty cycle clearly leads to less fragmentation of the starting monomer which contains two Si-Cl bonds. The peak at 1260 adds further evidence since the lowest duty cycle film has the most intense absorption, corresponding to retention of the Si-C bonds present in the starting monomer, of which there are four. The relative intensity of the Si-O band is most pronounced in the CW, followed by the 10/30 film indicating they are more silica-like films. This too would be consistent with destruction of the monomer under higher energy input.

Figure 3.16 FTIR spectra of PPP DCTMDS films deposited at varying duty cycles.
The slow initial growth layer was originally inserted to prevent intermixing with layers below, presumably due to sputter damage and re-deposition. Leakage current through PPP DCTMDS films deposited atop gold coated glass substrates was measured. Leakage current measurement is used as an indication to check if intermixing occurs during PPP deposition. Serious intermixing will incorporate Au into the PPP DCTMDS dielectric film and cause electrical shorting. As will be illustrated following, a slow initial sublayer also reduces leakage current density through the PPP DCTMDS films.

To evaluate the leakage current density in the PPP DCTMDS films, the Au/polymerized-DCTMDS/Au diode test structures were formed by depositing electrodes of five sizes on top of the PPP DCTMDS films. The diameters of the diodes were 1.11 mm, 0.98 mm, 0.86 mm, 0.73 mm, and 0.60 mm. As expected, the overall trend is that the leakage current increases with bigger diode size (Fig. 3.17). The hysteresis behavior implies interface and insulator traps. The hysteresis is most pronounced in SIP samples. Because SIP has the smallest leakage current, on the order of pA, the measured numbers are more likely to be skewed by an equipment offset. Therefore, the equipment offset accounts partially for the large hysteresis in SIP samples.
Figure 3.17 Leakage current of samples deposited with (a) CW plasma; (b) standard pulsed plasma; (c) pulsed plasma with a slow growth initiation layer of 500 Å.
The leakage current density (Fig. 3.18) in the plot was the average of the five leakage current densities calculated for each size. Leakage current density plot reveals that SIP has significantly less leakage. Its leakage current density is $10^3$ to $10^4$ lower than the CW control sample and P sample. This result indicated that SIP effectively controlled the leakage through the PPP film.

It was expected that the P sample should have a lower leakage than the CW sample because pulsed plasma deposition should cause less intermixing than CW. However, the test results show that the leakage current density in P sample was almost twice that of CW sample, even though the P sample is thicker. This phenomenon may be caused by the higher peak power used for the P sample deposition. The high power excites Au particles which settle back down onto the sample before the next pulse occurs. The Au particles could then embed themselves into the PPP film. This experimental result illustrated that to take the advantage of reduced intermixing with PPP deposition, the on/off ratio needs to be small enough.
Figure 3.18 (a) Leakage current density of PPP DCTMDS films; and (b) leakage current density of SIP with an expanded scale.
As listed in Table 3.4, the CW sample has the highest breakdown field, even though its surface roughness data showed that the granularity in P sample is a little finer. The SIP sample exhibited the worst breakdown properties, probably due to its large granularity.

<table>
<thead>
<tr>
<th></th>
<th>CW</th>
<th>P</th>
<th>SIP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thickness (Å)</td>
<td>1672 ± 56.0</td>
<td>2178 ± 97.0</td>
<td>2005 ± 17.5</td>
</tr>
<tr>
<td>Surface roughness (Å)</td>
<td>8.1</td>
<td>6.6</td>
<td>103.3</td>
</tr>
<tr>
<td>Leakage current density at 10 V (nA/mm²)</td>
<td>78</td>
<td>199</td>
<td>0.03</td>
</tr>
<tr>
<td>Breakdown field (MV/cm)</td>
<td>2.4</td>
<td>1.6</td>
<td>1.2</td>
</tr>
</tbody>
</table>

Table 3.4 Properties of PPP DCTMDS films deposited with continuous wave plasma, standard pulsed plasma and slow initial growth pulsed plasma.

AFM images showed that the SIP sample was composed of bigger particles than the CW and P samples (Fig. 3.19). The surface roughness of SIP was more than 10 times higher than that of CW and P. Larger sized particles in the SIP should be attributed to self-organization during the slow initial growth. It is surprising that subsequent growth at higher on/off ratio could not smoothen the film even if the thickness of the subsequent growth was almost three times thicker than that of initial sublayer.
Figure 3.19 AFM of images PPP DCTMDS films deposited under (a) continuous wave; (b) standard pulsed plasma 10/30 on/off ratio; and (c) slow initial growth conditions.
Therefore, pulsed plasma deposition can reduce leakage current through PPP DCTMDS films as long as the on/off ratio is sufficiently small. However, a slow growth renders larger granularity in the film deposited on the substrate. The breakdown property of the deposited film deteriorates if the particle size in the film is too large.

3.3.4.2 The effect of the thickness of the slow initial sublayer

As shown previously, a slow initial growth layer can reduce the leakage current density in PPP DCTMDS films effectively, but PPP DCTMDS films exhibited greater roughness when a slow initial growth layer was inserted below the bulk layer. In this section, we would like to explore how the thickness of this slow initial layer influences the overall film surface roughness and leakage current density.

Five thicknesses for the slow initial layer were used in this experiment. The pulse ON/OFF ratio for slow initial layer was 1-ms/30-ms, and that for upper-layer was 10-ms/30-ms. The experimental details are shown in Table 3.5. The surface roughness of PPP DCTMDS film was inspected using AFM before and after annealing at 160°C for 3 hours. For leakage current measurements, a top electrode was deposited atop the film to form a gold/polymerized-DCTMDS/gold metal-insulator-metal (MIM) test capacitor. The diameter of the diodes was about 700 µm.
Table 3.5 Deposition parameters and properties of PPP DCTMDS films with slow initial growth sublayer.

The optical microscopic images of samples SI-1 up to SI-5 are shown in Fig. 3.20. Sample SI-5 has too many defects, which invalidates it for the subsequent AFM and leakage measurements. It is hard to determine why the SI-5 sample has more defects than the other samples.
Figure 3.20 Optical microscopic images of SI-1 up to SI-5.
The AFM images of SI-1 up to SI-4 shown in Fig. 3.21 clearly illustrate that the thicker the slow initial layer, the bigger the feature size of the patterns in PPP DCTMDS films.

Figure 3.21 The AFM images of SI-1 up to SI-4.
The AFM images of samples after anneal are shown in Fig. 3.22 and the roughness listed in Table 3.6 illustrate that annealing changes the morphology of the films by making the feature boundaries less sharp, and improves the surface smoothness of DCTMDS films. The thermal anneal process was at 160°C for 3 hours.

Figure 3.22 The AFM images of samples after thermal anneal at 160 °C for 3 hrs.
Table 3.6 Surface roughness of SI-1, SI-2, SI-3, and SI-4 before and after anneal.

The plots of leakage current density vs. gate voltage in Fig. 3.23 and Table 3.7 show that the leakage current density increases from SI-1 to SI-4, which indicates that a thicker slow-initial-layer reduces the leakage current density. The reason for the curves jiggling up and down is yet unknown.

Table 3.7 Leakage current density of samples SI-1, SI-2, SI-3, and SI-4.
Therefore, very low leakage current densities are achieved with PPP DCTMDS films. The leakage current density reduces for films with a thicker overall slow initial growth layer. The size of the ordered structures increases for thicker slow initial layers. The surface roughness, in turn, is also larger for samples with a thicker slow initial growth layer. Thermal annealing smoothen the film surface to a certain extent, but the surface roughness is still relatively large when compared with samples deposited using a single duty cycle.
Two control samples deposited using single duty cycle for the full thickness were included in this data set. One was deposited entirely with an ON/OFF ratio of 1-ms/30-ms with the thickness of 200 Å, and the other 10-ms/30-ms for 2000 Å. As shown in the AFM images in Fig. 3.24, if only a single duty cycle is used for film deposition, neither 1-ms/30-ms nor 10-ms/30-ms pulse generates patterns with big feature sizes.

![AFM images of PPP DCTMDS films deposited using a single duty cycle for the full thickness.](image)

The surface roughness was only 13 Å for films deposited with a 1/30 plasma ON/OFF ratio and 6 Å for a 10/30 duty cycle. Even though there is a possibility that the roughness of the 1/30 sample could accumulate with thicker films, it is suggestive, based on the available data, that the big sized patterns are formed due to the combined use of two duty cycles during film growth for the slow-initial-layer and faster upper-layer deposition.
Based on the information of leakage current density through the PPP DCTMDS films, it is clear that the low duty cycle of 1/30 plasma ON/OFF ratio is the major factor which limits the overall leakage current density. As this layer becomes a significant portion of the overall film, then the leakage reduces accordingly. The surface of samples using a single duty cycle is much smoother than the samples using two combined duty cycles. The growth rate at 1-ms/30-ms ON/OFF pulse is acceptable (almost 500 Å for 8 min) and the required film thickness is usually below 1000 Å. Therefore, it is suggestive that the film can be deposited at the single duty cycle of 1-ms/30-ms for the full thickness for both good smoothness and low leakage current.
CHAPTER 4

STUDIES ON FIELD EFFECT TRANSISTORS

BASED ON ELECTROACTIVE POLYMER SEMICONDUCTORS

4.1 Field dependence of mobility in organic FETs

Polymer field effect transistors (PFETs) have received tremendous attention lately for their potential application in flexible displays and foldable logic using solution-processible polymers. Vacuum deposited oligomers are a second type of organic semiconductor that has been implemented as organic field effect transistors (OFET). High channel mobilities have been demonstrated up to 1 cm$^2$/V·s for pentacene OFETs by vacuum deposition of single crystal active layers [74, 77]. Even though reported channel mobility of PFETs are one order of magnitude lower than that of crystalline pentacene, solution-processible polymers are drawing further interest, for their potential to scale up to cheaply reel-to-reel batch processing [54-64]. The advantage of solution processibility makes semiconducting polymer electronics attractive for large-area and low-cost applications. Research on PFETs has caught up quickly even though the first
OFETs were based on sublimed oligomer electroactive materials. Already PFETs have been monolithically integrated with polymer light emitting diodes (PLED) [63-64].

The field effect mobility is the central figure-of-merit for overall current drive capability. Unlike inorganic thin film transistors (TFTs), the drift mobility in OFETs are gate and source/drain bias dependent. It was reported in 1995 that in vacuum evaporated oligothiophene FETs, the field-effect mobility depended upon longitudinal electric fields across the source and drain when the field is higher than $10^5 \text{ V/cm}$ [39]. Later work described a gate voltage dependent mobility in oligomer and polymer FETs. The dependence of field effect mobility on gate voltage in highly ordered OFETs is not the same as amorphous OFETs. Experimental results showed that the field-effect mobility was quasilinearly dependent on gate bias in sublimated oligothiophene FETs [144]. On the other hand, a theoretical study found that in amorphous OFETs the gate-voltage dependence followed a power law and good agreement between theory and experiment data was obtained in amorphous polythienylene vinylene and pentacene [37].

Here we examine the mobility variation with channel length in polythiophene (PT) PFETs. It is surprising that a higher mobility is obtained using shorter channel lengths at high source/drain voltages, which is opposite to the trend for amorphous Si thin film transistors (TFTs) [40, 145-147]. This is probably due to the electric field dependence of mobility in an organic semiconductor system. For higher $|V_{DS}|$ or shorter channel lengths, the superlinear trend in gate bias dependence of mobility becomes obvious. Since the PT used in this study is non-crystalline, the relationship between mobility and gate bias is expected to follow the power law.
4.2 Fabrication and testing of short-channel polythiophene PFETs

Polythiophene (PT) PFETs with channel lengths ranging from 7 µm down to 1 µm in 1 µm decrements were fabricated in a coplanar configuration. The active channel is composed of the conducting polymer, poly(thiophene-2,5-diyl) (PT). As sketched in Fig. 4.1, a layer of SiO₂ with a thickness of about 1 µm has been thermally grown on a piece of Si substrate.

Figure 4.1  Schematic of the upside down PFET structure with an underlying metal gate used in this study.

This layer of SiO₂ provides electrical isolation between the Si wafer substrate and the rest of the PFET structure. In most published work, the conductive Si wafer serves the dual function of a supporting substrate and the gate at the same time. The function of the Si substrate is different in this experiment where the Si wafer is capped with an insulator, so a metal gate can be deposited onto it. Though doped Si is quite conductive, its conductivity is still a few orders of magnitude lower than that of metal. Using a metal
gate can minimize the power dissipated within the gate material itself. A gate metal (Ti/Au) was electron beam evaporated on top of the thermally grown SiO$_2$ layer which isolates the Si substrate and the PFET structure. With the PFET structure in this study, the substrate can be glass, or even plastic, which is the preferred substrate material for flexible electronics. The Si wafer is used only as the support substrate in this experiment. Due to the device configuration of our PFET design, the gate insulator needs to be deposited on top of the gate metal instead of Si, which prevents the use of thermally grown SiO$_2$. To solve this problem, a SiO$_2$ gate dielectric was electron beam evaporated. The thickness of the gate dielectric was about 2500 Å. The tradeoff is the e-beam SiO$_2$ does not have as a high breakdown voltage as thermally grown SiO$_2$, but it is effective as a gate insulator within the range of voltage studied. Interdigitated source and drain electrodes were defined by standard liftoff photolithography. The PFETs had multiple source/drain spacings leading to multiple channels, and each channel was 75 µm wide. Interdigitated configurations are widely used in power transistors to handle large currents generated due to the large W/L ratio. One of the intended applications of PFETs is to drive PLEDs, which requires an output current on the order of milliamperes. The interdigitated configuration is a good choice for high driving power capability. The size of the PFETs is denoted by $W \times (L \times n)$ where $W$ is the gate width, $L$ is the gate length and $n$ is the number of channels. After source and drain contact metal lift-off, the commercial grade PT was applied in solution form (about 0.5% in the solvent xylene) by spin coating at 4000 rpm for 30 seconds. The PT solution was filtered with a 1 µm pore size to reduce impurity concentrations. The PT PFETs were characterized with an Agilent HP 4156 parameter analyzer using a Cascade probe station.
4.3 Channel mobility in polythiophene PFETs

The $I_{DS}$-$V_{DS}$ characteristics were determined with applied drain-source voltage ranging from 0 to $-40$ V and with gate biases varying from 0 to $-16$ V. The test results showed a slight deviation in the $I_{DS}$-$V_{DS}$ relationships from the expected ideal case. For devices with channel lengths above 3 $\mu$m, $I_{DS}$ demonstrates reasonable saturation. Figure 4.2 shows the gradual loss of saturation as channel lengths are reduced from 7 $\mu$m to 1 $\mu$m in 1 $\mu$m decrements.

![Graph (a)](image1)

![Graph (b)](image2)

Figure 4.2 Measured $I_{DS}$-$V_{DS}$ curves for $V_{DS}$ up to $-40$ V and $V_{GS}$ up to $-16$ V with channel lengths varied from (a) 7 $\mu$m to (g) 1 $\mu$m.
Figure 4.2 Continued

(c) Gate Voltage
- 0 V
- -4 V
- -8 V
- -12 V
- -16 V

Drain-Source Voltage (V)

Drain-Source Current (µA)

75 x (5 µm x 10)

(d) Gate Voltage
- 0 V
- -4 V
- -8 V
- -12 V
- -16 V

Drain-Source Voltage (V)

Drain-Source Current (µA)

75 x (4 µm x 12)

(e) Gate Voltage
- 0 V
- -4 V
- -8 V
- -12 V
- -16 V

Drain-Source Voltage (V)

Drain-Source Current (µA)

75 x (3 µm x 14)

(Continued)
Figure 4.2 Continued

(f) 

Drain-Source Current (µA) vs. Drain-Source Voltage (V) for a device with dimensions 75 x (2 µm x 18).

(g) 

Drain-Source Current (µA) vs. Drain-Source Voltage (V) for a device with dimensions 75 x (1 µm x 24).
Similar behavior was observed in oligothiophene OFETs and short channel effects cause the deviation [39]. Short channel effects were also described in amorphous Si thin film transistors [145 - 147]. The effect of decreasing channel lengths on $I_{DS}$ saturation is observed in Si TFTs, oligomer TFTs and polymer TFTs, which implies that the channel length effect on $I_{DS}$ saturation is device structure dependent rather than semiconductor material related. The PT PFETs studied here can also operate in depletion mode, as in the PFETs based on poly(3-hexylthiophene) [61]. The PT PFETs required at least 20 V gate bias to completely turn the channel off (Figure 4.3) due probably to charged residual impurities in the commercial polymer.

![PT PFETs Depletion Mode](image)

**Figure 4.3** Measured $I_{DS}$-$V_{DS}$ curves for polythiophene PFETs operated in depletion mode.
To compare the different sized PFETs, the measured current $I_{DS}$ was normalized, defined as $I_{DS}/n$ with $n$ being the corresponding number of multiple channels per PFET structure. Figure 4.4 shows an increase in the normalized $I_{DS}$ with decreasing channel length.

This can be explained by the reduction in channel resistance with decreasing channel length. As the gate voltage decreases, the normalized $I_{DS}$ drops for the increased channel resistance. However, this observation is opposite to amorphous Si TFTs. The reduction in drain current with decreasing channel length in amorphous Si TFTs was due to the increased role of parasitic resistance compared to the intrinsic channel resistance at low dimensionality. The parasitic resistance decreases with increased source/drain to gate
overlap [40]. In the oligothiophene FET study by Torsi et al. who also used an un-patterned gate, similar to this work, it was found that the parasitic resistance is more than ten times lower than the total resistance of the device due to a very large source/drain to gate overlap [39]. Therefore, the role of the parasitic resistance should be less sensitive to the change in channel length if the parasitic resistance is low while the channel resistance is high, which is true for semiconductor polymers. This reasoning could explain the increased drain current in PFETs but decreased current in amorphous Si TFTs when channel lengths are shorter.

The channel mobility was extracted from $I_{DS}$ versus $V_{DS}$ plots at varying $V_{DS}$ values. When $|V_{DS}| < 20$ V, the PT PFETs with all seven sizes exhibit a linear behavior. The channel mobility is calculated for each size from the linear equation

$$ I_D = \frac{Z\mu C_o}{L} \left[ (V_G - V_T) V_D - \frac{V_D^2}{2} \right] $$  \hspace{1cm} (4.1)

Once $|V_{DS}|$ increases to over 20 V, the longer channel transistors enter the saturation region. At $V_{DS} = -40$ V, all PT PFETs with channel lengths greater than 3 µm achieve $I_{DS}$ saturation. Under these conditions, the saturation mobility is calculated from

$$ I_{DSat} = \frac{Z\mu C_o}{2L} (V_G - V_T)^2 $$  \hspace{1cm} (4.2)
The data at $V_{DS} = -10 \, \text{V}$, -20 V, and -40 V is used to calculate PT PFETs mobility and the results are summarized in Figure 4.5. The calculated mobility might deviate from the real mobility because no correction factors such as channel-length modulation, leakage current and velocity saturation were included in Eqns. 4.1 and 4.2. The inclusion of these factors would reduce the error between the calculated mobility and real mobility, but it is hard to accomplish due to a lack of necessary information such as permittivity of the PT, charge carrier concentration in the channel, at the PT/SiO$_2$ interface, contact resistance and barrier height between the electrodes and PT, local heating and so on. Therefore, for the present work, equations in their simple forms like Eqns. 4.1 and 4.2 are used for the mobility derivation, so that an initial estimation of mobility in PFETs is permissible in this way.

The mobility of 1 $\mu$m PT PFETs exhibits the lowest value at $V_{DS} = -10 \, \text{V}$, whereas the mobility of other sized PFETs are slightly higher and similar [Fig. 4.5(a)]. The intrinsic semiconductor material is likely the major cause of the observed differences. Doped Si has a much higher conductivity than semiconducting polymers, so a PT channel must have a much higher total resistance than an amorphous Si channel. Since the channel resistance is already so high, the effect of contact resistance is likely masked. Previous work showed that by getting rid of the source/drain series resistance, the apparent field effect mobility was independent of channel length [147]. However, the high polymer resistance only reduces the effect of source/drain series resistance, rather than eliminates the effect. The PFETs with 5, 6, and 7 $\mu$m channel lengths exhibit higher extracted mobilities than smaller gate lengths. This result is consistent with previous results in amorphous Si TFTs [40]. PFETs with small channel lengths had lower
mobilities because the source/drain contact series resistance has a larger effect on short channel devices. When $V_{DS} = -20$ V, the extracted mobility for PT PFETs with channel lengths 2, 3, and 4 $\mu$m still remains lower than that with channel lengths 5, 6, 7 $\mu$m. However, the mobility of 1 $\mu$m PFETs is no longer the smallest. It rises to be comparable with larger channel lengths [Fig. 4.5(b)]. The extracted mobility at high $V_{DS}$ (-40 V) continues this trend and is even more contradictory to the previous results in amorphous Si TFTs. As illustrated in Fig. 4.5(c), the PFETs with 1 $\mu$m channel lengths now have the highest extracted mobility, which is above longer channel PFETs. In addition, PFETs with 2 $\mu$m channel length have the second highest extracted mobility. However, the extracted mobilities of the remaining sized PFETs are closely spaced and indistinguishable.

Based on the previous comparison of Fig. 4.5(a), 4.5(b), and 4.5(c), it is clear that some factor other than source/drain resistance is influencing the mobility dependence on channel length in PFETs. This factor becomes stronger as $|V_{DS}|$ increases and surpasses any customary short channel effects eventually. The high intrinsic resistance of polymers can weaken the effect of source/drain contact resistance to some extent, but it is difficult to completely cancel out the contact resistance effect. The intrinsic resistance of polymers is also not likely to change with $V_{DS}$ at a set gate bias. However, the longitudinal electric field changes proportional to $V_{DS}$. It is already known that the drift mobility in many organic materials exhibits an electric field dependence, though the origin of the field dependent mobility is not quite clear yet.
Figure 4.5 Calculated mobility dependence on gate bias at various $V_{DS}$ for PFETs with different channel lengths. (a) $V_{DS} = -10$ V; (b) $V_{DS} = -20$ V; and (c) $V_{DS} = -40$ V.
The drift mobility increases significantly when the longitudinal electric field across the source and drain exceeds a critical value of 100 kV/cm. By dividing the applied $V_{DS}$ with the channel length, it is easy to determine that at $V_{DS} = -10$ V, only the PFETs with 1 µm channel lengths are at the threshold of this high longitudinal electric field. Then at $V_{DS} = -20$ V, the 1 µm PFETs have a longitudinal electric field of 200 kV/cm, so their mobility is more greatly influenced by this high field than other sized PFETs. The 1 µm PFETs acquire a 400 kV/cm longitudinal electric field at $V_{DS} = -40$ V, and the corresponding 2 µm devices have 200 kV/cm at this bias. The very high longitudinal electric field explains why 1 and 2 µm PT PFETs possess the highest and second highest mobility at $V_{DS} = -40$ V, respectively. It is interesting to note that even when the longitudinal electric field is slightly higher than 100 kV/cm, the shortest channel PFETs still have lower mobility than longer channel PFETs. Only when the longitudinal electric field reaches a sufficiently high value ($\geq 200$ kV/cm) will the mobility of the short channel PFETs rise above longer channel PFETs. These results indicate that the increasing longitudinal electric field gradually cancels out and eventually surpasses any short channel effects.

Finally, it is observed that the mobility can also increase with increasing gate bias. The gate bias dependence of mobility has already been reported in pentacene and a series of oligothiophenes. The gate bias may have the effect of lowering the activation barrier for carrier hopping [148]. An alternative explanation for the gate-voltage dependence of the mobility would be related to the charge concentration, which increases with the gate voltage [144]. As already mentioned in the introduction, for amorphous organic transistors, the gate bias dependence of mobility follows a power law $\mu_{FE} = \alpha V_G^\beta$, and the
expressions for constant \( \alpha \) and exponent \( \beta \) can be found in Horowitz et al. [36]. The semiconductor layer in this work was an amorphous PT film spin coated from solution, and the mobility data obtained fits a power law. However, the degree of fitting seems to be different for PFETs with varying source-drain bias \( (V_{DS}) \) and channel lengths. It appears that at higher \(|V_{DS}|\), the channel mobility is more sensitive to the gate bias and therefore their extracted mobility fits the power law theory more clearly. On the other hand, PFETs with shorter channel lengths begin to show correlation between their field effect mobility and gate bias at reduced \(|V_{DS}|\). In other words, the mobility becomes more strongly gate bias dependent with increasing longitudinal electric field. Therefore, this work illustrates that the longitudinal electric field also modulates the dependence of channel mobility on gate bias.

By fitting the mobility and gate bias data into a power law, the exponent, which is related to the operating temperature and activation energy for carriers to hop according to Horowitz et al. [36], can be obtained. A threshold voltage is included in the fitting process to justify the factor that when \( V_{GS} = 0 \) V, the FETs are actually on. The threshold voltage was determined by plotting the square root of the saturation current of \( I_{DS}^{1/2} \) versus \( V_{GS} \). An average threshold voltage of 68 V is obtained and used in the power law fitting. Since the whole process of sample preparation and characterization was in ambient and no surface passivition was employed, the PT PFETs in this experiment had a relatively high threshold voltage. However, the high value does not affect its validity in power law fitting calculation. Only when \( V_{DS} = -40 \) V are trends for all seven mobility curves clear, so power law fitting is done with these data.
Figure 4.6 Variation of the square root of the saturation current (taken at $V_d = V_g$) as a function of the gate bias to derive threshold voltage (Adopted from Horowitz et al.).

The exponents for the 1 to 7 µm PFETs obtained by power law fitting are 0.007, 0.047, 0.043, 0.059, 0.047, and 0.054 respectively. No trend can be found between the exponent and channel length, at least among these available exponents. It is not surprising because the exponent is related to the device operating temperature and carrier activation energy. Higher current densities at smaller channel lengths do cause some localized heating in the device, but there exist too many unknowns to evaluate the importance of local heating to the exponent value. It is hard to define the relationship between the activation energy and channel length or longitudinal electric field at this
point, but by observation it is very clear that high longitudinal electric field enhances the correlation between field effect mobility and gate bias.

In conclusion, this work presents some unique features of PT PFETs with short channel lengths at high electric fields. Due to the high longitudinal electric field, the field effect mobility can increase rather than drop at short channel lengths due to short channel effect. Nevertheless, the short channel effect does result in the lack of \( I_{DS} \) saturation in PT PFETs with channel length lower than 3 \( \mu \text{m} \). The relationship between field effect mobility and gate bias follows a power law in amorphous PFETs. A final discovery in this study is that the high longitudinal electric field enhances the dependence of field effect mobility on gate bias.
CHAPTER 5
LIGHT SENSITIVE PFETs

5.1 Polymer photodiodes

Conjugated polymers have shown great promise as polymer light emitting diodes (PLEDs) and polymer field effect transistors (PFETs). Shortly after the discovery of polymer light emitting diodes, the light detecting properties of polymer diodes were also reported. It was found that polymer light emitting diodes can act as photodetecting diodes under reverse bias [149]. Photodiodes with a charge separator were later presented, such as the titanium dioxide dispersed in an MEH-PPV host [150]. Polymer based resonant cavity enhanced photodiodes were also implemented, which exhibited a tunable photodetection energy range [151]. Recently polymer semiconductors found further applications as ultraviolet light photodiodes [152].

5.2 Chemistry of BAS-PPE

The highest occupied molecular orbital (HOMO) and lowest unoccupied molecular orbital (LUMO) levels of semiconductor polymers can be critical in building a working device because the energy barrier for charge injection is determined by the energy difference between the metal electrode and the HOMO and/or LUMO levels.
Fortunately, the HOMO and LUMO properties of polymer semiconductors can be engineered by proper chemical synthesis. Polyphenyleneethynylene (PPE) derivatives are such a group of polymers whose bandgaps can be altered by changing the substitute side chains on the PPE main chain [153]. As the dehydrogenated congener of polyphenylenevinylene (PPV), PPE did not receive as much popularity in the early boost of semiconductor polymer research due to its low HOMO level. However, recently PPE derivatives have attracted more attention due to work on cross-conjugated polymers. The cross-conjugated PPE-PPV hybrids 2,5-bis(dibutylaminostyryl)-1,4-phenylene-b-alkyne-b-1,4-bis(2-ethylhexyl)benzene terpolymer (BAS-PPE) demonstrate the combined advantages of both PPV and PPE (Fig. 5.1).

Figure 5.1. The chemical structure of BAS-PPE.
PPEs feature a triple instead of double bond in the conjugated backbone. The electron withdrawing nature of the alkyne groups determines that hole injection into PPE is subject to a high energy barrier [153-154]. The styryl side chains are laterally attached to the benzene rings in the PPE backbone. The bulky nature of the styryl side chains prevents conformational order in BAS-PPE, so this polymer is amorphous and has broad absorption/emission spectra. Due to the strongly electron-donating side chains 2,5-bis(dibutylaminostyryl), BAS-PPE is easily oxidized and has a greatly improved HOMO level for carrier injection (Fig. 5.2). The butyl and ethylhexyl groups are introduced to promote the solubility of BAS-PPE in toluene or chloroform. The maximum and minimum electrochemical bandgaps for BAS-PPE are 2.43 eV and 1.50 eV, ideal for visible light absorption and emission.

Fig. 5.2 Band diagram illustrating improved charge injection in BAS-PPE.
5.3 Light sensitive FETs

When BAS-PPE is incorporated into polymer field effect transistors (PFETs) as the active semiconductor film, it is observed that the BAS-PPE based PFETs are strongly responsive to light. The drain-source current $I_{DS}$ is greatly increased under illumination. Actually, similar behaviors of $I_{DS}$ amplification with light illumination have been reported in metal-oxide-semiconductor field effect transistors (MOSFETs), metal-semiconductor field effect transistors (MESFETs), and other polymer based FETs [155-159]. The light responsive FETs are mainly utilized as light detectors. The working mechanism of light responsive FETs is that photogenerated electron-hole pairs form either a photo-current or a photo-voltage which in turn enlarges $I_{DS}$. In light responsive silicon on insulator (SOI) MOSFETs, the source-substrate-drain is analogous to a lateral bipolar junction transistor (BJT), so the photo-current is magnified by the BJT current gain [155-158]. In MESFETs, the gate Schottky barrier develops a photovoltage under illumination which acts as an additional gate bias to modulate $I_{DS}$ [158-159]. There are not many reports on light responsive PFETs, but one paper by Narayan and Kumar demonstrated light responsive behavior in PFETs based on regioregular poly(3-octylthiophene-2,5-diyl) (P3OT) [112].

In the P3OT light responsive PFETs by the Narayan group, the effect of light illumination from the gate side was attributed to be equivalent to an external gate bias [112]. On the other hand, Narayan et al. also remarked that the $I_{DS}$ amplification in light responsive PFETs is analogous to a lateral bipolar action, when light generated holes join the channel while electrons stay in the bulk and form a voltage bias opposing the source [112]. Here we examine the photosensitivity of BAS-PPE PFETs. The light intensity
influences not only the absolute value of $I_{DS}$, but also the ratio of $I_{DS}$ in light and under darkness ($I_{light}/I_{dark}$). The gate bias also impacts the $I_{light}/I_{dark}$ ratio.

5.4 BAS-PPE FETs fabrication and testing

In this work, BAS-PPE PFETs were built using a coplanar configuration, as shown in Fig. 5.3. Fabrication commenced by depositing gold as the gate metal on a glass substrate. A commercial polyimide (HD MicroSystems) was used as the gate dielectric. The polyimide was spin-coated on top of the gold gate from solution and then cured, by soft baking at 200°C for 30 min followed by 350°C for 1 hr in nitrogen. The thickness of the gate dielectric determined by Dektek profilometry was approximately 1 µm. A thick gate dielectric ensures that no electrical breakdown occurs even at high gate voltages. Interdigitated source and drain electrodes were defined by standard liftoff photolithography. BAS-PPE PFETs with a range of sizes were built, similar to the size and configuration used in the previous short channel PT PFET study.

Figure 5.3 Schematic of BAS-PPE PFETs.
The dimension of the PFETs is denoted by \( W \times (L \times n) \) where \( W \) is the gate width, \( L \) is the gate length and \( n \) is the number of channels. In the interdigitated configuration, the multiple source/drain spacings leads to a number of parallel channels. After the source and drain contact metal was defined by lift-off, the BAS-PPE is applied in solution form (about 2% in the solvent toluene) by spin coating at 5000 rpm for 30 seconds. The thickness of the resulted BAS-PPE film is determined to be about 40 nm by Dektek profilometry. The BAS-PPE PFETs were characterized with an Agilent HP 4156 semiconductor parameter analyzer using a Cascade probe station. The photo illumination is provided by the probe station’s incandescent light bulb. The incident light is normal to the top side of the sample. Overall light intensities were controllably varied by filtering the light source with a neutral density filter set without modification of the spectral output. Spectral analysis of the white light showed a broad output from approximately 400 nm to 800 nm and a peak wavelength of 600 nm, which was assumed for photo responsivity calculation.

5.5 Light responsivity of BAS-PPE FETs

Figure 5.4 shows the I-V characteristics of a BAS-PPE PFET with a \( 75 \times (3 \times 12) \) channel dimension. Figure 5.4 demonstrates that the terpolymer BAS-PPE works successfully as the semiconductor channel in PFETs. A sweep of \( V_{DS} \) shows that BAS-PPE is a p-type polymer and favors hole injection and transport. Without the chemical modification of cross-conjugation, PPE has a HOMO level of 6.0 eV and therefore there would be a small probability of hole injection through the gold S/D electrodes, which has
a workfunction of 5.1 eV. The barrier for hole injection is largely reduced by cross conjugation with the HOMO level varying between 5.1 to 5.5 eV in the BAS-PPE samples studied to date [153].

Figure 5.4 $I_{DS} - V_{DS}$ of BAS-PPE PFETs with $75 \times (3 \times 12)$ gate lengths under (a) illumination, and (b) darkness.
The electrical measurements under illumination also clearly indicate a strong dependence on overall incident light intensity for the BAS-PPE PFETs. A much higher value of $I_{DS}$ is obtained under strong light illumination than under darkness. With incident light, the gate voltage still has a slight modulation on the conductance of BAS-PPE PFETs, but saturation of $I_{DS}$ is suppressed during strong illumination. The lack of a saturation region suggests that pinch-off can not be reached due to persistent photo-generation. However, in previously reported P3OT PFETs, saturation was observed under illumination [112]. The difference in the appearance of saturation region could be caused by the difference in configuration of the PFETs. The P3OT PFETs utilized a staggered configuration, or top contact configuration, while the BAS-PPE PFETs studied here used a coplanar, or bottom contact, configuration. It can be assumed that in a staggered configuration, photoillumination can be shadowed by source/drain electrodes so that only the channel area is illuminated. On the other hand, PFETs in a coplanar configuration will not shadow the illuminated region and light is concurrently incident on the channel and the source/drain contacts. Therefore, the semiconductor polymer has a much larger effective collection region in this study.

For the BAS-PPE PFETs studied, with incident light, the channel can not be turned off, even at high positive gate biases. The number of thermally generated carriers should be small compared to the photogenerated carriers when the light is incident, so that the current at zero gate bias is mostly attributed to light generation in and near the channel region. Figure 5.4(b) illustrates that BAS-PPE is a relatively poor conductor under darkness, but the saturation region is clearly present without the influence of light.
Figure 5.5 shows that under darkness $I_{DS}$ is at the lowest value at around 10 V gate bias, then increases with more positive $V_{GS}$.

Figure 5.5 $I_{DS} - V_{GS}$ of BAS-PPE PFETs at varying light intensities.
It is surprising that $I_{DS}$ under darkness at 40 V gate bias is even higher than at -40 V, even though there is carrier injection in addition to thermal generation at a negative gate bias. It is surmised that a negative gate bias attracts holes to the polymer/insulator interface, and some holes may be trapped at the interface which may never reach the drain. On the other hand, a positive gate bias likely expels holes from the polymer/insulator interface and therefore fewer holes become trapped. Thus at positive gate bias, more holes are collected at the drain electrode and reflected in the higher $I_{DS}$ values measured.

A sweep of $V_{GS}$ demonstrates an increase in $I_{DS}$ with different light intensities. It is observed that the dependence of $I_{DS}$ on gate bias becomes weaker as the light intensity increases, coincident with P3OT PFETs. This phenomenon indicates that light generated carriers are less restricted by gate bias. Light generated carriers can reach the drain electrode from the channel, but they can still be collected at the drain without going through the channel because they are created throughout the bulk semiconductor polymer. As the population of light generated carriers surpasses the number of the source injected carriers with increasing light intensity, the gate bias gradually loses its ability to modulate the channel conductivity.

The intensity of the incandescent light source peaks at 600 nm, so the intensities of the incident light were measured with a calibrated Si photodetector assuming this peak wavelength. The peak light intensity used in this experiment is set to correspond to the light intensity of 16 mW. The smaller filtered intensities are normalized to the highest intensity. The approximate size of the incident light spot is about 5 mm in diameter. The samples tested have an active area of $75 \times 75 \mu m^2$, which equates to an approximate
incident optical power of 4 µW. The photoresponsivity in the BAS-PPE PFETs is estimated to be at least 5 mA/W.

Figure 5.6 shows $I_{DS}$ increases with higher light intensities.

Figure 5.6 The effect of light intensity on BAS-PPE PFETs at varying gate biases (a) $I_{DS}$ versus light intensity and (b) $I_{\text{light}}/I_{\text{dark}}$ ratio versus light intensity.
Comparing the data at $V_{GS}$ of -40 V, 0 V and 40 V, the highest $I_{\text{light}}/I_{\text{dark}}$ ratio occurs at zero gate bias. The $I_{\text{light}}/I_{\text{dark}}$ ratio reaches as high as about 6000 at an incident light intensity of 4 µW. The $I_{DS}$ under light illumination is actually composed of three current components: photogenerated current + injection current + thermal current, while dark current is composed of only injection and thermal generation. The highest $I_{\text{light}}/I_{\text{dark}}$ ratio occurs at zero gate bias because both carrier injection and thermal generation have the smallest contribution at this bias, so the percentage of photogeneration reaches a maximum in this case. The $I_{\text{light}}/I_{\text{dark}}$ ratio is lowest for 40 V gate bias due to the elevated dark current.

In conclusion, cross-conjugated polymer BAS-PPE allows a successful engineering of HOMO level to suit hole injection, which ensures its performance as a p-type PFETs. In addition, BAS-PPE PFETs are greatly light sensitive where a much larger $I_{DS}$ is measured under light illumination than under darkness. Gate bias still modulates $I_{DS}$ in the presence of incident light, but the dependence of $I_{DS}$ on the gate bias is weakened with the increase of incident light intensity. The weaker effect of $V_{GS}$ at higher light intensities can be explained by the large amount of photogenerated carriers outside the channel. BAS-PPE is a relatively poor conductor under darkness, so the influence of thermal generation on measured $I_{DS}$ can surpass that of injected charges. It is observed that not only $I_{DS}$, but also the ratio of $I_{\text{light}}/I_{\text{dark}}$, increase with light intensity. Comparing the data at $V_{GS}$ of -40 V, 0 V and 40 V, it is found that the highest $I_{\text{light}}/I_{\text{dark}}$ ratio occurs at zero gate bias, due probably to the lowest dark current at this point among the three gate bias.
CHAPTER 6

CONCLUSIONS

In this work, techniques to improve the performance of PFETs by using pulsed plasma polymerized (PPP) insulator films with high dielectric constant were extensively explored. The operating mechanism of PFETs, especially the electric field dependence of mobility, was studied. The application of PFETs as light sensors was also demonstrated.

6.1 PPP insulator films

Currently more attention of PFETs research focuses on improving their mobility. However, for PFETs to be adopted in real-life application, their driving voltage is of great concern. Our strategy to reduce the driving voltage is to use gate dielectrics with a high permittivity, and at the same time keep the gate dielectric material compatible with subsequent polymer processing. Pulsed plasma polymerization was chosen because it is suitable for large area deposition in one simple step, with concurrently good control of thickness in the desired range ($\leq 200$ nA).
In the early stage of this study, allylamine was used as the monomer based on previous experience of the Timmons team with successful deposition of polymerized allylamine by pulsed plasma. It was found that a heat treatment during deposition elevates the dielectric constant of the resulted polymer film, but the magnitude of improvement is too small to fulfill the purpose. The first goal for this study is to find a polymer insulator which has a dielectric constant higher than that of SiO$_2$. SiO$_2$ is the most popular gate dielectric in MOSFETs, and often adopted in PFETs when only the properties of the polymer semiconductor are the prime interest of the study. However, SiO$_2$ should be eliminated from PFETs because it is rigid, which is contradictory to the primary application of PFETs, namely flexible polymer electronics. To be a qualified replacement of SiO$_2$, the new polymer gate insulator is definitely desired to possess a dielectric constant higher than 3.9. In polymerized allylamine films, the dielectric constant of as-deposited films was 3.0 while that of the heated sample was still only 3.5. To achieve a large jump of the dielectric constant, a new approach other than just a heat treatment has to be pursued.

The new approach taken in the second phase of this study is to use a monomer with high polarizability. The dielectric constant of a material is higher if it has high polarizability. The exact polarizability is tedious to calculate with too many unknowns, but the polarizability of a molecule can be roughly estimated by summing up the tabulated polarizability of the functional groups in the molecule. Therefore, dichloromethylsiloxane (DCTMDS) was chosen in this work. DCTMDS contains –Cl groups, which has high tabulated polarizability. The experimental results proved that polymerized DCTMDS have high dielectric constants. Polymerized DCTMDS films
have dielectric constants in the range of 7 to 10, depending on varying deposition conditions such as duty cycle.

With the dielectric constant reasonably high, the large leakage current through the polymerized DCTMDS films prevent it from being used as a gate insulator. This problem was mostly solved by post-deposition annealing. With the optimum annealing temperature in the range of 150 to 200°C, the leakage current can be reduced an order of magnitude in samples annealed in this temperature range versus as-deposited samples. Temperatures lower than this range are less effective, while higher than this range will overheat the sample and damage the film. Films heated at 300°C and above have low breakdown voltages and terrible leakage.

6.2 Field dependent mobility in polythiophene FETs

One feature of polymer semiconductors is that the mobility of charge carriers in the channel is electric field dependent. In this work, it is observed that the mobility in polythiophene FETs changes not only with gate bias, but also source-drain bias. The gate field dependence of mobility was revealed by the increase of mobility with more negative gate bias. The relationship between field effect mobility and gate bias follows a power law, as predicted by the theoretical study for amorphous organic semiconductors described by Horowitz et al. [36]. The variation of longitudinal electric field (across source and drain) was accomplished by applying the same level of source-drain voltage to devices with varying channel lengths ranging from 7 µm down to 1 µm. PFETs with smaller channel lengths have higher longitudinal electric field than devices with larger channel length at the same source-drain bias. It turns
out that the mobility in polythiophene obtained a large increase once the longitudinal electric field exceeded $10^5 \text{ V/cm}$. High longitudinal electric fields even enhance the dependence of the field effect mobility on gate bias. Another observation in this work is that the drain current gradually loses its saturation as the channel length shrinks, similar to short channel effect in inorganic FETs, only that in PFETs, the short channel behavior occurs at larger channel length than in inorganic FETs.

6.3 Light sensors based on BAS-PPE FETs

It was observed that the conductance of BAS-PPE FETs increases drastically upon the illumination of light. The light-current over dark-current ratio reaches as high as 6000 at an incident light intensity of 4 $\mu \text{W}$. The high drain current was obtained during illumination due to the photo-generated electron-hole pairs. The gate bias has weaker control over the drain current during illumination because it does not affect the electron-hole pairs generated in the bulk outside of the channel. The dark-current has its lowest value in depletion region, when residual doping and thermal generated charge carriers are repelled from the BAS-PPE/insulator interface. Due to the low base current, the highest light-current over dark-current ratio usually occurs in the depletion mode. The magnitude of the drain current, as well as light-current over dark-current ratio, increases with incident light intensity.

Overall, the work presented here explored the working mechanism of PFETs and sought ways to improve their performance. The information described in this dissertation can serve as the study of polymer electronics for further progress in the field of large-area flexible electronics.
6.4 Future studies

6.4.1 Further studies on high performance gate dielectrics

To evaluate the performance of FETs, mobility and ON/OFF ratio are the two criteria used most often. The carrier mobility in PFETs is largely dependent on the properties at the insulator/polymer interface. A smooth surface of the gate dielectric is beneficial to improving mobility. At the same time, the leakage through the gate dielectric is expected to be as low as possible so that the FETs can exhibit a high ON/OFF ratio.

Previous work showed that PPP DCTMDS films have high dielectric constants and can work successfully as the gate insulator in PFETs, but mobility and ON/OFF ratio still need to be improved. Therefore, low leakage and smooth surface need to be achieved simultaneously in PPP DCTMDS films, by adjusting the duty cycle and other parameters during deposition.

Mobility in PFETs can also be improved by introducing ordering in the electro-active polymer. Though mechanical rubbing is one of the most often used techniques, it introduces damage to the device and roughens the interface of semiconductor/insulator where the channel resides. Therefore, self-organization is more preferable in terms of enhancing mobility. As in P3HT FETs, the surface of an SiO$_2$ gate dielectric can be treated with HDMS, which promotes self-organization and at the same time, does not impair the surface smoothness.

In addition to eliminating electrical leakage through the gate dielectric, the ON/OFF ratio can also be enhancing by de-doping the polymer semiconductor. One example is that P3HT can be de-doped by depositing a layer of SiO$_x$ on its surface.
Polymer semiconductors are often un-intentionally doped due to the residue from chemical synthesis and/or impurities in the test environment. De-doping can remove the charge carriers in the bulk of PFETs, so that reduce leakage through the bulk.

6.4.2 Staggered versus coplanar PFETs

PFETs are often built in two configurations: staggered and coplanar (Fig. 2.10). The processes for building staggered and coplanar PFETs are different. In a staggered configuration, the source and drain contacts are deposited on top of the semiconductor polymer, normally by thermal evaporation through a shadow mask. On the other hand, the contacts are deposited before the semiconductor polymer is applied in a coplanar configuration. The published body of work all shows that the staggered configuration induces a lower contact resistance in PFETs and OFETs. The common explanation given is that the staggered configuration has a larger effective contact area than the coplanar configuration [46]. However, none of this work considered the effect of hot metal impinging upon soft organic films during thermal evaporation of the contacts in a staggered configuration. The semiconductor polymer under the contacts can easily be melted, creating an interpenetrating network of polymer and metal, which will change Schottky-like contacts to Ohmic contacts. Conversely, the polymer is spin-coated onto preformed contacts in the coplanar configuration. Therefore, much less chemical reaction is expected at the metal/polymer interface in a coplanar than configuration. We speculate that the metallization process may be the principle reason for a lower contact resistance in the staggered configuration rather than the larger contact area. To test this hypothesis,
PFETs in a staggered configuration need to be built while avoiding any thermal evaporation of contacts. In that way, the major effect which lowers the contact resistance can be verified. The method proposed uses a cold deposition process of the source/drain top contacts by transferring preformed metal contacts onto a freshly applied electroactive layer using stamping techniques. This needs further investigation.

6.4.3 Gate dielectric for ambipolar PFETs

Recent development in PFETs demonstrated that many polymer semiconductors which were previously believed to exhibit only p-type field-effect conduction can actually support both hole and electron transport. The failure of n-type conduction in those polymers is now suspected to be the surface properties of the gate dielectric materials in addition to the polymer semiconductor itself. By using gate dielectric materials with a low electron affinity, n-type behavior was observed by Zaumseil et al. in even P3HT [160], which was considered a p-channel semiconductor only for so many years. Dielectric materials, such as a benzocyclobutene derivative (BCB), produced via chemical synthesis have also been reported by Chua et al. supporting n-channel polyfluorene FETs [161]. Chua et al. pointed out that the previously elusive n-type behavior was due to the trapping of electrons by electrochemically-active groups. For example in commonly used SiO₂ dielectric, the hydroxyl groups formed on the dielectric surface in the presence of water vapor were the electron traps that ruined the n-channel conduction. To take advantage of this inspiring opportunity to achieve ambipolar PFETs by modifying the
properties of gate dielectric, it is worthwhile applying the technology for dielectric films by using monomers with low electron affinity, such as aromatic monomers. PPP deposition is uniquely positioned due to the flexibility on the choice of monomers and simplicity of one-step process.
APPENDIX A

A.1 Polymer solution preparation

1. Clean 10 ml amber glass bottle with DI water, acetone, methanol, isopropynol. Leave the bottle upside down for the solvents to dry.

2. Weigh the bottle together with an Al cap and a PTE liner and record the weight.

3. Transfer the bottle and lined cap to the spinner glovebox through antechamber.

4. Put a small amount of the polymer into the amber bottle.

5. Clamp the lined cap on the amber bottle.

6. Take the capped amber bottle out and weigh it. The difference of the weight before and after the bottle capped is the weight of the polymer in the bottle.

7. Transfer the capped bottle back to the spinner glovebox.

8. Draw the solvent from the solvent bottle with a syringe and inject the solvent to the capped amber bottle. The amount of solvent injected into the amber bottle is determined by the desired weight/volume ratio. For example, to prepare a solution with 2% concentration with 80 mg polymer, the volume of solvent needed is

\[(80 \text{ mg}/4 \text{ ml}) \times (1 \text{ g}/1000 \text{ mg}) = 2\% \text{ g/ml}\]

9. Heat the solution if the polymer does not dissolve well. It is better to keep the heating temperature under 100 °C to avoid thermal degradation of the polymer. Longer heating time is required for the polymers hard to dissolve.
A.2 Operation of antechamber & Trash can

Samples and tools are transferred in and out gloveboxes or from one glovebox to another through antechambers. There are two small antechambers, each is attached to a glovebox. There is also a big antechamber between the two gloveboxes in CL319. This big antechamber can transfer big substances in and out or between gloveboxes.

To transfer samples and tools from outside to inside gloveboxes, the operation should be:
1. Open the outer door of the antechamber.
2. Put the transferred substance in the tray of the antechamber.
3. Tighten the outer door of the antechamber.
4. Evacuate/Refill antechamber three times to get rid of air remaining in the antechamber and backfill it with nitrogen gas.
5. Open the inner door of the antechamber.
6. Take transferred substance out of the tray.
7. Tighten the inner door of the antechamber.

Even after you have already tightened the doors at atmospheric pressure, the doors feel loose when the antechamber is under vacuum. Don’t try to tighten the doors further when the antechamber is under vacuum. Otherwise the door may burst out by the extremely high pressure during refill.

To transfer samples and tools from inside the glovebox to the outside, the operation should be:
1. Evacuate and refill the antechamber three times to make sure that the antechamber is purged of residual moisture and oxygen before you open the inner door to the glovebox.

2. Open the inner door of the antechamber.

3. Put the transferred substance in the tray in the antechamber.

4. Tighten the inner door of the antechamber.

5. Open the outer door of the antechamber.

6. Take transferred substance out of the tray.

7. Tighten the outer door of the antechamber.

8. Evacuate and refill the antechamber three more times in case the next operator forgets to do so before he/she opens the inner door of the antechamber.

The Evacuate and refill operation for small antechambers proceeds with a black knob, which operates the bell valve, right under each small antechamber. There is also a pressure meter above each small antechamber to monitor the pressure in the antechamber during purging.

The large antechamber between the two gloveboxes has a different Evacuate/Refill procedure. Instead of a knob, the Evacuate/Refill is controlled by k3 (autom./vacuate antech.) on the OP17 display panel. Follow the messages on the display to proceed to the evacuate and refill operation for the large antechamber.

Trash cans are designed to remove trash from the gloveboxes. There is a trashcan in the bottom of each glovebox. The operation of the trashcan occurs exactly like the
operation for transferring substances from inside to outside gloveboxes through the antechamber.

A.3 Operation of thermal evaporator in glovebox

1. Vent the evaporator chamber to atmosphere pressure.

2. Open the front door of the evaporator. A door control button at the bottom right hand corner under the glove box controls the seal of the door. When the button is positioned “in”, the door is sealed. To release the seal, push the white button to “out” position. Then the front door can be opened by sliding it to the left.

3. Load samples.

4. Close the front door of the evaporator and seal it by pushing the door control button to “in” position.

5. Press “cycle” button under chamber pressure display to draw a chamber vacuum (base pressure is required to be at least in the order of $10^{-6}$ Torr).

6. On crystal thickness monitor controller, input layer information. There are three crystal monitors in the evaporator chamber. The left thickness display shows information of crystal monitor 1 & 2, and the right thickness display shows information for crystal monitor 3.

7. Push the “run” button at the right of thickness display to reset the thickness to zero.

8. Select the evaporation source. There are six sources in the evaporator chamber. There are two source heater controllers. The left heater controller controls sources 1, 2, & 3; while the right heater controller controls sources 4, 5, & 6.

9. Turn the tension knob to LT and see green light on. Never use HT.
10. Record the base pressure and make sure the selected source is covered by the shutter.

The shutters are controlled by two source shutter controllers. The left source shutter controller controls shutters 1, 2, & 3, while the right source shutter controller controls shutters 4, 5, & 6. Shutters 1 & 2 are controlled by “SS1” button in the left source shutter controller. When SS1 is in the “out” position, source 1 is covered and at the same time source 2 is open, and when SS1 is in the “in” position, source 2 is covered while source 1 is open. The SS2 in the left source shutter controller controls only shutter 3. When SS2 in the left source shutter controller is “out”, source 3 is covered and when SS2 is “in”, source 3 is open. The SS1 button in the right controller controls only shutter 4. When SS1 in the right source shutter controller is “out”, source 4 is covered and when SS2 is “in”, source 4 is open. The SS2 button in the left controller controls shutters 5 & 6. When SS2 is in “in” position, source 5 is covered and at the same time source 6 is open, and when SS2 is in “out” position, source 6 is covered while source 5 is open.

11. Ramp up current knob slowly at a few steps and observe the chamber pressure change. The evaporator chamber pressure will go up once it is heated so impurities on the surface of the source evaporate. First keep the shutter closed to catch the evaporated impurities and wait for the chamber pressure to drop back to the base pressure.

12. Open the source shutter after the chamber pressure drops back to the base pressure and ramp up the current knob a little further to activate the evaporation. Once the evaporation is activated, ramp down the current knob a little to avoid the deposition
rate from getting too high suddenly. Adjust the current knob while watching the depositon rate display to reach a reasonable deposition rate.

13. Once the deposition reaches the desired thickness, close the source shutter and ramp down the current knob at the same time, followed by turning the tension knob back to “O” and the source selection knob to “OFF”.

14. Repeat step 6 to 13 for the other metal layers.

15. After finishing all the layers, wait about 5 min for the sources to cool down.

16. Vent evaporator chamber to atmospheric pressure with dry nitrogen.

17. Open the front door of the evaporator and take samples out.

18. Close the front door.

19. Press “cycle” button to draw chamber vacuum. Make sure to see the “fine pumping” message on the display before leaving the system.

A.4 C-V measurement of MIS structure using MDC software

1. Turn on both Agilent 4156 semiconductor parameter analyzer and 4284 LCR meter.

2. Insert hard key to the computer in CL316 (the hard key is normally already on the CPU).

3. Open the MDC CV measurement program on the computer from start -> all programs -> CSM-WIN C-V Plotter.

4. No password is set for the program, so click “continue” button without input any password.
5. Window pop up displaying “Connect meter 4284 to device under test”, just click the “Ok” button.

6. A list of analyze programs will show up, choose “Engineering MOS C-V tests” from the screen.

7. “MOS-mode” window will pop up, choose “MOS C-V Plotting”.

8. “MOS-function” window will pop up, choose “Edit Test Recipe”.

9. According to your needs, pick one of the .MCV file and open it.

10. Input all the test parameters as you desire, then click the “Save This Recipe” button and save this recipe to your own folder.

11. Now on the “MOS-function” screen, click “Start Test”.

12. “Sample” window pop up, input your sample number and click “measure” to perform the measurement.
REFERENCE


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