SI-BASED QUANTUM FUNCTIONAL TUNNELING DEVICES AND THEIR APPLICATIONS TO LOGIC AND OTHER FUTURE CIRCUIT TOPOLOGIES

DISSERTATION

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By

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ABSTRACT

The aim of this Ph.D. project is to develop high performance Si-based tunneling structures for integrated circuitry applications. In this work, three kinds of Si-based tunneling structures, namely, Si-based resonant interband tunneling diodes (RITD) for mixed signal integrated circuit and low power digital applications, Si-based backward diode for millimeterwave detection applications, and fabrication of Ge quantum dots for single electron transistor (SET) and quantum-dot cellular automata (QCA) applications, were studied.

Since peak-to-valley current ratio (PVCR) is a very important figure-of-merit for tunnel diodes, one of the primary tasks in this work is to improve the PVCR of Si-based RITDs. The key to obtain a higher PVCR is to reduce the excess current component while maintaining the desired interband tunneling current. Two approaches were taken to improve the PVCR: The first one is to modify the RITD structure by growing SiGe layers cladding the B δ-doping plane to suppress the B diffusion; The second approach is to use spike annealing to limit the motion of dopant profile. Both of these two approaches result in improved PVCR and was experimentally determined to be successful. The optimized structure with cladding layer was used as the template for later RITD growths.

Peak current density, $J_p$, is another important parameter for circuit performance. Both high and low $J_p$ are separately desirable for different circuit applications. Since
tunneling current is exponentially related to the tunneling barrier thickness, a study of the spacer thickness effect on $J_p$ was conducted to explore the range over which the Si-based RITD can reach. The dependence of other performance figures, such as PVCR and voltage swing, on spacer thickness were also studied. The highest PVCR of 3.8 was obtained using a 6 nm tunneling spacer thickness. A record high $J_p$ of 151 kA/cm$^2$ is obtained by using a 3 nm spacer thickness. A 16 nm spacer yields the lowest recorded $J_p$ of 20 mA/cm$^2$. The $J_p$ experimentally measured for Si-based RITD in these studies spans nearly seven orders of magnitude. The spacer thickness affects the voltage swing in the same way as it affects PVCR. Furthermore, it affects the voltage swing by changing the slope of the excess current on a semi-log scale.

One of the attractive features of tunnel diodes is its inherent multi-state behavior. Vertically integrated npnp Si-based RITD pairs were successfully built with double negative differential (NDR) regions under forward bias. Tri-state logic was demonstrated using the vertically integrated RITD pair.

A unified model which combines both the small and large signal models of an RITD grown on a SOI wafer was developed. The small signal equivalent circuit was obtained by fitting the RF measurement results. The large signal model was obtained by fitting the DC I-V characteristics using empirical equations.

Radiation-effects experiments were performed on Si-based RITDs. The observation of a strong contribution of $\Delta I_t$ to $\Delta I$ in proton-irradiated SiGe RITDs demonstrates their operation in reduced dimension, distinguishes them from Esaki diodes and confirms the existence of a true resonant interband tunneling state.

A commercial Si$_{0.8}$Ge$_{0.2}$ virtual substrate was used to grow Si-based RITDs. There are two advantages by using Si$_{0.8}$Ge$_{0.2}$ substrate: (1) the tunneling probability can be
enhanced by increasing the Ge content in the spacer without exceeding the critical thickness; (2) a tensilely strained Si layer can be grown, which provides flexibility in engineering the band diagram of the overall RITD. To take advantage of the tensile strain in the Si layer, structures with Si layers which clad the P $\delta$-doping plane and structures with barriers outside the tunneling region were studied. However, due to the large surface roughness of the commercially available SiGe substrate, the RITDs grown on SiGe substrates exhibit inferior performance to RITDs on conventional Si substrates. Better performance is expected by using better SiGe substrates with a smaller surface roughness.

Si-based backward diodes were grown by LT-MBE. Post-growth annealing removes the point defects and leads to dopant diffusion. There exists an optimal annealing temperature for the highest curvature coefficient at zero bias. The high sensitivity and SiGe HBT compatibility of the Si-based backward diodes make them very attractive for zero-bias millimeter-wave detector applications.

The oxidization of Si and Si/SiGe nano-pillars patterned by electron beam lithography (EBL) were studied. The Si pillars were successfully oxidized using an RTP 600S system. The TEM image clearly shows a crystalline Si pillar embedded within a SiO$_2$ casing. The Si/SiGe nano-pillars were oxidized using a conventional furnace. The swelling during oxidization could also lead to large lateral strain on the nano-pillars and cause some breakage. However, the QDs survived that were closely packed pillars could readily be utilized as a QCA chain.

Overall, the work presented here was to extend Si technology, as articulated on the International Technology Roadmap for semiconductors, and can serve as a guide for the future exploitation of Si-based RITDs.
This is dedicated to those I love.
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CHAPTER 1

INTRODUCTION

The aim of this Ph.D. dissertation is the development of epitaxially grown tunneling structures and circuits on a Si platform. It has been demonstrated that tunneling structures, that exhibit a negative differential resistance (NDR), such as resonant tunnelling diode (RTD)/transistor logic, and realized to date primarily in III-V material systems, enhances any transistor technology [124],[125] by reducing the number of components per circuit function, increasing speed, and lowering power consumption. Given the fact that Si and SiGe still hold a much larger semiconductor market share than III-V semiconductors, it is desirable to transfer NDR technology to a Si platform. Since the development of Si-based resonant interband tunneling diodes (RITD) [113] that can potentially be integrated with CMOS transistors for highly functional tunnel diode-transistor circuits, numerous experimental attempts have been made to improve RITD performance [111],[109],[140], [29],[60],[142], [37],[34],[101]. However, the Si-based RITD has yet to be integrated with CMOS and/or heterojunctio bipolar transistor (HBT). The main body of this Ph.D. dissertation is to improve the performance of Si-based RITD further and develop a comprehensive model to foster circuit designers to incorporate NDR devices into their toolbox. Efforts were also spent in developing the Si-based backward diode for millimeter wave detection applications.
The fabrication of Ge quantum dot by oxidizing SiGe nano pillars for SET (Single Electron Transistor) and QCA (Quantum-dot Cellular Automata) application was also studied.

The remainder of this dissertation is organized as follows.

Chapter 2 will describe the performance metrics of tunnel diodes, the theory behind quantum mechanical tunneling, the operating theory of various tunnel diodes (Esaki diodes, RTDs, and RITDs). The current status of Si-based epitaxial grown tunnel diodes will be summarized. The last section will discuss the background and theory related to the growth and processing. Chapter 3 will present the digital and microwave circuit application of tunnel diodes.

Chapter 4 will present two studies to raise the peak-to-valley current ratio. In the first study, the RITD structure was optimized, while in the second study, the post-growth annealing process was optimized. Chapter 5 will present studies to both maximize and minimize the peak current density for two different types of circuit applications. A low power one-transistor tunnel diode SRAM was demonstrated using the low current density RITD developed. In chapter 6, vertically integrated RITDs showing two successive NDR regions under the forward biasing condition are presented. Subsequently, tri-state logic was demonstrated. Chapter 7 presents a comprehensive model which combines both the small and large signal models of RITDs. The microwave performance of RITDs is also discussed. Several simple RITD circuits are simulated using this model. Chapter 8 presents a radiation experiment on the Si-based RITD, which provides experimental evidence for resonant tunneling as opposed to Esaki-like tunneling.
Chapter 9 presents RITDs grown on SiGe substrate. The ability to engineer the band offsets by strain modification was also employed.

In chapter 10, Si-based backward diodes for zero-biased millimeter wave detection are presented.

Chapter 11 presents the fabrication of Ge quantum dot by oxidizing Si and SiGe nano-pillars.

Chapter 12 summarizes the conclusions of the experimentation, and provides suggestions for future research.
CHAPTER 2

INTRODUCTION OF TUNNEL DIODES

This chapter gives a brief introduction to tunnel diodes. Section 2.1 discusses the tunnel diode I-V characteristics and its small signal model. In Sect. 2.2, the tunnel diode’s performance metrics are defined, as well as the theory of tunnel diodes. Sect. 2.3 will describe the operation of three variations of tunnel diodes: (i) Esaki tunnel diodes, (ii) resonant tunneling diodes (RTDs), and (iii) resonant interband tunneling diodes (RITDs). Most of this section will discuss the Esaki tunnel diodes generated by early work in the 1960’s following the discovery by Leo Esaki in 1958, because both Esaki diodes and RITDs rely on interband tunneling transitions. In Sect. 2.3, the experimental realization of the Si-based RITD developed by Rommel et al is presented. Sect. 2.3 reviews the current status of epitaxial grown Si-based tunnel diode.

2.1 Tunnel Diodes I-V characteristics and Small Signal Model

The current-voltage (I-V) characteristic of a typical tunnel diode is shown in Fig. 2.1 [135]. Compared to the I-V characteristic of a conventional diode, there exists an ‘n-shaped” NDR region in its forward biasing condition. Beyond the peak voltage, $V_p$, there is a sudden drop in the current. This drop in current continues until the
valley voltage, $V_v$ is reached. Beyond $V_v$, the current starts to increase again. The second voltage, $V_s$, is defined as the voltage at which the current reaches $I_p$ again. Clearly, there are three regions in the forward biased I-V characteristics, which are (1) first positive differential resistance (PDR) region ($0 < V < V_p$), (2) negative differential resistance (NDR) region ($V_p < V < V_v$), (3) second positive differential resistance (PDR) region ($V_v < V$), respectively.

Figure 2.2 shows the small signal model of a tunnel diode. It consists of a junction conductance $g_d$, junction capacitance, $C_d$, series resistance, $R_s$, and series inductance, $L_s$, which is similar to the one of a conventional diode, except for a negative $g_d$ when the tunnel diode is biased in its NDR region.
2.2 Tunnel Diodes Performance Metrics

Since tunnel diodes have many applications, there are many performance metrics to characterize tunnel diodes for various applications. In general, the performance metrics can be classified into two categories, ones relating to the I-V characteristics and ones relating to the tunnel diode switching speed.

2.2.1 Performance Metrics Related to I-V Characteristics

This section defines the performance metrics related to tunnel diode I-V characteristics.

Peak-to-Valley Current Ratio (PVCR)

The most important parameter used to distinguish the tunnel diodes from the conventional diode is the peak-to-valley current ratio (PVCR), which is defined by Eqn. 2.1. The PVCR of a tunnel diode should be greater than 1. A substantially larger PVCR is desirable for digital applications.
\[ PVCR = \frac{I(V_p)}{I(V_c)} \]  

(2.1)

**Peak Current Density** \((J_p)\)

The peak current density, \(J_p\), is another important parameter of tunnel diode performance. \(J_p\) is defined by Eqn. 2.2.

\[ J_p = \frac{I_p}{A} \]  

(2.2)

where, the value \(A\) is the cross sectional area of the device. For high speed circuits applications, high \(J_p\) is desired to switch the charge quickly, while for low power circuit applications, a low \(J_p\) is ideal to reduce power consumption.

**Voltage Span**

The voltage span \((V_v - V_P)\) is used to characterize the width of the NDR region. A large voltage span is preferred for oscillator applications, since the maximum oscillation power is proportional to the voltage span, as will be discussed in Sect. 3.3.1. However, a large voltage span will slow down the switching speed, as will be shown in Sect. 2.2.2. The value of the voltage span can be a function of the series resistance, \(R_s\) at high currents, because the voltage dropped across \(R_s\) become significant with a large current. In essence, \(R_s\) can shift \(V_P\) to higher voltages more so than the magnitude of \(V_v\) due to the difference in current. A large enough \(R_s\) can actually make \(V_P\) equal to \(V_v\) with a corresponding zero voltage span. Further increasing \(R_s\) will result in a phenomena called hysteresis, i.e., the valley position actually becomes
tucked under the peak position, but due to restrictions in measurements with parameter analyzers, the position of the valley when sweeping forward-only is identified incorrectly. The true valley voltage can only be revealed by sweeping backward.

**Voltage Swing**

Voltage swing, which is defined as $V_S - V_P$, characterizes the broadness of the valley region. Compared to voltage span, the value of the voltage swing is an intrinsic value which will not be affected by the series resistance $R_s$, since the voltage dropped across $R_s$ is cancelled out. A large voltage swing will lead to a large separation between the two stable states for digital applications, hence a large noise margin can be achieved. However, it will unfavorably increase the power consumption and reduce the switching speed.

**Current Span**

Current span is defined as $I_P - I_V$. A large current span will result in fast switching speeds and large oscillating powers.

**Junction Resistance**

Junction resistance is the slope of the I-V characteristics. This value at zero bias is of particular importance. In some applications where the tunnel diode is biased at 0 $V$, such as envelope detectors, a value matched to the source impedance is desired to reduce the mismatch loss. In some applications where the tunnel diode is reversed biased and serves as a small resistor connecting two opposite polarity devices, a very small value is desired to reduce the voltage drop from the parasitic resistance.
Curvature Coefficient

To characterize the second order nonlinearity of the tunnel diode I-V curve, the curvature coefficient $\gamma$ is defined as

$$\gamma = \frac{d^2I/dV^2}{dI/dV}$$  \hspace{1cm} (2.3)

In applications where the quasi-square-law behavior of the tunnel diode I-V characteristics is used, such as for mixers and detectors, the curvature coefficient is an important parameter. A larger curvature coefficient is preferred for better performance.

2.2.2 Performance Metrics Related to Speed

Speed of tunnel diodes can be characterized in both the time domain and frequency domain. The speed index is a time domain metric and it is used primarily in digital applications. The negative-resistance cutoff frequency characterizes the tunnel diode in the frequency domain, and it is useful for RF applications.

Speed Index

The switching time of a tunnel diode is determined by the available charging current as denoted by the load line shown in Fig. 2.3, and the change of total charge between the initial state and final state. Assume a constant junction capacitance, the switching time can be given as

$$\tau = \int_{V_P}^{V_F} \frac{C(V_F - V_P)}{I_S(V) - I_{TD}(V)} dV$$  \hspace{1cm} (2.4)

where $I_S(V)$ represents the current of resistive load and $I_S(V)$ represents the tunnel diode current.
Equation 2.4 can be simplified using a lower bound and it can be written as

\[
\tau = \frac{C(V_F - V_P)}{I_P - I_V} = \left[\frac{C}{I_P}\right] \frac{V_F - V_P}{1 - 1/PVCR} \tag{2.5}
\]

The factor \(I_{peak}/C_j\) is called the speed index, which is a widely used figure-of-merit. Eqn. 2.5 also shows that while PVCR is important, increasing the PVCR beyond 3 does not substantially increase the speed [123].

**Negative-resistance Cutoff Frequency**

The input impedance of the tunnel diode can be calculated from Fig. 2.2 as

\[
Z_{in} = \left\{R \pm \frac{G}{G^2 + \omega^2 C^2}\right\} + j\omega\left\{L - \frac{C}{G^2 + \omega^2 C^2}\right\} \tag{2.6}
\]

When biased in its NDR region, the real part of the impedance is negative only if

\[
R < \frac{|g|}{|g|^2 + \omega^2 C^2} \tag{2.7}
\]
which can be re-written as

\[ f < f_c = \frac{|g|}{2\pi C} \sqrt{\frac{1}{R|g|}} - 1 \]  

(2.8)

where \( f_c \) is called the negative-resistance cutoff frequency, because the diode will not exhibit negative resistance above this frequency. Therefore, \( f_c \) sets an upper frequency limit for RF applications.

Note, there is a frequency at which the reactive part of the device impedance is zero, which is called the self-resonant frequency \( f_r \). It can be calculated using the following formula:

\[ f_r = \frac{1}{2\pi} \sqrt{\frac{1}{LC} - \frac{|g|^2}{C^2}} \]  

(2.9)

Typically, \( f_c \) is less than \( f_r \). If \( f_c \) exceeds \( f_r \), then spurious oscillations may occur.

### 2.3 Variations of Tunnel Diodes

A variety of tunnel diode configuration will now be discussed. Each design has its own advantages and disadvantages.

#### 2.3.1 Esaki Tunnel Diodes

To build an Esaki tunneling diode, both sides of the p-n junction require degenerate doping to form an abrupt junction with a sufficiently narrow depletion region to permit quantum mechanical tunneling to take place. The band diagram and I-V characteristic of an Esaki tunnel diode under various biasing conditions are shown in Fig. 2.4. When the diode is in its reverse biasing condition as in Fig. 2.4 (a), electrons tunnel from occupied states in the p-side valence band into available states in the n-side conduction band generating a large reverse tunneling current. When there is no bias voltage across the junction as shown in (Fig. 2.4 (b)), there is no
current, because there are no available states for carriers to tunnel into. When the
forward bias is small, electrons from occupied states in the n-side conduction band
tunnel into unoccupied states in the p-side valence band, leading to a forward tun-
neling current (Fig. 2.4 (c)). The tunneling current continues to increase with bias
until the conduction and valence bands uncross. Once this condition is reached (Fig.
2.4 (d)), the probability of tunneling abruptly decreases, leading to the onset of a
negative differential resistance region (NDR). Finally, when the bias approaches the
built-in potential, the diffusion current starts to dominate the I-V characteristic, once
again leading to an increase in current.

Figure 2.4: Electrostatic band diagram of an Esaki tunnel diode under various biasing
conditions. Adopted from Hall [56].
As shown in Fig. 2.5, the I-V characteristic of an Esaki diode consists of three current components: a band-to-band tunneling current, an excess current, and a thermal diffusion current.

**Band-to-band Tunnel Current**

According to Esaki’s theory, there are tunneling currents flowing in both directions in a Esaki junction. The tunneling current from the conduction band to the valence band can be expressed as

\[
I_{c\rightarrow v} = A \int_{E_c}^{E_v} f_c(E)\rho_c(E)[1 - f_v(E)]\rho_v(E)T_{c\rightarrow v}dE
\]  

(2.10)
where \( f_c(E) \rho_c(E) \) is the number of electrons in the conduction band, \([1 - f_v(E)] \rho_v(E)\) is the available, unoccupied states in the valence band, \( T_{c\rightarrow v} \) is the probability for tunneling from the conduction band to an identical energy level in the valence band.

Similarly, the tunneling current from the valence band to the conduction band is

\[
I_{v\rightarrow c} = A \int_{E_c}^{E_v} f_v(E) \rho_v(E) [1 - f_c(E)] \rho_c(E) T_{v\rightarrow c} dE \tag{2.11}
\]

Thus, under forward-biased condition, the net current is the difference between Eq. 2.10 and Eq. 2.11. At a forward biased voltage \( V(a) \), the current is

\[
I(V_a) = A \int_{E_c}^{E_v} [f_c(E) - f_v(E)] \rho_c(E) \rho_v(E) T_t dE \tag{2.12}
\]

It can be further expressed as

\[
I(V_a) = K \int_{E_c}^{E_v} [f_c(E) - f_v(E)] T_t \sqrt{(E - E_c)(E_v - E)} dE \tag{2.13}
\]

where the Fermi-Dirac distribution function \( f(E) \) is given as

\[
f(E) = \frac{1}{1 + e^{(E-E_f)/kT}} \tag{2.14}
\]

**Excess Current**

The excess current is due to carrier tunneling through energy states within the forbidden gap. Chynoweth theoretically studied the excess current and revealed its exponential nature. Figure 2.6 shows the possible tunneling routes for the excess current. (1) an electron starting at C in the CB might tunnel to level A, from where it can then drop down to D in the VB; (2) the electron could drop from C to an empty level B from where it could tunnel to D; (3) \( C \rightarrow A \rightarrow B \rightarrow D \), where the electron loses its excess energy in an impurity band conduction process from A to
B; (4) a stair-case tunneling and losing energy from C to D. Based on Route 1, i.e., $C \rightarrow A \rightarrow D$, Chynoweth derived the excess current as follows:

$$I_x = A \times D_x \exp\left\{\frac{-\alpha_x \times W \times e^{0.5}}{2}[E_g - eV + 0.6e(V_n + V_p)]\right\}$$ \hspace{1cm} (2.15)$$

where $A$ is a voltage and temperature independent prefactor; $\alpha_x$ is a material constant; $V_n$ is the potential difference between the Fermi level and the bottom of the CB; $V_p$ is the potential difference between the Fermi level and the top of the VB; $W$ is the depletion region width; $D_x$ is the density of states in the band gap at a corresponding energy; $V$ is the forward bias.

The origins of the available states in the forbidden gap can be (1) crystal defects, such as dislocations, point defects; (2) unwanted chemical impurities; (3) dopant pairs; and (4) surface states.

Crystal defects (disorder) play an important role in determining the amount of excess current. Researchers in the 1960’s first discovered increases in the excess current during irradiation studies of Ge and Si Esaki diodes [39, 85]. The increase in
excess current for a given voltage was found to depend linearly on the dose of radiation bombardment [85]. Heat treatments of these diodes following the ion bombardment were found to suppress the induced excess current, eventually returning the diode to its original I-V characteristic.

**Thermal Diffusion Current**

This is the normal diode diffusion current, which can be given as:

\[ J_{th} = I_{th} \times \exp\left(\frac{v}{nkT}\right) - 1 \]  \hspace{1cm} (2.16)

where \( n \) is the ideality factor.

### 2.3.2 Resonant Tunneling Diodes

The development of non-equilibrium epitaxial processing techniques such as molecular beam epitaxy (MBE) in the 1970’s lead to a novel tunneling structure using primarily the III-V materials system: resonant tunneling diodes (RTD) [145]. The band diagram of a typical double barrier RTD is shown in Fig 2.7 [94]. At zero bias, the resonant tunneling condition is not satisfied, and therefore no current will flow (Fig. 2.7(a)). At some critical bias, the energy of electrons at the electrode coincides with the energy level of confined states in a quantum well, and the diode enters resonance (2.7(b)), in which state resonant tunneling take place, and the current increases with applied bias. For biases beyond the peak voltage (2.7(c)), the diode is no longer in resonance, and an NDR region will be observed. Biases beyond this valley region provide sufficient energy for carriers to surmount the potential barriers on either side of a quantum well (Fig. 2.7(d)), which leads to an increase in forward current. The quantum well is formed by a pair of heterojunctions which produce large offsets in the
conduction band. The magnitude of the band offset creating the quantum well should be large enough to obtain confined quantum states. Note that the RTD symmetry leads to a symmetry of the I-V characteristics in reverse and forward biasing.

![Electrostatic band diagram of an resonant tunneling diode under various biasing conditions.](image)

Figure 2.7: Electrostatic band diagram of an resonant tunneling diode under various biasing conditions. Adopted from Mizuta [94].

The structure presented in Fig 2.7 is an n-type RTD based on electron tunneling. A p-type RTD based on hole tunneling has a structure with a quantum well in the valence band. Since the hole effective mass is much larger than the electron effective mass, the confined states are less defined and broader which leads to significantly smaller PVCR. Therefore, the n-type RTD is the preferred configuration. A number of groups in the early 1990’s investigated Si/SiGe RTDs based on hole transport, but
none of those structures demonstrated NDR above a temperature of 77K. [72], [49]. Ismail et al. [65] reported an n-type RTD showing a PVCR of 1.2 at 300K. Recently, See and Paul [127] fabricated a small area n-type resonant tunneling diodes (RTDs) with strained Si$_{0.6}$Ge$_{0.4}$ potential barriers and a strained Si quantum well grown on a relaxed Si$_{0.8}$Ge$_{0.2}$ virtual substrate. A room temperature $J_P$ of 282 kA/cm$^2$ with a PVCR of 2.43 were recorded for a 55 $\mu$m$^2$ sample.

### 2.3.3 Resonant Interband Tunneling Diodes

A number of methods were suggested by Sweeny and Xu to define quantum wells in an RITD [133]. One type of device uses narrow gap materials to define a type I heterojunction double quantum well. Reports of double quantum well RITDs using InAlAs/InGaAs have demonstrated PVCRs as high as 144, the highest of any existing
tunnel diode technology to date [144]. A second device uses type II heterojunctions to define the quantum well. One example of this structure is an InAs/AlSb/GaSb RITD [33].

A third device incorporates $\delta$-doping planes on both sides of the p-n junction to define the quantum states for the majority carrier, and is essentially a hybrid between an Esaki diode and an RTD. $\delta$-doping planes create triangular potential wells with confined quantum states. III-V RITDs employing this structure have demonstrated PVCRs as high as 5.0 [161]. Rommel et al. developed the first Si-based RITD using this method. A typical Si-based RITD structure is shown in Fig. 2.17.
Figure 2.10: Confinement of quantum states in a triangular potential well due to δ-doping. Adopted from Gossmann [53].

Figure 2.11: Example of a δ-doped p-n junction resonant interband tunnel diode. This is the template which will be used in this dissertation. Adopted from Sweeny [133].
2.4 Growth and Processing Issues of Tunnel Diodes

This section will present the experimental realization of the Si-based RITD developed by Rommel et al.

This section starts with the theory of molecular beam epitaxial growth used to realize the structure proposal. Two mechanisms that occur during MBE growth and which will greatly influence RITD performance will be presented: segregation and diffusion. This section will also present the rationale for developing a post-growth rapid thermal annealing process to reduce the defect density. Dopant diffusion behavior within the spacer will be discussed.

2.4.1 Molecular Beam Epitaxial Growth

Molecular beam epitaxy (MBE) is a non-equilibrium process of growing crystalline semiconductors via the reaction of one or more thermal molecular beams with an existing crystalline surface under ultra-high vacuum conditions [17]. The MBE technique can control the deposition of one atomic layer at a time. Several parameters such as the substrate temperature, the temperature of the individual constituent species, and the duration that mechanical shutters allow flux to impinge on the substrate, govern the growth kinetics. This flexibility of MBE makes it very useful for research and development of nano-scale semiconductor devices.

Fig 2.12 shows the schematic of a simple MBE system. A substrate is mounted on a heating block a fixed distance away from a series of effusion cells which contain the constituent elements. These effusing species may be atomic or molecular and impinge on a crystalline substrate leading to the epitaxial growth as they incorporate into the lattice during growth. The substrate is rotated at a fixed rate to improve growth
Figure 2.12: Schematic Diagram of a molecular beam epitaxy chamber. Several constituent fluxes simultaneously impinge on a substrate. The temperature of the substrate and individual constituents are separately controlled. Adopted from Ghandi [50].

uniformity. Two types of sources are generally used for the effusion cells: Knudsen cells where species either sublimate directly from the solid state or are essentially extracted as a vapor from a molten liquid and electron beam (e-beam) cells.

E-beam sources are typically used for the deposition of materials with high melting points such as Si and Ge. Knudsen cells are generally used for the deposition of dopants in Si MBE. Fig. 2.13 shows a typical Knudsen cell. A charge containing the dopant is placed at the bottom of a crucible, typically boron nitride, graphite or silicon carbide, which is resistively heated until the material begins to evaporate. Dopants with higher melting points, such as B, often require a modified water-cooled high temperature Knudsen cell. Cracker cells are also sometimes employed to liberate
Figure 2.13: Schematic diagram of a Knudsen thermal evaporation cell. Adopted from Sze [136].

P dopants from a GaP charge. Cracker cells can also be used to convert molecular species into elemental fluxes.

Several mechanisms are simultaneously occurring during MBE growth. Two kinetically limited phenomena, segregation and diffusion, are responsible for the redistribution of atoms.

When the number of impurities arriving at the substrate during growth exceeds the equilibrium solid solubility, surface segregation occurs and leads to a buildup of impurities on the growth surface. Doping in Si-MBE at growth temperatures greater than 450 °C is well known to suffer from surface segregation [53]. If segregation is pronounced during growth, the dopant profile broadens and an abrupt profile can not
be obtained. Three theories have been developed to address possible mechanisms for segregation [52]: the rate theory, the theory of Coulomb repulsion, and Fermi-level-pinning-induced segregation.

Atomic species incorporated into the lattice are susceptible to diffusion, which also leads to variations in doping profiles. Fickian laws describe the dopant diffusion behavior, that is, over a fixed time \( t \) and temperature \( T \), on the average, an impurity will be displaced a length of

\[
    l = \sqrt{D t}
\]

where \( D \) is referred to as the diffusion coefficient \((\text{cm}^2/\text{s})\). The quantity \( l \) is known as the diffusion length. For the case of intrinsic diffusion, where the concentration of impurities is relatively small [53],

\[
    D = D_0^{(0)} \exp \left[ \frac{-E_a^{(0)}}{kT} \right] + D_0^{(1)} \exp \left[ \frac{-E_a^{(1)}}{kT} \right] + D_0^{(2)} \exp \left[ \frac{-E_a^{(2)}}{kT} \right]
\]

The prefactors \( D_0^{(i)} \) and activation energies \( E_a^{(i)} \) are given in Tables 2.1 and 2.2 [42].

For extremely high doping concentrations, this treatment must be altered to consider extrinsic diffusion. For extrinsic diffusion, \( D \) is a function of \( N \), the impurity concentration. \( D \) is now given as:

\[
    D(N) = h \left[ D_0^{(0)} \exp \left[ \frac{-E_a^{(0)}}{kT} \right] + \left( \frac{N}{n_i} \right) D_0^{(1)} \exp \left[ \frac{-E_a^{(1)}}{kT} \right] + \left( \frac{N}{n_i} \right)^2 D_0^{(2)} \exp \left[ \frac{-E_a^{(2)}}{kT} \right] \right]
\]

\( n_i \) represents the intrinsic carrier concentration of Si, which is a function of temperature. The prefactor \( h \) is defined to be 1 if \( N << n_i \) and 2 if \( N >> n_i \). For degenerate doping, \( n \) is therefore taken to be 2.
Table 2.1: Prefactors and activation energies for calculating bulk diffusion in Si. Adopted from Fair [42].

<table>
<thead>
<tr>
<th>Element</th>
<th>$D_0^{(0)}$ (cm$^2$ s$^{-1}$)</th>
<th>$E_a^{(0)}$ (eV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>p-Type</td>
<td></td>
<td></td>
</tr>
<tr>
<td>B</td>
<td>0.037</td>
<td>3.46</td>
</tr>
<tr>
<td>Al</td>
<td>1.385</td>
<td>3.41</td>
</tr>
<tr>
<td>Ga</td>
<td>0.374</td>
<td>3.39</td>
</tr>
<tr>
<td>In</td>
<td>0.785</td>
<td>3.63</td>
</tr>
<tr>
<td>n-type</td>
<td></td>
<td></td>
</tr>
<tr>
<td>P</td>
<td>3.85</td>
<td>3.66</td>
</tr>
<tr>
<td>As</td>
<td>0.066</td>
<td>3.44</td>
</tr>
<tr>
<td>Sb</td>
<td>0.214</td>
<td>3.65</td>
</tr>
</tbody>
</table>

Diffusion and segregation are separate mechanisms. Segregation occurs when impurities exceed the solid solubility leading to an increased surface concentration. The resulting dopant profile is asymmetric toward the growth direction. In contrast, diffusion leads to a symmetrical spreading in the profile in the shape of a Gaussian with full width at half maximum given by Eq. 2.17. Once a particle has been incorporated into the lattice, it will not segregate, but it may diffuse. Particles which suffer from severe segregation are not necessarily rapid diffusers.

Sb suffers from severe segregation. But, Sb diffusion has been shown to be vacancy-mediated due to its large size [41]. Thus Sb diffuses very slowly in a highly crystalline material.

P also suffers from segregation, but to a less extent than Sb, due to the smaller atomic size of P. P diffusion is interstitially mediated and therefore faster than Sb [41].
Table 2.2: Prefactors and activation energies for calculating bulk diffusion in Si. Adopted from Fair [42]

<table>
<thead>
<tr>
<th>Element</th>
<th>$D_0^{(1)}$ (cm$^2$ s$^{-1}$)</th>
<th>$E_a^{(1)}$ (eV)</th>
<th>$D_0^{(2)}$ (cm$^2$ s$^{-1}$)</th>
<th>$E_a^{(2)}$ (eV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>p-Type</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>B</td>
<td>0.76</td>
<td>3.46</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Al</td>
<td>2480</td>
<td>4.20</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ga</td>
<td>28.5</td>
<td>3.92</td>
<td></td>
<td></td>
</tr>
<tr>
<td>In</td>
<td>415</td>
<td>4.28</td>
<td></td>
<td></td>
</tr>
<tr>
<td>n-Type</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>P</td>
<td>4.44</td>
<td>4.00</td>
<td>44.2</td>
<td>4.37</td>
</tr>
<tr>
<td>As</td>
<td>12.0</td>
<td>4.05</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sb</td>
<td>15.0</td>
<td>4.08</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

B is a moderate segregator [52]. B diffusion is interstitially mediated and diffuses much faster than Sb and P due to its small atomic size.

2.4.2 Growth of $\delta$-Doping Plane by Low Temperature MBE

A $\delta$-doping plane of dopants is a region of doping impurities contained within a two dimensional plane of the epitaxial layer, as depicted in Fig. 2.14. The impurities in this picture occupy substitutional lattice sites. Generally sheet carrier concentrations are quite high, exceeding $10^{13}$ cm$^{-2}$.

Schubert outlined 3 steps for the realization of a $\delta$-doping layer[119]: (i) suspend epitaxial growth, (ii) allow a flux consisting only of dopants to impinge on the semiconductor surface, and (iii) resume growth of the epitaxial layer.

Ideally, the sticking coefficient is nearly unity, and very little diffusion or segregation occurs. In reality, the growth of a $\delta$-doping layer is kinetically limited. Phenomena such as segregation and diffusion will result in undesirable broadening of
the δ-doping planes. A true δ-doping plane should be a spike with a full width at half maximum less than 2.5 nm [119]. The key to achieving such a profile is to suppress segregation and diffusion by using low temperature MBE.

Hobart et al. demonstrated that LT-MBE is sufficient to substantially suppress dopant segregation. Fig. 2.15 shows the secondary ion mass spectrometry (SIMS) profiles of a monolayer of Sb grown at various substrate temperatures. Clearly, the growth temperature of 320 °C significantly suppresses the segregation and leads to the sharpest Sb profile.

However, the films grown by LT-MBE will have more point defects than those grown by standard MBE temperatures. It is believed that LT-MBE leads to the

Figure 2.14: Schematic of an ideal δ-doping plane of dopants. Note that in this idealized case, all of the impurities have been confined to one atomic monolayer. Adopted from Schubert [119].
Figure 2.15: Secondary ion mass spectrometry plots showing the segregation of 1 monolayer of Sb resulting from various growth temperatures. Note that the profile is sharpest for the lowest growth temperatures. Adopted from Hobart [57].

presence of vacancy-like defects throughout the film [3] due to the reduced atom surface mobility. A recent deep-level transient spectroscopy (DLTS) study on Si step junction diode (SJD) grown by MBE revealed that two vacancy-related fundamental defects, doubly and singly negatively charged divacancies, are created at growth temperatures at or below 600 °C without intentionally introducing defects and/or impurities. [22] One approach to removing these defects is annealing the samples in an RTA furnace [20].
2.4.3 Post-growth Annealing and Dopant Diffusion in the Spacer of Si/SiGe RITD

The more recent DLTS study [20] on MBE grown Si SJD confirmed that, when the as-grown LT-MBE samples were annealed at 700 °C, 800 °C, and 900 °C for 60 seconds by rapid thermal annealing, the total density of defects were decreased without generating new defects and most defects were annihilated at temperatures around 900 °C.

However, post-growth annealing will lead to unwanted dopant diffusion, hence broadened dopant profiles, which will make the tri-angular quantum well lose its carrier confinement. Another problem resulting from the dopant diffusion is the formation of dopant pairs [23] within the intrinsic spacer. If both the n- and p- type doping densities are $10^{20} \text{cm}^{-3}$, then the average spacing between n- type and p- type atoms would be 10 Å, which is a short enough distance to form loosely-coupled ion pairs tending to give rise to neutral defect sites. The variation of n- type and p- type atomic spacings will lead to a spectrum of defined energy levels, which may range over a large fraction of the host semiconductor band gap. Thus, dopant pairs formed within the spacer will increase the excess current component and will degrade the tunnel diode PVCR.

Two phenomenon which affects the dopant diffusion in the spacer of Si/SiGe RITD are discussed as follows.

**Dopant Pairing Effect**

In Si-based RITDs, two δ-doped layers are separated by a thin intrinsic spacer which is only several nanometers thick. Therefore, during the post-growth annealing, the n-type dopant atoms will diffuse into the p-type heavily doped region and
p-type dopant atoms will diffuse into the n-type heavily doped region. Studies have been performed in which donors diffuse in acceptor-type backgrounds and acceptors in donor-type backgrounds. Reduced diffusion of B in heavily doped P layers was observed [93]. Sb and P diffusion in a heavily B doped layers also exhibits the same behavior [41]. The reduced diffusivity most likely indicates the dopant pairing reactions [41]

\[ Sb^+ + B^- \rightleftharpoons (Sb^+B^-) \]  \hspace{1cm} (2.20)  
\[ P^+ + B^- \rightleftharpoons (P^+B^-) \]  \hspace{1cm} (2.21)

**Dopant diffusion in SiGe Strained Layer**

A thin (≤ 4 nm) SiGe layer is often grown as part of the intrinsic spacer of Si-based RITD to increase the tunneling probability. Since the lattice constant of Ge is about 4% larger than a Si crystal, biaxial compressive strain will exist in the SiGe layer, provided that the thickness of the SiGe layer does not exceed the critical thickness and relax the strain by misfit dislocation generation at the heterojunction interface. Both the addition of Ge atoms and the existence of biaxial compressive strain will affect dopant diffusion, and they are often referred to as the chemical effect and strain effect.

The diffusivity of Sb was found to increase with the Ge alloy content in relaxed Si\(_{1-x}\)Ge\(_x\) layers [98]. Compressive strain also enhances Sb diffusion in Si\(_{1-x}\)Ge\(_x\) layers [99]. Therefore, both the chemical effect and strain effect enhance the diffusion of Sb.

The diffusivity of P will increase with the Ge alloy content in relaxed Si\(_{1-x}\)Ge\(_x\) layers. However, the compressive strain results in a decrease in diffusivity. [19]
Kuo [76] found that both the chemical effect and strain effect retards the diffusion of B. The major part of the retardation is due to the chemical effect, with only a small influence by the biaxial strain.

In short, the dopant diffusion during post-growth annealing will offset the improvement by the removal of point defects, an optimal annealing temperature exists for highest PVCR.

2.5 Current Status of Si-based Tunnel Diodes

Since the development of the Esaki diode in 1958 based upon interband tunneling [40], the tunnel diode has been an additional option for the circuit designer, with its unusual negative differential resistance (NDR) property. But, due to the lack of robust manufacturing techniques and compatibility with Si CMOS processing, the discrete Esaki tunnel diode has become relegated to niche applications, such as local oscillators and frequency locking circuits.

The development of the resonant tunneling diode (RTD) in 1974 based upon intraband tunneling using double barriers [15] provided an alternative pathway, using electron confinement within the conduction band through bandgap engineering, by harnessing advancements in epitaxial growth techniques in the late 1960’s and early 1970’s. This approach works well for the III-V compound semiconductor material systems where significant conduction band offsets are possible to create the confinement needed.

Until recently, a viable Si-based tunnel diode for integration with CMOS has eluded investigation. Some of the first attempts explored Si-based RTDs. For intraband tunneling, the natural heterojunction system is Si/SiGe, but due to a small
conduction band offset between Si and Ge, the achievable electron confinement reported is below 150 meV and only with the use of thick relaxed SiGe buffer layers to engineer the strain energy to place the Si wells and Si barriers under compressive strain. Initial reports on Si-based RTDs demonstrated a peak-to-valley current ratio (PVCR) of 1.2 at room temperature [64]. Nevertheless, some recent progress is advancing the state-of-the art in Si/SiGe RTDs with PVCRs reported up to 2.9 [126] and $J(p)$ of 282 kA/cm$^2$ [127].

Research on alternative Si-based RTDs is seeking a suitable wide bandgap barrier that is also compatible with crystalline Si wells, but this presents a daunting epitaxial growth problem. Some Si-based RTD structures used SiO$_2$ [63], [78] or Al$_2$O$_3$ [129] barriers, but severe constraints upon epitaxial overgrowth of a thin (< 5nm) crystalline Si quantum well atop the amorphous oxide barrier as well as the Si/oxide interface roughness have hampered progress [117]. A more promising avenue amongst recent Si-based RTD investigations is exploring alternative barriers such as CaF$_2$ that do permit epitaxial overgrowth of crystalline Si. But, epitaxial growth of the CaF$_2$ is on <111> Si substrates, which are not CMOS compatible [152], [153].

An interesting approach that is gaining attention is a paradigm shift back to an Esaki-like interband tunnel diode. This effectively replaces the challenging epitaxy found in the Si-based RTDs with a new challenge of achieving degenerate doping during a near-equilibrium epitaxial growth technique. The discrete Esaki tunnel diodes of the 1960’s using alloying techniques have set benchmarks for Si Esaki diodes with room temperature PVCR as high as 4.0 [43] and Ge Esaki diodes with PVCR of 8.3 [1]. A modern version of the Esaki diode using spin-on glass dopant diffusion
has reported PVCRs up to 2.2 that could be more promising for monolithic integration [151]. It should be noted that a PVCR beyond 3 does not increase the speed index significantly [123]. Also, a significant advantage for interband tunnel diodes is that both elastic and inelastic scattering can contribute to valley current in an intraband tunnel diode, but only inelastic scattering can contribute to the valley current of an interband tunnel diode [123].

The first successful epitaxially grown Si-based interband tunnel diode was shown by Jorke et al. with a PVCR of 2 at room temperature by inserting a thin i-layer between the p(+)n(+) emitter-base junction [68], but this fine work was largely overlooked by the scientific community, as the context of the overall paper was upon bipolar junction transistors (BJT).

Another interband tunnel diode structure was proposed by Sweeny and Xu [132] using δ-doping to create confined states in the valence and conduction bands on the p-side and n-side of a p-n junction, respectively. This creates an interband resonance tunneling condition between the states. This class of tunnel diodes was aptly named resonant interband tunnel diodes (RITD). An initial attempt at creating an epitaxially grown Si-based RITD using δ-doping injectors showed some bistability, but no room temperature NDR [163].

More fundamental to the success of a Si-based interband tunnel diode are the processing steps that are used that anticipate dopant segregation and diffusion during epitaxial growth and processing and minimize their detrimental effects. Eventually, dopant segregation effects [58] were overcome by the far-from-equilibrium technique of low-temperature molecular beam epitaxy (LT-MBE) [38], [54] to effectively create the first Si-based RITD [114]. This Si/SiGe RITD combined several key points: (i)
δ-doping injectors, (ii) a composite i-layer inserted as a spacer layer between the δ-doped injectors to minimize interdiffusion, (iii) LT-MBE to suppress segregation and diffusion, and (iv) a short post-growth rapid thermal anneal (RTA) heat treatment to reduce point defects created during the LT-MBE process that elevate the excess current. Using this modified approach resulted in initial reports of room temperature PVCR in Si-based RITDs using δ-doping began at 1.54 at a peak current density of 3.2 kA/cm² [26], but quickly leaped to over 2 at a peak current density of 22 kA/cm² when the substrate temperature during MBE growth was further reduced [110]. A variety of alternative Si/SiGe RITDs have been demonstrated as well as some that are Si-only [110], [112], [141] and both polarity “n-on-p” [114], [110], [112], [141], [143] and “p-on-n” RITDs [59] as well as vertically-stacked pnp RITDs that exhibit symmetrical NDR about the origin for simple latches [66]. Measured peak current densities have been engineered between 0.2 A/cm² and 32 kA/cm² using Sb as the n-type dopant [114], [110], [112], [141], [143], [59], [66].

![Figure 2.16: Structure of a typical Si RITD](image)

Fig. 2.16 shows the schematic diagram of a typical Si-base RITD. As shown in Fig. 2.17, the calculated energy band diagram of this structure, the δ-doping planes...
on either side of the p-n junction define the quantum states for the majority carrier [111].

Figure 2.17: Calculated energy band diagram and resonant states of SiTD1. The Sb and B activation of the $\delta$-doped regions is assumed to be 50%. $X_z$ denotes the conduction band minimums along the $k_z$ axis of the Brillouin zone, and $X_{xy}$ denotes the conduction band minimums along the $k_x$ and $k_y$ axes where $z$ is the growth direction. SO denotes the split-off valence band-edge. Adopted from Rommel [111].

These four basic points and structure show in Fig. 2.16 have now led other research groups to reproduce these results using other MBE growth reactors with P instead of Sb as the n-type dopant [36], [35], [30] and have even lead to PVCRs up to 6 at room temperature in a Si-based interband tunnel diode [35].

35
Figure 2.18 summarizes the status of Si-based interband tunnel diodes before this work. It is encouraging that PVCR of 6.0 [34] and $J_p$ of 47 kA/cm$^2$ [29] were achieved.

Table 2.3 summarizes the current status of epitaxial grown Si-based tunnel diodes. It is clear that Si RITDs outperform Si RTD in terms of highest PVCR achieved. However, Si RTDs exhibit a $J_p$ of 282 kA/cm$^2$, which is the highest $J_p$ for any type of Si-based tunnel diodes.

2.6 Conclusion

This chapter discusses the tunnel diode I-V characteristics, small signal model and performance metrics. The operation theories of three variations of tunnel diodes are
Table 2.3: Summary of current status of epitaxial grown Si-based tunnel diodes.

<table>
<thead>
<tr>
<th>Study</th>
<th>Type</th>
<th>Dopant</th>
<th>PVCR</th>
<th>(J(!p))</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ismail, 1991 [65]</td>
<td>Si/SiGe RTD</td>
<td>P</td>
<td>1.2</td>
<td>400 A/cm²</td>
</tr>
<tr>
<td>See, 2001 [127]</td>
<td>Si/SiGe RTD</td>
<td>As</td>
<td>2.43</td>
<td>282 kA/cm²</td>
</tr>
<tr>
<td>Jorke, 1993 [69]</td>
<td>Si p⁺-i-n⁺ Esaki</td>
<td>Sb, B</td>
<td>2.0</td>
<td>600 A/cm²</td>
</tr>
<tr>
<td>Dashiel, 2000 [29]</td>
<td>Si p⁺-i-n⁺ Esaki</td>
<td>P, B</td>
<td>1.3</td>
<td>47 kA/cm²</td>
</tr>
<tr>
<td>Morita, 1997 [95]</td>
<td>Si/SiO₂/Si RTD</td>
<td>P, B</td>
<td>1.8</td>
<td>3 μA/cm²</td>
</tr>
<tr>
<td>Rommel, 1999 [108]</td>
<td>Si/SiGe/Si RITD</td>
<td>Sb, B</td>
<td>2.2</td>
<td>6.4 kA/cm²</td>
</tr>
<tr>
<td>Thompson, 1999 [140]</td>
<td>Si-only RITD</td>
<td>Sb, B</td>
<td>2.1</td>
<td>9.4 kA/cm²</td>
</tr>
<tr>
<td>Duschl, 1999 [34]</td>
<td>Si/SiGe/Si RITD</td>
<td>P, B</td>
<td>6.0</td>
<td>1.5 kA/cm²</td>
</tr>
</tbody>
</table>

discussed. The experimental realization of the Si-based RITD developed by Rommel et al is also presented. The current status of epitaxial grown Si-based tunnel diode is also reviewed.
CHAPTER 3

CIRCUIT APPLICATIONS OF TUNNEL DIODE

Since the tunnel diode was invented by Esaki, it immediately attracted much attention due to the advantages inherent in the tunnelling principle which produced the negative resistance characteristic. Numerous circuit applications in both the digital and microwave realms have been demonstrated by using tunnel diodes. In this chapter, the circuit applications for tunnel diodes are presented. Section 1 discusses the TD stability issue, it clearly shows that different circuit applications correspond to the stability of tunnel diodes. Section 2 presents novel 3-terminal NDR devices, which greatly boost the tunnel diode circuit applications by using the third terminal to control its I-V characteristics. In section 3 and 4, digital and microwave tunnel diode circuits are discussed.

3.1 General Stability Analysis of Tunnel Diode Circuits

Assume that the diode is biased in the NDR region at the quiescent point \((I_0, V_0)\) as shown in Fig. 3.1. The negative conductance at this point \(-g\) is given by the slope of the curve at this point. Assuming the linearity of the I-V curve near the operating point and applying Kirchhoff’s law to the equivalent circuit shown in Fig. 3.2, two
loop equations can be obtained as follows:

\[ E = L \frac{di_2}{dt} + Ri_2 + \frac{1}{C} \left( \int i_2 dt - \int i_1 dt \right) \]  

(3.1)

\[ V_1 = \frac{1}{C} \left( \int i_2 dt - \int i_1 dt \right) \]  

(3.2)

Where \( R = R_s + R_d \), \( L = L_s + L_d \). The above equations yield

\[ \frac{d^2 i_2}{dt^2} + (\frac{R}{L} - \frac{|g|}{C}) \frac{di_2}{dt} + \frac{1 - R|g|}{LC} i_2 = \frac{i_0 + (V_0 - E)|g|}{LC} \]  

(3.3)

The solution to the above equations is:

\[ i_2 = A_1 e^{\lambda_1 t} + A_2 e^{\lambda_2 t} + \frac{i_0 + (V_0 - E)|g|}{1 - R|g|} \]  

(3.4)

Where \( A_1 \) and \( A_2 \) are arbitrary constants whose values are to be determined from the initial conditions; and

\[ \lambda_{1,2} = \frac{1}{2} \left( \frac{|g|}{C} - \frac{R}{L} \right) \pm \left\{ \frac{1}{4} \left( \frac{R}{L} - \frac{|g|}{C} \right)^2 - \frac{1 - R|g|}{LC} \right\}^{\frac{1}{2}} \]  

(3.5)
Depending on the values of $\lambda$, four different situations may rise:

1. If $\lambda_1$ and $\lambda_2$ are real and positive, the noise induced initial small change of operating point will result in an exponentially growing current $i_2$, which will drag the operating point out of the NDR region in a very short period. This situation corresponds to the bistable mode of operation. Due to the self-latching property and high switching speed, this situation is suitable for switching applications.

2. If $\lambda_1$ and $\lambda_2$ are complex numbers with positive real parts, the noise will cause the current $i_2$ to grow sinusoidally. This situation is suitable for oscillator applications.

3. If $\lambda_1$ and $\lambda_2$ are real and negative, the operating point is stable, because the initial small change of operating point due to noise will be damped exponentially. This situation is useful for amplifiers, mixers, converters and detectors applications.

4. If $\lambda_1$ and $\lambda_2$ are complex numbers with negative real parts, a stable operating point is also obtained, because the current will decay sinusoidally. [18]
3.2 3-terminal NDR Devices

The two-terminal nature of tunnel diode limits its application. A solution is to monolithically integrate the tunnel diode into the structure of a three-terminal device, such as a bipolar or FET, so that the I-V characteristics can also be controlled by using a third terminal. Since the first RTD/HBT [13] and the first RTD/FET [128] were demonstrated, numerous studies have been conducted in this area. Now, 3-terminal NDR devices have become an important circuit element and found many circuit applications.

3.2.1 Monolithic Integration of TD with FET

A TDFET device is created by integrating TDs and FETs. A compact integration method is to grow tunnel diode layers directly on top of the source or drain region of the FET. Different types of TDFETs can be built by connecting the tunnel diode to drain, source or gate terminals of the FET. Figure 3.3 shows four typical TD-FETs, which are source TDFET, drain TDFET, gate TDFET, and parallel TDFET, respectively.

In a source TDFET, the tunnel diode is connected from the source to ground. In a drain TDFET, the tunnel diode is connected from the drain to the power supply. In the $I_{DS}$ vs. $V_{DS}$ characteristics of both of these two configurations, the NDR region exists before the saturation region as shown in Fig. 3.4. Furthermore, the slope of the NDR region can be varied by changing the gate voltage, which makes this device an excellent candidate as a voltage-controlled oscillator (VCO) when biased in its NDR region. However, when the TDFET exhibits NDR, the FET is in its linear regime, when the FET reaches its saturation regime, the tunnel diode is in its post-NDR
Figure 3.3: Four types of TDFET. (a) source TDFET, (b) drain TDFET, (c) gate TDFET, (d) parallel TDFET

Figure 3.4: I-V characteristics of a source TDFET. [27]
region. In another words, the source TDFET and drain TDFET can not be in NDR region and in saturation region simultaneously. Therefore, these two types of TDFET are more suitable for applications like VCO rather than amplifier [27].

In a gate TDFET, the tunnel diode is connected from the gate to the grounded source. The tunnel diode will not change the I-V characteristics of the FET, however, when the tunnel diode is biased in its NDR region, the gate TDFET exhibits a higher gain (S21) than the FET alone. The S11 of the gate TDFET is also higher than the FET alone. The enhancement is due to a resonance in the gate-source loop of the TDFET resulting from the negative impedance of the tunnel diode. This device is suitable for oscillators and mixers [27].

One important integration scheme is to connect the anode of the tunnel diode to the drain and connect the cathode to the source, so that the tunnel diode and the FET are in parallel. This device will exhibit an I-V characteristics with adjustable peak current. One possible application is the monostable-bistable transition logic elements (MOBILE) [16], which will be discussed in detail in section 3.4.3.

3.2.2 Monolithic Integration of TD with HBT

The concept of resonant-tunneling bipolar transistor (RTBT) was proposed by Capasso and Kiehl in 1984 [12]. The new negative conductance device consists of a heterojunction bipolar transistor with a quantum well and a symmetric double barrier in the base region. Resonant tunneling is achieved by high-energy minority carrier injection into the quantum well state rather than by the application of an electric field. In 1986, Capasso et al. [13] demonstrated the first RTBT with a single double barrier in the base. Alternatively, Futatsugi et al. [48] reported an RTBT with a
single double barrier in the emitter at about the same time. Velling et al. [148] reported a HBT/RTD transistor with an RTD in the collector. The RTBT shows adjustable peak current, which is suitable for MOBILE application.

The insertion of RTD layers into HBT using III-V materials system is straightforward, since RTD is a unipolar device. However, to integrate Si based RITD with HBT, a backward diode has to be inserted to connect the RITD and HBT. In a recent study by Chung et al. [21], the first Si-based RITD/HBT was developed using a backward diode as the connecting block. The resulting devices have a distinguishing characteristics of infinite, negative, and adjustable PVCR with adjustable PCD by the control of the HBT base current, as shown in Fig. 3.5.

Figure 3.5: I-V characteristics of a Si-based integrated RITD/HBT. [21]
3.3 Tunnel Diode Microwave Circuit

This section discusses the tunnel diode amplifiers, tunnel diode mixers, converters and detectors, tunnel diode oscillators,

3.3.1 Tunnel Diode Oscillators

According to Eqn. 3.5 and the stability analysis in Sect. 3.1, the necessary condition for self-sustaining oscillation is

\[ \sigma = \left( \frac{|g|}{c} - \frac{R}{L} \right) \geq 0 \]  

(3.6)

And the corresponding frequency of oscillation is given by

\[ \omega = \left\{ \frac{1}{LC} \left( 1 - R|g| \right) - \frac{1}{4} \left( \frac{R}{L} - \frac{|g|}{c} \right)^2 \right\}^{\frac{1}{2}} > 0 \]

(3.7)

The oscillations build up in the NDR region until the current swings extend into the positive differential resistance region, where Eqn. 3.7 no longer holds and oscillations are stabilized.

The output power developed in a tunnel diode oscillator is given by the following empirical relation [18]

\[ P_o = \frac{3}{16} (I_p - I_v)(V_p - V_v) \]

(3.8)

This equation is not valid when the oscillator frequency exceeds one-third of the resistive cut-off frequency.

Bergman et al. [26] demonstrated a heterojunction interband tunnel diode (HITD) C-Band oscillator in InP system. The oscillator is biased at 0.45 volt. The fundamental output power is -18.83 dBm at 4.70 GHz. The second, third, and fourth harmonic
output levels are -43.2, -40.5, and -57.0 dBm, respectively. The phase noise is measured to be -87.0 dBc/Hz at 1 MHz from the peak. The total power consumption is 0.32 mW.

Cidronali et al. [24] presented a InP-HEMT-TD-based VCO operating in the 4-6-GHz band suitable for wireless applications. The circuits generated an output power in the range of -11 to -18 dBm when operated at a bias current of 1.75 mA at 500 mV. The maximum tuning range of 150 MHz and the maximum single sideband-to-carrier ratio of -97 dBc/Hz at 200 kHz have been achieved.

To increase the output power, an oscillator using a cascaded connection of tunnel diodes in series was proposed and demonstrated at low frequencies in 1965 [149]. The key issue is to bias all the serially-connected tunnel diodes simultaneously in their NDR regions.

Normally a circuit consisting of serially-connected tunnel diodes is unstable in DC when all of them are biased in the NDR region. If a DC bias voltage sufficient to bias all tunnel diodes in their NDR regions is applied by a simple DC battery, the DC instability will divide the bias voltage so that all the tunnel diode are biased instead in the PDR region. As a result, multiple-peaks are observed during DC measurement instead of one wider peak with an accompanying large voltage span. However, when the bias voltage is applied in a fast way, for example, using a fast electrical pulse, the capacitive current will dominate, and the initial distribution of the total voltage can be equally partitioned among individual tunnel diode. Consequently, all diodes can be biased in their NDR region simultaneously [162].

For oscillator applications, the serially connected tunnel diodes can be biased by using an external RF source, with a frequency close to the circuit resonant frequency.
Boric-Lubecke et al [7] demonstrated a 2 GHz oscillator with two tunnel diodes in series. Nair et al [96] built a single and dual HITD VCO which integrated single, and double HITDs with a FET. The power output of a single HITD VCO was 2.0 dBm and that of the dual HITD VCO was 4.3 dBm. The dual HITD VCO also exhibited a wider tuning range than the single HITD VCO.

3.3.2 Tunnel Diode Amplifier

There are two basic types of tunnel diode amplifiers: the transmission type and the reflection type [118]. Both types require that the tunnel diode be biased in its NDR region. In the transmission tunnel diode amplifier, the negative resistance of the tunnel diode increases the available power of the signal source by lowering the internal impedance of the source signal, hence the signal is amplified. In the reflection type tunnel diode amplifier, the incident signal on the tunnel diode is reflected at an increased amplitude with the same characteristic impedance. Then the output signal has to be separated from the input signal by some other means.
Transmission tunnel diode amplifiers

Figure 3.6 shows a circuit model of a transmission tunnel diode amplifier, in which the negative resistance appears directly in parallel with the source and load resistance. The signal source is represented as a current source $i$ in parallel with an internal conductance $g_s$. The load is represented by the conductance $g_l$. At the center frequency $\omega$, the circuit becomes that shown in Fig. 3.7.

At the center frequency, the transducer power gain, which is the ratio between the power delivered to the load and the power available from the source is given by

$$G = \frac{4g_sg_l}{(g_s + g_l)^2 \left\{1 - \left(\frac{g_d}{g_s} + g_l\right)\right\}^2} \tag{3.9}$$

The available gain, which is defined as the ratio of the available power from the source, plus negative conductance, to the available power of the source alone, is given by

$$G_{AV} = \frac{g_s}{g_s - g_d} \tag{3.10}$$

Both transducer power gain and available gain can be set to any arbitrary value just by a suitable choice of the source and load resistances, which distinguish tunnel diode amplifiers from the more conventional amplifiers. However, for tunnel diode
amplifiers with very high gain, any small changes in the component values can lead to
significant changes in gain, which is not desirable. The 3-dB bandwidth for available
gain can be given as:

$$B = \frac{g_d}{(G_{AV} - 1)} \pi C$$  \hspace{1cm} (3.11)

This shows that bandwidth decreases as gain increases.

**Reflection tunnel diode amplifier**

A reflection tunnel diode amplifier is one which the tunnel diode terminates as one
or two ports of an n-port network, and the generator and load terminates the other
ports. When the tunnel diode is biased in its NDR region, the reflection coefficient
$\Gamma$ is a value greater than 1. Therefore, the reflected signal has a larger amplitude
than the incident signal. The key is then to separate the reflected signal from the
incident signal. There are two common ways to achieve that. One way is by means
of a circulator which is a 3-port network. Another way is to use two identical tunnel
diodes and a 90° 3-dB hybrid coupler, which is a 4-port reciprocal network.

Figure 3.8 shows the topology of a reflection amplifier using a hybrid coupler. The
principle of operation is as follows: The signal S1 is fed into port 1. It splits into two
signals, S2 and S3 of equal amplitude but 90° out of phase. S2 is then fed to amplifier
1 at port 2 and reflected with a value of $\Gamma S2$. $\Gamma$ is the reflection coefficient, which is
greater than 1 when the tunnel diode is biased in its NDR region. $\Gamma S2$ is fed back to
the coupler and splits into two signals, $\Gamma S2a$ and $\Gamma S2b$ of equal amplitude but 90° out
of phase. $\Gamma S2a$ is fed to port 1 and $\Gamma S2b$ is fed to port 4. Similarly, S3 is amplified
by amplifier 2 and splits into two signals, $\Gamma S3a$ and $\Gamma S3b$ of equal amplitude but 90°
out of phase. $\Gamma S3a$ is fed to port 4 and $\Gamma S3b$ is fed to port 1.
Figure 3.8: topology of a reflection amplifier using hybrid coupler. Adopted from Sze

Ideally, at port 1, the following identity holds

$$\Gamma S_{2a} + \Gamma S_{3b} = \Gamma (S_{2a} + S_{2a} \angle -180^\circ) = 0$$  \hspace{1cm} (3.12)

And at port 4, we have

$$\Gamma S_{2b} + \Gamma S_{3a} = 2\Gamma S_{2a} \angle -90^\circ$$  \hspace{1cm} (3.13)

Therefore, the output at port 4 is

$$S_{out} = \Gamma S_1 e^{-j(\pi/2 + \theta)}$$  \hspace{1cm} (3.14)

Where $\theta$ is the total delay of a signal traveling into and out of the amplifier unit.

The transducer power gain of this amplifier is $\Gamma^2$. The bandwidth is generally limited by the coupler bandwidth.

The bidirectional nature of the reflection type tunnel diode amplifier is a very attractive feature. Recently, the concept of bidirectional amplifier (BDA) has been proposed to reduce the overall cost of transceivers. Currently, most MMIC transceivers
designs are limited by the reduced performance resulting from the transmit/recieve (T/R) switches and the larger chip area required to implement the dual T/R signal paths. By using BDA, the need for additional T/R switch will be eliminated and only a single signal path will be required. This new technology will greatly reduce the complexity of the transceiver system [2].

Recently, Cidronali et al [27] demonstrated a monolithic heterojunction interband tunnel diode (HITD) bidirectional amplifier (BDA) for RF-ID application. The fabricated tunnel diode BDA shows a maximum gain of 5 dB at 5.8 GHz with a 3 dB bandwidth of about 300 MHz. The BDA is biased at 400 mV and a drain current equal to 1 mA of DC current, which consumes only 0.4 mW. The very low power consumption is a key feature which makes it very suitable for RF-ID applications.

3.3.3 Tunnel Diode Frequency Converters and Detectors

The non-linearity of tunnel diode I-V characteristics can be detrimental for its application as an amplifier. However, this makes tunnel diodes an excellent candidate for frequency converters such as subharmonic mixers [84] [25] and frequency multipliers [5]. Another important application for TD non-linearity is envelope detectors for microwave imaging and atmospheric radiometry [11] [121].

The remarkable features of tunnel diode frequency converters are its low noise figure, and high gain (low loss). For tunnel diode mixers, the local oscillator power requirement is very low.

It was also shown that the tunnel diode I-V characteristics can be well fitted using a third order polynomial equation with the second-order coefficient much larger than the third-order coefficient [25]. This indicates the quasi-square-law behavior of the
I-V characteristics when the tunnel diode is biased at zero volt. Since an nth degree nonlinearity generates nth-order mixing products, the approximately second-degree nonlinearity allow inherently good performance in terms of third-order intermodulation (IM3).

Zero-biased nonlinear circuits (mixer, detector) are very attractive, because such circuits simplify the system by eliminating the need for bias control circuits and minimize the power consumption.

To characterize the second order nonlinearity of the tunnel diode I-V curve, the curvature coefficient, $\gamma$, is defined as

$$\gamma = \frac{d^2 I/dV^2}{dI/dV}$$

The larger $\gamma$ is, the more the I-V characteristic will be nonlinear.

The current sensitivity, $\beta_i$, of a detector, which is defined as a measure of the change in DC output current for a given input RF power [106], can be directly related to $\gamma$ by equation

$$\beta_i = \frac{\gamma}{2} A/W$$

The open-circuit voltage sensitivity, $\beta_v$, is defined as the voltage drop across the junction resistance when the diode is open-circuited.

Cidronali et al. [25] built a highly linear single balanced mixer based on an InGaAs/InAlAs HITD. Working in down-conversion mode, the HITD mixer exhibited a third-order intercept point power level of +17.5 dBm, a conversion loss of 11 dB and a 1-dB compression point of +7 dBm at the operative frequency of 1.8 GHz with a +5-dBm local-oscillator drive level.
Meyers et al. [92] fabricated InAs/AlSb/GaSb-based heterostructure backward diodes for zero-bias millimeter wave detection. A record-high curvature, $\gamma = 39.1$ V$^{-1}$, at zero bias was measured. On-wafer sensitivity measurements from 1 to 110 GHz gave a record-high average sensitivity of 3687 V/W for zero-bias operation.

### 3.4 Tunnel Diode Digital Circuit

To date, in the digital circuit arena, the increase in logic gate and bit density has followed Moore’s law by continuously scaling down the device size. However, it is questionable how long this trend can continue, as critical dimensions in the devices are already at the nano-scale and are fast approaching the atomic level. To continue the growth of the VLSI industry, unconventional devices enabling new systems and circuit functionalities are of great interest. The tunnelling devices promise a dramatic improvement in circuit performance as a result of picosecond switching speeds and reduction in device counts per circuit function. Compared with conventional logic circuits, logic circuits using tunnelling devices have the following advantages [91]:

- Reduced circuit complexity for a given function
- Low power consumption
- High speed operation

#### 3.4.1 Operation Modes

A tunnel diode can be operated in two modes: the monostable and the bistable mode. Consider a simple circuit shown in Fig. 3.9, for monostable operation, the load resistance and bias supply are arranged in such a way, that there is only one stable state, A or B, as shown in Fig. 3.9
Figure 3.9: A simple tunnel diode circuit with resistor as its load and its monostable and bistable operation.

Figure 3.9 also shows the bistable operation. There are two stable states A and B which can be obtained. State C is unstable, because an imbalance between the currents will force the node voltage away from this state and will evolve into state A or state B extremely quickly.

Figure 3.10 shows that the load resistance can be replaced by a tunnel diode to form a serially connected tunnel diode pair, which was originally proposed by Goto [55], and later called a Goto pair. Compared with a resistor loaded circuit, a Goto pair exhibits faster operation because of the larger maximum charging and discharging current. Furthermore, the Goto pair has a lower static power consumption due to the low bistable bias voltage and low static current in both equilibrium states. Because of these features, a Goto pair is a very important element for tunnel diode digital circuitry [89].

This inherent bistable behavior originating from its unique folded I-V characteristics make tunnel diode extremely useful in digital circuits. Up to date, tunnel diode
has been used to demonstrate numerous applications and potential market opportu-
nities, such as analog-to-digital converters [70] [9], square wave clock generation [10],
shift registers [6], ultra low power SRAMs [146], multiple-valued signed digit adders
[51], and clocked comparators [8].

The following sections presented two important applications: One transistor tun-
nel diode SRAM (1T-TSRAM), and monostable-bistable transition logic elements
(MOBILE).

3.4.2 One Transistor Tunnel Diode SRAM (1T TSRAM)

The large footprint of an six-transistor SRAM cell prevents the development of
high density arrays, and SRAM arrays are often limited to smaller cache memo-
ries. Due largely to their small footprint, one-transistor DRAM cells are the most
widely used cells for memory. However, the power consumption of DRAMs cells is much higher than the one of SRAM, because refresh current is required to store the information. An ideal memory circuit would have the footprint of a DRAM cell, while simultaneously offering the refresh-free of an SRAM cell. This is precisely what one-transistor tunneling-based SRAM cells (1T TSRAM) offer. Figure 3.11 shows a schematic circuit of a 1T TSRAM demonstrated by van der Wagt et al. [147], which consists of a pass transistor, a pair of tunnel diodes and a sensing capacitor, which is realized as part of the tunnel diode. Compared with a standard DRAM cell, the 1T TSRAM has the same sensing capacitor, so the read and write operation is the same as DRAM cell. What makes it different from a DRAM cell is the additional serially connected tunnel diode, by which the information is latched at the storage node. Therefore, the need for a refresh current is eliminated in 1T TSRAM, which would substantially reduce the circuit power consumption. The optimal TD for 1T TSRAM should have a ultra-low peak current density to reduce overall power consumption, and a sufficiently large PVCR to ease the requirement of small leakage current to ensure the latch points exists. A very wide valley region is also desired to provide a large voltage difference between the two stable latch points, which, in turn, provides a larger noise margin. However, to reduce the power consumption, a small valley region is desired.

An extremely low current density of tunnel diode will not degrade the operating speed of the 1T TSRAM. Because the tunnel diode pair provides only a means to store the information. The speed of write operation is determined by the amount of charging or discharging current, which is controlled by the pass transistor, while
the speed of read operation is mainly affected by the sensing amplifier and peripheral circuitry.

3.4.3 Monostable-Bistable Transition Logic Elements (MOBILE)

The MOBILE circuit was first proposed and demonstrated by Maezawa et al. in 1993 [86]. MOBILE consists of two serially connected NDR devices and is driven by an oscillating bias voltage $V_{bias}$. The MOBILE is in its monostable state when the bias voltage is smaller than twice of the peak voltage $2V_p$. When the bias voltage increases and exceeds $2V_p$, the monostable-bistable transition will take place. The circuit’s state after the transition is determined by the small difference in peak current of the two NDR devices. Therefore, the key in applying MOBILE for logic operation is to develop a three-terminal NDR device with controllable peak current. As discussed in Sect. 3.2.1, a monolithic integration of a FET and TD in parallel is well suited for
this application. The significant advantage of this operation is that a large number of fanouts is possible without sacrificing the high-speed operation.

The MOBILE circuit features both the edge-triggered and latching properties: the input signal at the rising edge of the clock $V_{bias}$ determines the output level, which is the edge-triggered behavior; the output is kept constant while the clock voltage is high. Thus, the MOBILE can be regarded as a delayed flip-flop with a return-to-zero mode output. Maezawa et al. [87] demonstrated a data flip-flop circuit using MOBILE’s that operates at 12.5 Gb/s at room temperature in III-V materials system. The gate length of the MODFET was 0.7 $\mu$m, so it is quite possible to achieve higher operating speed with more aggressively sub-micron processing. Other demonstrated applications by using MOBILE include a 15 GHz static binary frequency divider [90], and a 10 GHz 3-valued quantizer [150].
CHAPTER 4

STUDIES TO INCREASE PVCR OF SI-BASED RITD

4.1 Introduction

PVCR is such an important figure-of-merit for tunnel diode that the competition for higher PVCR never stops. In this work, a great amount of time and effort has been spent in the improvement of PVCR. For interband tunneling diodes, the PVCR is determined by the ratio between the desired interband tunneling current and the unwanted excess current through the energy states in bandgap. Therefore, the key to obtain a higher PVCR is to reduce the excess current component while maintaining the desired interband tunneling current. The excess current component in Si RITDs grown by LT-MBE can be mainly attributed to the point defects formed during the growth, which are singly and doubly charged vacancies [22], therefore, post-growth annealing is required to remove the point defects. However, post-growth annealing can also unfavorably lead to dopant diffusion, which will broaden the dopant profile and widen the tunneling barrier, hence reduce the desired interband tunneling current. Therefore, ideally, the annealing process will effectively remove the point defects without concurrently causing appreciable dopant profile redistribution. In this study, two approaches were taken to reach this goal. Section 4.3 presents the
first approach, the optimization of the RITD structure, while section 4.4 discusses the second approach, the optimization of post-growth annealing process.

4.2 Experimental

Epitaxial growth was achieved with an MBE growth system using elemental Si and Ge in electron-beam sources. The structures were grown on 75mm B-doped ($\rho = 0.015 - 0.04\Omega \cdot \text{cm}$) Si (100) wafers. The doping level for both $n^+$ and $p^+$ layers are $5 \times 10^{19} \text{ cm}^{-3}$, while the B $\delta$-doping sheet concentration was maintained at $1 \times 10^{14} \text{ cm}^{-2}$ and the P $\delta$-doping sheet concentration was varied from $1 \times 10^{14} \text{ cm}^{-2}$ to $3.4 \times 10^{14} \text{ cm}^{-2}$.

Prior to device fabrication, portions of the grown wafers were annealed in a forming gas ambient (95%N$_2$/5%H$_2$) in a Modular Process Technology corporation RTP-600S furnace at various temperatures for 1 minute. Ti/Au dots with various diameters were patterned on the surface of the wafers via standard contact lithography. A buffered oxide etch was used prior to metallization. Using the metal dots as a self-aligned mask, HF/HNO$_3$ wet etching was performed to isolate the diodes into mesas. Finally, a Ti/Au backside contact was evaporated on all of the samples.

4.3 A Study of SiGe Diffusion Barriers Cladding the B $\delta$-doping Layer

To maximize the PVCR, a higher peak current density and a lower valley current density are desired. For a Si-based RITD, the peak current density is determined by the electron tunneling probability through the tunneling barrier, which depends on the dopant profile of both sides of the p-n junction. A sharper dopant profile will lead to a higher tunneling current, thus higher peak current density. Valley current density
becomes elevated by defects within the tunneling barrier created during the LT-MBE growth process. LT-MBE is needed to minimize dopant diffusion and segregation during epitaxy. Post-growth annealing can reduce the point defect density, thus lowering the valley current density. However, this also unfavorably broadens the dopant profiles, especially B, which is a fast interstitial diffuser, thus the peak current density can also be reduced if over-annealed. Given that SiGe can act as an effective diffusion barrier for B in a Si matrix [75], structures with SiGe layers cladding the B δ-doping layer were grown in order to preserve the sharp B profile during high temperature post-growth annealing to reduce the point defect density.

Three structures were designed to study the effect of the SiGe cladding layer. All structures maintained the fundamental tunnel barrier thickness of 6 nm as measured between the two δ-doping layers, which to first order determines the tunneling distance. RITD(1/4/1), the control device, employed a symmetrical 1 nm Si / 4 nm Si$_{0.6}$Ge$_{0.4}$ / 1nm Si (1/4/1) spacer as shown in Figure 4.1, which is similar to many past structures studied by the authors. Figure 4.2 shows RITD(0/4/2) with an asymmetrical 0nm Si / 4 nm Si$_{0.6}$Ge$_{0.4}$ / 2 nm Si (0/4/2) spacer, resembling the modification provided by Duschl et al. [36], [35]. Note, the SiGe layer was directly grown atop the B-layer without the thin Si offset layer. Figure 4.3 shows RITD(0/4/2) clad, which is the same as RITD(0/4/2), except that a 1 nm Si$_{0.6}$Ge$_{0.4}$ cladding layer was also grown below the B δ-layer and outside the tunneling spacer. In this structure, the B δ-layer was essentially clad by thin SiGe on both sides. It should be stressed that all structures maintained the same fundamental tunnel barrier thickness of 6 nm, as measured between the two δ-doping layers, to facilitate easy comparison of the results. For all these three structures, the nominal n-type and p-type bulk doping
Figure 4.1: Schematic diagram of structure A, the Si/Si$_{0.6}$Ge$_{0.4}$/Si (1/4/1) RITD

Figure 4.2: Schematic diagram of structure B, the Si$_{0.6}$Ge$_{0.4}$/Si (0/4/2) RITD

levels in the injectors are $5 \times 10^{19}$ cm$^{-3}$, while the nominal n-type and p-type $\delta$-doping levels are $1 \times 10^{14}$ cm$^{-2}$.

Figure 4.4 shows the I-V characteristics of these 3 structures with the highest PVCR. RITD141 a PVCR of 2.7 with 1 minute annealing at 725 °C. RITD042 obtained a PVCR of 3.2 using 1 minute annealing at 800 °C. Whereas, RITD042clad further improved its PVCR to 3.6 with 1 minute annealing at 825 °C. The peak current density was reduced with the higher anneal temperatures. It is evident that RITD042clad exhibited superior PCVR performance over structures RITD141 and RITD042 and also withstood a much higher annealing temperature. To gain insight to why the
Figure 4.3: Schematic diagram of structure C, the $\text{Si}_{0.6}\text{Ge}_{0.4}/\text{Si}$ (0/4/2) RITD with SiGe cladding layer

I-V characteristics of the three structures are so different, further investigation of the dopant interdiffusion was performed, both experimentally and through theoretical calculations.

To fully understand the influence that B out-diffusion has on tunnel diode performance, the diodes were subjected to a range of anneal temperatures, Figure 4.5. Post-growth RTA processing has been shown to reduce point defects that contribute to elevated valley currents, but it also deleteriously broadens the B $\delta$-doping $[114]$. Consequently, an optimal RTA temperature exists that maximizes PVCR, which is clearly shown in Fig. 4.5. Note the optimal annealing temperatures for these three structures are different, RITD042clad shows the highest optimal annealing temperature, while RITD141 shows the lowest optimal annealing temperature. These results illustrate that insertion of the SiGe cladding layers suppresses B out-diffusion, so that higher RTA temperatures can be employed to more effectively reduce point defects, while minimizing the B diffusion to ensure a high peak current density. There is a 100 °C difference between the best PVCR from RITD141 and the best PVCR
Figure 4.4: I-V characteristics of RITDs showing highest PVCR for these 3 different structures.
from RITD042clad, indicating RITD042clad can withstand a higher thermal budget. Consequently, RITD042clad demonstrates the highest PVCR among these three structures.

The effect of the SiGe cladding layer can also be demonstrated by Fig 4.6 which shows a comparison of the isothermal I-V characteristics of these three structures all annealed at 825°C for 1 minute. All three of these structures show similar valley current density indicating equivalent point defect removal, while RITD042clad shows the highest peak current density, due to the least amount of B out-diffusion.

To approach the interdiffusion from a different angle, a commercial software package [62] was employed to predict the dopant displacement during the post-growth
Figure 4.6: The I-V characteristics of structures RITD141, RITD042 and RITD042clad are compared with all having undergone the same RTA heat treatment at 825°C for 1 minute.
RTA anneal. Figure 4.7(a) shows the simulated boron profile of RITD141, RITD042, and RITD042clad when subjected to a 1 minute anneal at 800 °C. RITD042clad, which has SiGe cladding layers on both sides of the B δ-layer, shows the sharpest B peak as expected. The boron profiles with phosphorus profiles of these 3 structures are shown in the inset of Fig. 4.7(a).

Figure 4.7(b) shows the band diagram calculated using the modeled interdiffusion profiles shown in Fig 4.7(a). Here a strong shift in the band diagrams is visible for the three structures modeled. This is consistent with the large changes in tunnel diode PVCR for the three different structures.
4.4 A Study of Post-growth Annealing Process

In section 4.3, the optimization of the RITD structure is presented. This section will discuss the optimization of post-growth annealing process.

4.4.1 Introduction

As device sizes shrink down, ultra-shallow junction formation become an increasingly important technique [32]. Low energy ion-implantation is commonly employed to form this junction. A subsequent annealing process is required to activate dopants and remove the point defects (Si-interstitials) due to the ion-implantation damage while minimizing the profile motion. Spike annealing technique is proved to be a success means to meet these requirement [74]. Due to the similarity between the issues of post-ion-implantation annealing in ultra-junction formation and post-growth annealing in RITD fabrication, spike annealing has been employed to improve the RITD performance, especially to increase PVCR. A complementary furnace annealing at low temperature with prolonged duration is also studied.

4.4.2 Spike Annealing

Realization of Spike Annealing Using RTP600S

The spike annealing is performed using the RTP600S system. The temperature profile of spike annealing is programmed as follows: The target temperature is 900 °C with the temperature ramping rate set as 150 °C/sec, which is the maximum value allowed by the RTA system. After 1 second holding time, the lamp is turned off and a large volume of N₂ gas starts to flow which cools down the chamber. The temperature dropping rate will depend on the flow rate of N₂ gas. However, the resulting temperature profile significantly deviated from the programmed one, as
shown in Fig. 4.8(a). The overshoot is as large as 200 °C due to the high temperature ramping rate. Furthermore, there exists another spike after the main spike, which will greatly increase the time at high temperature. The unpredictable and uncontrollable deviation from the programmed profile could render the spike annealing impractical for manufacturing.

To avoid the huge overshooting and the secondary spike, the heating process was manually terminated by turning off power to the lamp assembly. After user practice, a resolution of about 20 °C for the final annealing temperature can be obtained. Figure 4.8(b) shows the temperature profile for a 1000 °C spike annealing using this method. The average temperature ramping and dropping rate above 800 °C are 146 °C/sec and 100 °C/sec, respectively. The duration above 800 °C is as short as less than 4 seconds.

**Device Results**

A standard RITD, which is a replica of RITD042clad discussed in Sect. 4.3, was repeated and subjected to spike annealing. Figure 4.9 shows the performance of devices annealed for 1-minute at various temperatures. The RITD exhibits the highest PVCR of 3.5 with a $J_p$ of 1.0 kA/cm$^2$ by 825 °C 1-minute annealing, which is slightly inferior to the RITD042clad studied in Sect. 4.3 possibly due to slightly variations in the growth or reactor conditions.

Portions of the same RITD042clad sample were then spike annealed at 985 °C, 1000 °C, and 1012 °C, respectively. The resulting I-V characteristics are plotted in Fig. 4.10. The highest PVCR achieved was 3.6 with a $J_p$ of 1.1 kA/cm$^2$ was obtained using a 1000 °C spike annealing condition, which is slightly higher than 3.5, the best value obtained by a fixed 1-minute annealing. An RITD spike annealed at 985 °C
showed a PVCR of 1.3 and $J_p$ of 4.1 kA/cm$^2$, while spike annealing up to 1019 °C turns the RITD into a usual diode with no visible NDR region presented.

Figure 4.11 plots the PVCR vs. annealing temperature for both 1-minute RTA and spike annealing durations. The data shows that when the RITDs are spike-annealed at high temperature, the PVCR is extremely sensitive to the annealing temperature change, because the dopant diffusion rates exponentially increases with furnace temperature. A small annealing temperature change ($< 20$°C) can greatly alter the PVCR. The extreme thermal sensitivity of the PVCR suggests that a PVCR higher than 3.6 could be obtained using a different annealing furnace that enable sub-second duration and much tighter control on the spike annealing temperature. In conclusion, spike annealing can lead to a slightly higher PVCR than a 1-minute
Figure 4.9: PVCR, $J_p$, and $J_v$ as functions of 1-minute RTA annealing temperature
Figure 4.10: The I-V characteristics of RITDs spike-annealed at various temperatures.
RTA anneal, as a result of the more effective point defect removal and reduced dopant profile changes.

### 4.4.3 Low Temperature Long Duration Annealing

In the previous section, samples were spike annealed at a high temperature using an extremely short duration pulse. To complement the spike annealing study, the same RITD layers were also furnace annealed at lower anneal temperatures (600 °C) for prolonged times up to 48 hours. The PVCR, $J_p$ and $J_v$ vs. annealing time are plotted in Fig. 4.12. The highest PVCR of 1.7 with $J_p$ of 4 kA/cm² was obtained by 11-hour annealing, and it is substantially lower than the PVCRs obtained by 1-minute annealing. However, compared to the 1-minute annealed RITDs, furnace annealed
RITDs show higher peak current densities, which suggest that further increasing annealing time may improve the PVCR, but probably not to a significant degree.

### 4.4.4 Discussion

Both spike annealing (high temperature, short duration) and furnace annealing (low temperature, prolonged duration) were studied. A 1000 °C spike annealing only slightly improved the PVCR from 3.5, the highest PVCR obtained using a 1-minute RTA, to a value of 3.6. However, the PVCR of RITDs is very sensitive to the change of spike annealing temperature compared to 1-minute RTA temperature. A small change of spike annealing temperature (within 20 °C) will significantly degrade RITD performance. Furnace annealing at low temperatures with prolonged durations result
in substantially lower PVCRs, which also suggests that rapid thermal annealing is desirable and even optimal to obtain the highest PVCR.

4.5 Conclusion

To obtain a higher PVCR, it is desirable to anneal the RITD to effectively remove point defects with a concurrent minimal dopant profile redistribution. In this chapter, two studies aiming towards less dopant diffusion but with more effective defect removal are presented. The first approach is to optimize the RITD structure itself. A SiGe cladding layer successfully suppressed B out-diffusion from the $\delta$-doping spike, so that higher annealing temperatures could be used to more effectively remove the point defects created by LT-MBE. The second approach tried spike annealing to limit the motion of dopant profile. Both of these approaches proved to be successful, but the former much than the later. Long duration anneals at lower temperatures were ineffective in reducing point defect densities at a faster rate than dopant diffusion.
CHAPTER 5

THE EFFECT OF SPACER THICKNESS ON SI-BASED RITD PERFORMANCE

5.1 Introduction

Peak current density \( (J_p) \) is another important parameter in addition to PVCR. For high speed applications, a large \( J_p \) is required to quickly charge or discharge the junction capacitance; for low power applications, a small \( J_p \) is desired to lower the power consumption. The objective of this study is to explore the \( J_p \) range over which the Si-based RITD can reach. The direct pathway to vary \( J_p \) is simply to adjust the spacer thickness, since the \( J_p \) of the RITD is exponentially dependent on the thickness of the tunneling barrier. The effects of the spacer thickness on PVCR and VS are also studied.

5.2 Experimental and Device Structures

Epitaxial growth was provided by Dr. Phillip Thompson at NRL using molecular beam epitaxy (MBE) with elemental Si and Ge in electron-beam sources. The structures were grown on 75mm B-doped \( (\rho = 0.015 - 0.04\Omega \text{ cm}) \) Si (100) wafers. The doping level for both \( n^+ \) and \( p^+ \) layers are \( 5 \times 10^{19} \text{ cm}^{-3} \), while both the B and P delta-doping sheet concentration were maintained at \( 1 \times 10^{14} \text{ cm}^{-2} \).
Prior to device fabrication, portions of the grown wafers were annealed using a forming gas ambient (N₂/H₂) in a Modular Process Technology corporation RTP-600S furnace at various temperatures for 1 minute. Ti/Au dots with various diameters were patterned on the surface of the wafers via standard contact lithography. A buffered oxide etch was used prior to metallization. Using the metal dots as a self-aligned mask, HF/HNO₃ wet etching was performed to isolate the diodes into mesas. Finally, a Ti/Au backside contact was evaporated on all of the samples.

The basic structure, shown in Fig 5.1, of the Si-based RITDs was grown by LT-MBE. The spacer layer sandwiched between the two δ-doping layers is comprised of two layers, an intrinsic Si layer of thickness \( L_1 \) which is below the P δ-doping layer and an intrinsic Si₀.₆Ge₀.₄ layer of thickness \( L_2 \) that is above the B δ-doping layer. Two sets of RITDs were grown. The first set has thin spacers with thickness of 6 nm \( (L_1 = 2 \text{ nm} / L_2 = 4 \text{ nm}) \), 5 nm \( (L_1 = 1.5 \text{ nm} / L_2 = 3.5 \text{ nm}) \), 4 nm \( (L_1 = 1 \text{ nm} / L_2 = 3 \text{ nm}) \), 3 nm \( (L_1 = 1 \text{ nm} / L_2 = 2 \text{ nm}) \), 2 nm \( (L_1 = 1 \text{ nm} / L_2 = 1 \text{ nm}) \) and 1 nm \( (L_1 = 0.5 \text{ nm} / L_2 = 0.5 \text{ nm}) \). The second set has thick spacers with a fixed \( L_2 \) of 4 nm, and the total spacer thickness of 8 nm \( (L_1 = 4 \text{ nm}) \), 10 nm \( (L_1 = 6 \text{ nm}) \), 12 nm \( (L_1 = 8 \text{ nm}) \), 14 nm \( (L_1 = 10 \text{ nm}) \), 15 nm \( (L_1 = 11 \text{ nm}) \), and 16 nm \( (L_1 = 12 \text{ nm}) \). Note, there are SiGe cladding layers surrounding the B δ-doping layer in order to suppress the B outdiffusion, so that the sharp B peak can be maintained during the growth and short 1-minute post-growth annealing. As a result, the Si/SiGe RITDs have an elevated thermal budget to remove point defects within the spacer more effectively, so that the valley current will be decreased, which leads to a higher PVCR [67]. Also, the inclusion of a SiGe alloy to the tunnel spacer...
acts to increase momentum mixing which enhances tunneling probability and current density provided the critical thickness is not exceeded.

5.3 Device Results

5.3.1 Device Results of Set 1 (Spacer Thickness ≤ 6 nm) and an Optimized RITD

Pieces of all each RITD of Set 1 were annealed at 600, 650, 700, 750, 775 °C for 1 minute. It is observed that there is a tradeoff between high $J_p$, shown in Figure 5.2(a) versus spacer thickness, and high PVCR, shown in Figure 5.2(b) versus spacer thickness. From the data it is evident that at each spacer thickness there is an optimal annealing temperature for maximum PVCR and a set of lower annealing temperatures for more elevated peak current densities. A maximum PVCR is reached by annealing the sample at the highest annealing temperature possible, to effectively remove the point defects created by the LT-MBE process that contribute to a defect related tunneling valley current component, before diffusion of the δ-doping layers and Ge within the tunneling spacer results in a marked modification to its original structure.

For instance, the sample with a 2 nm spacer has its maximum peak current density of 42 kA/cm$^2$ and PVCR of 1.6 when annealed at 600 °C for 1 minute. The rolloff of $J_p$ as the spacer thickness is reduced below 3 nm, shown in Fig 5.2(a), is indicative of the interdiffusion at the p-n junction that results in an actual increase in the depletion width, and subsequently the tunneling distance and therefore a reduction in tunneling probability. The optimal spacer thickness for the highest peak current density decreases if the annealing temperature is lowered and interdiffusion is suppressed. Generally, below a nominal spacer thickness of 4-6 nm, the PVCR
Figure 5.1: A schematic of the basic RITD structure used in this study
Figure 5.2: 1 minute RTA anneals varying from 650°C to 775°C decreases as the spacer becomes thinner, as shown in Fig 5.2(b). This is because when the $p$ and $n$ δ doping planes are placed closer to each other, more dopant pair defect states will be formed within the spacer, hence more energy levels exist in the forbidden energy bandgap for the excess current to tunnel through.

5.3.2 3-nm-spacer RITD With Optimized P Dopant Profile Showing Record High Peak Current Density

The offsetting trends of PVCR and $J_p$ vs. spacer thickness indicate the trade-off between high PVCR and high $J_p$. Ideally, RITDs with a high $J_p$ should concurrently manifest a reasonable PVCR. The maximum RF power from a tunnel diode when
biased in its NDR region for high frequency oscillator applications can be simply expressed as:

\[
\frac{3}{16} \times A \times \Delta V \times (J_p - J_v)
\]  

(5.1)

where \( \Delta V \) is the voltage swing from the peak to the valley, \( J_p - J_v \) is the current density swing, and \( A \) is the area of the tunnel diode [154]. The magnitude of \( J_p \) directly impacts the speed index, \( I_{\text{peak}}/C_j \), which is another important figure-of-merit for tunnel diodes, where \( I_{\text{peak}} \) is the maximum current before entering the NDR regime and \( C_j \) is the capacitance of the tunnel diode. Since \( J_p - J_v \) figures so prominently in both the maximum RF power and is also related to the speed index, this is a factor that we should optimize, which represents the available current density swing. Therefore, RITD with a 3 nm was chosen for further optimization due to its highest current density swing.

A simulation program was developed to predict the diffusion behavior of n and p type dopants in RITDs and relate this to experimental RITD results. Diffusivity coefficients are calculated by their Arrhenius equation and adjusted for good agreement with SIMS data of bulk Si with several \( \delta \)-doping layers inserted during growth under similar conditions by LT-MBE [139]. A numerical algorithm was employed so that the simulation program can start with an arbitrary doping profile and then simulate interdiffusion as a function of temperature and time. Effects of Ge concentration, which reduces B diffusivity, were also included. The simulations show that mismatched p and n \( \delta \)-doping spikes on either side of the junction will result in a widened depletion region (tunneling barrier) width. As shown in Fig. 5.4, for an RITD with a 6nm Si intrinsic layer, the minimum depletion region width occurs when Sb/B is around 1.5.
Figure 5.3: Band diagram of Si/SiGe RITD with 3 nm spacer at an applied bias of 0.4V showing the conduction band longitudinal, $X_z$, and transverse, $X_{xy}$, valleys and heavy hole, light hole and split off hole bands. The fundamental $X_z$, $X_{xy}$, LH and HH states in the quantum wells are shown. It is calculated by solving five independent single band effective mass equations. The potential is calculated semi-classically.
Therefore, $J_p$ are sensitive to the relative doping levels in the $\delta$-doped peaks. By increasing the P $\delta$-doping concentration to $3.4 \times 10^{14}$ cm$^{-2}$ while maintaining the B $\delta$-doping concentration at $1 \times 10^{14}$ cm$^{-2}$ in an RITD having a 3nm spacer ($L_1 = 1nm$ / $L_2 = 2nm$), the $J_p$ increased to 63 kA/cm$^2$ with an associated PVCR of 2.5. Figure 5.3 presents the calculated band diagram of this Si/SiGe RITD by Prof. Roger Lake at University of California at Riverside. It shows the conduction band longitudinal, $X_z$, and transverse, $X_{xy}$, valleys and heavy hole, light hole and split off hole bands at an applied bias of 0.4V. The fundamental $X_z$, $X_{xy}$, LH and HH states in the quantum wells are shown. It is calculated by solving five independent single band effective mass equations. The potential is calculated semi-classically. P $\delta$-doping of $3.4 \times 10^{14}$ cm$^{-2}$ is assumed spread out over 3 nm and the B $\delta$-doping of $1.0 \times 10^{14}$ cm$^{-2}$ is spread out over 2 nm, based upon previous secondary ion mass spectroscopy (SIMS) measurement.

To further increase $J_p$, another Si/SiGe RITD was grown with a sharpened P $\delta$-doping peak by dropping the substrate temperature following the growth of the P $\delta$-doping spike to reduce P segregation. After 4 nm of growth at 250 °C, the growth is momentarily stopped and the substrate temperature increased to 450 °C before resuming growth of the final 100 nm P-doped $n^+$ contact layer. Because of the higher substrate temperature relative to the other $n^+$ contact layers, this layer may have a slightly lower concentration of dopants. This results in a measured $J_p$ of 151 kA/cm$^2$ with PVCR of 2.0, which corresponds to a $J_p - J_v$ of 76 kA/cm$^2$, as shown in Figure 5.5. To the authors’ knowledge, this is the highest $J_p$ ever reported for Si-based interband tunneling diodes and the highest $J_p - J_v$ current span. The 151 kA/cm$^2$ current density reported here is commensurate to a number of reports for III-V-based
RTDs [123]. The actual active diode area is less than the lithographic area, used in these current density calculations, due to the undercut of the mesa isolation etching during wet etching of the mesa diode. SEM measurements show the undercut is on the order of 0.2 $\mu$m, which would inflate the actual $J_p$ value by about 18% over the conservative value calculated here.

It should be pointed out that, no area dependence on $J_p$ was observed in our diodes. $J_p$ is very consistent while measuring diodes with different sized areas, which indicates that high current values can simply be obtained by increasing the diode area. This property makes this kind of Si-based RITD particularly suitable for high power oscillator applications. At the very high currents measured here, the nominal series resistance can act to skew the shape of the I-V characteristics. For the Si/SiGe
Figure 5.5: Measured I-V characteristics of 3nm Si/SiGe RITD with elevated and sharpened P \( \delta \)-doping peak showing \( J_p \) of 151 kA/cm\(^2\) with PVCR of 2.0, which corresponds to a current span of 76 kA/cm\(^2\).
Figure 5.6: A graph of peak-to-valley current ratio plotted against the current density of a number of Si-based interband tunnel diodes including those presented in this study.
RITD showing a $J_p$ of 151 kA/cm$^2$, $R_s$ is estimated to be 14.1 Ω using the same method in Ref. [141]. The consequence of the series resistance leads to a measurement artifact for higher current density samples. Voltage sweeps in backwards and forwards directions showed a hysteresis indicating that the valley position actually becomes tucked under the peak position for the higher current density devices, but due to restrictions in measurement systems like parameter analyzers, the position of the valley when sweeping forward-only is identified incorrectly. Figure 5.5 illustrates how the measured NDR region has become seemingly exactly vertical due to the peak current position being shifted farther to the right than the valley current position by the series resistance. Previous RITD results of a 22 kA/cm$^2$ sample using a curve tracer for I-V measurements have shown this artifact is avoided [110]. This hysteresis is not evident for current densities below about 5-10 kA/cm$^2$. As a result of the data skewing, the PVCR was falsely recorded by as much as 10% less for the 151 kA/cm$^2$ sample than its actual intrinsic PVCR. By extrapolating $I_{\text{measured}} - V_{\text{measured}}$, the tucked valley voltage can be obtained as 620 mV, rather than 724 mV as it appears in the parameter analyzers. Thus, the real PVCR is estimated to be 2.2 at room temperature. The I-V characteristics of the intrinsic RITD, can then be extracted and is plotted in Fig 5.5 also adjusted for the mesa undercut and series resistance. Note, both $V_v$ and $V_p$ are shifted leftwards towards smaller values, with $V_p$ equal to 306 mV and $V_v$ equal to 432 mV.

Pulsed measurements with low duty cycles were performed to remove any contributions to internal Joule heating that could deleteriously affect RITD performance. Preliminary indications show no heating degradation is present, even though no heat sinking precautions were taken.
As noted above, the reason that we have concentrated on maximizing the peak current density of the RITD is that it is a critical component for determining the speed index of the device. To facilitate direct comparisons, the speed index units below will all be converted to the common units, mV/ps. Reports from the 1960’s indicated that the speed index for a traditional Si Esaki was 1.2 mV/ps [43]. RF measurements from Auer et al. [4] indicated that a SiGe RITD with a PVCR of 2.1 and peak current density of 0.5 kA/cm$^2$ had a speed index of 0.46 mV/ps. Dashiell et al. [30] also performed RF measurements on a Si Esaki diode that exhibited a PVCR of 1.02 and a peak current density of 16 kA/cm$^2$. Their measurements indicated an impressive speed index of 7.1 mV/ps. However, the results presented here achieve an extremely high peak current density of 151 kA/cm$^2$ that equates to an estimate of the speed index equal to 34 mV/ps, assuming the mesa diode is a parallel plate capacitor with the intrinsic thickness equal to the 3 nm tunneling spacer between the two $\delta$-doping layers. Finally, Fig 5.6 summarizes these new results by plotting the PVCR against its corresponding $J_p$ for a number of previous Si-based interband tunnel diodes including those presented in this study. The plotted data from this study shows the maximum peak current density with its corresponding PVCR. Data points from other research groups are shown as open squares, data from previous work by the authors is shown as solid circles, and data from this study is shown as solid stars for directly measured data and open stars for extrapolated data.

In conclusion, our study shows over 151 kA/cm$^2$ peak current densities and PVCR greater than 2 in Si/SiGe resonant interband tunneling diodes at room temperature, which results in an estimated speed index of 34 mV/ps. This result demonstrates the high potential of this type of Si-based tunnel diode for mixed-signal applications.
5.3.3 Device Results of Set 2 (Spacer Thickness \( \geq 6 \) nm)

Pieces of all the RITD of Set 2 were annealed at 800, 825, 850, 865 °C for 1 minute. Figure 5.7(a) and Fig. 5.7(b) show the \( J_p \) and PVCR for RITDs with various spacer thickness as a function of annealing temperature. Clearly, both the temperatures which yield highest \( J_p \) and PVCR shift to higher values, as the spacer become thicker. This trend is also observed in RITDs of Set 1. RITDs with a 16 nm spacer exhibit the lowest \( J_p \) of 20 mA/cm\(^2\) with PVCR of 1.35. With the highest \( J_p \) of 151 kA/cm\(^2\), the \( J_p \) of Si-based RITDs can be varied 7 orders of magnitude by varying the spacer thicknesses from 3 nm to 16 nm, which illustrates the tremendous flexibility in engineering the \( J_p \) for different applications. Figure 5.8 summarizes the results of the work of RITD with thick spacer (\( \geq 6 \) nm).
Figure 5.8: A graph of the peak-to-valley current ratio plotted against the peak current density of a number of Si-based interband tunnel diodes including those presented in this study.
5.4 Discussions

In this section, the results of RITDs of both Set 1 and Set 2 are combined. The spacer thickness effect on RITD performances are discussed.

5.4.1 The Effect of Spacer Thickness on PVCR

Figure 5.9 plots the highest PVCR obtained from each structure as a function of spacer thickness. The annealing temperatures to obtain the PVCRs are also labelled. The graph shows that RITDs with a 6 nm spacer lead to the highest PVCR. Both decreasing and increasing spacer thickness will result in a reduced PVCR. It is also observed that the optimal annealing temperature increases from 650 °C to 850 °C as spacer thickness increases from 1 nm to 16 nm.
The decline of the PVCR as the spacer thickness exceeds 6 nm is due to the decreasing ratio between the desired tunneling current and the excess current. Both the desired tunneling current and excess current are exponentially dependent on the tunneling barrier according to Chynoweth’s theory [23], however, it is hypothesized that the desired tunneling current may decay faster than the excess current with increasing tunneling barrier. In another words, the tunneling selection rules are reduced for thicker spacer thicknesses.

The hypothesized tunneling selection rule can be validated by the fact that RITDs with thin spacers outperform RITDs with thick spacer under the same low temperature annealing. For example, an as-grown 3-nm-spacer RITD exhibits a PVCR of 1.6 with the presence of unremoved point defects, while a 16-nm-spacer doesn’t show any NDR until the annealing temperature is increased to 825 °C to remove most of the point defects. The performance difference indicates that thin tunneling barrier intrinsically allow more desired tunneling current than excess current, therefore larger PVCR.

However, as the spacer thickness is reduced below 6 nm, the PVCR decreases with a dropping optimal annealing temperature. This is because the decreasing spacer thickness will result in an increasing amount of opposite carrier type dopant pairs within the tunneling barrier, which will lead to a larger excess current relative to the desired tunneling current ratio. Furthermore, the interdiffusion of dopants during post-growth annealing leads to more dopant pairs being formed, therefore, RITDs with a thin spacer (≤ 6 nm) can not be annealed at temperature as high as the RITDs with thicker spacers (≥ 6 nm) to effectively remove point effects. Therefore, RITDs with thin spacers (≤ 6 nm) have a lower optimal annealing temperature, and
therefore there exists more point defects and dopant pairs within the tunneling barrier than comparable RITDs with thicker spacers (≥ 6 nm) which are annealed at higher temperatures.

In conclusion, RITDs with a 6 nm spacer layer thickness lead to the highest recorded PVCR. Thicker spacers lead to smaller measured PVCRs, because the desired tunneling current decays faster than the excess current as tunneling barrier thickness increase. However, decreasing the spacer thickness below 6 nm will not yield higher PVCR due to the creation of more dopant pairs within the tunneling barrier as the $p$ and $n$ δ doping planes come closer, which provides energy levels in the forbidden bandgap for the excess current to tunnel through to the other side of the junction. Furthermore, RITDs with thinner spacers can not be annealed at high enough temperatures to effectively remove point defects, else interdiffusion will become excessive and lead to more dopant pairs. As a result, RITDs with thinner spacers will have more point defects and dopant pairs formation within the tunneling barrier than RITD with 6 nm intrinsic spacer thickness, consequently, smaller PVCRs are observed.

5.4.2 The Effect of Spacer Thickness on Peak Current Density

Fig. 5.10 plots $J_p$ vs. spacer thickness ranging from 1 nm to 16 nm. The highest PVCR obtained from each structure as a function of spacer thickness is also plotted. The solid triangles (▲) indicate the maximum PVCR by varying the annealing temperature for each RITD spacer thickness. The solid squares (■) show the corresponding $J_p$ at that optimized PVCR. The open squares (□) illustrate the spread in $J_p$ at various temperatures as the annealing temperature is varied. For clarity, the
Figure 5.10: The effect of spacer thickness on peak current density. The highest PVCR for each structure as a function of spacer thickness is also plotted.

PVCR at the different annealing temperatures examined are not plotted here. The highest $J_p$ of 151 kA/cm$^2$ with a PVCR of 2.0 was obtained with a 3 nm spacer, while the lowest $J_p$ of 20 mA/cm$^2$ with a PVCR of 1.35 was obtained with a 16 nm spacer. It is observed that, $J_p$ increases exponentially as the spacer thickness decreases from 16 nm to 3 nm, due to the increasing tunneling barrier. The relationship between $J_p$ and spacer thickness, $W$, can be fitted exponentially as:

$$J_p = 1.82 \times 10^6 \times 10^{-0.47W} \text{A/cm}^2$$  \hspace{1cm} (5.2)

Further reduction of the spacer thickness leads to a broadened depletion region due to dopant interdiffusion and corresponding compensation, therefore, $J_p$ starts to reduce. By examination of the fitted equation of the $J_p$ data of the RITDs versus spacer thickness, the y-intercept indicates that the $J_p$ of a Si-based RITD with a 0 nm tunneling barrier is about 1.82 MA/cm$^2$, which can be regarded as the upper limit of $J_p$ for Si-based RITDs.
Ideally, a low $J_p$ could be obtained by simply increasing the spacer thickness. However, the decay of the PVCR with increasing spacer thickness sets a lower limit on this $J_p$. Figure 5.11 shows the I-V characteristics of the RITDs annealed at 825 °C for 1 minute. It clearly shows that the NDR region become diminished as spacer thickness is increased. Figure 5.12 plots the $J_p$ as a function of PVCR for RITDs of Set 2 annealed at 825 °C. Surprisingly, a linear correlation is observed between the $J_p$ and PVCR. By extrapolating the measured data, a lower limit of imposed $J_p$ can be projected as about 3 mA/cm$^2$.

In conclusion, the peak current density of Si-based RITDs is exponentially dependent on the spacer thickness. The highest $J_p$ of 151 kA/cm$^2$ is obtained with a 3 nm spacer, while a 16 nm spacer yields the lowest recorded $J_p$ of 20 mA/cm$^2$. Overall, the
range of $J_p$ for the Si-based RITDs reported here spans nearly 7 orders of magnitude, which make this device very adaptable for disparate applications. The interdiffusion and compensation of dopants broadens the tunneling barrier and reduces $J_p$ when the spacer thickness is further decreased below 3 nm. Eventually, the decreasing PVCR with increasing spacer thickness limits the lowest $J_p$ that can be achieved by the reduction in the rating of the desired tunneling current to the undesired excess current.

### 5.4.3 The Effect of Spacer Thickness on Voltage Swing

As discussed in Section 2.2.1, voltage swing is an important parameter related to the noise margin for digital applications. A large VS will lead to a large separation between two stable operating states, hence a large noise margin can be achieved. The value of the voltage swing is not affected by the series resistance, which makes
the voltage swing more useful than voltage span, which is defined as the difference between the peak voltage and valley voltage.

Like PVCR and $J_p$, voltage swing is also dependent on the annealing temperature. Figure 5.13 shows the dependency of voltage swing and PVCR for an 8-nm-spacer RITD on the annealing temperature. It is observed that the voltage swing and PVCR are very well correlated. All the RITD structures in this study exhibit a close correlation between PVCR and voltage swing, i.e., the optimal annealing temperature for PVCR generally yields the highest voltage swing. Figure 5.14 plots the highest VS and PVCR obtained from each structure vs. spacer thickness ranging from 1 nm to 16 nm. A good correlation between PVCR and voltage swing is also observed again.

The voltage swing is defined as the difference between the second voltage and peak voltage. For an intrinsic Si-RITD with zero series resistance, the second voltage of an intrinsic Si-based RITD is generally smaller than 0.7 V, therefore, the thermal
Figure 5.14: Voltage swing and PVCR as a function of spacer thickness.

diffusion current can be neglected in the range from valley voltage to second voltage. As a result, in this range, the excess current dominates and the I-V characteristics appear to be a straight line when plotted on a semi-log scale. As discussed in Chapter 4, RITDs with a higher PVCR have a smaller excess current component, which results in a larger second voltage. The above analysis can be clearly observed by examining Fig. 5.15, where the I-V characteristics of RITDs with 14 nm and 15 nm spacers are normalized to the same peak current as an RITD with a 16 nm spacer. Clearly, the RITD with a 14 nm spacer exhibits the highest PVCR, because it has the smallest excess current, which also results in the largest voltage swing.

The above analysis is based on the assumption that the excess currents for different RITDs have the same slope in a semi-log scale. However, according to Chynoweth’s
Figure 5.15: The I-V characteristics of 825 °C annealed RITDs with 14 nm, 15 nm, and 16 nm spacer. The current of RITDs with 14 nm and 15 nm spacers are normalized to peak current of an RITD with a 16 nm spacer.
excess current equation, which is repeated here:

\[ I_x = A \times D_x \exp\left\{ \left( -\frac{\alpha_x \times W \times e^{0.5}}{2} \right) [E_g - eV + 0.6e(V_n + V_p)] \right\} \]  \hspace{1cm} (5.3)

the slope will vary with the tunneling barrier width \( W \). A thicker tunnel barrier will result in an excess current with a larger slope in the semi-log scale, hence a smaller second voltage. Therefore, it can be hypothesized that for two Si-based RITDs with the same PVCR, the RITD with a thinner tunneling barrier will exhibit a larger voltage swing. This is verified by re-plotting Fig. 5.14 into Fig. 5.16, where the voltage swing is plotted as a function of PVCR instead of spacer thickness. The solid line represents the data from RITDs of Set 1 (spacer thickness \( \leq 6 \text{ nm} \)), while the dashed line represents the data of RITDs from Set 2 (spacer thickness \( \geq 6 \text{ nm} \)). The fact that the solid line is well above the dashed line verifies this hypothesis. Note, the solid line starts to drop sharply between the 2 nm and 3 nm data points, which is indicative of the increasing tunneling barrier width due to dopant interdiffusion that leads to compensation, when the spacer thickness is reduced from 3 nm to 2 nm. It is also consistent with the fact that an RITD with a 3 nm spacer yields the highest \( J_p \).

In conclusion, voltage swing is dependent on spacer thickness, because (1) spacer thickness affects PVCR (the ratio between desired tunneling current to excess current); and (2) spacer thickness affects the slope of the excess current under semi-log scaling.

5.5 Demonstration of Low Power 1T TSRAM

To demonstrate the concept of 1-T TSRAM memory cell shown in Fig. 3.11, a low-frequency breadboarded circuit was constructed using a commercial N-channel
Figure 5.16: The voltage swing as a function of PVCR

depletion mode FET as the access control to the storage node. To ease the requirement for small leakage current and to ensure latching characteristics, RITDs with 10 \( \mu \)m diameters, which show PVCR of 2.2 and \( J_p \) of 0.5 A/cm\(^2\), were fabricated and used in this circuit. \( V_{DD} \) was biased at 0.5 V and \( V_{SS} \) was grounded. Figure 5.17 shows the signals of 100 KHz word line and 50 KHz bit line as well as the resulting waveform measured at the storage node. The "write" operation was effectively demonstrated. When the word line is high, the SN will copy the value on the bit line, and keep it until the next write cycle begins. The state of "0" and "1" are 0.05 V and 0.46 V, respectively. The standby power of this 1-T TSRAM is estimated to be 75 nW/cell using 10 \( \mu \)m diameter RITDs. Since previous Si-based RITD studies have shown no area dependence, the RITD device area could be easily scaled downwards accordingly leading to an even further reduction in standby power. It is believed that
Figure 5.17: An oscilloscope capture of the measured waveforms from the word line, bit line and the resulting storage node showing 1T TSRAM write functionality.

a 0.25 µm diameter RITD cell would exhibit a 1600 × reduction in standby power estimated to be about 50 pW/cell.

5.6 Conclusion

In this chapter, the dependence of PVCR, \( J_p \), and voltage swing on spacer thickness are discussed. The highest PVCR results from a 6 nm tunneling spacer thickness. Thicker spacers lead to diminished PVCRs, because the desired tunneling current decays faster than the excess current as the tunneling barrier thickness increases. Reducing the spacer thickness also will degrade PVCR due to dopant pairs formed within the tunneling barrier that create defect sites that contribute to excess current. A record high \( J_p \) of 151 kA/cm\(^2\) is obtained with a 3 nm tunneling spacer thickness. Reducing the spacer thickness does not yield a higher \( J_p \), because dopant interdiffusion effectively broadens the tunneling barrier. Increasing the spacer thickness leads
to an exponentially decreasing $J_p$. A 16 nm tunneling spacer thickness yields the lowest $J_p$ measured at 20 mA/cm$^2$. The obtained $J_p$ span of Si-based RITDs fabricated and tested here is over nearly 7 orders of magnitude. Spacer thickness affects the voltage swing in the same way as it affects PVCR. Furthermore, it affects the voltage swing by changing the slope of the excess current on a semi-log scale. A low power 1-T TSRAM was demonstrated using the low current density Si-based RITD developed here.
6.1 Introduction

As ULSI moves towards deep-submicron technology (< 90 nm), chip area, signal delay and dynamic power dissipation are becoming dominated by interconnections rather than the intrinsic device speed [116]. Compared to conventional binary logic, multiple-valued logic (MVL) has a tremendous potential to overcome the limitations associated with interconnection complexity, because more information can be conveyed by multivalued signals than binary logic, so that fewer interconnects are required to transmit the same information [130]. The success of the MVL approach is greatly dependent on the availability of devices which are suitable for MVL operations. Due to the bi-state nature of conventional transistors, the resulting MVL basic building blocks are relatively complex, which would unfavorably increase device count and offset the advantages of MVL. With the unique folded I-V characteristics, multiple-peaked tunneling diodes are ideal for MVL implementation, because multi-level quantization and switching between several operation points can be very easily obtained. This is clearly evident when a resistive load line or transistor load is
placed across multiple negative differential resistance (NDR) peaks. Since MVL circuitry was demonstrated by using a multiple-peaked resonant tunneling diode (RTD) for the first time [105], many RTD-MVL circuits, such as multi-valued memory cell, analog-to-digital converters (ADC), counter, decoder and programmable logic array (PLA) [81] with greatly reduced complexity and component count have been reported. Ultra-high circuit speed is also achievable due to the picosecond switching speed of multiple-peaked RTDs. However, all these above mentioned multiple-peaked RTDs utilize III-V semiconductors, which are not compatible with mainstream Si CMOS technology. The recent development of Si-based resonant interband tunneling diodes (RITD) [5, 6, 7] and successes in vertical integration of RITDs [7, 8, 9] show great potential for their integration with CMOS transistors [7] and Si/SiGe heterojunction bipolar transistor (HBT) technology [8] for highly functional tunnel diode-transistor circuits. In this chapter, the first double peaked Si-based tunneling structure, in a vertical stack which is suitable for MVL operations, is presented. A tri-state logic circuit is then demonstrated using the vertical RITD stack with an external resistor.

6.2 Vertically Integrated RITD Pair I

The generic structure of a single Si-based RITD is shown in Fig. 6.1(a). Figure 6.1(b) shows the structure of the vertically stacked RITDs with an npnp configuration. The top RITD and bottom RITD have the same spacer configuration with L1 of 4 nm and L2 of 4 nm in order to obtain similar PVCR and \( J_p \) values. Note, there is a backwards diode between the top diode and bottom RITD, which will be reverse biased during active operation, that effectively connects the top RITD and bottom RITD as a small series resistance, under the forward biasing condition for the
Figure 6.1: (a) Schematic of the generic Si-based RITD design used in this study, and (b) schematic of the vertically stacked RITD pair using an npnp configuration of two generic Si-based RITDs connected serially by a backwards diode.
vertically stacked RITDs. The entire vertically integrated RITD pair was grown by molecular beam epitaxy (MBE) using elemental Si and Ge in electron-beam sources on 75mm B-doped ($\rho = 0.015-0.04 \ \Omega \cdot \text{cm}$) Si (100) wafers. The doping levels for both n+ and p+ layers are $5 \times 10^{19} \ \text{cm}^{-3}$, while both the B and P-doping sheet concentrations were maintained at $1 \times 10^{14} \ \text{cm}^{-2}$. Prior to device fabrication, portions of the grown wafers were rapid thermal annealed (RTA) using a forming gas ambient ($\text{N}_2/\text{H}_2$) in a Modular Process Technology corporation RTP-600S furnace at various temperatures for 1 minute. Ti/Au dots with various diameters were patterned on the surface of the wafers via standard contact lithography and liftoff. A buffered oxide etch was used prior to metallization. Using the metal dots as a self-aligned mask, HF/HNO$_3$ wet etching was performed to isolate the diodes into mesas. Finally, a Ti/Au backside contact was evaporated on all of the samples.

Figure 6.2 shows the I-V characteristics of a vertically integrated RITD pair with the best combination of PVCR using an 825 °C, 1 minute anneal. Double NDR regions in the forward biasing condition were observed, with one diode showing a PVCR of 3.25 and $J_p$ of 0.37 kA/cm$^2$, and another diode showing a PVCR of 3.21 with $J_p$ of 0.39 kA/cm$^2$. Note, the peak voltage of the first NDR region occurs around 1.2 V, which is much higher than the 0.1-0.2 V observed for prior discrete RITDs [5,6,7]. Hysteresis was observed when the voltage was swept forward and backward, which is also indicative of a large series resistance [77]. To properly identify the specific contribution to the double NDR and large series resistance by the upper RITD, lower RITD and backwards diode, etching was performed to isolate each p-n junction. The I-V characteristics of both “discrete” RITDs are also plotted in Fig. 6.2 for comparison. The discrete upper and lower RITDs exhibit almost identical
Figure 6.2: Measured I-V characteristics of 50 µm vertically stacked RITD pair and “discrete” upper RITD, backward diode and lower RITD annealed at 825 °C for 1 minute I-V characteristics with their peak voltage around 0.2 V. The upper RITD shows a slightly lower peak current, therefore it will reach the bias state for NDR before the lower RITD in the integrated RITD pair and manifest as the first measured NDR for the vertical pair. The I-V characteristic of the “discrete” backward diode, Fig. 6.2, confirms that the large nonlinear series resistance in the integrated RITD pair causing the peak voltage shift and hysteresis originated from the reverse biased backwards diode.

6.3 Demonstration of Tri-State Logic

To demonstrate tri-state logic, the vertically stacked RITD pair was combined with a resistor. The stacked RITDs operated as the drive and a 1 kΩ off-chip resistor as the load, as shown schematically in Fig. 6.3(a). The load line analysis of the circuit
with a representative stacked RITD pair and 1 kΩ resistor is shown in Fig. 6.3(b).

The initial operating point of the tri-state latch is P1 by biasing $V_{\text{pulse}}$ with a DC bias of 5.8 V, a positive triggering pulse is then fed to the resistor to momentarily lift the load line past the first peak and the operating point is moved to P2 at the trailing edge of the pulse. Note, that during this “write” operation, $V_{\text{out}}$ deviates slightly from P2, until $V_{\text{pulse}}$ is returned to its quiescent state of 5.8 V. An even higher triggering pulse then allows P3 to be accessed. Similarly, negative pulses superimposed on the DC bias of 5.8 V can lower the load line past the valley region and shift the operating point backwards, stepping down from P3 to P2 or P1. Figure 6.3(c) shows the resulting waveform of the state transitions from “0” to “1”, “1” to “2”, “2” to “1” and “1” to “0”, effectively demonstrating the tri-state latching operation. The “0”,

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**Figure 6.3:** (a) circuit schematics of tri-state logic operation; (b) Load line analysis of the circuit with a representative vertically stacked RITD pair as the drive and 1 kΩ resistor as the load; (c) Oscilloscope capture of the resulting waveform with $V_{\text{pulse}}$ and $V_{\text{out}}$ showing tri-state logic functionality.
"1" and "2" latched states correspond to 1.05 V, 1.55 V and 2.04 V, respectively. Note, the intermediary point P2 can be bypassed when moving between states P1 and P3, although this operation is not shown here. Intrinsic switching speeds were not evaluated at this time as the circuit should be limited by the parasitics associated with the external and series resistance. Substitution of a monolithic transistor would greatly improve the switching speed.

The noise margin of each state was defined as the minimum value of the current difference between the operating point and peak, and the current difference between the operating point and valley [158]. In this circuit presented, using a DC bias of 5.8 V, the noise margin for states “0”, “1” and “2” were estimated to be 2.36 mA, 2.05 mA, and 1.42 mA, respectively. Therefore, the noise margin of this circuit is equal to 1.42 mA, which is limited by state “2”. By increasing the DC bias to 6.3 V and therefore equalizing the noise margin of states “0” and “2”, this circuit would have a maximum noise margin of 1.88 mA. Using a constant current source as the load should further improve the noise margin up to half of the peak and valley current difference.

6.4 Vertically Integrated RITD Pair II

Section 6.2 shows that vertically integrated npnp Si-based RITD pairs with double NDR regions under forward bias were successfully built. Tri-state logic was also demonstrated by a breadboarded circuit using the vertically integrated RITD pair as the drive and an off-chip resistor as the load. However, two issues associated with that vertically integrated Si based RITD design need to be addressed: (1) Since the two RITDs exhibit almost identical peak currents and valley currents, the pair is more
Figure 6.4: Structure of vertically integrated tunnel diode pairs II

susceptible to noise interference when using a constant-current-source as the load. For example, to make the transition from state “0” to “1”, the pulse lifting up the flat load line to pass the first peak may accidentally pass the second peak and reach state “2” with the presence of noise; (2) A large nonlinear series resistance originated from the backward diode that is needed to serially connect these two bipolar devices without introducing a reverse biased rectifying junction in series. A significant shift in the peak voltage positions resulted, which would lead to a larger power consumption. To solve these problems, a modified vertically integrated RITD pair with unequal spacer thicknesses and a δ-doped backward diode was fabricated.

Figure 6.4 shows the generic structure of the vertically stacked RITDs with an npnp configuration. The spacer configuration of the upper RITD was slightly modified with L1 increased from 4 nm to 4.2 nm, while the lower RITD was kept intact. The purpose of this modification is to lower the peak and valley current of the upper
RITD to facilitate a transistor type load, while keeping the peak current of the upper RITD greater than the valley current of the lower RITD to ensure tri-state logic operation. The backward diode in vertically integrated RITD pair I was formed naturally by the p+ injector layer of the top RITD and the n+ injector layer of the bottom RITD, which is essentially a p-n junction with doping levels on both sides of $5 \times 10^{19} \text{cm}^{-3}$ and no intrinsic spacer between the p and n sides. The relatively low doping density on both sides plus dopant diffusion during the 825 °C 1-minute rapid thermal annealing resulted in a wide tunneling barrier and a large nonlinear resistance, which unfavorably shifted the 1st peak to around 1.2 V. In this modified structure, a δ-doped backward diode is used to obtain a significantly higher doping density and a thinner tunneling barrier, as shown in Fig. 6.4(b). Both the B and P δ-doping layers have a sheet concentration of $0.25 \times 10^{14} \text{cm}^{-2}$. A 6 nm intrinsic spacer is inserted between the δ-doping layers to prevent dopant interdiffusion and compensation. However, it is problematic to grow B-doped layers on top of a P δ-doping layer due to P segregation. Segregated P atoms will incorporate into the overlayer and lead to an unintentionally doped spacer and compensate the B doped layer which will result in a smaller effective doping density. To minimize the effect of P segregation on both the backward diode and the upper RITD, a stop growth technique associated with a substrate temperature reduction to 320 °C to control the P segregation [60] was employed.

Figure 6.5 shows the I-V characteristics of the modified RITD pair with an 18 µm mesa diameter and post-growth annealed at 835 °C for 1 minute. The large peak voltage shift previously observed in the I-V characteristics shown in Sect. 6.2 is now greatly reduced, with the first peak occurring at 0.235 V and the second
Figure 6.5: I-V characteristic of vertically integrated tunnel diode pairs II.

Vertically Integrated RITD II
18 μm diameter
835°C annealed, 1 minute

Current (mA)

Voltage (V)

Lower RITD
Upper RITD
Backward Diode

0.0
0.5
1.0
1.5
0.0
0.5
1.0
1.5

-0.5

0.0

1.5

1.0

0.5

0.0

-0.5
peak occurring at 0.975 V. No hysteresis was observed in the NDR region. Etching was performed to isolate each p-n junction and characterize them separately. The zero bias junction resistance of the backward diode is estimated to be 280 Ω, which is about 350 times less than 0.1 MΩ, observed for the backward diode presented in Sect. 6.2. The zero bias junction resistances of the upper and lower RITDs are estimated to be 220 Ω and 80 Ω, respectively, which are comparable to the backward diode. Therefore, the peak voltage shift is greatly reduced in this study. I-V characteristics of the upper diode shows a PVCR of 3.5 with $J_p$ of 155 A/cm$^2$, and the lower diode shows a PVCR of 3.6 with $J_p$ of 515 A/cm$^2$. The slightly suppressed PVCR of the upper RITD may be due to some residual segregation of P from the backward diode despite the reduced growth temperature of 320 °C during the top layers or the prolonged reduced substrate temperatures. The unequal spacer thickness of the two RITDs results in differences in the peak and valley current differences between the upper and lower RITDs, compared with the original vertically integrated RITD pair in Sect. 6.2. The peak current difference is 0.68 mA and the valley current difference is 0.18 mA. This feature makes the modified RITD pair more suitable for circuit implementation using a constant-current-source load, such as a transistor. A current source load of 0.5 mA would result in 3 stable operational points, which are 0.17 V, 0.76 V and 1.29 V, respectively.

6.5 Conclusion

Vertically integrated npnp Si-based resonant interband tunneling diode (RITD) pairs were successfully built with double NDR regions under forward bias. Tri-state
logic was demonstrated by a breadboarded circuit using the vertically integrated RITD pair as the drive and an off-chip resistor as the load.

The asymmetric design manifests as unequal peak current densities that provides for much larger and uniform separation of the holding states for multi-valued logic. A $\delta$-doped backwards diode connects the two serially connected RITDs with a very small series resistance.

A vertically integrated and serially connected npnp Si-based resonant interband tunneling diode (RITD) pair was successfully built with PVCRs above 3.5. Double NDR regions under forward bias were observed. Small shifts in the peak voltage were obtained to lower power consumption by modifying the backward diode. Unequal peak currents facilitate circuit implementation with constant-current-source loads and larger noise margins.
CHAPTER 7

MODELING OF SI-BASED RITD

Since Si-based resonant interband tunneling diode (RITD) grown by low temperature Molecular Beam Epitaxy (LT-MBE) was built by Rommel et al, numerous studies have been carried out to improve its performance. Recently, monolithic integrations of RITD with HBT [4] and CMOS [5] have been realized. However, little work has been done to provide appropriate models for circuit designer, which limits the application of tunnel diodes. This chapter presents a unified model which combines both the small and large signal model of a RITD grown on Silicon-on-insulator (SOI) wafer. The RF performance of Si-based RITD was simulated using the small signal model. The effect of circuit elements on RF performance were discussed.

7.1 Small signal model of RITD

7.1.1 Device fabrication

Figure 7.2 shows the structure of RITD grown on SOI, which is the standard RITD (-1/4/2) structure with a 280 nm thick p+ buffer layer aiming at a better crystal quality on SOI wafer and a smaller series resistance. The doping level for both n+ and p+ layers are $5 \times 10^{19} \text{ cm}^{-3}$, while both the B and P δ-doping sheet concentration was maintained at $1 \times 10^{14} \text{ cm}^{-2}$. The structure was grown by low
temperature MBE using elemental Si and Ge in electron-beam sources on 4” B-doped high resistivity SOI (100) wafers. Prior to device fabrication, the grown wafer was rapid thermal annealed (RTA) using a forming gas ambient (N$_2$/H$_2$) in Modular Process Technology Corporation RTP-600S furnace at 825 °C for 1 minute. The diode has a double-mesa structure using standard photolithography. The first mesa of 10 μm diameter was defined by photoresist and formed by etching through the junction in a HF/HNO$_3$/H$_2$O mixture. The second mesa was aligned to the first mesa and formed by etching down to the SiO$_2$ layer using the same method. A photo-sensitive polyimide layer was then spincoated on the wafer followed by lithography to open the contact windows for both anode and cathode. The polyimide layer was then cured in N$_2$ ambient at 350 °C for 90 minutes. The thickness of polyimide layer was measured to be 4000 Å using Dektek. Another level of lithography was performed to define the pad. Finally, Ti/Al/Au was deposited followed by lift-off process.

7.1.2 DC and RF measurement

The diodes were measured DC as well as from 45 MHz to 5 GHz using a HP network analyzer. Figure 7.3 shows the I-V characteristics. PVCR of 2.9 with $J_p$ of 316 A/cm$^2$ was obtained. Smooth I-V curve indicates that there was no oscillation during the measurement. The 50 Ω microwave probe was calibrated by the short-open-load-through method before measurement. The signal delivered to the diodes was estimated to be 10 mV peak-to-peak. The value of source signal power is important as it affects the correctness of measurement result. A source signal with too much power will over drive the RITD due to its high nonlinearity, while a source signal with too little power can not drive the RITD to overcome the loss and noise of
Figure 7.1: The structure of RITD grown on SOI

Figure 7.2: Device structure of RITD grown on SOI
Figure 7.3: Measured I-V characteristics of RITD grown on SOI annealed at 825 °C measurement system. To de-embed the intrinsic parameters of intrinsic RITD from the pad parasitic, S11 of open pad test structure was measured. Figure 7.4 shows the small signal model of the probe pad. There are two signal paths from SIGNAL pad to GND pad. The first path is through the fringe capacitor $C_P^1$. Another path is through the substrate due to the coupling effect. By fitting the measured S11 of probe pad to the model in ADS, the values of $C_{P1}$, $C_{P2}$ and $R_P$ were determined as 29 fF, 165 fF and 870 Ω, respectively.

10 µm diameter RITD with 1-port configuration was then measured with biasing voltage of 50 mV, 150 mV, 200 mV, 250 mV, 300 mV, 350 mV, 400 mV and 500 mV. The measured S11 of each bias condition was then fitted to the circuit model with determined pad parasitic, which is shown in the inset of Fig. 7.5. In this equivalent circuit, the RITD provide the third path for signal to reach GND pad from
Figure 7.4: The small signal model of probing pad
Figure 7.5: The measured (symbols) and fitted (lines) reflection gain of the RITD. The small signal model of both probe pad and intrinsic RITD are shown in the inset.

The small signal model of both probe pad and intrinsic RITD are shown in the inset. SGIMAL pad, and it consists of 3 basic circuit elements, which are a series resistance, $R_s$, junction resistance, $R_j$, and junction capacitance $C_j$, respectively. The $R_j$ and $C_j$ are bias dependent. The symbols in Fig. 7.5 represent the measured reflection gain ($20\log \Gamma$) of the diode as a function of frequency for several representative bias voltages. The lines in Fig. 7.5 represent the modeled reflection gain, which is in excellent agreement with the measured values. It should be mentioned that the value of $R_s$, which is bias independent, was also optimized during the fitting process, and it converges into a range of $60.8 \sim 61.2 \, \Omega$ for each bias voltage, which also indicates the correctness of the established model.
Figure 7.6: The Gj and Cj versus bias voltage. The dot line is the diode I-V characteristics

Figure 7.6 plots both the junction conductance and junction capacitance as a function of bias voltage. Note the NDR region judging from DC I-V characteristics is in very good agreement with the NDC region from the conductance-voltage curve. The $C_j$ increases as bias voltage increases, this is because larger bias voltage will reduce the depletion width, hence increase the junction capacitance. The $C_j(V)$ is fitted into a second order polynomial as follows:

The maximum DC gain is 0.8 dB and associated with a cutoff frequency of 400 MHz was obtained when biased at 200 mV. All these values are inferior to Dashiell’s results, mainly due to the smaller peak current density of this RITD.
7.2 Large signal model of RITD

The forward I-V characteristics of a tunnel diode consists of 3 components: tunneling current $I_t$, excess current $I_e$ and thermal diffusion current $I_{th}$. To establish the large signal model, one has to decouple these 3 components and add them up to a single $I(V)$ function.

7.2.1 Thermal diffusion current

This is the normal diode current, which can be well modeled as follows:

$$I_{th} = J_{th} \times \exp\left(\frac{V}{nkT}\right) - 1$$ (7.1)

7.2.2 Excess current

According to Chynoweth’s theory [23], excess current increases exponentially with bias voltage and can be simplified as:

$$I_e = J_e \times \exp(W \times V)$$ (7.2)

where $J_e$ is a coefficient related to the defect density inside the tunneling barrier and $W$ is a parameter related to the tunneling barrier width. It is assumed that $W$ is not dependent on bias voltage.

7.2.3 Tunneling current

There are generally two different approaches to fit the tunneling current for both interband and intraband tunnel diode, one is to fit measured data and obtain empirically equations, another is physics based which derives the $I(V)$ from its physical origin. In this study, the empirical approach was tried for simplicity.
A commonly used empirically fitted equation [115] for interband tunneling current is

\[ I_t = J_t \times \frac{V}{V_p} \times \exp(1 - \frac{V}{V_p}) \]  

(7.3)

where \( J_t \) is the peak current density, \( V_p \) is the peak voltage.

Before fitting the equations, the series resistance \( R_s \) obtained from small signal model was used to correct the I-V characteristics.

Figure 7.7 shows the best fit result using the empirically model, which is much better than the fit result using the physics based model. Excellent agreement between corrected and modeled I-V characteristics was obtained using the empirical model. The 3 current components are also plotted in Fig. 7.7. It is shown that the thermal current is too small at valley voltage to affect the value of valley current, which indicates PVCR is mainly determined by the ratio between desired interband tunneling current and undesired excess current.

### 7.3 A Unified Model and Its Implementation Using ADS

Figure 7.8 shows a unified model which combines the large and small signal model. The \( I_j(V) \) is from the large signal model while the \( R_s \) and \( C_j(V) \) are obtained from the small signal model. The unified model was then implemented into ADS. A transient simulation is performed to simulate the response of the diode with a series connected 50 H inductor to a voltage ramped from 0 V to 1 V in 0.1 msec. The simulation result is plotted in Fig. 7.9. Strong oscillation occurs when the diode is biased in its NDR region, which will lead to the commonly observed plateau in its NDR region during the DC measurement, in which case the probe needle acts as an inductor.
Figure 7.7: Corrected and modeled I-V characteristics. The 3 current components are also plotted.

Figure 7.8: The unified model which combines large signal model and small signal model
Figure 7.9: Transient simulation result shows strong oscillation when the RITD is biased in its NDR region

7.4 Discussion of RF Performance of Si-based RITD

The reflection gain and resistive cutoff frequency of Si-based RITDs are of great interest to circuit designers. The reflection gain determines the gain of the tunnel diode bi-directional amplifier as presented in Sect. 3.3.2. The resistive cutoff frequency sets the upper limit on the operating frequency of tunnel diode based RF circuitry.

These performances are affected by the junction resistance, $R_j$, junction capacitance, $C_j$ and series resistance, $R_s$. In this section, the effect of each of these circuit elements on the overall RF performance of Si-based RITDs was simulated using the small signal model developed in Sect. 7.1.
7.4.1 Simulated Effect of Circuit Elements on RF Performance of Si-based RITD

Figure 7.10 shows the test bench used for simulation of the Si-based RITD circuit elements. The value assignment of circuit elements were based on the extracted ones in the previous RF measurement (shown in the inset of Fig. 7.5). The $C_{p1}$ and $C_{p2}$ were assigned to be 25 fF and 150 fF, which are comparable to the extracted ones. The $R_p$ was assigned to be 100 Ω, which is much smaller than the extracted value, as a result of using highly conductive Si substrate instead of highly resistive Si substrate. The $R_s$, $R_j$ and $C_j$ were assigned to be 20 Ω, -100 Ω and 1 pF, which are estimated values of a 5-µm-diameter RITD with $J_p$ of 30 kA/cm².

Junction Resistance

The effect of $R_j$ is simulated by varying $R_j$ from -10 Ω to -10000 Ω while keeping other parameters unchanged. Figure 7.11 shows the DC gain and cutoff frequency as a function of $R_j$. 

![Figure 7.10: Test bench for circuit elements of Si-based RITD.](image)
Figure 7.11: The effect of $R_j$ on DC reflection gain and resistive cutoff frequency.
The DC gain is very sensitive to $R_j$ in the range of -10 $\Omega$ to -200 $\Omega$. The DC gain reaches its maximum value of 21.6 dB at -75 $\Omega$. It drops rapidly when $R_j$ deviate from this value. The DC gain drops and approaches zero when the absolute value of $R_j$ increases. It will drop below zero when the absolute value of $R_j$ reduces.

The cutoff frequency is also dependent on $R_j$ as shown in Fig. 7.11, and it decreases linearly with increasing $R_j$ in the log scale plot.

**Junction Capacitance**

The effect of $C_j$ is simulated by varying $C_j$ from 0.1 pF to 10 pF while keeping other parameters unchanged. Figure 7.12 shows the DC gain and cutoff frequency as a function of $C_j$. The cutoff frequency decreases linearly with increasing $C_j$ in the log scale plot as a result of increasing the RC product. The DC gain decreases slightly as $C_j$ increases from 0.1 pF to 1 pF, and it drops rapidly upon further increase in $C_j$.

**Series Resistance**

The effect of $R_s$ is simulated by varying $R_s$ from 1 $\Omega$ to 100 $\Omega$ with other parameters unchanged. Figure 7.13 shows the DC gain and cutoff frequency as a function of $R_s$. With increasing $R_s$, the DC gain increases at an accelerated pace until it reach its peak at 50 $\Omega$, it then decreases sharply to -0.5 dB at 100 $\Omega$, which is the same as the absolute value of $R_j$. The cutoff frequency drops from 10 GHz to 0.8 GHz when $R_s$ is increased from 1 ohm to 75 $\Omega$.

**Discussion**

The simulation results show that a smaller $C_j$, $|R_j|$ and $R_s$ will result in a higher DC reflection gain and a larger resistive cutoff frequency. Therefore, small RITDs with high current densities will exhibit the best RF performance. However, special
Figure 7.12: The effect of $C_j$ on DC reflection gain and resistive cutoff frequency.
Figure 7.13: The effect of $R_s$ on DC reflection gain and resistive cutoff frequency.
care has to be taken to keep $R_s$ small. The RF performance of a high current density RITD will be presented in the next section.

### 7.4.2 Measured RF Performance of a High Current Density RITD

A 3-nm-spacer RITD structure which was grown for the spacer thickness study in Chapter 5 was used here. The structure is shown in Fig. 7.14. Following the 1-minute annealing process at 650 °C, the RITD was fabricated using the same process as described in Sect. 7.1.1.

Figure 7.15 shows the measured I-V characteristics of a 10 µm RITD, which exhibits a $J_p$ of 33 kA/cm² with a PVCR of 1.5. Strong oscillations are evident in its NDR region.

The microwave performance was measured using the same method as in Sect. 7.1.2. The DC biasing voltage was swept from 0.78 V to 1.02 V with steps of 20 mV. The reflection gain, $\Gamma$, as a function of frequency for several representative biasing
voltages, is plotted in Fig. 7.16. The highest DC reflection gain is 5.5 dB by biasing at 900 mV, while an 840 mV biasing voltage leads to the maximum resistive cutoff frequency of 900 MHz. However, the strong oscillations present during measurements renders the measured resistive cutoff frequency inaccurate. Furthermore, small signal parameters can not be correctly extracted due to the strong oscillation.

In a previous study by Dashiell et al. [31], the microwave performance of a 15 µm Si Esaki diode with peak current density of 16 kA/cm$^2$ was measured. Their diode exhibited a microwave reflection gain of 12 dB and resistive cutoff frequency of 1.6 GHz. Compared to their diode, the Si-based RITD in this study has a higher current density and a smaller size, therefore, it should exhibit better microwave performance according to the simulation results in Sect. 7.4. The resulting inferior performance is due to the large series resistance ($R_s$), which was estimated as large as 30 - 50 Ω, while the $R_s$ of their diode was determined to be only 7 Ω. The large $R_s$ estimated here is attributed to the contact resistance, because no silicidation step was employed in the fabrication process for ohmic contact. With an improvement in contact technology, a smaller contact resistance is expected that result in better microwave performances.

### 7.5 Conclusion

This chapter presents a unified model which combines both the small and large signal model of RITDs grown on silicon-on-insulator (SOI) wafers. The effect of circuit elements on RF performance were discussed based on the simulation result using the developed small signal model. Generally, smaller $R_j$, $C_j$ and $R_s$ will yield better RF performances. A Si-based RITD with a $J_p$ of 33 kA/cm$^2$ was fabricated and measured. The maximum DC reflection gain is 5.5 dB and the highest resistive
Figure 7.15: Measured I-V characteristics of 10 µm RITD.

Figure 7.16: Measured reflection gain vs. frequency for several representative biasing voltages of 10 µm RITD.
cutoff frequency is 900 MHz. The RF performance could be improved with a better ohmic contact technology.
CHAPTER 8

PROTON IRRADIATION EFFECTS IN SI-BASED RITDS

8.1 Introduction

Radiation-effects experiments have the potential to reveal the physics of device operation by introducing defects which systematically perturb the solid state [156]. In the present study, 2-MeV protons were used to create defects (mainly vacancies and interstitials) in SiGe RITDs. Disorder-induced changes in the current-voltage (IV) characteristics of the devices were determined, then compared to particle-induced changes in AlAs/InGaAs/InAs/InGaAs/AlAs RTDs grown on InP, InAs/AlSb/GaSb RITDs grown on GaAs, Si Esaki diodes and Ge Esaki diodes [155] [157] [88] [23]. By examining radiation-induced changes in the tunneling component of the current, evidence of resonant interband tunneling in SiGe RITDs was obtained.

8.2 Experimental

The standard RITD042clad was used in the radiation experiment. Figure 8.1 shows the structure grown by LT-MBE. The RITDs were patterned using standard photolithography techniques into devices having diameters between 10 and 75 µm. The radiation experiment was performed at the Naval Research Lab by Dr. B. D. Weaver.
In a typical experiment, IV curves were obtained for as many as 100 devices by measuring the current passing through the RITDs as the applied voltage was swept from -1.5 V to 1.5 V. Devices were then irradiated with 2-MeV protons to a predetermined fluence, $\Phi$, and the IV curves were remeasured. This process was repeated up to a maximum fluence of $\Phi = 1 \times 10^{15} \text{ H}^+/\text{cm}^2$. In all cases considered here, incident particles traversed the devices without significant loss of energy and hence created a uniform damage profile.

8.3 Results and Discussions

Five parameters were determined from each IV curve - the peak and valley currents, $I_p$ and $I_v$, the peak and valley voltages, $V_p$ and $V_v$, and the PVCR. In about 30% of the devices studied, changes in the contact resistance between measurements caused the peak and valley voltages to shift by 2-3%. The data presented here were obtained from devices in which the contact resistance remained constant.

Typical IV curves are shown in the inset of Fig. 8.2 for an unirradiated and an irradiated device. A fluence of $1 \times 10^{15} \text{ H}^+/\text{cm}^2$ reduced the PVCR from 3.6 to about 1.2. The roughly N-shaped IV characteristics, now familiar for SiGe RITDs, are seen.

Figure 8.1: Schematic diagram of structure used for radiation experiment.
Figure 8.2: PVCR vs 2-MeV proton fluence for irradiated SiGe RITDs. Inset: Current vs voltage for an unirradiated and an irradiated device. Minority carrier devices begin to degrade around $10^{10}$-$10^{11}$ 2-MeV H$^+$/$\text{cm}^2$ and are generally seriously degraded by $10^{13}$ H$^+$/$\text{cm}^2$. 
at all fluences. The general effect of proton irradiation is to increase the excess current while causing a slight increase in the peak current. Similar effects are observed on e⁻- and n⁺-irradiated Esaki diodes and H⁺-irradiated GaSb-based RITDs.

The effect of radiation damage on the PVCR is shown in the main body of Fig. 8.2. Below about $\Phi = 10^{12}-10^{13}$ H⁺/cm², no radiation-induced changes are observed. The same result was obtained for all measured devices, regardless of device diameter. (The diameter had no effect on the radiation-sensitivity of any parameter considered here.) In comparison, silicon-based solar cells and other minority carrier diodes begin to degrade at 2-MeV proton fluences between about $10^{10}$ and $10^{11}$ H⁺/cm², and are generally seriously degraded by $\Phi = 10^{13}$ H⁺/cm². Only majority carrier diodes such as InP-based RTDs display a degree of radiation-tolerance comparable to that of the SiGe RITDs of Fig. 8.2 [157].

Values of $I_v(\Phi)/I_v(0)$ for a typical SiGe RITD are shown in Fig. 2 plotted vs fluence. Also shown are values of $I_v(\Phi)/I_v(0)$ for InP-based RTDs, GaSb RITDs and Si- and Ge Esaki diodes. Normalizing $I_v(\Phi)$ by $I_v(0)$ by removes differences due to device size and material properties, and emphasizes the effect of irradiation on $I_v$. Because the Esaki diodes were irradiated with fast fission neutrons and the RTDs with 3-MeV helium ions, a standard technique based on the energy lost to displacement damage was used to convert n⁺ and He⁺ fluences to equivalent fluences of 2-MeV protons [157]. An average 3-MeV helium ion, for example, displaces about 10.3 times more atoms than a 2-MeV proton, which displaces about 15.5 times more atoms than does an average fission neutron.

As can be seen in Fig. 8.3, the valley current increases with increasing fluence for all devices. Comparable behavior is observed for many other kinds of diodes.
Figure 8.3: Normalized valley current vs equivalent fluence for Ge- and Si Esaki diodes, SiGe RITDs, InP-based RTDs and GaSb RITDs.
In conventional p-n diodes, for instance, irradiation increases the reverse-bias leakage current in proportion to the induced defect concentration (and hence the fluence) [61]. In the valley region of an Esaki diode’s IV curve, leakage current, also referred to as excess current, has been attributed to conduction via localized defect gap states, and is expected to vary nearly exponentially with bias voltage and to increase in direct proportion to the induced defect concentration [14].

The most disorder-tolerant devices, as shown in Fig. 8.3, are the Esaki diodes. Then, in decreasing order of tolerance, are the SiGe RITDs, the InP-based RTDs and the GaSb RITDs. This result is interesting because if SiGe RITDs were true Esaki diodes, their $I_v$-vs-$\Phi$ curves would be expected to fall between the Si and Ge Esaki data in Fig. 8.3. Such is not the case. One possible explanation is that a structural factor in the SiGe RITDs causes an enhanced sensitivity to disorder. Another possibility is that the physics of operation for SiGe RITDs with two-dimensional-to-two-dimensional (2D-to-2D) resonant tunneling between valence band and conduction band quantum wells differs significantly from 3D-to-3D interband tunneling in Esaki diodes.

Values of $I_p(\Phi)/I_p(0)$ for the various diodes are shown plotted vs fluence in Fig. 8.4. Again, the Esaki diodes are the least affected by radiation damage, followed respectively by the SiGe RITDs, the GaSb RITDs and the InP-based RTDs. The peak current in the RTDs decreases rapidly with increasing disorder, while in the other devices it increases. The reason for this will be discussed shortly. As in Fig. 8.3, the behavior of the SiGe RITDs in Fig. 8.4 falls outside the range of behavior that would be expected for SiGe-alloy Esaki diodes.

To gain further insight, it is useful to consider the effect of induced disorder on the IV characteristics of a generic tunnel diode. At any time, the total device current
Figure 8.4: Normalized peak currents vs equivalent fluence for Ge- and Si Esaki diodes, SiGe RITDs, InP-based RTDs and GaSb RITDs. Inset: Radiation-induced increases in current for a neutron-irradiated Si Esaki diode. The difference current increases monotonically with voltage and fluence, indicating that the increase arises from leakage.
I(V,Φ) can be written as the sum of the excess current $I_e(V,\Phi)$ and the tunneling current $I_t(V,\Phi)$. For the time being, no distinction is made between resonant and non-resonant tunneling. Radiation-induced changes in $I(V,\Phi)$, $\Delta I(V,\Phi)$, can then be written as

$$\Delta I(V,\Phi) = \Delta I_t(V,\Phi) + \Delta I_e(V,\Phi)$$

Values of $\Delta I(V,\Phi)$ (i.e., the 'difference current') can be obtained by subtracting the IV curve of an unirradiated device from that of an irradiated one. An example is shown in the inset of Fig. 8.4 for irradiated Si Esaki diodes,14 where it can be seen that the difference current increases monotonically with voltage and approximately linearly with fluence. These are well-known signs of radiation-induced increases in leakage (or excess) current.19-21 The tunneling component of the current in Esaki diodes is determined by disorder-insensitive parameters such as the band gap, the effective mass and the reciprocal lattice vectors,21 so most if not all of the excess current shown in the inset of Fig. 8.4 is due to radiation-induced increases in $I_e(V,\Phi)$.

A difference current curve for an irradiated SiGe RITD is shown in Fig. 8.5 along with the original IV curves. Difference current curves of similar shape were observed for all fluences and for all irradiated SiGe RITDs. Above about $V = 0.44$ V, the difference current curve resembles the Esaki diode curves in the inset of Fig. 8.4. In Fig. 8.5, the dashed line extending from $V = 0.44$ V to 0 V indicates the smooth behavior expected of radiation-induced leakage current increases. The area enclosed by the dashed line and the difference current curve indicates a negative contribution of $I_t(V,\Phi)$ to $I(V,\Phi)$. It is known that at high currents, oscillations induced by semiconductor parameter analyzers occur within the negative differential resistance (NDR) region of IV curves. However, the w-shaped deviation of the difference current
Figure 8.5: Difference current curve and original IV curves for a SiGe RITD. Dashed line: Expected leakage current behavior extrapolated from higher voltage down to $V = 0$ V. Inset: Difference current curves for Si- and Ge Esaki diodes, GaSb RITDs and InP-based RTDs.
curve in Fig. 8.5 cannot be due to this particular instrument effect because the deviation extends well beyond the NDR region from about 0.2 V down to about 0 V.

Difference current curves for the other tunnel diodes are shown in the inset of Fig. 8.5. In order to compensate for various device sizes and peak currents, the difference currents have been normalized by $I_p$. Except for a small, low-voltage decrease in $\Delta I$ (not visible on the scale of the inset), the Esaki diodes show only leakage-induced increases in current.

The curve for the InP-based RTDs reveals leakage-type current increases at voltages far from $V_p$, but near the resonance the current decreases markedly. This decrease has been shown to arise from the scattering of carriers from radiation-induced defects in the quantum well [157]. More specifically, only those incident electrons whose energy and momentum lie on a narrow disk in k-space can undergo resonant tunneling across the RTD [123], and if a carrier scatters from a radiation-induced defect while tunneling, the direction of its momentum changes and it is ejected from the resonance state with high efficiency. In other words, the reduced-dimensional aspect of tunneling in InP-based RTDs, combined with carrier scattering from radiation-induced defects in the quantum well, causes $\Delta I_t(V,\Phi)$ to be both large and negative.

Dimensional restrictions on carrier energy and momentum also apply to GaSb RITDs, but the lattice excitation that mediates the required interband transition causes the k-space resonance disk to be broadened by an amount equivalent to the excitation energy [88] [123]. This broadening reduces the efficiency with which scattering removes carriers from resonant tunneling, and lessens the degree to which $\Delta I_t(V,\Phi)$ contributes to $\Delta I(V,\Phi)$. Thus the GaSb RITD difference curve in the inset of Fig. 8.5 does not show a strong reduction in current, but rather a lessening of the
expected leakage current increase for voltages around $V_p$. Likewise, the significant reduction of the difference current observed for the SiGe RITD in the main body of Fig. 8.5 provides compelling evidence that a resonant interband tunneling state exists.

A qualitative picture of $\Delta I_t$ can be obtained from the data of Fig. 8.5 by extrapolating smooth curves from higher voltages down to $V = 0$ V to represent the effect of radiation-induced leakage current increases, and then by subtracting the resulting curves from the actual data. This has been done for the tunnel diodes of Fig. 8.5, and results are shown in Fig. 8.6. It can be seen in the figure that radiation-induced changes in $\Delta I_t$ for the Esaki diodes is several orders of magnitude smaller than for the RITDs. Also, the maximum value of $\Delta I_t$ for the RITDs is about 40% of that for the InP-based RTD.

The data of Figs. 8.5 and 8.6 can be fully explained as follows. Two main radiation-damage effects are observed on the IV curves of tunnel diodes. The first is a steady increase in leakage current with increasing defect concentration. The second is a decrease in current due to the scattering of carriers out of the tunneling state. The efficiency, $\xi$, with which a carrier is removed from tunneling depends on the k-space dimensionality of the tunneling state itself. For Esaki diodes, tunneling is nearly three dimensional (3-D), so the value of $\xi$ is small, and $\Delta I_t$ makes little contribution to $\Delta I$. For InP-based RTDs the resonance disk is sharp (nearly 2-D), so the value of $\xi$ is close to unity. In GaSb and SiGe RITDs, the interband transition causes the resonance to be broadened in k-space and the value of $\xi$ to be reduced. Judging solely by the relative peak heights in Fig. 8.6, if the carrier removal efficiency for InP-based RTDs is about 1, then for SiGe and GaSb RITDs it is about 0.4 and for Si and Ge Esaki
Figure 8.6: Radiation-induced change in tunneling current for various tunnel diodes at an equivalent fluence of $1 \times 10^{15}$ 2-MeV $H^+/cm^2$. The vertical scale of the Esaki diode data has been expanded by a factor of 10. The relative amplitude of the SiGe RITD curve demonstrates the existence of resonant interband tunneling.
diodes it is about 0.006. The small value of $\xi$ for the Esaki diodes is consistent with 3D-to-3D nonresonant tunneling, while the larger values for the RTDs and RITDs is consistent with 2D-to-2D tunneling, broadened, in the case of the RITDs, by the interband transition.

8.4 Conclusion

In conclusion, the observation of a strong contribution of $\Delta I_I$ to $\Delta I$ in proton-irradiated SiGe RITDs demonstrates their operation in reduced dimension, distinguishes them from Esaki diodes and confirms the existence of a true resonant interband tunneling state.
CHAPTER 9

STUDIES ON SI-BASED RITD GROWN ON SIGE SUBSTRATE

9.1 Introduction

Strain induced band offsets in Si/SiGe system was discovered by People et al. in 1986 [103]. Figure 9.1 shows the calculated conduction band and valence band offsets of a $\text{Si}_{1-x}\text{Ge}_x$ layer that is strained to conform to a substrate of $\text{Si}_{1-y}\text{Ge}_y$ [107]. The offsets are defined by $E_c(x) - E_c(y)$ and $E_v(x) - E_v(y)$. For example, the CB offset of tensially strained Si on $\text{Si}_{0.8}\text{Ge}_{0.2}$ substrate is 0.2eV (dashed line and circle in Fig. 9.1(a)), the VB offset of compressively strained $\text{Si}_{0.5}\text{Ge}_{0.5}$ on $\text{Si}_{0.8}\text{Ge}_{0.2}$ substrate is 0.22 eV (dashed line and circle in Fig. 9.1(b)). This discovery lead to tremendous flexibility in Si-based device design and has given rise to a number of novel devices, such as n-channel modulation-doped field effect transistors (MODFET) [28], p-channel MODFETs [102], photodetectors [138], resonant tunneling diodes [127].

This chapter presents Si-based RITDs grown on commercially available virtual $\text{Si}_{0.8}\text{Ge}_{0.2}$ substrates that utilize a Si substrate with a SiGe buffer using defect filtering to minimize defects intersecting the surface. Compared with the Si substrate,
Figure 9.1: Offsets in (a) conduction band and (b) valence band between a $\text{Si}_{1-x}\text{Ge}_x$ layer on $\text{Si}_{1-y}\text{Ge}_y$ substrate. [107]
Si$_{0.8}$Ge$_{0.2}$ substrates make it possible to grow tensially strained Si layers, which provides flexibility in strain engineering the band diagram of Si-based RITDs.

### 9.2 Experimental

The commercial p-type Si$_{0.8}$Ge$_{0.2}$ virtual substrate was grown on a Si substrate (Boron doped, 0.01-0.015 Ωcm) by the CVD technique. The CVD epi-layers consist of 0.5 μm Si buffer layer (p-type doping > 7×10$^{17}$/cm$^3$), 2 μm graded SiGe layer (p-type doping > 7×10$^{17}$/cm$^3$), 1.2 μm Si$_{0.8}$Ge$_{0.2}$ uniform layer (p-type doping < 1×10$^{15}$/cm$^3$), and a 17.5 nm Si cap layer (p-type doping > 1×10$^{15}$/cm$^3$). The SiGe uniform cap relaxation is greater than 98%. The total threading dislocations is expected to be less than 2×10$^{16}$ cm$^{-2}$.

The RITD structures were grown by Dr. Phillip Thompson on the p-type Si$_{0.8}$Ge$_{0.2}$ virtual substrate with an MBE growth system using elemental Si and Ge in electron-beam sources. The doping level for both $n^+$ and $p^+$ layers are $5×10^{19}$ cm$^{-3}$, while both the B and P δ-doping sheet concentrations were maintained at $1×10^{14}$ cm$^{-2}$. Prior to device fabrication, portions of the grown wafers were annealed using a forming gas ambient ($N_2/H_2$) in a Modular Process Technology corporation RTP-600S furnace at various temperatures for 1 minute. Ti/Au dots with various diameters were patterned on the surface of the wafers via standard contact lithography. A buffered oxide etch was used prior to metallization. Using the metal dots as a self-aligned mask, HF/HNO$_3$ wet etching was performed to isolate the diodes into mesas. Finally, a Ti/Au backside contact was evaporated on all of the samples.
9.3 The Effect of Si Layers Cladding P $\delta$ Plane

As shown in Fig. 9.2, the structure of a standard RITD grown on Si$_{0.8}$Ge$_{0.2}$ substrate is the same as the one of RITD on Si substrate which yield the highest PVCR, except the Ge concentration of each layer was raised by 20% to match the 20% Ge content elevation in the substrate. The increasing Ge content in spacer should reduce the tunneling barrier height and should also result in a higher PVCR, which is one of the predicted advantages for using a Si$_{0.8}$Ge$_{0.2}$ substrate.

Another advantage is that tensially strained Si layers can be grown to clad the P $\delta$-doping layer and deepen the conduction band quantum well by creating larger band offsets. Figure 9.3 (a) shows the structure of the designed device, in which the P $\delta$ plane is clad by two 2-nm Si layers. The tensile strain in the Si layer will result in a conduction band offset of 0.2 eV and a valence band offset of 0.05 eV as shown in Fig. 9.1. Fig. 9.3 (b) is a sketch of the resulting band diagram for this structure.

Figure 9.4(a) shows the peak and valley current densities of each structure annealed at various temperatures. Figure 9.4(b) shows the PVCR of each structure annealed at various temperatures for 1 minute. The highest PVCR obtained from the standard RITD on Si$_{0.8}$Ge$_{0.2}$ is 1.6, and the insertion of Si cladding layers substantially improves the highest PVCR to 2.8, which is a nearly two-fold increase. Another significant performance difference between the two structures is the shift in the optimal annealing temperature.

The higher optimal annealing temperature of the RITD with strained Si cladding the P layer suggests that this structure is more immune to dopant diffusion at high temperatures. As discussed in Sect. 2.4.3, both Ge concentration and strain can affect P diffusion by alteration to the cladding layer. P diffusivity in pure Si is smaller than
### Figure 9.2: The structure of a standard RITD grown on $\text{Si}_{0.8}\text{Ge}_{0.2}$ substrate.

<table>
<thead>
<tr>
<th>Layer Description</th>
<th>Thickness</th>
<th>Composition</th>
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<tbody>
<tr>
<td>100 nm n+ $\text{Si}<em>{0.8}\text{Ge}</em>{0.2}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>P delta doping layer</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2 nm i Si spacer</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4 nm i $\text{Si}<em>{0.4}\text{Ge}</em>{0.6}$ spacer</td>
<td></td>
<td></td>
</tr>
<tr>
<td>B delta doping layer</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 nm p+ $\text{Si}<em>{0.4}\text{Ge}</em>{0.4}$</td>
<td></td>
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</tr>
<tr>
<td>260 nm p+ $\text{Si}<em>{0.8}\text{Ge}</em>{0.2}$</td>
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<td>$\text{Si}<em>{0.8}\text{Ge}</em>{0.2}$ substrate</td>
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### Figure 9.3: (a) The structure of an RITD with P cladding layers grown on a $\text{Si}_{0.8}\text{Ge}_{0.2}$ substrate; and (b) show a sketched of the approximate band diagram of this structure.

<table>
<thead>
<tr>
<th>Layer Description</th>
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<tr>
<td>100 nm n+ $\text{Si}<em>{0.8}\text{Ge}</em>{0.2}$</td>
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<td>2 nm n+ Si</td>
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<td>2 nm i Si spacer</td>
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<td>4 nm i $\text{Si}<em>{0.4}\text{Ge}</em>{0.6}$ spacer</td>
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<td>B delta doping layer</td>
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<td>1 nm p+ $\text{Si}<em>{0.5}\text{Ge}</em>{0.5}$</td>
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<td>260 nm p+ $\text{Si}<em>{0.8}\text{Ge}</em>{0.2}$</td>
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<td>$\text{Si}<em>{0.8}\text{Ge}</em>{0.2}$ substrate</td>
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QW resulting from strain-induced band offset + delta doping

- 0.2 eV
- 0.05 eV

$B$ delta

$P$ delta
in SiGe, however, the tensile strain in the Si layer actually enhances P diffusion. As a result, the chemical and strain effects offset each other, and the P diffusion is not significantly changed by the insertion of Si cladding layers. Therefore, the significant performance difference between the two structures tested can not be explained by modification to P diffusion alone.

A reasonable explanation is that the strain induced band offset deepens the quantum well formed by the P $\delta$ plane, hence it increases the PVCR. The optimal annealing temperature is also increased, because the quantum well depth is not only dependent on the doping profile, but also on the strain-induced band offset. Therefore, the RITD can be annealed at a higher temperature without less reduction in confinement than the control sample.

Figure 9.4: Comparison of performances of RITDs with and without P cladding layers.
9.4 The Effect of Outside Barriers

In the development of III-V double quantum well RITDs, outside barriers were employed to block the non-resonant tunneling current component and hence improve the PVCR [160]. Theoretical analysis shows that the maximum resonance effect is obtained when the transparencies, $T_i$ ($i=1,2,3$), of the three barriers are matched in such a way that $T_1 = T_3 = T_0^{0.5}$, where barrier 1 and 3 are the outside barriers and barrier 2 is the central barrier.

The use of a Si$_{0.8}$Ge$_{0.2}$ substrate makes it possible to introduce outside barriers by employing strain induced band offsets. Figure 9.5 sketches the band offset of Si$_{0.5}$Ge$_{0.5}$ layer and Si layer on Si$_{0.8}$Ge$_{0.2}$ substrate with the values estimated from Fig. 9.1. By alternating the sequence of Si$_{0.5}$Ge$_{0.5}$ layer and Si layer grown on Si$_{0.8}$Ge$_{0.2}$ substrate, a 0.2 eV valence band QW with a 0.05 eV outside barrier (Fig. 9.5 (a)) and a 0.2 eV conduction band QW with a 0.1 eV outside barrier (Fig. 9.5 (b)) can be formed.

Figure 9.6 (a) shows the structure of the control RITD. Note, two Si layers clad the P $\delta$ plane to deepen the QW formed by P $\delta$ plane. Fig. 9.6 (b) shows the structure of RITD with outside barriers, which is formed by a 2 nm tensially strained Si layer on the p- side and a 2 nm compressively strained Si$_{0.5}$Ge$_{0.5}$ layer on the n- side. As shown in Fig. 9.7, a sketch of the band diagram of the RITD with outside barriers, illustrates how the outside barriers can effectively block the non-resonant tunneling current component by increasing its effective tunneling barrier width. Furthermore, the outside barriers can also deepen the QW, so that a better quantum state confinement can be achieved.

Fig. 9.8(a) clearly shows that the peak current densities of RITDs with outside barriers annealed at various temperatures are higher than the control samples, while
Figure 9.5: The band offset of Si$_{0.5}$Ge$_{0.5}$ layer and Si layer on Si$_{0.8}$Ge$_{0.2}$ substrate estimated by Fig. 9.1. (a) a 0.2 eV valence band QW with a 0.05 eV outside barrier; (b) a 0.2 eV conduction band QW with a 0.1 eV outside barrier
Figure 9.6: (a) Structure of the control RITD without outside barriers; (b) Structure of the RITD with outside barriers.

Figure 9.7: An approximate Sketch of the band diagram of the RITD with outside barriers.
The peak and valley current densities as functions of annealing temperatures for each structure

(a) The PVCR as a function of annealing temperature for each structure

Figure 9.8: Comparison of the performance of RITDs with and without outside barriers.

the valley current densities of RITDs with outside barriers are lower than the control RITDs. The increased peak current density and decreased valley current density suggest the outside barriers both deepen the QW and block the non-resonant tunneling current. As a result, the PVCR of RITDs with outside barriers are significantly higher than the ones of control RITDs, as shown in Fig. 9.8(b). The highest PVCR of 3.5 is obtained by 825 °C with 1 minute annealing.

9.5 Discussion

As demonstrated in the previous sections, by using Si$_{0.8}$Ge$_{0.2}$ virtual substrates, strain induced band offsets can be employed to effectively deepen the QW and form
potential barriers outside the tunneling spacer. The barriers block undesired current and effectively improves the PVCR. However, the highest PVCR achieved on a Si$_{0.8}$Ge$_{0.2}$ substrate is only 3.5, which is slightly lower than 3.8, the highest value obtained using Si substrate. The supressed overall performance of the RITD on Si$_{0.8}$Ge$_{0.2}$ substrate is attributed to the modest quality of the SiGe virtual substrate.

The clear cross-hatching pattern on the surface wafer with the epitaxially grown RITD is indicative of a large surface roughness. Atomic force microscopy (AFM) was used to characterize the surface roughness before and after the MBE growth. Figure 9.9 shows the AFM image of the Si$_{0.8}$Ge$_{0.2}$ substrate before MBE growth. Within a range of 2.5 $\mu$m and 50 $\mu$m, the surface Z-ranges are as large as 14.2 and 46.5 nm, respectively. The large surface roughness can not be smoothed even by growing a thick buffer layer, as shown in Fig. 9.10, which shows an AFM image of a 300 nm thick Si$_{0.8}$Ge$_{0.2}$ layer grown on the Si$_{0.8}$Ge$_{0.2}$ substrate. The surface Z-ranges are 28.0 nm and 57.1 nm, over a range of 2.5 and 50 $\mu$m, respectively. Note, the thickness of the active RITD layers are only 6-10 nm, which is a much smaller value compared to the surface roughness of the substrate. It is then not surprising that the overall device performance could be significantly degraded by the large surface roughness versus conventional Si (100) substrates. A much higher PVCR should be possible if the RITDs were grown on a high quality SiGe substrate with much smaller surface roughness.

9.6 Conclusion

In conclusion, Si-based RITDs grown on commercially available Si$_{0.8}$Ge$_{0.2}$ virtual substrates were studied. There are two advantages by using Si$_{0.8}$Ge$_{0.2}$ substrates: (1)
Figure 9.9: AFM image of Si$_{0.8}$Ge$_{0.2}$ substrate before MBE growth. (a) range of 50 $\mu$m $\times$ 50 $\mu$m; (b) range of 2.5 $\mu$m $\times$ 2.5 $\mu$m.
Figure 9.10: AFM image of a 300 nm Si$_{0.8}$Ge$_{0.2}$ layer grown on the Si$_{0.8}$Ge$_{0.2}$ substrate. (a) range of 50 μm × 50 μm; (b) range of 2.5 μm × 2.5 μm.
the Ge content in the spacer can be increased without exceeding the critical thickness; (2) a tensially strained Si layer can be grown, which provides flexibility in engineering the band diagram of the RITD.

By growing the tensially strained Si layer cladding the P $\delta$ plane, the QW of P $\delta$ plane is deepened, as a result, an increase in the optimal annealing temperature and improved PVCR were observed.

Outside potential barriers are formed by growing a tensially strained Si layer on the p- side and a compressively strained Si$_{0.5}$Ge$_{0.5}$ layer on the n- side. The outside barriers are effective to both deepen the QW and block the non-resonant tunneling current, hence improve the overall PVCR.

However, due to the large surface roughness of the SiGe substrate used here, the RITDs grown on SiGe substrate exhibit inferior performance to RITDs studied on Si substrate. Better performance is expected by using higher quality SiGe substrates with smaller surface roughnesses.
10.1 Introduction

Passive imaging systems and radiometers require highly sensitive detectors which can operate at millimeter-wave frequencies. Biased Schottky diodes are commonly used for these applications, however, the biasing circuit greatly increases the system complexity and also leads to extra noise and drift [134]. Zero-bias diode detectors are advantageous because no biasing circuit is required, but they require a large zero bias nonlinearity or curvature. Discrete Ge backward diodes [11] and planar-doped barrier diodes [73] have previously been used for zero bias detection with high nonlinearity. However, these devices are not readily suitable for imaging applications, where a mass-producible technology is required to fabricate a large numbers of identical devices into compact pixilated imaging arrays. Recently, Sb-based heterojunction backwards diodes [120] [121] were realized that have been demonstrated to be an excellent candidate for zero bias detector applications due to their high sensitivity, high bandwidth, modest temperature dependence and massive production capability [92]. However, the high cost of Sb-based backward diodes and their incompatibly
with main-stream silicon circuitry, will likely limit their implementation at the system level. In this chapter, the first Si-based p-i-n backward diodes which can be readily integrated with Si/SiGe CMOS or HBT circuitry is presented. The fabricated diode exhibits a curvature coefficient of 30.9 V$^{-1}$ and an associated junction resistance of 540 kΩ at room temperature. The predicted low frequency voltage sensitivity $V$ for a 50 Ω source is 3090 V/W. The low frequency optimal sensitivity $\beta_{max}$ is estimated to be 8370 kV/W, with a lossless matching network between the source and diode. With recent developments in SiGe heterojunction bipolar transistor (HBT) technology showing the potential of Si-based devices to be operated at frequencies over 200 GHz [44], the integration of Si-based backward diodes would be very attractive for zero-bias millimeter-wave detector applications.

### 10.2 Device Design and Fabrication

The key to obtain a highly nonlinear current-voltage characteristic with a high curvature coefficient at zero bias is to minimize any forward tunneling current, so that it can be substantially smaller than the backward tunneling current at comparable voltage levels. Since the amount of forward tunneling current depends on the available empty states on the p-side and available electrons in n-side, one straightforward approach is to reduce the doping density for both sides, so that the Fermi level is just below the valence band on the p-side and just above the conduction band on the n-side, respectively [71]. Figure 10.1 shows the Si-based backward diode structure studied here, which is a modified structure of a Si-based resonant interband tunnel diode (RITD). Compared to the RITD structures, both sides are uniformly doped without $\Delta$-doping planes. The thickness of the centrally located intrinsic spacer was
Figure 10.1: Schematic of layered structure of the Si/SiGe backward diode used in this study

Reduced to 2 nm with a composite configuration of 1 nm Si and 1 nm Si$_{0.6}$Ge$_{0.4}$, between the P-doped n+ Si layer and B-doped p+ Si layer.

This entire structure was provided by Dr. Phillip Thompson at NRL using molecular beam epitaxy (MBE) with elemental Si and Ge in electron-beam sources on 75 mm B-doped ($\rho = 0.015-0.04$ $\Omega \cdot \text{cm}$) Si (100) wafers. The substrate temperature was held at 320 $^\circ$C during growth of the active region to minimize Ge and dopant segregation. The nominal doping levels for both the p-side and n-side are $5 \times 10^{19}$ cm$^{-3}$.

Prior to device fabrication, portions of the grown wafers were rapid thermal annealed (RTA) using a forming gas ambient ($\text{N}_2/\text{H}_2$) in a Modular Process Technology corporation RTP-600S furnace at various temperatures between 600 $^\circ$C and 900 $^\circ$C for 1 minute. There are two functions for the anneal: the main purpose is to controllably interdiffuse the dopant atoms so that the effective doping levels will be modified at the metallurgical junction. Thus, various effective doping levels can be readily obtained by simply varying the annealing temperatures rather than growing multiple wafers. The second purpose is to remove any point defects created during LT-MBE which will
suppress the excess current component attributed to defect-related tunneling. Excess current increases exponentially with bias voltage and has a concave upwards characteristic, which will unfavorably compete with the concave down forward tunneling current and effectively reduce the curvature coefficient at zero bias. Ti/Au dots with 18 $\mu$m diameters were patterned on the surface of the wafers via standard contact lithography and liftoff. A buffered oxide etch was used prior to metallization. Using the metal dots as a self-aligned mask, HF/HNO$_3$ wet etching was performed to isolate the diodes into mesas. Finally, a Ti/Au backside contact was evaporated on all of the samples.

10.3 Results and Discussions

The curvature coefficient, $\gamma$, which is defined in Eq. 3.15 and repeated here as

$$\gamma = \frac{d^2 I/dV^2}{dI/dV} \quad (10.1)$$

is the most commonly used figure-of-merit to characterize the diode nonlinearity at zero bias. The voltage sensitivity, $\beta_V$, can subsequently be calculated to the first order by $\beta_V = 2 \gamma \cdot Z_s$, where $Z_s$ is the source impedance. Another important figure-of-merit is the junction resistance $R_j = dV/dI$ at zero bias. A typical value for the diode $R_j$ is much larger than the typical circuit impedance 50 $\Omega$. Therefore, a large $R_j$ will lead to a significant mismatch loss between the source and backward diode. However, if a lossless matching network is included between the source and the diode, a maximum sensitivity can be achieved. The maximum sensitivity $\beta_{\text{max}}$ at low frequency can be estimated as $R_j \times \gamma / 2$ [122].
Figure 10.2 shows the measured curvature coefficient and junction resistance for the Si/SiGe backward diodes studied here that were annealed at various temperatures. The junction resistance increases slowly as the annealing temperature increases for annealing temperatures below $800^\circ C$. When the annealing temperature exceeds $800^\circ C$, $R_j$ rises sharply, which can be attributed to a significantly increasing tunneling barrier width due to the P and B dopant interdiffusion and compensation of the central tunneling spacer region. The curvature, $\gamma$, exhibits a very good correlation with $R_j$ when annealing temperatures are below $875^\circ C$. At $875^\circ C$, the maximum value of $30.1 \ V^{-1}$ is obtained, which is almost double of a commercial discrete Ge backward diode for square law radiometry application [120]. When the annealing temperature is further increased to $900^\circ C$, $\gamma$ drops to $22.6 \ V^{-1}$. The predicted low
Figure 10.3: I-V characteristics are plotted of several backward diodes annealed at different temperatures. Note, the negative biased I-V characteristics of the diodes annealed at 600 °C, 800 °C, and 900 °C are normalized to the diode annealed at 875 °C for easy comparison of their relative forward bias current components.

frequency voltage sensitivity $\beta_V$ of a 875°C annealed backward diode with a 50 Ω source is 3010 V/W. With the junction resistance, $R_j$, of 22 kΩ, the low frequency optimal sensitivity $\beta_{max}$ is estimated to be 330 kV/W. The high sensitivity of the Si-based backward diodes makes them very attractive for zero-bias millimeter-wave detector applications.

The relationship between and the annealing temperatures can be readily explained by Fig. 10.3, in which several I-V characteristics of diodes annealed at 600 °C, 800 °C, 875 °C, and 900 °C are plotted. Since the current of these diodes are of several orders’ difference, the negative biased I-V characteristics of diodes annealed at 600 °C, 800 °C, and 900 °C are normalized to the one of diode annealed at 875 °C, so that their
backward tunneling current components are almost identical. Because the curvature coefficient at zero bias is dependent on the ratio between the backward tunneling current and the forward tunneling current at the same small voltage level, a diode having a smaller normalized forward current will yield a larger $\gamma$. It is clearly shown that when the annealing temperature increases from 600 °C to 800 °C, the forward biased current decreases only slightly. This can be the result of two processes: (1) the excess current component is significantly reduced, because the point defects within the tunneling barrier, which induce an excess current, are more effectively removed by higher annealing temperatures [22]. (2) As revealed by the small change in $R_j$ at annealing temperatures below 800 °C, the dopant atoms start to interdiffuse, but not enough to significant alter the effective doping levels. As a result, the Fermi level on both sides changes only slightly. Therefore, the slowly increasing curvatures in the range between 600 °C and 800 °C are attributed to the reduced excess current component concurrently with only a slightly altered Fermi levels. However, when the diodes are annealed with a temperature above 800 °C, dopant atoms diffuse much faster and begin to alter the Fermi level significantly. This leads to a sharp increase in the curvature in the range from 800 °C to 875 °C. When the annealing temperature is further increased to 900 °C, a strong concave up current component appears that reduces the curvature. The concave up current is identified as recombination-generation current. By 900 °C annealing, the dopant diffusion is so severe that a high concentration of dopant atoms diffuse into the nominally intrinsic depletion region. As a consequence, P-B pairs may be formed that introduce extra energy states [23], hence recombination-generation centers are created. Furthermore, the depletion region is greatly widened by 900 °C annealing. Therefore, the recombination-generation
current component dominates the I-V characteristics under positive bias and reduces the curvature coefficient at zero bias.

10.4 The Effect of Substrate Temperature on Performance

When the backward diodes are integrated with HBT, the high annealing temperature required to obtain high curvature coefficient will lead to undesired dopant diffusion for an HBT. Therefore, it is desired to lower the annealing temperature by increasing the substrate temperature during the growth. The same structure was grown with a substrate temperature of 400 °C. Figure 10.4 shows the measured curvature coefficient and junction resistance for the Si/SiGe backward diodes grown at 400 °C that were annealed at various temperatures. For comparison, the results of diodes grown at 320 °C are also plotted. Compared to diodes grown at 320 °C, diodes grown at 400 °C exhibit similar trends for both curvature coefficient and junction resistance. The results show, however, that the junction resistances of diodes grown at 400 °C are 2-3 orders higher than the ones of diodes grown at 320 °C for each annealing temperature. This is not surprising, because dopant atoms diffuse and/or segregate faster with a higher substrate temperature during the growth. As expected, the optimal annealing temperature for the highest curvature coefficient shifts from 875 °C to 850 °C, when the substrate temperature is increased from 320 °C to 400 °C. It is also observed that, in order to obtain the same curvature coefficient, the annealing temperatures for diodes grown at 400 °C are 50 - 100 °C lower than the ones for diodes grown at 320 °C. The shift to lower annealing temperature can also be attributed to more dopant diffusion during the growth, so that less dopant diffusion
is required to reduce the effective doping level. The highest curvature coefficient measured increased to $30.9 \text{ V}^{-1}$ by raising the substrate temperature, which could be the result of less point defects generated during growth when the substrate temperature is higher. A further increase in the substrate temperature will lower the annealing temperatures and might improve the curvature coefficient even more.

Figure 10.5 shows the I-V characteristics of a diode grown at 400 °C and annealed at 850 °C. The junction resistance and curvature coefficient vs. bias voltage are also plotted. When the diode is biased at 40 mV, the highest curvature coefficient of 37.8 $\text{V}^{-1}$ is obtained.
Figure 10.5: I-V characteristic of diode showing highest curvature coefficient of 30.9 $V^{-1}$ at zero bias. The junction resistance and curvature coefficient vs. bias voltage are also plotted.
10.5 Conclusion

Si-based backward diodes were grown by LT-MBE. Post-growth annealing removes the point defects. More importantly, various effective doping levels can be obtained by varying the annealing temperatures. There exists an optimal annealing temperature for highest $\gamma$ at zero bias. When annealed below the optimal temperature, the effective doping level is too large, while annealed at a higher temperature, recombination-generation current component dominates the I-V characteristics under positive bias. Increasing the substrate temperature leads to more dopant diffusion and/or segregation and less point defects during the growth. As a result, higher junction resistances, lower optimal annealing temperatures, and a higher curvature coefficient were obtained by increasing the substrate temperature. For backward diode grown at 400 °C, the highest $\gamma$ of 30.9 V$^{-1}$ is obtained by 850 °C annealing, which projects a low frequency voltage sensitivity $\beta_v$ for a 50 Ω source of 3090 V/W and the low frequency optimal sensitivity $\beta_{max}$ of 8370 kV/W. The high sensitivity and SiGe HBT compatibility of the Si-based backward diodes make them very attractive for future zero-bias millimeter-wave detector applications.
CHAPTER 11

FABRICATION OF GE QUANTUM DOT BY OXIDIZING SIGE NANOPILLARS

11.1 Introduction

11.1.1 Motivation for QDs in SET circuits

The key for room temperature SET circuits is that the charging energy to add one electron, $e$, to the channel, which is given by $E_a = e^2/C$, where $C$ is the capacitance of the island, must exceed the background thermal noise. Generally, this requires that $E_a < 10k_B T$, but it may need to exceed $100k_B T$ for some digital applications [47] [80]. In order to achieve this result, a constraint is held upon the QD size to achieve the desirable C value. Experimentally, an $E_a$ in excess of 100 meV has exhibited noticeable Coulomb blockade oscillations at room temperature. For a Si/SiO$_2$ QD [137], a sphere size of approximately 20 nm resulted in a $3 - 5 \alpha F$ capacitance for a 150 meV charging energy and room temperature operation. However, the placement of QDs in the SET channel and ability to fashion electrical contacts has proved problematic, resulting in low device yields. For instance, in one study, only 3 out of 56 SETs worked at room temperature [100].
A strong advantage in studying the SETs above is that prior to achieving the dimensional control goals, larger multi-electron SETs can be fashioned into RTDs [45]. This provides for an immediate impact for this proposed project.

11.1.2 Oxidation of Si Nanopillars and bulk SiGe

It is hypothesized that the key element for realizing quantum dots useful for room temperature logic circuits (i.e. diameters less than 3 nm, preferably less than 1 nm) [80] with device-to-device uniformity, lies in the different heats of formation of semiconductor oxides. For instance, SiO$_2$ (-204 kcal/mol) has nearly double the heat of formation of GeO$_2$ (-119 kcal/mol) [79] [97] [82]. Thus, the proposed Ge QD embedded in an SiO$_2$ matrix could be realized by nano-oxidation laterally of a nano-pillar composed of a Si/SiGe/Si single quantum well. Previous work has demonstrated that oxidation of Si nano-pillars can create Si quantum wires and dots encased in SiO$_2$ [83] [46] [104], but without the degree of freedom created by SiGe alloys. It was demonstrated that the Si/SiO$_2$ strain field alone suffices to pinch the oxidation front off and self-limit the oxidative process resulting in Si QDs below 10 nm diameters [83] [46]. It has also been shown that for oxidation of planar SiGe structures, a Ge pile-up occurs in front of the oxidation growth front as the Ge is expelled during the preferential oxidation of Si versus Ge [79] [97]. By careful control of the nano-pillar lateral dimensions, these two effects could be used to control this pile-up to create QD spheres embedded, and therefore self-aligned, within the pillar. Tailoring in the vertical direction during epitaxial growth of the quantum well alloy composition and thickness further provides a mechanism for controlling the QD shape and diameter. Thus, this template introduces a self-limiting process for the realization
11.1.3 Overview of the self-aligned and self-limited quantum dot process

This novel process is to fashion quantum dots of a predictable size, shape and placement, suitable for mass production and simple electrical contact or sensing. Fig 11.1 shows the basic process flow. Starting with an epitaxial layer, electron-beam lithography and anisotropic plasma etching will then be used to fashion nanometer-scale pillars (on the order of 10-80 nm). Limitations on pillar size are imposed by the resolution limits of the electron-beam lithography process. Oxidation will further confine the 2-D quantum wells to 0-D quantum dots by the preferential oxidation of Si vs. Ge.
11.2 Experimental

Epitaxial growth was achieved with an MBE growth system using elemental Si and Ge in electron-beam sources. The structures were grown on 75 mm B-doped ($\rho = 0.015 - 0.04 \Omega \cdot \text{cm}$) Si (100) wafers. The doping level for $p^+$ layers are $5 \times 10^{19}$ cm$^{-3}$. As shown in Fig 11.2, the epitaxial structure consists of an 1 nm Si$_{0.95}$Ge$_{0.05}$ sandwiched by two Si layers. The nano-pillars were patterned on both the grown structure and a Si wafer using electron-beam lithography and anisotropic plasma etching in University of Illinois at Urbana-Champaign [159]. The fabricated Si and Si/SiGe pillars are of 100 nm diameter with periods of 125, 150, 175, 200nm. The etching depth is typical about 200 nm.

11.3 Oxidation of Nano-pillars

Oxidation of the Si and Si/SiGe pillars was performed in Ohio State University. Both the Si and Si/SiGe pillars were oxidized using the Modular Process Technology
(RTP-600S) rapid thermal annealing (RTA) furnace. Due to the self-protection feature of the RTP system, there is an upper limit for the oxidation time. For example, the maximum oxidation time at 1200 °C is 2.5 minutes, which will limit the oxidation process. To obtain the desired SiO$_2$ thickness, several oxidation cycles have to be used.

The Si and Si/Si$_{0.95}$Ge$_{0.05}$ nano-pillars were dry oxidized at 1200 °C for 3 × 2.5 minutes. Transmission electron microscopy (TEM) was then performed to inspect the oxidized Si nano-pillar. As shown in Fig. 11.3, a crystalline Si QD of about 50 nm diameter is embedded within a 50 nm thick SiO$_2$ casing.

The patterns of Si/Si$_{0.95}$Ge$_{0.05}$ pillars disappeared after 1200 °C oxidation for 3 × 2.5 minutes, because the Si/Si$_{0.95}$Ge$_{0.05}$ pillars were broken during the oxidation. To analyze the broken mechanism, another run of oxidation at 1200 °C was performed on Si/Si$_{0.95}$Ge$_{0.05}$. The pattern disappeared again after only one oxidation cycle.
The breakage of Si/Si$_{0.95}$Ge$_{0.05}$ pillars indicates Si/Si$_{0.95}$Ge$_{0.05}$ pillars can not sustain the same oxidation process in RTP 600S as Si pillars. Since the linear thermal expansion coefficient of Ge (5.9$\times$10$^{-6}$ °C$^{-1}$) is much larger than the one of Si (2.6$\times$10$^{-6}$ °C$^{-1}$), the high temperature ramping rate in RTP 600S (30 °C/sec) could lead to a large thermal strain at the interface of Si/SiGe and lead to the observed breakage. Slowing down the temperature ramping rate may allow the thermal strain time to relax that could prevent breakage of the Si/SiGe pillars.

Since the temperature ramping rate in a conventional oxidation furnace with preset oxidation temperature can be manually controlled by adjusting the speed of sliding the boat loaded with the sample into or out of the furnace, the Si/Si$_{0.95}$Ge$_{0.05}$ pillars were then oxidized using a conventional oxidation furnace instead of RTP-600S.

The pillars were oxidized at 1100 °C with a temperature ramping rate of approximately 10 °C/sec. To monitor the oxidation process, the sample was taken out of the furnace for quick optical microscopy inspection at 5-, 15- and 35-minute time points. After inspection, the sample was put back into the furnace. The observed pattern remains clear up to 35 minutes. At this point, the sample already survived 3 heating cycles, which indicates that the SiGe pillar can sustain the thermal stress when the temperature ramping rate is reduced to 10 °C/sec. The sample was further oxidized for 25 more minutes, then it appears to be blurred under the optical microscope, especially for the patterns with smaller periods. The sample was then inspected under a Scanning Electron Microscopy (SEM). Figure 11.4(a) shows that after 60 minutes oxidation at 1100 °C, the SiGe pillars with 175 nm period grow to a point that they start to touch each other, and the pressure exerted on each other may break the pillars off the substrate. This experiment revealed another reason for
the breakage of SiGe nano pillars, that is, the limited space for growth will result in high mechanical stress, hence could break the nano pillars. Using a conventional oxidation furnace can prevent pillars from thermal stress breaking, while mechanical stress break can be avoided by increasing the spacing between pillars.

However, there are some exceptional cases for the mechanical stress break. Figure 11.4(b) shows some pillars with 125 nm period that survived the severe shape changing during the oxidation process. These closely packed pillars could be readily utilized as a QCA chain.
For all the oxidized SiGe dots, three layers are observed, which could be an evidence of Ge segregation during oxidation process. As shown in Fig. 11.4(c), the outside ring could be SiO$_2$, the inner ring could be a Ge riched SiGe region, while the core could be SiGe with the initial composition. However, TEM characterization is needed to confirm this observation.

The oxidized Si/Si$_{0.95}$Ge$_{0.05}$ pillars were dipped into HF to remove the SiO$_2$. It was then further oxidized for 30 minutes at 1100 °C. Figure 11.5 shows the SEM picture of Si/Si$_{0.95}$Ge$_{0.05}$ pillars with 200 nm period. The pillars were reduced to approximately 50 nm. This demonstrates that a sequential oxidation $\Rightarrow$ SiO$_2$ strip $\Rightarrow$ oxidation can ease the requirement on EBL and the following dry etching to obtain much smaller QD sizes. It should also help to relax the stress between SiO$_2$ and Si/SiGe pillars.

Figure 11.5: SEM image of a re-oxidized SiGe nano-pillar after stripping the outside SiO$_2$ layer.

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11.4 Conclusion

The oxidization of Si and Si/SiGe nano-pillars were studied. The Si pillars with 100 nm diameter were successfully oxidized using an RTP 600S system. An initial TEM image clearly showed the crystalline Si embedded in SiO$_2$. However, Si/SiGe nano-pillars with 100 nm diameters broke using the same oxidization process, due to the high temperature ramping rate and the resulting large thermal strain. By switching to a conventional oxidization furnace, the thermal strain was lowered and the Si/SiGe nano-pillars were successfully oxidized. The swelling during oxidization could also lead to a large strain on the nano-pillars and break them at the base. However, the closely packed pillars that survived thermal cycling could be utilized as a QCA chain. Three layers are observed for all the oxidized SiGe dots, which could be the first evidence of Ge segregation in a QD during the oxidation process. TEM inspection is needed to confirm the Ge segregation. Sequential oxidation $\Rightarrow$ SiO$_2$ strip $\Rightarrow$ oxidation can ease the requirement on EBL and the following dry etching to obtain smaller QD sizes.
CHAPTER 12

CONCLUSIONS

In this work, three kinds of Si-based tunneling structures, namely, Si-based RITD for mixed signal integrated circuit and low power digital applications, Si-based backward diode for millimeterwave detection applications, and fabrication of Ge quantum dots for SET and QCA applications, were studied.

12.1 Study of Si-based RITD

Since PVCR is a very important figure-of-merit for tunnel diodes, one of the primary tasks in this work is to improve the PVCR of Si-based RITDs. For interband tunneling diodes, the PVCR is determined by the ratio between the desired interband tunneling current and the unwanted excess current through the energy states in the forbidden energy bandgap. Therefore, the key to obtain a higher PVCR is to reduce the excess current component while maintaining the desired interband tunneling current. Two approaches were taken to improve the PVCR: The first one is to modify the RITD structure by growing SiGe layers cladding the B $\delta$-doping plane to suppress the B diffusion. As a result, a higher annealing temperature can be used to more effectively remove the point defects without losing the quantum well confinement; The second approach is to use spike annealing to limit the motion of dopant profile.
Both of these two approaches result in improved PVCR and was experimentally determined to be successful. The optimized structure with cladding layer was used as the template for later RITD growths. However, spike annealing was not extensively used due to the relatively poor process controllability using the existing equipment available.

Peak current density, $J_p$, is another important parameter for circuit performance. Both high and low $J_p$ are separately desirable for different circuit applications. Since tunneling current is exponentially related to the tunneling barrier thickness, a study of the spacer thickness effect on $J_p$ was conducted to explore the range over which the Si-based RITD can reach. The dependence of other performance figures, such as PVCR and voltage swing, on spacer thickness were also studied. The highest PVCR of 3.8 was obtained using a 6 nm tunneling spacer thickness. Thicker spacers lead to smaller PVCRs, because the desired tunneling current decays faster than the excess current as tunneling barrier thickness increases. Reducing the spacer thickness will also degrade PVCR due to dopant pair formation within tunneling barrier that creates defect states which elevated the excess current. A record high $J_p$ of 151 kA/cm$^2$ is obtained by using a 3 nm spacer thickness. Reducing the spacer thickness does not yield higher $J_p$, because dopant interdiffusion effectively broadens the tunneling barrier. Increasing the spacer thickness will lead to an exponentially decreasing $J_p$. A 16 nm spacer yields the lowest recorded $J_p$ of 20 mA/cm$^2$. The $J_p$ experimentally measured for Si-based RITD in these studies spans nearly seven orders of magnitude. The spacer thickness affects the voltage swing in the same way as it affects PVCR. Furthermore, it affects the voltage swing by changing the slope of the excess current on a semi-log scale.
One of the attractive features of tunnel diodes is its inherent multi-state behavior. Vertically integrated npnp Si-based RITD pairs were successfully built with double NDR regions under forward bias. Tri-state logic was demonstrated by a breadboarded circuit using the vertically integrated RITD pair as the drive and an off-chip resistor as the load. However, the obtained vertically RITD pairs exhibited a large peak voltage due to the large backward diode junction resistance. Furthermore, the noise margin was small as a result of the almost identical peak current for the two NDR regions. These two problems were solved by growing a modified structure with δ-doped backward diodes and unequal spacer thickness design for the two RITDs.

A unified model which combines both the small and large signal models of an RITD grown on a SOI wafer was developed. The small signal equivalent circuit was obtained by fitting the RF measurement results. The large signal model was obtained by fitting the DC I-V characteristics using empirical equations. The effect of circuit elements on RF performance was discussed based on the simulation results using the small signal model developed. Generally, a smaller $R_j$, $C_j$ and $R_s$ will yield better RF performance. A Si-based RITD with $J_p$ of 33 kA/cm$^2$ was fabricated and measured. The maximum DC reflection gain was 5.5 dB and the highest resistive cutoff frequency was 900 MHz. The RF performances could readily be improved with a better ohmic contact technology.

Radiation-effects experiments were performed on Si-based RITDs. The observation of a strong contribution of $\Delta I_t$ to $\Delta I$ in proton-irradiated SiGe RITDs demonstrates their operation in reduced dimension, distinguishes them from Esaki diodes and confirms the existence of a true resonant interband tunneling state.
A commercial Si$_{0.8}$Ge$_{0.2}$ virtual substrate was used to grow Si-based RITDs. There are two advantages by using Si$_{0.8}$Ge$_{0.2}$ substrate: (1) the tunneling probability can be enhanced by increasing the Ge content in the spacer without exceeding the critical thickness; (2) a tensilely strained Si layer can be grown, which provides flexibility in engineering the band diagram of the overall RITD. To take advantage of the tensile strain in the Si layer, structure with Si layers which clad the P $\delta$-doping plane and structures with barriers outside the tunneling region were studied: By growing tensilely strained Si layers which clad the P $\delta$-doping plane, the QW of the P $\delta$-doping plane is deepened. As a result, increased optimal annealing temperature and improved PVCR were obtained; Outside barriers are formed by growing a tensilely strained Si layer on the p- side and a compressively strained Si$_{0.5}$Ge$_{0.5}$ layer on the n- side. The outside barriers proved to both deepen the QW and block the non-resonant tunneling current, hence improve the PVCR. However, due to the large surface roughness of the commercially available SiGe substrate, the RITDs grown on SiGe substrates exhibit inferior performance to RITDs on conventional Si substrates. Better performance is expected by using better SiGe substrates with a smaller surface roughness.

12.2 Study of Si-based Backward Diode

Si-based backward diodes were grown by LT-MBE. Post-growth annealing removes the point defects and leads to dopant diffusion. There exists an optimal annealing temperature for the highest $\gamma$ at zero bias. When annealed below the optimal temperature, the effective doping level is too large, while annealed at a higher temperature, the recombination-generation current component dominates the I-V characteristics under positive bias. Increasing the substrate temperature during epitaxial growth
leads to more dopant diffusion and/or segregation and less point defects during the growth. As a result, higher junction resistances, lower optimal annealing temperature, and a higher curvature coefficient were obtained by increasing the substrate temperature. The high sensitivity and SiGe HBT compatibility of the Si-based backward diodes make them very attractive for zero-bias millimeter-wave detector applications.

### 12.3 Fabrication of Ge Quantum Dot

The oxidization of Si and Si/SiGe nano-pillars were studied. The Si pillars were successfully oxidized using an RTP 600S system. The TEM image clearly shows a crystalline Si pillar embedded within a SiO$_2$ casing. However, the Si/SiGe nano-pillars fractured at the base using the same oxidization process, due to the high temperature ramping rate and the resulting large thermal strain. By switching to a conventional oxidization furnace, the thermal strain was lowered and the Si/SiGe nano-pillars were successfully oxidized. The swelling during oxidization could also lead to large lateral strain on the nano-pillars and also cause some breakage. However, the QDs survived that were closely packed pillars could readily be utilized as a QCA chain. Three layers are observed for all the oxidized SiGe dots, which could be the first evidence of Ge segregation during the oxidation process. TEM inspection is needed to confirm the Ge segregation. A successive oxidation $\Rightarrow$ SiO$_2$ strip $\Rightarrow$ oxidation can ease the requirement on EBL and the following dry etching to obtain smaller pillar size.

Overall, the work presented here was to extend Si technology, as articulated on the International Technology Roadmap for semiconductors, and can serve as a guide for the future exploitation of Si-based RITDs.
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