DEEP DEFECTS IN WIDE BANDGAP MATERIALS
INVESTIGATED USING DEEP LEVEL TRANSIENT SPECTROSCOPY

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DEEP DEFECTS IN WIDE BANDGAP MATERIALS
INVESTIGATED USING DEEP LEVEL TRANSIENT
SPECTROSCOPY

BY

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Deep Defects in Wide Bandgap Materials Investigated Using Deep Level Transient Spectroscopy (219 pp.)

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Deep levels in GaAs, GaN, ScN and SiC, have been investigated using Deep Level Transient Spectroscopy (DLTS). Properties of deep levels, such as electronic behavior, activation energy, capture cross-section and concentration have been calculated.

In order to be able to perform DLTS measurements, Schottky or p-n junctions were fabricated from the material of interest. For this, contact formation and characterization has been studied. For each material, several types of contacts have been investigated. The contacts with the best properties in terms of leakage currents, band bending, and interface states density were used for DLTS measurements.

GaN materials have been synthesized using metalorganic chemical vapor deposition (MOCVD), molecular beam epitaxy (MBE) and rf-sputtering, in an attempt to compare and correlate the existence of the B defect (activation energy of $E_C-E_T=0.59$ eV) with the method of growth. Only material grown using MOCVD could be used for DLTS analysis.

ScN material grown using plasma assisted physical vapor deposition (PAPVD) and rf-sputtering, has been used with p-type Si to form p-n junctions. Depending upon the method of growth, different defects are found in the material. A defect with
activation energy of 0.51 eV has been identified as an electron trap in the PAPVD material and one electron trap with activation energy of 0.91 eV in rf-sputtered material.

The influence of substrate annealing upon the deep levels in two SiC polytypes, 4H- n-type SiC and 6H- p-type SiC has been investigated. For each set of annealed samples, several new defects were found (activation energies of $E_C-E_T=0.41$ eV, $0.50$ eV for $n$-type 4H-SiC, $E_C-E_T=0.37$ eV and $0.33$ eV for $p$-type 6H-SiC), all of them being electron traps, with the exception of one hole trap on the 4H-SiC material ($E_T-E_V=0.14$ eV). The activation energies range from $(0.14-0.50)$ eV below the conduction band. The nature of five of the found defects is not clear. For all the other defects, their existence has been correlated with published studies.

Approved

Professor of Physics and Astronomy
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List of Abbreviations and Acronyms

1. **C-V** - Capacitance-Voltage Characterization
2. **DFT** - Density Functional Theory
3. **DLTS** - Deep Level Transient Spectroscopy
4. **EPR** - Electron Paramagnetic Resonance
5. **HEMT** – High-Electron Mobility Transistors
6. **I-V** – Current – Voltage Characterization
7. **LED** – Light Emitting Diode
8. **LVP** - Liquid Phase Epitaxy
9. **LMTO** - Linear Muffin-Tin Orbital
10. **MBE** – Molecular Beam Epitaxy
11. **MOCVD** – Metalorganic Chemical Vapor Deposition
12. **MOSFET** - Metal Oxide Semiconductor Field Effect Transistors
13. **O-DLTS** - Optical DLTS
14. **OMVPE** – Organometalic Vapor Phase Epitaxy
15. **PAPVD** - Plasma Assisted Physical Vapor Deposition
16. **PICT** - Photoinduced Current Transient Spectroscopy
17. **SEM** - Scanning Electron Microscopy
18. **SIMS** – Secondary Ion Mass Spectrometry
19. **SCR** – Space Charge Region
20. **VPE** - Vapor-Phase Epitaxy
Chapter 1

Introduction

The perfect crystal is a simple model that is studied in any solid state introductory course; however in nature this perfect crystal is very hard to find, if not impossible. Many things contribute to the departure of crystals from the perfect form, such as impurities, broken bonds, stress, etc., that occur in the process of crystal formation or growth. Fortunately, imperfect crystal have a large area of application in everyday life, for example in devices and circuits, from silicon chips to opto-electronic devices; therefore it is important to be able to introduce some amount of impurities in a crystal semiconductor. However, there are cases when the presence of impurities affects the properties of a device in an undesired way, and to understand and control their presence in the lattice is crucial.

Impurities, either intentionally of inadvertently introduced, play an important role in determining the applicability of semiconductors for device fabrication, through the energetic level that they introduce in the band gap. These impurities can be viewed as imperfections in the crystal structure of a semiconductor that disturb the lattice periodicity by creating point defects. They can substitute for native crystal atoms (substitutional impurities) or form complexes (two impurity atoms at neighboring atoms
forming a pair) [1]. In either case, sets of localized energy levels, for which the ground state or some excited state lies in the band gap, are created. As a consequence, the semiconductor properties (optical and electrical) will strongly depend upon the location of the energy levels within the band gap, their concentration, and nature.

### 1.1 Shallow and deep levels

Imperfection in crystal structure other than impurities, are created during material growth and processing, being called structural defects. A first category are defects created as a result of strain due to differences in the lattice constants of the material being grown and the substrate used. This gives rise to stacking faults, line dislocation, etc. A second category includes imperfection created as a consequence of impurities that are introduced in the crystal during growth.

According to the location of the energy levels in the band gap of the semiconductor, the defects can be classified as shallow and deep defects. Shallow levels have energy located near the band edges (conduction or valence band) of the semiconductor. Impurities that introduce shallow levels are usually substitutional; there are, however, cases when interstitial atoms may introduce shallow levels as well (Li in Si on the tetrahedral interstitial site) [2]. Impurities that create shallow levels are used for doping, in this way changing the type of electrical conductivity, mobility and resistivity of the semiconductor.
Deep-levels, introduced by impurities but also by structural defects, play a different role in semiconductors. Their contribution to conduction is in general negligible, their concentration being very small compared with that of shallow level dopants. Through processes such as generation and recombination of electrons and holes, deep levels can control the lifetime of carriers and influence the opto-electronic properties. For example, deep levels degrade solar cell performance and limit the efficiency of hetero-junction lasers [3].

From a theoretical point of view, descriptions and models have been successful so far only in explaining shallow levels (hydrogenic effective mass theory, generalized effective mass theory, general perturbative and non-perturbative methods) with no general formalism for deep levels [411].

An earlier work by Glodeanu [12] considers bivalent substitutional impurities that generate two localized energy levels in the band gap and uses a helium-like model in a single band approximation and calculates the deep donor and acceptor levels of several impurities in GaAs, Si, and Ge. Even using several parameter values obtained from experimental results, the values calculated for the deep impurities energy levels differ from experimental ones by 0.1-0.5 eV.

There are many methods and techniques that have been employed in an attempt to develop a suitable theory for deep levels. These methods can be divided into “general perturbative” and “nonperturbative” methods. The first category solve the Hamiltonian assuming a perturbative potential introduced by the defect, and the eigenvalue problem is solved by a variety of techniques such as the linear combination of atomic orbitals-
type energy band calculation. The most notable results are those of Jaros and co-
workers for the substitutional oxygen impurity in GaP [13] and Baraff et al. for the
localized levels of the vacancy in Si [14][15]. The calculations based on this method are
limited by the complexity associated with no convergence of the calculation or
production of no bound states in the band gap.

The non-perturbative methods treat the crystal as a finite cluster of atoms and
attempt to solve directly the eigen-value problem using a single potential function. The
methods are flawed by the presence of impurities in the crystal and by surface states
that arise from unsaturated surface bonds. Despite these shortcomings, calculated values
for example for the positively charged sulfur defect in Si are in good agreement with
experiment [16].

With the development of Density Functional Theory (DFT), a number of
theoretical studies have been dedicated to semiconductors of interest for optoelectronic
devices such as GaAs, GaN and related materials. For example, *ab initio* calculations
based on DFT, together with the linear muffin-tin orbital (LMTO) Green’s function,
were employed to characterize native point defects in cubic GaN and AlN [17] This
allows the study of ideal substitutional defects without taking structural relaxation into
consideration. Another approach by the same group uses the DFT and LMTO and a
supercell and full-potential approach, which allows calculation for substitutional defects
including lattice relaxation. Both approaches allow calculation for vacancies and
antisite defects as well as for defects introduced by substitutional impurities such as C,
Zn and Mg. Even more, the methods allow calculation of pressure induced deep levels.
The results are in good agreement with those obtained using first principle pseudopotential calculations.

To conclude the theoretical review, there are numerous methods to calculate deep level characteristics, each method with its own specific approximations that makes it suitable only for one situation (in general only for one semiconductor and type of impurity) or at most for a group of systems that are similar.

### 1.2 Review of experimental work

From an experimental point of view, deep impurities in semiconductors have been the subject of investigation for more than 40 years. The experiments involve either thermal or optical excitation and de-excitation such as temperature dependence of Hall effect, photoconductivity, and electroluminescence.

The first experiment using a junction technique is that of William done in 1966 [18], but the foundation for the junction technique family was set by Sah and co-workers [19–23]. These techniques study the deep level impurities located in the space charge region of a junction. Because of the band bending at the junction, in the depletion region, all shallow donor or acceptor impurities will be ionized, and mobile carriers will be swept away, in this way eliminating their contribution to the results.

Junction techniques can be divided into static and dynamic method. Static techniques involve the measurement of capacitance or current as a function of
temperature, such as thermally stimulated capacitance [21] and thermally stimulated current [24].

Transient techniques measure a transient capacitance or current at different temperatures, after the level occupation returns to equilibrium after a perturbation. The excitation can be either electrical as in Deep Level Transient Spectroscopy (DLTS) [20][25][26], optical as in Photoinduced Current Transient Spectroscopy (PICTS) [27][28], or a combination of both – Optical DLTS [29][30].

1.3 Deep Level Transient Spectroscopy

DLTS is one of the most powerful tools for semiconductor characterization that has been used in the past 30 years, for investigating defects in materials such as Si (a review of Au, Pt, Pd and Rh deep levels in Si using DLTS can be found in Ref.[31]), GaAs (a review of deep levels in GaAs using DLTS can be found in Ref.[32]) and GaN (for a review of deep levels in GaN see Ref.[33][34]), to exotic materials such as NiSi$_2$ precipitates in silicon [35] and poly(p-phenylene vinylene) Schottky diodes [36].

DLTS measurements have been done on devices starting from simple Schottky barriers to complex systems such as solar cells [37], quantum wells [38][39] and high-electron mobility transistors (HEMTs) [40].

There are many variations on the DLTS technique, many of them requiring the use of a powerful computer for additional data analysis and simulation. A computer-
controlled system reported in the literature is the “Spectral analysis of DLTS” [41], used to obtain more information from a single-temperature DLTS scan for Si:Au, rather than data acquisition of multiple scans.

The large area of applications together with the low defect concentration limit and recent relatively easy-to-use devices (see SULA and BioRad DLTS systems), make DLTS techniques important tools in semiconductor fabrication and processing laboratories.

1.4 Outline of the project

The study in this work focuses on DLTS investigation of deep levels in a variety of wide band-gap materials, namely GaN, ScN, and SiC. The study is organized in 8 chapters.

Chapter 1 is an introductory chapter to present the scope and organization of this study.

Chapter 2 is an introduction to junction theory and techniques based on the existence of barriers at either metal-semiconductor or semiconductor-semiconductor interfaces. Current-Voltage (I-V) and Capacitance-Voltage (C-V) techniques will be summarized together with experimental apparatus used.
Chapter 3 is dedicated to a background description of deep level defects, summarizing the theory behind the DLTS technique and describing the experimental set-up used in this work.

In Chapter 4 results obtained for GaAs are presented. The work on GaAs has been done in order to test the apparatus and method of measurement acquisition as well as to provide a reference for the data analysis by comparing obtained results with existent studies.

Chapter 5 focuses on DLTS of GaN. Results regarding the B defect for MOCVD-grown samples are taken as a reference point. A discussion regarding the experiments performed on MBE and rf-sputtered GaN will be presented.

A novel study on ScN is presented in Chapter 6. ScN is a material that is of interest from several points of view, some of them being the value of the band-gap, the high melting point and the good lattice match with cubic GaN.

Chapter 7 is dedicated to deep levels in 4H n-type and 6H p-type SiC. A study of how the annealing temperature influences the deeps levels in this material will be presented.

Finally, in Chapter 8 the work in this study is summarized, and future directions are presented.
Chapter 2

Heterojunctions: Theory and Experimental Techniques

2.1 Introduction

In this chapter, a summary of heterojunction barrier formation and behavior is presented. Two of the techniques used in conjunction with DLTS that employ the use of heterojunction barriers, Current-Voltage (I-V) and Capacitance-Voltage (C-V), are presented. These techniques are helpful tools in assessing the suitability of a specific junction to be used for DLTS measurements and also for extracting useful information about the materials used and the barriers formed.
2.2 Summary of heterojunction theory

In this chapter, a summary of heterojunction barrier formation and behavior is presented. Two of the techniques used in conjunction with DLTS that employ the use of heterojunction barriers, Current-Voltage (I-V) and Capacitance-Voltage (C-V), are presented. These techniques are helpful tools in assessing the suitability of a specific junction to be used for DLTS measurements and also for extracting useful information about the materials used and the barrier formed.

Heterojunctions are contacts between two different materials that have interesting electrical or optoelectrical properties. Most known junctions can be divided in 4 categories:

a. junctions made out of same the semiconductor but with different type of doping (p-n homojunctions)

b. junctions between two different semiconductors, such as GaAs and AlGaAs.

These can be p-n junctions or isotype (n-n or p-p heterojunctions)

c. junctions created from metal layers on semiconductors (Schottky barriers)

d. junctions created from metals on semiconductors that form ohmic contacts.

For electrical measurements and characterization (I-V, C-V and DLTS), the junctions of interest are the p-n, isotype and Schottky junctions. The last category of metal contacts is interesting for applications such as fast response diodes and photodetectors.
I-V measurements are widely employed in characterization of contacts properties such as contact formation and degradation, contact resistance, etc, while C-V measurements are used to investigate the height of the barrier.

The basic Schottky barrier is shown in Fig. 2.1 on a $n$-type material. Similar barriers can be obtained on $p$-type materials as well. The metal is characterized by the work function of the metal $\Phi_m$ (energy required to remove an electron from the metal Fermi level to the vacuum level), and the semiconductor is characterized by the electron affinity of the semiconductor (energy required to remove an electron from the conduction band edge to the vacuum level), $\chi_s$.

Bringing the metal and the semiconductor together will result, according to the Schottky model, in an energy band diagram which will be discussed in the following.

According to the Schottky model, the energy band diagram is constructed by reference to the vacuum level (the energy of an electron at rest outside the material) of the work function of the metal and the electron affinity of the semiconductor. The values for these quantities are assumed to be constant throughout the material right to the interface. The vacuum level is assumed to be continuous across the interface. In thermal equilibrium, the Fermi levels in the metal and semiconductor must be aligned, and this condition results in a band diagram of the interface as shown in Fig.2.1.
At the interface itself, the vacuum level is the same for the two materials such that there is a step due to the difference between $\phi_m$ and $\chi_s$. This difference, the ideal barrier of the junction, $\phi_b$, is given by

$$
\phi_b = e\phi_m - e\phi_s + (E_C - E_{F_s}) = \phi_m - \chi_s
$$
(2.1)
$E_C$ is the lower edge of the conduction band of the semiconductor and $E_{FS}$ is the energy if the Fermi level of the semiconductor.

Even if the value for the barrier of a Schottky junction cannot be accurately predicted theoretically [42], the Schottky model is usually an acceptable approach for construction of the band diagram of the contact [43]. In practice, the barriers of Schottky junctions follow this model, i.e. they can be characterized by a value of $\phi_b$ which depends upon only weakly on the applied bias, and such junctions can be used for C-V profiling.

It is important from Fig. 2.1 to note that the condition to have a Schottky barrier is $\phi_m > \chi_s$ for a $n$-type semiconductor (opposite for $p$-type).

Moving away from the interface, the conduction band bends to match the “bulk” value with respect to the Fermi level at large distances from the contact. The resulting band bending excludes free electrons from the semiconductor in the vicinity of the contact, leaving a distribution of fixed positive charge due to ionized donors, thus forming a “depletion region” (space charge region SCR). At the edge of the depletion region, the bands become flat and the associated electric field is zero. In the metal, a neutralizing negative charge in the form of free electrons is accumulated at the contact over a distance $x_m$, which is the free carrier SCReening length in the metal; therefore, a Schottky junction can be seen as consisting of two regions- a space charge region beneath the barrier which is entirely depleted of mobile charge and a bulk region which is everywhere electrically neutral, separated by a sharp interface [44].
Electrons coming from the semiconductor into the metal face a barrier denoted $eV_{bi}$ as in Fig.2.1. This potential is called the “built-in potential” and is given by

$$eV_{bi} = \phi_m - \phi_s$$

(2.2)

Experimentally it is found that the Schottky barrier height is almost independent of the metal employed. This can be understood qualitatively in terms of non-ideal surfaces. In this model, the metal-semiconductor interface has a distribution of interface states which may arise from the presence of defects (chemical or structural). The defect region will lead to a distribution of electronic levels in the band gap at the interface, characterized by a neutral energy level $\phi_0$ such that states below it are neutral if filled, and states above it are neutral if empty. If the density of bandgap states near this neutral level is large, then addition or depletion of electrons in the semiconductor does not alter the Fermi level position at the surface (pinning of the Fermi level).

The depletion width for a Schottky barrier on an $n$-type semiconductor can be obtained following calculations described by Schroder [44] and has the following expression:

$$x_d = \left( \frac{2e \varepsilon_0}{eN_d} V \right)^{\frac{1}{2}}$$

(2.3)
where \( N_d \) is the concentration of donors, \( \varepsilon \) and \( \varepsilon_0 \) are the dielectric constants of the material and vacuum, \( V \) is the total band bending barrier.

If a voltage is applied to the junction, the band bending will change. In general the band bending \( V \) is the sum of the built-in voltage \( V_{bi} \) and the applied bias \( V_a \):

\[
V = V_a + V_{bi}. \tag{2.4}
\]

A forward bias has the opposite effect upon the built-in voltage and serves to reduce the overall band bending while a reverse bias does the opposite. In practice, application of reverse bias to a Schottky barrier on \( n \)-type material requires the semiconductor to be connected to the positive terminal of the external bias supply.

The current flow across a Schottky diode can involve a number of different mechanisms. The most important and desirable mechanism is that of thermionic emission of electrons (holes for \( p \)-type material) in which electrons with energies greater than the barrier height can overcome it and pass across the junction (Fig.2.2).

As the bias changes, this barrier increases or decreases; in this way the injected electron current can be modified, resulting in rectifying properties as depicted in Fig.2.3. The rectifying properties of a diode are characterized by a region of the I-V characteristic where the current flow is very small (reverse bias region) and a direct bias region where the current increases exponentially, as it will be described later.
In addition to thermionic emission, electrons can also tunnel through the barrier to generate current. This is important for heavily doped semiconductors where the depletion width is small.

The $p$-$n$ junction is also based on band bending but now this is formed at the interface between two semiconductors having different location of Fermi levels. Description of $p$-$n$ junctions physics and characteristics can be found in any solid state textbook and will not be presented here. However, a comparison between the two types of junctions is exemplified in Table 2.1.
Here are some of the advantages of using Schottky diodes for DLTS analysis:

a. only one type of carrier—no need to dope both n- and p-type the same material as opposed to p-n homojunctions,

b. use only one type of material as opposed to p-n heterojunctions,
c. no injection of minority carriers since there is only majority conduction, making the analysis more simple

d. space charge region extending only into the semiconductor.

Details regarding the capacitance and current flow through a Schottky barrier will be presented in the I-V and C-V sections.

<table>
<thead>
<tr>
<th></th>
<th>Schottky junctions</th>
<th>p-n junctions</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Materials</strong></td>
<td>metal+ semiconductor (only one type of conduction)</td>
<td>two semiconductors (different conduction types)</td>
</tr>
<tr>
<td><strong>Band bending</strong></td>
<td>YES</td>
<td>YES</td>
</tr>
<tr>
<td><strong>Space charge region</strong></td>
<td>YES</td>
<td>YES</td>
</tr>
<tr>
<td><strong>Conduction mechanisms</strong></td>
<td>thermionic emission majority carriers</td>
<td>diffusion +drift minority carriers</td>
</tr>
</tbody>
</table>

Table 2.1 Comparison of Schottky and p-n junctions
2.3 Current-Voltage (I-V) measurements

The subject of ohmic contacts to semiconductors is a large topic that has been under study for many decades. The performance of many semiconductor devices (p-n and Schottky junctions, metal oxide semiconductor field effect transistors (MOSFET), solar cells, reverse-biased photodiodes, etc.) are, in general, evaluated in terms of their current-voltage (I-V) characteristic. The extent of performance and degradation depends upon the material, series resistances, the operating current flowing through the device, and other parameters. The series resistance is determined by the semiconductor resistivity, contact resistance, and sometimes by geometrical factors. Large series resistance limits the current that passes through a device, most of the time being a quantity that needs to be as small as possible. However, there are cases when the series resistance, even if it has a high value, is a minor consideration in the device performance, such as a reverse-biased photodiode. Also, the series resistance introduces errors in the capacitance and carrier concentration profiling.

The diode current of a p-n and Schottky junction as a function of voltage have similar expressions:

\[ I = I_0 \left( e^{qV/nk_B T} - 1 \right) \]  

(2.5)
where $q$ is the electron charge, $k_B$ is the Boltzmann constant, $I_0$ is the prefactor, $n$ is the ideality factor, $T$ is the temperature of the diode, and $V$ is the applied voltage. $I_0$ and $n$ generally vary over the I-V range of a diode.

For the $p$-$n$ junction, at low currents, where space-charge recombination/generation dominates, $I_0$ is the SCR current and $n$ is close to 1 (only for ideal diodes the ideality factors are 1, for real diodes, for example, for Si diodes, $n=1.5$ to 2). At higher currents, $I_0$ accounts for quasi-neutral region recombination/generation and $n=1$.

For Schottky diodes, $I_0 = AA''T^2 e^{-\frac{q\phi_B}{k_BT}}$ where $A$ is the diode area, $A''$ is the Richardson constant multiplied by a factor taking into account phonon scattering and quantum mechanical reflection ($A'' = 4\pi^2 m^* h^3 = 120(m^*/m) A \text{cm}^{-2} \text{K}^{-2}$), $\phi_B$ is the effective barrier height, $n$ is the ideality factor, $h$ is Planck constant, and $m^*$ is the electron effective mass [46].

If both $I_0$ and $n$ are constant over some current range, then a plot of log(I) vs. V yields a straight line. When series resistance $R_s$ contributes to device behavior, the diode voltage becomes $V_d = V - IR_s$, where $V$ is the measured voltage across the entire diode including contact resistance as well as other resistance components. Eq.2.5 becomes in these conditions:

$$I = I_0 e^{q(V-IR_s)/nk_BT} - 1$$

(2.6)
A plot of log(I) vs V gives a straight line only over that portion of the curve where \( k_B T / q < 1 \) and \( IR_s << V \). The measured current deviates from the straight line at low currents due to the \(-1\) in the parenthesis of Eq. 2.6 and at high currents because of the series resistance. The straight line portion of the curve yields \( I_0 \) by extrapolation to \( V=0 \), and it gives \( n \) from the slope \( S = d \log(I)/dV \). Knowing the sample temperature, the ideality factor is obtained from the measured slope according to

\[
n = \frac{1}{\text{Slope} \times k_B T / q}
\]

An analogous analysis can also be done using plots of \( I(dV/dI) \) vs. \( I \), which gives \( nk_B T / q \) as the intercept and \( R_s \) as the slope, as shown in Fig. 2.4 and calculated in Eq. 2.8:

\[
I \frac{dV}{dI} = IR_s + \frac{nk_B T}{q}
\]

A plot of log(I) vs. V is also linear only for \( V >> k_B T / q \).

For the case of well-behaved Schottky diodes, the ideality factor is near 1. However, it does deviate from unity as a result of current flow due to mechanisms other than thermionic emission. For example thermionic-field emission current, interface damage, and interfacial layers tend to increase \( n \) above unity.
Figure 2.4 $I(dV/dI)$ vs. $I$ plot to obtain the ideality factor and series resistance of a diode (after D.K. Schroder [44])

For GaN for example, the I-V characteristic is given by:

$$J = A^{**}T^2 \exp \left(-\frac{\phi_B}{k_B T}\right) \exp \left(\frac{eV}{n k_B T}\right) \left[1 - \exp \left(\frac{eV}{n k_B T}\right)\right]$$

(2.9)
where \( J \) is the current density, \( A^{**} = 26.4 \text{ Acm}^{-2}\text{K}^{-2} \) for \( n \)-GaN and 96.1 \( \text{Acm}^{-2}\text{K}^{-2} \) for \( p \)-GaN [45].

From I-V characteristics, one can also extract the turn-on voltage which is an important quality of a functioning device, the break-down voltage which in the case of diodes limits the reverse-bias voltage that can be applied. From temperature dependence of the I-V characteristics, the barrier height of the junction can be extracted also.

To summarize, useful information can be extracted from I-V characteristics, such as barrier heights, ideality factors, turn-on voltages, series resistances, and breakdown voltages.

### 2.4 Capacitance-Voltage (C-V) technique

Studies of capacitance associated with the depletion region of a Schottky diode or \( p-n \) junction provide information on the concentrations and characteristics of electrically active centers in the bulk and near the surface region of semiconductors. The net doping density of a semiconductor and its variation with depth may be obtained from measurements of the voltage dependence of the capacitance.

C-V measurements rely on the fact that the width of a reverse -biased SCR of a semiconductor junction device depends upon the applied voltage. However, the results obtained from C-V measurements could have errors which are due to other
characteristics of the diode, such as leakage current, by deep states in the sample or interface states.

There are many reviews of the C-V technique that discuss its advantages as well as pitfalls, the most common being those of Blood [44] and Schroder [46]. In the following the most important results are presented.

Assuming the existence of a depletion layer at the interface between a uniformly doped semiconductor and a metal (similar case on a abrupt asymmetric $p^+-n$ junction), this layer will contain a distributed fixed charge due to the ionized donors. When the bias is increased by a small increment $\Delta V$, the depletion width increases which causes an increase in the fixed charge per unit area $\Delta A$. A small signal capacitance associated with the depletion region can be defined as

$$C = A \lim_{\Delta V \to 0} \left( \frac{\Delta Q}{\Delta V} \right)$$

(2.10)

where $A$ is the area of the diode.

If the built-in voltage, $V_{bi}$, is independent of the applied voltage $dV_a$, then since $dV = dV_a + dV_{bi}$, the capacitance $C$ can be measured in terms of the change in the applied voltage $dV_a$.

Using the second assumption, integration of the total charge $Q$ stored in the depletion region will give ($N_d$ is the free electron concentration in neutral material, $V$ is the total applied voltage) [44]:
Differentiating the above expression with respect to $V$ and neglecting the exponential factor (at room temperature $(kT/e) \approx 0.025 \, \text{V}$, and in reverse bias $V > \Phi_b$) $(E_g/2e) \approx 0.7 \, \text{V}$ for common semiconductors, so that $(kT/e) \ll V)$ the expression for the capacitance of the space charge region is obtained to be:

$$Q = (2\varepsilon\varepsilon_0 eN_d)^{1/2} \left\{ V - \frac{k_BT}{e} \left[ 1 - \exp\left(-\frac{eV}{k_BT}\right) \right] \right\}^{1/2}$$

(2.11)

Differentiating this expression with respect to voltage results in an expression for the carrier concentration in the material:

$$C = A \left( \frac{\varepsilon \varepsilon_0 eN_d}{2} \right)^{1/2} \left\{ V - \frac{k_BT}{e} \right\}^{1/2}$$

(2.12)

From Eq. 2.13, it can be seen that a plot of $C^2$ versus reverse applied bias $V_r$ in uniform material, is linear and has a slope proportional to $N_d^{-1}$ and an intercept of $(V_{b-}$
kT/e). If the material is compensated by \( N_a \) acceptors, the net fixed charge is \( e(N_d - N_a) \) and the slope gives \( (N_d - N_a) \). This is exemplified in Fig.2.5 for two Si diodes.

Assuming that \( V \gg k_B T/e \) and using Eq.2.3, the capacitance of the space charge region can be expressed as

\[
C = \frac{\varepsilon_0 A}{x_d}
\]

which is exactly the expression of a parallel-plate capacitor of area \( A \) containing a dielectric. Typical values for \( C \) are in the range 1nF-100pF (for example for a commercial GaN blue light emitting diode, \( C = 40pF \)).

It is important to differentiate between the capacitance of a parallel-plate capacitor where the charge varies linearly with \( V \) and the capacitance is constant and independent of \( V \) and the capacitance of a Schottky junction. In a depletion region the charge increases roughly proportional to \( \sqrt{V} \), and a fixed linear capacitance cannot be defined. A differential capacitance only can be obtained which decreases with increasing voltage.

The differential capacitance is usually obtained by superimposing a small-amplitude ac voltage of typically 1 MHz on the dc reverse bias. Because of the dependence of free carrier concentration, Eq.2.13, on area squared of the barrier, it is very important that the device area be precisely determined for accurate doping profiling.
Figure 2.5 (a) C-V curves for two Si p+n diodes, (b) $1/C^2$ vs. V curves, (c) n (carrier concentration) versus W (depth) profiles. A=7.9x10^{-3} \text{ cm}^2, T=300K (after D.K. Schroder [46])
It is important to note that for a Schottky diode there is no ambiguity in the space charge region (SCR) width $x_d$, since it can only spread into the substrate. SCR spreading into the metal is totally negligible. The doping profile theory is equally applicable for asymmetrical $p$-$n$ junctions if one side of the junction is more doped than the other. If the doping concentration of the heavily doped side is 100 or more times higher than that of the low doped side, then the spreading of the SCR in the heavily doped region of the junction can be neglected. If this condition is not met, than the equations must be modified; otherwise, the concentration profiling will have errors [47].

In Eq.2.12 the assumption that the depletion region was completely free of minority carriers was used. This is reasonable considering that the charges that actually respond to the small probe voltage are the mobile electrons and not the donor ions. From this point of view, the differential capacitance-voltage profiling technique determines the majority carrier concentration and not the doping concentration [48 50].

All the above were based on the assumptions that were made regarding the space charge region (assumption 1 through 3). A measure of the abruptness of the space charge distribution near $x_d$ is the Debye length (distance over which free electrons redistribute themselves in the vicinity of a fixed charge, or a measure of the distance over which a charge imbalance is neutralized by majority carriers under steady-state or equilibrium conditions),

$$L_D = \left( \frac{\varepsilon_0 k_B T}{e^2 N_d} \right)^\frac{1}{2}.$$  

The Debye length sets a limit to the
spatial resolution of the measured C-V profile. In compensated materials $N_d$ is replaced by $(N_d - N_a)$. As a consequence, assumption No.3 is satisfied when the depletion depth is much greater than $L_d$, and when this condition is not met, errors in the estimated majority carrier concentration are introduced [44][46].

2.4.1 Measurement errors and precautions

One of the limitations of C-V measurements is the Debye length discussed above. Briefly, free carries do not follow the profile of the dopant atoms if the dopant atom profile varies spatially over distances less than the Debye length. The majority carriers are more spread out than the dopant atoms, and a measured profile of steep dopant gradients will result in neither the doping nor the majority carrier profile. Instead, an effective or apparent carrier profile is obtained, which is closer to the majority carrier profile that it is to the dopant profile. This applies to abrupt high-low junctions and to steep-gradient ion implants [46].

Another source of errors is the series resistance of a junction. A $p$-$n$ or Schottky diode consists of a junction capacitance $C$, a junction conductance $G$, and a series resistance $R_s$ as shown in Fig. 2.6.
The conductance determines the junction leakage current and can be varied by process conditions. The series resistance depends upon the bulk wafer resistivity and on the contact resistance. If one uses a capacitance meter, then the actual circuit sensed by it is shown in Fig.2.16b. If $C_m$ and $G_m$ are the measured capacitance and inductance, then their expressions are [51]

\[
C_m = \frac{C}{(1 + R_s G)^2 + (2\pi f R_s C)^2} \quad (2.14a)
\]

\[
G_m = \frac{G(1 + R_s G) + R_s (2\pi f C)^2}{(1 + R_s G)^2 + (2\pi f R_s C)^2} \quad (2.14b)
\]
For the measured capacitance to be approximately equal to the true capacitance, it is necessary that $(R_s G) \ll 1$ and $(2\pi fR_s C)^2 \ll 1$. The first requirement is not always met. For example, if one uses a capacitance meter operating at 1MHz, for 1% accuracy in capacitance measurements, $R_s$ should be less than $1.6 \times 10^4 / C$ (pF). For example, for $C=50$ pF the series resistance should be less than 320 ohms.

C-V profiles rely on an accurate measure of the capacitance and of the device area. While the capacitance can be accurately measured, the area cannot always be accurately determined. Furthermore, the capacitance may contain stray capacitance components. The device contact area can be measured, but the effective area differs from the contact area due to lateral SCR spreading. The effective capacitance has the following expression [51]

\[
C_{\text{eff}} = C(1 + bW/r)
\]

\[
C = \frac{\varepsilon_0 A}{xd}, \quad A = \pi r^2
\]

where $d$, $A$, and $b$ are material constants (e.g. $b=1.5$ for Si and GaAs and 1.46 for Ge).

Eq.2.15 shows the lateral SCR effect to diminish as the contact radius increases and that $r > 100 \cdot b \cdot W$ ensures for the second term in the bracket to contribute no more than 1% to the effective capacitance.
Errors are also introduced in the doping profiles because of excess leakage currents. This is specific to Schottky barriers. The assumption is that the voltage is measured only across the space charge region. For most devices this is a good approximation since the impedance of the reverse-biased SCR is much higher than the semiconductor quasi-neutral region resistance. If, however, excess leakage currents flow, then an appreciable voltage can be developed across the quasi-neutral regions. This voltage is automatically included in the recorded voltage introducing errors in the measured profiles [52].

Deep traps present in the material, since are charge responding to an applied time-varying voltage, will determine any charge that can respond to the applied voltage. Deep level impurities or traps in the semiconductor bulk can also produce errors in capacitance profiles. The contribution from these is a complicated function of the density and energy level of the traps as well as the sample temperature. This contribution can usually be neglected for trap concentration 1% or less than the doping concentration [53] [54].

To summarize, C-V profiling is a suitable technique to investigate the majority carrier concentration and depth distribution for different junctions, provided that certain precautions have been met. Influenced by recombination effects, deep traps, and factors attributed to junction fabrication, it should be used in conjunction with other techniques such as Hall effect and SIMS profiling.
Chapter 3

Deep Level Transient Spectroscopy

In this chapter a short description of deep levels in semiconductors, mechanisms that involve deep levels, and their behavior in time is presented. Deep level transient spectroscopy is described from a theoretical point of view. Last section is dedicated to the experimental apparatus used in this work.

3.1 Introduction

Deep state characterization methods can be broadly divided into space charge methods and bulk methods. In general, space charge methods have greater sensitivity but have the disadvantage that the measured parameters are determined in the depletion field, a factor that may result in significantly different values being observed for some properties (e.g. reduced thermal activation energies due to the Poole-Frenkel effect). In contrast, bulk techniques (such as Hall measurements) provide parameter values in the
neutral (low field) region of the material, but for these techniques to be applicable, the concentration of the deep states must be sufficient to have a measurable effect on the position of the Fermi level at some accessible temperature.

All techniques used for the measurement of the electrical parameter of the deep states can be regarded as having three stages:

1. The occupancy of the deep electrical state is set,
2. The occupancy is perturbed;
3. The change in occupancy is measured.

In the DLTS method, the occupancy of the deep electrical state is set by applying zero bias to the normally reverse biased junction. The shift of the Fermi level will tend to result in states becoming occupied by majority carriers. The voltage of the diode is then restored to the reverse bias and at a sufficiently high temperature the majority carriers will be thermally emitted from the deep state. This sequence provides a transient perturbation of the occupancy that is monitored by observing the small signal capacitance of the diode using a simple analogue signal processing technique to evaluate the resultant capacitance transient.
3.2 Physical description of deep levels

The band diagram of a perfect single crystal consists of a valence and conduction band separated by the band gap. When the periodicity of the single crystal is perturbed, either by foreign atoms or crystal defects, discrete energy levels are introduced into the band gap.

Fig. 3.1 shows an overview of some of the principal charge exchange mechanism involving deep states. $e$ and $c$ stand for the emission and capture rate. The subscript $p$ or $e$ indicates a hole or an electron. The energy of the deep state is $E_T$ and consists of $N_T$ impurities/cm$^3$ uniformly distributed throughout the semiconductor. $E_C$ and $E_V$ are the edges of the conduction and valence band. Empty circles represent holes, filled circles electrons.

![Figure 3.1 Overview of some of the principal charge exchange mechanism involving deep states [46].](image)
Following the discussion of P. Blood [44] and D.K. Schroder [46] on representation of deep levels in semiconductor, let us assume that the semiconductor has \( n \) electrons/cm\(^3\) and \( p \) holes/cm\(^3\) introduced by shallow-level dopants. In an initial state, let the deep center first capture an electron from the conduction band with a capture coefficient \( c_n \). After capture, one of the two events takes place. The center can emit the electron back to the conduction band (probability \( e_n \)–process (b)) or it can capture a hole from the valence band (probability \( c_p \)–process (c)). After these events, the deep center is occupied by a hole and again has two choices. Either emits the hole back to the valence band with rate \( e_p \) (process (d)), or captures an electron. These are the only four possible events that involve the edges of the bands and the impurity.

Process (a) followed by (c) is a recombination event, process (b) followed by (d) is a generation event. Both band edges and the center are involved in these processes. If event (a) is followed by (b), or event (c) is followed by (d), this are trapping events, which involve only one band edge and the center.

Whether an impurity acts as a trap or a generation-recombination (G-R) center, depends upon the location of the Fermi level in the band gap, the temperature and the capture cross section of the impurity. The electron emission rate for centers in the upper half of the band gap is much higher than the hole emission rate, while the hole emission rate is generally much higher than the electron emission rate for centers lying in the lower half of the band gap.

A G-R center can be in one of the two charge states. When occupied by an electron it is in the \( n_T \) state, and when occupied by a hole it is in the \( p_T \) state. The
concentration of G-R centers occupied by electrons, \( n_T \), and by holes, \( p_T \), must equal the total concentration \( N_T \) or

\[
N_T = n_T + p_T
\]  

(3.1)

The electron concentration is diminished by electron capture processes (a) and increased by electron emission, process (b). The time rate of change of \( n \) due to G-R mechanism is [44][46]:

\[
\frac{dn}{dt}\bigg|_{G-R} = (b) - (a) = e_n n_T - c_n n p_T
\]  

(3.2)

Electron emission depends upon the concentration of G-R centers occupied by electrons and the emission rate through the relation (b) = \( e_n n_T \). This relationship does not contain \( n \) because it is not necessary to have electrons in the conduction band during emission processes. But there must be G-R centers occupied by electrons, otherwise there will be no emission of electrons. The capture process is more complicated because it depends upon \( n, p_T \) and the capture coefficient \( c_n \) through the relation (a) = \( c_n n p_T \). The electron concentration is important in this case because, to be able to capture electrons, there must be electrons in the conduction band. The situation is similar for holes.
The emission rate $e_n$ represents the number of electrons emitted per second from electron-occupied G-R centers. The capture rate $(c_n n)$ represents the number of electrons captured per second from the conduction band. In this simple picture, the electron-hole emission process is just an electron jumping from the valence band to the conduction band by using the $E_T$ level. To describe the capture coefficient $\sigma_n$, the G-R center is considered as moving with the velocity $v_{th}$ while the electrons are immobile. The center then sweeps out a volume per unit time of $(\sigma_n n v_{th})$ and $c_n = \sigma_n v_{th} n$.

Those electrons that find themselves in this volume have a high probability of being captured. Capture cross sections vary widely depending upon whether the center is neutral or negatively or positively charged. In general, a center with a negative or repulsive charge has a smaller electron capture cross section as compared with neutral or positive charged centers. Neutral capture cross sections are on the order of $10^{-15}$ cm$^2$.

### 3.3 Mathematical description of time evolution of concentration of deep centers

Whenever an electron or hole is captured or emitted, the center occupancy changes, and the rate of change is given by
\[
\frac{dn_T}{dt} \bigg|_{G-R} = \frac{dp}{dt} - \frac{dn}{dt} = (c_n n + e_p)(N_T - n_T) - (c_p p - e_n)n_T \quad (3.3)
\]

This equation is in general nonlinear since \( n \) and \( p \) are time-dependent. But in two cases it can be simplified. In a reversed biased space-charge region, both \( n \) and \( p \) are small and can be neglected in a first order. Also, in the quasi-neutral region \( n \) and \( p \) are reasonable constant. Solving Eq.3.3 for the second assumption gives \( n_T(t) \) as

\[
n_T(t) = n_T(0)e^{-\tau t} + \frac{c_n n + e_p}{c_n n + e_n + c_p p + e_p}N_T(1 - e^{-\tau t}) \quad (3.4)
\]

where \( n_T(0) \) is the concentration of G-R centers occupied by electrons at \( t = 0 \) and

\[
\tau = \frac{1}{c_n n + e_n + c_p p + e_p}N_T
\]

The steady-state concentration as \( t \to \infty \) is

\[
n_T = \frac{c_n n + e_p}{c_n n + e_n + c_p p + e_p}N_T \quad (3.5)
\]

The steady-state occupancy of \( n_T \) is determined by the electron and hole concentration as well as by the emission and capture rates. The last two equations are the basis for DLTS measurements. Eq.3.4 is difficult to solve in the general case because emission rates are usually not known and \( p \) and \( n \) vary with time and distance.
in a device. However the equation pertains to certain simplifications (e.g. an \( n \)-type substrate, in the first order \( p \) could be neglected).

The concentration for G-R centers above the Fermi level in the three stages of a DLTS experiment changes as described below.

When the occupancy of the deep electrical state is set and at equilibrium, for example by keeping a diode at zero bias for a long time, \( n_T = N_T \) (capture dominates emission since there are \( n \) mobile electrons) and most centers will be occupied by electrons.

When the diode is pulsed from zero to reverse bias, electrons are swept out of the reverse-biased region very quickly, thereby reducing the chance of being recaptured (typically, the electron swept-out time is \( t_e = W/v_n \), for \( v_n = 10^7 \) cm/s and \( W \approx \) few microns, \( t_e \approx \) tens of picoseconds), and emission dominates. The time dependence of \( n_T \) becomes

\[
n_T(t) = n_T(0) \exp \left( -\frac{t}{\tau_e} \right) \approx N_T \left( -\frac{t}{\tau_e} \right)
\]

(3.6)

while the steady-state concentration is now

\[
n_T = \frac{e_p}{e_n + e_p} N_T
\]

(3.7)
Some G-R centers will be in the $n_T$ state and some in $p_T$ state. When the diode is pulsed from reverse bias to zero bias, electrons rush in to be captured by G-R centers that are in the $p_T$ state. The time dependence of $n_T$ during this capture period is

$$n_T(t) = N_T - [N_T - n_T(0)] \exp \left( -\frac{t}{\tau_c} \right)$$

(3.8)

where $\tau_c = 1/c_n n$ and $n_T(0)$ is the initial steady-state concentration given by Eq. 3.7.

The above equations describe the G-R centers in terms of their concentration, emission, and capture coefficients. Similar equations apply to G-R centers that are below the Fermi level. The impurities can be negatively, positively charged or neutral.

### 3.4 Transient measurements

As described in Chapter 2, if one considers a Schottky diode, the capacitance of the junction has the expression

$$C = \frac{A}{2} \sqrt{\varepsilon \varepsilon_0 \frac{N_{\text{at}}}{2 \sqrt{(V_b - V)}}}$$

(3.9)
where \( N_{\text{SCR}} \) is the ionized impurity concentration in the SCR. The ionized shallow-level donors in the SCR are positively charged and \( N_{\text{SCR}} = N_D^+ - n_T^- \) for deep-level acceptor impurities that are negatively charged when occupied by electrons (\( N_{\text{SCR}} = N_D^+ + p_T^+ \) for deep-level donors occupied by holes). \( N_{\text{SCR}} \) increases with time.

With DLTS, one determines the deep-levels by monitoring the time-varying capacitance of, for example, a Schottky barrier, which reflects the time dependence of \( n_T(t) \) or \( p_T(t) \). As electrons are emitted from G-R centers, the SCR width, \( W \), changes. In transient measurements it is this time-varying \( W \) that is detected as a time-varying capacitance. From Eq.3.9 can be found that

\[
C = A \sqrt{\frac{\varepsilon \varepsilon_0 \epsilon}{2}} \sqrt{\frac{N_D}{(V_{\text{bi}} - V)(1 - \frac{n_T(t)}{N_D})}} = C_0 \sqrt{1 - \frac{n_T(t)}{N_D}} \tag{3.10}
\]

where \( C_0 \) is the capacitance without any deep-level impurities at reverse bias \(-V\). Since in real semiconductors the deep-level impurities form only a small fraction of the SCR impurity concentration, \( N_T << N_D \), the capacitance can be approximated (using a simple Taylor expansion) by

\[
C = C_0 \left(1 - \frac{n_T(t)}{2N_D}\right) \tag{3.11}
\]
This is a very important result that is used in determining the concentration of deep-levels in a semiconductor and for most cases Eq.3.11 is sufficiently accurate.

### 3.5 Emission of majority carriers

The most common measurements using DLTS are for emission and capture of majority carriers, for which a simple Schottky barrier is necessary. Measurements of minority carriers are also done using DLTS, in which case one uses $p$-$n$ junctions (for the case of Schottky barriers, minority carriers cannot be injected in the SCR).

Consider the emission of majority carriers. For this case, the diode is initially zero biased, allowing the impurities to capture majority carriers. The capacitance is the zero-bias value of $C$ ($V=0$). Following a reverse bias pulse, majority carriers are emitted as a function of time. Using Eq.3.11 the capacitance has the following expression

$$C = C_0 \left(1 - \frac{n_p(0)}{2N_o} \exp \left(-\frac{t}{\tau}\right)\right)$$

(3.12)

The SCR is widest and the capacitance is lowest immediately after the device is reverse biased, then $C$ increases until the steady state is reached (Fig.3.2) (majority carrier emission).
From the decay time constant of the C-t curve one could derive the emission rate constant and from the reversed-biased capacitance change one could obtain $n_T(0)$.

Defining $\Delta C_0 = C(t = \infty) - C(t = 0)$

\[
\Delta C_0 = C(\infty) - C(t) = \frac{n_T(0)}{2N_D} C_0 \exp \left( -\frac{t}{\tau} \right)
\]

(3.13)

Under equilibrium conditions, $dn_T/dt = 0$ and

\[
e_n n_T = c_n n (N_T - n_T)
\]

(3.14)
For a non-degenerate semiconductor (i.e. \( n < N_C \)), the free electron concentration is determined by the Boltzmann factor [44]

\[
n = N_C \exp \left( - \frac{E_C - E_F}{k_B T} \right)
\]

(3.15)

while the occupancy of the trap is defined by the Fermi-Dirac distribution

\[
n_T = \frac{N_T}{1 + \frac{g_0}{g_1} \exp \left( \frac{E_T - E_F}{k_B T} \right)}
\]

(3.16)

where \( g_0 \) is the degeneracy factor for the case of \( E_T \) empty of electrons, and \( g_1 \) for the case of \( E_T \) being occupied by one electron.

Combining Eq.3.14 and the above,

\[
\frac{e_n}{c_n} = \frac{g_0}{g_1} \exp \left( \frac{E_T - E_F}{k_B T} \right) \quad \text{for electrons}
\]

(3.17a)

\[
\frac{e_p}{c_p} = \frac{g_0}{g_1} \exp \left( \frac{E_F - E_T}{k_B T} \right) \quad \text{and for holes}
\]

(3.17b)

For \( \frac{g_0}{g_1} = 1 \), these equations show that when \( E_F \) is above \( E_T \), \( e_n > c_n \) and \( e_p > c_p \) so that the state is occupied by electrons, and when \( E_F \) is below \( E_T \), \( e_n > c_n \) and \( c_p > e_p \) and the
state is empty. When \( E_F \) and \( E_T \) are coincident, \( e_n / c_n = g_0 / g_1 \ 1 \), since the degeneracy ratio is of order unity and the occupancy is one-half. Strictly speaking \( e_n = c_n \) when \( E_F \) is located at \( E_T - k_B T \ln(g_0 / g_1) \).

The change in the relative magnitude of \( e_n \) and \( c_n \) (and \( e_p \) and \( c_p \)) with Fermi level position is that the capture rates are determined by the free carrier concentration, so when \( E_F \) is near the band edge and above \( E_T \), \( c_n \) is large because \( n \) is large, whereas when \( E_F \) is below \( E_T \), \( n \) and \( c_n \) are small. This shows how the dynamic quantities \( e_n \) and \( c_n \) are related to the equilibrium occupancy of the trap defined by \( E_F \) and \( E_T \). One needs to keep in mind that \( c_n \) and \( c_p \) are dependent upon the doping of the sample, whereas \( \sigma_n \) and \( e_n \) (\( \sigma_p \) and \( e_p \)) are intrinsic properties of the deep level.

Unlike the hydrogenic levels, deep states may be occupied by more than one electron, in which case there will be a series of deep levels with energies \( E_{T1}, E_{T2}, \) etc, associated with the deep state. If \( E_F \) is below the lowest level, all \( E_T \) are empty of electrons and as \( E_F \) moves up, then the levels become occupied by one electron.

Given Eq. 3.17a and \( c_n = \sigma_n v_{th} n \), then [44]

\[
e_n(T) = \sigma_n v_{th} \frac{g_0}{g_1} N_C \exp\left(-\frac{E_C - E_T}{k_B T}\right) \tag{3.18a}
\]

\[
e_p(T) = \sigma_p v_{th} \frac{g_1}{g_0} N_V \exp\left(-\frac{E_T - E_V}{k_B T}\right) \tag{3.18b}
\]

(the thermal velocities are not identical for electrons and holes).
The inverse of the emission rate is $e_n = 1/\tau_e$, where $\tau_e$ is the emission time constant of a deep level and has the expression:

$$\tau_e = \frac{\exp[(E_C - E_T)/k_B T]}{\frac{\frac{0}{\varepsilon_0}}{\frac{1}{\varepsilon_1}} \sigma_n v_{th} N_C}$$

(3.19)

and for holes

$$\tau_p = \frac{\exp[(E_T - E_V)/k_B T]}{\sigma_n v_{th} \frac{\frac{1}{\varepsilon_0}}{\frac{1}{\varepsilon_1}} N_V}$$

(3.20)

Using the thermal velocity and the effective density of states in the conduction band as:

$$v_m = \sqrt{3 k_B T/m_n},

N_C = 2^{2\pi \frac{k_B T}{h^2}}$$

and assuming a temperature-dependence of the capture cross-section of exponential type:

$$\sigma(T) = \sigma_\infty \exp\left(-\frac{\Delta E_\sigma}{k_B T}\right)$$

(3.21)
then, the temperature dependence of the emission rate and emission time constant are given by

\[
\tau_e = \frac{1}{e_n} = \frac{\exp[-E_{na}/k_B T]}{T^2 \sigma_{na} \gamma_n}
\]  

(3.22a)

or

\[
\tau_e T^2 = \frac{1}{e_n} = \frac{\exp[-E_{na}/k_B T]}{\sigma_{na} \gamma_n}
\]  

(3.22b)

where now \(E_{na}\) and \(\sigma_{na}\) are the \textit{apparent} energy and capture cross section of the defect.

In general, \(\sigma_{na} = \frac{\sigma_0}{g_1} \sigma_\infty, \gamma_a = \frac{v_a}{T^2} = \frac{N_e}{T^2} = 3.25 \times 10^{10} (m_e/m_e) \text{cm}^2 \text{s}^{-1} \text{K}^{-2}\), \(m_n\) is the electron density-of-states effective mass (for n-GaAs \(\gamma_n = 2.3 \times 10^{20} \text{cm}^{-2} \text{s}^{-1} \text{K}^{-2}\), for p-type GaAs \(\gamma_p = 1.7 \times 10^{21} \text{cm}^{-2} \text{s}^{-1} \text{K}^{-2}\), for n-type Si \(\gamma_n = 1.07 \times 10^{21} \text{cm}^{-2} \text{s}^{-1} \text{K}^{-2}\), for p-type Si \(\gamma_p = 1.78 \times 10^{21} \text{cm}^{-2} \text{s}^{-1} \text{K}^{-2}\) [55].

A plot of \(\ln(\tau_e T^2)\) or \((e_n/T^2)\) vs. \(1/T\) is a straight line with the activation energy \(E_{na}\) given by the slope and a pre-exponential factor defined by \(\sigma_{na}\) that can be extracted from the intercept of \(\ln(1/(\gamma_n \sigma_{na}))\) at \(1000/T = 0\). Experimentally it is found that data for most traps fit an equation of this form over many orders of magnitude for \(e_n\).
Care must be taken in the physical interpretation of $E_{na}$ and $\sigma_{na}$. In the formulation above, $E_{na} = (E_C - E_T) + \Delta E_\sigma$. The value of $E_{na}$ does not give information regarding the energy of the trap directly and, even more, this equation holds only if $(E_C - E_T)$ is independent on temperature. $\sigma_{na}$ is an apparent capture cross-section and is proportional to the value of the capture cross-section value from extrapolation of $T = \infty$ through the degeneracy ratio. A thermodynamical approach for the energy and capture-cross section of a trap is given in Appendix 1.

### 3.6 Precautions

The method one uses to fabricate the junction, the electrical properties of the structure as well as the nature of the defects and method of performing DLTS can be sources of errors.

High leakage currents could influence the DLTS peak amplitude in that it will have a rate window dependence. This dependence could be attributed to competition between carrier capture due to leakage current and thermal emission, often leading to errors in the trap energy extracted from the Arrhenius plot [56].

The effect of the device series resistance upon the capacitance of a junction have been mentioned in Section 2.4.1 “Measurement errors and precautions”. For this case, a DLTS measurement will record a change in capacitance given by
\[
\Delta C_m = \frac{\Delta C}{1 + (2\pi f R_s C)^2} \left[ 1 - \frac{2(2\pi f R_s C)^2}{1 + (2\pi f R_s C)^2} \right]
\]

(3.23)

where \(\Delta C_m = \Delta C\) for \(R_s = 0\). As \(R_s\) increases, \(\Delta C_m\) (DLTS signal) decreases and can become zero or even change sign. For example, in Eq.3.23, when \(R_s \approx 1500 \Omega\), for \(C = 100 \text{ pF}\) and \(f = 1\text{MHz}\), \(\Delta C_m = 0\). However, by taking the difference of integration over finite intervals, this can be avoided [57][58].

Interfacial layers can affect DLTS results in two ways: by introducing peaks that are associated with interface states, and by modifying the overall capacitance transient which is observed in response to thermal emission from traps in the bulk of the semiconductor. The interfacial layer may be due to a thin oxide layer at the interface semiconductor-metal. Interface states can produce features in a DLTS spectrum due to thermal release of trapped carriers [59]. Because these states are often distributed in energy across the band gap, these features are usually broad and the decay is not a single exponential. To avoid this problem, the reverse bias should be large and the filling voltage should represent only a small increase in bias, such that the occupancy of these states will not be perturbed and the transient will be due to states in the bulk of the semiconductor. The second effect, that of modification of the transient capacitance due to the charged trapped at the interface can be avoided by using quasistatic changes in the voltage such that the interface states will always respond. Provided that DLTS experiments are performed on diodes with ideality factors close to unity, interface states effects should not distort the transient.
The method of performing the experiment can also lead to errors in the analysis. For example, incomplete trap filling could introduce errors if the filling pulse is too narrow and examples for this situation can be seen (for example) in the analysis for DLTS data for GaAs (Chapter 4).

Related to the nature of the investigated traps, one of the precautions that have to be taken when analyzing DLTS results is that in the reverse-biased region, where all capacitance measurements are being done, there is a high electric field to which the traps may respond. If the bands are changed by an electric field, Poole-Frenkel emission over the lowered barrier and phonon-assisted tunneling may influence the results. For example, for fields around $10^5$ V/cm, it was found that the emission coefficient for the Au acceptor in Si increases with higher fields but is negligible at fields below $10^4$ V/cm [60][61].

Other errors in the analysis of transient and extraction of the activation energy and capture cross-section have a thermodynamic nature. Eq.3.20a (3.20b for holes) where deducted within the implicit assumption that the band-gap remains constant throughout DLTS experiments. Since to perform DLTS scans one needs to change the temperature of the sample, it is important to take into account the temperature dependence of the band gap.

In summary, the theory behind the DLTS technique has been presented. There are experimental precautions that must be followed when performing DLTS measurements, which could, otherwise, lead to substantial errors in the estimated activation energy and capture cross section.
3.7 Experimental set-up

Deep level transient spectroscopy (DLTS) has been used in this work in relation to observation of emission from majority carrier traps. The bias on the diode is pulsed between a voltage near zero \( V_f \), called filling potential, and some reverse bias \( V_r \), within a period \( t_p \), as exemplified in Fig.3.3.

Figure 3.3 Voltage sequence for DLTS measurements
The filling bias need not be zero depending upon the condition of the experiment. Since by applying a reverse bias to a Schottky diode the SCR region is pushed more into the sample, by using a suitable choices of $V_f$ and $V_r$, the distribution of deep levels at different depths can be examined. The $V_f$ voltage is held fixed for a time $t_f$ (filling time), during which time the traps are filled with majority carriers. The duration of the filling pulse $t_f$ should be long enough to guarantee complete traps filling. At the edge of the filling pulse, the recording of the capacitance transients is initiated while the voltage is returned to $V_r$. The period insures that the time during which the diode is reversed biased is long enough such that the capacitance transient reaches its steady-state value. The temperature is then changed, allowing the diode to stabilize, and the process is repeated. The capacitance vs time is visualized in Fig.3.2 and has the general form of Eq.3.13.

The heart of the DLTS is the implementation of the rate window concept initially described by D.V.Lang [56] in 1974. The capacitance transient is fed to a “rate window” which provides maximum output when the trap time constant $\tau$ is equal to a known preset time constant $t_{ref}$. Imagine the case of a diode made out of a material that contains a trap with activation energies $E_T$ and capture-cross sections $\sigma$. As the temperature of the diode is increased, according to Eq.3.21, the emission rate increases and a peak occurs in the rate window output as $\tau = e_n^{-1}$ passes through $t_{ref}$ for the trap. This temperature is characteristic for the trap and for the case of multiple traps, peaks at different temperatures may be visible. The height of the peak is proportional to $\Delta C_0$ and gives the trap concentration $N_t$ (Eq.3.12). Repeating the process with different values of
t_{\text{ref}}, sets of values for e_n and T_{\text{peak}} are obtained, from which the Arrhenius plot is generated and the energy and cross-section are determined.

### 3.7.1 Experimental set-up

The experimental setup is presented in Fig. 3.4. The components are

- SULA Deep Level Transient Spectrometer
- Eurotherm temperature controller and dc power supply for heating the sample.
- vacuum chamber (kept at a pressure of approximately 10 mTorr, sufficiently low to avoid condensation of water on the sample during the cooling and warming up process) and sample holder;
- Computer and LabView software.
Figure 3.4 Apparatus used for DLTS
3.7.1.1 SULA DLTS

The SULA DLTS have 4 modules: pulse generator module, capacitance module, correlator and pulse generator/correlator modules.

The pulse generator module generates the desired sequence of voltages, by setting the value of the $V_r$ (values between 0V to –13V, can be also used as offset for the C-V profiling) and $V_f$ (the value of the filling pulse and the duration can be set). $V_f$ can be set between the value of the $V_r$ and 0V. The duration $t_f$ can have values between 100 nsec-100 msec (the accuracy of the pulse width readings is about 2%).

The period $t_p$, the time interval between successive bias pulses, is set using intervals between 50 µsec to 1000 µsec. BNC connectors are used to communicate with the DLTS, for applying a step up voltage in C-V measurements and for reading the voltage signal that is correlated either with the capacitance or the DLTS signal from the sample.

The Capacitance module is used for monitoring the steady-state capacitance, the value of $V_r$ and $V_f$ and leakage current. The leakage current is very important to be less than 120 µAmp when doing simple C-V measurements or when the pulse is off, since at this value the capacitance meter undergoes overloading. However, during pulsing periods, the capacitance meter can tolerate large currents (up to 30mAmps).

The correlator module allows control and amplification of the capacitance transient. The signal-to-noise ratio is independent of this parameter. The rate windows can be set from this module, and the range of accessible values is between 0.086 – 430
msec. The rate windows selected are accurate within 2%. This represents a shift of less than 1K in the DLTS Arrhenius plot with essentially no change in the slope.

The last module can be used, having the same settings as those in the Pulse-Generator module, to record the value of $\Delta C$ at a different rate window.

The difference between Lang’s rate window concept and this DLTS is that $\Delta C$ recorded here is the difference between two average capacitance values obtained by integrating over finite time intervals the transient (both values are obtained from integrating over $3 \cdot t_i$, first starting at time $t_i$ and then at time $5 \cdot t_i$). This method reduces the sensitivity of the technique to noise influences, especially for low trap concentrations.

### 3.7.1.2 Temperature controller

The Eurotherm temperature controller is an extremely small and versatile device. It can be used with a variety of temperature sensors (Pt sensors, K and J thermocouples, etc) and over a large range of temperatures (-200 to 1200°C) and performs a PID control on the voltage applied on a resistor. For this work, I used the device mostly for reading temperatures since, for the resistor used to heat up the sample, the overshoot in the temperature could not be controlled accurately, resulting in a temperature overshooting of 5-10 degrees, which would have made the spectra recording and analysis difficult. The temperature is read using a J thermocouple, and the values are recorded using the computer and a LabView program through a driver for the
DLTS device (Appendix 2). The resistor used for heating up the sample is a simple 5W power resistor. Since the diodes used in this work have been fabricated in our lab, their leakage currents do not permit heating of the samples at very high temperatures (>470K).

3.7.1.3 Dewar and Sample Holder

The sample is mounted on the sample holder that is mounted on the bottom of a dewar, inside a vacuum chamber. When the dewar is filled with liquid nitrogen, the diode temperature could be as low as 170 K, depending upon how good the thermal contact is made. This makes the available temperature range for DLTS experiments to be between 170 K-470K, depending upon thermal contacts and sample leakage currents.

The diodes are usually held in place on the sample holder (made out of SG10 double circuit board that has been milled down such that there are four Cu corners for making the contacts) using pressure pins.

During this work, I have been using different methods to hold the samples in place and make the electrical contacts. In a first stage, when the electrical contacts to the samples were made using Epoxy, the sample holder was just the circuit board to which the wires from the sample and the wires to the DLTS were soldered. The thermocouple was held in place using a small screw, while the thermal contact of the sample with the board was made using thermally conductive epoxy. The disadvantages
of this set-up were that once the wires were attached to the sample they could not be removed, the contacts being also big (epoxy contact spreading is hard to control for diameters less than 2mm. Another disadvantage was that once the sample was glued to the holder it could not removed, and no other analysis could be performed.

In the second stage, the electrical contacts to the sample were made using Au or Ni covered spring pins, from which wires were going to the DLTS. This new approach enabled reductions in the size of the contacts, currently as small as 1/2 mm. Multiple and close contacts could be deposited. The sample could be removed from the holder for further analysis or contact deposition. The major disadvantage of this set-up is the degradation of the contacts by repetitive use of the pins, through scratches and metal penetration. Measures were taken to prevent these effects, such as using magnifying glass to select the intact contact, avoidance of too much pressure of the pins, and thicker metallic contacts. The thermal contact of sample to the circuit board is made through the pressure the pins exercise on the sample. The thermocouple is fixed using a screw very close to the sample. For all set-ups, the thermocouple could not be fixed on the samples due to an increase in the noise of the transient.

The schematic of the sample holder for this case is shown in Fig.3.5.
3.7.1.4 Software set-up

For this experiment I wrote several programs using LabView, given the necessity to record temperature changes and DLTS signal at the same time. In LabView, the user builds an user-interface, behind which the flow diagram is hidden. The flow diagram and the interface are presented in Appendix 2.
To perform a DLTS scan the following steps are necessary:

1. preparation of sample (growth or purchase of material, x-ray and other analysis, cleaning);
2. fabrication and I-V characterization of contacts, elimination of junctions with high leakage currents;
3. C-V characterization of Schottky barriers obtained and elimination of those that exhibit no change in the capacitance as a function of voltage (a result of poor adhesion or reminiscent oxide layer at the interface);
4. fast DLTS scan for optimization of DLTS conditions ($V_r$, $V_f$, $t_f$ and rate window);
5. slow DLTS scans (ramping in temperature of approximately 5-10 sec/degree) for different rate windows with same $V_r$, $V_f$, and $t_f$ to obtain activation energies and capture cross-sections;
6. slow DLTS scans with the same rate window and different $V_r$, $V_f$ or $t_f$ to investigate defect concentration in the bulk (by varying only $V_r$, $V_f$) and pulse width dependence of the trap concentration (by varying $t_f$ only).

Each of the above steps has been followed in the analysis for all the samples described in the next chapters and the results will be explained accordingly.
Chapter 4

DLTS for GaAs

4.1 Introduction

GaAs is a III-V direct gap semiconductor (band gap of 1.35-1.445 eV at 300K) with a zinc-blende structure (lattice constant at 300K is 5.65 Å) which has been the subject of intense research since middle 1950’s as a suitable semiconductor for a variety of applications. However, deep defects in the crystal structure, though known to greatly influence the electrical properties of GaAs devices, were not investigated in this material until 1970. The first published work on defects in GaAs investigated using deep-level transient spectroscopy is that of D.V. Lang [26]. This paper is a follow up of another article that introduces a fast capacitance transient apparatus with application to ZnO [62], which is the predecessor of DLTS. Using DLTS on GaAS, D.V. Lang found signatures for two defects with energies of 0.44eV and 0.76 eV, respectively, which were identified as being hole traps. Since then, many papers have been published on the
subject of defects in GaAs. A review of the energy levels depending upon the growth conditions is given in [63].

DLTS investigation on material grown by a variety of techniques (LPE, VPE, MOVPE, MBE) has shown that, independent of the growth method, one defect is always present, having an activation energy of (0.285-0.825 eV). This defect, labeled EL2, has been associated with the arsenic antisite complex (a complex of arsenic on a gallium site and an arsenic interstitial). EL2 in a high concentration in VPE grown GaAs (up to $3 \times 10^{14} \text{cm}^{-3}$) sometimes results in semi-insulating material or in local variation of FET threshold voltages.

### 4.2 Samples description

I have started this work with investigation of EL2 defect in two sets of GaAs Schottky barriers (SB). One sample was obtained from Dr. Danie Auret, University of South Africa, Pretoria, South Africa (will be referred to as S1). The second sample was fabricated from a purchased GaAs wafer, from Wafer World, Inc (will be referred to as S2). Table 4.1 summarizes the information that was available regarding both samples.
<table>
<thead>
<tr>
<th>Sample from Dr. Auret (S1)</th>
<th>Sample from Wafer World, Inc (S2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MBE growth method</td>
<td>Growth by Horizontal Bridgeman method</td>
</tr>
<tr>
<td>Si doped, doping concentration of 1\times10^{18}\text{cm}^{-3}</td>
<td>Si doped, doping concentration of 0.6-1 \times10^{18}\text{cm}^{-3} mobility of 1.4-2.6 \times 10^3\text{cm}\Omega.</td>
</tr>
<tr>
<td>OMVPE epilayer , doping concentration of 1\times10^{16}\text{cm}^{-3}</td>
<td></td>
</tr>
</tbody>
</table>

Table 4.1 Description of GaAs samples used in this study

### 4.3 Sample preparation - cleaning

The first step in preparing samples for contact deposition is cleaning the sample. This is very important since on the surface of the material, besides oil and other impurities deposited during handling and packing of wafers, oxides could form as a result of air exposure.

For the case of the S1, the following recipe has been followed:

1. 2 min in boiling trichloroethylene (TCE), 2 min in boiling isopropanol, rinse in water holder #1 for 1 min, rinse in water holder #2 for 1 min, etch in 100:1:3 water:peroxide:ammonia for 45 sec, rinse in water holder #1 for 1 min, rinse in water holder #2 for 1 min, 2 min in 1:1 HCl:water, rinse in water holder #1 for 1 min, blow dry in N2.
For S2, in a first stage there has been no cleaning applied to the sample, upon the presumption that the wafer has been packed under inert Ar atmosphere. However, after contact fabrication, desiring to improve the I-V characteristics, I have cleaned the samples using the following recipe:

5 min in boiling Ethanol, 5 min ammonia hydroxide solution 1:20 with deionized water, rinse in deionized water several times, blow dry with air.

4.4 Sample preparation – contact fabrication

In the case of S1, the ohmic contacts have been fabricated on the bulk-\textsuperscript{n+}-side (back side of the sample) by sputtering of 5 nm Ni, followed by 100 nm AuGe (+/- 8% Ge) and 200 nm Au, then annealing at 450 C for 5 min.

The Schottky barrier has been formed on the OMVPE epilayer by deposition of 1000 Å of Ru small dots (diameter of 0.5 mm) by dc-sputtering.

To obtain a sample suitable for DLTS, I have used several metals for ohmic contacts and Schottky barriers, depending upon the electrical characteristics as seen in I-V curves. The contacts used are shown in Table 4.2.

The Al contacts have been evaporated in a standard Edwards evaporator system with a base pressure of 4x10\textsuperscript{-6}Torr, while the sputtered contacts have been fabricated using a Denton Vacuum sputtering chamber with a base pressure of 1x10\textsuperscript{-6} Torr.
The small contacts for SB fabrication have been deposited using brass masks that have been cleaned in acetone and methyl alcohol prior to use.

<table>
<thead>
<tr>
<th>Cleaning method</th>
<th>Ohmic contact</th>
<th>Schottky contact</th>
<th>Discussion of I-V</th>
</tr>
</thead>
<tbody>
<tr>
<td>No cleaning</td>
<td>epoxy back contact</td>
<td>Evaporation of Al small dots (3mm, 2mm, 1mm diam.) (1000 Å thickness)</td>
<td>high ideality factors and leakage currents (Fig.4.1)</td>
</tr>
<tr>
<td>Cleaning as described</td>
<td>epoxy back contact</td>
<td>Evaporation of Al small dots (3mm, 2mm, 1mm diam.) (2000 Å thickness)</td>
<td>Improvement of ideality factor still high leakage currents</td>
</tr>
<tr>
<td>Cleaning as described</td>
<td>Evaporation of Al back contacts (2000 Å thickness)</td>
<td>Dc-sputtering of Pd (1000 Å thickness) dots (2mm diam.)</td>
<td>Improvement in ideality factor and leakage currents</td>
</tr>
<tr>
<td>Cleaning as described</td>
<td>Evaporation of Al back contacts (2000 Å thickness)</td>
<td>Dc-sputtering of Au (1000 Å thickness) dots (2mm diam.)</td>
<td>Even more improvement in ideality factor and leakage currents</td>
</tr>
</tbody>
</table>

Table 4.2 Methods of cleaning, contact deposition and I-V results for GaAs
4.5 Connecting wires to the sample

One of the problems that had to be overcome was to find the method of connecting wires to the SB thus fabricated. In the beginning I was using Cu pins, which turned out to be too big and required permanent scratching off of the oxide. Next, I have tried epoxy contacts on the dots and the back of the sample to attach regular wires. The problem with this method was that the epoxy wets the surface and spreads on it, therefore if small diameters SB dots are used, the precision with which the epoxy contacts can be made is decreasing. Other problems were to keep the wire in place while the epoxy was drying (1 h at 60ºC) and the degradation of the contact performances as the sample was left in the air for several days. Considering this, I designed a small sample holder and used Au/Ni small pressure pins for making the contacts. The advantages are that the Schottky barriers (SB) can be as small as 0.5 mm diameter or less, the pins are inert to oxygen, wires can be easily attached to them and their electrical resistance is very small, and that the SB dots can be placed close to each other. The major disadvantage is that by applying too much pressure on the pins, the SB can be damaged. This is the main method of making the electric contacts of samples to the DLTS.
4.6 I-V characterization - Results

After contact fabrication, the junctions I-V characteristics have been analyzed. The results for the case of Al Schottky contacts and epoxy back contacts are shown in Fig.4.1. In Fig.4.1 right, linear characteristics are presented while in Fig. 4.1 left, logarithmic dependence of the current at forward bias is shown.

As it can be deduced from the slope of the log I vs. V, high ideality factors (higher than 8) characterize these junctions; therefore I have decided to use metals that are inert to oxygen, such as Pd and Au, as shown in Table 4.2.

I-V results are shown in Fig.4.2. The diodes fabricated this way had lower ideality factors and leakage currents, and the barriers made out of Au show better characteristics than the Pd SB. As a comparison, I-V characteristics for the best diode that I have fabricated (S2) and the diode fabricated by Dr. Auret (S1) are shown in Fig.4.3.
Figure 4.1 Linear (left) and logarithmic (right) I-V characteristics for GaAs-Al SB.

On the right, the direct currents are shown in Log display to emphasize the differences between the different Schottky diodes.
Figure 4.2 Linear and logarithmic I-V characteristics for GaAs-Au, GaAs-Pd and GaAs-Al SBs.

It can be seen that the diode fabricated using Au has the best direct current characteristics.
Figure 4.3. I-V characteristics (linear and logarithmic) for GaAs-Ru and GaAs-Au Schottky diodes. The data show that the GaAs-Ru diode has better characteristic in terms of leakage current and direct current, as seen on the right side of the Figure.
4.7 I-V characterization - Discussion

The high ideality factors obtained for the case of Al SB could be associated with interface states existent at the interface of the metal and the semiconductor [64].

These interface states can be introduced during the process of contact formation or with an oxide layer at the surface of the sample. Since the Al deposition is done using small pieces of Al cut out of a Al rod that is stored in air, I believe the Al small contacts were already contaminated with oxygen and water. Also, because the contacts are fairly thin layers (approx. 1000Å), oxidation of Al could take place while taking the sample out of the chamber for testing and storing.

On the other hand, the difference between the Au and Pd contacts could come from other causes. These materials are fairly stable during cooling and warming and since both Pd and Au are deposited in a sputtering chamber and the targets are always under vacuum, there is less interaction of the material with the atmosphere.

It is also known [65] that, depending upon the annealing temperature, Au or Pd contacts have better characteristics. If the samples are annealed to temperatures above 420º C, Au interacts with Ga forming AuGa complex, which is responsible for poor morphology of the contact, while Pd does not. At temperatures well below 420º C, Au does not interact with Ga while Pd forms an intermediate complex Pd₃GaAs, reducing the characteristics of the contact.

The total number of SB that were fabricated and tested for GaAs investigation of EL2 defect, was 15 Al SB (each in average with 6-8 Al dots), 10 Pd SB diodes (also
with 6-8 Pd dots each sample) and 15 Au SB (each with 6-8 Au dots). The size of the GaAs pieces used was between 2x2 to 6x6 mm, while the contact dimension was varied from 0.5 - 2mm in diameter.

As compared with the best SB I have fabricated, the S1 SB has better I-V characteristics as shown in Fig.4.3. It can be seen that both the forward and the reverse characteristics for the S1 SB are at least one order of magnitude better than those of the S2. The ideality factors, a measure of how interface states affect the performance of a diode, were 1.1 and 3.2 for S1 and S2, respectively. The difference in the value of the ideality factors could come from a better interaction of Ru with the GaAs surface and the absence of a highly doped epilayer in the case of S2.

The series resistance for these two junctions, calculated from a plot of $(I \frac{dV}{dI})$ vs. $I$, had values of approximately 50Ω and 250Ω for the GaAs-Ru and GaAs-Au SB, respectively.

After performing I-V characterization, the best in terms of ideality factors and leakage currents (sample S2) were chosen for C-V and DLTS analysis.
4.8 C-V characterization – Results

C-V measurements were performed for both samples and are presented in Fig. 4.4. From experimental data, values of 0.98eV and 1.02eV for the build-in voltage ($V_b$) were obtained for S2 and S1.

From C-V measurements, i.e. $1/C^2$ vs. V, the values for the majority carrier density have been estimated to be $3.4 \times 10^{17}$ cm$^{-3}$ and $1.1 \times 10^{17}$ cm$^{-3}$ for S1 and S2.

From C-V measurements the carrier concentration profile as a function of depth was calculated for each SB and is presented in Fig. 4.5.
Figure 4.4 C-V characteristics for GaAs-Ru and GaAs-Au Schottky diodes. The free carrier concentration and built-in voltages are obtained from the data on the left.

Built-in voltages are
0.98 V for GaAs-Ru
1.02 V for GaAs-Au

\[ N_d = 3.4 \times 10^{17} \text{ cm}^{-3} \text{ for GaAs-Ru} \]
\[ N_d = 1.1 \times 10^{17} \text{ cm}^{-3} \text{ for GaAs-Au} \]
Figure 4.5 Carrier concentration distribution in the bulk for both SB
It can be seen that the free carrier concentration is fairly uniform within the bulk of the samples.
4.9 C-V characterization – Discussion

The values obtained for the built-in voltage for both junctions, indicating the band bending at the interface of the metal and semiconductor, are in good agreement with the experimental values usually found in literature [64].

From the simple point of view of the Schottky model, which assumes that the built-in voltage should depend upon only on the work function of the metal and the electron affinity of the semiconductor as ($\phi_m - \chi_s$), for GaAs-Ru, $V_b = 4.71 - 4.07 = 0.64$ eV and $V_b = 5.1 - 4.07 = 1.03$ eV for GaAs-Au. The difference in these values and the experimental ones (from page 74) comes from the fact that the theoretical Schottky model neglects the effect on the band bending that interface states might have.

The carrier concentration values obtained for the junctions are lower than the reported ones from Dr. Auret and the GaAs wafer. As pointed out in Chapter 3, the values determined from C-V profiling represent the majority carrier density and not the doping density.

From the depth profiling of the carrier concentration, it can be seen that there is no visible variation with depth, as sampled by SCR spreading into the substrate with increasing the reverse voltage.
4.10 DLTS characterization – Results

For each of these two samples, DLTS measurements were performed under several different conditions:

1. same reverse bias and filling pulse values, but different rate windows, to determine the activation energy and estimate the capture cross section;

2. same reverse bias, filling pulse and rate window but different duration for the filling pulse to investigate any dependence of the trap on the width of the pulse;

3. same filling pulse and rate window but different reverse biases to investigate the distribution of the defects with the depth in the bulk.

Figure 4.6 shows the dependence of the $\Delta C/C$ DLTS signal for the GaAs-Ru and GaAs-Au for different rate windows. The $\Delta C/C$ signal has been converted to defect concentration according to

$$N_T = 2 N_D (\Delta C/C_0)$$  \hspace{1cm} (4.1)

where $N_T$ is the concentration of the defect, $N_D$ and $C_0$ are the free carrier concentration and capacitance of the junction at the applied reverse bias voltage. The EL2 defect is present in concentrations of approximately $8\times10^{13}$ cm$^{-3}$ for S1 and $2\times10^{13}$ cm$^{-3}$ for S2.
Figure 4.6 DLTS signal for different rate windows for GaAs-Au (left) and GaAs-Ru (right)
The dependence of the peak size upon the width of the filling pulse is shown in Fig. 4.7 for both junctions.

To investigate the concentration of EL2 within the bulk, DLTS measurements were performed for a fixed rate window and filling pulse and different reverse biases and filling pulse values and are presented in Fig. 4.8.

Arrhenius analysis was performed for both samples and the Arrhenius plot is presented for both samples in Fig. 4.9. Assuming a temperature independent capture cross section, the activation energies for EL2 defect in both samples was found to have a value of $(0.87 \pm 0.01) \text{ eV}$ for the GaAs-Ru and $(0.85 \pm 0.01) \text{ eV}$ for GaAs-Au.
Figure 4.7 Peak dependence on the width of the filling pulse for fixed $V_r$, $V_p$ and rate window for GaAs-Ru (left) and GaAs-Au (right).
Figure 4.8 Defect concentration of EL2 defect in the bulk

Figure 4.9 Arrhenius plot and energy values for GaAs-Ru and GaAs-Au SB
4.11 DLTS characterization – Discussion

From Fig. 4.6 it can be seen that the two junctions are fabricated from materials with different EL2 defect concentrations. It is known that many factors such as method and temperature of growth, flux of nitrogen, etc, have influence upon the concentration of this defect [63]. The values for EL2 concentration found for these two samples are similar to values obtained by other groups as can be seen in Table 4.3.

<table>
<thead>
<tr>
<th>Method of growth</th>
<th>Concentration of EL2 (cm$^{-3}$)</th>
<th>Activation Energy (eV)</th>
<th>Capture cross section (cm$^2$)</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>(LEC)</td>
<td>2x10$^{15}$-6x10$^{15}$-3x10$^{16}$</td>
<td>0.825</td>
<td>1.2 x 10$^{-13}$</td>
<td>[66]</td>
</tr>
<tr>
<td>MOVPE</td>
<td></td>
<td>0.785</td>
<td></td>
<td>[67]</td>
</tr>
<tr>
<td>MBE</td>
<td>10$^{12}$-10$^{14}$</td>
<td>0.825</td>
<td></td>
<td>[68]</td>
</tr>
<tr>
<td>S1</td>
<td>8x10$^{13}$</td>
<td>0.87</td>
<td>1.3x10$^{-11}$</td>
<td>[this study]</td>
</tr>
<tr>
<td>S2</td>
<td>2x10$^{13}$</td>
<td>0.85</td>
<td>3.3x10$^{-11}$</td>
<td>[this study]</td>
</tr>
</tbody>
</table>

Table 4.3 Concentration, activation energy and capture cross section of EL2 defect for GaAs grown by different techniques

In the case of S1, it can be seen from Fig. 4.7 that there is no evident change in the size of the peak as the width of the filling pulse is increased from 10μsec to 10
msec, while in the case of S2, there is a decrease in the size of the peak as the width is decreased to 100 µsec, but it saturates for width pulses longer than 10 msec. This could be explained assuming an electron capture rate that is limited by a time-dependent Coulomb barrier, with the barrier height proportional to the number of electrons already trapped [69]. Such a situation would occur if the traps would be distributed along line defects in the crystal, i.e. dislocation lines (typical dislocation densities in LEC grown crystals, for example, are in the range $10^6$-$10^8$ cm$^{-2}$). Similar studies on GaN [70] have found a similar behavior for two deep centers upon the density of dislocation in RMBE-grown Si-doped GaN.

The depth investigated in the case of GaAs-Ru sample were between near contact interface to 0.13 µm deep in the bulk, depending upon the reverse bias voltage. As seen in Fig. 4.8, there is no substantial change in the EL2 concentration. For the case of $V_r = -4V$, $V_f = -2V$, a volume of bulk between 90 nm and 0.13 µm deep was sampled, with no change in the concentration of the defect. The EL2 depth dependence for the GaAs-Au SB was not investigated due to the relatively high leakage currents and degradation of the junction with repeating heating and cooling. All the analysis was done using $V_r = -1.4V$ and $V_f = +0.5V$ which pushes the space charge region to about 0.1µm deep in the bulk.

The activation energies for EL2 defect in both samples from Arrhenius analysis (0.87 eV and 0.85 eV for the GaAs-Ru and GaAs-Au, respectively) are in good agreement with the ones presented in Table 4.3 and agree with others within the errors.
Estimated values for the capture cross section are calculated from the intercept of the Arrhenius plots to have values of $2 \times 10^{-12}$ and $8 \times 10^{-11}$ cm$^2$, for GaAs-Ru and GaAs-Au, respectively. However, the error associated with these values cannot be estimated since, as pointed out in Chapter 3, and Appendix 1, the true capture cross-section differs from the one inferred from Arrhenius analysis by prefactors dependent upon the degeneracy of the deep center and an entropy factor that accounts for the entropy change when an electron is emitted from the center.

4.12 Conclusions

The analysis presented above on two GaAs Schottky barriers is in agreement with published results. This proves that the apparatus and methods I am using in this work give the correct results and therefore are suitable for investigating deep defects in semiconductors.
Chapter 5

DLTS for GaN

5.1 Introduction

In this chapter GaN samples grown using different techniques are investigated to determine the suitability for DLTS analysis. MOCVD grown n-type GaN show the predominant B defect as seen by other experimental groups as well. No DLTS analysis on MBE and rf-sputtered GaN material was performed due to the absence of a suitable Schottky barrier.

The advancements and developments in the light-emitting devices area that has seen recent years have spurred an impressive amount of publications regarding research in III-V materials, such as GaN, GaAlN, etc. Some of their most interesting applications in optoelectronic devices are, for instance, the fabrication of blue/green light emitting diodes (LED) and lasers. These devices have properties that are by far better than LED’s and lasers made out of conventional GaAs and related materials.
The performance improvements of optoelectronic devices fabricated out of GaN and other related materials depend strongly upon the features of structure properties and the intrinsic and extrinsic impurity defects in nitride compounds; therefore, having accurate knowledge about these properties has a major impact on the device fabrication and optimization. Since GaN is a successful candidate material for high temperature electronics and for blue-UV lasers, it is important to know in what degree the operational parameters depend not only on the structure as grown of the crystals, but also on the doping and impurities.

GaN usually crystalizes in the hexagonal wurtzite (WZ) structure with two formula units per unit cell (4 atoms per cell). Strain and defects may distort the lattice constant from their intrinsic values and thus there is a wide dispersion in the reported values. For WZ GaN, at room temperature, lattice parameters of $a_0 = 3.1892 \pm 0.0009 \text{Å}$ and $c_0 = 5.1850 \pm 0.0005 \text{Å}$ are generally accepted. For the zinc blende (ZB) polytype of GaN, the calculated lattice constant based on the measured Ga-N bond distance in WZ GaN is $a = 4.503 \text{ Å}$, while the measured values ranges from 4.49 to 4.55 Å.

The band gap as obtained from theoretical calculation is found to be approx. $3.34$ eV for zinc blende structure, while for wurtzite the predicted value is only $0.11$ eV larger ($3.45$ eV).

One of the major problems in producing high quality GaN sample is the lack of an ideal substrate material. Sapphire remains the most common substrate for nitride heteroepitaxy. GaN grown on (0001) plane sapphire has its (0001) plane parallel to the substrate. Since there is a mismatch of about $13\%$ between the lattice constant of GaN
and sapphire, large numbers of dislocations are inevitably formed in the epitaxial material. Dislocation defects with concentration of up to $10^{10} \text{ cm}^{-2}$ are found on samples grown by MOCVD. Beside dislocations, the most prevalent structural defect observed in GaN thin films are threading dislocations, stacking faults and nanopipes.

As grown GaN samples are almost always n type with the concentration of the conduction electrons ranging typically from $10^{17}$ to $10^{20} \text{ cm}^{-3}$, which is much higher than the detected impurities. This strongly suggests that the doping is due to native defects. The residual donor was tentatively identified with the nitrogen vacancies [71][72], while more recent studies exclude nitrogen vacancies as being the source of intrinsic n-doping and suggest contaminants such as oxygen as the cause [73][74].

One of the earliest theoretical studies regarding deep levels generated by point defects in GaN [72], reported energies for point defects such as nitrogen vacancies (thermal activation energies between 30meV and 400 meV below conduction band $E_c$), nitrogen anitisesites (0.8 and 1.1 eV below $E_c$), and gallium vacancies. A later study [75] summarized theoretical calculations regarding native defects in GaN. Values for the thermal activation energies for nitrogen and gallium vacancies as well as interstitial Ga and N, were calculated. Later studies [76] [73] confirmed that nitrogen vacancies are most probably forming in p-type GaN while Ga vacancies are forming in n-type material.

Experimental studies regarding deep defects in GaN include techniques such as DLTS, optical DLTS, electron-paramagnetic resonance, etc. Many researchers investigated the as-grown material using the space charge region of Schottky diodes
Numerous groups investigated the effects of electron, helium, and proton radiation upon defect formation and evolution.

The method of contact (ohmic and Schottky) deposition might create defects at and near interface between GaN and the metal, such as is the case for metal sputter deposition in GaN.

Another important aspect regarding GaN is what deep defects are promoted by the method and parameters of growth. Extensive studies on this topic include those of Fang and Look. Most of these studies were done on as grown n-type GaN material using DLTS.

As compared with n-type GaN, there are fewer studies regarding defects in p-type GaN, due mainly to the difficulties in growing and activation of dopants for p-type material.

One of the predominant defect, characteristic to all GaN samples, irrespective of growth method is the so-called “B defect” (earlier denoted E2) with an activation energy of $E_c - E_T = (0.58-0.62)$ eV. Earlier studies suggested that this defects could be due to impurities such as C or Mg. A more recent study showed that this defect could be effectively suppressed by In doping and it was suspected of being a $N_{Ga}$ defect. A later study associated this defect with $N_{Ga}$ present along dislocation lines.

Theoretical studies show that indeed $N_{Ga}$ forms a defect below the conduction band and has activation energy similar with that of the experimentally found B defect.
5.2 MOCVD grown GaN

5.2.1 Sample growth and structural characterization

Several MOCVD grown GaN, n-type, were grown using the MOCVD reactor in the Chemical Engineering Department. The recipes used can be found in Ref [92]. Typical thickness for the samples used in this study was 0.6-1.2 µm, as measured using a profilometer (as described in Ref. [93]).

X-ray diffraction was used to analyze the crystal quality of several samples, depending upon the growth conditions. Typical x-ray diffraction data are presented in Fig.5.3 for sample S1029. The dominant feature is the GaN (0002) peak at $34.22^\circ$.

Values for lattice constants as obtained from data using Bragg’s law are in the following ranges:

- for the in-plane lattice constant $a = (3.3-3.4) \, \text{Å}$ (reported value of 3.19 Å)
- for the out-of plane lattice constant $c = (5.16-5.24) \, \text{Å}$ (reported value of 5.18 Å)

GaN material grown on sapphire or any other mismatched substrate is known to grow in island, forming crystallites of sizes dependent on growth method and conditions. Samples investigated in this work show crystallite sizes varying from 900Å–60µm. A scanning electron emission picture is shown in Fig. 5.2 for a GaN film made of crystallites with sizes from 1-60µm.
Figure 5.1 X-ray diffraction data for MOCVD GaN

Figure 5.2 Scanning Electron Microscope micrograph of a GaN crystallite.
Samples grown using this reactor are known to form a large number of dislocations as seen from the predominant yellow band present in photoluminescence experiments [93]. Usually a very strong luminescence is observed at 358.5 nm, 378 nm and 388 nm corresponding to near band edge emission and emission from free and donor-bound exciton, as well as emission from donor levels. A wide band can be seen in all samples between 500 – 700 nm (around 2.2eV), in the yellow part of the spectrum. This band has been associated by many groups with transitions between a shallow donor level and a deep level created as a consequence of high number of dislocation defects present in the samples [94].

Hall effect data at 300K showed that carrier concentration values are in the range (2x10$^{16}$-7x10$^{17}$) cm$^{-3}$.

### 5.2.2 Diode preparation

Attempts to prepare Schottky barriers were carried out using several different samples following cleaning and contact deposition recipes that can be found in literature [65] [95 98]. The best diodes as judged from I -V characteristics were obtained for contacts to samples that were done using the following recipe:
• For cleaning: 5 min in ammonia hidroxide: deionized water, rinsing with deionized water. Samples were placed immediately in the deposition chamber;

• Ohmic contacts were fabricated by dc-sputter (as described in Section 4.4) of 1000 Å of Ti (stripes of approx. 2x6 mm). After Ti deposition, the sample was fast annealed at 300 C for 5 min in N$_2$ in order to improve the quality of the ohmic contact;

• Ni and Au Schottky contacts with thickness 1000-1200 Å were also dc-sputtered using masks with dots having diameters of 0.5 mm.

5.2.3 I-V characterization – Results

To estimate the quality of a junction, pressure pins were used to provide the electrical connection, as discussed in Chapter 4. Care was taken not to damage the contacts. I-V measurements were taken for several samples. Several different samples were investigated using similar contacts. I-V characteristics for six samples are presented in Fig. 5.3. It can be seen that the electrical properties of the junctions differ from sample to sample. In general, the ideality factors are in the range of 1.8-2 while the series resistance values obtained from I-V characteristics are in the range $10^2$-$10^5 \, \Omega$. 
Figure 5. 3 I-V characteristics for several GaN MOCVD grown samples with Ni and Ti contacts.

The junctions have been made from different samples, grown by MOCVD.

No correlation between the growth process and the quality of the sample can be inferred from I-V data.
In order to estimate the quality of the various dots on the same sample, for each prepared sample a number of 16 small dots were used for Ni or Au Schottky contact and two big (2x6 mm) stripes for ohmic contacts. It was observed that different dots have different thickness and shape, therefore influencing the quality of the contact. Several I-V characteristics for same ohmic contacts but different Schottky dots on the same sample are presented in Fig. 5.4.

To compare barriers formed by different metals, beside Ni, Au contacts have been also fabricated on the same sample. The I-V measurements were done using the same ohmic contacts as those used for Ni barriers. The characteristics are presented in Fig. 5.5. It can be seen that both metals form suitable Schottky barriers with Ni barriers being slightly better. Turn on voltages for the diodes are between 1.3-1.7 V while the barriers values obtained from logarithmic I-V data (intercept of a linear-squares fit to the linear portion of the I-V characteristic) are between 1.5-1.8 eV. No I-V-T analysis was performed on these samples.
Figure 5.4 I-V characteristics for different Schottky contacts on the same sample. Using different dots on the sample, different diodes are actually investigated. Their properties differ because of non-uniformity of material and contacts.
Figure 5.5 Ni and Au Schottky barriers on same MOCVD GaN. In terms of I-V characteristics, the junctions have similar characteristics, with the GaN-Ni ones being slightly better.
5.2.4 I-V characterization – Discussion

One of the most important problems in producing GaN devices is to have reliable and reproducible contacts. Review of contact fabrication and optimization can be found in [65][98][99].

The quality of a contact is influenced not only by the quality of the GaN material, but as well as by the material used for contacts. The best ohmic contacts to date are fabricated using an Al/Ni alloy or using a semiconductor with a narrower band gap such as InN/GaN superlattice [100]. Due to the limited choices existent in our laboratory, only Ni, Ti, Pd and Au can be dc-sputtered, while Au and Al can be also evaporated. It is therefore to be expected that the specific resistance of contacts fabricated in this work will be high. The diode performance will be affected by the contact resistance, and it can be seen in all I-V characteristics.

It is clear from numerous studies that there are two factors that affect the performance of contacts on GaN, namely the island nature of GaN growth on mismatched substrates and the interface states. The first factor can lead to lateral and local variation on the defect density affecting the transport properties. This can be seen in Fig.5.5, for the reverse biasing of the GaN-Ni diode, while it is absent from GaN-Au sample, probably due to the non-uniformity of the sample. The second factor plays a role in the exponential factor for the current through high ideality factors [64]. For all investigated samples in this work, the ideality factors, greater than 1, indicate that the surface states play a role in the transport properties.
Leakage currents up to several microamperes, due to either tunneling through interface states or trap related recombination are present in some of the diodes fabricated for this work, making them unsuitable for DLTS analysis. The junction of choice for further analysis is the GaN-Ni Schottky barrier (sample S1029) shown in Fig. 5.5.

5.2.5 C-V characterization-Results

C-V measurements were performed at room temperature using same technique as described in Chapter 4. C-V characteristics are shown in Fig.5.6. A build-in voltage of 1.99V was found for the structure. From $1/C^2$ vs. V intercept, the concentration of free carriers was calculated to be approximately $2 \times 10^{16}$ cm$^{-3}$, in good agreement with Hall effect results. From C-V data, depth profiling calculation were performed to obtain the profile of free carriers with depth.
Figure 5.6 C-V characteristics for GaN-Ni Schottky barrier at 300K.

The free carrier concentration and the built-in voltage are obtained from the left side of the graph.
5.2.6 C-V characterization-Discussion

The value obtained for the built-in voltage, representing the band bending at the interface of the metal and semiconductor, is slightly higher than typical values found in the literature (0.58-0.81 eV) [45]. This is not unusual since it has been found that the barrier height of n-type GaN Schottky junctions is often reduced by using different cleaning method. It has been reported by Cao et al. [45] that boiling n-type GaN in \((\text{NH}_4)_2\text{S}\) solution immediately prior to metal deposition reduces the barrier height by minimizing oxide formation. Other methods of cleaning, even using HF which also removes the surface oxides are not as efficient, mostly due to the fact that cleaning using \((\text{NH}_4)_2\text{S}\) also prevents immediate oxidation by forming a Ga-S monolayer on the surface. In this work, the method of cleaning was ammonia hidroxide, and a short time elapsed between cleaning and placing the sample in the metal deposition chamber, resulting in a thin oxide that might have already formed on the surface and thus increasing the barrier height.

The free carrier concentration obtained from C-V measurements is roughly uniform within the sample. C-V characteristics are usually excellent methods to investigate the profile of free carriers within the bulk of a sample by controlling the applied reverse voltage applied to the sample. For the sample shown in Fig. 5.6, the depth sampled is within 0.6 \(\mu\text{m}\) from the surface of the sample. The depth sampled in C-V measurements is often limited by leakage currents. In this work for example, for many samples, high leakage currents (in the order of 100\(\mu\text{A}\)) saturate the C-V test unit,
making impossible to sample the whole depth of the sample. If the sample is highly doped, then the depth sampled is reduced even further, and sometimes the increased tunneling probability of free carriers to the conduction band (for \(n\)-type material), makes impossible any C-V measurements.

The great advantage of using C-V measurements on Schottky diodes is that, no matter how large a reverse voltage is applied, providing that the leakage current is not exceeding the limit for saturation, only the material is sampled. This simplifies the results analysis, as compared with C-V on \(p-n\) junctions, where the space charge region is spreading within both materials.

The values obtained for the barrier height represent the band bending at the metal-semiconductor interface and at least for the GaN-Ni diode are in agreement with the value obtained from logarithmic I-V characteristics in the forward regime.

### 5.2.7 DLTS analysis – Results

DLTS measurements were performed in a similar manner as described in Chapter 4. To determine the activation energy and estimate the capture cross section, same reverse bias and filling pulse values were used with different rate windows. A reverse bias of -2V and a filling pulse of 0V with a duration of 1 msec were used with rate windows from 0.43 msec to 21.5 msec, corresponding to emission constants of \((46.5-2325) \text{ sec}^{-1}\).
The DLTS results are shown in Fig. 5.7 and Fig. 5.8 for the Arrhenius plot.

The concentration of the trap is found to be of the order of \(1.6 \times 10^{12} \text{ cm}^{-3}\). The activation energy obtained has a value of \(E_c - E_T = 0.58 \pm 0.01 \text{ eV}\) and the capture cross section is \(4.6 \times 10^{15} \text{ cm}^2\).

---

**Figure 5.7 DLTS Spectra for Gan-Ni Schottky diode**
The characteristics of the trap were investigated by varying the duration of the filling pulse. This was done using the same reverse bias voltage (-2V), same filling pulse (0V) and rate window 8.6 msec – 116 sec\(^{-1}\) (Fig.5.9).
By varying the reverse bias, the carrier concentration of the defect within the bulk can be investigated. The reverse biases used in this work with values between –1V and –3V sample bulk depth in the range (0.1–0.6)µm within the bulk as shown in Fig. 5.10. It is found that the trap concentration decreases from $1.6 \times 10^{12}$ cm$^{-3}$ to $9 \times 10^{11}$ cm$^{-3}$ further from the substrate interface to the film surface, shown in Fig. 5.11.
Figure 5.10 DLTS investigation of trap concentration within the bulk

Figure 5.11 Trap concentration as a function of distance from the substrate interface
5.2.8 DLTS analysis – Discussion

The B defect investigated in this work is one of the most common defect associated with GaN material grown by MOCVD, and is believed to be related to $N_{Ga}$ formed along dislocation lines [34].

From DLTS peaks, the concentration of the B defect is calculated to be $2.2 \times 10^{12}$ cm$^{-3}$, which is two orders of magnitude smaller than the first report [78]. This can be interpreted to be an improvement in recent years in the growth of GaN material as compared with 6-7 years ago. As a consequence of growth improvement, the dislocation density in MOCVD GaN has dropped from $10^{11}$ cm$^{-2}$ to $10^{6}$ cm$^{-2}$. If the B defect is associated with dislocation in the film, than a decrease in its concentration should be expected.

The values obtained for the activation energy (uncorrected for the temperature dependence of the capture cross section), 0.59eV, is in the range found by other groups 0.49-0.62 eV [101]. The capture cross section value obtained from Arrhenius analysis has a value of $\sigma = 4.6 \times 10^{-15}$ cm$^2$, is on the same order of magnitude ($\sigma = 7.4 \times 10^{-15}$ cm$^2$) as that obtained for metalorganic vapor-phase grown GaN [79].

The filling time is an important parameter in correctly estimate the concentration of a trap. If there is a variation in the trap concentration as the filling time is increased, it can be inferred that the trap has a specific behavior, such as time-dependent Coulomb barrier that limits the electron capture for traps distributed along line defects in the crystal, i.e. dislocation lines [69]. Several studies confirmed that some defects found in
GaN samples do exhibit such a behavior [70][102]. However, no reports regarding the B defects suggest such a time-dependence, a result that is also obtained in this work.

The fact that the filling of trap B is independent of time suggests that the potential barrier associated with this defect is independent of the number of electrons trapped at it, or rather that the number of electrons trapped at the defect does not change in time. Mattila et al..l [103] has showed that the N$_{Ga}$ creates several stable charge states below the conduction band, having different electron occupation numbers and of whose energies depend upon the position of the Fermi level. This would explain the stability of the B defect and also the difference in the activation energy obtained in this study.

The depth profile for the trap concentration has been found to roughly double as the sampled region gets closer to the sapphire substrate. The fact that the trap concentration increases with depth is easily understood assuming a correlation of B defect with dislocation present in the film, as pointed out earlier. Closer to the buffer layer, where the density of dislocation is greatest, the concentration of traps should reach a maximum and saturate, while moving further away from the buffer layer, the concentration should decrease as a result of reduced number of defects.
5.3 MBE GaN

MBE GaN grown by Dr. Smith’s group has been investigated for DLTS analysis. Two pieces from distinct regions on the sample, characterized by different thickness, have been cut from the initial wafer.

After cleaning using the recipe described in the MOCVD GaN section, the usual Ni and Ti metals have been deposited in order to fabricate the Schottky and ohmic contacts. I-V characteristics for the structures thus obtained are presented in Fig.5.12.

It can be seen that the junctions formed are characterized by non-rectifying contacts with high leakage currents at relatively low voltages. Other metals, such as Au and Pd have been also used to investigate the formation of a rectifying contact with similar results as those obtained above. Also, different region on the sample, corresponding to different film thickness have been probed for contacts, as shown in Fig. 5.13.
Figure 5.12: I-V characteristics for MBE GaN.
The shown I-V characteristics correspond more to poor ohmic contacts. The relatively large reverse current even at low voltages (90\mu A at 0.7V) was an impediment in pursuing the samples analysis using C-V technique. This is probably a consequence of high level of doping due to, most probably, incorporation of oxygen during growth or possibly a non-stoichiometric sample. If the doping concentration is too high, tunneling of free carrier will occur and the structure will not have a rectifying characteristic, but rather the current will depend upon the applied voltage, resembling more with accumulation (i.e. ohmic) contact.

In order to confirm the hypothesis of high level of oxygen, a band gap measurement and analysis would be necessary. The presence of oxygen would shift the band gap absorption characteristics to higher values.
5.4 Rf-sputtered GaN

One of the goals of this work was to be able to investigate the existence of deep levels in rf-sputtered GaN, and, if any found, its dependence upon the growth parameters, especially substrate temperature.
5.4.1 Preparation of samples

A first step was to grow the samples. They were grown in a chamber with a base pressure of $1 \times 10^{-7}$ Torr. The growth pressure, $6 \times 10^{-2}$ Torr, was obtained using N$_2$ gas. A ceramic heater was used to heat up the sapphire substrates. All samples had a buffer layer of GaN grown at 200 ºC for approximately 10 min. The films were grown at different temperatures, ranging from 900º C to 300º C. The rf-power used was 180 W. The growth duration was between 3h - 4h 30 min resulting in films with thickness of (5000 –8000) Å as obtained from IR measurements (see Ref.[93] for details on the measurements).

5.4.2 Characterization of samples

After cooling the samples were taken out of chamber and x-ray characterized. X-ray data are shown in Fig. 5. 14 for sample grown at 900º C, 600º C, 400º C, and 300ºC.

The main feature for all samples is the (0002) main peak of GaN. However, for the sample grown at 300º C, there are two additional peaks that I could not label. They do not belong to Ga, Ga$_2$O$_3$, or GaO$_2$. From the x-ray data, using a program that I have written (it uses the relationships between Miller indices, lattice constants and 2θ diffraction peak) the out-of plane lattice constants (assuming a=3.4 Å) has a value of c=5.15 Å.
Rocking curves, from which one can extract the grain size are displayed in Fig. 5.15.

Using Scherrer formula to compute the grain size \( t = \frac{0.9\lambda}{b\cos\theta_d} \) ( \( b \) is the width at half maximum divided by 2 in radians, \( \lambda=1.514\text{Å} \)), the size of the grains for these samples was found to be in the range (700-14000) Å. The grains for these samples are 5 orders of magnitude smaller than the MOCVD one.
Optical measurements were done for all samples in order to measure the band gap. The band gap measured from absorption data was between (3.4-3.8)± 0.1 eV. As compared with theoretical value (3.50 eV), the bandgap for some samples is higher by 0.1-0.5 eV. This could be related to incorporation of oxygen during growth.

Hall measurements indicate that the free carrier concentration for these films is in the range (8x10^{13} – 7x10^{15}) cm^{-3} with no consistent relation to the temperature of the substrate during growth.
5.4.3 Contact preparation and I-V results

The samples were cleaned before placing the contacts. The metals used for contact fabrication have been deposited using same system as described in Section 5.2. The following combinations for ohmic and Schottky contacts have been used:

<table>
<thead>
<tr>
<th>Ohmic contact (5x4)mm stripe</th>
<th>Schottky contact 0.5 mm radius</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ti</td>
<td>Ni</td>
</tr>
<tr>
<td>Ti</td>
<td>Au</td>
</tr>
<tr>
<td>Ni</td>
<td>Ti</td>
</tr>
<tr>
<td>Ti</td>
<td>Pd</td>
</tr>
</tbody>
</table>

Table 5.1 Metals used for contact fabrication to rf-sputtered GaN

The I-V characteristics for all combinations and all samples except the ones grown at 900° C show only ohmic behavior. However, the sample grown at 900° C, using Ni for Schottky and Ti for ohmic contacts, shows a rectifying behavior, as seen in Fig.5.16. However, most of the “junctions” fabricated from this samples do not sustain the rectifying behavior, in the sense that after repeatedly applying voltage, the samples loose the rectifying behavior and becomes ohmic. This could be due to the relative small size of the crystal grains, low angle boundaries and diffusion of the metal in the sample which changes as voltage is applied.
Several “junctions” fabricated from the sample grown at 900º C did not degrade after repeated voltage application and since the leakage currents were less than 100µm at -3V, they were used for C-V characterization.
5.4.4 C-V measurements- Results and Discussion

C-V measurements were done in the same way as described in previous chapters. During the measurements I have noticed that after several sets of measurements, the characteristics were changing, as shown in Fig. 5.16. Using the very first measurements, a free carrier concentration and built-in voltage were extracted. The values are $N_D = 9.4 \times 10^{13} \text{ cm}^{-3}$, and $V_b = 3.6 \text{V}$. After repeated measurements, the capacitance changed and almost lost the $C^2$ vs. $V$ behavior, as seen in Fig. 5.17.

The explanation for this behavior could be correlated to the same factors as for the I-V case. The fact that after several measurements the samples were losing the rectifying behavior made them unsuitable for DLTS analysis.
Figure 5.17 C-V characteristics for sputtered GaN. After repeated voltage application the C-V characteristic changes.

\[ N_d = 9.4 \times 10^{13} \text{ cm}^{-3} \]

\[ \text{Built-in voltage is 3.6 V} \]
5.4 Conclusions

To conclude, the existence of trap B in MOCVD GaN has been investigated. The results suggest that the activation energy is 0.59 eV from the bottom of the conduction band. The concentration of this trap decreases moving away from the buffer layer toward the top of the film.

MBE and rf-sputtered GaN were also investigated. However, the samples that were available proved to be unsuitable for DLTS analysis. The measurements that were done on these samples were discussed as well as probable causes for not obtaining a Schottky barrier.
Chapter 6

DLTS for ScN

6.1 Introduction

In this chapter, some of the properties of ScN will be reviewed in order to provide a background for the C-V and DLTS analysis. After a short introduction, a discussion of results on contacts (ohmic, Schottky) and junction barrier formation and performance will be followed by results and discussion regarding the DLTS analysis.

Transition-metal nitrides are well known for their remarkable physical properties including high hardness and mechanical strength, chemical inertness, and electrical resistivity that vary from metallic to semiconducting. As a result, they are widely studied and have become technologically important for applications such as hard wear-resistant coatings, diffusion barriers, and optical coatings. While TiN has received by far the most attention and is presently used commercially in all of the above applications, the neighboring nitride on the periodic table, ScN, was very little explored [104] and only in recent years has seen an increased interest.
ScN is a III-V material that crystallizes in cubic form (rock-salt structure) [93] and is a good lattice match for the IIIA nitrides such as GaN.

Optical absorption measurements indicate a direct bandgap at about 2.2 eV [105][106][107], in agreement with recent theoretical calculations, which predict also an indirect gap of 0.9eV in the Γ-X point of symmetry [108]. The much smaller band gap, compared with GaN and SiC, might be a great advantage in obtaining heterostructures and devices of whose performances depend upon band gap differences.

Other known properties for ScN are summarized in Table 6.1.

<table>
<thead>
<tr>
<th>Property</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Band Gap</td>
<td>Indirect gap at 0.9eV [108]</td>
</tr>
<tr>
<td></td>
<td>Direct gap at 2.2eV [105]</td>
</tr>
<tr>
<td>Crystal structure</td>
<td>Rock-salt (fcc) a = 4.48Å, predominantly (111) orientation [93]</td>
</tr>
<tr>
<td>Dielectric constant</td>
<td>4.4 [108]</td>
</tr>
<tr>
<td>Heat capacity</td>
<td>Cp=11.60+1.23<em>10^-5T-2.08</em>10^-5T^-2</td>
</tr>
<tr>
<td>Thermal conductivity</td>
<td>27W/cm-deg for ScN_{0.98}</td>
</tr>
<tr>
<td>Melting point</td>
<td>2400 ± °C</td>
</tr>
</tbody>
</table>

Table 6.1 List of some of the known ScN properties

To be able to investigate the commercial applications of a new material, one important step is to research the best way to make contacts to it. From this point of view, research results are very scarce, our group being the only one that has obtained
results regarding contact formation. Analysis of the characteristics of different metallic contacts with ScN as well as investigation of homo- and hetero-junction formation and properties are published in several articles [109][110].

6.2 Preparation of samples

The samples used in this study were mainly grown by Plasma Assisted Physical Vapor Deposition (PAPVD), but samples grown by rf-sputtering were investigated as well. Details regarding the growth, x-ray, band gap, and Hall effect measurements can be found in Ref. [93]. To proceed with contact formation, the samples were cleaned using procedures described in Ref.[109].

6.3 Ohmic contacts to ScN

Several metals have been used to form metallic contacts to ScN. Details regarding the method of deposition can be found in Ref [109].

The specific contact resistance values obtained for the investigated materials show that the optimum ohmic contact for PAPVD samples is formed by depositing Pd (9.0 \( E+01 \ \Omega \text{cm}^2 \)). All other metals tried form ohmic contacts with specific contact resistance values in the range of 2.3-5.6 \( E+06 \ \Omega \text{cm}^2 \).
For the samples grown by rf-sputtering, it was found that the quality of the ohmic contacts, judged from the specific contact resistance, depends upon the growth temperature (for example, films grown at 300º C substrate temperature, have a polycrystalline structure, with the structure being improved for films grown at 1000º C). Pd contacts to rf-sputtered samples grown at 1000º C have specific contact resistance of 1.6 $E+02 \ \Omega \text{cm}^2$, while the values obtained for other materials are higher. The difference between the contacts on the two sets of sputtered samples could be related to an improved crystal structure as X-ray data suggest. The formation of a thin layer of oxide at the surface of ScN, combined with the fact that the values obtained in this work are for non-annealed contacts, could explain the difference in the specific contact resistance of 8-12 orders of magnitude higher than values found for other nitrides [65].

The data obtained show that none of the metals tried formed rectifying contacts with ScN. One explanation could be that the roughness concurs in forming states at the interface of ScN/metal that provide energy levels which will increase the probability for thermionic emission across the barrier between the two structures.

### 6.4 ScN homo- and heterojunctions

One of the purposes of ScN fabrication is the investigation of its suitability for device fabrication. The most simple junction is a Schottky barrier, in the sense that one needs to have only one form of doping, either $p$- or $n$-type. However, the results from
ohmic contacts suggest that such a structure will be difficult to form and it may require additional sample processing techniques.

The next junction, if one can overcome the doping of the samples to obtain both \( n \)- and \( p \)-type material, is the homo- \( p-n \) junction. Several structures were investigated for this study by X. Bai [93] and it was found that even if ScN can be doped both \( n \)- and \( p \)-type, the \( p-n \) junction obtained were characterized by poor rectification properties with high leakage currents. For DLTS analysis is very important to have good rectification properties and low leakage currents, especially if the samples are to be heated repeatedly.

One last form of junctions, that uses the band bending at the interface between two materials with different band gap values, are heterojunctions, which comprises iso-type (the two materials brought together are having the same type of free carriers) and \( p-n \) heterojunctions. ScN-GaN iso-type heterojunctions were fabricated and structural and electrical characterization measurements were performed. The results on this study can be found in Ref.[110]. The aim of this study was to obtain junctions that could be used for DLTS analysis. However, it turned out that repeated heating of samples above 50º C results in irreversible degradation of the junctions. This degradation is usually characterized by an increase in the leakage currents at even low reverse voltages. This is the most important impediment in using a specific junction for DLTS analysis, and thus the use of ScN/GaN heterojunctions was not possible for DLTS analysis. However, one of the most important results is that such heterojunctions can be fabricated. The electrical properties of these junctions are discussed in Ref. [110].
Finally, $n$-$p$ ScN/Si heterojunctions have been fabricated from PAPVD and rf-sputtered ScN on $p$-doped Si. From Hall effect measurement for ScN samples grown in the same conditions as the ones used for the ScN/Si junctions, it was found that ScN films were $n$-type with free carrier concentration of $(1.0-5.0) \times 10^{15} \text{ cm}^{-3}$. The Si substrates were purchased from a commercial vendor, and were $p$-type doped with boron, with a free carrier concentration of $2.0 \times 10^{18} \text{ cm}^{-3}$. The difference in the doping level of almost 3 orders of magnitude simplifies the DLTS analysis in that the space charge region will mostly spread into the ScN side. The ohmic contacts were fabricated using Pd for ScN and Al for Si.

Several heterojunctions have been fabricated from rf-sputtered (substrate temperature during growth was $300^\circ$ C) ScN on p-Si as well. Since for rf-sputtered samples, the results from Hall effect are not very reliable [93], no value for the free concentration of carriers in the ScN was available. The only way to estimate the free carrier concentration in these films was to perform C-V measurements. The ohmic contacts for this sample were provided by the Au and Ni pressure pins.

The I-V and C-V properties for heterojunctions made out of PAPVD and rf-sputtered will be described in the following sections.
6.5 I-V results for ScN/Si heterojunctions

The I-V characteristics for all samples were performed at 300\degree C and are displayed in Fig.6.1 for PAPVD ScN/Si.

Ideality factors were in the range of 3.2-3.5, which again suggests the existence of interface states, as discussed in previous sections. The turn on voltage values for these junctions were in the range of (2.6-3) V, with series resistance values of about 300 k. From logarithmic characteristics, barriers of (1.6 - 1.7) eV are calculated.

For rf-sputtered ScN/Si, the I-V characteristics for several samples are shown in Fig.6.2.
Figure 6.1 I-V direct (left) and logarithmic (right) characteristic for ScN/Si p-n junctions.
Figure 6.2 I-V direct (left) and logarithmic (right) characteristics for rf-sputtered ScN/Si p-n junctions. The data are for different samples.

No correlation between I-V and sample growth parameters can be implied from this data.
For rf-sputtered samples, the ideality factors for the heterojunctions were in the range of 2.3-7, which again suggests the existence of interface states. The turn on voltages for these junctions could not be extracted from I-V fitting data except for one of the junctions, and the value was 2.19. The series resistance values for these junctions were higher than those obtained for the PAPVD samples, and have values in the range 300-1200 k. From logarithmic characteristics, barriers of 0.85 eV, 1.73 eV and 2.04 eV are calculated.

### 6.6 I-V measurements – Discussion

The fact that all junctions fabricated from PAPVD as well as rf-sputtered samples, are characterized by ideality factors greater than 1 suggests that no matter the growth technique used, the interface roughness (due to the way the ScN grows and the lattice mismatch with Si) plays an important role in degradation of I-V properties.

The values obtained for the turn-on voltages for the PAPVD junctions are reasonable compared with p-n junctions made out of wide gap semiconductors, even if they seem to be high. For example, for a p-n GaN LED, the turn on voltage, which is not necessarily the voltage at which the diode begins to emit, is roughly 3V, from measurements performed in our lab. This applies as well to some of the rf-sputtered junctions. However, there were junctions fabricated from rf-sputtered ScN that did not show a strong rectifying behavior. This, together with sometimes less current being
drawn through the junctions can be correlated with oxides present in the samples, either at the interface with Si or on the surface of the films.

The series resistance values are rather high for all junctions, but the result is not a surprise since the ohmic contacts formed on ScN are all characterized by high values for specific contact resistance, which will be the dominant resistance for any junction that uses ohmic contacts.

The fact that the leakage currents were reasonable small and that after repeated heating the diodes still retained this characteristic, made the subsequent C-V and DLTS analysis to be possible.

6.7 C-V results and discussion for ScN/Si heterojunctions

6.7.1 C-V for PAPVD ScN/Si junctions

From C-V measurements, displayed in Fig. 6.3 for PAPVD samples, the carrier concentration for ScN was calculated to be $2.0 \times 10^{15} \text{ cm}^{-3}$, with built-in voltages of 3.5 eV and 0.40 eV, seen by electrons and holes, respectively.
Figure 6.3 C-V characteristic for ScN/Si p-n junction. The free carrier concentration and the built-in voltage are extracted from the right graph.
The free carrier concentration obtained for ScN is in very good agreement with Hall results for PAPVD samples, which confirms once more the suitability of C-V measurements, and also proves that ideally, two or more techniques that measure the same quantities but using different principles, should be used.

The built-in voltage value is different than the value obtained for the barrier from I-V measurement. The difference could come from the pining of the Fermi level at the interface between the materials.

Assuming an effective electron mass equal to the electron mass $9.1 \times 10^{-31}$ Kg, the Fermi level can be calculated using Boltzmann approximation

$$ E_F = k_B T \ln \left( \frac{n}{N_C} \right) $$

In this approximation, the Fermi level will be placed at 0.24 eV below the conduction band. In order to be able to estimate the barrier and the band bending of the conduction band in ScN, as seen in Fig. 6.4, one needs to know the electron affinity value for ScN. This value is not yet calculated or measured; therefore, the band bending can only be approximated to be $\Delta E_C + \Delta E_V = E_{g_{ScN}} - E_{g_{Si}} = 2.2 - 1.11 = 1.09$ eV.
Figure 6.4 Tentative band diagram of ScN/Si heterojunctions left side corresponds to ScN, right side to Si

Depth concentration for the free carriers within the bulk of the sample is roughly unchanged.

### 6.7.2 C-V for rf-sputtered junctions

For the rf-sputtered ScN/Si junctions, a typical C-V characteristic is displayed in Fig. 7.5. The carrier concentration for the rf-sputtered samples was calculated to be $1.9 \times 10^{14}$ cm$^{-3}$, with a built-in voltage seen by electrons of more than 34 eV. The value for the carrier concentration is smaller than for PAPVD junctions, while the very high intercept for the built-in voltage suggests that an oxide is present. This is further
supported if one does a simple calculation, assuming a depletion width of approximately 0.2µm (roughly half of the sample thickness), one obtains for the junction capacitance a value of approximately 38 pF, which is two orders of magnitude larger than the measured value.

A profiling of the free carriers in the bulk is possible only for the region of the C-V were there is a change in the slope of the $1/C^2$ s. V. However, if one uses the capacitance value obtained, one finds that the depth sampled is greater than the total thickness of the sample. This again suggests that the values measured are not true values of the junction capacitance.
Figure 6.5 C-V characteristic for rf-sputtered ScN/Si heterojunctions. The built-in voltage has a high value for this junctions due to, most probably, the presence of oxides in the sample or at the contact interface.
6.8 DLTS results

DLTS analysis has been performed on PAPVD samples that had good I-V and C-V characteristics. Also a tentative DLTS analysis has been done on the rf-sputtered ones.

The analysis was done following the steps below (as explained in previous chapters), namely:

1. same reverse bias and filling pulse values, but different rate windows, to determine the activation energy and estimate the capture cross section;

2. same reverse bias, filling pulse and rate window but different duration for the filling pulse to investigate any dependence of the trap on the width of the pulse;

3. same filling pulse and rate window but different reverse biases to investigate the distribution of the defects with the depth in the bulk.

The first step is finding the defects in the material. This task is most often difficult if no information is available on a possible energy range. In this case, one can only take wide temperature scans using rate windows that span decades, at the same time using different voltage values for both the filling and the reverse biases. If the experimental apparatus prevents the use of a wide range of temperature scans, i.e. one is limited to only high temperatures such is the case of this study, even if no defect is found, it does not mean that there is none, either defects are deeper in the bandgap, in which case one needs to heat the diode at higher temperatures, or it needs to cool the
sample at temperatures most often below liquid nitrogen. However, if the rate window set-up allows a wide range of selection, for example from 0.001 msec to 1000 msec, it might be possible to see the signature of both a deeper and more shallow defect.

6.8.1 DLTS results for PAPVD ScN/Si junctions

For this type of samples, I have started with a regular –3V reverse bias and the usual filling bias of +0V. The duration of the filling pulse was chosen to be 1msec. Out of the available rate windows, only five were accessible, in the sense that the DLTS peak could be recorded in the available temperature range. DLTS scans are presented in Fig. 6.6.
Figure 6.6 DLTS signal for different rate windows

Figure 6.7 Arrhenius plot and analysis for ScN
Due to the fact that the junctions are highly asymmetric, i.e. the Si side is heavily doped as compared to the ScN side, and that the peak seen in DLTS corresponds to majority emission from a trap, one can conclude that this defect is actually an electron trap in the ScN material, with an energetic level below the conduction band of ScN. From the Arrhenius analysis (Fig. 6.7), a value of 0.5 eV was extracted as the activation energy for the trap, which places the level at $E_c - E_T = 0.50 \pm 0.03$ eV. The error associated with this analysis is in the same range as that estimated for all other results that I have obtained, and is mainly due to how precise one can pinpoint the location of the DLTS maximum temperature. The analysis may be flawed by erroneous assuming that the level has a temperature independent capture cross section and an electric field-independent behavior.

To investigate if the level has a field dependence upon the environmental electric fields present in the space charge region, one usually keeps the reverse and filling voltages at the same value and uses the same rate window but different durations of the filling pulse. This analysis is shown for this defect in Fig. 6.8. The parameters used were $V_r = -2V$, $V_p = +0V$, and the rate window was 0.86 msec. The duration of the filling pulse was varied from 5 msec to 100 msec.
Finally, keeping the filling pulse bias and duration and the rate window at the same values and varying the reverse bias in such a way as to sample the bulk of the ScN, one can profile the trap concentration. The sequence of voltages used and the DLTS results are shown in Fig. 6.9.

This analysis, for the ScN sample investigates, is presented in Fig. 6.10.

The depth sampled with the chosen reverse bias values was between 0.2µm and 0.55 µm from the ScN/Si interface.
Figure 6.9 DLTS profiling for trap concentration

Figure 6.10 Trap concentration in the bulk of ScN
6.8.2 DLTS results for rf-sputtered ScN/Si junctions

In a similar way as for PAPVD samples, DLTS analysis was performed on the rf-sputtered ScN/Si junctions. Choosing a suitable voltage of $V_r = -2V$ and a duration of the filling pulse of 1 msec, was found that closer to the interface between ScN and Si, there is at least one electron trap, as seen in Fig. 6.11, the positive peak. A negative peak is visible as well.
Because the capacitance measured is not a true value of the junction-capacitance, than not even an approximate value for the concentration of the defects was possible to extract.

An Arrhenius analysis (Fig. 6.12) was difficult to perform and only a very approximate number was extracted for the activation energy of 0.91 eV below the conduction band.

Figure 6.12 Arrhenius plot for rf-sputtered ScN/Si
6.9 DLTS - discussion of results

6.9.1 Results for PAPVD junctions

From Arrhenius analysis a defect that is situated below the conduction band at approximately 0.5eV has been found for the PAPVD ScN/Si heterojunctions. Given the fact that this deep level has a signature that does not depend upon the duration of the filling pulse implies several things. One of them is that the capture cross section has a temperature independent behavior or an exponential dependence. This could be proved only by further analysis, by looking directly at the capacitance transient and using fitting procedures that take into account the temperature dependence of the capture cross section. This can be done using a digital oscilloscope or expensive computer hardware and software. Nevertheless, even if these would be available, the analysis still requires knowledge of the electron effective mass, which is not available as of now. Therefore, the value obtained for the activation energy might not be very accurate due to the absence, so far, of the electron effective mass. However, the fact that the DLTS peak does not change in intensity with the duration of the filling pulse is in favor of the assumption that the defect has a temperature independent capture cross section.

To reduce the error in estimating the value of the activation energy, one needs more data points for the Arrhenius analysis. This can be usually accomplished by a larger temperature scan that the one in this study. Due to limitation in the apparatus and
also because of diode degradation due to repeated heating, only a range of about 200 degrees has been investigated, which resulted in only five data points.

A trap concentration profiling shows that this defect has a higher concentration near the interface with Si. This could be understood if the defect is associated with the existence of structural defects, such as dislocation lines, a consequence of the mismatch between the two materials of about 10%. Keeping in mind that the mismatch of about 14% between GaN and sapphire leads to dislocation lines concentration of about $10^6-10^8$ cm$^2$ in good films, than the conclusion for ScN/Si is that the density of structural defects can be very high at the interface between the two materials as well. A transmission electron microscopy investigation of the cross section might give an insight into this problem. Important is that once the films become thicker, moving away from the Si interface, this defect appears in a smaller number. One future study could be concerned only with growing thicker films and see if this defect is always present. Of course, this defect might have an intrinsic nature and could be associated with either interstitials, vacancies or even antisites, and still have a dependence upon the structural environment, as was the case for the discussed EL2 defect in GaAs, which, even if associated with a arsenic interstitial complex, nevertheless has a dislocation line density dependence (see Chapter 4).
6.9.2 Results for rf-sputtered ScN/Si heterojunctions

The results obtained for the rf-sputtered junction show that an electron trap might be present in the structure with an activation energy of 0.91eV below the conduction band. As pointed out repeatedly, the value for the activation energy is prone to a number of errors and is only an approximation. Again, the available temperature range limits the number of data points that can be extracted for Arrhenius analysis to five. The fact that the activation energy is much higher than the value obtained for the PAPVD samples suggests that this could be related to a defect having a different nature. This is not a surprise since it is known that different growth techniques promote different defects in the material.

The negative peak could come from injection of holes and could represent the change in the space charge region as a consequence of injection of minority carriers, or could as well be a hole trap in the material. The first assumption is further supported by noticing that the minimum occurs at roughly the same temperature, an indication that the signature is not associated with any hole trap, but rather with injection of minority carriers in the space charge region. This phenomenon is often seen in low quality diodes and is associated with tunneling through interface states close to the valence band due to the band bending [64].
6.10 Conclusions

To conclude, ScN/Si p-n heterojunctions have been fabricated. DLTS analysis shows that an electron trap with activation energy of 0.51 eV is present in PAPVD material, and that this trap has a higher concentration closer to the Si interface, due to, probably, existence of a high number of structural defects. For rf-sputtered ScN/Si junction, an electron trap is present with an energy $E_C - E_T = 0.91$ eV. It has been shown that the quality of the junction influences the DLTS results and sometimes signatures that are not related to traps but rather injection of carriers in the space-charge region are present.

Improvements in the as-grown material as well as theoretical calculations are necessary in order to make assumptions about the nature the defects.
Chapter 7

Temperature Evolution of Deep Levels in $n$ and $p$-type SiC

7.1 Introduction

Silicon carbide (SiC) based semiconductor electronic devices and circuits are presently being developed for use in high-temperature, high-power, and/or high-radiation conditions under which conventional semiconductors cannot adequately perform. Silicon carbide's ability to function under such extreme conditions is expected to enable significant improvements to a variety of applications and systems. These range from greatly improved high-voltage switching [111-113] or energy savings in public electric power distribution and electric vehicles to more powerful microwave electronics for radar and communications [114].

Silicon carbide crystallizes in many polypitic forms (more than 200), of which 4H- and 6H-SiC electronic devices presently exhibit the most promise due to the
availability and quality of reproducible single-crystal wafers in these polytypes. The size of commercially available 4H- and 6H-SiC wafers has recently been increased to 2 inches in diameter, and are mostly commercialized by CREE Corp.

Its optical, electrical, mechanical and thermal properties make SiC an interesting material for a wide range of applications. SiC has a substantial advantage over many other binary compounds in that it can be oxidized to form a stable layer of insulating SiO$_2$ on its surface. The main disadvantage is its indirect band gap.

The cubic form of SiC ($\beta$-SiC), denoted 3C-SiC has a lattice constant of 4.3 Å at 300K and indirect gap of 2.416eV at 2K, while the hexagonal polytype denoted 2H-SiC (wurtzite-type crystal) has lattice constants a= 3.0 Å and c= 15.1 Å and indirect gap for 6H-SiC of 2.86eV at 300K;

The polytypes of interest in this study are the hexagonal 4H- and 6H- SiC.

7.2 Motivation of the study

SiC has a very low diffusion coefficient of the impurities, and almost the only way to dope it would be by ion implantation. The problem is that even if high temperature post-implantation is done to the samples, there is radiation damage left which introduces electrically active defects. For example, Al implantation in 6H-SiC introduces both deep acceptor ($E_T = E_V + 0.26eV$) and donor ($E_T = E_C - 0.44eV$) states in the bandgap [115], with, as seen by one group, at least six different Al levels [116].
Nitrogen is known to reside at the C lattice site with published activation energies in the range 0.08-0.150 eV [117]. Other deep levels detected in n- and p-type structures are having energies of $E_C-E_T = 0.38\,\text{eV}$ and $E_T = E_V + 1.1 \,\text{eV}$ [118-120].

Independent of the polytype, B residing at a Si lattice site forms a deep level at approximately $E_V + 0.30 \,\text{eV}$, while a complex of one B atom at a C site and a neighboring intrinsic defect such as a Si vacancy $V_{Si}$, or carbon vacancy $V_C$, forms a deep level (“D” defect) at approximately $E_C - (0.65 \pm 0.10) \,\text{eV}$ that acts as a donor (concentration of $7 \times 10^{14} - 3 \times 10^{15} \,\text{cm}^{-3}$) [121][122]. Recently it has been found that this center acts as an acceptor and degrades device performances. An important characteristic of this center is that its concentration depends upon the C:Si ratio during growth. A review of growth condition and results obtained for this center can be found in Ref.[121].

Oxygen in 4H-SiC form deep levels at (0.88-0.94) eV and (0.70-0.79) eV were measured [123].

Other impurities such as vanadium form deep levels at 0.35eV, 0.7eV and near midgap in 4H- and 6H-SiC [124].

Numerous groups have investigated defects in SiC with results slightly varying depending upon the sample preparation and conditions. The most important defects for 6H-SiC are found at $E_C-0.32 \,\text{eV}$, $E_C-0.49 \,\text{eV}$, $E_C-0.50 \,\text{eV}$, and $E_C-0.15 \,\text{eV}$ for 4H-SiC [125]. Similar results are obtained for vapor phase epitaxy (VPE) grown samples as well, suggesting that these defects have an intrinsic nature [126].
Radiation induced defects have been extensively studied, with one study reporting an impressive number (11) of defects, in the region (0.18 - 1.34) eV for 6H-SiC irradiated with electrons having energies of 5MeV [127].

It is therefore important to investigate the annealing influences upon the electrically active defects, especially since new defects might be formed or existing ones might be annealed out.

The samples in this study have been doped during growth, this being an approach to the implantation process. However, even if the dopants are incorporated during the growth, there might be defects formed in the material that are related to the doping process, and it would be interesting to investigated the existence of deep defects and their annealing temperature dependence.

### 7.3 Preparation of diodes

The material used in this study has been acquired from CREE Research Inc and the provided information is summarized in Table 7.1.
Both the $n$- and $p$-type material has been cleaned in HF: deionized water, 1:2, for 5 min, then rinsed in deionized water and dried in inert gas. Immediately after the cleaning process, the samples have been placed in the deposition chamber for Schottky metal dc-sputtering or evaporation. The deposition of the metals has been done using the same equipment as described in Chapter GaAs and GaN.

Details for the fabrication of the two types of Schottky barriers are presented in Table 7.2.

In order to investigate the relationship between defects in the material as a function of annealing temperatures, the samples used in this study have been annealed in air for 30 min at several temperatures. After annealing, all samples have been cleaned as described above and placed in the vacuum chamber for contact deposition.

<table>
<thead>
<tr>
<th>n-type material</th>
<th>p-type material</th>
</tr>
</thead>
<tbody>
<tr>
<td>4H SiC</td>
<td>6H SiC</td>
</tr>
<tr>
<td>$N$ doping $n=8.9\times10^{17}$ cm$^{-3}$ (during growth)</td>
<td>$Al$ doping $p=3.6\times10^{18}$ cm$^{-3}$ (during growth)</td>
</tr>
<tr>
<td>Thickness 400 µm</td>
<td>Thickness 390µm</td>
</tr>
</tbody>
</table>

Table 7.1 Description of SiC samples used in this study
<table>
<thead>
<tr>
<th>n-type Schottky diode</th>
<th>p-type Schottky diode</th>
</tr>
</thead>
<tbody>
<tr>
<td>dc- sputtered 1000 Å Ni Schottky circular dots, 0.5mm diameter</td>
<td>2000Å Al 0.5 mm diameter circular dots, evaporated</td>
</tr>
<tr>
<td>Al evaporated on the back side, large area to form the ohmic contact, with thickness of approximately 1µm</td>
<td>Al evaporated on the back side, large area to form the ohmic contact, 1µm thick</td>
</tr>
</tbody>
</table>

Table 7.2 Description of the junctions fabricated from SiC for this study

| n-type SiC-Ni samples were annealed at 400° C, 700° C and 900° C | p-type SiC-Al samples were annealed at 400° C, 600° C, and 800° C |

Table 7.3 Description of samples used in the study

### 7.4 I-V characterization – Results

I-V analysis was done at room temperature for all samples. In general, each sample has several contacts (dots), in average a number of 16. Each dot is analyzed and the best is used as the junction for further analysis.

The results for I-V characterization for n-type and p-type samples are presented in Table 7.4 and Table 7.5.
<table>
<thead>
<tr>
<th></th>
<th>As-grown</th>
<th>400 °C</th>
<th>700 °C</th>
<th>900° C</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Leakage current at –5V</strong> (A/cm²)</td>
<td>0.5x10⁻⁶</td>
<td>3.5x10⁻⁴</td>
<td>3.5x10⁻³</td>
<td>3.5x10⁻⁶</td>
</tr>
<tr>
<td><strong>Forward current at +5V</strong> (A)</td>
<td>2.5x10⁻⁵</td>
<td>2.0x10⁻⁵</td>
<td>3.0x10⁻³</td>
<td>1.0x10⁻⁴</td>
</tr>
<tr>
<td><strong>Ideality factor</strong></td>
<td>3.3</td>
<td>3.0</td>
<td>2.5</td>
<td>1.7</td>
</tr>
<tr>
<td><strong>Turn-on voltage</strong></td>
<td>1.8</td>
<td>1.8</td>
<td>1.7</td>
<td>2.2</td>
</tr>
<tr>
<td><strong>Barrier</strong> (kΩ)</td>
<td>2.4</td>
<td>2.3</td>
<td>1.6</td>
<td>1.1</td>
</tr>
<tr>
<td><strong>Series resistance</strong> (kΩ)</td>
<td>8-10</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 7.4 I-V results for n-type SiC-Ni Schottky junction
<table>
<thead>
<tr>
<th>p-type SiC-Al</th>
<th>As-grown</th>
<th>400 °C</th>
<th>600 °C</th>
<th>800° C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Leakage current at –5V (A/cm²)</td>
<td>1.0x10⁻⁷</td>
<td>1.0x10⁻⁶</td>
<td>0.5x10⁻⁶</td>
<td>2.0x10⁻⁸</td>
</tr>
<tr>
<td>Forward current at +5V (A)</td>
<td>2.5x10⁻⁵</td>
<td>1.5x10⁻⁵</td>
<td>4.7x10⁻⁴</td>
<td>7.8x10⁻³</td>
</tr>
<tr>
<td>Ideality factor</td>
<td>4.0</td>
<td>4.0</td>
<td>3.5</td>
<td>3.2</td>
</tr>
<tr>
<td>Turn-on voltage</td>
<td>3.7</td>
<td>3.7</td>
<td>3.3</td>
<td>3.1</td>
</tr>
<tr>
<td>Barrier</td>
<td>3.7</td>
<td>3.7</td>
<td>3.4</td>
<td>2.7</td>
</tr>
<tr>
<td>Series resistance (kΩ)</td>
<td>2-5</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 7.5 I-V results for p-type SiC-Al Schottky junction

A comparison of the I-V characteristics for both types of junctions is shown in Fig. 7.1. Figure 7.2 shows the direct and logarithmic characteristics for junctions on n-type material used to obtain the ideality factors, turn-on voltages, barriers, and series resistance. Similar analysis has been performed on p-type samples as well.

The series resistance for the junctions has been obtained from square least fit of the slope of plots of 1/I vs. IdV/dI, as shown in Fig.7.3.
Figure 7.1 I-V characteristics for junctions on n-type (left) and p-type (right) substrates for the annealing temperatures used in the study.
Figure 7.2 Direct (left) and logarithmic (right) I-V characteristics for samples obtained from n-type material. An improvement in the direct current can be seen only after annealing the junction at 900°C.
7.5 I-V Characteristics – Discussion

Schottky barriers on both 4H-Sic and 6H-Sic have been under extensive studies since 1964, mostly on high voltage break-down junctions. An extensive review of contacts on SiC can be found in Ref.[128].
7.5.1 Discussion of currents, turn-on voltages and series resistance

From Tables 7.4 and 7.5 one can see that in terms of leakage currents the samples from the $p$-type material are better by at least one order of magnitude. This could be explained in terms of the barrier formed between the Al and SiC which is higher than Ni and SiC, but within values obtained by other groups [128]. The values for the turn-on voltages are also similar with results from other groups [128]. There is a slight variation with temperature of the turn-on voltage but not significant as to be a definite trend. For the samples made of $p$-type material, the turn-on voltage is higher, almost twice the values obtained for the $n$-type samples.

The values obtained for the series resistance show that in general, the series resistance is smaller for $p$-type Schottky diodes than for the $n$-type ones. Usually the condition of the surface as well as the ohmic contact preparation play an important role in setting this quantity, as was pointed out in previous chapters. For SiC, I could not find another study that discusses this quantity. By comparison with other samples fabricated for this study, the values for SiC are smaller.
7.5.2 Discussion of ideality factors and barrier heights

From I-V characteristics one can see that the extracted properties differ from \( n \)-type samples to \( p \)-type. The ideality factor of all structures improves as the annealing temperature is increased.

For sample on \( n \)-type material, the ideality factor decreases from 3.3 to 1.7 for sample annealed at 900 °C, while for \( p \)-type material it decreases from 4 to 2.7. The values for the ideality factor are in good agreement with results from other studies [129][130].

In general, for SiC is not trivial to obtain ideality factors close to unity. The process, in general, requires extensive cleaning and etching of the surface oxides. For example, an ideality factor of 1.07 was obtained after cleaning the sample in concentrated HF, etched in molten sodium peroxide, rinsed in dilute HCl and deionized water, and then dipped in methanol and dried with N2 [131]. Recent studies involve cleaning and contact deposition in ultra-high vacuum [132].

The big difference in the ideality factors for the two sets of samples could come from the fact that for the \( p \)-type sample the Schottky and ohmic contacts used are formed by evaporating Al. Al is known to easily form vapor phase oxides (\( \text{AlO} \) and \( \text{Al}_2\text{O}_3 \)) because the \( \text{O}_2 \) has a more negative free energy than \( \text{O}_2 \) bound to Si [128]. This oxide layer might contribute in reducing the ideality factor and increasing the series resistance.
The fact that the ideality factor decreases with annealing temperature has been also observed by other groups, and is well established [128]. However, all the studies observed improvements in the diode qualities by annealing after the contacts have been deposited. The fact that the diodes improve in this case as well, can be associated with a reduction in the number of growth defects, which in turn reduces the probability of tunneling currents (which have a voltage dependence and reflects in a high ideality factor) [133]. It is also known that the I-V measurements greatly depend upon the homogeneity of the interface as well, as discussed in other chapters as well [134 136].

The existence of an Al oxide at the interface between the Al and p-type SiC, together with the high difference between the work function of Al and SiC could explain the barrier values higher for samples on p-type material. In general, for p-type material, the barriers tend to be higher [128] (6H-SiC work function =4.75eV, Al work function 4.24-4.41eV).

The fact that the barrier extracted from I-V measurements depends upon the temperature at which the samples have been annealed (for both n- and p-type samples) shows a consistent trend that might come from improvements in the structure at the near surface toward recovering from the effects of contact formation.

To conclude, several Schottky barriers have been obtained from p- and n-type SiC substrates annealed at different temperatures with characteristics that depend upon the annealing temperature. The main point is that these structures all show characteristics that make them suitable for DLTS analysis.
7.6 C-V measurements - Results

7.6.1 Importance of cleaning the samples

To investigate the influence of the oxide layer upon the C-V characteristics, two samples, one that has not been cleaned and one cleaned using the recipe described above, have been used to fabricate Schottky barriers. Both samples were fabricated from n-type material, using contact deposition as described in Section 7.5.

The results for C-V analysis are shown in Fig. 7.4

From the data, the carrier concentration values are $3 \times 10^{17} \text{cm}^{-3}$ for the not-cleaned sample, and $1 \times 10^{18} \text{cm}^{-3}$ for the sample that has been cleaned in HF. The biggest difference is seen in the values obtained for the built-in voltage, 5.3 eV for not-cleaned sample and 2.0 ev for the cleaned one. From the difference in the capacitance values, using a simple model which assumes that the oxide layer forms a capacitor in series with the junction capacitance, a value of 50 nm was calculated for the oxide thickness (SiO$_2$). To conclude, it is very important to clean the sample to try to remove as much of the native oxides as possible from the sample surface.
Figure 7.4 C-V characteristics for as-grown and cleaned SiC-Ni.

An oxide layer with a thickness of approximately 50 nm is present on the surface of the sample.
7.6.2 C-V for cleaned samples

C-V characterization has been performed for all cleaned samples. For all dots formed on the samples, both I-V and C-V measurements were done.

Figure 7.5 shows C-V data and analysis for Schottky barriers made of as-grown $n$- and $p$-SiC.

A comparison of C-V analysis for p-type samples depending upon the annealing temperature is presented in Fig.7.6. Similar results were obtained for samples on n-type substrate. The free carrier concentration and built-in voltage were obtained from least square fits to the $1/C^2$ vs $V$ data, as the slope and intercept.

The results obtained from C-V results are displayed in Table 7.6.

<table>
<thead>
<tr>
<th></th>
<th>Free carriers concentration</th>
<th>Built-in potential</th>
</tr>
</thead>
<tbody>
<tr>
<td>n- type SiC-Ni</td>
<td>$5.3 \times 10^{17} - 1.4 \times 10^{18}$ cm$^{-3}$</td>
<td>2.8 eV for as grown sample</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.8 eV for all others</td>
</tr>
<tr>
<td>p-type SiC-Al</td>
<td>(1.3-1.4) $\times 10^{18}$ cm$^{-3}$</td>
<td>3.6 eV for as grown sample</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3.3 for all others</td>
</tr>
</tbody>
</table>

Table 7.6 C-V results for SiC junctions
Figure 7.5 C-V Data and analysis for Schottky barriers on n- and p-type material.
The free carrier concentration and built-in voltage are extracted from the right side of the graph.
Figure 7. C-V data and analysis for p-type samples as a function of temperature. The built-in voltage has a smaller value (3.3 eV) for samples that have been annealed as compared to the junctions obtained from as-grown sample (3.6 eV).
The free carrier distribution in these samples has been investigated to see if the doping profile can be visualized by a change in the donor/acceptor concentration within the bulk. From the analysis, it can be concluded that all samples have a uniform free carrier concentration within the region of the bulk sampled by the space charge region. Due to the high doping of the material, the spreading of the space charge region in the bulk is not very large. Only a depth of approximately 0.08\( \mu \)m from the surface has been sampled in C-V measurements.

### 7.7 C-V measurements – Discussion

From C-V analysis it can be seen that in general, the free carrier concentration, within errors, has the same value as expected from Hall effect results that were supplied with the samples. The errors are associated mainly with the software card that is used for data acquisition. The signal is read in terms of voltages, with variations within Boltzmann noise, \( \pm k_B T \), which at room temperature translates into \( \pm 25\text{mV} \). For this study, where the capacitance signal is relatively large, the fluctuations represent about 5-10\%. Other errors are introduced in the analysis by data fitting. But the most important errors are introduced in fact by the junction formation in that the junctions are, probably, not perfect vertically and that there is some lateral spreading of the contact which changes the real area of the junctions (area appears in the calculation of the carrier concentration at power 2).
The built-in voltages show a correlation with the barriers obtained from I-V results. Also, by simply annealing the junction at even 400 °C improves the built-in voltage. The values obtained are similar with those obtained by other groups [129][118].

A study that I have performed, regarding the variation of the built-in voltage with temperature for the n-type sample (as grown) showed that the built-in voltage does not change its value for temperatures between 238K and 370K. Correlating this with the fact that a change in the built-in voltage is seen only for samples annealed at temperatures of 400 C or higher might indicate a pinning of the Fermi level by a defect that is deep in the band gap, which after annealing disappears or decreases its concentration.

### 7.8 DLTS measurements-Results

#### 7.8.1 n-type SiC

DLTS analysis has been done on all samples following same procedures as described in the previous chapters. First, a trap is identified, then its signature is analyzed in terms of filling pulse width and bulk distribution. In the following, all the data shown in the graphs were done by keeping the samples at a reverse voltage of $V_r =$
-4V and filling pulse of $V_p = -0.005V$ and a duration of filling pulse of 5msec. DLTS results for as grown sample is showed in Fig.7.7

For the samples that have been annealed at more than 400º C, more than one defect has been detected, as seen in Fig. 7.8 for sample annealed at 700º C.

Activation energies and capture cross sections have been calculated assuming a temperature independent capture cross section, with an electron effective mass of
(ml*mt*mt)\(^{1/3}\) =0.72m. Very small capture cross-section values have been obtained \((10^{-16} - 20^{-17})\) cm\(^2\) for all samples. The DLTS results are displayed in Fig. 7.9 and Table 7.7, where the traps have been labeled with “N” from n-type, “E” or “H” from electron or hole trap, such as NE1 is an electronic trap in n-type material.

<table>
<thead>
<tr>
<th>Name</th>
<th>As grown</th>
<th>400º C</th>
<th>700 ºC</th>
<th>900º C</th>
</tr>
</thead>
<tbody>
<tr>
<td>NE1</td>
<td>0.33 e-trap</td>
<td>NE2</td>
<td>0.23 e-trap</td>
<td>NE3</td>
</tr>
<tr>
<td>NE2</td>
<td>0.23 e-trap</td>
<td>NE3</td>
<td>0.19 e-trap</td>
<td>NE4</td>
</tr>
<tr>
<td>NE3</td>
<td>0.19 e-trap</td>
<td>NE4</td>
<td>0.41 e-trap</td>
<td>NE6</td>
</tr>
<tr>
<td>NE4</td>
<td>NE1 (2-5)</td>
<td>NE2 (2-3)</td>
<td>NE3 (30-35)</td>
<td>NE4 20</td>
</tr>
<tr>
<td>NE5</td>
<td>20</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NE6</td>
<td>25</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 7.7 Activation energies and concentration for traps in n-type samples
Figure 7.8 DLTS signal for sample annealed at 700 C

Figure 7.9 Activation energies for defects found in $n$-type SiC
Investigation of trap concentration within the bulk and peak dependence upon the width of the filling pulse showed that the traps are uniformly distributed in the volume that has been sampled and that most probably their dependence upon the electric fields existent in the SCR is very weak.

7.8.2  \textit{p-type SiC}

For the junctions made out of \textit{p}-type material, same procedure and steps as for \textit{n}-type junctions have been followed. It has been seen that only electron traps are active in the temperature range investigated and that more than one trap is present for all samples.

For the sample annealed at 400\textdegree{}C it has been observed that beside the trap that cannot be reached, depending upon the rate window chosen, there are two traps that occur in the same range of temperatures but at very different rate windows. One trap has an activation energy of $E_C - E_T = 0.37$ eV and the other 0.21eV. Both are electronic traps.
One trap could not be investigated to find the activation energy because a temperature higher than could possible be used was necessary, as seen in Fig. 7.10 for sample annealed at 600º C.

The results for analysis on p-type samples are shown in Table 7.8 and Fig. 7.11.
Table 7.8 Activation energies and concentrations for traps in $p$-type SiC

<table>
<thead>
<tr>
<th>Name</th>
<th>Type</th>
<th>(E ± 0.02) eV</th>
<th>400°C</th>
<th>600°C</th>
<th>800°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>PE1</td>
<td></td>
<td>0.12 e-trap</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PE2</td>
<td></td>
<td>0.21 e-trap</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PE3</td>
<td></td>
<td>0.37 e-trap</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PE4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PE5</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Concentration

<table>
<thead>
<tr>
<th>Name</th>
<th>Concentration</th>
<th>Type</th>
<th>(x 10$^{15}$ cm$^{-3}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PE1</td>
<td>(0.2-0.3)</td>
<td>PE2</td>
<td>(3-4)</td>
</tr>
<tr>
<td>PE3</td>
<td>(1-3)</td>
<td>PE4</td>
<td>(0.5-0.6)</td>
</tr>
<tr>
<td>PE5</td>
<td>(1.0-1.5)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Figure 7.11 Activation energies for traps in $p$-type SiC
7.9 DLTS analysis - Discussion

7.9.1 Discussion for n-type SiC

It can be seen from Table 7.7 that if the samples are annealed some defects are promoted while others are not present anymore. However, almost all defects have been seen by other groups as well, some of them in conjunction with sample annealing.

The defect that is present in the as-grown sample, labeled NE1, has activation energy (0.33eV) close, within the experimental errors, to the defect created by residual uncompensated donor residing at a Si lattice [121] [124] and are specific to every SiC sample [127]. The fact that is annealed out after heating to 400 C indicates that either the defect has a different nature [127] or that the residual boron shifts position within the lattice after annealing. The concentration of this defect is in agreement with numbers obtained by the groups cited above.

It is known that N can occupy a C or a Si lattice, resulting in formation of defects that have in general activation energies from (0.08-0.150) eV, depending upon the crystal polytype [127], with a value of 0.24 eV found by Ikeda et al. [137]. By looking at the defects found in this study, the NE2, NE3 and NE5 have all close activation energies and similar concentrations. I conclude that they all are in fact the same defect, associated with N sitting at a C or Si lattice site.

The NE4 defect, present in the samples annealed at 700C (E_C-E_T= 0.42eV) could be related to oxygen incorporated into the sample either during growth or during
annealing [123]. The depth profiling for these samples did not exceed 800-900Å, which is fairly close to the surface; therefore oxygen might be incorporated close to the SiC surface.

In the sample annealed at 900°C, one defect at 0.50 eV (NE6) has been found. As opposed to 6H-SiC, where this defect is present for electron irradiated as well as deuterium ion implanted samples [126], no association with sample processing has been made for the 4H-SiC. I am uncertain about the nature of this defect. The fact that it is present in as high a concentration as all the others, might suggest that it is also related to intrinsic impurities and that is unstable and annealing at higher temperature might reduce this defect.

Finally, the NH1 level, which is a hole trap, located at 0.14 eV above the valence band is seen only if the sample is annealed at temperatures as high as 900°C. This defect is present in a concentration that is lower than all others, (1-3) x10^{13} cm^{-3}. I could find no reference that might give an insight into the nature of this defect for 4H-SiC. Calculations for 3C-SiC suggest that a defect with this activation energy is due to the mobile silicon antisite [138]. Since it appears only after annealing, this defect might be as well related to intrinsic point defects as the silicon antisite.
7.9.2 Discussion for p-type SiC

As opposed to 4H-SiC, for the case of 6H-SiC, a more common polytype, there are more studies regarding electrically active defects. A broad range of defects has been found, with energies ranging from 0.08-1.34 eV, either below conduction band or above valence band. These defects have been associated with Al and B, with V and other impurities [115][127][137][138].

All the defects found in this study for the 6H-SiC, even if they are p-type samples, are electron traps. Some of the defects have been detected by other groups as well. For example, the PE1 defect is close to the L1 electron trap found by Ballandovich [127]. In his study on 6H-SiC, he found eleven defects, most of which have temperature dependence. Some of them have been found in the samples used in this study.

The PE2 and PE4 defects, present in the samples annealed at 400° C and 600° C have been associated with Al incorporation induced defects and are probably the same defect. It is known that the Al acceptor site has an activation energy between (0.19-0.28) eV, depending upon the crystal environment and symmetry [118].

The PE3 and PE5 defects, are probably different defects, especially since they are active at different temperatures. I assume that they are related to some intrinsic defects that have a complicated annealing pattern. They might be related to migration of a defect from one lattice point to another with annealing temperatures, which will result in different activation energies, a result that has also been proposed by Ballandovich [127].
The defect that appears at temperatures higher than could be reached with the experimental apparatus and samples could be a defect with activation energy > 1eV below the conduction band. Such deep defects have been observed by Kobayashi et al. [125].

For all samples, the capture cross section values obtained are smaller than published values. The errors associated with this quantity could be very large since it is extracted from a logarithmic analysis; therefore I do not assume that the values that I calculate are the true values. Investigation of the temperature dependence of the capture cross section is necessary before attempt to assign values. This is usually done using sophisticated software and represents an interesting subject for further research.

7.10 Conclusions

In this study, defects in $n$-type 4H-SiC and $p$-type 6H-SiC samples have been investigated. There are numerous published results pointing out that, depending upon the method of growth, polytype and post-growth processing, different defects are present in the band gap. Some of these defects disappear if the samples are annealed, while others are created in the process.

In this study, several defects were found for each set of samples (either $n$- or $p$-type). They have activation energies and concentration in agreement with published results.
Five new defects have been found for which there is no reference as to what could be their nature. These are listed in Table 7.9, with their names, in what type of substrate they are present, the activation energy and, if applicable, their possible nature.

<table>
<thead>
<tr>
<th>Defect</th>
<th>Material</th>
<th>Activation energy</th>
<th>Nature</th>
</tr>
</thead>
<tbody>
<tr>
<td>NE4 electron type</td>
<td>4H-SiC, n-type</td>
<td>$E_C-E_T=0.41 \text{ eV}$</td>
<td>Oxygen related? [123]</td>
</tr>
<tr>
<td>NH1 hole trap</td>
<td>4H-SiC, n-type</td>
<td>$E_T-E_V=0.14 \text{ eV}$</td>
<td>Mobile Si antisite? [138]</td>
</tr>
<tr>
<td>NE6 electron trap</td>
<td>4H-SiC, n-type</td>
<td>$E_C-E_T=0.50 \text{ eV}$</td>
<td>oxygen? [126]</td>
</tr>
<tr>
<td>PE3 electron trap</td>
<td>6H-SiC, p-type</td>
<td>$E_C-E_T=0.37 \text{ eV}$</td>
<td>[127]</td>
</tr>
<tr>
<td>PE5 electron trap</td>
<td>6H-SiC, p-type</td>
<td>$E_C-E_T=0.33 \text{ eV}$</td>
<td>[127]</td>
</tr>
</tbody>
</table>

Table 7.9 Summary of new defects found in SiC
Chapter 8

Conclusions

In this work, several wide gap materials (GaN, ScN and SiC) have been investigated in order to identify and characterize deep level defects. The analysis included contact characterization (I-V), junction characterization (C-V) and defect investigation (DLTS). In order to perform DLTS analysis on a sample, it is necessary to fabricate a device that is characterized by a space charge region, which can be a Schottky barrier or a $p-n$ junction. This task is most often very difficult, especially if the material used limits the device characteristics. A “good device” has to have low leakage currents, low series resistance, and low density of interface states. All these requirements are hard to satisfy in order to built an ideal device; therefore, before proceeding to DLTS analysis, it is necessary to do other experiments on the samples. This has been described for all the samples used in this study. It has been observed that for some materials it is relatively easy to fabricated good Schottky barriers (such as SiC) while for others no Schottky barrier could be obtained (MBE GaN, rf-sputtered GaN).
For the materials where a junction was fabricated, DLTS showed interesting results for defects with deep levels in the band gap. However, the temperature range available in this study limits the analysis. Probably other defects besides the investigated ones exist in the samples as well.

It has been seen that in general, DLTS is an extremely suited technique for finding defects in the semiconductor, but it not easy to use due to all the limitation described above.

Trap B in MOCVD GaN has been investigated and an activation energy of 0.59 eV from the bottom of the conduction band was calculated, while its concentration decreases moving away from the buffer layer toward the top of the film.

MBE and rf-sputtered GaN were also investigated and proved to be unsuitable for DLTS analysis due to the fact that no Schottky barrier could be made out of the material.

ScN/Si p-n heterojunctions have been fabricated. DLTS analysis shows that electron traps with activation energies of 0.51 eV and 0.91 eV are present in the PAPVD and rf-sputtered ScN. The quality of the junction influences the DLTS results and sometimes signatures that are not related to traps but rather injection of carriers in the space-charge region are present.

4H- SiC and 6H- SiC Schottky diodes have been fabricated and investigated. It has been shown that several defects exist in the structure with a dependence upon the sample annealing temperature. The results were correlated with theoretical studies in an attempt to elucidate the nature of these defects.
Further study should concentrate on several directions:

1. to obtain a rf-sputtered GaN Schottky diode. This will involve understanding the influence the crystal structure of the films play upon the contact characteristics. It might be necessary to grow films at temperatures higher than 900 C in order to further improve the structure of the GaN.

2. if an rf-sputtered GaN is difficult to obtain, then, as in the case of ScN, $p-n$ junctions with a heavily doped $p$-type semiconductor, such as Si should be used instead.

3. to obtain a ScN Schottky barrier as well. If such a junction would be available, then the found defects, if any, could be better correlated with the ScN structure. Also, interesting would be to study the effect of radiation and particle bombardment upon the defects in this material.

4. For SiC, depending upon the growth method and post-growth processes, different defects are found. It is important to understand how these defects evolve. Investigation of higher annealing temperatures (>900C) upon the evolution of deep defects in SiC is an interesting subject which has not been by far exhausted.
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Appendix 1

Thermodynamical approach for the energy and capture-cross section of a trap

The relationship between the emission coefficient and the capture cross section is:

\[ e_n(T) = \sigma_n v_{th} N_C \exp\left( -\frac{E_C - E_T}{k_B T} \right) \]

(A.1)

From thermodynamical point of view, the trap energy obtained from Arrhenius plots is identified with the Gibbs free energy of ionization:
\[ \Delta G_n = E_C - E_T = \Delta H_n - T \Delta S_n \]  
(A2)

\[ \Delta H_n = E_n + pV \]  
(A3)

where \( \Delta H_n \) and \( \Delta S_n \) are the changes in enthalpy and entropy, respectively, \( V \) is volume and \( p \) pressure. The energy to excite an electron from a G-R center to the conduction band is given \( \Delta G_n \) [139]. Therefore, Eq. A1 becomes [46]

\[ e_n (T) = \dot{\delta}_n v_{th} X_n N_C \exp \left( -\frac{\Delta H_n}{k_B T} \right) \]  
(A4)

where \( X_n = \exp \left( \frac{\Delta S_n}{k_B} \right) \) is an “entropy factor” for the change in the entropy when the electron is emitted from G-R center to conduction band.

Eq.A4, states that the energy determined from Arrhenius plots is an enthalpy while the capture cross section differs from the true one by the prefactor \( X_n \). If the capture cross section has a temperature dependence, such as

\[ \sigma_n = \sigma_\infty \exp \left( \frac{E_b}{k_B T} \right) \]  
(A5)

\( (\sigma_\infty \) is the cross section when \( T \to \infty \) then
In these conditions, the Arrhenius plot gives neither the trap energy level nor its capture cross section correctly. If the capture cross section has an electric-field dependence, this increases the inaccuracies even more. While the first problem, that of a temperature dependence for the capture cross section can be identified using powerful fitting techniques such as those described in Ref. [79], the second problem is easily spotted if the DLTS peak shifts in temperature with filling pulse duration.

\[ e_n(T) = \sigma_n v_{th} x_n N_C \exp\left(-\frac{\Delta H_n + E_b}{k_B T}\right) \]  

(A6)
Appendix 2

Schematic of LabView programs used with DLTS

Figure A2.1 Labiew Interface for C-V measurements
As seen in the interface, the user has the option to set the initial value and the final for the voltage, the increment steps and how often to take data. These quantities are written in red color and are necessary for the program to run. The quantities in blue are not required to run the program, but are necessary for records. The green boxes show what the computer is reading from DLTS and temperature controller and are only for checking. These are correlated with values read from a multimeter.
This interface is similar with the one for C-V measurements, only there is no quantity that is send to neither the DLTS nor the temperature controller. The quantities in red are required for data processing, together with the ones in blue are for records on the measurement.

For C-V measurements, the flow diagram is similar, except now there is one more step after the file is opened. That is, a voltage is send to DLTS, which is
incremented by the set amount. Data acquisitioned is continued, in the case of DLTS measurements, till the user presses the STOP button, while in the case of C-V measurements, till either the user stops the program or the voltage reaches the final value.