A COMPLEMENTARY THIN FILM PROCESS FOR DIGITAL APPLICATIONS

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By
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# TABLE OF CONTENTS

<table>
<thead>
<tr>
<th>CHAPTER</th>
<th>PAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>I. INTRODUCTION</td>
<td>1</td>
</tr>
<tr>
<td>II. COMPARISON OF BULK SILICON AND SEMICONDUCTOR ON INSULATOR DEVICE</td>
<td>3</td>
</tr>
<tr>
<td>III. THEORY OF THIN FILM TRANSISTOR OPERATION</td>
<td>13</td>
</tr>
<tr>
<td>IV. A PROPOSED SEMICONDUCTOR ON INSULATOR PROCESS.</td>
<td>26</td>
</tr>
<tr>
<td>V. CHARACTERISTICS AND DEPOSITION OF THE LAYERS</td>
<td>30</td>
</tr>
<tr>
<td>Drain-Source Aluminum</td>
<td>30</td>
</tr>
<tr>
<td>Tellurium</td>
<td>32</td>
</tr>
<tr>
<td>Cadmium Selenide</td>
<td>33</td>
</tr>
<tr>
<td>Silicon Monoxide</td>
<td>34</td>
</tr>
<tr>
<td>Gate Aluminum</td>
<td>35</td>
</tr>
<tr>
<td>Summary of Process Parameters</td>
<td>36</td>
</tr>
<tr>
<td>VI. PREDICTED RESULTS</td>
<td>38</td>
</tr>
<tr>
<td>VII. EXPERIMENTAL RESULTS</td>
<td>40</td>
</tr>
<tr>
<td>VIII. CONCLUSION</td>
<td>46</td>
</tr>
<tr>
<td>IX. BIBLIOGRAPHY</td>
<td>47</td>
</tr>
<tr>
<td>Figure</td>
<td>Description</td>
</tr>
<tr>
<td>--------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>1.</td>
<td>Parasitic Devices in Bulk Silicon CMOS</td>
</tr>
<tr>
<td>2.</td>
<td>Leakage Paths in SOS</td>
</tr>
<tr>
<td>3.</td>
<td>Staggered electrode configuration of the thin film transistor</td>
</tr>
<tr>
<td>4.</td>
<td>TFT configuration for calculation of V-L characteristics</td>
</tr>
<tr>
<td>5.</td>
<td>CMOS inverter and ideal characteristics</td>
</tr>
<tr>
<td>6.</td>
<td>Circuit for derivation of rise and fall times</td>
</tr>
<tr>
<td>7.</td>
<td>Proposed Complementary TFT Process</td>
</tr>
</tbody>
</table>
CHAPTER I
INTRODUCTION

Since the discovery of the bipolar transistor at the Bell Laboratories in 1947, many advances have been made in semiconductor technology. These advances have made possible the current "electronic age." In the early 1950's, an average household probably had a limited number of active electronic devices, most notably the vacuum tubes in a radio receiver. In today's society, the number of active devices has increased dramatically, with the emergence of home computers, video games, and microprocessor controlled appliances, all of which would have been economically and physically unthinkable to the general public without present day integrated circuit technology.

Present day integrated circuit technology can be divided into two main categories, namely, bipolar technology and field effect transistor (FET) technology. For large scale integration, defined as greater than 1,000 devices per chip, the desired technology appears to be CMOS field effect transistor technology. CMOS technology is complementary metal oxide semiconductor, a technology that uses both n-channel and p-channel field effect devices on the same substrate. The main advantages of CMOS technology are low power consumption and simplicity of fabrication,
as compared with bipolar technology. Currently, many variations of the CMOS technology are in use, for example, p-well on n-substrate, n-well on p-substrate, p\textsuperscript{-}-epitaxial layer on p\textsuperscript{+}-substrate, n\textsuperscript{-}-epitaxial layer on n\textsuperscript{+}-substrate, and silicon on sapphire (SOS) (1). Y. Okata, in his introductory statement to a discussion on CMOS Technology Direction at the International Solid State Circuits Conference in February, 1983, stated, "The SOI structure, including SOS, remains as one of the ideal configurations for CMOS" (2). The purpose of this work is to explore an alternative SOI (semiconductor on insulator) structure consisting of amorphous semiconductors evaporated on a substrate of glass to form a CMOS-like structure and compare its characteristics to characteristics of silicon on sapphire and bulk silicon CMOS technologies.
CHAPTER II
COMPARISON OF BULK SILICON AND
SEMICONDUCTOR ON INSULATOR DEVICE

Before a new semiconductor on insulator process is proposed, the existing semiconductor on insulator process should be compared to existing bulk silicon processes. The most common CMOS semiconductor on insulator process in use at the present time is silicon on sapphire. The silicon on sapphire consists of 15 to 20 mil sapphire substrate with a 0.6 to 0.8 micron layer of epitaxial single crystal silicon grown on top. Sapphire is used because of its chemical and physical properties, and a crystal plane can be selected that is a close enough match to silicon to grow a single crystal silicon layer on it. There are many advantages and disadvantages to using silicon on sapphire over bulk silicon for CMOS devices.

One advantage of silicon on sapphire over bulk silicon devices is that the silicon on sapphire has better latch up characteristics. In a bulk silicon CMOS integrated circuit, there exists a parasitic bipolar transistor formed by the n- source-drain, the p-well used to form the n-channel devices, and the n-substrate. This constitutes a vertical npn transistor. A lateral pnp bipolar transistor also exists between the p-well, the n-substrate and the p- region that
forms the p-channel device source-drains. These two bipolar devices, along with the input protection diodes, can form a pnpn device that can latch up if certain conditions are met. When the device is latched up, it draws an excessive amount of current. In order to latch up, the product of the gains of the vertical npn and the lateral pnp must be greater than one. Another condition is that the emitter-base junction of each transistor must become forward biased (3). This can occur when the input to the integrated circuits exceeds the supply voltage, which can occur during transient spikes. This is illustrated in Figure 1. The silicon on sapphire integrated circuits do not have a problem with latch up. There is no coupling between the n-substrate and the p-well because the n-type epitaxial silicon islands are physically separated from the p-type islands, eliminating the lateral pnp transistor. The vertical npn transistor is eliminated by the fact that islands of silicon used for n-channel devices are counter-doped completely to p-type, leaving no n-type for the collector. This is a desirable characteristic that any semiconductor on insulator process should retain.

Another advantage of the silicon on sapphire devices is lower propagation delay than CMOS bulk silicon devices. The silicon on sapphire devices are a factor of two better than bulk silicon devices. For geometry sizes down to
Figure 1: Parasitic Devices in Bulk Silicon CMOS.
2.0 microns, silicon on sapphire has a lower interelectrode capacitance, however, below 2 microns, the bulk silicon devices approach the silicon on sapphire devices. In practice, as geometry size shrinks, so do other parameters, for example, the field oxide is thinner, which would increase capacitance to substrate, so it is not clear at the present time whether bulk silicon can equal silicon on sapphire at even small geometries (4). The lower interelectrode capacitance and the lower propagation delay time are features that are favorable for large scale integration and should be retained in the proposed process.

With the island type structure of the semiconductor on insulator devices, a higher packing density is obtainable. In integrated circuits, devices must be electrically isolated from each other. This is achieved in silicon on sapphire by etching the epitaxial silicon all the way to the sapphire, thereby creating islands. These islands are isolated from each other, provided the sapphire substrate is not conductive. Using this method of isolation, the minimum distance between islands is equal to the smallest space that can be etched. In the bulk silicon process, the isolation must be done using either a junction or an oxide. For the junction isolation case, the isolation is achieved by a reversed bias junction, and the minimum distance between devices is now the minimum opening that can be
etched plus the lateral diffusion associated with the junction diffusion. In the oxide isolated case, the isolation between devices is obtained by a light surface implant in the field areas and a thick oxide over the field areas. The minimum distance between the devices with this method is a minimum opening that can be defined plus the "bird's beak", which is the amount of lateral growth of the field oxide. It is evident that the highest packing density that can be achieved is with the silicon on sapphire process.

The most notable disadvantage to the silicon on sapphire process is the cost of the starting material. The sapphire substrate is more expensive than a bulk silicon substrate and the single crystal epitaxial layer on the sapphire adds to the cost. The quality of the epitaxial silicon grown on the sapphire is very dependent on the surface of the sapphire prior to the deposition. The best results are obtained by firing the sapphire in hydrogen at 1500°C (5). The bulk silicon wafers are grown in ingots, 60 to 70 cm. long, and then sliced and polished into wafers approximately 20 mils thick. The cost advantage of bulk silicon CMOS should start to diminish as the use of epitaxial layers on bulk silicon wafers becomes necessary to reduce the latch up problem in bulk silicon devices as geometries decrease into the 2 micron region (6). It would
be advantageous to use a less expensive substrate than sapphire for any semiconductor on insulator process, and also to eliminate the single crystal epitaxial silicon layer that is difficult to fabricate.

Another disadvantage to the silicon on sapphire process is that the devices will have higher leakage currents than the equivalent bulk silicon CMOS device. Leakage current is the current that flows through the device when the device is turned off. The increase in leakage current is caused by two things: the first is back channel leakage and the second is edge leakage. Both types of leakage occur primarily in n-channel devices and are illustrated in Figure 2. Back channel leakage takes place at the silicon-sapphire interface. At this interface there are surface states that make the silicon appear to be doped n-type. In n-channel devices, this creates an n-type leakage path between the source and the drain. Back channel leakage can be reduced by using a heavy, deep, p-type implant into the p-type islands (that form the n-channel device) in addition to the p-type implant that is needed to set the device threshold. This extra implant will, of course, make the silicon on sapphire process more expensive. The edge leakage is not as simple to fix as the back channel leakage. The edge leakage, as the name implies, takes place at the top edge of the epitaxial islands. After the epitaxial islands are etched,
Figure 2: Leakage paths in SOS (a) bulk channel leakage, (b) edge leakage.
the gate insulating oxide must be grown on the island. Islands that will form the n-channel devices are doped with boron, and islands that become p-type devices are doped with phosphorus. When thermal oxidation takes place, the impurities in the silicon islands will redistribute. Each dopant can be characterized by a segregation coefficient which will give the ratio of the impurity concentration in the silicon to the impurity concentration in the oxide (1). If the segregation coefficient is greater than one, the equilibrium concentration in the silicon is higher than that in the oxide, and the dopant will tend to remain in the silicon. If the segregation coefficient is less than one, the dopant prefers to reside in the oxide. The segregation coefficient for boron is less than one, and that for phosphorus is greater than one. This causes a problem in the p-type islands, that is, the boron is leached from the silicon into the oxide. The island can be doped heavier to compensate for this, however, at the edge of the island the oxide is growing in two surfaces, on the top of the island and on the side. As a result of this, twice as much boron is leached from the edges as from any other area. The lack of boron in this area causes the edge of the island to turn on at a lower gate potential than the rest of the island, causing leakage. This problem can be solved by the use of edge implants, however, the existing
edge implant processes are difficult to implement, add a photomasking operation and reduce the effective width of the device, all of which are undesirable. Bulk silicon CMOS processes do not have either back channel leakage or edge leakage, so it would be desirable to eliminate these leakages in any future semiconductor on insulator process.

A third disadvantage of using silicon on sapphire technology is its susceptibility to wafer breakage and twinning. The twinning and breakage occur more readily in the silicon on sapphire process because the coefficient of thermal expansion for sapphire is different from that of silicon. Whenever the wafer is heated, the sapphire creates stress on the silicon and this can either break the wafer into pieces, or cause a crack and lifting of the silicon epitaxial layer. The crack, or twinning, of the epitaxial layer can extend across the entire wafer, ruining all the devices it cuts through, but more importantly, one side of the twin is several microns above the other side, causing photolithography problems. These photolithographic problems usually show up as one part of the wafer being out of focus, and the yield on the wafer is considerably reduced. To prevent twinning and breakage, very long ramp cycles are used while heating and cooling the wafers in a furnace. The long ramps slow down the process, thus adding cost to the silicon on sapphire devices. Bulk CMOS devices do not have
the twinning or breakage problem as severe as silicon on sapphire because the substrate and the active areas are the same material with the same coefficient of thermal expansion. The best way to eliminate the twinning and breakage problem associated with silicon on sapphire is to have a semiconductor on insulator process with all low temperature operations.

The main advantages listed above that will be maintained in the proposed semiconductor on insulator process are:

1. Reduced latch up
2. Better speed than bulk silicon CMOS
3. Higher packing density.

The disadvantages that the proposed process will try to overcome are:

1. High cost
2. High device leakage
3. Twinning/Breakage.

By incorporating the advantages of the silicon on sapphire process and the bulk CMOS process, the semiconductor on insulator process should be superior to both.
CHAPTER III
THEORY OF THIN FILM TRANSISTOR OPERATION

The semiconductor on insulator process to be proposed will employ thin film transistors of cadmium selenide and tellurium used for the n-channel and p-channel devices respectively. The original work with thin film transistors and the associated theory was done at the RCA Laboratories in 1962 by Paul Weimer (8). The structure of such a device is shown in Figure 3. The structure shown is known as the staggered electrode configuration because the drain and source electrodes are on a different level from the gate electrode. Other configurations are possible, however they will not be considered here.

Figure 4 shows an incremental section of the thin film transistor to be used for the derivation of the voltage-current characteristics of the device. Consider an incremental section of semiconductor a distance x from the source with a length dx. The gate electrode, insulating dielectric, and semiconductor form a capacitor. Let the capacitance per unit area be $C_g$. The charge transferred to the segment of semiconductor, $q_t$, is then

$$q_t = C_g(V_g - V_x) \quad (1).$$

The gate potential is $V_g$, which is a constant, and $V_x$ is
Figure 3: Staggered electrode configuration of the thin film transistor.

Figure 4: TFT configuration for calculation of V-I characteristics.
the potential a distance \( x \) from the source, which will vary continuously from the source to drain. If the source is grounded, and the drain at potential \( V_d \), the potential varies from zero to \( V_d \). In addition to the charge transferred from the gate, there exists an initial number of free carriers at the surface of the semiconductor which are free to conduct. If the number of carriers per unit area is given as \( N_o \), and the charge per carrier is \( q \), then

\[
q_o = qN_o
\] (2).

The total number of electrons free to conduct for a given gate voltage, \( V_g \), is the sum of equations (1) and (2). The total conducting charge, expressed per unit area, is

\[
q_c = qN_o + C_g(V_g - V_x)
\] (3).

The current density in the semiconductor can be found from the following relationship (9):

\[
J_x = q\mu n E_x
\] (4).

In this equation, \( qn \) is the charge per unit volume available for conduction, \( \mu \) is the mobility, expressed in cm\(^2\)/V - sec, and \( E_x \) is the electric field. Using equation (3) as an expression for the charge per unit area available for conduction, equation (4) can be written as

\[
J_x = \frac{(qN_o + C_g(V_g - V_x))\mu E_x}{\mu E_x} \] (5).
The term \( t \) is the thickness of the semiconductor layer. By dividing by \( t \), the assumption is made that \( N_0 \) is constant throughout the entire thickness of the semiconductor, which is reasonable because only thin films are being considered. By multiplying both sides of equation (5) by the cross sectional area of the device, \( w t \), the result will be the current in the x-direction. Assuming the voltage along the channel from source to drain varies only in the x-direction, equation (5) becomes

\[
I_d = w \mu (qN_0 + C_g(V_g - V_x)) E_x
\]

(6).

It is also known that

\[
E_x = \frac{dV_x}{dx}
\]

(7).

Using the relationship in equation (7), equation (6) can be written as

\[
I_d = w \mu (qN_0 + C_g(V_g - V_x)) \frac{dV_x}{dx}
\]

(8).

Equation (8) can be re-written in the following form:

\[
I_d dx = w \mu (qN_0 + C_g(V_g - V_x)) dV_x
\]

(9).

Equation (9) must be integrated with the proper limits to give an expression for the current in terms of the applied voltage. Since it is desired to find the total current in the semiconductor from the drain to the source, the left hand side of equation (9) should be integrated from zero to \( L \), where \( L \) is the length of the channel. The right hand
side should be integrated from zero to \( V_d \), where the source is grounded and the drain is at a potential of \( V_d \). Equation (9), with the proper limits of integration, is

\[
I_d \int_0^L dx = w \mu \int_0^{V_d} (qN_0 + C_g(V_g - V_x)) dV_x
\]  

Before the integration is performed, equation (10) can be rearranged to make the integration easier. Using the following definition

\[
V_o = \frac{-qN_0}{C_g}
\]

Equation (10) can be written

\[
I_d \int_0^L dx = w \mu C_g \int_0^{V_d} ((V_g - V_o) - V_x) dV_x
\]

Now the integration can be performed quite easily, and the result is

\[
I_d = \frac{w \mu C_g}{L} ((V_g - V_o)V_d - \frac{V_d^2}{2})
\]

Equation (12) gives the drain current as a function of the applied voltage and a term \( V_o \), which is the gate potential needed for the onset of conduction (10). If the voltage needed to start conduction is positive, the device is an enhancement device, that is, a device which with zero gate voltage has zero drain current. A device which has \( V_o \) negative is called a depletion device and with zero voltage applied has a drain current flowing.

Equation (13) is valid only when \( V_d \) is less than \( V_g - V_o \).
otherwise the drain current would decrease with increasing drain voltage. What actually happens is the drain current saturates at the maximum value given by equation (13). By differentiating equation (13), and setting the derivative equal to zero, the maximum $I_d$ occurs at

$$V_d = V_g - V_o$$  \hspace{1cm} (14).$$

For drain voltage greater than $V_g - V_o$, the drain current remains constant; this is called the saturation region. The saturation region is of particular interest for digital applications because most of the switching devices operate in this region. To find the saturation current equation (14) is substituted into equation (13), the result is

$$I_{d, sat} = \frac{w \mu C}{L} \frac{(V_g - V_o)^2}{2}$$ \hspace{1cm} (15).$$

The transconductance in the saturation region is also of interest. The transconductance in the saturation region, $g_{m, sat}$, is defined as the derivative of saturation current with respect to the gate voltage. The transconductance in the saturated region is

$$g_{m, sat} = \frac{dI_{d, sat}}{dV_g} = \frac{w \mu C}{L} (V_g - V_o)$$ \hspace{1cm} (16).$$

Using equation (15), the transconductance can also be expressed as

$$g_{m, sat} = \left[\frac{2w \mu C}{L} I_{d, sat}\right]^{\frac{1}{2}}$$ \hspace{1cm} (17).$$
This gives an expression for the transconductance in the saturation region which is a function of only one measured parameter, that being $I_{d,sat}$.

The gate used to study thin film transistors for use in digital applications is the inverter. A complementary thin film transistor inverter can be constructed very much like a standard CMOS inverter. The inverter configuration is shown in Figure 1, along with the ideal characteristics. When the input voltage is equal to zero, the gate to source voltage of the n-channel device is zero and the device is off, so a large resistance exists between the drain and source of the n-channel device. The gate to source voltage of the p-channel device is equal to $V_{DD}$, so the p-channel device is turned on, and the channel is essentially a short from drain to source. With the p-channel device on and the n-channel off, the output voltage is equal to the supply voltage. When the input voltage is equal to the supply voltage, the p-channel gate to source voltage is zero, and it is turned off. The n-channel device's gate to source voltage is equal to $V_{DD}$, so it is on. With the p-channel device off and the n-channel on, the output voltage is equal to zero. In a CMOS inverter, the current that flows when the output is high or low (but not switching) is equal to the reverse bias leakage of the junctions between the source-drain regions and the channel regions of the device.
that is cut off. For a thin film transistor, the current that flows with the output high or low is the supply voltage divided by the channel resistance of the device that is turned off. To lower static power consumption, it is necessary to have very high channel resistance in the cut-off region.

The speed of the thin film transistor must be considered. Consider the circuit shown in Figure 4. Assume that all the output capacitance is lumped into a single element, $C_L$. Further, assume that the time for the input voltage to go from zero to $v_{in}$ is negligible and the response of the transistors is instantaneous. The switching time will be a function of the saturation current of the devices and the load capacitance, $C_L$. Let the input voltage $v_{in}$ in Figure 4 switch from zero to some $v_{inH}$. The n-channel device will turn on, and $i_n$ will be $i_{n, sat}$, also the p-channel device will be turned off, so $i_p$ will be zero. Since the p-channel current is zero, the load capacitance must discharge through the n-channel device and

$$i_{n, sat} = -i_c \quad (18).$$

From equation (15),

$$i_{n, sat} = \frac{w_n \mu_n \frac{C}{L_n}}{v_{inH} - V_0} \cdot (v_{inH} - V_0) \quad (19).$$

It is also known that

$$i_c = C_L \frac{dV_{out}}{dt} \quad (20).$$
Figure 5: (a) CMOS inverter
(b) ideal characteristics.

Figure 6: Circuit for derivation of rise and fall times.
Combining equations (18), (19) and (20), the result becomes

$$\frac{w_n \mu_n C}{2L_n} (V_{inH} - V_o)^2 = -C_L \frac{dV_{out}}{dt}$$  \hspace{1cm} (21).$$

Solving equation (21) for $dt$, the equation becomes

$$dt = \frac{-C_L 2L_n}{w_n \mu_n C \cdot g_n} \frac{dV_{out}}{(V_{inH} - V_o)^2}$$

By integrating over the proper limits, equation (22) will yield the time the output voltage takes to fall from its initial value, $V_{outH}$, to its final value $V_{outL}$. Referring to the fall time as $t_f$, the integral equation is

$$\int_{0}^{t_f} dt = \frac{-C_L 2L_n}{w_n \mu_n C \cdot g_n} \int_{V_{outH}}^{V_{outL}} \frac{dV_{out}}{(V_{inH} - V_o)^2}$$  \hspace{1cm} (23).$$

Solving this equation gives

$$t_f = \frac{-C_L 2L_n}{w_n \mu_n C \cdot g_n} \frac{(V_{outL} - V_{outH})}{(V_{inH} - V_o)^2}$$  \hspace{1cm} (24).$$

Typically, the input voltage and, thus, the gate to source voltage for the n-channel device swings from zero to the supply voltage, $V_{DD}$, and the high and low output voltages are approximately $V_{DD}$ and zero respectively, making these substitutions, the result is

$$t_f = \frac{C_L 2L_n}{w_n \mu_n C \cdot g_n} \frac{V_{DD}}{(V_{DD} - V_o)^2}$$  \hspace{1cm} (25).$$

The rise time of the output can be found in a similar
fashion. In this case the input voltage falls to zero, and the p-channel device is in the saturation region. Now the current in the p-channel device equals the capacitor current and the equation can be written as

$$C_L \frac{dV_{out}}{dt} = \frac{w_p \mu_p C_p}{2L_p} (V_{inL} - V_{DD} - V_o)^2$$  \hspace{1cm} (26).$$

Rearranging this equation gives

$$dt = \frac{2L_p C_L}{w_p \mu_p C_p} \frac{dV_{out}}{(V_{inL} - V_{DD} - V_o)^2}$$  \hspace{1cm} (27).$$

The integration must be performed to find the rise time of the output. Since the output voltage is going from $V_{out\text{L}}$ to $V_{out\text{H}}$, the limits are opposite those in equation (23). The equation, ready for integration, is

$$\int_{0}^{t_r} dt = \frac{2L_p C_L}{w_p \mu_p C_p} \int_{V_{out\text{L}}}^{V_{out\text{H}}} \frac{dV_{out}}{(V_{inL} - V_{DD} - V_o)^2}$$  \hspace{1cm} (28).$$

Solving this integration yields

$$t_r = \frac{2L_p C_L}{w_p \mu_p C_p} \frac{V_{out\text{H}} - V_{out\text{L}}}{(V_{inL} - V_{DD} - V_o)^2}$$  \hspace{1cm} (29).$$

As was stated previously, $V_{out\text{H}}$ can be approximated as the supply voltage, $V_{out\text{L}}$ as zero, and $V_{inL}$ as zero. Using these values, equation (29) reduces to

$$t_r = \frac{2L_p C_L}{w_p \mu_p C_p} \frac{V_{DD}}{(-V_{DD} - V_o)^2}$$  \hspace{1cm} (30).$$
An analysis of the units of equations (30) and (25) show the result to be given in seconds. It should be noted that in these equations, $C_{gp}$ and $C_{gn}$ are given in capacitance per unit area.

As stated previously, the power under static conditions is very low if the channel resistances when the devices are off are high. During the switching time there is power consumed to charge the capacitive load. If it is assumed that the frequency of the input signal is low enough to allow the output to charge to maximum voltage, that is, the supply voltage, the power consumed is given by (11)

$$P = C_L V_{DD}^2 f_o$$

(31).

Where $C_L$ is the load capacitance, $f_o$ is the frequency of input voltage and $V_{DD}$ is the supply voltage.

The power drawn from the supply when the p-channel device is in saturation and the capacitor is charging is given by

$$P_{ps} = V_{DD} i_p$$

(32).

Substituting in the expression for the saturation current in the p-channel device, the result is

$$P_{ps} = V_{DD} \left[ \frac{\mu p w C_{gp}}{2 L_p} \right] (V_{DD} - V_o)^2$$

(33).

Likewise, when the n-channel device is in saturation, the
the power delivered by the source is

\[ P_{ns} = V_{DD} \left[ \frac{u_{n} w_{n} C_{gm}}{2 L_{n}} \right] (V_{DD} - V_{o})^{2} \]  \hspace{1cm} (34).

Both equation (33) and (34) assume that the input voltage swings from zero to the supply voltage.

Using equations (25), (30), (31), (33) and (34), the speed of the inverter, the power consumed by the inverter, and the power that must be dissipated in each device can be calculated.
CHAPTER IV
A PROPOSED SEMICONDUCTOR ON INSULATOR PROCESS

In chapter II, desirable characteristics for a semiconductor on insulator process were laid out. In chapter III, the equations that govern thin film transistor operation were derived. Using these two chapters as guidelines, the process will be proposed.

The process is shown in Figure 7. The configuration used is the staggered electrode configuration. The staggered electrode configuration was chosen because it lends itself to interconnection of devices more readily. This configuration gives two levels of interconnect separated by an insulator, allowing a more dense structure. If a coplanar structure, which has the source-drain and gate aluminum on the same level, were used, a process with one less step could be developed. The coplanar structure would add additional complications to the mask making and the gate aluminum could not cross drain-source aluminum as it can in the staggered electrode case.

The process is a complementary thin film process, that is, it uses both n-type and p-type thin film transistors. The complementary configuration was used to reduce power consumption. The n-type devices are made using cadmium
Figure 7: Proposed Complementary TFT Process
(a) top view of inverter
(b) cross section.
selenide and the p-type devices were made using tellurium. The drain-source contact was made using aluminum, however, this layer could be any good conductor that makes an ohmic contact to both cadmium selenide and tellurium. The gate insulator used is silicon monoxide. Again, any insulating material could be chosen for the gate insulator instead of silicon monoxide. The gate electrode used was also aluminum. With the gate electrode, any low resistivity metal could be used.

An optional layer, not shown in Figure 5, is a silicon monoxide overcoat. To keep the device's characteristics from deteriorating with time, the device should be sealed with an oxide layer. This layer will do three things: the first is physical protection to keep the aluminum from smearing, the second is to provide a contamination barrier, and the third is to reduce electromigration.

All layers used in the proposed process can be evaporated by heating of crucibles. The heating is done by sending large currents through low resistance crucibles filled with the material to be evaporated. The evaporation is done under high vacuum, and all evaporation may be done at room temperature.

The substrates to be used are made of glass. Glass was chosen because of its cost, and the fact that all the
materials adhere to it readily at room temperature. Using glass eliminates the cost associated with sapphire in the silicon on sapphire process.
CHAPTER V
CHARACTERISTICS AND DEPOSITION OF THE LAYERS

3.1 Drain-Source Aluminum

The first layer to be deposited is the drain-source aluminum. This layer makes ohmic contact to all source and drain areas of all p-type and n-type devices. This aluminum also makes any necessary connections between the drains and sources of different devices. It is also possible that this layer could contact the gate aluminum layer to make connections between sources, drains and gates. In the inverter circuit, the source-drain aluminum forms the output pad, the supply voltage pad and the pad for ground.

It is important that the aluminum have very low resistivity in order that there are no unnecessary voltage drops or power loss in the conductors. The resistivity of a thin film can be described by (12)

\[ \rho = \rho_B - \frac{3/8(k)}{1 - 3/8(k)} \rho_B \]  

(35).

Where \( k \) is the ratio of the thickness of the film to the mean free path of carriers in the film, \( \rho \) is the resistivity of the film and \( \rho_B \) is the bulk resistivity. For aluminum, the mean free path can be taken as 100 angstroms (13). If the thickness of the aluminum layer for the drain-source
interconnect is chosen to be 500 angstroms, the resistivity, using equation (35), and a bulk resistivity of 2.7 $\mu$ohms-cm, the resistivity is found to be 2.92 $\mu$ohms-cm, or 1.081 times the bulk value. Using the relationship

$$ R = \rho \frac{L}{A} $$ \hspace{1cm} (36)

where $R$ is the resistance, $\rho$ the resistivity, $L$ the length of the conductor, and $A$ the cross sectional area of the conductor, for a conductor of 1cm in length by 0.25 cm wide, which is representative of a metal run in the inverter, the resistance is 0.234 milliohms. This value is low enough to be neglected even at high currents.

Another characteristic of the aluminum drain-source contact is that it must be thin enough so the semiconductors can step over the metal edge without cracking. There must be a trade-off between this characteristic and the resistivity characteristic mentioned above. A value of 500 $\AA$ is the value chosen for this layer because it provides low resistivity and a small step for the thin semiconductor layer.

The surface of the first layer of aluminum layer must be smooth compared to the thickness of the overlaying layers. To make the surface smooth, the deposition of the aluminum must be controlled. To get a smooth surface, the deposition should be slow and the substrate hot to allow the aluminum to move freely on the surface of the substrate. The film
can be deposited at 5 angstroms per second to a thickness of 500 Å, using a current of 200 amps through a tungsten boat. The pressure for this deposition is chosen to be 5 x 10^{-6} torr. Since one of the objectives of the process is to eliminate temperature operations, the aluminum is deposited at room temperature.

5.2 Tellurium

Tellurium is the material chosen for the p-type enhancement devices. Even though the resistivity is in the order of tenths of an ohm-cm, good enhancement mode devices can be obtained if the tellurium film is kept very thin (14). The good saturation characteristics are achieved by keeping the film so thin that the depletion layer formed at the drain of the transistor extends through the entire film. Good results have been reported using a tellurium thickness of 150 angstroms (15).

Tellurium is an element, so when it is evaporated there is no problem with dissociation, like in the case of cadmium sulfide. The tellurium adheres well to the glass, so there is no need to heat the substrate. The tellurium should be deposited at 5 x 10^{-6} torr, passing 80 amps through a tungsten boat. This current will produce a rate of 4 angstroms per second. The thickness to be used is 150 angstroms, with the deposition performed at room temperature. Using this type of deposition, a mobility of 200 cm^2/volt-
seconds have been reported (16).

5.3 Cadmium Selenide

Cadmium selenide was chosen for the n-type devices. Also considered for the n-type devices was cadmium sulfide. Cadmium sulfide has a lower mobility than cadmium selenide and the problems with dissociation are greater with the cadmium sulfide. Dissociation is when one of the elements of a compound evaporates faster than the others, giving a film with an inconsistent composition. The vapor pressure for cadmium and selenide are very close to each other, while the vapor pressure of sulfide is much higher than cadmium for any temperature (17). The cadmium selenide can be deposited at room temperature, with no adhesion problems to the glass substrate.

The thickness of the cadmium selenide must be determined. To get good saturation and enhancement mode characteristics, the thickness that can be used is 100 angstroms (18). Mobilities as high as $30 \text{ cm}^2/\text{volt-second}$ have been reported (19).

The cadmium selenide was deposited at a rate of 5 angstroms/second, at a pressure of $5 \times 10^{-6}$ torr. The current needed for this evaporation is 60 amps. The substrate was at room temperature. The crucible used for evaporation was a tungsten boat.
5.4 Silicon Monoxide

Silicon monoxide was used for the gate insulating dielectric. In silicon monoxide, the dielectric constant, resistivity and composition of the film are very dependent on the deposition parameters. Either silicon monoxide or silicon dioxide would be sufficient for the insulator. By controlling the partial pressure of the oxygen in the vacuum system at the time of the deposition, the composition can be controlled (20). The resistivity of the dielectric is a function of the deposition rate (21). The slower the deposition rate, the higher the resistivity.

The layer of the silicon monoxide has to be thick enough to be a good insulator for the gate, but thin enough to keep the gate capacitance, $C_g$, high to have good charge transfer to the semiconductor, see equation (13). The silicon monoxide must also be thick enough to insulate the drain-source aluminum from the gate electrode aluminum, should the two layers cross. Because the oxide must insulate between the two aluminum layers, the oxide should be deposited everywhere except in the areas where contact must be made to the outside world. This is easily achieved if the device is laid out so that all areas where contact will be made to the drain-source aluminum are at the edge of the substrate. With the devices laid out as such, the oxide mask consists of covering the outer $\frac{1}{4}$ cm of the
substrate, around all the edges. In the case of the inverter, this leaves an area on the outer edge of the substrate for contact to be made for the supply voltage, the ground and the output voltage.

The thickness of the insulator was chosen to be 1500 angstroms. The pressure of the vacuum system should be \(5 \times 10^{-6}\) torr, and the rate of deposition should be 1.5 to 2.0 angstroms per second. The current for these depositions is about 340 amps. The crucible used for evaporation of silicon monoxide is a baffled box. This box consists of two compartments separated by a partition that extends three quarters the height of the box. On the top of the box, there is a chimney for each compartment, and one chimney is blocked by a removable cap. The silicon monoxide source is poured into the side with the cap, and the cap is replaced. During the deposition, the baffle prevents the source from splattering out and causing pinholes in the oxide. The baffle allows only vapor to pass to the other side and escape through the uncapped chimney to be deposited on the substrate.

5.5 Gate Aluminum

The gate aluminum thickness and composition are the least critical of any layer. The gate electrode of an insulated gate field effect device should draw no current, so the resistivity of the layer is not critical. The
thickness of the aluminum for the gate layer is chosen to be 500 angstroms. This is the same as the drain-source aluminum and the deposition parameters are identical.

The most critical aspect of the gate electrode is the alignment of the gate. If the gate is offset, the electrode will hang over the drain or source aluminum, causing a capacitor to be formed. The capacitor is made up of the gate electrode that is misaligned, the gate oxide, and the drain-source aluminum. The capacitor's area will be determined by the amount of overlap. The capacitor will couple the input to either the source or drain, which will slow the device down, and possibly prevent the device from operating. To prevent this from happening, the gate electrode should be narrower than the length of the channel.

5.6 Summary of Process Parameters

A summary of the proposed process parameters and deposition conditions is found in Table I.
### Table I: Summary of Process Parameters

<table>
<thead>
<tr>
<th>Level</th>
<th>Rate (A/sec)</th>
<th>Current (Amps)</th>
<th>Thickness (Angstroms)</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain-Source Aluminum</td>
<td>5</td>
<td>200</td>
<td>500</td>
<td>3.0 μohm-cm</td>
</tr>
<tr>
<td>Tellurium</td>
<td>4</td>
<td>80</td>
<td>150</td>
<td>( \mu_p = 300 \text{ cm}^2/\text{V-sec} )</td>
</tr>
<tr>
<td>Cadmium Selenide</td>
<td>5</td>
<td>60</td>
<td>100</td>
<td>( \mu_n = 30 \text{ cm}^2/\text{V-sec} )</td>
</tr>
<tr>
<td>Silicon Monoxide</td>
<td>1.5-2.0</td>
<td>340</td>
<td>1500</td>
<td>( C_g = 28.9 \text{ nF/cm}^2 )</td>
</tr>
<tr>
<td>Gate Aluminum</td>
<td>5</td>
<td>200</td>
<td>500</td>
<td>Same as Drain-Source Aluminum</td>
</tr>
</tbody>
</table>

**Note:**

1) All depositions at 5 x 10^{-6}.

2) \( C_g = \epsilon/\epsilon_{ox}, \epsilon_r = 4.9 \) from Reference (20).
CHAPTER VI
PREDICTED RESULTS

Using the equations derived in chapter III, and the parameters listed in chapter V, a prediction of speed and power consumption can be made.

In order to calculate the fall time using equation (26), the following parameters must be known: $C_L$, the load capacitance, $L_n$, the channel length, $V_{DD}$, the supply voltage, $w_n$, the width of the transistor, $\mu_n$, the mobility, $C_{gn}$, the gate capacitance, and $V_o$, the turn-on voltage of the device. The width and length of the transistor can be chosen by the designer. The load capacitance and supply voltage can be at any fixed value, for this calculation, assume the supply voltage of five volts and a load capacitance of 20 pf. The mobility of the cadmium selenide will be taken as 30 cm$^2$/V-sec as given in Table I. The gate capacitance is fixed by the process and is 28.9 nf/cm$^2$. The term $V_o$ in equation (26) can be neglected, since it is a function of the number of free electrons in the cadmium selenide with no applied voltage, and the thin film was made to have very high resistivity with no applied gate voltage.

Using the values given above, a transistor width of 0.5 cm, and a length of 0.1 cm, the fall time is calculated as 1.8 microseconds. From equation (34), the power can be
calculated as 0.27 milliwatts. These are representative numbers that should be obtained in the laboratory.

To compare this process with existing state of the art processes, the same equations can be used, with the sizes of the features appropriately scaled. Optimum results for silicon on sapphire have been reported in the literature (22). The parameters used to achieve these results are:

\[
\begin{align*}
C_L &= 22 \text{ fF}d \\
V_{DD} &= 3.0 \text{ volts} \\
w &= 5.0 \text{ microns} \\
L &= 0.75 \text{ microns} \\
t_{ox} &= 450 \text{ angstroms}
\end{align*}
\]

The results reported for silicon on sapphire are a fall time of 400 picoseconds and a power of 250 microwatts. Using equations (26) and (34), the thin film process, for the same parameters has a fall time of 761 picoseconds and a power of 260 microwatts. The bulk silicon CMOS has been reported to be a factor of two worse than silicon on sapphire, for fall time and power. This means that the thin film process lies between silicon on sapphire and bulk CMOS. It should be noted that the reported results are for two input NAND gates, and the delay is measured when the output is falling.
CHAPTER VII
EXPERIMENTAL RESULTS

Three generations of devices were fabricated. The first two generations yielded no good devices. With some process and design changes, the third generation yielded some data.

The depositions were done using a Veeco deposition system with a Kronos thickness and rate monitor. The substrates used were glass microscope slides, cleaned with acetone and methanol prior to the first deposition. The masks were made by cutting the features out of aluminum foil and putting the aluminum foil over the glass slide.

The first generation of devices were fabricated using 1000 Å drain-source aluminum and cadmium sulfide for the n-type device. The problems with this generation were three-fold. The first problem was that the drain-source aluminum definition was not good. This meant that the channel lengths were not well defined, and led to the decreasing of the thickness of the aluminum to 500 Å. The second problem was the dissociation of the cadmium sulfide. This problem was fixed by changing to cadmium selenide. The third problem was that the gate electrodes were shorted to the source-drains. The gate oxide thickness for this generation was 1000 Å. For future devices the gate oxide
thickness was increased to 1500 Å.

The second generation of devices was fabricated using a 1500 Å thickness of silicon monoxide, 500 Å of aluminum for the source-drain electrodes, and cadmium selenide for the n-type devices. This generation showed less gate to drain and gate to source shorts than the first generation. The problem with this generation was gate to source and gate to drain capacitance. The gate aluminum for this generation was 1000 Å thick, and the definition was not sharp. The electrodes on the gate mask were too wide. The wide mask and the poor definition combined to cause a large overlay capacitance, which probably prevented devices from functioning properly.

The third generation of devices was fabricated using the parameters given in Table I. To reduce the gate overlay capacitance, the gate was made noticeably narrower than the length of the channel. To facilitate this, the channel lengths were made large. The only problem seen with the devices was instability in the gate oxide. The characteristics appeared to have a severe case of ionic drift and slow trapping (24). These curves show hysteresis loops and sharp rises at the end of the curve when displayed on a curve tracer. Despite these instabilities, the saturation current at various gate potentials was measured. From this data, the mobility could be measured. The data appears in Table II.
Table II: N-type Device Data

<table>
<thead>
<tr>
<th>$V_{gn}$ (volts)</th>
<th>$I_{dn,sat}$ (μA)</th>
<th>calculated $\mu_n$ ($\frac{cm^2}{V\cdot sec}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>3.0</td>
<td>51.90</td>
</tr>
<tr>
<td>4</td>
<td>5.5</td>
<td>23.80</td>
</tr>
<tr>
<td>6</td>
<td>7.3</td>
<td>14.03</td>
</tr>
<tr>
<td>8</td>
<td>8.8</td>
<td>9.50</td>
</tr>
<tr>
<td>10</td>
<td>10.0</td>
<td>6.92</td>
</tr>
</tbody>
</table>

Table III: P-type Device Data

<table>
<thead>
<tr>
<th>$V_{gn}$ (volts)</th>
<th>$I_{dn,sat}$ (μA)</th>
<th>calculated $\mu_n$ ($\frac{cm^2}{V\cdot sec}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>2.4</td>
<td>55.4</td>
</tr>
<tr>
<td>4</td>
<td>4.4</td>
<td>25.4</td>
</tr>
<tr>
<td>6</td>
<td>5.8</td>
<td>14.9</td>
</tr>
<tr>
<td>8</td>
<td>7.0</td>
<td>10.1</td>
</tr>
<tr>
<td>10</td>
<td>7.8</td>
<td>7.2</td>
</tr>
</tbody>
</table>
The data was taken from an n-type device with $w_n$ of 0.24 cm and $L_n$ of 0.24 cm. The mobility can be determined by using equation (15). The same data for a p-type device is shown in Table III. The p-type device has a $w_p$ of 0.24 cm and $L_p$ of 0.32 cm. All the data was taken with a drain voltage of five volts. The calculated mobilities decrease with increasing gate voltage. This mobility modulation has been explained as a change in the effective number of scattering centers (25). At low gate potential, the traps are occupied by carriers, raising the effective mobility. At higher gate potentials, these traps are emptied and the effective mobility is lowered.

Two inverters were fabricated using the third generation processing. One inverter had the gate electrode misaligned, and the gate shorted to the drain when voltage was applied. The other inverter showed some effects of ionic charge in the gate oxide, however, some data was obtained. With the supply voltage at five volts, the fall time was measured at 60 microseconds and the rise time at 40 microseconds. These measurements were made with a capacitive load of 47 pf. It should be noted that the output of the inverter was not exactly the inverted input. The output, when the input was zero, was about 1.8 volts. The reason for this was probably the narrow gate electrode, leaving a section of high resistivity semiconductor on each side, causing a voltage drop
between the supply and the output. When the input went high, the output went to the input voltage. This can be attributed to conduction through the oxide of the n-type device drain-source. Despite these problems, the output capacitor still has to discharge, on its falling edge, through the p-type device. Using equation (29), the calculated time should correspond to the fall time measured. The output capacitor was probably charged through the n-channel gate oxide, so the rise time measured can not be predicted. Using equation (29), the device dimensions, \( w_p = 0.24 \text{ cm} \) and \( L_p = 0.32 \text{ cm} \), and the mobility calculated in Table III, the calculated delay time is 29 microseconds. The difference between this value and the measured value of 60 microseconds is probably due to stray capacitance and the areas of semiconductor not covered by the gate electrode.

To further test the proposed process, the two discrete devices, which gave the characteristics of Table II and Table III, were connected externally into an inverter and tested. Using this configuration, the inverter functioned. The measured time for the output to fall was 80 microseconds and the measured rise time was 60 microseconds. The load was 20 pf, the supply voltage was 5.0 volts, and the input pulse was a 5 kilohertz square wave of 5 volts. Using these values and the mobility from Table II the
calculated fall time, from equation 25, is 14 microseconds. The rise time, using the transistor parameter from Table III, can be calculated as 18 microseconds. The difference between the calculated value and the measured value was caused mainly by the fact that the inverter was not integrated. The two devices had to be interconnected using external wiring, which added stray capacitance to the circuit.
CHAPTER VIII
CONCLUSION

From this work the following conclusions can be drawn:

1. Theoretically, the proposed thin film process can equal the existing silicon on sapphire process in speed and power consumption with some modifications. The modifications are a higher dielectric constant for the gate oxide and a higher mobility in the n-type semiconductor. The higher dielectric constant may be obtained by backfilling the chamber with oxygen during the silicon monoxide deposition. The higher mobility may be obtained by slowing the deposition of the cadmium selenide.

2. To improve the characteristics of experimental units, two improvements must be made. The first is to deposit a cleaner oxide. The second is to improve the alignment procedure for the gate aluminum.

The proposed process offers a low cost, low leakage, low temperature alternative to silicon on sapphire with all the advantages of a semiconductor on insulator process.


