THE DESIGN AND IMPLEMENTATION OF
A MICROCOMPUTER CONTROLLED CCD
CLOCK DRIVER

AT OHIO UNIVERSITY,

A Thesis Presented to
The Faculty of the College of Engineering and Technology
Ohio University

In Partial Fulfillment
of the Requirements for the Degree
Master of Science

by
Joseph Yuh-Shan Pai,
November 1985

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ACKNOWLEDGMENT

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ABSTRACT

The purpose of this thesis is to design and to implement a microcomputer controlled CCD testing circuit which can investigate the performance characteristics of a CCD, such as the effects of background noise, charge trapping effects, and transfer efficiency. This thesis is a design for the driver of the CCD121H charged-coupled device. It is able to supply variable period clocks with adjustable voltage levels and different rise and fall times for the CCD inputs to obtain very flexible test conditions.
INTRODUCTION

The CCD121H is a monolithic self-scanned 1728 Element Image Sensor designed for page scanning applications. The device provides a 200 line per inch resolution across an 8-1/2 inch page. In addition to a row of 1728 sensing elements, the CCD121H chip includes: two charge transfer gates, two 2-phase analog shift registers, an output charge detector/preamplifier, and a compensation output amplifier. It operates with two transfer gate clocks (\(gxa\) and \(gxb\)), two 2-phase shift register clocks (\(\phi_{a1}\), \(\phi_{b1}\), \(\phi_{2a}\), and \(\phi_{2b}\)), and a reset clock (\(\phi_r\)). There are also two clocks (TP2 and TP4) which control the electrical injection of charge into the shift registers. The photon generated electrons are accumulated in the sensing elements, the transfer gate clocks move the accumulated charges from the sensing elements to the CCD shift registers, whose 2-phase clocks in turn shift the charge packets to the output charge detector/preamplifier. Before each new charge packet is sensed, a high level reset clock turns on an MOS reset transistor to return the output voltage to a base level. After that, the preamplifier provides a signal voltage proportional to the size of each charge packet.

In order to investigate the CCD's performance
characteristics, all the clock rates and levels should be variable. The rise time and fall time of $\alpha_a$, $\alpha_b$, $\alpha_1$, and $\alpha_2$ will also be variable. In Chapter 2, the basic ideas of the operation of CCD's are discussed. The requirements of the testing circuit, the specifications of the CCD121H, and the block diagram of the system are described in Chapter 3. The description and operation of the controlling microcomputer MPF-1 will be introduced in Chapter 4. In Chapter 5, we have the description and circuitry of the clocks $\alpha_a$ and $\alpha_b$, and their timing diagrams. The content of Chapter 6 is a description of the timing diagrams of $\alpha_1$, $\alpha_2$, $\alpha_r$, and $\alpha_{sh}$, the circuitry for their generation, and limitations of the clocks. Charge injection for the CCD121H, a timing diagram of TP2 and TP4, and the generation circuit for these clocks is discussed in Chapter 7. The softwares for system control is described in detail in Chapter 8.

The objective of the testing system is to control the clocks by software. The microcomputer can be programmed externally, and it can dynamically change parameters on its own to meet different needs. The microcomputer sets data to control the timing circuit which can generate variable clocks to operate the CCD. Besides this, the microcomputer can start and stop the clocks. When the system is operated, its ROM program will get the initial values and output them to the
output port buffers which are connected to the testing circuit so that the testing circuit can generate variable clocks. Additionally, a "STOP" program is able to stop all the clocks except \( O1, O2, Or, \) and \( Osh. \) In total there are three types of signals controlled by software:

1. normal type (no background charge)
2. both (video information with background charge)
3. stop type (no video or background charge—only dark current)

This work is a continuation of that described in Townsend's thesis [Ref. 1-1]. In that thesis, a microprocessor controller for a CCD was outlined but the hardware was never built. That design had some difficulties:

1. There was an analog delay built in which made \( Oxa \) and \( Oxb \) loose synchronism with the master clock.
2. The upper frequency of \( O2 \) was only 250 KHz.
3. The reset clock, \( Or \), was not synchronized with \( O2 \) properly.
4. The microcomputer is not free for an operation during a run so that it can not vary any preset data, or change any operation during processing.

The CCD test station designed in this thesis does not have these difficulties. The circuit described here was built and performed as expected.
INTRODUCTION TO CCD's

INTRODUCTION

Charge Coupling is a simple but extremely powerful concept. The idea of it consists of storing electrons (or holes) in potential wells created at the surface of a doped semiconductor and moving this charge as a packet across the surface by the controlled movement of potential wells. The charge packets can then be detected at the output via the voltage change caused by putting the charge on a capacitor.

The charge-coupled device can be constructed as a surface channel device (SCCD) or as a buried channel device (BCCD), as shown in Figure 2.1(a) and Figure 2.2(a) respectively. The empty potential well with depth Øso of the SCCD is formed at the semiconductor-insulator interface under the electrode as shown in Figure 2.1(b). If charge is collected in the potential well, the potential well will be partially filled to Øs as shown in Figure 2.1(c). In contrast, the BCCD forms a well below the silicon surface. The energy band for an empty well is as shown in Figure 2.2(b) and for a charged well is as shown in Figure 2.2(c). A BCCD does not require a fat zero bias charge for high efficiency [Ref. 2-1], does not exhibit noise caused by the trapping of charge by the fast interface states, and has
Figure 2.1 (a.) A surface-channel CCD.

(b.) Band-bending at deep depletion with an empty potential-well.

(c.) Partially filled potential-well representation.
Figure 2.2 (a.) A buried-channel CCD.

(b.) Energy bands for an empty well.

(c.) This changes markedly when signal charge is presented.
a higher frequency response than a SCCD with the same dimensions. As with most other IC's, noise represents an important consideration in the evaluation of image CCD's. Therefore, the CCD121H is manufactured using buried channel technology.

OPERATION OF A CCD

A CCD is a simple device which is a shift register formed by a string of these closely spaced MOS capacitors. The MOS capacitors, pulsed by a multiphase clock voltage, form potential wells which are at or near a silicon-silicon dioxide interface. For a two-phase, N channel CCD, the charges transferred between potential wells are electrons. A two-phase CCD can be constructed as shown in Figure 2.3(a). Such two-phase CCD's consist of separate storage and barrier gates connected to a common clock voltage.

To illustrate the operation, assume initially we are at t1 with neither clock high. The charge is in a well under $\phi_1$. A positive step voltage $\phi_2$ to a gate electrode at time t2 forms a depletion region in the P-type silicon beneath the gate so that a minimum of electron energy—a potential well—exists at the Si-SiO$_2$ interface (Figure 2.3(b)). Charges transfer from wells under the $\phi_1$ electrodes to wells under $\phi_2$ because of the surface potential changes due to clocking as shown in Figure 2.3(c). After one complete clock cycle,
Figure 2.3 Two-phase drop-clock operation uses non-overlapping clock pulses.
the charge pattern has moved one stage to the right. Note that the clocks are overlapping pulses on the transition in this case. Of course, to be useful, means must be provided to introduce charge into the CCD register and then to detect signals at the output.

BACKGROUND CHARGE AND NOISE

Background charge may either be electrically generated at the input as "fat zeros" to suppress fast interface state losses or it may be generated thermally or optically via bias light. The dark current or thermally generated background charge can be measured: (1) either directly as the (average) Reset Drain current during the continuous operation of a CCD, or (2) the CCD clock can be periodically stopped for a fixed integration time while the thermally generated charge is collected. The clocks are then cycled and the dark current profile is read-out and detected.

Dark current background levels as low as 5 to 10 nA/cm² have been reported [Ref. 2-2]. However, the control of dark current and dark current spikes is still one of the more critical aspects of CCD manufacture. Note that the BCCD has a higher dark current than the SCCD.

CHARGE TRAPPING EFFECTS

Charges can be lost from the signal into fast
interface states, because the filling rate of these states is proportional to the number of free carriers and the emptying rate depends only upon their energy level. Thus, even though a roughly equal amount of time is available for filling and for emptying, many of the interface states can fill much faster than they can empty, and thus retain some of the signal charge which they release into trailing signal packets. On the average, then, there will be no net loss of charge into fast states. However, there will be fluctuations in the total number of carriers trapped at any instant of time. These fluctuations will be reflected in the free charge in the potential well, and hence in the output. Further, the fluctuation in the number of carriers in the charge packet will reflect the fluctuations in the trapped charge twice at each gate—once when the packet is transferred in and once when it is transferred out.

TRANSFER EFFICIENCY

The transfer efficiency, \( e \), which is defined as the ratio of transferred charge to initial charge in one transfer, depends on two factors: how fast the free charge can transfer between adjacent gates and how much of the charge gets trapped at each gate location by stationary states. If a single charge pulse with an initial amplitude \( P_0 \) is transferred down a CCD register,
after n transfers the amplitude $P_n$ will be:

$$P_n = P_0 \times e^n = P_0 \times (1-n\epsilon)$$

for small $\epsilon$, where $e=1-\epsilon$

The trapping of charge by the interface states can be avoided by means of buried channel construction. In buried channel CCD's small trapping type transfer losses have also been observed and are attributed to charge trapping by stationary buried states.

APPLICATIONS OF CCD's

The following are some of the applications of CCD's:

1. CCD image sensors are used as low-power, solid-state replacements of the vidicon-type tube for video camera applications. They have the advantages of high resolution, low thermal noise, low light level performance, flat spectral response (high sensitivity to blue as well as red light), and low cost. [Ref. 2-3]

2. Today, several different CCD memory IC's have been demonstrated. CCD's are inherently serial devices, so in a sense they functionally resemble disks except that they are volatile. A related device is the non-volatile charge-addressed memory (NOVCAM). For CCD dynamic serial memories, the major emphases of future development will be lower cost per bit and higher performance than that of MOS RAM's, magnetic bubbles,
etc. [Ref. 2-4]

3. At the outset, CCD's are inherently analog devices. The applications for CCD's in analog signal processing are ideally suited to performing sampled data filtering functions in the analog domain. [Ref. 2-5]
CHAPTER 3
THE REQUIREMENTS OF A MICROCOMPUTER CONTROLLED CCD TEST STATION

This Chapter is divided into 6 parts. Part 1 introduces the specifications of the CCD121H. Part 2 presents the definition of the required DC voltage levels; the remaining clock levels will be dealt with in Part 3. Part 4 discusses the gated charge amplifiers. Electrical injection action is described in Part 5. One important section is Part 6; it gives the specifications of the system.

THE CCD121H SPECIFICATIONS

The CCD121H consists of the following functional elements (see Appendix A):

1.) Image Sensor Elements-- A row of 1728 image sensor elements separated by diffused channel stops and covered by a silicon photogate. The amount of charge accumulated is a linear function of the incident illumination intensity and the integration period.

2.) Two Transfer Gates-- Gate structures adjacent to the row of Image Sensor Elements. Alternating charge packets are transferred to the right and left (A and B) analog transport shift registers via the transfer gates.
at the HIGH states of Øxa and Øxb.

3.) Two 866-BIT Analog Shift Registers-- The two registers are used to move the light generated charge packets serially to the charge detector/preamplifier via the transport clocks Ø1a, Ø2a, Ø1b, and Ø2b.

4.) A Gated Charge Detector/Preamplifier-- A precharged diode whose potential changes linearly in response to the quantity of the signal charge delivered is used to supply a potential to the gate of the output N-channel MOS transistor. The MOS transistor produces a signal output at OS and the reset transistor which is driven by a reset clock (Ør) recharges the diode capacitor before the arrival of each new signal charge packet from the transport registers.

The DC characteristics, timing diagram of drive signals, clock characteristics, and AC characteristics are shown in Appendix A-- The data sheet of the CCD121H.

DEFINITION OF DC VOLTAGE LEVELS

Vrd-- The reset drain voltage which establishes the reset level on the output collection capacitor prior to receipt of signal charge. The operating level of Vrd is normally 12 ± 1% V.

Vod-- The output drain voltage is normally operated at 15 V. The gain of the output amplifier will be changed when Vod is varied. Vod can be as high as 18 V.
Vog-- The output gate voltage can be set between 5.0 and 6.0 V. Since OG is directly coupled to the output, the noise specification is stringent and additional filtering close to the array is used as shown in Figure 3.1.

Vpg-- The photogate voltage establishes the depth of the potential well in the photosite area. Normally, it is set at 10 V.

TP1 and TP3-- The input gates meter the electrical injection charge. The test point gates are not used in most applications and are normally grounded to Vss. However, when electrical injection is to be operated, TP1 and TP3 must have a voltage between 0 and 5 V.

The circuit for Vog, Vpg, Vrd, Vod, TP1, and TP3 were not actually built in this work. Efforts were concentrated on the clocks.

CLOCK LEVELS

Øxa and Øxb-- The transfer gate clocks are to move the accumulated charge from the image sensor elements to the CCD shift registers. The HIGH level is $8 \pm 0.5$ V and the LOW level is $0.5 \pm 0.3$ V.

Ø1 and Ø2-- The analog shift register transport clocks are two sets of 2-phase clocks which are applied to the gates of the CCD shift registers to move the charge packets to the gated charge-detecting preamplifier. The high and low levels are the same as
Figure 3.1 The filtering of Vog.

Figure 3.2 Gated charge amplifier.
Øxa and Øxb.

Ør-- The high level of the Reset Clock must be high enough to saturate the reset transistor. It turns the FET on at its high level of 8 volts, and off at the low level of 0 ± .5 volts.

TP2 and TP4-- The electrical injection clocks which control the electrical injection of charge into the shift registers. These clocks will be synchronized with Ør and must be active low. The high level is 15 ± 0.5 V and the low level is 5 ± 0.5 V.

GATED CHARGE AMPLIFIERS

Gated charge amplifier (GCA)-- A GCA consists of a charge collection capacitor, an MOS transistor buffer, and an MOS reset transistor. It is as shown in Figure 3.2.

Output Amplifier (OA)-- An OA is used to amplify the buffered output as shown in Figure 3.2. Figure 3.3 shows the OA and the relation of video output from it to Ør.

INJECTION ACTION

Figure 3.4 shows the action of electrical injection. Figure 3.4(a) shows when TP2 is high (say at 15 V), Ø1b is low (say 0.5 V) and Ø2b is high (say 8 V). All electrons are pulled out of the silicon beneath TP2. When TP2 is pulsed low to a 5 V level, Ø1b is still held
Figure 3.3 The output amplifier and the timing diagram of video output with $\theta_r$. Capacitive feed-through from $C_{gs}$ of reset transistor.
low. TP2 is pushed low discharging its capacitance and flooding the area with electrons. The electrons will fill the well formed by TP1 as shown in Figure 3.4(b). In Figure 3.4(c), TP2 is high again (at 15 V) and Q1b is still low. The electrons are stored in the well formed by TP1 and extra electrons are pulled out of the silicon by TP2. Now, TP2 is high, Q1b becomes high (say 8 V), and Q2b changes to low (say 0.5 V). The trapped electrons are injected into the shift register as shown in Figure 3.4(d). TP2 is still high, Q1b changes to low, and Q2b becomes high. The trapped electrons will be transferred to the next shift register site. This is shown in Figure 3.4(e). For the other side, it is same action for TP4, TP3, Q2a, and Q1a. [Ref. 3-1]

Figure 3.5 shows the pulse synchronization for TP2 and TP4. TP2 is active low when Q2 is high and TP4 is active low when Q1 is high. The pulse widths of TP2 and TP4 are fixed and less than the minimum width of Q1 and Q2.

THE SPECIFICATIONS OF THE SYSTEM

1.) It generates ten clocks which are the transfer gate clocks (Qxa and Qxb), the shift register clocks (Q1a, Q2a, Q1b, and Q2b), the reset clock (Qr), the sample-&-hold clock (Qsh), and the injection clocks (TP2 and TP4).
Figure 3.4 The action of electrical injection.

(same action for TP4, TP3, Ø2a, and Ø1a).
Figure 3.5 Pulse synchronization for TP2 and TP4.
2.) Varies the periods of \( \theta x, \theta x b, \theta 1a, \theta 2a, \theta 1b, \) and \( \theta 2b. \)

3.) Changes the high and low levels of \( \theta x, \theta 1, \) and \( \theta 2. \)

4.) Varies the rise time and fall time of \( \theta x, \theta 1, \) and \( \theta 2. \)

5.) Synchronizes \( \theta r \) and \( \theta sh \) with \( \theta 1 \) and \( \theta 2. \)

6.) Synchronizes TP2 and TP4 with \( \theta r. \)

7.) Varies the read-out ratio \{Note 1\} of the video output.

\{Note 1\} The read-out ratio is the number of sets of 1730 video output pixels. For example, if we set 5 for the read-out ratio, the first set of 1730 pixels contains valid video information, and the remaining 4 sets of 1730 pixels are blank.
CHAPTER 4

THE SYSTEM MICROCOMPUTER : THE MPF-1

This Chapter introduces the MPF-1 microcomputer which controls the testing system to operate in 3 modes. One is the normal operation to output an optical signal with no electrical injection, the second is to operate with electrical injection, and the last one is to inhibit both optical output and electrical injection. In the first part of this Chapter, the hardware of the MPF-1 is introduced. The memory size and memory map is described in the second part. The last part is about the input and output ports. The remaining software specifications and microcomputer schematic are shown in Appendix B.

The MPF-1 singleboard microcomputer is used for the system for the following reasons:

1.) It is low cost.
2.) It has a fully functional keyboard.
3.) It can be directly read by a 4-digit hexadecimal address field and displays a 2-digit hexadecimal data field.
4.) It has high speed operation.
5.) It is small and easy to connect to the test circuit.
HARDWARE OF THE MPF-1

1.) The Z-80 CPU runs with a 1.79 MHz system clock.

2.) ROM area for the monitor program: $0000 -- $07FF, i.e. 2K bytes. ($XXXX means a Hexadecimal number).

3.) RAM area: $1800 -- $1FFF, 2K bytes.

4.) Memory expansion area: $2000 -- $2FFF, 4K bytes.

5.) I/O ports:
   (a.) A programmable I/O port 8255 for keyboard and display. I/O port numbers-- $00 to $03.
   (b.) A Z-80 PIO, I/O port numbers-- $80 to $83.
   (c.) A Z-80 CTC, I/O port numbers-- $40 to $43.

6.) A 6-digit display, a 36-key keyboard, and a speaker.

7.) Tape recorder interface-- can be connected to any cassette tape recorder for saving and loading programs.

8.) Only a single +5 VDC power supply needed. Power consumption is 2.5 W.

In this system, the Z-80 PIO is used as a buffer and programmed to output preset data and control signals. A block diagram of the system is shown in Figure 4.1. The A port and B port of the Z-80 PIO are programmed to be the output ports. The B port is connected to generate different pulses to buffers for latching data which are sent from the A port. The latched data represent 4 different preset values which can be from 1
Figure 4.1 Block diagram of the microcomputer controlled testing circuit.
to 15. One is for T1 and T3 generation, the second is for T2 and T4 generation, the third one is for Ø1 and Ø2 generation, and the last one is for the read-out ratio. The clock generation board will generate 7 clocks (T1, T2, T3, T4; Ø1, Ø2; and Ør) with pulse widths and frequency determined by 3 of the 4 preset values. In addition to the above 7 clocks, the clock generation board also supplies a sample-&-hold clock (Øsh) and the electrical injection clocks (TP2 and TP4). The read-out ratio of the video output is given by the last preset value.

Since the levels of the clocks of the CCD121H are not TTL compatible, we need the clock drivers to supply the high levels from 7 to 9 V and the low levels from 0.8 to 3 V to the CCD121H. The rise time and fall time of the clocks are also controlled by the clock drivers. When all the signals of the CCD121H are present, the device will be able to produce a video signal which can be digitized and stored.

For the operation with electrical injection, we need the Z-80 CTC to control the circuit. Details of this are in Chapter 7.

A control program is preserved in EPROM at location $2000 to $23FF. The preset data locations are defined at $1800, $1801, $1802, and $1803. All the software details are described in Chapter 8.
MEMORY SIZE AND THE MPF-1 MEMORY MAP

Refer to Figure 4.2, where the memory map is shown. The memory size (for user) can be either 2K-byte RAM, 4K-byte RAM, or 2K-byte RAM and 2K-byte ROM.

In this system, as Figure 4.2 shows, the area $1800 to $1FFF is the user area. However, the locations from $1F9F to $1FF3 are reserved for the monitor program; the user should not write in it.

INPUT AND OUTPUT PORTS

Figure 4.3 is the I/O addressing map:

1.) The 8255 is programmed by the monitor for controlling the keyboard, display, speaker, and tape read/write. Its control word (port $03) is set to a value of $90 so that port A is input and port B and port C are outputs. The details are as follows:

(a.) Port A of 8255:

bit 7 -- tape reading serial port.
bit 6 -- for a "user key" on the keyboard which can be programmed by the operator.
bit 5 to bit 0 -- for scanning the 6x6 matrix keyboard to detect a key being pressed.

(b.) Port B of 8255:

For activating the seven segment and decimal point of the LED display.
<table>
<thead>
<tr>
<th>Address</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$FFFF</td>
<td>Non-decoded</td>
</tr>
<tr>
<td></td>
<td>Not used.</td>
</tr>
<tr>
<td>$2800-$27FF</td>
<td>Expandable area for RAM or ROM.</td>
</tr>
<tr>
<td>$2000-$1FF</td>
<td>User RAM.</td>
</tr>
<tr>
<td>$1800-$17FF</td>
<td>Decoded Not used.</td>
</tr>
<tr>
<td>$0800-$07FF</td>
<td>EPROM Monitor.</td>
</tr>
<tr>
<td>$0000</td>
<td>Monitor.</td>
</tr>
</tbody>
</table>

Figure 4.2 Memory map for the system.
Figure 4.3 Input and Output addressing map.

<table>
<thead>
<tr>
<th>CB</th>
<th>CA</th>
<th>DB</th>
<th>DA</th>
<th>CTC</th>
<th>CTC</th>
<th>CTC</th>
<th>CTRL</th>
<th>C</th>
<th>B</th>
<th>A</th>
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<tr>
<td>Z-80 PIO</td>
<td>Z-80 CTC</td>
<td>8255</td>
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<td></td>
<td></td>
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</tr>
</tbody>
</table>

Figure 4.4 Port B of the 8255 and the seven segment LED display.
It is shown in Figure 4.4.

(c.) Port C of 8255:

bit 7-- tape writing serial port.
bit 6-- programmed by the monitor to execute single step and set break point.
bit 5 to bit 0-- multiplexes the 6-LED display.

It acts as a ring counter putting out a single 0.

2.) The CTC can be programmed by a user as a timer or a count-down counter. In this testing system, the CTC is programmed as a count-down counter to control the electrical injection operation. This is described in Chapter 7.

3.) The PIO can be programmed by a user. In this system, it is used as a buffer which is connected to two 74LS374 chips and one 74LS373 (for data or signal latching and driving). Port A and port B of the PIO are programmed to be outputs

Refer back to Figure 4.1. The MPF-1 has three kinds of control programs to operate three types of signals. The first one is the normal type: preset data and control signals are sent through the Z-80 PIO to TTL circuits which generate $\text{x}$, $\text{y}$, $\text{z}$, $\text{a}$, $\text{b}$, $\text{c}$, $\text{d}$, $\text{e}$, $\text{f}$, and $\text{g}$ to operate the CCD121H with no injection. With the second type of signal, both the CTC and PIO are programmed.
CTC is a count-down counter and the PIO is used as an output. After $\phi_a$ and $\phi_b$ are generated and a defined number of blank pixels have come out, we begin to introduce electrical charges into the shift registers. This control program can generate $\phi_a$, $\phi_b$, $\phi_1$, $\phi_2$, $\phi_r$, $\phi_{sh}$, and some preset number of TP2 and TP4 pulses. The last control program is the stop type, which only generates $\phi_1$, $\phi_2$, $\phi_r$, and $\phi_{sh}$.

The generation of $\phi_a$ and $\phi_b$ is discussed in Chapter 5. $\phi_1$, $\phi_2$, $\phi_r$, and $\phi_{sh}$ are described in Chapter 6. TP2 and TP4 (electrical injection) are presented in Chapter 7. Chapter 8 gives the software. Finally, Chapter 9 describes the performance of the system.
CHAPTER 5

DESCRIPTION AND OPERATION OF $\phi xa$ and $\phi xb$

This chapter discusses the generation of $\phi xa$, $\phi xb$, the design ideas, the requirements, and the circuit.

THE REQUIREMENTS AND DESIGN IDEAS

In order to investigate the effects of background noise, charge trapping, and transfer efficiencies, we would like to vary $\phi xa$ and $\phi xb$. The specifications for the CCD121H are given in Appendix A. The limits on the parameters are given below.

1.) Refer to Figure 5.1.
   
   $1.0 \mu s \leq t1 \leq 15 \mu s$
   
   $.5 \mu s \leq t2 \leq 7.5 \mu s$

   For the CCD121H, the minimum times are
   
   $t1 \geq 0.8 \mu s$

   $t2 \geq 0.1 \mu s$

2.) Variable HIGH levels of $\phi xa$ and $\phi xb\rightarrow V(H)$
   
   $+7 \, V \leq V(H) \leq +9 \, V$

   Variable LOW levels of $\phi xa$ and $\phi xb\rightarrow V(L)$
   
   $+0.8 \, V \leq V(L) \leq +3 \, V$

   Typically $V(H) = +8 \, V$

   $V(L) = +0.8 \, V$

3.) The rise time ($Tr$) and fall time ($Tf$)
   
   $600 \, ns \leq Tr \leq 1400 \, ns$
Figure 5.1 Timing diagram for T1 to T4, \( \varphi_1 \), \( \varphi_2 \), \( \varphi_{xa} \), and \( \varphi_{xb} \).
100 ns \leq T_f \leq 800 ns
with 500 pfd to 1000 pfd capacitance loading.

Tr does not necessarily equal Tf.

DESCRIPTION OF Øxa AND Øxb GENERATION

Figure 5.2 shows the simplified block diagram of the circuit used to generate Øxa and Øxb. Two signals N* and R* to be discussed in Chapter 6 activate the board: the N* signal means "next" and the R* signal means "reset". In this Figure, the Variable Frequency Generation Board (VFGB) generates 4 variable clocks labelled from T1 to T4. This is the main topic of this section. A timing diagram for the transfer gate clocks (Øxa and Øxb) and the shift register clocks (Ø1 and Ø2) is shown in Figure 5.1. This tells us when Øxa and Øxb are active, Ø1 and Ø2 should be held at a HIGH level and a LOW level, respectively. T1 is used to generate Øxa. Its period is the pulse width of Øxa. T2 is used as a delay time. After the period of T2, T3 is generated. Analogous to T1, it is used to generate Øxb and its period is the pulse width of Øxb. T4 is also a delay time. After the period of T4, Ø1 and Ø2 can be restarted.

The master crystal oscillator outputs a 1 MHz and a 2 MHz clock to the VFGB. The 1 MHz clock is connected to VFG-1 and VFG-3. It is the time-base of T1 and T3.
Figure 5.2 The block diagram of $\phi_{xa}$ and $\phi_{xb}$ generation.
In the same way, the 2 MHz clock is connected to VFG-2 and VFG-4. It is the time-base of T2 and T4. A 4-bit value from 1 to 15 is sent from the microcomputer buffer to VFG-1 and VFG-3 to generate 2 variable pulses on T1 and T3. Their widths both are the same: t1. Similarly, another 4-bit value from 1 to 15 is sent from the microcomputer to VFG-2 and VFG-4 to generate 2 more variable pulses on T2 and T4. Their widths are equal and set at t2. T1 and T3 will be used as the triggers for Øxa and Øxb generation. These clocks are TTL compatible levels. T1 and T3 are passed to Øxa and Øxb drivers which will be discussed later. The drivers reproduce Øxa and Øxb at higher voltage levels for CCD operation.

In Figure 5.2, the start signal S* from the microcomputer buffer will trigger VFG-1 to generate the T1 pulse which width t1 is varied by the preset 4-bit value. When pulse T1 goes from HIGH to LOW, it will trigger VFG-2 to generate the T2 pulse which width t2 is also varied by another preset 4-bit value. After T2 is generated, VFG-2 will trigger VFG-3 to generate the T3 pulse which has the same width as the T1 pulse. Shortly after T3 generation has finished, VFG-3 will trigger VFG-4 to generate the pulse T4. Its width is the same as pulse T2. A timing diagram for pulses T1 to T4 is shown in Figure 5.3.
Figure 5.3 The relationship of \( S^* \), \( R^* \), and 

\( T_1 \) to \( T_4 \).
The S* signal is to trigger VFG-1 to generate pulse T1 and to set Ø1 to the HIGH level (Ø2 to the LOW level). After pulse T4 is generated, VFG-4 will send a R* signal (reset) to enable Ø1 and Ø2. (This will be discussed in Chapter 6). In other words, S* is a signal to stop the shift registers when charge packets are being transferred to them and R* is a signal to begin the shifting when charge packets have been transferred.

t1 is the width of Øxa and Øxb. t2 is the delay time between Øxa and Øxb and also the delay time between Øxb and the enabling of Ø1 and Ø2. (Refer to Figure 5.1 and Figure 5.3). Therefore, we feed T1 and T3 into the Øxa and Øxb drivers to generate Øxa and Øxb for the CCD.

After R* is sent out, Ø1 and Ø2 again transfer the charge packets to the output preamplifier. The number of Ør pulses is counted by a counter. In other words, the number of pixels is counted. If the number of Ør pulses reaches 1730, the read-out ratio counter will be counted down by 1. (1730 = 1728 pixels of a frame in the CCD121H + 2 blanks). If the read-out ratio counter counts down to 0, a signal N* (discussed in Chapter 6) will be sent back to the VFGB to re-trigger VFG-1 which will generate pulse T1 and trigger VFG-2 to repeat the operation.
EXPLANATION OF THE CIRCUIT

The variable frequency generation board (VFGB):

(Refer back to Figure 5.1 and Figure 5.3 for the timing diagrams.) The circuit of the variable frequency generation board is shown in Figure 5.4. A 10 MHz crystal and four 74LS04 inverters are arranged to generate a 10 MHz clock. The 10 MHz clock is put into a 74LS90 (U5, divide-by-10 counter). Therefore, a 2 MHz clock is derived from Qb (pin 9) and a 1 MHz clock is gotten from Qd (pin 11). The timing diagram of these clocks is shown as Figure 5.5. The 1 MHz clock is connected to U7 and U17 (74LS169, binary, down counters) which are variable period controllers of pulses T1 and T3. Similarly, the 2 MHz clock is the time-base of U12 and U22 (74LS169) which are variable period controllers of pulses T2 and T4.

The A-port of the Z-80 PIO will output an 8-bit value to the buffer 74LS374 (U53) which is triggered to hold the data by a positive pulse sent by b0 of the Z-80 PIO. One of the two 4-bit values will be passed to the D to A IN pins (pins 6 to 3) of U7 and U17 as the input data. The other will be sent to the D to A IN pins (6 to 3) of U12 and U22.

A block diagram and timing diagram of the operation is shown in Figure 5.6. In the beginning, N* and R* are HIGH. b7 of the Z-80 PIO is LOW. (This means that S*


Figure 5.4 The Circuit of the $\varnothing x$ section of the Variable Frequency Generation Board.
Figure 5.5 Timing diagram of U5 (74LS90).
Figure 5.6 The block diagram and timing diagram of T1 generation.
is LOW). The initial states of Q' of all 74LS123's are high, RCO of all 74LS169's are high, the Q output of each 74LS74 is low (Q' is high), and the enables (pin 7 and 10) of all 74LS169's are held at high (this means all 74LS169's stop counting). Since Q of all 74LS74's are low, T1 to T4 are low. When the program in EPROM begins to execute, b7 of the Z-80 PIO is set to HIGH (1). A low-to-high trigger is transferred to pin 2 (positive trigger input) of U6 (74LS123, one-shot generator) to generate a negative pulse from pin 4 (Q') of U6. (Refer to the data sheet in Appendix C.) The negative pulse is connected to pin 4 (PR) of U10 (74LS74, D flip-flop) to set the Q of U10 from 0 to 1, so pin 3 of U26 (AND gate) will be changed from 0 to 1, generating the start of pulse T1.

Since pin 1 of U7 (U/D count of 74LS169) is grounded and pins 10 and 7 (enables of 74LS169) are held LOW by the Q output (pin 5) of U10, U7 (74LS169, count-down counter) begins to count-down from the preset value. When the count-down reaches 0, pin 15 of U7 (borrow output RCO) will go LOW. As a result, the CLR (pin 1) of U10 will be LOW and the Q (pin 5) of U10 will be cleared to 0. Thus pins 10 and 7 of U7 (enables) will be HIGH to stop U7 counting, pin 9 of U7 (Load) will be LOW to load the input data presented at the pins 3 to 6 (data in) of U7, and consequently pin 15 of U7 will be
HIGH again. At the same time, pin 2 of U26 (input of AND gate) goes LOW to set T1 from HIGH to LOW. Thus the pulse T1 is generated on pin 3 of U26. The pulse T2 is triggered at the same time T1 is ended.

As mentioned above, when pin 15 of U7 became HIGH from LOW, a 0-to-1 trigger is passed to pin 10 of U11 (positive-trigger of 74LS123—the 74LS123 is a dual one-shot package) to generate a negative pulse from pin 12 of U11 (Q'of the 74LS123). This negative pulse enables the PR of U15 (pin 10, preset of 74LS74; the 74LS74 is a dual D flip-flop package) to set pin 9 of U15 (Q of the 74LS74) to 1. Because pin 5 of U27 is HIGH and pin 4 of U27 goes HIGH, T2 (pin 6 of U27) will be changed from LOW to HIGH and U12 (74LS169) will begin to count-down. After the count-down of U12 reaches 0, the RCO (pin 15) of U12 will clear the Q (pin 9) of U15 so that T2 will be changed to LOW from HIGH. Therefore, T2 is finished on pin 6 of U27 and U16 (74LS123) is triggered. The same operations are repeated, so T3 and T4 will be obtained on pin 8 of U28 and pin 11 of U29, respectively.

The preset value can be from 1 to 15. The count-down scale for t1 is 1 µs and for t2 it is 0.5 µs, so that widths of pulses T1 and T3 are from 1 to 15 µs and the widths of pulses T2 and T4 are from 0.5 to 7.5 µs.
Øxa and Øxb Drivers:

Because the HIGH level voltage for the CCD121H operation is not TTL compatible, we need to have drivers to supply the HIGH level voltage. In addition, we also need the drivers to vary the rise time and fall time of Øxa and Øxb. The drivers for Øxa and Øxb are shown in Figure 5.7.

T1 is put into the 7407 (an open-collector non-inverting high voltage driver). When T1 is LOW, pin 2 of the 7407 will be LOW (VL), Q1 will be ON, and Q2 will be OFF. Therefore, the low level of Øxa, Vxal, is

\[ Vxal = Vq1cb + V_{r2} + VL \]

where \( Vq1cb = \) the collector-base voltage of Q1.

\( Vr2 = \) the voltage of R2.

Since Q1 is ON, typically Vq1cb is 0.5 V.

(Assume Vq1eb = 0.7 V, Vq1ec = 0.2 V.
So \( Vq1cb = Vq1eb - Vq1ec = 0.5 \) V.)

Where Vq1eb = emitter-base voltage of Q1.

Vq1ec = emitter-collector voltage of Q1.

Let VL = 0.2 V, R2 = 0 ohm.

Vr2 = 0 V, so

\[ Vxal(L) = 0.5 + 0 + 0.2 = 0.7 \text{ V} \]

where \( Vxal(L) \) is the lowest voltage of Øxa.
Figure 5.7 φxa and φxb drivers.
If $R_2 = 500$ ohms, measurement shows $V_{r2} = 2.3$ V.

\[ V_{\text{xal}(H)} = 0.5 + 2.3 + 0.2 = 3 \text{ V} \]

where $V_{\text{xal}(H)}$ is the upper limit of the low voltage level of $\text{xal}$.

When $T_1$ is HIGH, the high level voltage ($V_H$) of pin 2 of the 7407 will equal $+V_u - I_{b2} \cdot (R_1+560)$. (Refer to Figure 5.8). Thus $Q_1$ is OFF and $Q_2$ is ON. The high level voltage of $\text{xal}$ is

\[ V_{xah} = V_u - I_{b2} \cdot (R_1+560+R_2) - V_{q2bc} \]

$V_{q2bc}$ is the base-collector voltage of $Q_2$.

$V_{q2bc}$ is positive because $Q_2$ is saturated.

When $V_u$ was set to 12 V, measurements showed that the lowest voltage of the high level of $\text{xal}$, $V_{xah}(L)$, is 7 volts

and the highest value of the high level of $\text{xal}$, $V_{xah}(H)$, is 9 volts.

We can adjust $R_1$ to change the high level of $\text{xal}$.

$T_3$ is passed to pin 3 of the 7407 to generate $\text{xb}$. It will have the same analysis as $\text{xal}$.

The general conditions of the $\text{xal}$ and $\text{xb}$ drivers are as follows:

1.) When $+V_u = 12$ V and $R_1$ ($R_3$) is adjusted, the high
Figure 5.8 Diagram shows \( I_{b2} \) and \( V_{q2bc} \).
level of $\varnothing x a$ and $\varnothing x b$ has the range 

$$7 \leq \varnothing x \leq 9 \text{ V}$$

2.) The $\varnothing x a$ ($\varnothing x b$) lower level can be changed by adjusting R2 (R4). The low level range is 

$$0.7 \leq \varnothing x \leq 3 \text{ V}$$

3.) The rise time ($T_r$) of $\varnothing x a$ and $\varnothing x b$ can be varied by adjusting R1 or R3. According to the measured values:

$$600 \leq T_r \leq 1400 \text{ nsec}$$

with a 750 pfd capacitive load.

4.) The fall time ($T_f$) of $\varnothing x a$ and $\varnothing x b$ can be varied by adjusting R2 or R4. According to the measured data:

$$100 \leq T_f \leq 800 \text{ nsec}$$

with a 750 pfd capacitive load.

This chapter has given the circuit which generates T1 to T4 and the drivers of $\varnothing x a$ and $\varnothing x b$. Complete measured data of the driver is shown in Appendix D. All relevant TTL data sheets are put in Appendix C.
CHAPTER 6
DESCRIPTION AND OPERATION OF Ø1, Ø2, Ør, AND Øsh

This chapter discusses the timing diagram of Ø1, Ø2, Ør, and Øsh, the circuit to generate them, the limits of Ø1 and Ø2, and the drivers. S*, R*, and N* referred to in Chapter 5 is described in detail in this Chapter.

TIMING DIAGRAM

A timing diagram of Ø1, Ø2, Ør, Øsh, and the video output is given in Figure 6.1.

Ø1 is obtained by inverting Ø2. The frequency of Ør is twice that of Ø1 and the pulse width of Ør is much smaller than that of Ø1. Øsh is used to sample the level of the video output and its frequency is double Ør. These four clocks are synchronized by a time-base.

In the circuit described in this thesis, the frequency range of Ø1 and Ø2 is from 39 KHz to 312.5 KHz. The minimum width of the Ø1 and Ø2 pulses is 1.6 µsec (1/(312.5 KHz*2)), so that the minimum time between two Ør pulses is also 1.6 µsec. Øsh is used to catch the HIGH and LOW levels of the video output. The maximum time for an A/D conversion must be 800 nsec (1.6 µsec/2) if the system runs this fast. In this test station, the width of Ør needs to be less than 200 nsec and Øsh must be less than 50 nsec. Figure 6.2 shows the minimum dimensions of Ø1, Ø2, Ør, and Øsh.
Figure 6.1 The timing diagram of $\phi_1$, $\phi_2$, $\phi_r$, $\phi_{sh}$, and the video output. The widths of $\phi_1$ and $\phi_2$ are adjustable. The widths of $\phi_r$ and $\phi_{sh}$ are fixed. The width of the video output is changed by $\phi_1$ and $\phi_2$. 
Figure 6.2 The minimum time in one cycle of $\phi_1$ and $\phi_2$.

$\phi_{sh}$ period $= 850$ ns.
$t = 850$ ns.

period of $\phi_r = 2 \times \phi_{sh}$ period.
period of $\phi_1 = 4 \times \phi_{sh}$ period $= 4 \times 2 \times 850$ ns $= 6.8$ $\mu$s.
GENERATION OF Ø1, Ø2, Ør, AND Øsh

This section describes the generation of the shift register clocks (Ø1 and Ø2), the reset clock (Ør), and the Sample-&-Hold clock (Øsh). In Figure 6.3, the block diagram of the circuit to generate the Ø1, Ø2, Ør, and Øsh pulses is given. Some signals have been discussed in Chapter 5 such as N*, R*, and S*. Refer back to Chapter 5, especially Figure 5.2 and Figure 5.4 for the definitions of these and their origin.

A 10 MHz time-base clock controls the variable frequency generator which outputs a variable frequency under microcomputer control. The frequency range is from 625 KHz (10 MHz/16) to 5 MHz (10 MHz/2). This is controlled by the preset 4-bit value passed from the microcomputer buffer. The resulting signal is divided by the frequency divider which will output 3 kinds of clocks. The first clock (B) is divided by 4 and will be a trigger for Øsh generation. The second clock (C) is divided by 8 and will be a trigger for Ør generation. The last one (D) is divided by 16 and will be the Ø2 clock (Ø1 is generated by inverting Ø2). Therefore, the frequency of Ør is twice Ø1 and the frequency of Øsh is twice Ør and 4 times Ø1.

A start signal S* is sent by the microcomputer (described in Chapter 5) to turn on the controller to make Ø1 HIGH and to clear the counter CTR-1. After Øxa
Figure 6.3 The block diagram for $\phi_1$, $\phi_2$, $\phi_r$, and $\phi_{sh}$ generation.
and Øxb are generated, the reset signal R\* is transferred to the controller to reset it to enable Ø1 and Ø2 and to begin the counting of counter CTR-1. The counter CTR-1 counts Ør pulses. When CTR-1 counts up to 1730, it will trigger the read-out ratio counter CTR-2 to count down 1. It will then reset itself to 0. CTR-2 is preset by a 4-bit value which is given by the microcomputer buffer. When CTR-2 counts down to 0, it will output a NEXT signal N\* to re-trigger the T1 generation described in Chapter 5. Therefore, the next cycle of Øxa and Øxb begins.

**DETAILED CIRCUIT OF Ø1, Ø2, Ør, AND Øsh**

The circuit for Ø1, Ø2, Ør, and Øsh generation is shown as Figure 6.4. The counter 74LS169 (U32) is a 4-bit binary down-counter. The 4-bit value that is present at the inputs of U32 (D to A) is used to vary an adjustable frequency output. The 10 MHz time-base derived from pin 6 of U3 (Refer back to Figure 5.4 of Chapter 5), is used to trigger the counter U32. The range of the output frequency f1 of U32 is

\[ 625 \text{ KHz} \leq f1 \leq 5 \text{MHz} \]

The output frequency of U32 is fed to the counter 74LS93 (U33) to generate the three frequencies for Øsh, Ør, and Ø1. The timing diagram of the outputs of U33 is shown in Figure 6.5.
Figure 6.4 The circuit for $\phi_1$, $\phi_2$, $\phi_r$, and $\phi_{sh}$ generation.
The output of B of U33 is used to trigger the high speed one-shot generator 74221 (U39) to generate the $\phi$sh pulse. The width of the pulse is measured to be 40 nsec which matches the sample & hold specification in the read-out system. (The 2K resister for the 74221 was chosen to get this value). The output of C of U33 is used to trigger the one-shot generator 74LS123 (U40) to generate $\phi r$. The width of the $\phi r$ pulse is set at 120 nsec. (Refer to the data sheet of the 74LS123: the 5K ohm resistor and 22 pf capacitor with the one-shot generator can generate a pulse width of around 120 nsec). For the last clock, output D of U33 is used as $\phi 2$, and $\phi 1$ is obtained from the inverse of D. $\phi 2$ is obtained from pin 10 of the 74265 (U43) and $\phi 1$ is generated from pin 9. The timing diagram for these clocks is shown as Figure 6.6.

The start signal $S^*$ from pin 3 of U30 is used as a positive-edge trigger (after activation, normally high). It triggers the 74LS74 (U34) to set the Q of U34 to 1. Thus Q' of U34 is reset to 0 and $\phi 1$ is HIGH, $\phi 2$ is LOW. U34 inhibits $\phi 1$ and $\phi 2$ during the period T1 to T4 when $\phi xa$ and $\phi xb$ are active. This is necessary to properly run a CCD. Refer back to Figure 5.4 and note that R* is the inverse of T4. After the pulse T4 is generated, the reset signal R* will be passed to pin 1 of the 74LS08 (U42) to clear the Q of U34. Thus on start-up, Q of U34
Figure 6.5 The timing diagram of U33. The positive edge of B is used to trigger U39. The positive edge of C is used to trigger U40.

Figure 6.6 The timing diagram of Øsh and Ør generation.
will go to 1 when S* went to 1 from 0, then will cycle back to 0 when R* is 1 at the end of T4. Therefore, the Q' of U34 is changed to 1 and Ø1, Ø2 are passed through the 74265. The relationship of T1 to T4 and Ø1, Ø2 is shown in Figure 6.7.

Three binary counter chips (74LS93) are used to count the number of Ør pulses. The reset value of this counter (CTR-1) is 1730 (Hexadecimal number 6C2). Ør is transferred to the Ain pin of U35 to make the three counters count up. C,B of U37, D,C of U36, and B of U35 are used to decide whether the number 1730 is reached or not: (0110 1100 0010₂ = $6C₂ = 1730$). If the number 1730 is reached, then pin 8 of U45 (8-input NAND gate) will go from 1 to 0, pin 3 of U46 (an inverter on the 74265) will swing from 0 to 1 to clear the three 74LS93 counters and pin 3 of U47 will output a 0-to-1 trigger to the CK of U38; the inputs of U45 (1 to 5) become 0's, pin 8 of U45 goes to 1, and pin 3 of U47 will be LOW again. (Refer to Figure 6.8). The read-out ratio counter 74LS169 (U38), meanwhile, will be triggered by the same 0-to-1 trigger which comes from U45 via U46 and pin 3 of U47. The counter U38 counts down by 1 from the preset 4-bit value which transferred from the microcomputer buffer. When U38 counts down to 0, pin 15 of U38 (RC0) will go LOW so that pin 2 of U48 is HIGH. Then the 10 MHz clock goes to pin 1 of U47 and loads the
Figure 6.7 The relationship of T1, T2, T3, T4, Ø1, and Ø2.
Figure 6.8 The timing diagram of U38 loading data.
4-bit value into U38 again. Therefore, a signal \( N^* \) (negative pulse) is generated and triggers the T1 generator. (Refer to Figure 6.8). The generation of T1 to T4 and \( \phi_1, \phi_2, \phi_r, \) and \( \phi_{sh} \) will be repeated. Note that the pixel counter (U35, U36, and U37) is reset at the same time that \( \phi_1 \) and \( \phi_2 \) are disabled and begins to count at the same time that \( \phi_1 \) and \( \phi_2 \) are passed through U43. The pixel counter will be reset again when pin 3 of U46 outputs a pulse.

THE LIMITS OF \( \phi_1, \phi_2, \phi_r, \) AND \( \phi_{sh} \)

By the specifications, the width of the pulse for the sample-&-hold should be 40 ± 10 nsec and the minimum conversion time of the A/D converter is 800 nsec in the read-out system. The minimum period of \( \phi_1 \) and \( \phi_2 \) should therefore be 6.8 \( \mu \)sec (refer to Figure 6.2), although they can be adjusted from 3.2 \( \mu \)sec to 26.2 \( \mu \)sec. The preset value for \( \phi_1 \) and \( \phi_2 \) should be set greater than 3 so that the A/D converter can have enough time to do the conversion.

DRIVERS FOR \( \phi_1, \phi_2, \) AND \( \phi_r \)

Figure 6.9 shows a detailed circuit for the \( \phi_1, \phi_2, \) and \( \phi_r \) drivers. The operation of this circuit is similar to that of Figure 5.7 (refer to Chapter 5).

To meet the manufacturer's specifications for the
Figure 6.9 The drivers of \( \varnothing_1, \varnothing_2, \) and \( \varnothing_r. \)

Figure 6.10 The circuit of \( \varnothing_{sh} \) inversion.
sample-&-hold circuit, the clock Øsh needs to be inverted to a positive pulse by a pair of dual 4-input NAND gates. The circuit is shown in Figure 6.10.

In Chapter 5 and 6, the clock generators for Øxa, Øxb, Ø1, Ø2, Ør, and Øsh have been discussed. They can operate the CCD121H in the normal mode of operation. We will discuss electrical injection operation in Chapter 7, and in Chapter 8, the support software will be described in detail.
CHAPTER 7

CHARGE INJECTION

Charge injection is not used in most applications of the CCD121H. However, for the testing system, we discuss the topic in this Chapter. The first part tells about electrical injection and its timing relation with $\varnothing 1$ and $\varnothing 2$. Part 2 presents the circuit which can generate TP2 and TP4 pulses, the third part describes the pulse synchronization, and in the last part, the operation of pulsed electrical injection is discussed.

DESCRIPTION OF ELECTRICAL INJECTION

Charge injection into the CCD121H is done by means of a charge-presetting input mode (the fill and spill method). It is linear, has the advantage of low noise, and doesn't depend on the MOS threshold voltage. Figure 7.1 shows this method. The TP2 and TP4 clocks cause charge to be electrically injected into the shift registers of the CCD121H. TP2 is synchronized with the HIGH level of $\varnothing 2$ and TP4 is synchronized with the HIGH level of $\varnothing 1$. TP2 and TP4 are active low—the HIGH level is 15 V and the LOW level is 5 V. TP1 and TP3 are fixed by a voltage from 0 to 5 V to form a potential well. Figure 7.2 shows the relationship among TP2, TP4, $\varnothing 2$, and $\varnothing 1$. 
Figure 7.1 Charge-presetting input mode.
Figure 7.2 The relationship among TP2, Ø1, TP4, and Ø2.
Figure 7.1(a) shows a well formed under TP1. A potential well caused between two N+ diffusions is only a little lower than that under the barrier of Ø1b. A 15 V voltage is connected to TP2 to pull electrons out of the silicon to the deeper well which is formed by the 15 V. It should be noted initially the Ø1b is LOW and Ø2b is HIGH. When the applied voltage on TP2 drops to 5 V, charge is injected from the diode represented by TP2 and fills in the well under TP1 as shown in Figure 7.1(b). The excess input charge returns to the source diffusion when the applied voltage is raised to 15 V as in Figure 7.1(c). Later when Ø1b is changed to its HIGH level and Ø2b goes LOW, the charge in the well under TP1 will be transferred to the well formed by Ø1b. This is shown in Figure 7.1(d). Thus the charge is injected into the shift register of the CCD121H. The other register has charge injected in a similar manner using TP3, TP4, Ø1a, and Ø2a, as shown in the parentheses in Figure 7.1.

CIRCUIT FOR TP2 AND TP4 GENERATION

TP2 must be active low when Ø1 is low (Ø2 is high) and must be over before Ø1 goes high. TP4 must be active low when Ø1 is high and be over before the latter switches. Both conditions can be satisfied by using gated Ør pulses as triggers. If we allow TP2 (TP4) to
have a fixed 300 nsec pulse width, then we must make R28 4.7 Kohm and C28 22 pfd to generate a positive 120 nsec pulse for transistor Q1 (Q2) (Refer to the data sheet of the 74LS123 in Appendix C). In Figure 7.3, we use the same triggering as for Ør, that is, C of the 74LS93 (U33), positive-triggers the 74LS123 (U49). The Q of U49 will output positive pulses with 120 nsec width to U50 (a 3-input AND gate). Then to generate TP2 pulses we put Ø2 to U50. When the EN signal is changed from LOW to HIGH by the circuit shown in Figure 7.5, U50 will output positive pulses of 120 nsec duration. Transistor Q1 will be on when the HIGH level voltage drives its base and will be off when the level is LOW.

Assume the worst case, $\beta_{\text{min}}$ of Q1 is 20.

$V_{\text{be on}} = 0.75 \text{ V}$

$V_{\text{ce on}} = 0.2 \text{ V}$

HIGH level of pulse = 3.6 V

LOW level of pulse = 0.5 V

Then when the output of U50 is high:

$I_b = (3.6-0.75)/R29$

$= 2.85/47$

$= 60.6 \text{ mA}$

If Q1 works in the active region:

$I_c = 20 \times 60.6 \text{ mA}$

$= 1.212 \text{ A}$

$V_c = 15 \text{ V} - I_c \times (R31 + R30)$
Figure 7.3 Circuit for TP2 and TP4 generation.
\[ 15 \text{ V} - 1.212 \text{ A} \times (1000 + 470 \text{ ohm}) = -1766.6 \text{ V} \]

(This is impossible to occur.)

Therefore \( \text{Q1} \) is saturated.

\[ \text{Ic} = \frac{(15 - \text{Vce})}{(R31 + R30)} = \frac{(15 - 0.2)}{(1470)} = 10.1 \text{ mA} \]

\[ \text{TP2 voltage} = 0.2 + \text{Ic} \times R30 = 0.2 + 0.0101 \times 470 = 4.95 \text{ V} \]

If the low level output is applied to the base of \( \text{Q1} \), this voltage, 0.5 V, is smaller than \( V_{\text{be ON}} \) (0.75 V), so \( \text{Q1} \) should be off.

\( \text{Ic} \) is nearly equal to 0.

Therefore,

\[ \text{TP2 voltage} = 15 \text{ V} \]

Because of the resistors \( R29, R30, \) and \( R31 \), the width of the TP2 pulse will be greater than 120 nsec. The measurement shows a 300 nsec width. TP4 has the same operation using \( \text{Q1}, U51, \) and \( \text{Q2} \) as shown in the parentheses in Figure 7.3.

PULSE SYNCHRONIZATION OF TP2 AND TP4 GENERATION

Figure 7.4 shows the timing diagram of TP2 and TP4. The maximum pulse frequency of both is the same as \( \text{Q1} \) when EN is HIGH.
Figure 7.4 Timing diagram of TP2 and TP4.
THE OPERATION OF PULSED ELECTRICAL INJECTION

Figure 7.5 shows the circuit which controls the number of pulses of electrical injection. For the idea of this operation, refer to Figure 7.6. After T4 is generated and the photosites have been emptied (Refer back to Chapter 5), we wait a preset number of $n_r$'s and then begin to inject background charge. The relation of $n_r$ and the injection signal is shown in Figure 7.7. When the required number of sets of background charge packets is reached, we stop TP2 as shown in Figure 7.6. This allows a pulse train to be put in the register to test it. [Ref. 7-1]

In Figure 7.5, from the specification of the Z80-CTC, the clock high pulse width should be greater than 200 nsec (refer to Appendix B, CTC AC Characteristics). Therefore we put $n_r$ into U70 to generate the 320 nsec positive pulses to trigger the Z-80 CTC. Two 8-bit values are sent from the system computer to the Z-80 CTC, and stored into CTC-0 and CTC-1. $P^*$ is the control signal coming from the microcomputer through b6 of the Z80-PIO B port. When it is started, it will be from LOW to normally HIGH so that when $S^*$ (described in Chapter 5) is active, $R^*$ can be transferred through U54 to U52. Initially Q of U52 is LOW; when U52 is triggered by $R^*$, Q of U52 becomes HIGH and each pulse from Q of U70 goes through U55 to lower the CTC-0 counter value by 1. When
Figure 7.5 The circuit which controls the operation of pulsed electrical injection.
Figure 7.6 Signals for sending a pulse train of charges through the CCD.
Figure 7.7 Pulsed charge injection with 2 blank pixels followed by three injected pulses.
a zero is reached, C of CTC-0 outputs a positive pulse to reset U52, making Q of U52 LOW and clocking U53 to set Q of U53 to HIGH. Thereafter, the pulses from Q of U70 go through U57 to trigger the CTC-1 counter. This counter has stored the required number of sets of charge packets. When it counts down to 0, a positive pulse comes from D of CTC-1 and resets U53 to stop the pulses from Q of U70 going through U57. Thus a train of any number of charge packets is transferred after any desired delay from the start of the frame by Q1 and Q2 and are obtained at the output of the CCD121H after shifting through the registers.

For example, assume the read-out ratio is 2, the number of Q's between the start of frame and electrical injection is 5, and the required number of sets of background charge packets is 100. Then the outputs of the first 2 cycles of the read-out ratio will have 1728 video pixels, 2+5 blanks, 100 pixels of background charge, and 1625 blanks. For the next cycle of this operation, R* will be transferred to U52 again, and the operation will be repeated.

Because the maximum count of the CTC-0 and the CTC-1 are 255 ($FF$), we can only set the desired delay from the start of frame to be 255 maximum and the number of injection charge packets also at most 255. In this design, electrical injection is only read out in the
second cycle of the read-out ratio after the first frame. Charge injection read out beyond cycle 2, is not possible with this hardware. However, the switch allows continuous injection to occur during the entire frame if that is desired.

For further understanding, we should know the software operation of the system. Therefore, in Chapter 8 we will describe the software. Chapter 9 will summarize the entire project.
CHAPTER 8

SOFTWARE

This Chapter is divided into 6 parts. Part 1 is the description of the software. Part 2 discusses the format of the preset value which is entered from the keyboard. The operation of data key-in and program execution are discussed in Part 3. Part 4 and part 5 show the memory map and I/O map for the software. The sixth part describes the flowcharts. For further understanding, the control program is attached in Appendix B.

DESCRIPTION OF THE SOFTWARE

The microcomputer MPF-1 outputs all preset data to the A port of the Z-80 PIO (the chip number and data sheet are shown in Appendix B) and sends the control signals (latches and triggers) through the B port of the same PIO to choose the buffers (74LS374's) to accept the preset data or to trigger the master clock generation board (described in Chapter 5, 6, and 7). In addition, the number of Ør's between the start of frame and electrical injection and the required number of sets of background charges are stored into the Z-80 CTC (the chip number and data sheet are shown in Appendix B) at the beginning of operation. The simplified block diagram of the connections between the MPF-1 and the
buffers (73LS374's) is shown in Figure 8.1.

Although the Z-80 PIO is TTL compatible, its driving capacity is only for 1 TTL gate. The master clock generation board has more than 1 input gate connected to each signal from the Z-80 PIO, so we use 74LS373 and 74LS374's as the buffers and drivers. Because they are used as buffers, the outputs of the Z-80 PIO should always be present at the outputs of the TTL chips so we ground the OE (output enable) of these chips. The A port of the Z-80 PIO is directly connected to the inputs of the 74LS374's which buffer it. The CK (clock trigger) of the 74LS374's are not often triggered, they are always low or triggered by a positive pulse to catch data in. The B port of the Z-80 PIO is connected to the inputs of the 74LS373. b0 is for D0, b1 is for D1, and so on. The EN (enable) of the 74LS373 is high so the latch is always transparent. Thus, Q0 triggers CK of U53, Q1 triggers CK of U54, and Q2 triggers CK of U55. The S* is generated from Q7. Q6 is for P* to operate electrical injection.

Refer to Appendix B for information of the Z-80 PIO, the Z-80 CTC, and MPF-1 microcomputer. The actions of the software are as follows:

1.) Set the Z-80 CTC-0 as a count-down counter and send the number of Ør's between the start of frame and the beginning of injection to this counter.
Figure 8.1 The connection between MPF-1 and the buffers (74LS373 and 74LS374's).

(described in Chapter 5).

S* (described in Chapter 7).

U53

Q7

U54

Q7

U55

Q7

74LS374

Not used

CK

OE

DO

74

Q3

74

Q4

DO

74

Q1

DO

74

Q2

DO

74

Q0

DO

74

Q0

for t1

for t2

for \( \varnothing 1 \)

for read-out Q0 ratio

Z-80 PIO

MPP-1

A port

\begin{array}{c}
\text{a0} \\
\text{a1} \\
\text{a2} \\
\text{a3} \\
\text{a4} \\
\text{a5} \\
\text{a6} \\
\text{a7} \\
\end{array}

B port

\begin{array}{c}
\text{b0} \\
\text{b1} \\
\text{b2} \\
\text{b3} \\
\text{b4} \\
\text{b5} \\
\text{b6} \\
\text{b7} \\
\end{array}

\begin{array}{c}
\text{CTC-0} \\
\text{CTC-1} \\
\end{array}

\begin{array}{c}
\text{DO} \\
\text{D7} \\
\text{IN} \\
\text{74LS373} \\
\text{EN} \\
\text{U52} \\
\text{Q0} \\
\end{array}

\begin{array}{c}
\text{Q1} \\
\text{Q2} \\
\text{Q3} \\
\text{Q6} \\
\text{Q7} \\
\end{array}

\begin{array}{c}
\text{CK} \\
\text{OE} \\
\end{array}

\begin{array}{c}
\text{for read-out Q0 ratio} \\
\text{for \( \varnothing 1 \)} \\
\text{for t2} \\
\text{for t1} \\
\text{Not used} \\
\end{array}

\begin{array}{c}
\text{\textbf{Figure 8.1}} \\
\text{The connection between MPF-1 and} \\
\text{the buffers (74LS373 and 74LS374's).} \\
\end{array}
2.) Set the Z-80 CTC-1 as a count-down counter and send the required number of injected signals to this counter (the Z-80 CTC-0 and CTC-1 are two out of the four counters inside the Z-80 CTC chip).

3.) Set the A port of the Z-80 PIO to be an output port.

4.) Set the B port of the Z-80 PIO to be an output port.

5.) Get the preset data of t1 and t2 from the data area to the A port of the PIO.

6.) Send a positive pulse whose width of about 30.9 µs through b0 of the B port (output from Q0 of U52 74LS373) to trigger the CK of U53 (74LS374) for holding the data from the A port of the PIO.

7.) Get the preset data for the Ø1 width and the read-out ratio counter from the data area to the A port of the PIO.

8.) Send a positive pulse whose width of about 30.9 µs through b1 of the B port (output from Q1 of U52) to trigger the CK of U54 (74LS374) for holding the data from the A port of the PIO.

9.) There are three variations here:

   (a.) Only the S* (start) signal is generated. This is normal optical signal output operation (have Øxa, Øxb, Ø1, Ø2, Ør, and Øsh outputs).

   (b.) The P* signal is generated first, then S*
occurs. This causes a defined number of TP2 and TP4 pulses in addition to the signals in part (a).

(c.) No P* and S* are generated. This results in shutting off $\phi x, TP2, and TP4$. Only $\phi 1, \phi 2, \phi r, and \phi sh operate to sweep out the dark current from the CCD.

DATA FORMAT

The required preset data to generate the above signals are entered from the keyboard and stored in the data area. The preset data for $t1$ and $t2$ is stored in location $1800$ (two hexadecimal numbers, one byte) and the preset data for $(\phi 1, \phi 2, and \phi r)$ and read-out ratio counter is stored in location $1801$ (one byte). Another two 8-bit numbers for the $\phi r's$ between the start of frame and electrical injection and the required sets of injected charge are put into locations $1802$ and $1803$. The four data are 8-bit wide and their data formats are shown in Figure 8.2.

During a run, the data are entered from the keyboard into the data locations before the microcomputer starts the master clock generation board. After the microcomputer sends the preset data and signals out to the master clock generation board, it sends S* (or P* and S*) last of all, then it goes back to the monitor mode (where it is controlled by its built-in monitor, not the software of the system). Therefore, even while
The number of \( \tilde{O}_r \)'s between the start of frame and beginning of injection. This value is from 1 to 255.

The required number of sets of background charges. The number is from 1 to 255.

Figure 8.2 The data formats of the preset values.
the system is running to supply all the clocks for the CCD, we can vary any preset data, change any operation, or stop any operation (by altering the S* and P* signals) during processing.

OPERATION OF DATA KEY-IN AND SYSTEM EXECUTION

The data key-in and program execution are controlled by the monitor. The operator uses the keyboard to specify a destination location to put in data or a starting address to run a program. The user should put an $FF at the end of the program so that the microcomputer will return to the monitor mode after it finishes execution.

Refer to Figure 8.3 which illustrates the operation of a change of data and program execution. The program in EPROM can not be erased, so we can only change the data in the RAM area ($1800 to $1F00) and specify the starting address of an operation in the EPROM area ($2000 to $27FF) to execute. After an operation is run, the display will show an address which is the next location after the last byte of the program for the operation. The microcomputer is running in monitor and free from the master clock generation board after a program for an operation has finished execution.
**Example:**

<table>
<thead>
<tr>
<th>Press keys</th>
<th>display</th>
<th>remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADDR 1 8 0 0</td>
<td>1.8.0.0..</td>
<td>find the location for t1, t2 preset values.</td>
</tr>
<tr>
<td>DATA 5 C</td>
<td>1.8.0.0.5.C</td>
<td>The first preset value $5C. $5 for t1 and $C for t2.</td>
</tr>
<tr>
<td>+</td>
<td>1.8.0.1..</td>
<td>find the next location for the second preset value.</td>
</tr>
<tr>
<td>6 A</td>
<td>1.8.0.1.6.A</td>
<td>$6 for $1 and $A for the read-out ratio.</td>
</tr>
<tr>
<td>+</td>
<td>1.8.0.2..</td>
<td>find the next location for the 3rd preset value.</td>
</tr>
<tr>
<td>0 7</td>
<td>1.8.0.2.0.7</td>
<td>$7 for $r's between start of frame and injected charges.</td>
</tr>
<tr>
<td>+</td>
<td>1.8.0.3.3.0</td>
<td>set 48 sets of background charges.</td>
</tr>
</tbody>
</table>

**Figure 8.3** The operations to enter data and run a program for an operation.
MEMORY MAP FOR SOFTWARE

Figure 8.4 shows the memory map for the software. Four preset values are stored in locations $1800$ to $1803$. The address of $2000$ is the starting address of the program for the normal mode. For the operation with electrical injection, its program is put from locations $2100$ to $21FF$. The starting address of the program for no video output is at $2200$. All the programs above are stored in EPROM and can not be erased.

The program listings which were written in Z-80 assembly language are shown in Appendix B and the Z-80 instructions are attached in Appendix B also.

I/O MAP FOR SOFTWARE

In this system, we use the Z-80 PIO and the Z-80 CTC for outputs and counters. The I/O ports of the PIO are from $80$ to $83$, and the I/O ports of the CTC are from $40$ to $43$. They are shown in Figure 8.5. For signal specifications of these two I/O ports, refer to the system schematics in Appendix B.

FLOWCHART

Figure 8.6 shows the flowchart for the normal mode. The flowchart illustrates the sequence of operations which initializes the system and starts the signal S*.
### Memory Map for the Software

<table>
<thead>
<tr>
<th>Address</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$1800</td>
<td>$1800</td>
<td>the first preset value</td>
</tr>
<tr>
<td>$1801</td>
<td>$1801</td>
<td>the second preset value</td>
</tr>
<tr>
<td>$1802</td>
<td>$1802</td>
<td>the third preset value</td>
</tr>
<tr>
<td>$1803</td>
<td>$1803</td>
<td>the fourth preset value</td>
</tr>
<tr>
<td>$2000</td>
<td>$2000</td>
<td>for normal mode.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>S* signal generated.</td>
</tr>
<tr>
<td>$2100</td>
<td>$2100</td>
<td>for electrical injection.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>P* generated first, then S* starts.</td>
</tr>
<tr>
<td>$2200</td>
<td>$2200</td>
<td>CCD not operating.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>no P* and S* generated.</td>
</tr>
</tbody>
</table>

Figure 8.4 The memory map for the software.
port #:  
$40  CTC-0  control word $55 for setting counter mode.
$41  CTC-1  control word $55 for setting counter mode.
$42  CTC-2  not used.
$43  CTC-3  not used.
$80  PIO DA  output data buffer.
$81  PIO DB  output signal buffer.
$82  PIO CA  control word $0F for setting output mode.
$83  PIO CB  control word $0F for setting output mode.

Figure 8.5 I/O map for the software.
Flowchart  

Normal mode of CCD clocking

1.) Set the A port of the Z-80 PIO to be an output port. Control word is $0F.

2.) Set the B port of the Z-80 PIO to be an output port. Control word is $0F.

3.) Get data from $1800 location.

4.) Is the preset value= 0?
   (4.1) "yes", Display FFFF FF and go to monitor. "no", go to 5.)

5.) Output to the first buffer (U53, 74LS374).

6.) Get the data from $1801 location.

7.) Is the preset value= 0?
   "yes", go to (4.1).
   "no", go to 8.)

8.) Output to the second buffer (U54, 74LS374).

9.) Output a signal $S^*$ through b7 to start system. The signal must stay high for the CCD to continue operating.

10.) Return to monitor control.

Figure 8.6 The flowchart for the normal mode.
The control word for an output port of the Z-80 PIO is $0F$ (refer to Appendix E, data sheets of the Z-80 PIO). Therefore, the accumulator A of the Z-80 CPU loads $0F$ and sends it to port number $82$ which is the control of port A. Then the accumulator A sends $0F$ again to port number $83$ which is port B. Therefore, ports A and B of the Z-80 PIO are set to be output ports. The accumulator A gets data from $1800$ and transfers it to the data of port A ($80$), and sends a sequence of values $00$, $01$, and $00$ through port B to latch the preset value into U53 (74LS374). Next the accumulator A obtains data from $1801$ and puts it into port number $80$, and sends a sequence of values $02$ and $00$ through port B to get the preset data in U54. Finally, a value $80$ is sent by the accumulator A through port B to generate the signal $S^*$ and the system is clocked for the normal mode.

For the operation with electrical injection, the flowchart is shown in Figure 8.7. First, the preset values of $1800$ and $1801$ are latched by U53 and U54 using the same operations as above. The number of $0r$ pulses between the start of frame and injected charges is gotten from $1802$ and sent to port number $40$ (CTC-0). The other value of the number of background pulses is obtained from $1803$ and transferred to port number $41$ (CTC-1). Then the accumulator A sends a value $40$ to activate $P^*$ from LOW to HIGH and later outputs a number $S0$ to generate $S^*$. At that point, read out with
Flowchart P* and S* signals generated

1.) Set the A port of the Z-80 PIO to be an output port. Control word is $0F.
2.) Set the B port of the Z-80 PIO to be an output port. Control word is $0F.
3.) Get the data from $1800 location.
4.) Is the preset value= 0?
   (4.1) "yes", Display DDDD DD and go to monitor.
   "no", go to 5).
5.) Output to the first buffer (U53, 74LS374).
6.) Get the data from $1801 location.
7.) Is the preset value= 0?
   "yes", go to (4.1).
   "no", go to 8.)
8.) Output to the second buffer (U54, 74LS374).
9.) Send a Control word $55 to CTC-0.
    port #: $40 to define CTC-0 to be a counter.
10.) Get the data from $1802 location.
    Value is from 1 to 255.
11.) Send to the CTC-0, port #: $40.
12.) Send a control word $55 to CTC-1.
    port #: $41 to define CTC-1 to be a counter.
13.) Get the data from $1803 location.
    Value is from 1 to 255.
14.) Send to the CTC-1, port #: $41.
15.) Output P* signal through b6; hold it at a high level.
16.) Send the START S* signal through b7 and hold it there to begin the Øx transfer.
17.) Return to monitor mode.

Figure 8.7 The flowchart for the operation with electrical injection.
electrical injection begins executing. (Note that the control words for the CTC-0 and CTC-1 are same, i.e. $55$. Refer to Appendix E for details).

Finally, for no video output, only port B is set to be an output port, and there is not any signal generated. The flowchart is shown as Figure 8.8.

We have introduced the CCD and discussed the whole system. A brief review of the system is given in Chapter 9 as a conclusion.
Flowchart

No P* and S* generated

1.) Set the B port of the Z-80 PIO to be an output port. Control word is $0F.

2.) Pull b6 and b7 of B port to low to stop P* and S* signals from being active, so that no $\phi x_a, \phi x_b, TP2, \text{ and } TP4 \text{ are generated.}$

3.) Return to monitor mode.

Figure 8.8 The flowchart for no video or charge injection.
CHAPTER 9

REVIEW OF THE SYSTEM

This system is a design to drive the clocks of the CCD121H. The boards for Chapter 5 and 6 are built and tested. All TTL chips are the "74LS" series for getting uniform DC and AC characteristics except those special functions supported by "74" numbers. The system microcomputer was designed and manufactured in Taiwan, Republic of China. The programs were written by the Z-80 instructions on the IBM PC XT system and saved in EPROM (2716); its locations are from $2000$ to $27FF$. The power supply supports three sets of voltages: $+5$ V (2 A), $+12$ V (1 A), and $+15$ V (1 A). The $+5$ V voltage is used for the TTL integrated circuits, and $+12$ V and $+15$ V are used for the drivers and TP2 and TP4 generators.

The microcomputer is in the monitor mode after it runs the program to start the CCD, so we can use the keyboard to control the system at any time. Therefore, the operation of the CCD121H is varied by the microcomputer any time the operator wishes.

The thesis is a design only for the clocks of the CCD121H. It supports variable frequency operation for the CCD121H to output the video signals with or without background charges.

The system was tested using an oscilloscope to
monitor the outputs. The pulse width of $\varnothing r$ is about 130 nsec and its frequency range is from 78 KHz to 625 KHz. The range of pulse width of $\varnothing xa$ and $\varnothing xb$ is from 1 $\mu$s to 15 $\mu$s and the range of the delay between these two clocks is from 0.5 $\mu$s to 7.5 $\mu$s. The results for the $\varnothing 1$ and $\varnothing 2$ driver measurements are given in Appendix D.

The system could not actually be used with a CCD because the DC signals and other inputs of the CCD were not available. This system will eventually be part of a larger one. Other workers are dealing with data acquisition, output amplifiers, etc. However, this driver board shows that the idea of a microprocessor controlled high speed CCD test station or camera is practical. This will allow construction of a "smart" camera where the digital system can both monitor the picture from the CCD and improve it by adjusting one of its parameters.
REFERENCES


[Ref. 7-1] Ensley Emanuel Townsend, "A MICROCOMPUTER CONTROLLED CCD TEST STATION", Ohio University, August 1981.
APPENDIX A

*************************************************************************
* DATA SHEET OF THE CCD121H *
*************************************************************************

Block Diagram .......... A-2
Circuit Diagram ........ A-6
Timing Diagram ........ A-7
CCD121H

1728 ELEMENT LINEAR IMAGE SENSOR
CHARGE COUPLED DEVICE

GENERAL DESCRIPTION: The CCD121H is a monolithic self-scanned 1728 Element Image Sensor designed for page scanning applications. The device provides a 200-line per inch resolution across an 8.1/2 inch page. Other intended applications are: facsimile readers, optical character recognition, as well as imaging applications that require high resolution, high sensitivity and high speed.

In addition to a row of 1728 sensing elements, the CCD121H chip includes: two charge transfer gates, two 2-phase analog shift registers, an output charge detector/preamplifier, and a compensation output amplifier. The 2-phase analog shift registers both feed the input of the charge detector resulting in sequential reading of the 1728 imaging elements.

The cell size is 13μ (0.51 mls) by 17μ (0.67 mls) on 13μ (0.51 mls) centers. The device is manufactured using Fairchild charge coupled device buried-channel technology.

- DYNAMIC RANGE TYPICAL: 500:1 (PEAK-TO-PEAK), 2500:1 (rms)
- 1728 ELEMENTS ON A SINGLE CHIP
- ON-CHIP PREAMPLIFIER AND COMPENSATION AMPLIFIER
- LOW POWER REQUIREMENTS
- ALL OPERATING VOLTAGES UNDER 15 V
- PACKAGED IN A 24-PIN DUAL IN-LINE HERMETIC PACKAGE
- LOW NOISE EQUIVALENT EXPOSURE
- WIDE RANGE OF VIDEO DATA RATE
- DIMENSIONALLY PRECISE PHOTOSITE SPACING

BLOK DIAGRAM

CONNECTION DIAGRAM
DIP (TOP VIEW)

PIN NAMES

FAIRCHILD

464 ELLIS STREET, MOUNTAIN VIEW, CALIFORNIA 94042 (415) 962 5211, TWX 710 378 6435
FAIRCHILD CHARGE COUPLED DEVICE * CCD121H

DEFINITION OF TERMS (Cont’d)

Peak-to-Peak Noise Equivalent Exposure — The exposure level which gives an output signal equal to the peak-to-peak noise level at the output in the dark.

Saturation Exposure — The minimum exposure level that will produce a saturated output signal. Saturation exposure is equal to the light intensity times the photosite integration time.

Spectral Response Range — The spectral band in which the response per unit of radiant power is more than 10% of the peak response.

Responsivity — The output signal voltage per unit exposure for a specified spectral type of radiation. Responsivity equals output voltage divided by exposure level.

Photoreponsenon-uniformity — The difference of the response levels of the most and the least sensitive element under uniform illumination. This is commonly expressed as a percentage of the saturation output voltage.

Average Dark Signal — The output signal level in the dark averaged over all elements and measured relative to the base line output voltage established by the reset clock. This is a linear function of the integration time. It is also strongly dependent on temperature. This is commonly expressed as a percentage of the saturation output voltage.

Dark Signal Non-uniformity — Maximum deviation of the output voltage of any element from the background level in the dark. This is commonly expressed as a percentage of the saturation voltage.

Saturation Output Voltage — The maximum signal output voltage.

Integration Time — The time interval between the falling edges of any transfer pulse \( \phi_XA \) and \( \phi_XB \) as shown in the timing diagram. The integration time is the time allowed for the photosites to collect charge.

Output Signal Range — The output signal range is defined as \( OSR = V_{sat} - \frac{t_{INT} + t_{Transport}}{t_{R}} \times \text{Rate of Average Signal Offset} \) where: \( t_{INT} = \) Integration Time; \( t_{Transport} = \) time necessary to transfer the charge packets from the analog shift registers and is equal to \( \frac{1728}{t_{R}} \). Integration time \( t_{INT} \) does not necessarily equal transfer time \( t_{Transport} \). If long integration times are required, \( t_{Transport} \) should be minimized (increase \( t_{R} \) to maximize \( OSR \).

Average Signal Offset — Average signal offset is a dc offset of the output voltage (due to the average leakage current in the CCD registers) which increases linearly with the transfer time.

TEST LOAD CONFIGURATION

DC CHARACTERISTICS: \( T_A = 25^\circ C \)

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>CHARACTERISTIC</th>
<th>RANGE</th>
<th>UNITS</th>
<th>CONDITIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>MIN</td>
<td>TYP</td>
<td>MAX</td>
</tr>
<tr>
<td>VDD</td>
<td>Output Transistor Drain Voltage</td>
<td>14.5</td>
<td>15.0</td>
<td>15.5 V</td>
</tr>
<tr>
<td>VDD</td>
<td>Reset Transistor Drain Voltage</td>
<td>11.5</td>
<td>12.0</td>
<td>12.5 V</td>
</tr>
<tr>
<td>VDD</td>
<td>Output Gate Voltage</td>
<td>4.5</td>
<td>5.0</td>
<td>5.5 V</td>
</tr>
<tr>
<td>VDD</td>
<td>Propagate Voltage</td>
<td>10.0</td>
<td>10.5</td>
<td>10.5 V</td>
</tr>
<tr>
<td>TP1, TP2</td>
<td>Test Points</td>
<td>0.0</td>
<td>0.0</td>
<td>V</td>
</tr>
<tr>
<td>TP3, TP4</td>
<td>Test Points</td>
<td>14.5</td>
<td>15.0</td>
<td>15.5 V</td>
</tr>
</tbody>
</table>
FAIRCHILD CHARGE COUPLED DEVICE - CCD121H

PHOTOELEMENT DIMENSIONS

All dimensions are typical values

TYPICAL PERFORMANCE CURVES

OUTPUT SIGNAL LEVEL VERSUS INTEGRATION TIME
2854 K TUNGSTEN SOURCE

TYPICAL SPECTRAL RESPONSE

Note 1. Internal responsivity is related to the responsivity at the output through integration time and preamp charge-to-voltage conversion gain.

Note 2. Internal responsivity pertains to photoelement signal only. It excludes the shift in black reference level produced by long wavelength irradiation.

MODULATION TRANSFER FUNCTIONS FOR TWO BROADBAND ILLUMINATION SOURCES
SPATIAL FREQUENCY - CYCLES/\text{\textmu \text{m}}

MODULATION TRANSFER FUNCTIONS FOR NARROW BAND ILLUMINATION SOURCES
SPATIAL FREQUENCY - CYCLES/\text{\textmu \text{m}}

The Corning 1-75 filter has the following typical transmission: normal characteristic.

\text{\textgreater} 85\% \text{at} \leq 600 \text{nm}, 80\% \text{at} 700 \text{nm}, 70\% \text{at} 800 \text{nm}, 5\% \text{at} 900 \text{nm} and \textless 2\% \text{at} \geq 1000 \text{nm}.
### Clock Characteristics: \( T_A = 25^\circ C \)

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>CHARACTERISTIC</th>
<th>RANGE</th>
<th>UNITS</th>
<th>CONDITIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{\text{C1A}}, V_{\text{C1B}} )</td>
<td>Analog Shift Register Transport Clocks LOW</td>
<td>0.0</td>
<td>0.5</td>
<td>0.8</td>
</tr>
<tr>
<td>( V_{\text{C2A}}, V_{\text{C2B}} )</td>
<td>Analog Shift Register Transport Clocks HIGH</td>
<td>7.5</td>
<td>8.0</td>
<td>8.5</td>
</tr>
<tr>
<td>( V_{\text{C3A}}, V_{\text{C3B}} )</td>
<td>Transfer Gate Clock LOW</td>
<td>0.0</td>
<td>0.5</td>
<td>0.8</td>
</tr>
<tr>
<td>( V_{\text{C3A}}, V_{\text{C3B}} )</td>
<td>Transfer Gate Clock HIGH</td>
<td>7.5</td>
<td>8.0</td>
<td>8.5</td>
</tr>
<tr>
<td>( V_{\text{R}} )</td>
<td>Reset Clock LOW</td>
<td>0.0</td>
<td>0.5</td>
<td>0.8</td>
</tr>
<tr>
<td>( \phi_{1A}, \phi_{1B} )</td>
<td>Maximum Analog Shift Register Transport Clock Frequency</td>
<td>5.0</td>
<td>MHz</td>
<td>Notes 4, 5</td>
</tr>
<tr>
<td>( \phi_{R} )</td>
<td>Maximum Reset Clock Frequency (Output Bit Rate)</td>
<td>10.0</td>
<td>MHz</td>
<td>Notes 4, 5</td>
</tr>
</tbody>
</table>

### AC Characteristics: \( T_A = 25^\circ C, I_{\text{PH}} = I_{\text{PH}} = 0.5 \text{ MHz}, I_{\text{AR}} = 1 \text{ MHz}, \text{ INT} = 1.78 \text{ ms}, \text{ TRANSPORT} = 1.73 \text{ ms}. \) See Note 14

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>CHARACTERISTIC</th>
<th>RANGE</th>
<th>UNITS</th>
<th>CONDITIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \text{DR} )</td>
<td>Dynamic Range</td>
<td>250</td>
<td>500</td>
<td></td>
</tr>
<tr>
<td>( \text{N} )</td>
<td>Peak-to-Peak Noise Equivalent Exposure</td>
<td>1 x 10^{-3}</td>
<td>( \mu \text{cm}^2 )</td>
<td>Note 7</td>
</tr>
<tr>
<td>( \text{SE} )</td>
<td>Saturation Exposure</td>
<td>1.0</td>
<td>( \mu \text{cm}^2 )</td>
<td>Note 7</td>
</tr>
<tr>
<td>( \text{SR} )</td>
<td>Spectral Response Range Limits</td>
<td>0.45 - 1.05</td>
<td>um</td>
<td></td>
</tr>
<tr>
<td>( \text{R} )</td>
<td>Responsivity</td>
<td>0.5</td>
<td>V per ( \mu \text{cm}^2 )</td>
<td>Notes 9, 10, 11</td>
</tr>
<tr>
<td>( \text{PRNU} )</td>
<td>Photoreponse Non-uniformity</td>
<td>( \pm 25 )</td>
<td>( \pm 50 )</td>
<td>mV</td>
</tr>
<tr>
<td>( \text{ADS} )</td>
<td>Average Dark Signal</td>
<td>5.0</td>
<td>25</td>
<td>mV</td>
</tr>
<tr>
<td>( \text{DSNU} )</td>
<td>Dark Signal Non-uniformity</td>
<td>20</td>
<td>50</td>
<td>mV</td>
</tr>
<tr>
<td>( \text{V}_{\text{S}} )</td>
<td>Saturation Output Voltage</td>
<td>500</td>
<td>750</td>
<td>1000</td>
</tr>
<tr>
<td>( \text{V}_0 )</td>
<td>Output DC Level</td>
<td>7.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( \text{P} )</td>
<td>Power Dissipation</td>
<td>165</td>
<td>mW</td>
<td>( V_{DD} = 15 \text{ V} )</td>
</tr>
<tr>
<td>( \text{Z} )</td>
<td>Output Impedance</td>
<td>1000</td>
<td>Q</td>
<td></td>
</tr>
<tr>
<td>( \text{N} )</td>
<td>Peak-to-Peak Output</td>
<td>1.0</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>( \text{RSO} )</td>
<td>Rate of Average Signal Offset</td>
<td>2.5</td>
<td>mV/ms</td>
<td></td>
</tr>
</tbody>
</table>

**Notes:**
1. \( V_{\text{PA}} \) should track \( V_{\text{DD}} \).
2. Receive transients on the clocks below 0.0 V may cause an increase in apparent dark signal.
3. \( C_{\text{PA}}, C_{\text{PB}}, C_{\text{PA}}, C_{\text{PB}}, C_{\text{PA}}, C_{\text{PB}} \approx 400 \text{ pf}, C_{\text{PA}}, C_{\text{PB}} \approx 10 \text{ pf} \).
4. The resulting clock frequency is twice that of each analog shift register clock \( \phi_{1A}, \phi_{2A}, \phi_{1B}, \phi_{2B} \).
5. Minimum clock frequency is limited by increase in dark current which reduces output signal range. See curves.
6. The dynamic range is measured by taking the ratio of the saturation output voltage to the peak-to-peak noise of the device in the dark. Because of the high degree of linearity of the device the dynamic range measurement is also approximately equal to the ratio of the saturation exposure to the peak-to-peak noise equivalent exposure.
7. 1 \( \mu \text{cm}^2 \) = 0.02 lcs at 2854K. 1 lcs = 50 \( \mu \text{cm}^2 \) at 2854K.
8. Measurement is done at \( +350 \text{ mV output level}. Measurement excludes first and last elements but includes both registers outputs.
9. See test load configurations.
10. See definition of terms.
11. For 2854K light source.
12. See curve.
13. DSNU has similar integration time and temperature dependence as ADS.
14. It is recommended to use an infrared blocking filter to obtain minimum PRNU and crosstalk.
FAIRCHILD CHARGE COUPLED DEVICE • CCD121H

CIRCUIT DIAGRAM

PACKAGE OUTLINE
24-Pin Dual In-line Hermetic Package

NOTES:
All dimensions in inches (bold) and millimeters (parentheses). Header is black ceramic (Al₂O₃). Transparent portion of package is glass. The CCD121H hermetic package carries the number “24” close to pin 1 of the device. This number should not be confused with pin 24 of the device, which is connected to Vgg (substrate).

ORDER INFORMATION — Order CCD121HC where “H” stands for hermetic package and “C” is commercial temperature range. The CCD121HC is the replacement for the CCD121DC. The two devices are pin-for-pin compatible. The output op-amp of the CCD121H is an improved design over the CCD1211 providing a higher saturation output voltage of typically 760 mV.

Also available is a printed circuit board that includes all the necessary clocks, logic, drivers and video amplifiers to operate the CCD121H. The printed circuit board is fully assembled and tested and requires three power supplies for operation (+5 V, +15 V and -15 V). The printed circuit board order code is: CCD121HB.
Timing requirements for Transfer Gate Pulses $\phi_{XA}, \phi_{XB}$

- $t_3 > 0.8 \mu s$
- $t_4 > 0.1 \mu s$

Timing requirements for Reset Pulse $\phi_{RA}$

- $t_5 = t_7 < 0.3 (t_{o2})$
- $0.25 (t_{o2}) < t_{oR} < 0.5 (t_{o2})$

Timing requirements for $\phi_{1A}, \phi_{1B}$

- $0.1 (t_{o2}) < (t_5 - t_7) < 0.4 (t_{o2})$
APPENDIX B

************************************************************
**INFORMATION OF THE MICROCOMPUTER MPF-1, Z-80 PIO,**
**AND Z-80 CTC.
************************************************************

1. The MPF-1 ........................................ B-2
2. The Z-80 PIO ................................. B-4
3. The Z-80 CTC ................................. B-7
4. The Z-80 Instruction Set .......... B-11
5. The Program Listing ................. B-14
Z80-PIO PIN ASSIGNMENT

CPU DATA BUS

PORT B/A SEL
CONTROL/DATA SEL

PIO CONTROL

CHIP ENABLE
MT
LORG
RD

INTERRUPT CONTROL

INT ENABLE IN
INT ENABLE OUT

FIGURE 10-1
PIO PIN CONFIGURATION
Z-80 PIO Z-80A PIO

Zilog

PIO Programming

COMPONENTS

LOAD INTERRUPT VECTOR

The Z80-CPU requires an 8-bit interrupt vector to be supplied
by the interrupting device. The CPU forms the address for
the interrupt service routine of the port using this vector.
During an interrupt acknowledge cycle the vector is placed
on the Z-80 data bus by the highest priority device request-
ning service at that time. The desired interrupt vector is
loaded into the PIO by writing a control word to the
desired port of the PIO with the following format.

<table>
<thead>
<tr>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Bit 7 = 1 indicates the control word is an interrupt
vector. If Bit 7 = 0, the remaining bits are used to
select an operating mode as shown below.

SELESTING AN OPERATING MODE

When selecting an operating mode, the 2-bit mode control
register is set to one of four values. These two bits are
the most significant bits of the register; bits 7 and 6; bits 5
and 4 are not used while bits 3 through 0 are all set to 1111
to indicate “set mode.”

<table>
<thead>
<tr>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1</td>
<td>M0</td>
<td>X</td>
<td>X</td>
<td>I</td>
<td>I</td>
<td>I</td>
<td>I</td>
</tr>
</tbody>
</table>

X = unused bit

MODE 0 active indicates that data is to be written from
the CPU to the peripheral.

MODE 1 active indicates that data is to be read from the
peripheral to the CPU.

MODE 2 allows data to be written to or read from the
peripheral device.

MODE 3 is intended for status and control applications.
When selected, the next control word must set the I/O
Register to indicate which lines are to be input and
which lines are to be output.

<table>
<thead>
<tr>
<th>Mode</th>
<th>M1</th>
<th>M0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Input</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Bidirectional</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Bit</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

The interrupt enable flip-flop of a port may be set or
reset without modifying the rest of the interrupt control
word by the following command.

<table>
<thead>
<tr>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>I</td>
</tr>
</tbody>
</table>
PIO PROGRAMMING SUMMARY

REGISTER SELECTION

<table>
<thead>
<tr>
<th>SELECT LINES</th>
<th>REGISTER SELECTED</th>
</tr>
</thead>
<tbody>
<tr>
<td>C/D</td>
<td>B/A</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

LOAD INTERRUPT VECTOR

07  00

Control Register

V7 V6 V5 V4 V3 V2 V1 0

SET OPERATING MODE

07  00

Control Register

<table>
<thead>
<tr>
<th>Mode Number</th>
<th>M1</th>
<th>M0</th>
<th>Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Output</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Input</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>0</td>
<td>Bidirectional</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>1</td>
<td>Bit Control</td>
</tr>
</tbody>
</table>

If Mode 3 selected, the next control word is

07  00

Control Register

1/O 1/O5 1/O4 1/O3 1/O2 1/O1 1/O0

1/O = 1 Sets bit to input
1/O = 0 Sets bit to Output

SET INTERRUPT CONTROL

07  00

Control Register

<table>
<thead>
<tr>
<th>Int Enable</th>
<th>AN07 OR</th>
<th>High Low</th>
<th>Mask Follows</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

In Mode 3 if Mask follows = 1, the next control word is

07  00

Control Register

MB7 MB6 MB5 MB4 MB3 MB2 MB1 MB0

MB = 0 Monitor the bit
MB = 1 Mask the bit

ENABLE / DISABLE INTERRUPTS

07  00

Control Register

<table>
<thead>
<tr>
<th>Int Enable</th>
<th>X X X 0 0 1 1</th>
</tr>
</thead>
</table>
3.0 CTC PIN DESCRIPTION

FIGURE 3.0-1
CTC PIN CONFIGURATION
SELECTING AN OPERATING MODE

When selecting a channel's operating mode, bit 0 is set to 1 to indicate this word is to be stored in the channel control register.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Interrupt</th>
<th>Mode</th>
<th>Channel Busy</th>
<th>Load Time Constant</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Enable</td>
<td>Only</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Enable</td>
<td>Only</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Bit 7 = 0 Channel interrupts disabled.

Bit 7 = 1 Channel interrupts enabled to occur every time Down Counter reaches a count of zero. Setting Bit 7 does not let a preceding count of zero cause an interrupt.

Bit 6 = 0 Timer Mode – Down counter is clocked by the prescaler. The period of the counter is:

\[ t_c = P \cdot TC \]

- \( t_c \) = system clock period
- \( P \) = prescale of 16 or 256
- \( TC \) = 8 bit binary programmable time constant (256 max)

Bit 6 = 1 Counter Mode – Down Counter is clocked by external clock. The prescaler is not used.

Bit 5 = 0 Timer Mode Only—System clock \( \Phi \) is divided by 16 in prescaler.

Bit 5 = 1 Timer Mode Only—System clock \( \Phi \) is divided by 256 in prescaler.

Bit 4 = 0 Timer Mode – negative edge trigger starts timer operation. Counter Mode – negative edge decrements the down counter.

Bit 4 = 1 Timer Mode – positive edge trigger starts timer operation. Counter Mode – positive edge decrements the down counter.

Bit 3 = 0 Timer Mode Only – Timer begins operation on the rising edge of \( T_2 \) of the machine cycle following the one that loads the time constant.

Bit 3 = 1 Timer Mode Only – External trigger is valid for starting timer operation after rising edge of \( T_2 \) of the machine cycle following the one that loads the time constant. The Prescaler is decremented 2 clock cycles later if the setup time is met, otherwise 3 clock cycles.

Bit 2 = 0 No time constant will follow the channel control word. One time constant must be written to the channel to initiate operation.

Bit 2 = 1 The time constant for the Down Counter will be the next word written to the selected channel. If a time constant is loaded while a channel is counting, the present count will be completed before the new time constant is loaded into the Down Counter.

Bit 1 = 0 Channel continues counting.

Bit 1 = 1 Stop operation. If Bit 2 = 1 channel will resume operation after loading a time constant, otherwise a new control word must be loaded.

LOADING A TIME CONSTANT

An 8-bit time constant is loaded into the Time Constant register following a channel control word with bit 2 set. All zeros indicate a time constant of 256.

LOADING AN INTERRUPT VECTOR

The Z80-CPU requires that an 8-bit interrupt vector be supplied by the interrupting channel. The CPU forms the address for the interrupt service routine of the channel using this vector. During an interrupt acknowledge cycle the vector is placed on the Z80 Data Bus by the highest priority channel requesting service at that time. The desired interrupt vector is loaded into the CTC by writing into channel 0 with a zero in D0. D7-D3 contain the stored interrupt vector. D2 and D1 are not used in loading the vector. When the CTC responds to an interrupt acknowledge, these two bits contain the binary code of the highest priority channel which requested the interrupt and D0 contains a zero since the address of the interrupt service routine starts at an even byte. Channel 0 is the highest priority channel.
CTC PROGRAMMING SUMMARY

REGISTER SELECTION

<table>
<thead>
<tr>
<th>SELECT LINES</th>
<th>CHANNEL SELECTED</th>
<th>PRIORITY</th>
</tr>
</thead>
<tbody>
<tr>
<td>CS₁ CS₀</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 0</td>
<td>0</td>
<td>Highest</td>
</tr>
<tr>
<td>0 1</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>1 0</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>1 1</td>
<td>3</td>
<td>Lowest</td>
</tr>
</tbody>
</table>

LOAD INTERRUPT VECTOR

CS₀ = CS₁ = 0

<table>
<thead>
<tr>
<th>V7</th>
<th>V6</th>
<th>V5</th>
<th>V4</th>
<th>V3</th>
<th>X</th>
<th>X</th>
<th>0</th>
</tr>
</thead>
</table>

XX is the binary equivalent of interrupting channel number

SET OPERATING MODE

<table>
<thead>
<tr>
<th>D7 Interrupt Enable</th>
<th>Mode</th>
<th>Range</th>
<th>Slope</th>
<th>Trigger</th>
<th>Load Time Constant</th>
<th>Reset</th>
<th>D0 Control Register</th>
</tr>
</thead>
<tbody>
<tr>
<td>Counter/Timer 256/16</td>
<td>+/-</td>
<td>On/Off</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

If Load Time Constant = 1 the next control word is the Time Constant:

<table>
<thead>
<tr>
<th>TC7</th>
<th>TC6</th>
<th>TC5</th>
<th>TC4</th>
<th>TC3</th>
<th>TC2</th>
<th>TC1</th>
<th>TC0</th>
</tr>
</thead>
</table>

CTC Channel interrupts when 01H is decremented to 00H

<table>
<thead>
<tr>
<th>Time Content</th>
<th>Decimal counts to interrupt</th>
</tr>
</thead>
<tbody>
<tr>
<td>01H</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>2</td>
</tr>
<tr>
<td></td>
<td>FFH</td>
</tr>
<tr>
<td></td>
<td>255</td>
</tr>
<tr>
<td></td>
<td>00H</td>
</tr>
<tr>
<td></td>
<td>256</td>
</tr>
</tbody>
</table>
### Z-80° CTC Z-80A CTC

#### TA = 0° C to 70° C, Vcc = +5 V ± 5%, unless otherwise noted

<table>
<thead>
<tr>
<th>Signal</th>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Φ</td>
<td>tc</td>
<td>Clock Period</td>
<td>250</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td>tP(ΦH)</td>
<td>Clock Pulse Width, Clock High</td>
<td>105</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td>tP(ΦL)</td>
<td>Clock Pulse Width, Clock Low</td>
<td>105</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td>tR, tF</td>
<td>Clock Rise and Fall Times</td>
<td>30</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td>τH</td>
<td>Any Hold Time for Specified Setup Time</td>
<td>0</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>CS, CE, etc</td>
<td>tCS(CE)</td>
<td>Control Signal Setup Time to Rising Edge of Φ During Read or Write Cycle</td>
<td>60</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>D0–D7</td>
<td>tD(D0)</td>
<td>Data Output Delay from Falling Edge of RD During Read Cycle</td>
<td>50</td>
<td></td>
<td>ns</td>
<td>[2]</td>
</tr>
<tr>
<td></td>
<td>tD(D1)</td>
<td>Data Setup Time to Rising Edge of Φ During Write or M1 Cycle</td>
<td>160</td>
<td></td>
<td>ns</td>
<td>[2]</td>
</tr>
<tr>
<td></td>
<td>tD(D2)</td>
<td>Data Output Delay from Falling Edge of IORG During INTA Cycle</td>
<td>110</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td>tD(D1)</td>
<td>Delay to Floating Bus (Output Buffer Disable Time)</td>
<td>140</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>IEO</td>
<td>τI(EI)</td>
<td>IEO Setup Time to Falling Edge of IORG During INTA Cycle</td>
<td>140</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td>τI(HIO)</td>
<td>IEO Delay Time from Rising Edge of IEO</td>
<td>160</td>
<td></td>
<td>ns</td>
<td>[3]</td>
</tr>
<tr>
<td></td>
<td>τI(LIO)</td>
<td>IEO Delay Time from Falling Edge of IEO</td>
<td>130</td>
<td></td>
<td>ns</td>
<td>[3]</td>
</tr>
<tr>
<td></td>
<td>τI(MIO)</td>
<td>IEO Delay from Falling Edge of M1 (Interrupt Occurring just Prior to M1)</td>
<td>190</td>
<td></td>
<td>ns</td>
<td>[3]</td>
</tr>
<tr>
<td>IORG</td>
<td>τS(I)</td>
<td>IORG Setup Time to Rising Edge of Φ During Read or Write Cycle</td>
<td>115</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>MI</td>
<td>τS(M1)</td>
<td>M1 Setup Time to Rising Edge of Φ During INTA or M1 Cycle</td>
<td>90</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>R0</td>
<td>τS(RD)</td>
<td>RD Setup Time to Rising Edge of Φ During Read or M1 Cycle</td>
<td>115</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>INT</td>
<td>τP(CL)</td>
<td>INT Delay Time from Rising Edge of CLK/TRG</td>
<td>2τ(CL)</td>
<td></td>
<td>ns</td>
<td>Counter Mode</td>
</tr>
<tr>
<td></td>
<td>τP(IT)</td>
<td>INT Delay Time from Rising Edge of Φ</td>
<td>2τ(CL)</td>
<td></td>
<td>ns</td>
<td>Timer Mode</td>
</tr>
<tr>
<td>CL/KTRGQ0–3</td>
<td>tc(K)</td>
<td>Clock Period</td>
<td>2τ(CL)</td>
<td></td>
<td>ns</td>
<td>Counter Mode</td>
</tr>
<tr>
<td></td>
<td>tC, tS</td>
<td>Clock and Trigger Rise and Fall Times</td>
<td>210</td>
<td></td>
<td>ns</td>
<td>Counter Mode</td>
</tr>
<tr>
<td></td>
<td>tS(C)</td>
<td>Clock Setup Time to Rising Edge of Φ for Immediate Count</td>
<td>210</td>
<td></td>
<td>ns</td>
<td>Counter Mode</td>
</tr>
<tr>
<td></td>
<td>tS(TR)</td>
<td>Trigger Setup Time to Rising Edge of Φ for enabling of Prescaler on Following Rising Edge of Φ</td>
<td>50</td>
<td></td>
<td>ns</td>
<td>Counter Mode</td>
</tr>
<tr>
<td></td>
<td>τW(ATH)</td>
<td>Clock and Trigger High Pulse Width</td>
<td>200</td>
<td></td>
<td>ns</td>
<td>Counter and Timer Modes</td>
</tr>
<tr>
<td></td>
<td>τW(CTL)</td>
<td>Clock and Trigger Low Pulse Width</td>
<td>200</td>
<td></td>
<td>ns</td>
<td>Counter and Timer Modes</td>
</tr>
<tr>
<td>ZC/TOQ0–2</td>
<td>τD(ZC)</td>
<td>ZC/TO Delay Time from Rising Edge of Φ, ZC/TO High</td>
<td>190</td>
<td></td>
<td>ns</td>
<td>Counter Mode</td>
</tr>
<tr>
<td></td>
<td>τD(LZC)</td>
<td>ZC/TO Delay Time from Falling Edge of Φ, ZC/TO Low</td>
<td>190</td>
<td></td>
<td>ns</td>
<td>Counter and Timer Modes</td>
</tr>
</tbody>
</table>

### Notes:

1. τC = τP(ΦH) + τP(ΦL) + τR + τF.
2. Increase delay by 10 nsec for each 50 pF increase in loading, 200 pF maximum for data lines and 100 pF for control lines.
3. Increase delay by 2 nsec for each 10 pF increase in loading, 100 pF maximum.
4. RESET must be active for a minimum of 3 clock cycles.

#### OUTPUT LOAD CIRCUIT

![Output Load Circuit Diagram](attachment:image.png)
### 8-BIT ARITHMETIC AND LOGICAL GROUP

<table>
<thead>
<tr>
<th>Mnemonic</th>
<th>Symbolic Operation</th>
<th>Flags</th>
<th>Op-Code</th>
<th>No. of Bytes</th>
<th>Cycles</th>
<th>States</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADD A, r</td>
<td>A - A + r</td>
<td></td>
<td>10 000</td>
<td>1</td>
<td>1</td>
<td>4</td>
<td>r Reg.</td>
</tr>
<tr>
<td>ADD A, n</td>
<td>A - A + n</td>
<td></td>
<td>11 000</td>
<td>1</td>
<td>2</td>
<td>7</td>
<td>000 B</td>
</tr>
<tr>
<td>ADD A, (HL)</td>
<td>A - A + (HL)</td>
<td></td>
<td>10 000</td>
<td>1</td>
<td>1</td>
<td>2</td>
<td>011 E</td>
</tr>
<tr>
<td>ADD A, (IX+d)</td>
<td>A - A + (IX+d)</td>
<td></td>
<td>11 011</td>
<td>1</td>
<td>3</td>
<td>5</td>
<td>011 H</td>
</tr>
<tr>
<td>ADD A, (IX+d)</td>
<td>A - A + (IX+d)</td>
<td></td>
<td>10 000</td>
<td>1</td>
<td>1</td>
<td>2</td>
<td>011 A</td>
</tr>
<tr>
<td>ADC A, s</td>
<td>A - A + CY</td>
<td></td>
<td>000</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>s is any of r, n.</td>
</tr>
<tr>
<td>SUB A</td>
<td>A - A - r</td>
<td></td>
<td>010</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>(HL), (IX+d),</td>
</tr>
<tr>
<td>SBC A, s</td>
<td>A - A - CY</td>
<td></td>
<td>011</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>(HL) as shown for</td>
</tr>
<tr>
<td>AND A</td>
<td>A - A - r</td>
<td></td>
<td>000</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>ADD instruction.</td>
</tr>
<tr>
<td>OR A</td>
<td>A - A - r</td>
<td></td>
<td>110</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>The indicated bits</td>
</tr>
<tr>
<td>XOR A</td>
<td>A - A - r</td>
<td></td>
<td>100</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>replace the 000 in</td>
</tr>
<tr>
<td>CP A</td>
<td>A - A - r</td>
<td></td>
<td>110</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>the ADD set above.</td>
</tr>
</tbody>
</table>

### JUMP GROUP

<table>
<thead>
<tr>
<th>Mnemonic</th>
<th>Symbolic Operation</th>
<th>Flags</th>
<th>Op-Code</th>
<th>No. of Bytes</th>
<th>Cycles</th>
<th>States</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>JP nn</td>
<td>PC - nn</td>
<td></td>
<td>11 000</td>
<td>1</td>
<td>3</td>
<td>3</td>
<td>10</td>
</tr>
<tr>
<td>JP cc, nn</td>
<td>if condition cc is true PC - nn, otherwise continue</td>
<td></td>
<td>11 cc 010</td>
<td>3</td>
<td>3</td>
<td>10</td>
<td>cc</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>cc</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>NZ non zero</td>
</tr>
<tr>
<td>001</td>
<td>Z zero</td>
</tr>
<tr>
<td>010</td>
<td>NC non carry</td>
</tr>
<tr>
<td>011</td>
<td>C carry</td>
</tr>
<tr>
<td>100</td>
<td>PO parity odd</td>
</tr>
<tr>
<td>101</td>
<td>PE parity even</td>
</tr>
<tr>
<td>110</td>
<td>P sign positive</td>
</tr>
<tr>
<td>111</td>
<td>M sign negative</td>
</tr>
</tbody>
</table>
LD A,(rp) — LOAD ACCUMULATOR FROM MEMORY LOCATION
ADRESSED BY REGISTER PAIR

Load the contents of the memory byte (addressed by the BC or DE register pair) into the Accumulator.

Suppose the B register contains 0816, the C register contains 4A16, and memory byte 084A16 contains 3A16. After the instruction

```
LD A (BC)
```

has executed, the Accumulator will contain 3A16.

Normally, the LD A (rp) and LD rp.data will be used together since the LD rp.data instruction loads a 16-bit address into the BC or DE registers as follows:

```
LD BC 084AH
LD A (BC)
```
OUT (port),A — OUTPUT FROM ACCUMULATOR

Output the contents of the Accumulator to the I/O port identified by the second OUT instruction object code byte.

Suppose $36_{16}$ is held in the Accumulator. After the instruction

\[
\text{OUT (1A\textsubscript{H}),A}
\]

has executed, $36_{16}$ will be in the buffer of I/O port 1A\textsubscript{16}.

The OUT instruction does not affect any statuses. Use of the OUT instruction is very hardware-dependent. Valid I/O port addresses are determined by the way in which I/O logic has been implemented. It is also possible to design a microcomputer system that accesses external logic using memory reference instructions with specific memory addresses. OUT instructions are frequently used in special ways to control microcomputer logic external to the CPU.
**NORMAL MODE OF CCD CLOCKING**

**DESIGNED BY JOSEPH Y. PAI**

<table>
<thead>
<tr>
<th>Line</th>
<th>Assembly Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0060</td>
<td>DPA EQU 80H</td>
<td>DA OF PIO</td>
</tr>
<tr>
<td>0061</td>
<td>DPB EQU 81H</td>
<td>DB OF PIO</td>
</tr>
<tr>
<td>0062</td>
<td>CPA EQU 82H</td>
<td>CA OF PIO</td>
</tr>
<tr>
<td>0063</td>
<td>CPB EQU 83H</td>
<td>CB OF PIO</td>
</tr>
<tr>
<td>1800</td>
<td>PV1 EQU 1800H</td>
<td>1st VALUE</td>
</tr>
<tr>
<td>1801</td>
<td>PV2 EQU 1801H</td>
<td>2nd VALUE</td>
</tr>
<tr>
<td>0000</td>
<td>ORG 2000H</td>
<td>CONTROL WD</td>
</tr>
<tr>
<td>0002</td>
<td>OUT (CPA),A</td>
<td></td>
</tr>
<tr>
<td>0004</td>
<td>OUT (CPB),A</td>
<td></td>
</tr>
<tr>
<td>0006</td>
<td>LD A,OFH</td>
<td></td>
</tr>
<tr>
<td>0009</td>
<td>CP OOH</td>
<td>VALUE=0?</td>
</tr>
<tr>
<td>000B</td>
<td>JP NZ,2016H;&lt;&gt;O,GO ON</td>
<td></td>
</tr>
<tr>
<td>000E</td>
<td>ERDIS LD IX,2070H;DISPLAY</td>
<td></td>
</tr>
<tr>
<td>0012</td>
<td>CALL SCAN ;BUILT-IN</td>
<td></td>
</tr>
<tr>
<td>0015</td>
<td>RST 38H</td>
<td>RETURN TO MONITOR.</td>
</tr>
<tr>
<td>0016</td>
<td>OUT (DPA),A</td>
<td>OUT TO DPA</td>
</tr>
<tr>
<td>0018</td>
<td>LD A,00H</td>
<td>READY TO</td>
</tr>
<tr>
<td>001A</td>
<td>OUT (DPB),A</td>
<td>GENERATE</td>
</tr>
<tr>
<td>001C</td>
<td>LD A,01H</td>
<td>A POSITIVE</td>
</tr>
<tr>
<td>001E</td>
<td>OUT (DPB),A</td>
<td>PULSE TO</td>
</tr>
<tr>
<td>0020</td>
<td>LD A,00H</td>
<td>LATCH</td>
</tr>
<tr>
<td>0022</td>
<td>OUT (DPB),A</td>
<td>1st DATA.</td>
</tr>
<tr>
<td>0024</td>
<td>LD A,(PV2)</td>
<td>GET 2nd VAL</td>
</tr>
<tr>
<td>0027</td>
<td>CP OOH</td>
<td>VALUE=0?</td>
</tr>
<tr>
<td>0029</td>
<td>JP 2,200EH;= 0, STOP.</td>
<td></td>
</tr>
<tr>
<td>002C</td>
<td>OUT (DPA),A</td>
<td>OUT TO DPA</td>
</tr>
<tr>
<td>002E</td>
<td>LD A,02H</td>
<td>GENERATE</td>
</tr>
<tr>
<td>0030</td>
<td>OUT (DPB),A</td>
<td>A PULSE TO</td>
</tr>
<tr>
<td>0032</td>
<td>LD A,00H</td>
<td>LATCH</td>
</tr>
<tr>
<td>0034</td>
<td>OUT (DPB),A</td>
<td>2nd DATA.</td>
</tr>
<tr>
<td>0000</td>
<td>ORG 2000H</td>
<td>CONTROL WD</td>
</tr>
<tr>
<td>0002</td>
<td>OUT (CPA),A</td>
<td></td>
</tr>
<tr>
<td>0004</td>
<td>OUT (CPB),A</td>
<td></td>
</tr>
<tr>
<td>0006</td>
<td>LD A,OFH</td>
<td></td>
</tr>
<tr>
<td>0009</td>
<td>CP OOH</td>
<td>VALUE=0?</td>
</tr>
<tr>
<td>000B</td>
<td>JP NZ,2016H;&lt;&gt;O,GO ON</td>
<td></td>
</tr>
<tr>
<td>000E</td>
<td>ERDIS LD IX,2070H;DISPLAY</td>
<td></td>
</tr>
<tr>
<td>0012</td>
<td>CALL SCAN ;BUILT-IN</td>
<td></td>
</tr>
<tr>
<td>0015</td>
<td>RST 38H</td>
<td>RETURN TO MONITOR.</td>
</tr>
<tr>
<td>0016</td>
<td>OUT (DPA),A</td>
<td>OUT TO DPA</td>
</tr>
<tr>
<td>0018</td>
<td>LD A,00H</td>
<td>READY TO</td>
</tr>
<tr>
<td>001A</td>
<td>OUT (DPB),A</td>
<td>GENERATE</td>
</tr>
<tr>
<td>001C</td>
<td>LD A,01H</td>
<td>A POSITIVE</td>
</tr>
<tr>
<td>001E</td>
<td>OUT (DPB),A</td>
<td>PULSE TO</td>
</tr>
<tr>
<td>0020</td>
<td>LD A,00H</td>
<td>LATCH</td>
</tr>
<tr>
<td>0022</td>
<td>OUT (DPB),A</td>
<td>1st DATA.</td>
</tr>
<tr>
<td>0024</td>
<td>LD A,(PV2)</td>
<td>GET 2nd VAL</td>
</tr>
<tr>
<td>0027</td>
<td>CP OOH</td>
<td>VALUE=0?</td>
</tr>
<tr>
<td>0029</td>
<td>JP 2,200EH;= 0, STOP.</td>
<td></td>
</tr>
<tr>
<td>002C</td>
<td>OUT (DPA),A</td>
<td>OUT TO DPA</td>
</tr>
<tr>
<td>002E</td>
<td>LD A,02H</td>
<td>GENERATE</td>
</tr>
<tr>
<td>0030</td>
<td>OUT (DPB),A</td>
<td>A PULSE TO</td>
</tr>
<tr>
<td>0032</td>
<td>LD A,00H</td>
<td>LATCH</td>
</tr>
<tr>
<td>0034</td>
<td>OUT (DPB),A</td>
<td>2nd DATA.</td>
</tr>
</tbody>
</table>
53       LD  A,80H
54       OUT (DPB),A
55       ;******************************
56       ;* GENERATE A POSITIVE PULSE *
57       ;* THROUGH B7 TO START THE *
58       ;* SYSTEM. IN OTHER WORDS, *
59       ;* S* HAS BEEN GENERATED. *
60       ;******************************
61       
62       RST 38H ;TO MONITOR
63       ;
64       
65       ;INTERNAL CODE OF "F"
66       ;AS ERROR MEASAGE.
67       
68       
69       
70       
71       SCAN  EQU 05FEH
72       ;"SCAN" BUILT-IN SUBROUTINE.
73       END
;**************************************************************
;* P* AND S* SIGNALS GENERATED
;* DESIGNED BY JOSEPH Y. PAI
;**************************************************************

-0040 10 CTC0 EQU 40H ;CHANNEL 0 CTC
-0041 11 CTC1 EQU 41H ;CHANNEL 1 CTC
-0080 12 DPA EQU 80H ;DA OF PIO
-0081 13 DPB EQU 81H ;DB OF PIO
-0082 14 CPA EQU 82H ;CA OF PIO
-0083 15 CPB EQU 83H ;CB OF PIO
-1800 16 PV1 EQU 1800H ;1st VALUE
-1801 17 PV2 EQU 1801H ;2nd VALUE
-1802 18 PV3 EQU 1802H ;3rd VALUE
-1803 19 PV4 EQU 1803H ;4th VALUE
20

-0000
2100 -3E 0F 21 ORG 2100H
2102 -D3 82 22 LD A,OFH ;CONTROL WORD
2104 -D3 83 23 OUT (CPA),A ;FOR PIO A PORT

;**************************************************************
;* PORT A AND PORT B ARE SET TO BE OUTPUT PORTS.
;**************************************************************

2106 -3A 00 18 30 LD A,(PV1) ;GET 1st VALUE
2109 -FE 00 31 CP 00H ;VALUE=0?
210B -C2 16 21 32 JP NZ,2116H ;<>0, GO ON
210E -DD 21 70 33 ERDIS LD IX,2170H ;DISPLAY
2112 -CD FE 05 34 21 35 CALL SCAN ;BUILT-IN SUB-
2115 -FF 36 37 ;DISPLAY "DDDD DD" AS ERROR-MEASAGE.
2116 -D3 80 38 RST 38H ;STOP
2118 -3E 00 39 ; RETURN TO MONITOR.
211A -D3 81 40 OUT (DPA),A ;OUT TO DPA.
211C -3E 01 41 LD A,OOH ;READY TO
211E -D3 81 42 OUT (DPB),A ;GENERATE
2120 -3E 00 43 LD A,01H ;A POSITIVE
2122 -D3 81 44 OUT (DPB),A ;PULSE TO
2124 -3A 01 16 45 LD A,OOH ;LATCH
46 OUT (DPA),A ;1st DATA.
47 ;1st DATA HAS BEEN LATCHED.
2124 -3A 01 16 48 LD A,(PV2) ;GET 2nd VALUE.
2127 -FE 00 49 CP 00H ;VALUE=0?
2129 -CA OE 21 50 JP Z,210EH ^= 0, STOP.
51 ; RETURN TO MONITOR.
212C -D3 80 52 OUT (DPA),A ;OUT TO DPA.
212E -3E 02  LD A,02H ;GENERATE
2130 -D3 81  OUT (DPB),A ;A PULSE TO
2132 -3E 00  LD A,COH ;LATCH
2134 -D3 81  OUT (DPB),A ;2nd DATA.
57 ; 2nd DATA HAS BEEN LATCHED.
2136 -3E 55  LD A,55H ;CONTROL WORD
2138 -D3 40  OUT (CTCO),A ;FOR CTCO.
213A -3A 02 18 60  LD A,(PV3) ;GET 3rd VALUE.
213D -D3 40  OUT (CTCO),A ;CONSTANT REG.
213F -3E 55 62  LD A,55H ;CONTROL WORD
2141 -D3 41 63  OUT (CTC1),A ;FOR CTC1.
2143 -3A 03 18 64  LD A,(PV4) ;GET 4th VALUE.
2146 -D3 41 65  OUT (CTC1),A ;CONSTANT REG.
2148 -3E 40 71  LD A,40H ;FOR P* GENER.
214A -D3 81 72  OUT (DPB),A ;P* IS HIGH.
214C -3E C0 73  LD A,OCOH ;FOR S* GENER.
214E -D3 81 74  OUT (DPB),A ;P* AND S* ARE
75 ; HIGH.
2150 -FF 80  RST 38H ;TO MONITOR.
2170 -B3 82 ;INTERNAL CODE OF "D"
2171 -B3 83 ;AS ERROR MEASAGE.
2172 -B3 84
2173 -B3 85
2174 -B3 86
2175 -B3 87
-O5FE 88 SCAN EQU 05FEH
89 ;"SCAN" BUILT-IN SUBROUTINE.
90  END
-0081 10 DPB EQU 81H ;DB OF PIO.
-0083 11 CPB EQU 83H ;CB OF PIO.

2200 -3E 0F -0000

2202 -D3 83 13 ORG 2200H

2204 -3E 00 14 LD A,OFH ;CONTROL WORD
2206 -D3 81 15 OUT (CPB),A ;FOR CPB.

2208 -FF 19 LD A,00H ;CLEAR B PORT

16 ;****************************************************************************
17 ;* SET B PORT OF PIO TO BE OUTPUT. *
18 ;****************************************************************************
22 ;****************************************************************************
23 ;****************************************************************************
24 ;****************************************************************************
25 ;****************************************************************************
26 ;****************************************************************************

2208 -FF 27 RST 38H ;TO MONITOR.
29 ;
END
APPENDIX C

******************************
DATA SHEETS OF RELEVANT TTL's
******************************

1. 74LS123 ................. C-2
2. 74LS169 ................. C-4
3. 74221 .................. C-6
TYPES SN54122, SN54123, SN54L122, SN54L123, SN54LS122, SN54LS123, SN74122, SN74123, SN74L122, SN74L123, SN74LS122, SN74LS123

RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

- D-C Triggered from Active-High or Active-Low Gated Logic Inputs
- Retriggerable for Very Long Output Pulses, Up to 100% Duty Cycle
- Overriding Clear Terminates Output Pulse
- Compensated for VCC and Temperature Variations
- '122, ‘L122,'LS122 Have Internal Timing Resistors

FUNCTION TABLE

<table>
<thead>
<tr>
<th>INPUTS</th>
<th>OUTPUTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLEAR</td>
<td>A</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>X</td>
<td>H</td>
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<td>H</td>
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<td>L</td>
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<td>L</td>
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FUNCTION TABLE

<table>
<thead>
<tr>
<th>INPUTS</th>
<th>OUTPUTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLEAR</td>
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<tr>
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<td>X</td>
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<td>H</td>
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<tr>
<td>H</td>
<td>H</td>
</tr>
</tbody>
</table>

See explanation of function tables on page 3-8.

description

These d-c triggered multivibrators feature output pulse width control by three methods. The basic pulse time is programmed by selection of external resistance and capacitance values (see typical application data). The '122, ‘L122, and ‘LS122 have internal timing resistors that allow the circuits to be used with only an external capacitor, if so desired. Once triggered, the basic pulse width may be extended by retriggering the gated low-level-active (A) or high-level-active (B) inputs, or be reduced by use of the overriding clear. Figure 1 illustrates pulse control by retriggering and early clear.

The ‘LS122 and ‘LS123 are provided enough Schmitt hysteresis to ensure jitter-free triggering from the B input with transition rates as slow as 0.1 millivolt per nanosecond.

NOTES
1. An external timing capacitor may be connected between Cext and Rext/Cext Internacional.
2. To use the internal timing resistors of ‘122,’ ‘L122 or ‘LS122, connect Rext to VCC.
3. For improved pulse width accuracy and repeatability, connect an external resistor across Rext, but use Rext = 10 kΩ with Rext open-circuited.
4. To obtain variable pulse widths, connect an external variable resistance between Rext and Cext. 

SN54122, SN54LS122... J OR W
SN54L122... J OR T
SN74122, SN74LS122... J OR N
(TOP VIEW: SEE NOTES 1 THRU 4)
TYPES SN54LS122, SN74LS122, SN54LS123, SN74LS123
RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

TYPICAL APPLICATION DATA FOR 'LS122, 'LS123

The basic output pulse width is essentially determined by the values of external capacitance and timing resistance. For pulse widths when $C_{\text{ext}} < 1000$ pF, see Figure 7.

When $C_{\text{ext}} > 1000$ pF, the output pulse width is defined as:

$$t_w = 0.45 \cdot R_T \cdot C_{\text{ext}}$$

where

- $R_T$ is in k$\Omega$ (internal or external timing resistance.)
- $C_{\text{ext}}$ is in pF
- $t_w$ is in nanoseconds

For best results, system ground should be applied to the $C_{\text{ext}}$ terminal. The switching diode is not needed for electrolytic capacitance applications.

'LS122, 'LS123
TYPICAL OUTPUT PULSE WIDTH
VS EXTERNAL TIMING CAPACITANCE

$C_{\text{ext}}$—External Timing Capacitance—pF

$R_T$—Resistor—k$\Omega$

The value of resistance exceeds the maximum recommended for use over the full temperature range of the SN54LS circuits.
description

These synchronous presettable counters feature an internal carry look-ahead for cascading in high-speed counting applications. The 'S168 is a decade counter and the 'LS169A and 'S169 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple-clock) counters. A buffered clock input triggers the four master-slave flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; that is, the outputs may each be preset to either level. The load input causes the outputs to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count-enable inputs (\( P \) and \( T \)) must be low to count. The direction of the count is determined by the level of the \( UP/DOWN \) input. When the input is high, the counter counts up; when low, it counts down. Input \( T \) is fed forward to enable the carry output. The carry output thus enabled will produce a low-level output pulse with a duration approximately equal to the high portion of the \( QA \) output when counting up and approximately equal to the low portion of the \( CA \) output when counting down. This low-level overflow carry pulse can be used to enable successive cascaded stages. Transitions at the enable \( P \) or \( T \) inputs are allowed regardless of the level of the clock input. All inputs are shield-coupled to minimize transmission-line effects, thereby simplifying system design.

These counters feature a fully independent clock circuit. Changes at control inputs \( ENABLE \) and \( LOAD \) (inputs that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable input and hold times.
**TYPES SN54LS169A, SN54S169, SN74LS169A, SN74S169**

SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

'S169A, 'S169 BINARY COUNTERS

typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to binary thirteen
2. Count up to fourteen, fifteen (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen

![Diagram of load, count, and inhibit sequences for SN54LS169A, SN54S169, SN74LS169A, SN74S169 synchronous 4-bit up/down counters.]
The '221 and 'LS221 are monolithic dual multivibrators with performance characteristics virtually identical to those of the '121. Each multivibrator features a negative-transition-triggered input and a positive-transition-triggered input either of which can be used as an inhibit input.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt trigger input circuitry (TTL hysteresis) for B input allows jitter-free triggering from inputs with transition rates as slow as 1 volt/second, providing the circuit with excellent noise immunity of typically 1.2 volts. A high immunity to VCC noise of typically 1.5 volts is also provided by internal latching circuitry.

Once fired, the outputs are independent of further transitions of the A and B inputs and are a function of the timing components, or the output pulses can be terminated by the overriding clear. Input pulses may be of any duration relative to the output pulse. Output pulse length may be varied from 35 nanoseconds to the maximums shown in the above table by choosing appropriate timing components. With \( R_{xx} = 2 \, k\Omega \) and \( C_{xx} = 0 \), an output pulse of typically 30 nanoseconds is achieved which may be used as a d-c-triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length. Typical triggering and clearing sequences are illustrated as a part of the switching characteristics waveforms.

Pulse width stability is achieved through internal compensation and is virtually independent of VCC and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

Jitter-free operation is maintained over the full temperature and VCC ranges for more than six decades of timing capacitance (10 pF to 10 \( \mu F \)) and more than one decade of timing resistance (2 k\( \Omega \) to 30 k\( \Omega \) for the SN54221, 2 k\( \Omega \) to 40 k\( \Omega \) for the SN74221, 2 k\( \Omega \) to 70 k\( \Omega \) for the SN54LS221, and 2 k\( \Omega \) to 100 k\( \Omega \) for the SN74LS221). Throughout these ranges, pulse width is defined by the relationship:

\[
t_{(\text{on})} = C_{ext} R_{ext} \ln 2 \approx 0.7 C_{ext} R_{ext}.
\]

In circuits where pulse overlap is not critical, timing capacitance up to 1000 \( \mu F \) and timing resistance as low as 1.4 k\( \Omega \) may be used. Also, the range of jitter-free output pulse widths is extended if VCC is

\( \text{TYPICAL} \)
TYPES SN54221, SN74221
DUAL MONOSTABLE MULTIVIBRATORS
WITH SCHMITT-TRIGGER INPUTS

**recommended operating conditions**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SN54221</th>
<th>SN74221</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage, VCC</td>
<td>4.5</td>
<td>4.75</td>
</tr>
<tr>
<td>High-level output current, IOH</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>Low-level output current, IOH</td>
<td>5.5</td>
<td>5.25</td>
</tr>
<tr>
<td>Low-level output current, IOH</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>Rate of rise or fall of input pulse, dv/dt</td>
<td>18</td>
<td>18</td>
</tr>
<tr>
<td>Input pulse width</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>External timing resistance, REXT</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>External timing capacitance, CEXT</td>
<td>0</td>
<td>1000</td>
</tr>
<tr>
<td>Output duty cycle</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Operating free-air temperature, TA</td>
<td>-55</td>
<td>70</td>
</tr>
</tbody>
</table>

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VT+ Positive-going threshold voltage at A input</td>
<td>VCC = MIN</td>
<td>1.4</td>
<td>2</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VT Negative-going threshold voltage at A input</td>
<td>VCC = MIN</td>
<td>0.8</td>
<td>1.4</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VT+ Positive-going threshold voltage at B input</td>
<td>VCC = MIN</td>
<td>1.65</td>
<td>2</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VT Negative-going threshold voltage at B input</td>
<td>VCC = MIN</td>
<td>0.8</td>
<td>1.35</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VR Input clamp voltage</td>
<td>VCC = MIN,</td>
<td>-1.5</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VON High-level output voltage</td>
<td>VCC = MIN, IOH = 800 mA</td>
<td>2.4</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VON Low-level output voltage</td>
<td>VCC = MIN, IOH = 80 mA</td>
<td>0.2</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I1 Input current at maximum input voltage</td>
<td>VCC = MAX, V1 = 5.5 V</td>
<td>1</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I1 High-level input current</td>
<td>VCC = MAX, V1 = 2.4 V</td>
<td>40</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I1 Low-level input current</td>
<td>VCC = MAX, V1 = 0.4 V</td>
<td>-1.6</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IQS Short-circuit output current</td>
<td>VCC = MAX</td>
<td>SN54221 -20</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ICC Supply current</td>
<td>VCC = MAX</td>
<td>SN74221 -55</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
2All typical values are at VCC = 5 V, TA = 25°C.
3Not more than one output should be shorted at a time.

switching characteristics, VCC = 5 V, TA = 25°C

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>FROM (INPUT)</th>
<th>TO (OUTPUT)</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>tPLH</td>
<td>A or B</td>
<td>Q or Q'</td>
<td>Cext = 80 pF, Rext = 2 kΩ</td>
<td>45</td>
<td>70</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tPHL</td>
<td>A or B</td>
<td>Q or Q'</td>
<td>Cext = 80 pF, Rext = 2 kΩ</td>
<td>50</td>
<td>80</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tPLH</td>
<td>Clear</td>
<td>Q or Q'</td>
<td>Cext = 80 pF, Rext = 2 kΩ</td>
<td>40</td>
<td>65</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tPHL</td>
<td>A or B</td>
<td>Q or Q'</td>
<td>Cext = 80 pF, Rext = 2 kΩ</td>
<td>27</td>
<td>40</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

1tPLH = Propagation delay time, low-to-high-level output
2tPHL = Propagation delay time, high-to-low-level output
3tPLH = Output pulse width

NOTE 2: Load circuit is shown on page 3-10.
APPENDIX D

*MEASUREMENTS OF THE DRIVERS*

1. The Measurements of Ø1 Driver ........... D-2
2. The Measurements of Ø2 Driver ........... D-3
Below are the measurements for one clock. A 750 pfd test load was used. Measurements were made with a 100 MHz oscilloscope with a 10:1 probe with a 1 Megohm input resistance shunted by 12 pfd. The results show that the upper level of the output can be set between 7.0 volts and 9.0 volts, with the lower levels between 1 and 3 volts. Rise times were in the range of 1 usec, while fall times typically were 700 nsec.

The measurements of Ø1 driver

<table>
<thead>
<tr>
<th>ohm</th>
<th>R1</th>
<th>R2</th>
<th>V</th>
<th>nsec rise time</th>
<th>nsec fall time</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1 K</td>
<td>0</td>
<td>outputs low high</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 K</td>
<td>0</td>
<td>0</td>
<td>1.0 7.0</td>
<td>1000</td>
<td>100</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1.0 9.2</td>
<td>600</td>
<td>100</td>
</tr>
<tr>
<td>0</td>
<td>500</td>
<td>0</td>
<td>2.9 8.4</td>
<td>900</td>
<td>700</td>
</tr>
<tr>
<td>1 K</td>
<td>500</td>
<td>0</td>
<td>2.3 7.4</td>
<td>1000</td>
<td>600</td>
</tr>
<tr>
<td>500</td>
<td>250</td>
<td>0</td>
<td>2.0 8.0</td>
<td>1400</td>
<td>600</td>
</tr>
<tr>
<td>0</td>
<td>250</td>
<td>0</td>
<td>2.0 8.9</td>
<td>840</td>
<td>500</td>
</tr>
<tr>
<td>1 K</td>
<td>250</td>
<td>0</td>
<td>2.0 8.4</td>
<td>840</td>
<td>600</td>
</tr>
<tr>
<td>500</td>
<td>0</td>
<td>0</td>
<td>1.0 8.6</td>
<td>1400</td>
<td>800</td>
</tr>
<tr>
<td>500</td>
<td>500</td>
<td>0</td>
<td>2.8 8.0</td>
<td>1100</td>
<td>700</td>
</tr>
</tbody>
</table>

Notes:
1. Load Circuit: +12 V

2. R1 = 0 to 1 Kohm.
   R2 = 0 to 500 ohm.
Below are the measurements for one clock. The table shows the relationship of the preset value and the width of $\phi_2$. The preset value is from 1 to 15 and the increasing step for the width of $\phi_2$ is 0.8 μsec.

The measurements of $\phi_2$ driver

<table>
<thead>
<tr>
<th>The preset value</th>
<th>The width of $\phi_2$ μsec</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1.6</td>
</tr>
<tr>
<td>2</td>
<td>2.4</td>
</tr>
<tr>
<td>3</td>
<td>3.2</td>
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<tr>
<td>4</td>
<td>4.0</td>
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<td>4.3</td>
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<td>6</td>
<td>5.6</td>
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<td>7</td>
<td>6.4</td>
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<td>8.0</td>
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<td>8.3</td>
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<td>11</td>
<td>9.6</td>
</tr>
<tr>
<td>12</td>
<td>10.4</td>
</tr>
<tr>
<td>13</td>
<td>11.2</td>
</tr>
<tr>
<td>14</td>
<td>12.0</td>
</tr>
<tr>
<td>15</td>
<td>12.8</td>
</tr>
</tbody>
</table>

Notes:

1. The preset value is sent from the system microcomputer.

2. There is no loading at the output.