COMPLEMENTARY ORTHOGONAL STACKED METAL OXIDE SEMICONDUCTOR: A NOVEL NANOSCALE COMPLEMENTARY METAL OXIDE SEMICONDUCTOR ARCHITECTURE

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Ahmad Aziz Al-Ahmadi
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COMPLEMENTARY ORTHOGONAL STACKED METAL OXIDE SEMICONDUCTOR: A NOVEL NANOSCALE COMPLEMENTARY METAL OXIDE SEMICONDUCTOR ARCHITECTURE

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Abstract

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COMPLEMENTARY ORTHOGNAL STACKED METAL OXIDE SEMICONDUCTOR : A NOVEL NANOSCALE COMPLEMENTARY METAL OXIDE SEMICONDUCTOR ARCHITECTURE (103 pp.)

Director of Dissertation: Savas Kaya

This dissertation presents a simulation study of a novel CMOS device architecture capable of building complementary logic operation using only a single gate stack. The new architecture, named complementary orthogonal stacked MOS (COSMOS), places the n and p-MOSFETs perpendicular to one another under a single gate. As a result of concurrent vertical and lateral integration, the COSMOS architecture can lead to dramatic savings in active device area of a conventional static CMOS pair, as well as significant reductions in R-C device parasitics. We demonstrate how the COSMOS devices may be built, operated, and optimized for symmetric operation, also verifying logic operation via 3D device simulations. The proposed COSMOS architecture is based on strained Si/SiGe on insulator (SSOI) technology that has recently become available. This work is the first comprehensive treatment of general properties of COSMOS architecture to our knowledge and should allow designers to understand and design COSMOS devices and circuits in future.

Approved:

Savas Kaya
Assistant Professor of Electrical Engineering and Computer Science
I would like to dedicate this work to:

My parents, Aziz and Norah

My wife, Ameenah

My children: Shatha, Wejdan, Rana, Abdulaziz and Jude

Each gave me the support, confidence, and love over the years to reach for my dreams
Acknowledgments

In the name of Allah (god), the Most Beneficent, the Most Merciful. All praise and thanks to Allah Lord of the universe and all that exists. I am grateful to Allah for giving me the strength and patience to finish this work.

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# List of Abbreviations

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
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<tbody>
<tr>
<td>COSMOS</td>
<td>Complementary orthogonal stacked Metal Oxide Semiconductor</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal Oxide Semiconductor Field Effect Transistor</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complementary Metal Oxide Semiconductor</td>
</tr>
<tr>
<td>IC</td>
<td>Integrated Circuit</td>
</tr>
<tr>
<td>SCE</td>
<td>Short Channel Effects</td>
</tr>
<tr>
<td>LER</td>
<td>line edge roughness</td>
</tr>
<tr>
<td>SOI</td>
<td>Silicon on Insulator</td>
</tr>
<tr>
<td>BOX</td>
<td>Buried Oxide</td>
</tr>
<tr>
<td>UTB</td>
<td>Ultra-Thin body</td>
</tr>
<tr>
<td>TCAD</td>
<td>Technology Computer Aided Simulation</td>
</tr>
<tr>
<td>ISE</td>
<td>Integrated Systems Engineering</td>
</tr>
<tr>
<td>DD</td>
<td>Drift-Diffusion</td>
</tr>
<tr>
<td>2DEG</td>
<td>2-dimensional electron gas</td>
</tr>
<tr>
<td>2DHG</td>
<td>2-dimensional hole gas</td>
</tr>
<tr>
<td>SiGe</td>
<td>Silicon Germanium</td>
</tr>
<tr>
<td>ITRS</td>
<td>International Technology Roadmap for Semiconductors</td>
</tr>
<tr>
<td>DIBL</td>
<td>Drain-Induced Barrier Lowering</td>
</tr>
<tr>
<td>FPGAs</td>
<td>Field Programmable Gate Arrays</td>
</tr>
<tr>
<td>SRC</td>
<td>Semiconductor Research Corporation</td>
</tr>
</tbody>
</table>
Chapter One

Introduction

1.1 General Introductions

The heart of every digital circuit is MOSFET (metal-oxide-semiconductor field effect transistor). The first MOSFET was fabricated in 1960, one year after the IC (integrated circuit). The MOSFET is four terminal devices (source, drain, gate and substrate). With no voltage applied to the gate, there is no current flow, so the current is controlled by the vertical applied electric filed.

There are two type of MOSFET n-MOSFET and p-MOSFET. The n-MOSFET consists of a source and a drain, which are isolated from the p-type substrate by reversed-biased p-n diodes. The gate covers the area between source and drain, and it separated from the semiconductor by the gate oxide. The basic structure of an n-MOSFET is shown in Figure 1.1a. When we apply voltage between the gate and the source terminals, the electric field penetrates throughout the oxide and creates a channel underneath in which current can pass. The channel is of the same type p-type or n-type as the source and drain [7]. The main advantages of the MOSFET are its simple structure and low fabrication cost [8].

The growth of digital technologies like microprocessors, memory, etc has provided the motivation to advance MOSFETs as building blocks. The reason for the success of the MOSFET was the development of CMOS digital logic. The first CMOS integrated circuit fabricated in 1968 was a combination of nMOSFET with a pMOSFET, wiring the same input to both in such a way that whenever one is conducting, the other is not (see Figure 1.1b)[7].
The major advantage of a CMOS device is the conservation of energy since it consumes very little energy when idle, when the input to logic gates is being switched it consumes much more energy. In addition, it prevents overheating that would cause chips to fail, resulting in vastly improved performance. This allows integrating many more CMOS gates on an IC than in bipolar technology that has large power dissipation. CMOS also allows a high density of logic functions on a chip.

The continuous need for more complex and higher performance circuits has led in the last 30 years to an amazing scaling down of IC technologies. In 1965, Gordon E. Moore predicted that the number of minimum cost components per IC would increase at a rate of roughly two per year. This prediction was, of course, for digital circuits. In 1975, Moore reviewed the "slope" of his prediction for the future, saying that the number of transistors per chip would double every 18 months. In 1996, the definition of “Moore’s
“Moore’s Law” has come to refer to almost anything related to the semiconductor industry, that when plotted on semi-log paper, approximates a straight line.

The scaling of CMOS technology has progressed so rapidly year after year that the Semiconductor Industry Association (SIA) has been publishing roadmaps for semiconductor technology since 1992. These roadmaps correspond to a outlook of industry trends, using history as a basis (see Table 1.1)[7][10]. As can be seen from this table, silicon devices in the next 10 years will deal with sub-100 nm scales and reach down to 20 nm range in gate length. Thus, any effort with silicon devices should consider dimensions in this range to be relevant for industry plans.

Table 1.1  Highlight of the 2000/2001 Semiconductor Industry Association National Technology Road Map for Semiconductors [9].

<table>
<thead>
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<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Feature Size</td>
<td>microns/nm</td>
<td>0.50</td>
<td>0.35</td>
<td>180</td>
<td>130</td>
<td>100</td>
<td>80</td>
<td>70</td>
<td>50</td>
<td>34</td>
<td>22</td>
</tr>
<tr>
<td>Internal Clock high performance</td>
<td>Mhz/Ghz</td>
<td>200</td>
<td>300</td>
<td>750</td>
<td>1.68</td>
<td>2.31</td>
<td>5.17</td>
<td>6.74</td>
<td>11.5</td>
<td>19.3</td>
<td>28.7</td>
</tr>
<tr>
<td>Logic transistors</td>
<td>million/cm²</td>
<td>2</td>
<td>4</td>
<td>6.6</td>
<td>13</td>
<td>24</td>
<td>44</td>
<td>109</td>
<td>269</td>
<td>664</td>
<td></td>
</tr>
<tr>
<td>Microprocessor</td>
<td>million transistors/chip</td>
<td>5.2</td>
<td>12</td>
<td>23.8</td>
<td>47.6</td>
<td>95.2</td>
<td>190</td>
<td>539</td>
<td>1523</td>
<td>4308</td>
<td></td>
</tr>
<tr>
<td>DRAM size</td>
<td>Mbit/Gbit</td>
<td>16</td>
<td>64</td>
<td>256</td>
<td>512</td>
<td>1</td>
<td>2</td>
<td>6</td>
<td>16</td>
<td>48</td>
<td></td>
</tr>
<tr>
<td>SRAM size</td>
<td>Mbit/Gbit</td>
<td>1</td>
<td>4</td>
<td>16</td>
<td>64</td>
<td>256</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Voltage</td>
<td>$V_{dd}$</td>
<td>5</td>
<td>3.3</td>
<td>2.5</td>
<td>1.2</td>
<td>1.0</td>
<td>0.9</td>
<td>0.7</td>
<td>0.6</td>
<td>0.5</td>
<td>0.4</td>
</tr>
</tbody>
</table>
1.2 Scope and Objectives

Every technology has its limits; after more than two decades of continual rapid progress in scaling down the bulk CMOS transistor, it is apparent that we are finally approaching the limits of CMOS scaling. In its 2003 edition, the International Technology Roadmap for semiconductors [11] forecasts that gate dimension in MOSFETs should reach 10 nm by 2014. More recently, Intel has announced an accelerated version of the roadmap [12], which envisages 50 nm devices by 2007. These rapid developments make scaling an even more dramatic and critical story in the next ten years, and the stakes are the highest ever. In fact, the ever-closer fundamental limits in CMOS integration and MOSFET scaling, such as power dissipation and power density problem, may mean that conventional CMOS may never be scaled to 10 nm, and that the Moore’s law may have an abrupt end. Thus, it is imperative to investigate novel device structures using predictive device modeling, which can provide alternative scaling scenarios and may delay the expected end of the Si scaling until nano-scale engineering can demonstrate a viable device architecture that can replace the billion-transistor integration capability of MOSFET at a comparable cost. No novel nano-engineered device can yet match the integration robustness and cost effectiveness of Si MOSFET.

At Ohio University, we designed a novel CMOS device architecture capable of building a complementary logic operation using only a single gate stack. The new architecture, named complementary orthogonal stacked MOS (COSMOS), places the n and p-MOSFETs perpendicular to one another under a single gate, integrating them vertically as well as laterally [1-6] (see Figure 1.2).
Figure 1.2 Complementary orthogonal stacked MOS (COSMOS).
The COSMOS architecture would not only mean significant savings in the active device area of a conventional static CMOS pair, but also significant reductions in RC device parasitics. We have demonstrated how the device may be built, operated and optimized for symmetric operation, as well as verifying logic NOT operation via 3D device simulations. The proposed COSMOS architecture is based on strained Si/SiGe on insulator (SSOI) technology that has recently become available. Electrons in a COSMOS device are confined to the Si cap layer, while holes are kept in the strained SiGe layer between the Si cap and buried insulator layer on silicon. Consequently, a single gate can be used to control the mutually exclusive populations of channels, while the orthogonal layout allows access to two sets of source and drain contacts necessary for transistor action. Therefore, COSMOS not only provides ample savings in area size and parasitic, but also performance leverage via higher hole mobility resulting from strained engineering in the Si/SiGe channels.

COSMOS architecture has never been researched before. It possesses unique features that can help tackle some of the principle roadblocks in sub-50 nm scaling and integration at the end of Si roadmap. Thus, COSMOS may provide a paradigm shift in the way logic functions are produced on Si, and also a platform for studying their interdependence in novel architecture.
Chapter Two

CMOS Devices

2.1 Fundamentals of CMOS Transistor Scaling

This chapter aims at introducing the limitations and challenges of extending the ability of transistor scaling. Over the last three decades, the scaling of transistor has vastly improved integrated circuits. The aim of scaling is to reduce the device dimensions to improve the circuit’s performance, increase transistor density, and reduce power consumption without introducing effects, which can disturb the good operation of the device. However, shrinking the device dimensions with no consideration to other processing parameters gives rise to a variety of non-ideal characteristics. According to the scaling laws, the device dimensions, voltages, and doping profiles are required to be adjusted to keep the electric field constant. The increase in the electric field is the most serious problem of scaling, because it breaks down the oxide and hot carriers, causing anxiety for device reliability. To reduce the oxide field, one may scale the oxide thickness with $1/\alpha^{1/2}$ rather than $1/\alpha$. It is known that the work function difference, sub threshold current, and built in potential do not scale [13, 14]. On the other hand, the success of CMOS has relied mainly on device scaling, which lately has been accelerated, surpassing the sub-100 nm barrier [15]. However, these achievements also indicate that planar scaling is fast approaching its limits, both technologically, as well as principally [15-18]. The most interesting scaling features are reported in Table 2.1.
Table 2.1 Scaling Features for MOS Transistors.

<table>
<thead>
<tr>
<th>Basic Device Scaling</th>
<th>Scaling Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>1) Channel length L</td>
<td>Voltage: V/α</td>
</tr>
<tr>
<td>2) Power supply voltage V&lt;sub&gt;dd&lt;/sub&gt;</td>
<td>Oxide: t&lt;sub&gt;ox&lt;/sub&gt;/α</td>
</tr>
<tr>
<td>3) Threshold voltage V&lt;sub&gt;T&lt;/sub&gt;</td>
<td>Wire width: W/α</td>
</tr>
<tr>
<td>4) Gate oxide thickness t&lt;sub&gt;ox&lt;/sub&gt;</td>
<td>Gate width: L/α</td>
</tr>
<tr>
<td>Scaling goals:</td>
<td>Diffusion: x&lt;sub&gt;d&lt;/sub&gt;/α</td>
</tr>
<tr>
<td>1) Reduce gate delay</td>
<td>Substrate: α*N&lt;sub&gt;A&lt;/sub&gt;</td>
</tr>
<tr>
<td>2) Increase operating frequency</td>
<td></td>
</tr>
<tr>
<td>3) Increase transistor density</td>
<td></td>
</tr>
<tr>
<td>4) Reduce power dissipation</td>
<td></td>
</tr>
</tbody>
</table>

2.2 Overview of Sub-100 nm Scaling Challenges

The prediction of Moore's has been achieved through scaling MOSFET from larger device dimensions to smaller device dimensions. After more than two decades of frequent rapid improvement in scaling the bulk CMOS transistor, it is apparent that we are finally approaching the limits of CMOS scaling. The limitations of extending the ability of transistor scaling are of concern to various challenges.

2.2.1 Lithography

Lithography is the key technology for nano devices. To produce an integrated circuit, thin films of different materials are used as barriers for implantation or diffusion of impurity atoms. Photolithography is the selective process that allows the patterning of a desired design that we want to fabricate onto the material. Photo resist is the first step in
applying a pattern in a uniform film. The mask is a metal sheet that holds the actual pattern that will be etched into the photo resist. The mask is cut so that when a UV light is shined from behind the exposed parts of the photo resist, it will be the actual pattern. These exposed parts can then be cleaned away (positive resist) or will remain on the fabricated device (negative resist).

Optical lithography, the main technology used today, is predicted to be applicable beyond 100 nm and 70 nm with the use of, respectively, 193 nm and 157 nm wavelength tools. The reduction of feature sizes down to 50 nm and below will require more advanced lithography tools. As the candidate for the next generation for the microelectronics industry, X-Ray Lithography and Extreme Ultraviolet Lithography (EUV) are being strongly supported. EUV lithography, at the wavelength of 13 nm, will achieve feature size at 45 nm and below. As the projected costs for Next Generation Lithography tools increase, people are looking for faster, cheaper, and more reliable ways to create sub-100 nm structures [19-21].

2.2.2 Leakage and Device Parasitics

There are three main sources of leakage: junction leakage, gate leakage, and off-state leakage. As transistors are scaled down towards 50 nm these sources of leakage increase [8]. The junction leakage occurs from the source or drain to the substrate through the reverse biased diodes when a transistor is off. A reverse-biased pn junction leakage has two main components: one is minority carrier diffusion/drift near the edge of the depletion region; the other is due to electron-hole pair generation in the depletion region of the reverse-biased junction [22, 23]. As channel lengths are reduced,
overlapping source and drain depletion regions cause the depletion region under the inversion layer to increase. When a high drain voltage is applied to a short-channel device, it lowers the barrier for electrons between the source and the channel, resulting in a further decrease in the threshold voltage. The source then injects carriers into the channel surface causing an increase in \( I_{\text{OFF}} \). The proximity of the valence and conduction bands in the depletion region of the junctions causes a parasitic tunneling current. As the junction thickness decreases, the series resistance of the junction increases (figure 2.1). This cannot be neglected for conventional shallow junction technologies [18, 20, 24, 25].

![Diagram of series resistance](image)

Figure 2.1 Series resistance. Adapted from [26].

The gate leakage flows from the gate through the oxide insulation to the substrate. For lower oxide thicknesses leakage current is caused by the tunneling of electrons into the conduction band of the oxide layer under a high applied electric field across the oxide layer. Moreover, gate-tunneling current is due to the tunneling of electrons (or holes) from the bulk silicon and source/drain (S/D) overlap region through the gate oxide potential barrier into the gate (or vice-versa) [27]. The tunneling current increases exponentially with the decrease in the oxide thickness and the increase in the potential
drop across oxide. However, direct tunneling through the silicon oxide layer is the leading effect. As transistor length and supply voltage are scaled down, gate oxide thickness must also be reduced to maintain effective gate control over the channel region. Unfortunately, this results in an exponential increase in the gate leakage due to direct tunneling of electrons through the gate oxide. Off-state leakage of a device is the drain-source current of a transistor operating in the weak inversion, or sub-threshold region ($V_{GS} < V_T$). This diffusion of minority carriers through the channel causes current to flow from the drain to the source of a transistor. This is known as sub-threshold current. The sub-threshold current depends exponentially on both gate-to-source voltage and $V_T$. A reverse bias applied at the substrate increases $V_T$, thereby reducing the sub-threshold current (Body effect) [28, 29].

2.2.3 Gate Dielectric

The gate dielectric has been scaled to improve device performance and decrease short channel effects. For more than three decades, silicon dioxide has served as the gate dielectric and therefore is widely studied. Silicon dioxide has several important properties such as good mobility of holes and electrons at the silicon dioxide interface, low number of electronic states at the interface, and low trapping rates of holes and electrons. One of the most challenging limits for continued down scaling of silicon dioxide, as a gate dielectric is the increase in gate current density as the oxide thickness is reduced.

The best control of the channel by the gate is obtained when the gate insulator is made as thin as possible. The scaling of MOSFETs requires an increase in the dielectric capacitance and, hence, a decrease in gate dielectric thickness. The gate leakage current
through ultra-thin oxides may, however, be limiting to the scaling of CMOS technology at thicknesses ranging from at least 10 nm to, more recently, 2 nm. Below two nm, thicker gate insulators with a higher dielectric constant than silicon dioxide are being considered as a way to reduce the tunneling current through the gate insulator. The gate insulator continues to threaten an end to CMOS scaling unless a suitable dielectric with higher permittivity is developed as a suitable replacement for silicon dioxide. So changing silicon dioxide with a different material is a very challenging. The new material bulk and interface properties must be comparable to silicon dioxide. Recently, a number of high dielectric constant materials are under study, such as Ta$_2$O$_5$, ZrO$_2$, HfO$_2$, Y$_2$O$_3$, La$_2$O$_3$, Al$_2$O$_3$, and their silicates [18, 30-32].

2.2.4 Power Consumption

CMOS technology has an advantage over bipolar technology, which consumes a amount of power all the time. CMOS circuits do not dissipate power if they are not switching. However, it appears that scaling CMOS my soon ended because of static power. The most important aspect of low power design is to reduce the switching activity to the smallest level necessary to achieve the computation. Therefore, power consumption increases with clock frequency. During such an event, the load capacitance, $C_L$, is charged with the supply voltage, $V_{DD}$. If a high to low transition takes place, the energy stored in the $C_L$ is discharged, but no power is consumed since no power is taken out of the power supply. The most effective way to reduce the power consumption of the CMOS logic gates is to lower the supply voltage. The gate delays increases with supply voltage scaling unless the threshold voltage of the transistors is also
scaled down. The unlucky effect of decreasing the threshold voltage is a significant increase in the leakage current of the transistors. Therefore, there is a clear tradeoff between the off-state leakage and the active power for a given application, leading to a required careful selection of $V_T$ and $V_{DD}$. This phenomenon can be thought of as a lowering of $V_T$ as $V_{DS}$ increases. There are three major sources of power dissipation in digital CMOS circuits, which are

$$P = P_{\text{switch}} + P_{sc} + P_{\text{off}}$$  \hspace{1cm} (1)

The first term ($P_{\text{switch}}$) is the switching or dynamic component of power consumption. The second term is due to the direct-path short circuit current ($I_{sc}$). The last term is leakage current ($I_{\text{leakage}}$). Therefore, the most common and described factor in reducing the power consumption is the reduction of the supply voltage or by reducing the following parameters: $V_{DD}$, $C$, $I_{off}$, and $f$[33-35, 39].

### 2.2.5 Random Fluctuations

As transistors are scaled down towards 50nm, lithography processes cannot give out perfect and sharp designs. Moreover, fluctuation is a significant problem, and will affect the design of next generation devices. As devices shrink into the nano-scale, the major problem results due to atomistic fluctuations, such as random dopant distributions, line-edge roughness (LER), and oxide thickness, all of which will affects the performance and the operation of the devices (see Figure 2.2) [36,37].

Dopant fluctuations increase as devices shrink and this will introduce a significant parameter variation in the number and position of dopants. Moreover it will create trapping of a single electron in the channel area, which can change device current.
Line edge roughness (LER) in extremely scaled nanometer technologies may cause a shift in average threshold voltages, a degradation in sub-threshold slope, extension in channel length, and off-state leakage current [25,38].

**Figure 2.2 Random fluctuation.**

**2.2.6 Wiring and Interconnections**

One of the most difficult challenges in the nanoscaling device is the interconnection lines, which may decrease the device performance. As the transistor is reduced to nanometer scale, the wire interconnection also need to scale, so we achieve
improvements in size and speed, but when the wire is getting shorter and narrower lines resistivity increased due to electron mobility surface scattering leading to increased delay. Research is underway to move from silicon dioxide insulators between wiring levels to various low-dielectric-constant insulators, which can further decrease wiring capacitance. Additionally, the industry is currently moving from aluminum to lower-resistance copper metallurgy, which can decrease both wiring resistance and capacitance [40]. Figure 2.3 shows the expected cross section of a typical 65 nm generation CMOS device.

Figure 2.3 a) Expected cross section of a 65 nm generation CMOS device [41]. b) RC delay time versus intrinsic gate delay [42].
2.2.7 Design Complexity (CAD tools)

If we want to continue Moore’s (1st) law for classical bulk-Si and SOI CMOS, planners are well aware that they need to be looking at “Non classical CMOS” device structures and materials.

Industry and academia investigate novel non-classical CMOS devices, new materials and new transistor structures. Using predictive device modeling, which can provide alternative scaling scenarios and may delay the expected end of the Si scaling until nano-scale engineering can demonstrate a viable device. For example, new devices include ultra-thin body (UTB) silicon on insulator (SOI) FETs, source/drain (S/D) engineered FETs, and multi-gate FETs (see Figure 2.4)[43,44].

Figure 2.4 Some of the most promising multi-gate device designs [Intel].
2.2.8 Materials

To continue CMOS scaling in sub-50 nm range during the next decade, IC designers must strongly consider materials issues. One of the most promising alternatives for the replacement of bulk Si substrates in the CMOS industry is the use of SOI substrates and strained-Si/SiGe. There is a clear consensus that planar MOSFET architecture will be replaced with novel SOI devices incorporating performance-enhancing features such as strain engineering, multiple-gates, or heterostructure channels and contacts [9, 45, 58].

It is of interest to develop SiGe devices in SOI substrates to benefit from the advantages associated with an insulating substrate, such as reduced parasitic capacitances, improved isolation, and reduced short-channel-effects. Strained Si/SiGe has the additional advantages of enhancing the effective mobility for both electron and hole.

2.2.8.1 Strained Si/SiGe

Strained Si/SiGe technology is currently available and promising for candidates for the next generation of devices. As opposed to III-IV compound materials, Si does not have other cubic semiconductor materials with a matching lattice. Germanium is the only elemental semiconductor with the closest lattice constant to that of Si. In other words, SiGe/Si is the only crystalline-crystalline interface on Si that can potentially be as high quality as those in III-V semiconductors. The lattice mismatch is about 4.2 % between Ge and Si, the lattice constant of Ge being slightly larger. It is well known that the hole effective mobility in Si is very low (about a third) when compared to the electron mobility. This is due to the effective mass of holes being greater than that of electrons.
However, at room temperature the mobility of holes in bulk germanium (1900 cm$^2$/Vs) is greater than electrons in bulk silicon (1500 cm$^2$/Vs). Therefore, to enhance hole mobility in a p-channel, a germanium-rich layer is grown between layers of silicon. Due to lattice mismatch, this also results in significant levels (Typical stress values are 1.5 GPa ± 20 MPa) of strain in the SiGe layer. The strain-induced modification of the band structure for alloyed SiGe causes a splitting of the heavy hole and light hole bands, and enhances hole mobility by lowering the effective mass at the top of the valence band in comparison to unstrained bulk silicon.

For strained Si nMOSFETS, device performance is increased by growing a thin silicon layer on top of a relaxed SiGe virtual substrate. The basic band structure of a strained Si/\(Si_{1-x}Ge_x\) structure is shown in figure 2.5. The band-gap of \(Si_{1-x}Ge_x\) layer is smaller than the band-gap of silicon under tensile strain. Therefore, by growing thin strained-Si on thick relaxed SiGe virtual-substrate the mobility of nMOSFETS may be also enhanced. It is important to emphasize that, the discontinuities of the band gaps edges in this heterojunction system is equally affected by the strain-induced splitting in the Si bands as well as band-gap reduction associated with Ge alloying. The band offsets increases with the Ge% and is known to be a Type II alignment for Strained Si on SiGe.

Strained layers must have limited thickness otherwise, they can develops defects and become relaxed. This is achieved by keeping strained layer below a thickens known as critical thickness limit [46-49]. Throw out this work, all strained layer with this requirement, and should be fully strained.
There are important changes to both the valence band and the conduction band due to biaxial tensile strain. In bulk Si, the conduction band consists of six degenerate valleys in the [100] directions as shown in figure 2.6 shows the energy band structure of a 2DEG in a Si channel under tensile strain. The strain lowers the energy of the two valleys with their long axis perpendicular to the 2D plane relative to the other four valleys. The amount of lowering depends on the strain. With lowering the energy, only the two-fold degenerate valleys are occupied at room temperature. Therefore, the longitudinal effective mass determines the quantization energy in a strained Si quantum well, whereas the transverse effective mass determines the electron motion along the 2D plane, such as in the channel of a MOSFET [46].

For strained SiGe p-MOSFETS channels the biaxial tensile splits the light hole and heavy hole degeneracy as shown in figure 2.6 and these affect the mass in the valance band because the effective mass of the light hole is lower than the effective mass of the heave hole.
Figure 2.6 Conduction-band structure of a) normal silicon valleys and b) strain-Si. Under biaxial tensile strain, the six-fold degeneracy is broken, and the two out-of-plane valleys ($\Delta_2$) become preferentially occupied with respect to the four in-plane valleys ($\Delta_4$) [38].

However, as we see from figure 2.5 higher germanium content (x) means a greater valence band offset and increased hole mobility due to the increase of the carriers. In addition, the channel thickness is reduced. So, interface scattering becomes more significant in limiting the mobility. Hence, there will be an optimum Ge fraction, which may be different for devices where high current or high mobility is the dominant requirement.

As we stated previously, the enhancement of mobility in strained silicon is due to the reduction of the carrier conductivity, effective mass and the inter valley scattering rates. In strained Si grown on relaxed silicon germanium, the silicon 6-fold degenerate valley is split into 2-fold and 4-fold degenerate valleys and the $\Delta_2$ minimum is lower in energy with respect to the $\Delta_4$ minima and is preferentially occupied. The compressively strained SiGe channel can provide much higher hole mobility enhancement than the strained-Si channel, making it possible for holes to have equal or higher mobility enhancement than electrons, as we shown in figure 2.7 [50,63].
Figure 2.7 Effective hole mobility versus effective field measured from p-MOSFETs. Adapted from [63, 50].

2.2.8.2 Silicon on Insulator (SOI)

Silicon on insulator (SOI) is a semiconductor fabrication technique developed by IBM that enables a transistor to be faster by eliminating the charging and discharging of a capacitance. Silicon on insulator is a semiconductor technology typically obtained by one of the following two techniques: 1) Separation of silicon by implanted oxygen (SIMOX), or 2) Bonded wafer and etch back (BESOI) techniques. The SOI process creates a thin insulating layer between a thin layer of silicon and the silicon substrate. This process helps reduce the amount of electrical charge that the transistor has to move during a switching operation, and eliminating the short-channel effect. Conversely, bulk CMOS relies on junction isolation between devices (see figure 2.8) [51, 52].
SOI offers many advantages over bulk CMOS. First, SOI improves device speed performance and Lower Power Consumption by 20% to 35% over that exhibited by bulk CMOS technology due to lower parasitic capacitance. Second, the SOI process creates an oxide layer over the silicon substrate and around all devices wells, eliminating the parasitic paths that can lead to latch-up. Third, SOI is better than bulk for low power and low voltage applications because of a reduction in the amount of electrical charge that the transistor has to move during a switching operation due to the insulator layer. SOI has a lower parasitic junction capacitance and higher transistor on-off characteristics, thus
making it faster and allowing it to switch using less energy. SOI chips cost more to produce and are generally used for high-end applications [54].

2.3 Device Simulation Outline

Technology computer-aided design (TCAD) is the numeric simulation of semiconductor processes and devices. TCAD dramatically reduces development time for new semiconductor technologies. TCAD is typically used to simulate a single device, but an extended region that includes several devices can also be simulated. Fabrication, reliability, and performance issues are determined early in the design process before the first model is fabricated. According to the ITRS Roadmap, the guideline for semiconductor technologies, TCAD saves up to 30 percent of the cost for developing new technologies.

2.3.1 1D Simulation

In 1D simulation, we used a Poisson/ Schrödinger program presented by Professor Snider [55], which uses the method of finite differences to find the 1D band diagram of a semiconductor structure. It can automatically calculate the band diagrams for multiple bias voltages and can determine C-V characteristics. The program calculates the conduction and valence bands and the hole and electron concentrations. Dopant ionization is included for both shallow and deep level dopants. Current flow is not calculated, so the structure can be simulated only in thermal equilibrium. In the current version of the program, three possible boundary conditions can be defined for the surface and substrate: Schottky barrier, ohmic contact, and energy band slope = 0. Unfortunately,
the program has limited text editing and graphing capabilities, so we wrote a MATLAB code that used the output from the simulation process as the input to the MATLAB program. In addition, we used a graphing program (KaleidaGraph) for plotting the results. The input to the 1D Poisson program is a text file, which contains the information necessary to simulate the structure. This file is created using a text-editing program. An example file is shown in Appendix B.

2.3.2 (2D/3D) Simulation

In 2D and 3D simulation, we used Integrated Systems Engineering package (ISE). It is one of the world's leading providers of TCAD modeling and simulation software. Semiconductor manufacturers around the world such as Motorola, Intel, and Texas Instrument use TCAD to support the design and manufacturing of integrated circuits. Since its establishment in 1993, ISE offers software solutions to some of the largest semiconductor fabrication facilities. These tools are mainly suitable for emerging technologies and complex applications including sub-100 nm CMOS and SOI, SiGe technologies, heterostructure electronics, optoelectronics, quantum devices, and nanoelectronics. ISE TCAD package is very large and multipurpose, so we use only the following modules: GENESIS, MDRAW, DESSIS, INSPECT, TECPLOT. GENESIS is ISE’s general simulation platform and primary graphical front end that integrates ISE simulation programs into one environment (figure 2.9).
2.3.2.1 MDRAW and Designing COSMOS Devices

The geometry of the device including materials is usually created by MDRAW. However, in our case we built COSMOS devices by using geometric axis (x, y, z) (see appendix A). The two main modes are boundary and doping. The boundary mode allows us to draw a particular device and to indicate its general dimensions and contacts. The doping mode allows us to set the doping concentrations as well as the grid spacing on the device. The automatic generation feature creates meshes with an axis-aligned structure that is fitted to the boundary. The mesh generator is fully unstructured and pays special attention to mesh elements near material interfaces. The doping concentration of each region is also a factor in the creation of the mesh. Anisotropic (stretched) elements of the mesh are incorporated because regions of high doping yield steep gradients. A finer mesh in these regions improve the speed of the simulation, while maintaining the required accuracy see figure 2.10 An example file is shown in Appendix B [56,57].
2.3.2.2 DESSIS

DESSIS is the most important device simulator program for 1D, 2D, and 3D geometries. It simulates and solves the electrical, thermal, and optical characteristics of semiconductor devices numerically by using finite difference method. In addition it have a set of physical models that can be useful to all significant semiconductor devices and operation conditions [56,57]. For simulation, we need first to generate a parameter file. This file has instruction parameters that are used in DESSIS. If we want to change mobility, or a dielectric constant, we change it in this file.
2.3.2.3 INSPECT and TECPLOT

For device simulation using ISE, tecplot is a recommended tool for visualizing a wide range of technical data. It offers a variety of 2D and 3D plots and is excellent for viewing 3-D images of physical quantities throughout the device. In addition, it is used to plot one physical quantity versus another, such as the traditional current vs voltage plot. It can be run either in graphical mode or in batch mode that is suitable when writing for processing a set of simulation data [56].
Chapter Three

COSMOS Device Architecture

3.1 Introduction

This chapter aims at introducing the principle of operation, basic properties and use of the novel CMOS architecture named COSMOS, which is the focus of this PhD work. Detailed design and optimization of COSMOS devices and circuits will be dealt with in the following chapters.

The Si nanoelectronic engineering have recently reached a level of capability, which make 3D processing on silicon-on-insulator (SOI) substrates not only possible [15,16], but also a necessity in order to surmount practical limitations of conventional planar CMOS [2,10]. Thus, device modelers are presented with a multitude of options in exploring new designs, as evident in the proliferation of alternative architectures, including multi-gate MOSFETs, Schottky MOSFET, and Tunneling MOSFET. While these structures have unique features superior to conventional MOSFETs, nonetheless, they merely aim to replace the bulk devices in traditional CMOS circuitry. In other words, they do not offer significant paradigm shifts in design and layout, thus still retaining the redundancy inherent to CMOS operation namely building two devices even though only one operates at a given stable output.

We demonstrate in this chapter, using 1D/2D/3D device simulations, a novel CMOS device architecture capable of building complementary logic operation using only a single gate stack [2-6]. The new architecture, named complementary orthogonal stacked MOS (COSMOS), places the n and p-MOSFETs perpendicular to one another under a single gate, integrating them vertically as well as laterally (see Figure 3.1). Thus,
COSMOS can eliminate the aforementioned redundancy in CMOS and may result in dramatic savings (up to 50%) not only in active device area of a conventional digital CMOS layout, but also in R-C device parasitic associated with building and wiring two sets of devices for a single Boolean output function. We argue that the COSMOS structure is a natural candidate for very dense, low-power circuitry required in sub-50 nm scale. We demonstrate how the device may be built and operated as well as verifying logic NOT operation via 3D device simulations.

Figure 3.1 Current paths for n or p MOSFET in conventional CMOS and the proposed COSMOS architecture.

3.2 COSMOS Architecture

The classical static-CMOS architecture, relies on the presence and co-operation of two separate MOSFETS (n-MOS and p-MOS), which are driven by the same input signal to their gates. While efficient from DC operation viewpoint, this has two major drawbacks: the R-C parasitic introduced by wiring two sub-networks and the need for
two separate gates and active areas even though only one sub-network is required for a stable output as outlined in Figure 3.1. In the proposed COSMOS architecture, these two drawbacks are eliminated by integrated the two channels under the same gate vertically with one of the device axis rotated by 90° to allow access to two independent sets of source and drain contacts. Thus, there is only one active field and a single gate stack in Figure 3.2, thereby dramatically reducing both the total device area and wiring parasitic.

An important aspect of COSMOS is the creation and spatial isolation of two channels by the use of strained Si/SiGe heterostructure technology, which allow electrons and holes to be confined to separate layers, as depicted in Figure 3.2a. Electrons are kept in either relaxed or strained Si cap layers, while holes are confined to strained Si$_{1-x}$Ge$_x$ channel with a high Ge content ($x \geq 0.3$), hence high hole mobility. Both channels must be undoped and extremely thin (2 to 8 nm) to facilitate threshold control and minimize parasitic conduction. Furthermore, the gate stack must be engineered to concurrently tune the two thresholds by the choice of a single barrier height (work function $\Phi_m$) and oxide thickness. This aspect is especially exciting since a move to metal-gate and high-k insulator in CMOS has been delayed mainly by the complexity in the integration of two separate gate metals in a single process. In other words, there is only one (metal) gate and one gate dielectric in COSMOS that require structural and electrical optimization compared two in conventional CMOS.
Figure 3.2 (a) Generic layer structure (b) top and cross-sectional view of the device geometry.

The COSMOS devices are based on strained silicon-on-insulator (SSOI) substrate technology, which has recently become available due to advances in strain layer growth and wafer bonding techniques [50,59-61]. There are already several examples of strained Si/SiGe heterostructures on SOI wafers with extremely thin, dual channels having symmetric electron and hole mobility’s [49,62,63,70]. These reports and general evolution of SOI technology imply that COSMOS layer structure can be built using existing material and technological toolsets. The only non-standard feature is the inclusion of two etch-steps to prevent the parasitic $p$-$i$-$n$ diode conduction by the partial removal of complementary channels near the drain end of each device (e.g., partial removal of Si cap in the pMOS device), as shown in Figure 3.2b.

### 3.3 COSMOS Operation

To explain COSMOS operation, we first focus on gate control in the vertical structure of two stacked channels using 1D Poisson-Schrödinger solution. Figure 3.3 show the electron and hole profiles (top plots) at two extreme cases of the gate voltage
(±1V) in an example COSMOS structure with 3 nm Si electron channel and 4 nm strained SiGe hole channel capped with a 1 nm SiO₂ insulator layer and a mid-gap metal gate. Clearly, a single gate is able to control both electron and hole concentrations. Moreover, the two distributions are comparable in terms of amplitude and are largely localized to their respective channels, eliminating parallel conduction possibility. Threshold voltage of the two populations extracted from similar Poisson-Schrödinger solutions show that the two distributions are separated by ~0.6V. Therefore both channels can be safely turned off at zero bias. Another important aspect is the symmetry between the two density curves in Figure 3.3 (lower plots), meaning that gate has equal strength to control electron and hole populations. Although the simulated characteristics in this example COSMOS device are not perfectly symmetric, such an operation with a low (0.1-0.5V) threshold voltage is easily accessible to COSMOS structures (see Figure 3.4). In any case, an accurate threshold calculation requires 3D simulations corrections and equal mobilities. Figure 3.3 omits 3D effects and current flow.

To illustrate how a single gate may be used to control two MOSFETs, we show in Figure 3.4 the full I-V characteristics of COSMOS transistors obtained from 3D drift-diffusion simulations. To save time in demanding 3D simulations, no quantum mechanical corrections was used. I-V characteristics of the two MOSFETs are almost comparable, with the small difference in ON state current resulting from the fact that the strained SiGe mobility parameters are not accurate in the present model of the TCAD simulator. The non-uniform sub-threshold slope is as a result of p-i-n leakage contribution to actual transistor current. It is clear that by tailoring the SiGe hole mobility
and choosing an appropriate vertical design a symmetrically operation COSMOS gate is possible.

3.4 COSMOS Logic Circuits

To demonstrate the usefulness of COSMOS device architecture we examine the feasibility of logic operations via a simple logic inverter (NOT gate) in this section. A COSMOS inverter can be realized by appropriate connections to the low (VSS) and high (VDD) rail voltages, and by simply shorting the two drains of COSMOS transistors, as shown in Figure 3.5a. Therefore a simple metallization should be sufficient for a NOT
gate, which illustrates the immense potential of the proposed architecture for lowering R·C parasitic, especially in the context of digital static CMOS applications. In the following transient drift-diffusion simulations, the quantum mechanical corrections are omitted to speed up the 3D solutions, the load capacitor is assumed to be 1fF, and a 36nm COSMOS device is used. As evident from Figure 3.5b, the logic inverter is fully functional at ±0.5V supply voltage with acceptable delay (~100 ps) figures. Note that with correct mobility values for Si/SiGe layers, and with further structural optimization, this delay could be further reduced in a truly symmetrically operating COSMOS device.

In these 3D drift-diffusion simulations we neglected quantization effects to save time, which imply that actual thresholds or current levels may be slightly different. We also observe a small amount of static leakage as a result of higher sub-threshold slope of pMOSFET augmented by leakage from p-i-n parasitic device. While this tested structure is not fully optimized, our results are sufficient to verify the potential of COSMOS in logic circuits.

Figure 3.5: a) Inverter operations verified in 3D isolate COSMOS layers and establish proper contacts, b) output response of a 40 nm COSMOS inverter to high and low logic inputs of ±0.5V, illustrating logic functionality using a single gate.
More complicated logic gates are also possible in COSMOS architectures, as will be discussed in Chapter 5. An example implementation for a NOR gate is given in Figure 3.6. Basically this structure is a simple combination of the two previous inverter gates in which n-MOSFETs construct the parallel, and p-MOSFETs the serial sub networks. Note, however, that there is no extra layers in the NOR implementation and a short metallization is sufficient to construct also multiple inputs circuits like the NOR gate.

Figure 3.6 An example layout for a two-input NOR geometry using only two COSMOS gates. Peel-off diagrams, in the center and on the right, allow to see the Si/SiGe layer structure under the input gates.
Chapter Four

COSMOS Design

4.1 Design Methodology

Having shown that COSMOS idea is workable, in this chapter, we will show how we can design a COSMOS gate for a given performance figure such as the threshold voltage or symmetry. To this end, we employ hierarchical 1D/2D/3D device simulations in our design methodology. This is needed because full-3D simulations are often long and redundant for setting vertical layer parameters only. On the other hand, for switching characteristics and logic design 3D simulation in classical limit is necessary. In 1D analysis, we typically tune the threshold voltage for both devices; using self-consistent Poisson-Schrödinger solutions. We analyze the leakage characteristics, I-V response and switching performance by 2D and 3D simulations, using DESSIS. Figure 4.1 outlines the methodology, important parameters, basic tools used in the following design study.

![DESIGN METHODOLOGY Diagram](image)

Figure 4.1 Outline of methodology and tools used in designing COSMOS devices.
4.2 1D Design

As Si CMOS scaling limit approaches fast to 10nm hallmark, device engineers are confronted with a multitude of options in exploring new designs. This is aided by the new heights in 3D device processing and strain engineering on silicon-on-insulator (SOI) substrates, surmounting practical limitations of conventional planar CMOS [58,64]. While welcoming these developments, device engineers are forced to use a wide range of tools and methods to adequately understand and optimize these novel architectures. COSMOS architecture presented in the previous chapter is no different in this regard and needs further tuning in order to be useful for circuit designers. The beginning point of all design efforts in modern devices is 1D design of vertical layer structure, just like the fabrication starts with substrate production. All other properties of the subsequent devices are closely related to the nature of the substrate and active layers. Therefore, the analysis below incorporates 1D simulations steps that can be used in the choice of appropriate layers for COSMOS operation, especially in terms of threshold and symmetry. We first look into the design of strained channels, followed by the gate stack (insulator and gate conductor), which reflect their order in the fabrication.

4.2.1 Channel Ge Content and Thickness.

In COSMOS, there are several design parameters for tuning the vertical layer structure, including strained layer composition (Ge %) and channel thickness, which can be used to optimize a symmetric pair of device thresholds. As mentioned in Section 2.2.8, built-in strain of SiGe layers leads to significant changes in the electronic and transport properties of the alloy channel, which gets larger at higher Ge levels. Accordingly, the
use of large Ge concentration is recommended in the buried strained SiGe channel as this would improve hole mobility considerably, even above that of electrons in unstrained Si inversion channel. For $x \geq 0.3$, hole mobility in strained Si$_{1-x}$Ge$_x$ layers should be comparable to or larger than electron mobility in undoped Si inversion layer [62]. By aligning $p$-MOSFET along the [011] direction [50,60], hole mobility may be further improved, thus restoring $p$-MOSFET transconductance deficit due to larger separation from the gate. In COSMOS, there are several independent parameters of layer structure, including layer composition, thickness and their order, which can be used to optimize a symmetric device threshold.

In Figure 4.2, we demonstrate how these parameters can be tailored to prevent parallel conduction and to set $V_T$ accurately. We find that an additional benefit of large Ge% is the increased separation between the main and parasitic hole channels, as can be seen in Figure 4.2a. Str. SiGe layer thickness mainly influences the pMOS threshold and the parasitic channel buffer is ~0.2V for 70% Ge and 0.45V for 35% Ge. The total channel thickness also affects the overall design, leading to less separation in smaller channels. As a result, both thickness and Ge% cannot be chosen arbitrarily at a given threshold, while there are multiple optimum choices such as low Ge% ($x = 0.35$) and a thick (5-6 nm); or high Ge% ($x = 0.7$) and an ultra-thin (1-2 nm) channel. Obviously, the former is more favorable from manufacturing point of view. Therefore, Figure 4.2 is helpful for the design of channel properties and shows that sufficient latitude for design of symmetric COSMOS operation exists.
4.2.2 Work Function and the Insulator (SiO$_2$) Thickness

After the layer design, the gate engineering comes as the most important device feature. Even the best designed substrates can result in worst device performance if the gate stack is not properly chosen. Essentially, the gate engineering determines the nature of electrostatic balance between the external charges (applied via gate bias) and the conducting channel in the MOSFET. To elucidate this point further, we plot in Figure 4.3 the dependence of the threshold in COSMOS layers on varying levels of gate barrier height, and oxide thickness. Gate barrier height is decided by the work-function of the metal used in the gate, which corresponds to the Si gap values shown in Figure 4.3a. Its impact is straightforward and provides the easiest way to tune threshold asymmetry. On the contrary, the insulator (SiO$_2$) thickness impacts only the p-MOSFET parasitic channel. In all cases, the threshold is not oversensitive to any of the parameters, which can be varied within the practical bounds of current technology.
Figure 4.3 Dependence of simulated threshold voltage on: a) work function of gate material and b) the insulator (SiO$_2$) thickness in the same COSMOS layer structure.

In device fabrication, Figure 4.2 and 4.3 corresponds to substrate growth (Ge content and channel thickness) and gate-stack engineering steps, respectively, and are not mutually exclusive. Therefore, independent optimization of the mobility and density in individual channels is possible [63], providing ample room for designing COSMOS devices capable of symmetric operation. It is also important to note that overlap of carrier distributions in the two channels is not problematic along the main (nMOS or pMOS) device axes since only one channel exists at a given time. This would be a problem only for conduction via the parasitic p-i-n diode, which is inhibited by the under-etch and over-etch regions of the channels, as explained above. Since the reduction of channel thickness below 5 nm significantly lowers mobility due to excessive interface scattering, vertical spread of carriers along the major transport axes is beneficial in this case for both types of devices.
4.3 2D Design

Next level in the design hierarchy is the use of 2D simulations for I-V response of transistors built on the layers designed in the previous section. In 1D analysis, neither drain and source regions nor current flow are accounted for. Also infamous short channel affects are not included. Thus, 2D simulations below are the first step toward observing actual device characteristics and obtaining accurate predictions for device threshold and current. They offer a good compromise for a quick evaluation of device performance without full-3D simulations. 2D analysis is also more suitable for the inclusion of quantum mechanical corrections.

Figure 4.4 shows simulated I-V response obtained from 2D slices of n and p-MOSFETs in a 100 nm COSMOS gate. Quantum corrections are included in these simulations using density gradient approach of DESSIS [65]. As in the case of 1-D Poisson–Schrödinger results, the threshold obtained from the 2-D simulations is also asymmetric because of lack of optimization in this particular layer configuration. The characteristics of the two MOSFETs are comparable with the small difference in the ON state current resulting from the fact that the strained SiGe mobility parameters are not accurate in the current model of the technology computer aided design (TCAD) simulator. Although the general features of 2D I-V plots are correct, there are two deficiencies in device behavior: a) the parasitic p-i-n leakage device is missing and b) 3D geometry effects (90° corners etc.) are absent. We shall investigate the former in the following section, since this makes a great impact on COSMOS performance studied in Chapter 5.
Figure 4.4 Simulated 2-D transfer ($I_d-V_g$) and output ($I_d-V_d$) characteristics of 100 nm COSMOS devices. Each MOSFET simulated separately using standard Si mobility values ($\mu_n = 2.5\mu_p$).

4.4 p-i-n Parasitic Leakage in COSMOS

Semiconductor p-n junctions, i.e. diodes, can pass significant amounts of current when p-side is positively biased, while a very small but finite thermal current (also known as saturation current) flows under reverse bias. A p-i-n diode is formed when these two regions are separated by an intrinsic (undoped) region, which increases the series resistance of the diode and the voltage drop across it under a given current level. This is because the intrinsic region is very easily depleted in the absence of space charge and does not completely halt the current flow. Thus p-i-n diodes may be regarded as poor diodes that take larger voltage to turn on.

An intrinsic feature of the COSMOS architecture is the close packing of several p and n regions separated with undoped channels, with at least one positively-biased ($V_{DD}$)
p-region and one negatively-biased ($V_{SS}$) n-region. Thus, there is sufficient condition in COSMOS operation for the formation of parasitic p-i-n diodes normally not intended. This parasitic diode action is likely to be the most important factor limiting the performance of COSMOS (see Chapter 5). For instance, the gradual turn-on of the parasitic diodes were the cause of non-flat sub-threshold slope in 3D I-V characteristics of COSMOS device pair (Figure 3.4) and the static leakage currents during logic switching of NOT gate (Figure 3.5b). In the following, we explain how the leakage from the parasitic diodes occurs in more detail using 2D simulations.

To analyze the onset of static leakage in the 3D structure we simulate in Figure 4.4a a representative 2D slice of the path the electric current follows from positive to negative supply voltage of the parasitic p-i-n diode. Although this abstraction neglects the 90-turn in the current path (see Figure 4.5b), it allows room for better visualization and 2D simulations. We find in Figure 4.5a that the leakage through the p-i-n channel is very sensitive to the sign of the gate voltage, having two distinct states separated by three orders of magnitude. At 0V gate bias, it is possible to observe a transition from low to high level of leakage between 0.2 to 0.4V of diode bias.
Figure 4.5 2-D simulation of leakage via the parasitic p-i-n diode present in the COSMOS inverter as a function of gate bias. The leakage increases by three orders of magnitude when gate induces an electron inversion layer in the SiGe material, below the region where Si cap is removed.

In Figure 4.5a, as the gate bias gets more positive, the higher-leakage state dominates. Therefore we can claim that the higher-leakage state is associated with the formation of an electron inversion layer within the SiGe channel just below the etched section of Si cap layer. In other words, the application of large gate voltage forms an electron inversion channel in the SiGe layer, under the region where Si cap is removed, thus completing the leakage path for electrons. Therefore it should be possible to lower total static leakage by exploring asymmetric device geometries and the choice of dielectric material used to fill the etched regions. However, the presence of this leakage path ultimately limits the use of COSMOS, especially in low-power applications, where it is expected to be most useful. To further support this claim and show the damaging impact of leakage on COSMOS performance, we show in Figure 4.6 COSMOS inverter’s transient response at different supply (drive) voltages. Each sub-plot in this figure is similar to Figure 3.5b, except obtained at higher voltages. Clearly high drive voltages
above 1.0V causes a significant static leakage current (not to be confused with large current peak associated with capacitive discharge events). In agreement with Figure 4.5a, static leakage is only found for positive gate input conditions and absent for the low input state of the inverter (Vg<0). In summary, 2D simulation analysis above is helpful in identifying the origin of static leakage and its magnitude without extensive 3D simulations.

It is possible to reduce the static leakage by i) raising the V_T above 0.3V in the present circuits, for instance by relaxing oxide thickness slightly, which can be tolerated in such ultra-thin channels, ii) adding an extra stop etch beneath the top Si electron channel as opposed to a single etch used in the original COSMOS design [1], and iii) optimizing the device layout by way of shifting the center of the COSMOS cross [6]. These options will be tested in Chapter 5.

Figure 4.6. The transient response of a 40 nm COSMOS inverter gate obtained from 3D drift-diffusion simulations at different drive voltage (logic) levels. The logic NOT function is successfully implemented in this particular layer structure (tSi = 2 nm and tSiGe=3 nm, 30% Ge, mid-metal gate, and 1 nm SiO2).
Chapter Five

3D COSMOS Optimization and Scaling

5.1 3D Design

The previous chapter has already established a methodology for the design and optimization of COSMOS architecture. In the present chapter, we shall complete this methodology using full-3D simulation of COSMOS inverter and look into its scaling properties as a function of voltage, gate geometry and channel thickness. In addition, we also present a power-delay analysis of basic static logic gates with multiple inputs. The chapter ends with an evaluation of geometrical errors in fabrication and other layout considerations for efficient COSMOS implementation. Collectively, simulations in this chapter should allow designers to appreciate COSMOS architecture’s advantages and weaknesses in different technological settings.

5.2 COSMOS Scaling

One of the most important advantages of CMOS technology is its ability to be optimized for different technological constrains such as drive voltage standards, chip area limitations, power levels etc. This is evident from 30 years of Moore’s scaling laws, which prove the immense capability of CMOS technology for wide range of integrated technologies. In this section we will investigate using 3D TCAD simulations how COSMOS devices can cope with scaling of electrical and physical design variables, including supply voltage (power) and gate length (technology node) that plays a very central role in device and circuit performance.
5.2.1 Voltage Scaling

ITRS envisages rail voltages less than 1.0 V for sub-50 nm era, progressively getting as low as 0.5V [11]. It is extremely important to understand how COSMOS can operate under different supply standards especially below 1.0V. Here, we must take note of the total rail voltage drop between the V\textsubscript{DD} and V\textsubscript{SS} supplies (i.e. V\textsubscript{DD}+|V\textsubscript{SS}|) not the individual supplies. Because total current flow during a logic transition is powered by both of these supplies.

In Figure 4.6 we have already showed COSMOS logic inverters’ response to use of different rail voltages. It appears that for rail voltages larger than ±0.5V, the static leakage and noise margin performance quickly deteriorates, while the gate delay does not improve substantially. Using this data and similar ones repeated for 18nm COSMOS gates, we can compile the voltage scaling performance of COSMOS architecture, as shown in Figure 5.1. Gate delay is calculated from average of two durations (L→H or H→L transitions) defined between the |slope| = 1 of the transient output and the static leakage is simply the total supply current at the stable inputs. The noise margin is the total voltage drop at the output with respect to input, i.e. NM = |V\textsubscript{drive}-V\textsubscript{out}| p-p. As a rule of thumb, we observe that an increase in drive voltage leads to faster operation at the expense of higher static leakage and loss of noise margins. Also according to this plot, 1.0V drive voltage is a good compromise between speed and static leakage (power) for both 18 nm and 36 nm COSMOS gates.

It is evident that typical rail voltages for a given COSMOS device geometry will have an upper limit that appears to be (±0.5 V) for devices considered in this work. Therefore COSMOS is most suitable for low-power applications that place greater
importance in active area saving than speed. Another important aspect of Figure 5.1 is the fact that 18 nm COSMOS gate performs worse than longer (36 nm) counterpart in terms of switching delay, even though excess leakage is reduced. We also see that at sufficiently high rail voltages (±1.0 V) 18 nm COSMOS gives way to additional leakage current associated with drain-induced barrier lowering (DIBL) effect.

![Figure 5.1 Dependence of COSMOS inverter performance on drive voltages.](image)

**5.2.2 Vertical Scaling**

In Chapter 4 we have already gave a full account of 1D design approach for the optimization of vertical layer structure for both device channels and gate stack. We therefore have a general knowledge of how the symmetric threshold control in COSMOS
can be obtained for a given set of design parameters. In this section, therefore, we will limit our discussion to the impact of channel thickness (i.e. \( V_T \) changes) on COSMOS switching performance such as gate delay and static leakage.

Useful range of channel thickness in COSMOS for threshold control is between 1 and 10nm. A more practical range would be 3 to 6 nm, since a) <3 nm is very hard to fabricate in a uniform manner and leads to mobility reduction due to two close interfaces [66] and b) above 6 nm parallel conduction and excess p-i-n leakage are concerns. The impact of total channel thickness (Si cap + strained SiGe channel) on COSMOS inverter performance is plotted in Figure 5.2 below. It is obvious from our results that a very thin channel is beneficial for both gate delay and static leakage through COSMOS. Obviously this is good news, since threshold control in Section 4.1 favored thin channels since it is easier to obtained symmetric operation. Moreover, this is also good for gate channel reduction trends, since the harmful short-channel effects in MOSFETs are always minimized in thin body SOI devices [67]. As a result, 3D simulations show that vertical scaling is recommended for COSMOS and minimum channel thickness should be preferred at all times.
Figure 5.2 Inverter delay and state leakage as a function of total (n+p) channel thickness.

5.2.3 Lateral Scaling

So far in our simulation analyses, only a single COSMOS gate length (40 nm) is considered, with no information on the scaling capability of this novel structure. We evaluate the scaling potential of COSMOS architecture and develop guidelines in this section by comparing I-V characteristics of COSMOS gates same in all aspects except the gate dimensions in x-y plane.

Figure 5.3a plots the transfer characteristics ($I_d$-$V_g$) of COSMOS transistor pair at various gate dimensions. The extracted thresholds are given in Figure 5.3b. We find a reversed gate scaling trend in COSMOS devices, with smaller gates having larger thresholds and lower ON currents. This seemingly counter-intuitive scaling behavior results from 2 nm-wide gate-to-source and gate-to-drain overlap areas which do not scale in these simulations. Since 2 nm is a lower limit for the source or drain overlap region, it is not reduced in successive gate lengths considered in the analysis. Hence, the reduction
of gate length causes this 2 nm section to become comparable to channel resistance, thus reducing current drive. It is important to clarify that the cross-shape of the gate layout, i.e. \((W/L)_{\text{nMOS}} = (L/W)_{\text{pMOS}}\), where \(L\) and \(W\) refers to gate length and width of each transistor, does not affect this scaling behavior, because gate area is still a square and scaled in both directions. Therefore, the scaling of the compact nature of COSMOS layout is primarily limited by parasitic series resistances of source and drain regions.

The lowering of ON current with gate scaling means that the devices with smaller gate dimensions get progressively slower in COSMOS, as found in Figure 5.4. However, the channel length has a weak positive impact on the static leakage, especially for COSMOS gates driven below \(\pm 0.5\)V. Thus there is an optimum gate dimension that trades-off active device area with speed and static leakage for a given layer structure, as will be investigated in detail in the next section.

![Figure 5.3 Dependence of a) transfer characteristics (total \(t_{\text{ch}} = 5\) nm) and b) threshold voltage of COSMOS gates (total \(t_{\text{ch}} = 5\) nm), on effective channel length. The peculiar scaling trend is due to reciprocal coupling of gate dimensions in COSMOS.](image)
5.3 Multiple-input COSMOS Logic Circuits

As the scaling becomes more difficult and expensive in sub-50 nm technology, both SIA roadmap [58] and Semiconductor Research Corporation (SRC) [68] expect circuit optimization to become progressively important for silicon industry. In this uncharted territory, where the compact SPICE models either lacks rigor or are totally absent, mixed-mode TCAD simulations are the only means for design and circuit development. Consequently, we use mixed-mode TCAD technique here for COSMOS circuit performance and optimization as a natural extension of our work.

In logic gates with multiple inputs and large loads, deterioration of noise margin and the number of maximum allowable inputs/outputs may become a serious limitation. At this stage the driving ability of the multiple-input COSMOS gates is unknown and requires attention. So in this part of the study, we analyze multiple-input logic circuits as

Figure 5.4 Dependence of delay and static leakage (total $t_{ch} = 5$ nm) on effective channel length.
a function of COSMOS device parameters. In addition, it is useful to compare the performance of the various COSMOS devices optimized earlier in realistic logic gates.

5.3.1 Two-input NOR Gate

To demonstrate the usefulness of COSMOS for general digital design problems, we analyze below the temporal response of a two-input COSMOS NOR gate, built using two COSMOS gates as shown in Figure 5.5. Note that the two inputs are applied to the gates, shown as semi-transparent contacts. The transient response of the NOR gate, plotted in Figure 5.6, confirms that output remains low except the ‘00’ input to the gates for a rail-to-rail \((V_{DD} + |V_{SS}|)\) voltage of 0.6V. Further simulations at higher voltages (Figures 5.7) indicate that, while the NOR gate is operational, its leakage performance and noise margin deteriorate rapidly above \(V_{DD} + |V_{SS}| = 0.8V\). At the same time, however, the delay improves rapidly, indicating the importance of optimizing power delay product in COSMOS circuits. As in the case of a NOT gate, the up and down transitions are not equal in duration due to unequal mobility used in the simulator.

![Figure 5.5 The 3D view of a two-input NOR circuit using only two COSMOS gates. All contacts are labeled and gates are shown in semitransparent fashion to aid the reader.](image-url)
Figure 5.6: The transient response of output voltage (top) and total supply current (bottom) in the COSMOS NOR gate with 40 nm gates. The top figure also includes the input waveforms to the two gates. Only ‘00’ input produces a high output.

Figure 5.7: Similar to Fig.5.9 except at higher rail-to-rail voltages. At larger bias conditions the static leakage through the of 90°-bent $p$-$i$-$n$ diode becomes visible as well as the deterioration of the noise margins.
Figure 5.8 Summary of major performance figures for the COSMOS NOR gates driven at different rail-to-rail voltages.

Figure 5.9 The 3D view of a two-input NOR circuit using only two 40 nm COSMOS gates. a) Single-etch. b) Double etch is used for isolation of p-MOSFETs from n-MOSFETs.
The most important performance figures obtained from transient simulation of two-input NOR gates are summarized in Figure 5.8 for two different implementation of COSMOS gates: one with a single etch near the drain (similar to NOT gate) and one having two etches for p-MOSFET. These two etch scenarios are depicted in Figure 5.9 using TCAD visualization interface TecPlot. The uppermost subplot shows the static leakage observed in each case when the inputs are stable. In calculating this leakage data, we take a simple average of the 4 input cases assuming equal probability for each input to occur. This is reasonable for most general cases and should give an average evaluation of leakage performance. Gate delay and noise margin figures are calculated using the same approach as in logic NOT gate: \( t_{\text{delay}} = (t_{\text{LH}} + t_{\text{HL}})/2 \) and \( \text{NM}=|V_{\text{drive}}-V_{\text{out}}| \text{ p-p}. \) While delay improves for high drive voltages, the penalty is severe in terms of noise margin and static leakage. As expected in a two-input NOR gate \( t_{\text{LH}} \) and \( t_{\text{HL}} \) are very dissimilar, because of series p-MOSFETs being very slow to charge the load capacitor \( (C_L=1\text{fF}) \) compared to two parallel nMOSFETs charging it. This imbalance worsens further because of unequal electron and hole mobility used.

### 5.3.2 Three-input NOR Gate

The next step in COSMOS circuit configurations is to test a three-input COSMOS NOR gate block, which represents one of the ‘tough’ cases in static-logic circuit design due to three slower p-MOSFETs in series. Thus it is a very slow path from \( V_{\text{DD}} \) to output for charging the load capacitance. On the other hand it has three nMOSFETs in parallel, which makes the discharge times very fast, thus making the overall transient response very uneven. However, for generality, we use in Figure 5.10b the same average-delay
approach as before, due to equal number of transitions (one L→H and one H→L) per switching pulse, so do not see a significant slow-down. However, noise margin suffers significantly from having three series resistive MOSFETs in this circuit and 0.8V appears to be the preferred operation point for optimum performance. Also at a drive voltage of 0.6V there is a significant slow-down of switching response, due to poor response of three pMOSFETs in series at such low drive voltage.

Figure 5.10 a) The 3D view of a three-input NOR circuit using three 40nm COSMOS gates. b) The corresponding performance figures for various drive voltages.

5.3.3 General Three-input Gates

The final COSMOS logic-circuit analysis concerns a three-input gate with a general function \( F = (A' + B' + C') \). This is a good example for a three input circuit block and contains both NOR and NAND-like blocks, as described in Figure 5.11a. Transient response and performance metrics are provided in Figure 5.11b and 5.11c.
Figure 5.11 a) Schematic/Layout hybrid view of a general 3-input circuit, b) Its truth table, and c) Simulated transient response for a drive voltage of 0.6V.

While general characteristics of this new circuit is similar to the previous ones, it is obvious that NM and gate delays are improved while leakage characteristics are more gradually changing with significantly lower levels of leakage. Gate delay improvement in this three-input circuit is more than 300% over that of three-input NOR gate, and leakage reduction is almost one order of magnitude. These improvements prove that the previous
circuit is indeed an extreme case and does not reflect true potential of COSMOS for most general multiple-input circuits. Thus we can assume that most general circuits with up to three series transistor elements in individual pull-up and pull-down networks can be realized with COSMOS architectures. Of course the most important aspect is that the supply voltage is minimal at 0.5-1.0V range, in agreement with Silicon roadmap [58]

5.4 COSMOS Power*D Delay Product Analysis

At the heart of the power versus delay trade-off in COSMOS circuit is the static leakage stemming from the intrinsic formation of 90°-bent $p-i-n$ diode between the $V_{DD}$ and $V_{SS}$ contacts. The number of such contacts in close proximity increases in logic gates with multiple inputs, leading to more leakage. The leakage also becomes dependent on the input combinations and which channels are ON. Like all logic technologies, the large-scale COSMOS circuits can benefit from identification of power*delay product and how dynamic switching depends on drive conditions. We perform such an analysis in Table 5.1 below for the three example circuits analyzed previously and summarize cumulative performance comparison for two drive conditions 0.6V and 1.0V. Static leakage related power is also considered, as it can be a series limitation for the usability of a given technology. Their ratio is provided in the bottom row.
Table 5.1 Performance Comparison and Simulated Power • Delay Product in COSMOS Logic Circuits with Multiple Inputs.

<table>
<thead>
<tr>
<th>Circuit</th>
<th>NOT</th>
<th>2NOR</th>
<th>3NOR</th>
<th>3 AND/OR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drive Voltage</td>
<td>0.6V</td>
<td>1.0V</td>
<td>0.6V</td>
<td>1.0V</td>
</tr>
<tr>
<td>Dynamic Power (µW)</td>
<td>1.15</td>
<td>13.75</td>
<td>1.032</td>
<td>16.13</td>
</tr>
<tr>
<td>Delay (ps)</td>
<td>360</td>
<td>102</td>
<td>454</td>
<td>91</td>
</tr>
<tr>
<td>Power•Delay (10^{-12} W•s)</td>
<td>0.41</td>
<td>1.4</td>
<td>0.47</td>
<td>1.50</td>
</tr>
<tr>
<td>Static power (µW)</td>
<td>0.0084</td>
<td>2.28</td>
<td>0.0036</td>
<td>3.967</td>
</tr>
<tr>
<td>Static/Dynamic Power Ratio (%)</td>
<td>0.73</td>
<td>16.6</td>
<td>0.35</td>
<td>24.6</td>
</tr>
</tbody>
</table>

It is obvious from this comparative analysis that 1.0V drive is definitely a hard-limit for operation since static leakage is intolerable for all circuits except simple inverters. Except the 3-input NOR circuit, 0.6V operation acceptable for all circuits, since static power should be limited to ≤~1%. More importantly, figures in this table compare well with similar building blocks using conventional CMOS architecture [69]. In any case, since NAND gates are preferred over NOR gates in logic designs, our figures are likely to improve dramatically in real applications. One can manipulate logic functions to ensure their form is most suitable for COSMOS implementation that has the best power•delay product available for a given technology. Of course, it must be re-emphasized that COSMOS has the added advantage of reducing parasitics and substantial area gain, which can bring further performance gain in large system integration. In other words, even at similar gate-level performance COSMOS may have additional gains over conventional CMOS in terms of total system power•delay product, especially in low-power applications.
5.5 COSMOS Geometry Variations

This section is an attempt at determining how the novel COSMOS architecture is affected by fabrication and mask tolerances in sub-50 nm, which can be significant due to finite critical thickness control ability in such low dimensions [71]. Fabrication tolerances can result in a number of changes to ideal COSMOS gate dimensions used in the above analyses. The first error we consider is the impact of error in gate width (length) for the nMOS (pMOS) device in the COSMOS inverter, while the pMOS (nMOS) length (width) remains the same (see Figure 5.12). Currents in this figure has been normalized with respect to the nominal 40nm COSMOS gate with minus sign implying reduction in magnitude. Changes in the threshold and ON-current are shown in each sub-plot for variations in both n and p-MOSFET widths.

Figure 5.12  Sensitivity of a nominally 40 nm COSMOS device pairs to variations in gate width. In all cases both variations are linear, small and decoupled. Percentage change in the ON current of each MOSFET as a result of changes in the width are similar.
In COSMOS gates a square-gate geometry is generally desirable, a small departure from this shape may be conveniently utilized in device design to fine-tune small differences in the currents of the two MOSFETs not accounted for in vertical layer design. Figure 5.12 shows that geometrical variations in one of the transport direction is decoupled from the other, and linearly scales with the magnitude of the variation. For both MOSFETs, the device ON current is more affected with negligible effect in $V_T$ when $W/L$ is varied. The relative change in ON current with respect to nominal device ($L=36\text{nm}$), is similar in magnitude and follows a linear trend for both MOSFETs.

The second geometrical error is concerned with the shifting of the center channel-cross with respect to the gate. Such a shift can happen due to printing, alignment or etching errors in COSMOS active area definition. Luckily, we find that such errors would have minimal impact on device characteristics, as can be understood from Figure 5.13. In fact, the sub-threshold slope (bottom sub-plot) and threshold voltage (top sub-plot) have no dependence on the location of the center point at all. It only affects the ON-current, when the center shift exceeds 20% of overall gate length in that direction.

The rotation of square gate around center axis is not explicitly simulated in this work. However, it is obvious from Figure 5.13 results that it should be fairly limited since rotated gate may be approximated as gate segments in which center point gradually shifts between the two extremes. The above simulations hence show that COSMOS structure is not sensitive to geometrical variations resulting from manufacturing errors and orthogonal placement of the two MOSFETs causes no real concern.
5.6 COSMOS Layout Considerations

In the original COSMOS layout given in Figure 5.14b, we have assumed that the gate may be contacted from directly above with a via hole, which is not a standard practice in CMOS. While this may be possible in future generations with metal gates such as considered here, an alternative COSMOS layout that allows a more standard gate contacting option is given in Figure 5.14c. In this scheme, the smallest feature of the MOSFET layout ($\lambda/2$) is gate straddle on either side of gate widths along the length of the channels. Therefore, we assume that the minimum feature in the proposed COSMOS layout does not correspond to the gate length/width. Note that in the side gate contacting scheme proposed in Figure 5.14c, the source–to-center distance is greater in both MOSFETs, i.e. gate is shifted toward the drains, and the gate lengths are now slight to
larger (3.5 \textit{\lambda}) to open room for side contacts. The previous analysis has shown that shifting of COSMOS center cross toward drain(s) in Figure 5.14c does not degrade device performance, while it allows room for the gate contact pad to be placed. Compared to area of a standard SOI CMOS pair $112.5\lambda^2 (9\lambda \times 10.5\lambda)$, designed with similar constrains using a pMOS device twice-larger (i.e. $\mu_N=2\mu_P$), we find that the original COSMOS pair with a top gate contact requires only $81\lambda^2 (9\lambda \times 9\lambda)$, while the modified design takes no more than $100\lambda^2 (10\lambda \times 10\lambda)$. Thus area saving for the modified design is of the order of $\sim 12.5\%$ whereas in the original design this is $28\%$. However, these estimates are based on modest mobility improvements of $\mu_N(Si)=2\mu_P(Si)=\mu_N(SiGe)=\mu_P(SiGe)$. As electron and hole mobilities are improved in strained Si/SiGe heterolayer design, the area savings may increase further up to $50\%$. Also, further (20\%) area can be gained by inserting an additional COSMOS gate in the empty area between in the middle of 4 adjacent COSMOS gates in a 2\times2 matrix.

An additional benefit expected of the above layout scheme is the elongation of intrinsic channel region in the parasitic \textit{p-i-n} diode that is responsible for static leakage in high drive conditions (see Figure 5.1). This should make the series resistance of the parasitic diode larger, hence reducing its leakage current at high bias conditions [72]. Therefore, we find that the modified COSMOS layout offers more realism and flexibility for fabrication, while also reducing the parasitic leakage possibility in COSMOS.
Figure 5.14. The layout examples for the a) planar SOI, b) original, and c) modified COSMOS devices. $\lambda$ refers to the basic unit in the layout design rules. Note that SOI device is made the same gate length as COSMOS. The elongation of source-to-source (south to east) distance in the modified layout is helpful for reduction of static leakage through the $p$-$i$-$n$ parasitic diode.
Chapter Six

Conclusions and Future Work

We presented the principles of operation of a novel CMOS architecture, named COSMOS, which is capable of static logic operation using only a single gate and active area. In the proposed COSMOS architecture, the MOSFET pair are orthogonally integrated under a single gate by a careful engineering of dual electron-hole channels in strained Si/SiGe on insulator substrates. As a result, we can eliminate the need to build two separate active areas with individual gate stacks, thus leading to significant saving in silicon chip area and reduction in RC parasitics, the most important delay component in nano-scale chips. It is expected that the saving in Si area is typically (~20%) and can run up to 50%, which may have dramatic financial and performance implications.

We explained design guidelines for symmetrical operation of COSMOS devices using 1D, 2D and 3D simulations. In our design methodology for COSMOS gates, 1D simulations are useful for accurate threshold design, while 2D simulations allow for quick evaluation of transistor characteristics and leakage concerns. 3D simulations were performed to fully-analyze COSMOS characteristics and switching performance. We verified logic operation using COSMOS inverter (NOT) gates.

The lateral scaling of COSMOS gate dimensions is limited by series parasitic resistance from source and drain overlap regions, which lead to lower ON current at smaller gate length. Full 3D simulations with quantum mechanical corrections and accurate mobility values for electron and hole channels are required to obtain precise
limits of this scaling limit. Present work only considers classical transport, which indicates that the scaling limit is around 20 nm for minimum gate length. Vertical design and scaling has less headroom: 3-6 nm channels appear to be optimum for COSMOS.

We can build multi-input logic circuits using combinations of COSMOS NOT gates in a very efficient layout with minimum routing lines, which should further benefit COSMOS design in large systems. Two and three-input NOR gates and a three-input general function have been simulated and analyzed in this PhD work. While excessive static-leakage and loss of noise margin is a serious limitation for operation above 1.0V drive (±0.5V supplies), these more realistic COSMOS gates appear to perform reasonably (~500 ps delay) at 0.6V drive, i.e. ultra-power operation. Therefore, using efficient routing techniques, very-dense logic circuits may be implemented in the proposed COSMOS architecture. Which is especially suitable for low-power applications. The main limitation for all circuits in high drive conditions is the static leakage from a parasitic p-i-n diode at high supply voltages. For operation with drive voltages ≤1.0V, power•delay product (typically between 0.5 Ws and 1.5 Ws) of COSMOS is comparable to conventional low-power CMOS logic gates [69]

In this work, we also address concerns for layout, mask tolerances in COSMOS architecture, and show that the cross-shaped active area is resilient to geometrical errors in the layout due to process tolerances. The variations in the gate width of one of the orthogonal device have no influence for the other and the shifting of the center-cross with respect to gate has minimal impact on device characteristics. This shows how significant area and performance gains can be obtained in CMOS logic circuits by a unique combination of layout and channel engineering.
This work is the first comprehensive treatment of general properties of COSMOS architecture to our knowledge and should allow designers to understand and design COSMOS devices and circuits. However, it would benefit immensely if the following steps are taken in immediate future in order to make COSMOS potential perfectly clear for designers:

Use of realistic electron and hole mobilities from ongoing experimental works on dual channel strained SiGe layers. Several such works became available in the last several months. Without actual experimental mobility values COSMOS optimization is not unique.

Employing quantum mechanical corrections, as computational resources become available. Since most COSMOS channel lengths and layer thicknesses are below typical limits (20-30 nm in length and <10 nm for layer thickness) for Si transistors, more accurate (but also rather lengthy) quantum mechanical corrections may be inescapable in future works.

Future work on this novel architecture can also focus on logic style investigation: It may be possible that COSMOS is utilized in other logic styles, such as gate-array logic circuits, FPGAs, pass gate logic or even phase-clocked dynamic logic circuits. COSMOS may be useful in a number of other applications: an obvious candidate is analog circuits that may use COSMOS gates and test structures for electron and hole transport experiments under the same physical gates. For instance, it will be quite interesting to analyze COSMOS gate as an analog mixer, where two AC signals are allowed to intermodulate the output. The orthogonal, compact integration of COSMOS may allow unique AC intermodulation performance.
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Appendix A

List of Publications From This Work


Appendix B

Example Input Files for Simulators

**Poisson-Schrodinger Solver Input File**

# 1D Layer structure for P-S solution

<table>
<thead>
<tr>
<th>Surface</th>
<th>t</th>
<th>x</th>
<th>Na</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiO2</td>
<td>10</td>
<td></td>
<td></td>
</tr>
<tr>
<td>str_Si</td>
<td>40</td>
<td>0.35</td>
<td>1e15</td>
</tr>
<tr>
<td>str_SiGe</td>
<td>30</td>
<td>0.35</td>
<td>1e15</td>
</tr>
<tr>
<td>SiO2</td>
<td>50</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SiO2</td>
<td>50</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SiO2</td>
<td>300</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SiO2</td>
<td>600</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Si</td>
<td>1000</td>
<td></td>
<td>1e15</td>
</tr>
</tbody>
</table>

substrate

fullyionized

v1 -1.5 1.5 0.1

# v1 0

# CV

schrodingerstart = 2

schrodingerstop = 120

temp = 300K

dy = 1
MATLAB Integration code

# MATLAB code integrating electron density from Poisson-Schrodinger Solver
clc;
clear all;
format short e

%variables

disp('This is a MATLAB program to collect ');
disp('electron/hole densities from PS solver');
vstart=double(-1.50e0);
vstop=double(1.5e0);
vstep=0.10e0;

% All thicknesses in Angstrom
tox=10;
tsi=60;
tsige=30;
tmargin=10;
t1=tsi;
t2=tsi+tsige;
p1=tox+tsi;
p2=tox+tsi+tsige+tmargin;
mypoints=[p1 p2];
thickness =[t1 t2];
thickness =1e-10*thickness;

[firstfile, mypath] = uigetfile('*.out', 'Pick a data file');

% hardwired USER FILENAME
%rootfile=input('tell me root filename [XXXX.txt.V]?','s')
%vstart=input('tell me start point for the sweep [vstart]?',)
%vstep=input('tell me step size for the sweep [vstep]?',)
%vstop=input('tell me stop point for the sweep [vstop]?',)

rootfile='cosmos60.txt.V'

vdata=vstart:vstep:vstop;

size=length(vdata);

count=length(mypoints);

for k=1:size
    mystring(k)=vstart +(k-1)*vstep;
    turnstring=num2str(mystring(k),''%4.2f'');
    myfile=[rootfile turnstring '.out'];
    fullfile= [mypath myfile];

    [x,n,p] = textread(fullfile,'%f%*f%*f%*f%*f%*f%*[^
]','headerlines',1);
    nint=cumtrapz(x,n);
    pint=cumtrapz(x,p);

    for t = 1:count
        result(k,t,1)=nint(find(x==mypoints(t)));
        result_rial(k,t,1)=thickness(t)*result(k,t,1);
        result(k,t,2)=pint(find(x==mypoints(t)));
        result_rial(k,t,2)=thickness(t)*result(k,t,2);
    end

%cubic_result(k)= [mystring(k)' result(:,2,1)' result(:,2,2)' result(:,1,2)];
%carial_result(k)= [mystring(k)' result_rial(:,2,1)' result_rial(:,2,2)' result_rial(:,l,2)];

cubic_result(1,k)= mystring(k);

cubic_result(2,k)= result(k,2,1);
cubic_result(3,k) = result(k,2,2);
cubic_result(4,k) = result(k,1,2);
cubic_result(5,k) = result(k,2,2) - result(k,1,2);
arial_result(1,k) = mystring(k);
arial_result(2,k) = result_arial(k,2,1);
arial_result(3,k) = result_arial(k,2,2);
arial_result(4,k) = result_arial(k,1,2);
arial_result(5,k) = result_arial(k,2,2) - result_arial(k,1,2);
end

cubic_result = cubic_result';
arial_result = arial_result';
save cubicedensity.txt cubic_result -ASCII -TABS
save arialdensity.txt arial_result -ASCII -TABS
Boundary and doping file for ISE TCAD Mesh

# The Doping mode allows us to set the doping concentrations as well as the grid spacing on the device.
# parameter declaration for boundary file
@ DUP 1 @

Definitions {
  # Refinement regions
  Refinement "default region"{
    Max Element Size = 0.02
    Min Element Size = 0.005
  }
  Refinement "top cross"{
    Max Element Size = (0.008, 0.008, 0.002)
    Refinement "active"{
      Max Element Size = (0.004, 0.004, 0.0005)
    }
  }
  # Profiles
  Constant "p-type epi"{
    Species = "Boron Concentration"
    Value = 1e+15
  }
  Constant "n-contact"{
    Species = "Phosphorus Concentration"
    Value = 1e+20
  }
  Constant "p-contact"{
    Species = "Boron Concentration"
    Value = 1e+20
  }
}

Placements{
  # Refinement regions
  Refinement "default region instance"{
    Reference = "default region"
  }
  Refinement "top cross instance" {
  }
}
Reference = "top cross"
Refine Window = cuboid \(((0.03, 0.03, 0.000), (-0.03,-0.03, 0.006)) \}

Refinement "active instance"{
  Reference = "active"
  Refine Window = cuboid \(((0.018, 0.018, 0.000), (-0.018,-0.018, 0.005))\}

# Profiles
Constant "p-type epi"{
  Reference = "p-type epi"
  Evaluate Window{
    Element = cuboid \[ (-0.04,-0.04, 0.0), (0.04,0.04,0.005) ] \}}

Constant "p-contact"{
  Reference = "p-contact"
  Evaluate Window {
    Element = cuboid \[ (0.01,0.018,0.0), (-0.01,0.03,0.003) ] \}}

Constant "n-contact"{
  Reference = "n-contact"
  Evaluate Window {
    Element = cuboid \[ (-0.03,-0.01,0.003) (-0.018,0.01,0.005) ] \}}

Constant "p-contact"{
  Reference = "p-contact"
  Evaluate Window {
    Element = cuboid \[ (0.01,-0.018,0.0), (-0.01,-0.03,0.005) ] \}}

Constant "n-contact"{
  Reference = "n-contact"
  Evaluate Window{
    Element = cuboid \[ (0.03,-0.01,0.0) , (0.018,0.01,0.005) ] \}}

The boundary mode allows us to indicate its general dimensions and contacts.
# Solid region

StrSiGe {cuboid [(-0.01,-0.03, 0.0) (0.01, 0.03, 0.003)]}
StrSiGe {cuboid [(-0.01,-0.01, 0.0) (0.03, 0.01, 0.003)]}
Oxide   {cuboid [(-0.01,-0.01, 0.0) (-0.03, 0.01, 0.003)]}
Si  {cuboid [(0.03, 0.01, 0.003) (-0.03,-0.01, 0.005)]}
Si  {cuboid [(0.01, 0.01, 0.003) (-0.03,-0.01, 0.005)]}
Oxide {cuboid [(0.01, 0.01, 0.003) (-0.01,0.02, 0.005)]}
Oxide {cuboid [(0.02, 0.01, 0.005) (-0.02,-0.01, 0.006)]}
Oxide {cuboid [(-0.01,-0.02,0.005) ( 0.01, 0.02,0.006)]}
Oxide {cuboid [(0.01, 0.01, 0.0) (0.02, 0.02, 0.006)]}
Oxide {cuboid [(-0.01,-0.01, 0.0) (-0.02,-0.02, 0.006)]}
Oxide {cuboid [(-0.01, 0.01, 0.0) (-0.02, 0.02, 0.006)]}
Oxide {cuboid [(0.01,-0.01, 0.0) (0.02,-0.02, 0.006)]}

# Contact area

Contact "gate" {rectangle [(0.02, 0.02, 0.006) (-0.02,-0.02, 0.006)]}
# Contact area
Contact "vdd" {rectangle [(0.01, 0.02, 0.003) (-0.01, 0.03, 0.003)]}
# Contact area
Contact "vss" {rectangle [(-0.03,-0.01, 0.005) (-0.02, 0.01, 0.005)]}
# Contact area
Contact "set1" {rectangle [(0.03,-0.01, 0.005) (0.02, 0.01, 0.005)]}
# Contact area
Contact "set2" {rectangle [(0.01,-0.02, 0.005) (-0.01,-0.03, 0.005)]}
DESSIS input deck for a transient mixed-mode simulation of COSMOS inverter.

```plaintext
# define COSMOS device block;

Device NOR_COSMOS { 
  File { 
    Grid = "nor_cosmos_msh.grd"
    Doping = "nor_cosmos_msh.dat"
    Plot = "nor_cosmos_drive7_des.dat"
    Current = "nor_cosmos_drive7_des.plt"
  }

  Electrode { 
    { Name = "vss" Voltage=0.0 }
    { Name = "vdd" Voltage=0.0 }
    { Name = "gate1" Voltage=0.0 Barrier=0.0 }
    { Name = "gate2" Voltage=0.0 Barrier=0.0 }
    { Name = "set1" Voltage=0.0 }
    { Name = "set2" Voltage=0.0 }
  }

  Physics { 
    Mobility ( Doping Dep E normal High Field sat )
    Effective Intrinsic Density (Old Slot boom)
    Mole Fraction (Region Name= ["Region.0" "Region.1"]
    X Fraction = 0.35 Grading = 0.0 )
  }
}
Device COSMOS {

  File {
    Grid = "slim2_msh.grd"
    Doping = "slim2_msh.dat"
    Plot = "slim2_drive7_des.dat"
    Current="slim2_drive7_des.plt"
  }

  Electrode {
    Name="vss" Voltage=0.0
    Name="vdd" Voltage=0.0
    Name="gate" Voltage=0.0 Barrier =0.0
    Name="set1" Voltage=0.0
    Name="set2" Voltage=0.0
  }

  Physics {
    Mobility( Doping Dep E normal High Fieldsat )
    Effective Intrinsic Density ( Old Slot boom )
    Mole Fraction (Region Name="Region.0" "Region.1")
    X Fraction = 0.35 Grading = 0.0
  }

  System {
    V source_pset vA (n6 n0) { pwl = (0.0e+00 -0.7
                               60.0e-11 -0.7
                               60.5e-11 0.7
                               120.0e-11 0.7
                               120.5e-11 -0.7
                               180.0e-11 -0.7)
    }

    Vsource_pset vB (n1 n0) { pwl = (0.0e+00 -0.7
                               30.0e-11 -0.7
                               30.5e-11 0.7
                              )
  }
Vsource_pset vC (n5 n0) { pwl = (60.0e-11  0.7
60.5e-11  -0.7
90.0e-11  -0.7
90.5e-11  0.7
120.0e-11  0.7
120.5e-11  -0.7
180.0e-11  -0.7))

Vsource_pset vC (n5 n0) { pwl = (0.0e+00  -0.7
15.0e-11  -0.7
15.5e-11  0.7
30.0e-11  0.7
30.5e-11  -0.7
45.0e-11  -0.7
45.5e-11  0.7
60.0e-11  0.7
60.5e-11  -0.7
75.0e-11  -0.7
75.5e-11  0.7
90.0e-11  0.7
90.5e-11  -0.7
105.0e-11  -0.7
105.5e-11  0.7
120.0e-11  0.7}
120.5e-11  -0.7
180.0e-11  -0.7)}

NOR_COSMOS nor_cosmos("vss"=n2 "vdd"=n4 "gate1"=n1 "gate2"=n5 "set1"=n3 "set2"=n3) COSMOS cosmos("vss"=n7 "vdd"=n4 "gate"=n6 "set1"=n2 "set2"=n3)

Capacitor_pset c1 ( n3 n0 ){ capacitance = 1e-15 }  

Set (n0 = 0.0)  

Plot "nodes.plt" (time() n0 n1 n2 n3 n4 n5 n6 n7)}

File { Current = "drive7nandor"

        Output = "drive7nandor"}

Plot { e Density h Density  

        e Current h Current  

        Electric Field Potential Doping Space Charge  

        Donor Concentration Acceptor Concentration}

Math { Extrapolate  

        Digits = 6

        Not damped=50  

        Iterations=15  

        New Discretization  

        Derivatives  

        RelErrControl  

        Err Ref(Electron) = 1.0E10  

        Err Ref(Hole) = 1.0E10  

        Const Ref Pot}
Direct Current

Solve { Poisson

Coupled { Poisson Circuit }

Coupled { Poisson Contact Circuit }

Coupled { Poisson Electron Hole Contact Circuit }

call(Filename="NANDOR_drive7_INIT")

# ramp vdd and vss to bias conditions:

New Current="NANDOR_drive7_setup_"

Quasi stationary ( Initial Step=1e-2   Max Step=0.05     Min Step=1e-8

Goal { Node=n1 Voltage=-0.7}

Goal { Node=n5 Voltage=-0.7}

Goal { Node=n6 Voltage=-0.7}

Goal { Node=n7 Voltage=-0.7}

Goal { Node=n4 Voltage=0.7}

{ Coupled {poisson electron hole contact circuit} } }

call(Filename="NANDOR_drive7_setup")

Set (n7 = -0.7)

Set (n4 = 0.7)

NewCurrent="NANDOR_drive7_timerun_"

Transient (Initial Time=0       Final Time=180e-11   Initial Step=1e-12

Max Step=5e-12   Min Step=1e-15     Increment=1.3  )

{ Coupled { poisson electron hole contact circuit } } }

call(Filename="NANDOR_drive7_timerun_end")}