Linearity Analysis of Single and Double-Gate Silicon-On-Insulator Metal-Oxide-Semiconductor-Field-Effect-Transistor

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Abstract

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As the scaling of MOSFET into sub-100nm regime, silicon-on-insulator (SOI) and
double-gate (DG) MOSFET are expect to replace traditional bulk MOSFET. These novel
MOSFET devices will be strong contenders for RF applications in wireless
communications market. Of all the figure of merits for RF design, this work is concerned
about the linearity design of bulk, single-gate SOI and DG SOI MOSFET in a
comparative manner. By using ISE TCAD suite, 2D device simulations are conducted to
analyze the influences of different physical mechanisms on linearity including quantum
mechanics, non-equilibrium transport, impact ionization and self-heating effects. Then,
influences of gate length scaling, silicon body thickness scaling and device sidewall
scaling on linearity performance are investigated. In general, this work studies linearity
performance of novel SOI MOSFET devices in terms of device physics and scaling
effects with the hope of giving guidance to SOI MOSFET designers for high RF linearity
design.

Approved:

Savas Kaya

Assistant Professor, School of Electrical Engineering and Computer Science
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<td>CMOS</td>
<td>Complimentary Metal Oxide Semiconductor</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal Oxide Semiconductor Field Effect Transistor</td>
</tr>
<tr>
<td>IC</td>
<td>Integrated Circuit</td>
</tr>
<tr>
<td>SCE</td>
<td>Short Channel Effects</td>
</tr>
<tr>
<td>SOI</td>
<td>Silicon on Insulator</td>
</tr>
<tr>
<td>BOX</td>
<td>Buried Oxide</td>
</tr>
<tr>
<td>FD</td>
<td>Fully Depleted</td>
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<tr>
<td>PD</td>
<td>Partially Depleted</td>
</tr>
<tr>
<td>DG</td>
<td>Double Gate</td>
</tr>
<tr>
<td>RF</td>
<td>Radio Frequency</td>
</tr>
<tr>
<td>IM</td>
<td>Intermodulation</td>
</tr>
<tr>
<td>IP3</td>
<td>Third Intercept Point</td>
</tr>
<tr>
<td>ISE</td>
<td>Integrated Systems Engineering</td>
</tr>
<tr>
<td>TCAD</td>
<td>Technology Computer Aided Simulation</td>
</tr>
<tr>
<td>DIBL</td>
<td>Drain-Induced Barrier Lowering</td>
</tr>
<tr>
<td>BTE</td>
<td>Boltzmann transport equation</td>
</tr>
<tr>
<td>DD</td>
<td>Drift-Diffusion</td>
</tr>
<tr>
<td>HD</td>
<td>Hydrodynamic</td>
</tr>
<tr>
<td>QM</td>
<td>Quantum Mechanical</td>
</tr>
<tr>
<td>II</td>
<td>Impact Ionization</td>
</tr>
<tr>
<td>SHE</td>
<td>Self-Heating Effects</td>
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Chapter 1. Introduction

1.1 General Introduction

Silicon CMOS technology has emerged over the last 25 years as the predominant technology of the microelectronics industry. The evolution of CMOS technology is governed by the Moore’s law, which states that the transistor density on integrated circuits doubles every couple of years. The continuing scaling of CMOS transistor has enabled integrated circuit with higher packing density, higher speed and lower power dissipation [1]. These have been key components leading to today’s computers and communication systems. However, as the CMOS dimension is scaled to the nanometer regime (<100nm), many physical barriers arise, which will finally prevent the traditional CMOS to be the candidate for future applications. Thus modifications to CMOS device structure to boost performance are necessary [2].

In sub-100nm scale, MOSFET are expected to undergo rapid and fundamental architectural changes, which are likely to include variants of silicon-on-insulator (SOI) MOSFET and double-gate (DG) MOSFET. Single gate SOI MOSFET has many advantages over traditional bulk MOSFET such as high speed and low power for digital circuit design. Double-gate SOI MOSFET is also wildly recognized as one of the most promising devices because of its short channel effect immunity, reduced leakage current and more scaling potential. Due to the inherent performance advantages, SOI MOSFET out-performs the conventional CMOS technology Fig. 1.1.
In addition to digital circuits, these novel MOSFET devices will be strong contenders also for analog RF applications in the wireless communications market [3]. RF CMOS provides a cost-efficient path for integration of digital logic circuits with analog and RF functions, allowing optimal system partitioning and reduction of parts count. It is expected that RF CMOS will have a 10% market share of the 40 billion semiconductor market for wireless integrated circuits. As a result, RF performance of SOI CMOS devices has attracted significant amount of interest recently [4]. Majority of these RF CMOS studies, however, place the emphasis only on understanding of several RF figures of merit such as cutoff frequency, maximum oscillation frequency and noise figure. There is, however, another important RF performance parameter, namely linearity, which has not yet received sufficient interest from the SOI CMOS design community. In this thesis work, I attempt to focus on linearity analysis of bulk MOSFET, single-gate SOI MOSFET and dual-gate MOSFET in a comparative manner.
1.2 Scope and Objectives

The investigation of RF linearity for novel SOI MOSFET structures has not received enough attention in the semiconductor device society. There are only several papers talking about MOSFET linearity for the past several years. Sanghoon Kang [5] reports the linearity analysis of bulk CMOS based on compact device models. Alberto O. Adan [6] gives an experimental work about RF performance of SOI MOSFET including linearity study of single gate SOI MOSFET. However, the impact from semiconductor device physics and device scaling for device linearity has not been investigated for either bulk or SOI MOSFET. Furthermore, linearity analysis of DG SOI MOSFET has not been reported.

In my thesis work, the RF linearity performance of sub-100nm gate length SOI and DG-MOSFET are investigated and compared with traditional bulk MOSFET. To study these devices, I use an industry-grade design package, ISE TCAD suite [7], which can realistically represent and simulate sub-100nm MOSFET with SOI substrate and double gate structures. It has efficient tools to design, simulate and eventually record the desired performance characteristics, which may then be further processed to calculate RF linearity characteristics. First of all, I carry out a study to analyze the influence of different physical mechanisms on linearity using 2D device simulations. In contrast with compact models used in [5], the use of physics-based device simulators provides a more complete and accurate alternative to include quantum mechanics (QM), non-equilibrium transport, impact ionization and self-heating effects for linearity analysis. Secondly,
influence of gate length scaling, silicon body thickness scaling and device sidewall scaling on linearity performance of SOI and DG MOSFET are investigated.

The main objectives of this thesis are to understand the structure design of novel SOI MOSFET while comparing them with traditional bulk MOSFET, to investigate the linearity performance of single gate and double gate SOI MOSFET in terms of device physics and scaling effects. Thus I hope to give guidance to SOI MOSFET designers and manufacturers of how to optimize and control RF linearity with respect to device physics and scaling effect.
Chapter 2. Device Scaling

2.1 MOSFET Scaling

MOSFET (Metal-Oxide-Semiconductor-Filed-Effect-Transistor) device (Fig.2.1) has been the predominant technology during the past three decades for semiconductor industry, becoming the backbone of today’s Integrated Circuit (IC) technology in middle 70’s. The advancement of IC industry is largely driven by the technology of MOSFET transistor minimization, which is called MOSFET down scaling.

The basic idea of MOSFET scaling is the progressive reduction of MOSFET dimensions, which will finally result in higher packing density, higher switching speed and lower power dissipation of integrated circuits [1]. When the dimensions of a MOSFET are scaled down, some basic guidelines must be followed. A proper scaling of MOSFET requires not only reduction of gate length and width, but also needs the reduction of other
device parameters such as gate oxide thickness, junction depth and doping density. Generally, there are two types of scaling rules. The first one is full scaling or constant field scaling which is proposed by Dennard et al. [1] and illustrated in Fig.2.2. Constant field scaling means that all device dimensions are scaled by the same factor $S$ and the supply voltage and other voltages are also scaled to maintain a constant electric field throughout the device. The second scaling rule is constant voltage scaling, which maintains a constant voltage during scaling.

![Figure 2.2 MOSFET constant field scaling [1]](image)

In reality, constant field scaling is not a feasible solution. In order to be compatible with the existing circuit technology, supply voltage cannot be scaled arbitrarily. Otherwise, it would be much more expensive to provide multiple voltage supplies to circuit component. On the other hand, scaling potential of threshold voltage is limited. It would be difficult to turn off the device if the threshold voltage is scaled too low. Constant voltage scaling does not have a supply voltage modification problem, which makes it a more preferred scaling law. But the disadvantage of constant voltage scaling is that the
electrical field increases when device is scaled to smaller dimension, which will lead to a series of negative physical effect as velocity saturation, mobility degradation, increased leakage currents and lower breakdown voltages. These two scaling laws are listed in the Fig 2.3, which illustrates that scaling MOSFET is not a trivial task requiring precise changes in many parameters at each technology generation. The complexity of scaling causes scaling technology to become also very expensive.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Before Scaling</th>
<th>After Full Scaling</th>
<th>After Constant Voltage Scaling</th>
</tr>
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<tbody>
<tr>
<td>Channel length</td>
<td>L</td>
<td>L/S</td>
<td>L/S</td>
</tr>
<tr>
<td>Channel width</td>
<td>W</td>
<td>W/S</td>
<td>W/S</td>
</tr>
<tr>
<td>Gate oxide thickness</td>
<td>t_{ox}</td>
<td>t_{ox}/S</td>
<td>t_{ox}/S^*</td>
</tr>
<tr>
<td>Junction Depth</td>
<td>x_j</td>
<td>x_j/S</td>
<td>x_j/S</td>
</tr>
<tr>
<td>Doping Densities</td>
<td>N_A, N_D</td>
<td>S·N_A, S·N_D</td>
<td>S^2·N_A, S^2·N_D</td>
</tr>
<tr>
<td>Power supply voltage</td>
<td>V_{DD}</td>
<td>V_{DD}/S</td>
<td>V_{DD}</td>
</tr>
<tr>
<td>Threshold Voltage</td>
<td>V_{T0}</td>
<td>V_{T0}/S</td>
<td>V_{T0}</td>
</tr>
</tbody>
</table>

Figure 2.3 Two laws of MOSFET scaling [9]

As the dimensions of the traditional MOSFET are scale down to the nano-meter regime, many physical barriers need to be dealt with, such as the short channel effects (SCE) and increased leakage current. Short channel effects are related to undesirable device characteristics which become stronger as the gate length is reduced without re-scaling the entire device. All of these physical limits and economic prevent traditional MOSFET to be the candidate for future nano-scale application. In this case, continued scaling of MOSFET may be pushed by adopting novel device structures. Two of the solutions for
nano-scale MOSFET are the Silicon-On-Insulator (SOI) technology and Double-Gate (DG) MOSFET.

2.2 SOI MOSFET

SOI is initially invented for application in many special environments, such as radiation-hardened or high-voltage integrated circuits. It is only in recent years that SOI has emerged as a serious contender for low-power and high-performance applications [10]. SOI MOSFET is different from the traditional bulk MOSFET. For bulk MOSFET, the silicon channel region is built on the substrate directly. For SOI MOSFET, a buried oxide layer is formed on the bulk silicon substrate. On the top of the buried oxide layer there is a silicon thin film, where active MOS devices and circuits are located. The cross section of a basic n-type MOSFET on SOI is shown in Fig.2.4 (a) and a photograph of a fabricated SOI MOSFET example is shown in Fig. 2.4 (b).

![Fig.2.4 (a) Structure of SOI MOSFET](image1)

![Fig.2.4 (b) Photograph of real SOI MOSFET](image2)
SOI MOSFET has many advantages over bulk MOSFET in device and circuit level. Because of the buried oxide (BOX) layer, the parasitic capacitances of SOI MOSFET devices are smaller than those of bulk MOSFET. Thus, the delays of digital CMOS circuit due to the junction capacitances can be reduced by using SOI MOSFET, which therefore increase the speed of the digital CMOS circuit. In another aspect, the power-delay product of SOI CMOS circuit is much smaller as compared to the bulk counterpart, again owing to the smaller parasitic capacitances in SOI MOSFET as well as reduced leakage currents through BOX. So we can say that, SOI MOSFET technology has high-speed and low-power properties. In device aspect, SOI MOSFET has no latch-up due to the buried oxide isolation and device isolation is much simpler for the SOI MOSFET as compared to the bulk MOSFET, which make SOI CMOS technology a higher device density and an easier device isolation structure.

Although these advantages of SOI technology are well known, the successful introduction of SOI technology for large-scale applications faces some key challenges across the entire spectra of material, process, manufacturing, devices, and designs. The SOI manufacturing processes are just becoming mature enough for mass production of low-cost, low-defect-density substrates. Another major concern is the control of silicon film thickness to accurately control the threshold of fully depleted devices.

SOI MOSFET can be further divided as partially depleted (PD) and fully depleted (FD) SOI device Fig.2.5. For FD SOI device, the SOI layer is much smaller than the depletion width of the device and its potential is tightly controlled by the gate. That means that
there is no neutral region of the body of the MOSFET that can be charged. The advantages of the FD SOI MOSFET include the elimination of the floating-body effect and better short-channel behavior. However, the better control of short-channel effects comes from the reduced source/drain junction depth, which increases the series resistance of the source/drain.

![Fig.2.5 (a) Structure of partially depleted SOI MOSFET](image1)
![Fig.2.5 (b) Structure of fully depleted SOI MOSFET](image2)

Furthermore, the requirement of silicon thickness smaller than depletion width results in a low device threshold voltage with high sensitivity to process and thickness variations. For PD SOI device, the SOI layer thickness is thicker than the maximum depletion width of the gate. Usually, the silicon film thickness is more than 50nm, which alleviates the constraint on device threshold voltage and its sensitivity. Also, PD SOI device make the manufacturing easier and the process and device design are much more compatible than with traditional bulk CMOS. However, the major issue of the partially depleted device is the floating-body effect and the resulting parasitic bipolar effect.
In general, PD SOI device is optimal for high speed and is being targeted for applications where highest clock rates are needed. FD SOI device allows optimization for high temperature and extremely low power applications. What is more important is that FD SOI device is considered as the best candidate for low noise RF microelectronics. RF figures of merit of FD SOI device such as cutoff frequency, maximum oscillation frequency, noise and transconductance are much better than bulk MOSFET and PD SOI MOSFET. Consequently, all of the SOI devices simulated and studied in this thesis are FD SOI MOSFET, which are more likely to be used in RF CMOS circuit in the next decade.

2.3 Double-Gate MOSFET

Double-Gate MOSFET has been generally recognized as one of the most promising device structures enabling MOSFET to be scaled under 25nm successfully. It is a special SOI MOSFET with two gates controlling the channel instead of one gate as in the traditional bulk MOSFET as shown in Fig.2.6. The two gates surrounding the conducting channel ensures that a better gate control over the channel can be applied, which reduces the leakage current, the drain-induced barrier lowering effect and the short-channel effect. The features of DG MOSFET are [2]: (1) the control of the short channel effects is mainly accomplished by novel device geometry not by channel doping or halo doping, (2) the thin silicon channel leads to tight coupling of the gate potential with the channel potential. These features provide DG FET advantages that include: (a) the reduced SCE leads to a shorter allowable channel length compared to bulk MOSFET. (b) A sharper subthreshold slope (60 mV/dec compared to 80 mV/dec for bulk FET) which allows for a
larger gate overdrive for the same power supply and the same off-current; (3) DG structure has a better carrier transport as the channel doping is reduced or even undoped. This reduced channel doping also relieves a key scaling limitation due to the drain-to-body band-to-band tunneling leakage current.

Fig. 2.6 (a) Structure of Double Gate MOSFET  
Fig. 2.6 (b) Photograph of real Double Gate MOSFET

As far as the electrostatics of a DG MOSET is considered, it can be designed as symmetric and asymmetric device. Here symmetry is defined in relation to gate impact on channel potential, with asymmetric device having different characteristics for each gate. Because of dissimilar metal-semiconductor work-function difference at the two interfaces, these two devices have considerable differences in terms of threshold and drain current. In general, for symmetric DG MOSFET, both the top gate and the bottom gate have the same work function and are tied to the same bias. So there are two surface channels at two sides of the silicon body. Those two surface channels conduct at the same time. For the asymmetric DG MOSFET, the two gates are fabricated utilizing both n+ and p+ polysilicon gates, which makes two different work functions for the two gates. In another way, these two different work functions can be generated by biasing the two gates at
different voltages. Thus, contrary to the symmetric DG MOSFET, only one of the two channels turns on at the beginning and as the gate voltage is increased the other channel also inverts [13].

The comparison of symmetric and asymmetric DG MOSFET is given rigorously by Taur [14]. Schematic of the band diagram for the symmetric case is shown in Fig.2.7 and asymmetric case is shown in Fig.2.8.

For asymmetric DG MOSFET at zero gate voltage in Fig.2.7 (a), the silicon bands have a near constant slope. For asymmetric DG MOSFET near the threshold voltage in Fig.2.7 (b), the conduction band of the silicon body at the left surface is bent to near the conduction band of the n source-drain. For symmetric DG MOSFET at zero gate voltage in Fig.2.8 (a), the silicon bands are flat. For symmetric DG MOSFET near the threshold
voltage in Fig. 2.8 (b), the conduction band of the silicon body is bent at both surfaces.

Linearity analysis of DG MOSFET based on the difference of symmetric and asymmetric structure has been reported [13]. In the present thesis work, only the symmetric DG MOSFET will be studied for linearity analysis.
Chapter 3. MOSFET Linearity

3.1 RF CMOS

The explosive growth of communication technology has created mass consumer markets for Radio-Frequency (RF) electronics. Take mobile communications as an example, it is one of the fastest growing areas over the past decade. Currently, the multiple access techniques such as time division multiple access (TDMA), code division multiple access (CDMA), and global system for mobile communications (GSM) are used in the 2G systems [15]. Looking further ahead, the third-generation (3G) mobile communication system will have huge market potentials.

RF semiconductor devices are the backbone of advanced communication systems. Traditionally, the RF electronics were once considered the exclusive domain of III-V or silicon bipolar technologies. Several competing semiconductor device technologies serve as the basics of RF electronics. They range from III-V compounds based on GaAs and InP, wide bandgap materials (SiC and III-nitrides), MESFET - Metal Semiconductor FET, HEMT - High Electron Mobility Transistor, HBT - Heterojunction Bipolar Transistor and BJT - Bipolar Junction Transistor. Although in the past decade, III-V technology dominates RF market, RF MOSFET becomes a strong contender recently.
Traditionally, CMOS technology is mainly used in digital circuit design. As the scaling of MOSFET into the sub-100 nm regime and the enormous momentum of the digital market, the delay in CMOS technology is getting smaller and analog performance is becoming appropriate for the Radio-Frequency (RF) circuits. Contrast to digital CMOS design, which is optimized and characterized for primarily one tradeoff between speed and power dissipation, analog/RF circuits entail a multidimensional design space. This is illustrated in Fig.3.1, where almost every two parameters trade with each other. As marked in Fig.3.1, linearity is one of the RF figures of merit and has implications for gain and noise.

Another important parameter, which marks the entrance of MOSFET into RF market, is cutoff frequency $f_c$. It is the frequency at which the small signal current gain of the transistor rolls off to unity (0 dB). Fig.3.2 shows the cutoff frequency versus gate length.
of MOSFET reported at 2002 [17]. We can see that for MOSFET with gate length under 100nm, the cutoff frequency can reach up to 200GHz.

For the fact that the cutoff frequency should be around 10 times the transistor’s operating frequency, these MOSFET can be used to design integrated circuits operating up to 20GHz, an operating frequency higher than that for the majority of modern RF circuits. This trend of continuing increased cutoff frequency of MOSFET make CMOS get more attention for RF applications in the wireless communication market. However, cutoff frequency is not the only requirement for good RF design. There are other figures of merits important for RF design including maximum oscillation frequency $f_{\text{max}}$, linearity and noise figure $NF_{\text{min}}$. High maximum oscillation frequency, high linearity and low noise figure are also critical for RF design. The formulas of figures of merit for RF design are given below [18],

$$ f_i = \frac{1}{2\pi} \frac{g_m}{C_{gg} + C_{par} + C_{gso} + C_{gdo}} $$

(3.1)
\[ f_{\text{max}} = \frac{f_i}{2\sqrt{\left(R_g + R_i\right)g_{ds} + 2\pi f_i C_{gdo}}} \]  
\[ NF_{\text{min}} = 1 + K \frac{f}{f_i} \frac{1}{\sqrt{g_m(R_g + R_i + R_s)}} \]

where the capacitances \( C_{gg}, C_{par}, C_{gso}, C_{gdo} \) are the intrinsic input capacitance, parasitic gate-bulk capacitance, and the gate-source and gate-drain overlap capacitances. \( R_g \) is the gate resistance and \( R_i \) is the real part of the input impedance due to nonquasistatic effects. \( R_s \) and \( g_{ds} \) are the source series resistance and output conductance.

To date, the research on \( f_i, f_{\text{max}} \) and noise figures of CMOS have been widely reported [17, 19, 20] while little focus has been applied to the linearity figure of CMOS technology [3, 5, 6]. Furthermore, currently, the RF MOSFET structures are conventional single gate bulk and SOI MOSFET, the linearity study of novel Double Gate SOI MOSFET has not been investigated at all.

### 3.2 Nonlinear Systems

Although many analog and RF circuits can be approximated with a linear model to obtain their response to small signals, nonlinearities often lead to interesting and important phenomena. [18] In some analog building blocks, such as power amplifier and low noise amplifier, nonlinearity results in harmful effects which degrade the system performance. So in these cases, nonlinearity needs to be minimized to guarantee high performance. While in some other applications, circuit designer may need nonlinearity to build circuits such as mixer and frequency multipliers. These applications need to maximize
nonlinearities. For example, let us consider a time-variant system and assume the input
x(t) output y(t) relationship can be approximated with a polynomial,

\[ y(t) = \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) + \ldots \]  

(3.4)

Where \( \alpha_j \) are in general function of time.

If a sinusoid is applied to a nonlinear system, the output generally exhibits frequency
components that are integer multiples of the input frequency. If \( x(t) = A \cos(\omega t) \), then

\[ y(t) = \alpha_1 A \cos(\omega t) + \alpha_2 A^2 \cos^2(\omega t) + \alpha_3 A^3 \cos^3(\omega t) \]

\[ = \alpha_1 A \cos(\omega t) + \frac{\alpha_2 A^2}{2} (1 + \cos(2\omega t)) + \frac{\alpha_3 A^3}{4} (3\cos(\omega t) + \cos(3\omega t)) \]

\[ = \frac{\alpha_2 A^2}{2} + (\alpha_1 + \frac{3\alpha_3 A^3}{4}) \cos(\omega t) + \frac{\alpha_2 A^2}{2} \cos(2\omega t) + \frac{\alpha_3 A^3}{4} \cos(3\omega t) \]  

(3.5)

In Eq. (3.5), the term with the input frequency is called the “fundamental” and the higher-
order terms the “harmonics”.

### 3.3 Intermodulation

While harmonic distortion is often used to describe nonlinearities of analog circuits,
certain cases, such as a low-pass filter, require other measures of nonlinear behavior.
“Intermodulation distortion” in a “two-tone” test is another important measurement of
nonlinear behavior.

When two signals with different frequencies are applied to a nonlinear system, the output
in general exhibits some components that are not harmonics of the input frequencies.
Called intermodulation (IM), this phenomenon arises from multiplication of the two signals when their sum is raised to a power greater than unity. For example, if input $x(t)$ consists of sinusoids of two frequencies $\omega_1$ and $\omega_2$, then output contains intermodulation terms at the frequencies $n\omega_1 \pm n\omega_2$

![Fig.3.4 Intermodulation of a nonlinear system [18]](image)

The order of an intermodulation product is $(n+m)$. Of particular interest are the third-order IM products at $\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$, which are the largest components (Fig.3.4).

![Fig.3.5 Corruption of a signal due to intermodulation between two interferers [18].](image)
Intermodulation is a troublesome effect in RF systems. For example in Fig. 3.5, if a weak signal accompanied by two strong interferers experiences third-order nonlinearity, then one of the IM products falls in the band of interest, corrupting the desired component [18].

### 3.4 Third Intercept Point

The corruption of signals due to third-order intermodulation of two nearby interferers is so common and so critical that a performance metric has been defined to characterize this behavior called “third intercept point” (IP3), this parameter is measured by a two-tone test in which $A$ is chosen to be sufficiently small so that higher-order nonlinear terms are negligible and then gain is relatively constant and equal to $\alpha_1$. We also know that as $A$ increases, the fundamentals increase in proportion to $A$, whereas the third-order IM products increase in proportion to $A^3$. So the magnitude of the IM products grows at three times the rate at which the main component increase. The third-order intercept point is defined to be at the intersection of the two lines. The horizontal coordinate of the point is called the input $\text{IP}_3$ ($\text{IIP}_3$), and the vertical coordinate is called the output $\text{IP}_3$ ($\text{OIP}_3$). The higher value of third-order intercept point means more linear the device.

Fig. 3.6 Growth of output components in an intermodulation test [18].
3.5 Calculation of Device Linearity

For a direct evaluation of RF linearity performance of MOSFET, drain saturation current, \( I_{\text{Dsat}} \), and threshold voltage, \( V_T \), are not suitable figures of merit in the way they are used in digital circuits. A reliable and simple metric used to evaluate linearity performance of individual MOSFET is the input-referred IP3 point.

To model the non-linearity, a MOSFET modulated with an AC gate voltage, \( V_g \), producing a drain current, \( I_d \), can be viewed as a time variant non-linear system

\[
I_d = I_0 + g_{m1}V_g + g_{m2}V_g^2 + g_{m3}V_g^3 + \ldots
\]  

(3.6)

where Taylor expansion coefficients are \( g_{mn} = \frac{1}{n!} \frac{\partial^n I_d}{\partial V_g^n} \) and \( I_0 \) is the current at DC operation point. Thus, a nonlinear MOSFET, even for a pure sinusoidal input, would produce many harmonics and a DC term, wasting useful output power. Moreover, the third-order non-linearity term, \( g_{m3} \), is especially troublesome for RF systems, since it leads to inter-modulation, i.e. distortion of the fundamental amplitude via signals in the adjacent bands. Signal power, \( P_{\text{IP3}} \), where this spurious term is equal to the fundamental one is called the third-order inter-modulation intercept point. Using (3.6) and assuming a matched input resistance of \( R_s=50\Omega \) for the system, \( P_{\text{IP3}} \) can be expressed in terms of non-linearity coefficients [18]:

\[
P_{\text{IP3}} = \frac{2g_{m1}}{3g_{m3}R_s} - \frac{4(\partial I_d / \partial V_g)}{R_s(\partial^3 I_d / \partial V_g^3)} \ldots
\]  

(3.7)
3.6 Output Conductance Considerations

So far, I have only accounted for nonlinearities due to the device transconductance. However, other important transfer parameters of MOSFET, notably the output conductance $g_d$ also have a dependence on the operation point as well as frequency, hence introduce further nonlinearities [6]. The equivalent circuit model of MOSFET is shown in Fig.3.7, where not only the transconductance nonlinearity $g_{m2}$, $g_{m3}$ are considered but also the output conductance nonlinearity $g_{d2}$ is included.

![Fig.3.7 Equivalent Circuit Model of MOSFET including nonlinear transconductance $G_m$ and output conductance $G_d$ [6].](image)

Including (3.6) currents due to nonlinear output conductance terms in a similar manner, a more accurate relationship for $P_{IP3}$ may be obtained [6]:

$$G_m = g_m + g_{m2} \cdot V_m + g_{m3} \cdot V_m^2$$

$$G_d = g_d + g_{d2} \cdot V_o$$

$$g_{mn} = \frac{1}{n} \frac{\partial^n I_d}{\partial V_{gs}^n}, \quad g_{dn} = \frac{1}{n} \frac{\partial^n I_d}{\partial V_{ds}^n}$$
\[
P_{IP3} = \frac{2}{3R_s} \left| \frac{g_m^3}{g_m} + \frac{4}{3} \frac{g_m g_{d2}}{G_0(\omega_i)G_0(\Delta \omega)} \right|^{-1},
\]

where \( g_{d,n} = \frac{1}{n!} \frac{\partial^n I_d}{\partial V_d^n} \) and \( G_0(\omega) = G_L + g_d(\omega) + j\omega C_d \). Here \( G_L = 0.02 \) S, which corresponds to the conductance of a 50 \( \Omega \) load typically found in matched RF systems. Note that (3.7) and (3.8) are identical for MOSFET with negligible nonlinearity in the output conductance, which is also a function of frequency. In partially depleted SOI MOSFET, the ‘kink’ effect associated with the impact-ionized carriers [4] result in further \( g_d \) nonlinearity, which is largely minimized in FD designs.
Chapter 4. Device Simulation

4.1 ISE Introduction

ISE TCAD (Technology Computer Aided Design) is a software package providing simulation for semiconductor device, integrated circuit and semiconductor manufacturing. Its advanced semiconductor device and process simulator can generate accurate prediction of the fabrication processes and the operation of devices, which make ISE TCAD widely used semiconductor companies, such as Intel, Texas Instrument and Motorola. The products of ISE TCAD which are used in my thesis research includes: GENESIS, MDRAW, MESH, DESSIS, INSPECT and TECPLOT.

4.1.1 GENESIS

GENESIS (Fig.4.1) is ISE’s primary graphical front end that integrates ISE simulation programs into one environment. Its intuitive graphical user interface is used to design, organize, and run simulations for semiconductor research and manufacturing. GENESIS automatically manages the information flow, which includes preprocessing of user input files, project parameterization, setting up and execution of tool instances, and visualization of results with appropriate viewers. The use of mathematical and logical expressions serves to preprocess the simulation input dynamically [7].
4.1.2 MDRAW

MDRAW offers flexible two-dimensional device editing features, including contact handling, refinement, and doping specification, and a direct link to the ISE meshing engines. It is a device editor and mesh generator that can be used either through a GUI or in a script mode. Gaussian, error, and constant functions, 1D external data, and general analytic functions are used as analytic doping profiles in both the primary and lateral directions. The doping profiles of MDRAW contain species, such as boron, arsenic, phosphorus, and antimony, which can be used for analytic doping [7].
4.1.3 MESH

ISE provides approaches for the automatic generation of meshes. The meshes are not only adapted to the geometry, but also to the doping concentration in order to capture steep gradients.

In my simulations, I use a combination of refinement and multi-box to mesh the interested region of devices. The mesh points for single device are around 2500-3000. According to my experience, the number of mesh points larger than 3000 will dramatically decrease the speed of simulation. In the case that is smaller than 2000, the result curves will not be smooth enough.

4.1.4 DESSIS

The comprehensive semiconductor device simulator DESSIS simulates the electrical, thermal, and optical characteristics of semiconductor devices. It is the leading device simulator and handles 1D, 2D, and 3D geometries, mixed-mode circuit simulation with
compact models, and numeric devices. It contains a comprehensive set of physical models that can be applied to all relevant semiconductor devices and operation conditions. DESSIS is used to evaluate and understand how a device works, optimize devices, and extract SPICE models and statistical data early in the development cycle.

In my simulation, all the device structures are 2D. The electrical and thermal simulations are conducted to investigate the device performance. Various electron transport models from DESSIS are used to study the physics effect on device linearity performance.

4.1.5 INSPECT

INSPECT is ISE’s plotting and analysis tool for X-Y data, such as doping profiles and electrical characteristics of semiconductor devices. In my thesis work, INSPECT is mainly used to view the simulation results, such as $I_d/V_g$, $I_d/V_d$ curves from DC simulation and $g_{mn}$, $g_d$ curves from AC simulation. After getting these curves, I export the data from INSPECT as ASCII format for plotting and post processing by other software.

4.1.6 TECPLOT

Tecplot-ISE is plotting software with extensive 2D and 3D capabilities for visualizing data from simulations and experiments. It represents state-of-the-art scientific visualization. In addition, Tecplot-ISE is used to explore and analyze data, to produce informative 2D and 3D views. In my thesis work, Tecplot-ISE is used to view various dataset generated by simulations to investigate the device operations. I can plot carrier density, carrier mobility, doping density, electrical field, band structure and so on by Tecplot-ISE
4.1.7 DIOS

DIOS is a multidimensional process simulator for semiconductor devices. It allows for the simulation of complete fabrication sequences including etching and deposition, ion implantation, diffusion, oxidation, and silicidation. It is the most accurate process simulator available. DIOS has been applied to a wide variety of technologies such as VLSI CMOS, SiGe HBT, power devices, and advanced SOI processes, in many of the leading semiconductor companies. Although DIOS has not been used in my thesis work, process modeling and advanced CMOS device will be my future interest.

4.2 Simulation Transport Models

4.2.1 Charge Transport Models

In my thesis work, impact of various device physics on linearity performance is studied based on simulation of different physical transport models. This section will give a brief introduction of different transport models.

Physical phenomena in semiconductor devices are very complicated and are described by partial differential equations of different level of complexity. For conventional semiconductor devices, such as field-effect transistor, the device behavior is adequately described within the classical model of charge transport models, which is defined by the Boltzmann transport equation (BTE) (4.1) [7]

\[
\frac{\partial f(r,k,t)}{\partial t} + \frac{1}{\hbar} \nabla_k E(k) \ast \nabla_r f(r,k,t) + \frac{F}{\hbar} \ast \nabla_k f(r,k,t) = \frac{\partial f(r,k,t)}{\partial t} \bigg|_{coll}
\]  

(4.1)
Where, \( f(r,k,t) \) is the one-particle distribution function, \( E(K) \) is the energy of the particle, \( F \) is the force acting on it, and \( \hbar \) is the reduced Planck’s constant.

Traditionally, most device simulation methods are based on the BTE or its simplified forms such as the Hydrodynamic transport equations or the Drift-Diffusion, which are derived from the moments of the BTE [21]. A full solution to BTE is either very complicated in terms of computational resources or impossible in some cases. The easiest exact solution of BTE is to use statistical Monte Carlo methods, which track carrier trajectories in real and momentum space as a function of time and energy. However, the Monte-Carlo methods are very demanding and have statistical noise, which make it unsuitable for the linearity analysis considered in this thesis.

DESSIS allows for arbitrary combinations of transport equations and physical models, which allows for the possibility to simulate all spectrums of semiconductor devices. The carrier transport models used in my simulation includes: Drift-Diffusion model, Hydrodynamic model and Thermodynamic model, which will be described below.

**Drift-diffusion:**

The drift-diffusion model is widely used for the simulation of carrier transport in semiconductors. It can be derived from the BTE by taking zero moment of the distribution function and assuming complete thermal equilibrium. In drift-diffusion formalism, the basic semiconductor equations include the Poisson equation and carrier continuity equations, where the current results from either drift or diffusion processes.

The Poisson equation is:
\[ \nabla \epsilon \cdot \nabla \Psi = -q(p - n + N_{D^+} - N_{A^-}) \] (4.2)

where \( \epsilon \) is the electrical permittivity, \( q \) is the elementary electronic charge, \( n \) and \( p \) are the electron and hole densities, and \( N_{D^+} \) is the number of ionized donors, and \( N_{A^-} \) is the number of ionized acceptors.

The electron and hole continuity equations are:

\[ \nabla \cdot \overline{J_n} = qR + q \frac{\partial n}{\partial t} \] (4.3)

\[ -\nabla \cdot \overline{J_p} = qR + q \frac{\partial p}{\partial t} \] (4.4)

where \( R \) is the net electron–hole recombination rate. \( \overline{J_n} \) is the electron current density, and \( \overline{J_p} \) is the hole current density.

It is suitable for low power density devices with long active regions [7]. The collision (scattering) time is assumed to be constant independent of energy, which gives this method both its strength (speed) and weaknesses (accuracy: lack of detailed physics).

**Hydrodynamic:**

With continued scaling into the deep submicron regime, neither internal nor external characteristics of state of-the-art semiconductor devices can be described properly using the conventional drift-diffusion transport model. In particular, the drift-diffusion approach cannot reproduce velocity overshoot and often overestimates the impact ionization generation rates. Although the Monte Carlo method for the solution of the BTE is more accurate, because of its high computational requirements, it cannot be used for
the routine simulation of devices in an industrial setting. In this case, the hydrodynamic model provides a very good compromise. It accounts for energy transport of the carriers and is suitable for devices with small active regions [7].

**Thermodynamic:**

The thermodynamic model extends the drift-diffusion approach to account for electro-thermal effects. It couples thermal diffusion equations to drift-diffusion equations described above. It is suitable for devices with low thermal exchange, particularly, high-power density devices with long active regions. In my simulation, it is used to account for self-heating effect in SOI devices [7].

**4.2.2 Quantization Model**

Quantization effects, which account for the quantum mechanical considerations in devices, are also employed in our simulations. Due to the ever shrinking feature size of CMOS devices, some features of current MOSFET (oxide thickness, channel width) have reached quantum mechanical length scales. Therefore, the wave nature of electrons and holes can no longer be neglected, which make simulation based purely on classical BTE not appropriate. In this case, quantization model in the transverse direction is used to account for threshold voltage and carrier density shifts in the actual solution, while the lateral transport is still treated with classical BTE formalism, resulting in semi-classical approach convenient for large-scale simulations. The type of the quantization model implemented in ISE TCAD package is the Density Gradient model, which gives a reasonable description of terminal characteristics and charge distribution inside a device in the presence of QM quantization [7]. Quantum tunneling effects, both vertically and
laterally, are not considered in this model. Although the absence of tunneling in our simulations is a drawback, this is strictly true for devices less than 10nm, which are too small for RF devices considered in this work.

### 4.3 Simulation Frame

A typical design flow involves creation of a device structure by process simulation (DIOUS) followed by remeshing using MDRAW (for 2D studies). In this scheme, control of mesh refinement is handled automatically through the file _mdr.cmd. Alternatively, MDRAW may be used to build the device structures and to create a suitable mesh. DESSIS is used to simulate the device electrical characteristics.

Such a seamless flow through ISE tools, with the associated file types, is represented in the figure 4.4. INSPECT is used to plot the electrical characteristics. The output from above simulation is fed into the MATLAB program (explained in the next section) and the IP3 values are calculated. Then, with the help of graphic software, IP3 values are plotted against the desired parameters.

An example of the input file is given in appendix A. The File block specifies the input and output files necessary to perform the simulation. The names are specified if they are created by MDRAW or DESSIS. The Electrode block defines all the electrodes to be used in the DESSIS simulation, with their respective boundary conditions and initial biases. The Physics block allows selection of the physical models to be applied in the
device simulation. The Plot block specifies all of the solution variables that are saved in the output plot files.

![Diagram of design flows with DESSIS device simulation]

The Math block defines the settings for the numerical solver. DESSIS solves the device equations self-consistently on the discrete mesh in an iterative fashion. For each iteration, an error is calculated and DESSIS attempts to converge on a solution that has an acceptably small error. And finally the Solve block defines a sequence of solutions to be obtained by the solver.

Figure 4.4 Typical design flows with DESSIS device simulation.
4.4 MATLAB Data Processing

The MATLAB code (Appendix B) is used to calculate the IP3 values, which gives a direct measure of the linearity. The output from the simulation process, i.e., the $I_D$-$V_G$ data sets, serve as the input to the MATLAB program. In order to increase the number of points, simulated data is first interpolated, and then a higher order (usually an 8-order or 9-order) polynomial is fitted data points to reduce unwanted numerical noise. This conditioned data is then differentiated three times to obtain $g_{m1}$, $g_{m2}$ and $g_{m3}$, which refer to first, second and third differentials of the drain current with respect to gate voltage. First and third derivatives are then used to calculate the IP3 value using Equation (3.7) or (3.8). All important variables are plotted out for visual inspection at the end of this code.
Chapter 5. Results and Discussions

5.1 Device Structures Simulated

Bulk MOSFET, single gate SOI MOSFET and double gate SOI MOSFET structures are designed and simulated in this thesis work. General features of the devices and other structural information are outlined in Fig. 5.1. These structures are representative of well-scaled depletion-mode analog devices at 50nm, with 1.5nm gate oxide and highly-doped thin body channels designed to optimize linearity at the expense of maximum transconductance achievable, as suggested with previous works on Si/SiGe MODFETs.

![Diagram of device structures (a-c) and technology parameters used in our simulations. Bulk doping ($N_d=10^{19}$ cm$^{-3}$) and oxide thickness ($t_{ox}=1.5$ nm) has been chosen to minimize short channel effects and comply with ITRS requirements. Sidewall spacing is 100nm in all simulations unless otherwise noted.](image)

### Device Parameters

- $N_d=10^{19}$ cm$^{-3}$
- $L_g=60$ nm
- $x_{jd}(b)=30$ nm
- $x_{jd}(c)=40$ nm
- $N_d=10^{20}$ cm$^{-3}$
- $L_{eff}=50$ nm
- $x_{jd}(b)=15$ nm
- $x_{jd}(c)=30$ nm
- $t_{ox}=1.5$ nm
- $d_L=10$ nm
- $t_{gd}(b)=30$ nm
- $t_{box}=100$ nm
- $t_{sa}(a)=10$ nm
Both devices have identical gate stacks and substrates to allow a meaningful comparison in our simulation study. DESSIS allows us to include different transport models in the simulation such as drift-diffusion (DD) and hydrodynamic (HD) approximations. In addition, first-order quantum mechanical (QM) corrections, self-heating effect (SHE) and impact ionization (II) can also be included.

The silicon body thickness of DG MOSFET is 10nm, while the silicon body thickness of bulk and SOI MOSFET are 30nm. The reason to choose different body thickness is that DG MOSFET inherently has thinner body thickness than single gate MOSFET, which is one of the advantages for DG MOSFET with better scaling potential.

5.2 Impact of Device Physics on MOSFET Linearity

5.2.1 Output Conductance Considerations

As mentioned above, output conductance, $g_d$, as well as device junction capacitances can impact device linearity, because these parameters are dependent on applied voltages. So at first, I will investigate the impact of output conductance for device linearity.

The drain voltage dependence of $g_d$ is first studied. In Fig 5.2, I plot drain bias dependence of $g_d$ for the three device architectures in question at a gate overdrive of 1V. I find that $g_d$ reduces more rapidly in SOI and DG MOSFET, which have a thinner active Si layer, hence a lower output conductance. For $V_d>0.5V$, $g_d$ remains relatively flat in SOI MOSFET, while DG and bulk MOSFET have comparable response, except lower value of $g_d$ in the former case. At typical operation conditions, i.e. saturated operation for
Fig.5.2 Drain-bias dependence of $g_d$ is typically low in saturation but non-zero. As device body becomes thinner $g_d$ drops.

MOSFET, my simulations predict weak voltage dependence for $g_d$. This in turn would result in lower distortion associated with output conductance. In addition, similar results (not shown) are obtained also for junction capacitances, which are minimal in SOI devices due to fully-depleted operation and compact source/drain geometry.

To demonstrate the negligible impact of output conductance, I have compared in Fig 5.3 $P_{IP3}$ values calculated using expressions (3.7) and (3.8), assuming a load resistance of 50Ω. Indeed, for DG MOSFET device, I find no output conductance contribution to nonlinearity at all. Similar results obtained also for SOI MOSFET. However, it is important to note that the dominant term in the second term in (3.8) is $G_L$. If a larger load resistance than present value is chosen, the importance of the $g_{d2}$ term may be larger, as demonstrated recently by Kang et al. [5]
5.2.2 Non-equilibrium Transport Effects

How can we identify the contribution of various transport phenomena in the channel to device linearity? Since experimentally it is hard to separate out different transport mechanisms, and simulations based on compact models do not have sufficient handle on device physics, TCAD simulations provide a unique platform to relate device physics to linearity. More accurate Monte-Carlo simulations are not practical in linearity simulations because of large fluctuations associated with this technique.

In an attempt to discover the impact of actual device physics on the linearity performance, I simulated DG and SOI MOSFET (V_d=1.0V) at different degrees of transport complexity. By using ISE-DESSIS, I applied density gradient corrections to drift-diffusion or hydrodynamic transport equations. This allows first-order quantum mechanical (QM) corrections to be included in our simulations. Hydrodynamic equations are required to incorporate non-stationary effects, which play a central role in device performance via velocity overshoot. Fig 5.4-Fig 5.7 show the linearity performance (P_{IP3} figure) of SOI and DG MOSFET obtained using various degree of sophistication in transport models. For both SOI and DG devices at all current levels, I found that QM transport model increases the linearity slightly, while inclusion of non-stationary effects via hydrodynamic model reduces it. Traditional DD transport model, most common for device simulation, overestimates the linearity about 4dBm in SOI MOSFET and 8dBm in DG MOSFET.
I show in Fig.5.4 & Fig.5.5 the linearity of MOSFET simulated using different transport formalisms at maximum trans-conductance bias conditions, where gain is maximized. I again observe that the non-equilibrium effects, included in HD but not DD model, lower device linearity.
In other words, DD simulations overestimate linearity by as much as 6dBm at large drain bias conditions where non-equilibrium effects are strongest. Moreover, the inclusion of impact ionization (II) in HD simulations reveals that this effect does not play a significant role in linearity evaluation. Finally, bulk-Si control device with an identical architecture as SOI MOSFET, but without the BOX layer, has similar linearity performance, indicating that linearity advantage of basic MOSFET architecture over bipolar devices is preserved in the novel device configurations in question.

Quantum mechanical effects in MOSFET increase the threshold, which is equivalent to decrease device current. This is interesting to note because smaller currents are generally associated with lower linearity, as evident from Fig.5.6&Fig.5.7. Thus our observation concerning the influence of QM effects on linearity is also counter-intuitive. However, it is important to note that QM effects *dynamically* changes the channel density as the gate voltage is raised, which causes steeper confining potentials and raises the bound state energies further. I believe that super-linear dependence of gate voltage on electron current in MOSFET approaches closer to ideal line due to quantum effects, hence improving the overall linearity. This is to say that the quantum mechanical gate-channel charge coupling mechanism is more linear than classically assumed.

### 5.2.3 Self-Heating Effects

Because of the low thermal conductivity of the buried oxide, SOI and DG MOSFET performance is influenced by the heat dissipation within the active device layers
including primary channel, parasitic conduction paths and series S/D resistances. Typically self-heating effects (SHE) reduces available drain current and also may introduce further distortion at the output due to kink-effect, reduced but not completely eliminated in the fully-depleted SOI MOSFET such as those used in this work.

We combine both electrical and thermal effects self-consistently in our simulations, by imposing thermal boundary conditions at the bottom of the substrate and the top of the front gate for each device. Thermal contacts used in the simulations, fixed at the room temperature (300K), are assigned small lumped resistances to account for the full-scale geometry including the substrate and the device package. Also the simulated device domain is extended out sufficiently (~5 m) to allow heat distributions to relax appropriately.

**Fig.5.8** $I_d - V_g$ characteristics with or without self heating effect (SHE). Note that SHE reduces the current at large bias conditions as expected.

**Fig.5.9** Corresponding trans-conductance curves for the same devices ($g_m$) obtained at 2GHz using AC simulations with SHE, and fitted with high-order (>7th) polynomials.
Fig. 5.10 Temperature distribution in SOI MOSFET at $V_G=1.5V$ and $V_D=1.0V$.

Fig. 5.11 Temperature distribution in DG MOSFET at $V_G=1.5V$ and $V_D=1.0V$.

Fig. 5.8 & Fig. 5.9 show the electrical-thermal simulation of DG MOSFET, single gate SOI MOSFET and bulk MOSFET. We observe that the drain current (Fig. 5.8) is reduced due to SHE, as expected. In addition, under equal thermal boundary conditions, DG MOSFET heats about 20K higher than SOI counterpart and the drain current of both devices decrease at high drain bias (Fig. 5.10 & Fig. 5.11) due to SHE. Consequently, the linearity of DG and SOI MOSFET are slightly comprised when the drain voltage is raised above 1V as can be seen in Fig. 5.4 & Fig. 5.5. The impact of SHE on linearity is similar in magnitude ($\leq 2$dBm) in both devices, even though the temperature rise is larger in the DG case. Thus it can be concluded that SHE does not seriously degrade linearity, especially in the DG architecture. Note that SHE degradation may grow in poorly designed fully-depleted structures due to increasing temperature [23], and likely to be suppressed at high frequencies as a result of high-pass heating response of the SOI substrate [24].
To investigate the influence of ambient temperature on linearity, I have altered the thermal contact (ambient) temperature between 250 and 325 K, which corresponds to extreme climate conditions where devices may operate, as seen in Fig. 5.12. Surprisingly, the increase in ambient temperature improves linearity slightly, up to 2dBm. Although this seems to be counter-intuitive, it may be understood if I consider that change in boundary conditions (heating/cooling) have an overall impact on device performance which does not occur in the case of SHE. SHE impacts device temperature mainly locally (around the channel), while top-gate and substrate thermal contacts change the overall heat distribution as well as series parasitic resistances strongly. Increasing temperature also changes junction leakage considerably, which is shown to increase linearity despite the loss of gate control in the transistor as a whole. It is noted that the vertical shifts in the linearity curves of DG and SOI MOSFET, when drain voltage is changed from 1.0V to 2.0V is consistent with Fig.5.4&Fig.5.5.

Fig.5.12  Linearity of DG and SOI MOSFET slightly improve at higher ambient temperatures. Note also that DG is more linear at large drain biases.
5.3 Scaling Effects Impact of MOSFET Linearity

5.3.1 Gate Length Scaling

Generally, gate length scaling of MOSFET improves the performance and speed of integrated circuits as well as lowers their manufacturing cost and power consumption per switching event. The microelectronics industry has been scaling down transistors for the past 30 years to meet demand for smaller and more capable electronic devices. In this section, I will study the impact of gate length scaling on device linearity performance.

![Graph showing linearity performance of DG and SOI MOSFET as a function of gate length.](image)

Fig. 5.13 Linearity performance of DG and SOI MOSFET as a function of gate length. The linearity decreases as the gate length is reduced. The increase at very short gate lengths is an artifact of high leakage due to excessive short channel effects in SOI device.

To compare the linearity performance of novel SOI and DG MOSFET, the effective gate length of devices is laterally scaled from 100nm down to 20nm, while keeping all other
parameters same. For reliable simulations, I employ HD transport model to account for non-equilibrium carrier dynamics and density gradient approximation for quantum mechanical effects. Impact ionization of channel carriers and SHE are also included in the simulation of thin-body devices considered in this study. I find that the linearity performance of DG MOSFET degrades gradually as the gate length is reduced Fig.5.13. At high drain bias ($V_d=2V$), the degradation is about 4dBm, while at low drain bias, the reduction is approximately 2dBm. The advantage of high drain bias is compromised under 30nm gate length, which implies that the linearity of DG MOSFET can be kept relatively stable at low power dissipation. In other words, in extremely short gate (<30nm) DG MOSFET, appreciable RF linearity performance can be achieved at a considerably lower power dissipation. For SOI device, the decreasing trend in linearity is similar to that in DG MOSFET above 50nm. The increase in linearity at gate lengths below 50 nm is believed to be an artifact of excessive short channel effects in SOI device and is not realistic due to poor transistor switching characteristics in this regime. Because of the dual gates, which have a stronger control over the channel, DG MOSFET is immune from this deviation. The reduction in linearity with gate scaling is previously reported also for bulk Si-MOSFET [3] and Si/SiGe MODFETs [22] down to 50nm. Here, I confirm this trend also for SOI and DG architectures and extend it down to 30nm. Intuitively, the reduction in linearity with gate scaling may be attributed to increase in electrostatic coupling between channel, source and drain depletion regions and highly complex charge control mechanism in the short channel devices.

In Fig.5.13, it is clear that DG MOSFET has higher linearity than SOI counterpart at longer gate lengths (>50nm) and at high drain bias ($V_d=2V$), while it has lower linearity
at low drain bias ($V_d=1\text{V}$). Under the gate length of 50nm, considering both linearity and device scalability, DG MOSFET is still a good candidate for a nano-scale RF MOSFET with a sufficient linearity and low power consumption.

### 5.3.2 Silicon Body Thickness Scaling

Scaling silicon film thickness is desirable for better short channel behavior and reduced floating body effect [25]. Therefore, it is useful to investigate the impact of silicon body thickness on device linearity performance, which is the topic of this section.

![Linearity performance of DG and SOI MOSFET as a function of thin silicon body thickness on SOI substrates. DG linearity is more susceptible to body thickness changes than the SOI counterpart.](image)

While silicon body thickness is a crucial parameter to optimize digital performance in fully depleted SOI MOSFET, its importance is even greater in DG MOSFET due to the dependence of threshold, carrier density and mobility to this parameter in this device
To test its impact on RF linearity perspective, the silicon body thickness is vertically scaled from 30nm down to 3nm for SOI and DG MOSFET with a gate length 50nm and 100nm, while other device parameters remain unchanged (Fig. 5.14). At 100nm gate length, SOI MOSFET linearity first increases slightly (~1dB), than sharply decreases as body thickness is reduced. For DG MOSFET, linearity decreases steadily down to 10nm body thickness before it falls rapidly. Linearity drops almost 3dBm in both devices when body thickness scaled below 10nm. In 50nm gate-length devices, the same degradation trend is repeated again, though reductions are slightly less due to smaller overall linearity. By switching off thermal models in the simulation, I observe that this trend is not generated by SHE. Indeed, although self-heating effect can slightly reduce linearity at thick body thickness, its impact disappears when body thickness shrinks under 10nm. I believe that quantum mechanical shift in $V_T$ and reduction in channel density as a result of smaller Si channel thickness is responsible for the drop in linearity.

### 5.3.3 Sidewall Scaling

Series resistance is another important factor affecting the performance of MOSFET below 100nm. MOSFET operation is very sensitive to the variation of sidewall thickness [27] due to changes in series resistance.
Fig. 5.15 Comparison of linearity in DG and SOI MOSFET identical in all aspects except the sidewall spacer dimensions and body thickness. The series resistance associated with extension regions plays a more significant role in DG MOSFET linearity, with thinner spacers resulting in higher linearity.

To investigate the impact of sidewall thickness on device linearity, I simulated devices with sidewall thickness of 20nm, 40nm, and 80nm (Fig. 5.15). For SOI MOSFET, the linearity can be improved slightly (1dBm) for large drain biases if sidewall thickness is increased from 20nm to 80nm. For DG MOSFET, such a scaling results in approximately 3dBm decrease in linearity if $V_d \geq 1V$. The drop in linearity is even more significant (~5dBm) at lower drain biases. Thus the sidewall thickness scaling produces opposite trends in the linearity of SOI and DG MOSFET. A similar scaling study on Si/SiGe MODFETs by Yang et al. [22] indicate that an increase in the separation between S/D contacts and gate is helpful for device linearity, which is in agreement with our SOI results. Accordingly, it may be inferred that linearity in single-gate devices benefit from increasing series resistance effects due to thick sidewall spacers, while DG MOSFET
linearity does not. However, it is important to note that DG-MOSFET has thinner body than SOI device in these simulations; hence the differences may be attributed partly to unequal body thickness in two devices.
Chapter 6. Conclusions and Future Work

In my thesis work, the RF linearity performance of sub-100nm gate length SOI and DG MOSFET are investigated and compared with traditional bulk MOSFET. The impact of device physics and device scaling for MOSFET linearity are investigated.

In the first part, I have outlined the relationship between various aspects of device physics and linearity. I showed that linearity performance is particularly sensitive to non-local effects and is not seriously degraded with SHE, at least in the fully-depleted SOI devices. Quantum mechanical effects appear to have a small positive impact on linearity and impact ionization does not affect device linearity appreciably. DD simulations are found to be particularly unreliable for linearity analysis of DG MOSFET due to large overestimation from this model.

<table>
<thead>
<tr>
<th>Device Physics Phenomenon</th>
<th>Impact on $P_{IP3}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Non Equilibrium Effects</td>
<td>Large, (−)</td>
</tr>
<tr>
<td>Self-Heating Effects</td>
<td>Small, (−)</td>
</tr>
<tr>
<td>Quantum Mechanical a)</td>
<td>Small, (+)</td>
</tr>
<tr>
<td>Impact Ionization</td>
<td>Small, (−)</td>
</tr>
<tr>
<td>Downscaling (gate)</td>
<td>Medium, (−)</td>
</tr>
<tr>
<td>Downscaling (body)</td>
<td>Medium, (−)</td>
</tr>
<tr>
<td>DIBL / Junction Leakage</td>
<td>Large (+)</td>
</tr>
</tbody>
</table>

a) I refer here to impact of small shifts in carrier density peak in the channel. Note that strong quantization effects actually reduce linearity and quantum tunneling effects leading to excess leakage are not considered in the present QM (density gradient) model.
Finally, I summarize in Table 6.1, as a general guide, all of our current observations concerning the relationship between device physics and linearity. These observations reflect the general trends in SOI based MOSFET and may be subjected to change in other devices depending on the details of device geometry and operation. Using simulations, I explain the interplay between different physical mechanisms and RF linearity in a rigorous manner and present a full comparison of linearity performance of 50 nm SOI and DG MOSFET.

In the second part, I have investigated RF linearity performance of novel SOI and DG MOSFET as a function of important geometrical parameters such as gate length, silicon body thickness scaling and sidewall thickness. I observed that the linearity is compromised gradually as gate length is scaled down. Similarly the down scaling of body thickness has a negative impact on linearity for both devices. I clarified that these observations are not related to self-heating effects. Moreover, I also show that the linearity performance of DG MOSFET is more sensitive to the series resistance associated with gate spacers due to its thinner silicon body thickness.

In conclusion, my thesis work explains the interplay between RF linearity with different physical mechanisms and device scaling in a rigorous manner and presents a full comparison of linearity performance of sub-50nm SOI and DG MOSFET.
The future work of this thesis can be directed in two directions. First of all, this work is the first attempt to investigate linearity performance of single and double-gate SOI MOSFET. As mentioned before, linearity has a strong interaction with other RF figure of merits such as cutoff frequency $f_t$, noise and intrinsic gain $g_m/g_d$. The trade-off study between linearity and other RF figure of merits will be a valuable extension topic. Secondly, by using the 2D process simulator DIOS or the new 3D process simulator FLOOP available in the new version of ISE TCAD, we could study the impact of process variation for SOI device linearity to give a guide for high linearity SOI device fabrication.
References


[12] For more information on SOI technology, visit

http://www-lpm2c.grenoble.cnrs.fr/nanosciences/CIRP/cristoloveanu.pdf,


Appendix:

A. Simulation Input Command File Example

#-----------------------------------------------
# Simulation command file for Double-Gate MOSFET
#
#-----------------------------------------------

Electrode{
   { Name="Source" Voltage=0.0 }
   { Name="Drain" Voltage=0.0 }
   { Name="GateTop" Voltage=0 Barrier=-0.55 }
   { Name="GateBot" Voltage=0 Barrier=-0.55 }
}

File{
   Grid = "dg_body10_mdr.grd"
   Doping = "dg_body10_mdr.dat"

   Current = "dg_body10_undop_sym_EDLvg2vd1_mdr.plt"
   Plot = "dg_body10_undop_sym_EDLvg2vd1_des.dat"
   Param = "dessis.par"
}

Physics {
   Hydrodynamic( eTemperature )
   Mobility( PhuMob
      eHighFieldSaturation( CarrierTempDrive )
      hHighFieldSaturation( GradQuasiFermi )
      Enormal
   )
   EffectiveIntrinsicDensity( OldSlotboom )
   Recombination( SRH(DopingDep) )
   eQuantumPotential
}

Plot{
   *--Density and Currents, etc
   eDensity hDensity
   eCurrent hCurrent
   eMobility hMobility
   eVelocity hVelocity
   eQuasiFermi hQuasiFermi

   *--Fields and charges
   ElectricField Potential SpaceCharge
   eQuantumPotential
}
*--Doping Profiles
  Doping DonorConcentration AcceptorConcentration

*--Generation/Recombination
  SRH Auger
  AvalancheGeneration eAvalancheGeneration hAvalancheGeneration

*--Driving forces
  eGradQuasiFermi/Vector hGradQuasiFermi/Vector
  eEparallel hEparallel
}

Math{
  Extrapolate
  Digits = 5
  Notdamped=50
  Iterations=20
  NewDiscretization
  Derivatives
  AvalDerivatives
  RelErrControl
  ErrRef(Electron) = 1.0E10
  ErrRef(Hole) = 1.0E10
  DirectCurrent
}

Solve{
  Poisson
  Coupled{ Poisson eQuantumPotential }
  Coupled{ Poisson eQuantumPotential eTemperature }

  #-ramp gate
  Quasistationary(
    InitialStep=0.01 Increment=1.2
    Minstep=0.0001 MaxStep=0.1 DoZero
    Goal{ Name="GateTop" Voltage= 2}
    Goal{ Name="GateBot" Voltage= 2}
  )
  Coupled{ Poisson Electron Hole eQuantumPotential eTemperature}
}

  #- ramp drain
  Quasistationary(
    InitialStep=0.01 Increment=1.2
    Minstep=0.0001 MaxStep=0.1
    Goal{ Name="Drain" Voltage= 1.0 }
  )
  Coupled{ Poisson Electron Hole eQuantumPotential eTemperature}
}
B. MATLAB Code to Calculate IP3

```matlab
%% % A Matlab Program for calculation of IP3 from Id-Vg data
% clear
format short e
nth=7; % Order of polynomial fitting
vgstep=0.005;
vgfinestep=0.002;
new_data=[];

Rsd=50; % load resistance
Vdc=1.1;
peakscale=0.6;

disp('This is a Matlab program');
disp('to calculate gm from Id-Vg data');
file=input('filename for data (without any .<txt> extension) ? ','s');

datafile=[file '.txt'];
eval(['load ' datafile ' -ascii']);
data=eval(file);

%======Editing data to delete the edge points by setting a threshold
max_value=max(abs(data(:,2)))
threshold=0.0001*max_value
len=length(data(:,2));
j=1;
for i=1:len
    if data(i,2)>threshold
        new_data(j,:)=data(i,:);
        j=j+1;
    end
end

length(new_data(:,2))
data=new_data;

%======Reorder of the data from samll to large
vg=data(:,[1]);
vgmin=vg(1);
```
vgsize=length(vg);
vgmax=vg(vgsize);
if vgmin>vgmax
    dummy=vgmin;
    vgmin=vgmax;
    vgmax=dummy;
end
vg_int=vgmin:vgstep:vgmax;
vgsize=length(vg_int);
id=1e6*data(:,[2]);

%==========Polynominal fitting
id_int=spline(vg,id,vg_int);
[pn sn]=polyfit(vg_int,id_int,nth);
id_int=polyval(pn,vg_int);

%====Set position and name of the MATLAB result window===========
figure
set(gcf,'Position',[300 35 450 500])
set(gcf,'Name', file)

%================================%=%

%=========Draw Id/Vg curve=============
subplot(321)
plot(vg,id,'g')
hold on
plot(vg_int,id_int,'r')
xlabel('Gate Bias (V)')
ylabel('Drain Current (mA/mm)')
grid on
figname=['   ',file, 'nth=7 threshold=0.00005  Jun23' ];
title(figname)

gm(2:vgsize)=diff(id_int)./diff(vg_int);
if vgmin==0e0
    gm(1)=0;
else
    gm(1)=spline(vg_int(2:vgsize),gm(2:vgsize),vgmin);
end

[gmmax vgpeak]=max(abs(gm));
ileft= min( find(abs(gm)>gmmax*peakscale) );
iright= max( find(abs(gm)>gmmax*peakscale) );
ilist=ileft:iright;
% Draw gm/Vg curve
subplot(322)
plot(vg_int,gm,'r')
xlabel('Gate Bias (V)')
ylabel('Transconductance (mS/mm)')
grid on
gmdata=[vg_int' gm'];
gmdatafile=[file '.gm'];
eval(['save ' gmdatafile ' gmdata -ascii']);
string=['Saved gm data into ' file '.gm'];

dgm(2:vgsize)=diff(gm)./diff(vg_int);
if vgmin==0e0
    dgm(1)=0;
else
    dgm(1)=spline(vg_int(2:vgsize),dgm(2:vgsize),vgmin);
end

% Dran first order derivative of gm/Vg
subplot(323)
plot(vg_int(ilist),dgm(ilist))
xlabel('Gate Bias (V)')
ylabel('$\partial g_m/\partial V_g$')

ddgm(2:vgsize)=diff(dgm)./diff(vg_int);
if vgmin==0e0
    ddgm(1)=0;
else
    ddgm(1)=spline(vg_int(2:vgsize),ddgm(2:vgsize),vgmin);
end

% Dran second order derivative of gm/Vg
subplot(324)
plot(vg_int(ilist),ddgm(ilist))
xlabel('Gate Bias (V)')
ylabel('$\partial^2 g_m/\partial V_g^2$')

ddgmdata=[vg_int' ddgm'];
ddgmdatafile=[file '.ddgm'];

eval(['save ' ddgmdatafile ' ddgmdata -ascii']);
string=['Saved ddgm/dVg2 data into ' file '.ddgm'];
disp(string);
disp('bye');
vgsize=length(vg_int);

%=====Formula for calculating IP3=========
IP3=10*log10(gm(ilist)*4./(ddgm(ilist)*Rsd));

%=====Draw IP3 versus Id=========
subplot(325)
plot(id_int(ilist),IP3)
xlabel('Drain Current (mA/mm)')
ylabel('IP3 (dBm)')
grid on

%===== Calculation of LFOM
pin=(id_int.*vg_int);
Pdc=Vdc.*id_int(ilist);
LFOM=IP3./Pdc;

%===== Draw LFOM======
subplot(326)
plot(id_int(ilist),LFOM)
xlabel('Drain Current (mA/mm)')
ylabel('LFOM')
grid on

%=====Save IP3 data=====
IP3data=[id_int(ilist)' IP3'];
IP3datafile=['file '.ip3'];
eval(['save ' IP3datafile ' IP3data  -ascii']);
string=['Saved IP3 data into ' file '.ip3'];

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% To get the exact drain current at maximum transconductance

value=[vg_int,id_int,gm'];
order_maxgm=find(gm==max(gm))
value_vg=vg_int(1,order_maxgm)
value_id=id_int(1,order_maxgm)
ew_id=id_int(ilist);
for i=1:size(new_id,2)
    if new_id(1,i)==value_id
        m=i;
    end
end
IP3_maxgm=IP3(1,m)
C. Publications Based & Related to This Work

JOURNAL PUBLICATIONS


CONFERENCE PROCEEDING & PRESENTATIONS


CONFERENCE PAPERS UNDER REVIEW:
