LOW TEMPERATURE CO-FIRED CERAMIC (LTCC) SUBSTRATE FOR HIGH TEMPERATURE MICROELECTRONICS

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LOW TEMPERATURE CO-FIRED CERAMIC (LTCC) SUBSTRATE
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ABSTRACT

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Advances in aerospace technologies demand new ways to package electronics for high temperature and harsh environments. One packaging method of interest in academia and industry is Low Temperature Co-fired Ceramic (LTCC). LTCC is a multi-layer design and packaging system that can embed passive components and thermal management structures within a substrate. This thesis compiles research done to evaluate LTCC as a high-performance electronic packaging technique by determining the performance of embedded passives and thermal management structures at temperatures from -55°C to 225°C. The passive structures and thermal management structures are evaluated using theoretical calculations, simulations, and measurements of fabricated devices.
For my family and for fiancé, soon to be my wife
ACKNOWLEDGMENTS

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Packaging is an important issue to allow microelectronic systems to function under harsh environments such as high temperature, high shock, and vibration. In fact, the cost of packaging could be as high as 50 - 95% of the overall system cost. As a result, many industries and academic research groups are actively researching new methods to create environmentally robust electronics. One of these electronic packaging methods for harsh environments is with using the Low-Temperature Co-Fired Ceramic (LTCC) packaging system.

1.1 Background and Motivation

Printed Circuit Boards (PCBs) with embedded passives (EP) and thermal management capabilities are highly desirable features in the electronic packaging for extreme environments. By freeing surface area on a PCB from passive devices such as resistors and capacitors a larger amount of space for computing devices, such as Integrated Circuits (ICs) and memory is available. As a result, both the overall PCB size can be reduced and computing power on a single PCB can be increased.

As the size of PCBs decrease and component density increases, electronic devices have strayed away from Moore’s law, pictured as Figure 1.1, due to the limitations of the laws
of thermodynamics. For example, the transistors in an Intel Core™ i7-6900K generates 91 watts of power [5]. If thermal management structures, such as heat sinks, are not used to direct heat away from the PCB, it could result in catastrophic failure due to overheating.

Both civilian and military aviation are safety-critical applications. In military aviation, the failure of any avionics component in overheating could result in severe loss of life, property, and endanger national security. For military aircraft, there is a strong desire to minimize weight, improve reliability and reduce maintenance costs. Thus, the use of elaborate heat sinks and active cooling techniques are not practically feasible. As such, it has become desirable in to embed the thermal management structures inside of a PCB. Embedding thermal management structures inside a PCB not helps to save valuable space but also provides an efficient way of dissipating heat generated by active computational and interface devices.
Current electronic packaging techniques encase integrated chips (ICs) with an epoxy package and use wire-bonding to connect IC outputs to the package’s output pins. This is not always sufficient; exterior environmental hazards such as heat or precipitation can severely damage an IC. In order to protect sensitive electronics, researchers have looked into ways of hermetically sealing these devices to isolate them from potential hazards.

One solution is to use Low Temperature Co-Fired Ceramic (LTCC) packaging method. LTCC packaging techniques uses stacked layers of a ceramic dielectric material to create printed circuit boards with embedded passives (such as thick-film resistors and capacitors), embedded heat-sinks, and hermetic-sealing using Kovar\textsuperscript{TM} lids.

### 1.1.1 LTCC Characteristics

The LTCC packaging method shares many common features that are typically implemented on standard epoxy based PCBs. But LTCC based packaging provides some unique additional advantages including operating over a wide temperature range, high frequency (100 GHz), and high voltage (2000 V)[6][7]. There are multiple LTCC systems available on the market today, amongst these Ferro A6, DuPont 9K7, and DuPont 951 are the most common. While the dielectric layers in each of these design systems belong to the LTCC family of materials, each material has unique physical properties that make them more or less desirable for certain applications. Table 1.1 lists some common LTCC materials and some of their properties.

The low loss and relatively high dielectric constant of the LTCC materials make them desirable for high frequency applications, especially the DuPont 9k7 material, which has been shown to perform up to 100 GHz[6]. Furthermore, LTCC (in general) has a lower thermal expansion coefficient and higher flexural strength, indicating that LTCC is more rugged than FR-4 or RO4350B.
Table 1.1: Various Materials and Some Relevant Properties

<table>
<thead>
<tr>
<th>Material</th>
<th>$\varepsilon_r$</th>
<th>Loss Tangent (10 GHz)</th>
<th>Coefficient of Thermal Expansion (ppm/K)</th>
<th>Thermal Conductivity (W/mK)</th>
<th>Flexural Strength (MPa)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DuPont 951</td>
<td>7.8</td>
<td>0.0140</td>
<td>5.8</td>
<td>3.3</td>
<td>320</td>
</tr>
<tr>
<td>DuPont 9K7</td>
<td>7.1</td>
<td>0.0010</td>
<td>4.4</td>
<td>4.6</td>
<td>230</td>
</tr>
<tr>
<td>Ferro A6M</td>
<td>5.9</td>
<td>0.0008</td>
<td>8</td>
<td>2</td>
<td>170</td>
</tr>
<tr>
<td>Generic FR-4</td>
<td>4.5</td>
<td>0.008</td>
<td>15</td>
<td>.3</td>
<td>80</td>
</tr>
<tr>
<td>Rogers RO4350B</td>
<td>3.66</td>
<td>.0037</td>
<td>32</td>
<td>.69</td>
<td>255</td>
</tr>
</tbody>
</table>

[6],[7],[8],[9],[10]

1.2 Overview and History of Printed Circuit Boards

The development of printed circuit boards (PCBs) underwent a massive transformation from an experimental circuit fabrication technique to a fully-functioning and widely available technology since it was introduced in the 1940s [11]. During the $2^{nd}$ World War, the PCB saw its greatest development for the proximity fuze. The proximity fuze was an allied innovation that used sensors to determine its proximity from a target. The fuze would initiate the detonation of a sortie once it was less than a certain, pre-determined distance from said target[12]. While there were a variety of sensors that could be used to make this determination, all of them needed an electronic circuit that was resilient enough to be fired as a part of a munition, but also be simple enough to be produced in mass quantity. A solution was proposed by C. Brunetti of Centralab following the war in 1948[11]. The fabrication technique that Brunetti proposed was to print silver traces and punch through-holes in a thin ceramic plate. Through-hole components would then be soldered to the board to complete the fabrication process[11].
There have been enormous developments in technology starting from Brunetti’s ceramic PCB to the PCBs of today. Today, most PCBs are multi-layer, with as many as 40 stacked layers, boards designed for through-hole and surface-mount devices. Ceramic is no longer the material of choice in PCBs as woven fiberglass and phenolic paper (FR-4 and FR-2, respectively) have become the substrate material of choice in today’s market. Many extreme environment and high temperature applications use PCBs made with polyimide, woven glass reinforced with hydrocarbon/ceramics, Polytetrafluoroethylene (PTFE) composites reinforced with glass microfibers, and woven fiberglass reinforced, ceramic filled composite materials. Amongst the materials that are commonly accepted by industry are PTFE, for high frequency applications; Alumina, a high dielectric material that is particularly useful for printing antennas; and LTCC a ceramic material that is suitable for high-temperature, harsh environment, and high frequency applications[6].

1.3 Overview and History of Multi-Layer Design systems

The LTCC packaging methodology is a multi-layer circuit design and packaging system. Multi-layer ceramic systems have a long history beginning in the 1960s when H.W. Stetson demonstrated a fabrication method for creating multi-layer circuits using stacked ceramic dielectric sheets [13]. The fabrication method proposed by Stetson is briefly described below, 1. Cut holes for vias and traces in each dielectric sheet; 2. Fill the via and trace holes with a metallic paste; 3. Stack these sheets; 4. Fire them at a temperature that sinters the stack of dielectric together, forming a single, monolithic substrate[13]. While Stetson did not insist on a single type of ceramic dielectric sheet, he would propose a fabrication method that would continue to be used decades later for the fabrication of LTCC substrates [13].
The LTCC system follows the same fundamental concepts that Stetson demonstrated in the 1960s. An LTCC substrate is fabricated by: blanking and drying each of the ceramic dielectric sheets, punching vias and cavities in every sheet, filling all vias and printing all passives and conductors, stacking and laminating the layers, and firing of the substrate. Unlike Stetson’s system, however, passives and other structures are able to be printed on and cut out of each layer of LTCC before firing, allowing components to be embedded within the substrate. This allows components to be removed from the surface of the PCB, freeing valuable surface-area and decreasing the thermal density on the surface of the chip.

1.4 Thermal Management

Thermal management is a major concern that has always plagued high performance electronic systems. Electronic components, both active and passive, dissipate power in the form of heat. The closer together electronic components are, the denser the power dissipation, meaning more heat in a small area[14]. Traditional solutions to this problem have been to spread components out over a larger area and to add larger, more intricate heat-sinks[14]. Researchers are looking into new ways of dissipating heat that do not take up more space. Amongst these methods are micro-fluidic liquid cooling and embedded thermal management structures [15]. Micro-fluidic liquid cooling takes a similar approach to liquid cooled PC towers but on a much smaller scale. However effective this method may be, it is both complicated and expensive.

Embedded thermal management structures follows the same principle as traditional heat-sinks; using a material with a high thermal conductivity and putting it adjacent to a heat-dissipating device effectively changes the surface area that the device dissipates heat
from. By doing this, the heat is carried away from the device, keeping it cooler than it would have been had no thermal management structures been used.

In addition to being able to incorporate embedded thermal management structures into designs, LTCC also has the ability to hermetically seal its components using Kovar\textsuperscript{TM} frames and lids. Kovar\textsuperscript{TM} is a metal alloy that has a similar thermal coefficient of expansion as the LTCC ceramic layers [12]. The lid is brazed on an LTCC substrate in an ultra-low pressure environment in order to ensure the components are sealed in a vacuum. As a result of the vacuum, the Kovar\textsuperscript{TM} frame and lid not only protect sensitive electronics from external conditions, but also help keep electronic components cooler by shielding them from ambient heat.
Current demands in the aerospace industry seek to find new high temperature electronic packaging methods. As of today, that vast majority of ‘harsh environment electronics’ are only designed to operate between 40°C and 125 °C [16]. There is a frantic effort by industry to develop new high performance micro-electronics and packaging techniques that enable aerospace electronics to function over a wide temperature range from -55°C and 225 °C. Specifically for packaging aspects, there are two methods that are seeing a significant research interest: epoxy and polymer laminates reinforced with glass microfibers or composite materials and ceramic materials.

Epoxy- and polymer-based packaging has been the micro-electronic packaging technique of choice for decades since it is both a low-cost and easy to fabricate. While it may be a time-proven solution for micro-electronic packaging it has major short-falls when subjected to high temperatures. Two of the most prevalent shortfalls include the swelling and hydration of the epoxy material. Overall, these shortfalls make epoxy based micro-electronic packaging unreliable for high-temperature applications.
Ceramic-based packaging, as seen in Chapter 1 dates back to the very first printed and multilayer circuits. With the need for inexpensive, mass-produced PCBs, ceramic materials were marginalized to niche markets such as mm-wave and high frequency applications. However, interest in ceramic packaging techniques, particularly LTCC, has been resurrected as a result of the aerospace industry’s demand for high temperature electronic packaging.

The remainder of this section will provide comparative analysis of both of these packaging techniques, detailing both their strengths and their weaknesses. First, micro-electronic thermal management techniques will described in detail. Next, recent relevant research pertaining to epoxy-based micro-electronic packaging will be conferred. After this, relevant ceramic packaging research will be discussed. Following this, research pertaining to LTCC based packaging will be presented. Finally, a problem statement for this thesis will be given.

2.1 Micro-electronic Thermal Management Techniques

The reliability of high temperature packaging is reliant on the effectiveness of thermal management structures. The most common thermal management technique is the heatsink. A heatsink is a large piece of metal or other thermally conductive material that is placed in contact with active components. Heat dissipated from an active component is transferred into the heat sink and dissipated into air. While this approach is in many cases an effective thermal management technique, it presents several problems. First, although a heatsink transports heat away from an active component, it can also store heat if the active component dissipates into the heatsink faster than the heat sink can dissipate into air. This can result in the heatsink becoming hotter than the chip, meaning it no longer transports thermal energy away from the chip but instead dissipates heat into the chip. Second,
the best functioning heatsinks are generally large structures as larger surface area means more area to dissipate heat. While a larger heat sink may be superior to smaller ones for thermal management, it adds size and weight to electronics making them an impractical for aerospace electronics. As a result, researchers are scrambling to find new, lightweight thermal management techniques to incorporate into high performance electronic packages.

Amongst the emerging thermal management techniques are thermal vias. Thermal vias are an interesting solution to the problem presented by heat sinks. Thermal vias work by creating thermally conductive channels for the heat dissipated by active components to travel through. Using heat spreaders (planar metallization layers), heat carried away from an active component is then dissipated out of the back of a device [17]. Thermal via efficiency can be improved by increasing the density of thermal vias in a given area; more thermal vias means creating an overall lower parallel thermal resistance. Zampino [17] tested the efficiency of various thermal via sizes using numerous LTCC systems. The effectiveness of thermal vias was tested using arrays of embedded thermal vias with diameters ranging between 100 and 1200 µm. Using this setup, several conclusions were made: 1. high-density thermal via arrays provide a low resistance path for heat dissipation, 2. an array taking up of 20% of the total device area is a sufficient thermal management structure for most ICs, and 3. thermal spreading can be improved by intermediate metallization layers. In addition to these conclusions, a notable discovery was made: the thermal conductivity of the metal pastes from the design system differed from datasheet values by as much as a factor of 3 (in the case of the Ferro material) [17] [18].

N. Liu et al. [19] pursued an interesting micro-fluidic approach to thermal management. This approach couples thermal vias with micro channels in order to improve the thermal management on an LTCC chip. This approach uses thermal vias to direct the heat generated
by an active source into several liquid-filled channels. As heated liquid metal or water flows out of the substrate through an outlet, it is replaced with cool material flowing in through an inlet. A model of this system was created and simulated using COMSOL Multiphysics. The result of this experiment showed the substrate temperature could be maintained within a tolerable range using a high flow rate of either material through the micro-channels.

Another thermal management technique that is used in micro-electronic packaging is the thermally enhanced ball grid array (TEBGA) researched by Qi et al. [20]. A TEBGA package is a standard plastic ball-grid array (PBGA) that is covered with a thermally conductive heat spreader. The heat spreader is then connected to a heat sink for optimal heat dissipation. Heat is transported away from an IC (which is attached to the heat spreader using a thermally conductive adhesive) by dissipating heat directly into the heat spreader and out through the heat sink. This thermal management technique has been demonstrated to be an effective means for heat dissipation, by using forced convection.

Y.A. Elkady et al. [21] demonstrated an interesting approach to thermal management in PBGA packaging. PBGA packages consist of an IC mounted to a molded plastic case and wire-bonded to brazed outputs, which have a solder ’ball’ on their ends to simplify surface mounting. A general diagram for a BGA is pictured as Figure 2.1. After a BGA package is mounted to the surface of a PCB, the air gap between the BGA and PCB is filled with an underfill material. Since the solder balls and brazed outputs are conductive metals they provide a low-resistance path for heat to travel through (Elkady coined the term ’thermal balls’ to describe this structure). This research found thermal balls soldered to thermal vias can be a highly effective thermal management technique. This structure coupled with underfill material encourages increased thermal transportation away from the
PBGA package. Thermal resistances of as low as $18.08 \frac{K}{W}$ were able to be demonstrated by combining of thermal vias, thermal balls, and under-filling.

Another attempt to improve the thermal and electrical characteristics of BGA packaging is the super ball grid array package (SBGA). The SBGA is essentially an improved TEBGA that capitalizes on the successes with using both the heat spreaders and under-filling. The research presented by Pyland [23] showed that this particular BGA, when is used in conjunction with a low coefficient of thermal expansion (CTE) underfill, the stress on solder joints decreased and the overall life of the SBGA increased.

2.2 Epoxy Based Packaging Techniques

Early attempts for electronic packaging methods were often unreliable, leaving ICs exposed to the external environment as attempts to find ways to hermetically seal chips were either expensive or unable to maintain the required MIL883 standards for hermeticity and those that were[24]. As such, there was interest to develop simple, yet effective, plastic-based, or epoxy-based, electronic packaging techniques. These techniques, such as Quad Flat Packs (QFPs), Plastic Leaded Chip Carriers (PLCCs), and PBGAs, were exceptionally reliable, resistant to shock and vibration, and avoided many of the failures of other
packaging techniques, and as a result nearly 80% of IC packages in the late 1990s used epoxy-based packaging [24].

The low-cost and simple nature of PBGAs, has allowed it to become today’s most popular epoxy-based micro-electronic packaging technique. J. Liu [25] points out a number of advantages that has led them to become so popular including: simple assembly, a low manufacturing cost, small package size, low noise, and fast manufacturing time. In addition to these advantages, Liu also points out numerous issues including: cracked and broken joints resulting from solder fatigue, difficult board routing, larger package height (in comparison to other epoxy-based packaging techniques), hydration or absorbing moisture, and package warpage. Amongst the most concerning of these issues are cracked and weakened solder joints and hydration; weakened solder joints reduces package life and greatly diminishes reliability. Hydration can result in a package swelling or exploding due to absorbed water freezing after being subjected to extreme cold (a major problem for aerospace applications). While the plastic enclosures of PBGAs have comparable thermal conductivities to ceramic ball grid arrays (CBGAs), they have a higher significantly higher CTE, making them susceptible to expansion and warpage when exposed to high temperatures [26] [25]. As the IC placed inside the PBGA is fabricated using silicon (a low CTE material), the difference in expansion rates between the IC and the plastic package can cause large amounts of strain on solder joints reducing the life of a PBGA [25] [27]. Further soldering can be a problem for PBGAs as solder re-flow can cause package warpage, cracking, and delamination.

Due to the issues PBGA packages encounter at high temperatures, researchers have sought out methods to improve the thermal performance of PBGAs. As can be seen in section 2.1, Qi showed much success reducing the overall thermal resistance of a PBGA package through the development of thermally enhanced ball grid arrays (TEBGA). While
Qi was able to demonstrate improved thermal performance of TEBGAs over standard PBGAs, the TEBGA still experienced some major, familiar shortcomings. As seen in Qi’s [20] simulations, an increase in temperature can be detrimental if the thermal expansion coefficient and thermal conductivity of the heat spreader does not match the rest of the package. Specifically, as the temperature of the chip increases, the inability to match the TCE and thermal conductivity of the epoxy enclosure to that of the heat spreader results in the deformation of the enclosure and breakage of solder joints. The SPGAs explored by Pyland [23] also encounter these problems if the cumulative CTE of the package is not matched with that of the board it is mounted on. In general, the findings of both Qi and Pyland [20] [23] show that a failure to match the cumulative CTE of the plastic enclosure with that of a heat spreader, PCB, or underfill means they expand at different rates, putting stress on the solder joints, plastic enclosure, and PCB. Such phenomenon increases the required maintenance costs and seriously effects the reliability of circuits that use PBGA.

Elkady [21] shows that the PBGAs continued to experience similar problems even when using advanced thermal management structures such as thermal balls and thermal vias. Subjecting thermal vias and thermal balls to heating and cooling cycles results in an overall increased thermal resistance as a result of cracks and complete failure of thermal management systems. Further, this research showed that the system itself has been associated with increased failure at high temperature; increasing the number of elements in a thermal ball array (TBA) has been shown to reduce packaging life by up to 33%.

Using simulations and physical tests, Haiyu [28] helped to confirm that even with enhanced thermal management structures PBGAs are unreliable for avionics. In automobiles PBGAs had a failure rate of 63% and had less than half the lifetime of components packaged using ceramic-based packages and other epoxy-based leaded packages (QFPs and
PLCCs). Under simulated flight conditions PBGAs were shown to last only 5.3 years of the needed 10 year lifetime. The conclusion that Haiyu reached from the simulations is that non-underfilled PBGAs could not satisfy the needed life time for aerospace electronics.

All the prior research described above shows that using epoxy-based packaging techniques can be unreliable at high temperatures. As a result, it is necessary to consider different packaging techniques to find one that has good performance at high temperature. One of these techniques, talked about in section 2.3 below, is ceramic based packaging techniques.

2.3 Ceramic Based Packaging Techniques

There are two fundamental approaches to ceramic-based packaging for aerospace electronics. The first approach is surface-mount packaging techniques such as ceramic ball grid array (CBGA) technology. Nearly identical to PBGAs, CBGAs use a ceramic enclosure rather than an epoxy enclosure. In order to be used for applications such as engine control, CBGAs (like PBGAs) need to be mounted on the surface of a PCB along passive and active surface mount devices (SMDs). While the use of ceramic materials eliminates some of the problems associated with PBGAs, such as hydration and swelling of the material due to a high CTE, it does not solve all of the problems associated with BGA devices. The repeated exposure to heating and cooling cycles result in weakened solder joints and increased stress on components even in a CBGA[29]. As a results, a device that uses a CBGA mounted on a PCB will require maintenance to repair solder joints and replace components, resulting in higher overall higher costs and lower reliability. Additionally, another disadvantage of this system is adding components, such as passive (resistors, capacitors, etc) and active components (Amplifiers, switches, etc.) adds extra weight and bulk to a PCB.
An alternative approach to traditional ceramic packaging techniques such as CPGAs are embedded passive systems. Embedded passive are fabricated by depositing material on individual layers of a multi-layer ceramic system. There are two primary types of embedded passives: screen-printed passives and thin-film passives. While both of these types of passives offer many of the same benefits in comparison with SMDs, they have properties which give them an edge for certain applications. Screen-printed passives often have a low tolerance [7][30], resulting in deformation of the elements during the firing step in LTCC fabrication. Though this problem can be fixed using laser-shaping, the equipment required to do so is rather time consuming, which is not ideal for large-scale manufacturing. Furthermore, screen-printed resistors have a high thermal coefficient of resistance (TCR) which limits their operational temperature range. Though thin-film passives avoid the issues associated with screen-printed components by having a lower TCR and higher level of precision, they have their own problems such as a limited range of capacitance and resistance in comparison with thick-film screen-printed passives.

Regardless of the type of embedded passive used, embedded passive packaging systems have myriad of advantages when compared to traditional electronic packaging techniques and PCBs. In NASA’s overview of embedded passives [31], R. D. Gerke lists several of the benefits that make embedded-passive ceramic systems ideal for aerospace electronics. The first of these advantages is an increased density of active components; reducing the number of passive components (resistors and capacitors) on the surface of a chip results in more space for active components. Furthermore, since over 70% of components on a single-board computer (such as an engine controller) are resistors and capacitors [31] replacing surface-mount passives with embedded-passives can significantly reduces the weight of the device and potentially turn a double-sided device into a single-sided device. Not only
can embedded passives reduce weight and increase the density of active components, but also improve the device electrical performance by reducing the length of signal paths and line inductance. Additionally, the use of embedded passives also increases the overall reliability of a device by eliminating solder joints that ultimately reduce the cost of a device by decreasing maintenance and increasing board yield.

Gerke [31] also points out that the use of embedded passives also have several disadvantages. High materials cost, slow design period and a reduced design flexibility, and a high risk factor are all disadvantages associated with embedded passives. While the disadvantages listed above likely disqualify this technology from use in low-cost consumer electronics, the pros of embedded passives outweigh the cons especially for the development of advanced automotive and aerospace electronics.

2.3.1 LTCC Fabrication System

While there are a number of ceramic packaging techniques, the LowTemperature Co-fired Ceramic (LTCC) circuit design and packaging system offers several unique properties that make it an interesting substitute to traditional micro-electronic packaging techniques. The LTCC system avoids many of the problems that historically have been associated with High Temperature Co-fired Ceramics (HTCC), such as high firing temperatures, [32][33] while retaining many of its desired properties. Many of LTCC’s properties are explored by M. T. Sebastian et al. [34]. Sebastian et al. point out that interest in LTCC technology has grown significantly in the past decade-and-a-half, with approximately 1000 papers and 500 patents being filed for LTCC related applications. The LTCC design system uses multiple, ceramic tape stacked on top of each other to create a substrate that is useful for 3-dimensional printed circuits. Passive, screen-printed components can be embedded within the multiple layers, ultimately, saving surface space. While there are many varieties of
glass-ceramic composite LTCCs on the market, they all share various characteristics. One of these is that they will have a stable relative permittivity (\(\varepsilon_r\)) between 3 and 10 (though some can have much higher \(\varepsilon_r\)) and low batch-to-batch variation (unlike common substrate materials such as FR-4). Additionally, LTCC has a low sintering temperature making it more suitable for micro-electronic packaging than other ceramic packaging techniques such as HTCC. Specifically, the low sintering temperature means the LTCC system can use highly conductive metals such as Silver (Ag) and Gold (Au) can be used to fabricate transmission lines [32]. The combination of a stable relative permittivity and low sintering temperature means LTCC provides a stable, reliable, and desirable platform for not only micro-electronics but also microwave electronics.

One disadvantage, that was pointed out by both M. Zampino and M.T. Sebsatian [34] [17] is that LTCC has a low thermal conductivity of between 3-4 W/m-K. While still higher than organic laminate technology (FR-4), it is still an order of magnitude lower than that of Alumina (30W/m-K), another high frequency dielectric material. As a result, LTCC substrates require thermal management structures such as heat sinks. Unlike other high frequency substrates, LTCC has a low thermal coefficient of expansion, increasing the reliability of an LTCC chip and giving it an edge over materials such as alumina.

Kulke [32] compiled a comprehensive report comparing LTCC to high-performance epoxy-based packaging techniques. This report points out that epoxy based packaging techniques are often less expensive and can be used to make larger circuits than LTCC. On the other-hand, LTCC permits for greater integration due to embedded passives and the ability to create hermetically sealed cavities. The hermetically sealed cavities in conjunction with a significantly lower TCE, as opposed to materials like Polytetrafluoroethylene
PTFE) which have a TCE similar to many common metals, make them a robust system suitable for harsh environments.

2.4 Problem Statement

There are a number of unique features that make ceramic packaging systems ideal for high temperature micro-electronic packaging. LTCC ceramic systems have a number of characteristics that make them a particularly interesting micro-electronics packaging technique for aerospace electronic systems. Due to the high temperatures that aerospace electronics may encounter, it is of interest to look at the performance of the LTCC fabrication system, particularly its passive components and thermal vias structures, at high temperatures. This thesis compiles research done to evaluate LTCC as a high-performance electronic packaging technique by determining the performance of embedded passives and thermal management structures at temperatures reaching 225°C.
As mentioned in chapter II, there are a number of features that make LTCC a desirable material for a wide variety of applications. Amongst these features are embedded thermal vias and embedded screen-printed resistors and capacitors. This chapter will provide documentation of the theoretical calculations and simulations used to evaluate each of these structures for high temperature operation. All simulations and calculations are performed using the Ferro A6M LTCC design system.

3.1 Screen Printed Resistors

Several resistive materials are simulated in order to evaluate the performance of Ferro A6M LTCC screen-printed resistors (SPRs) over a wide temperature range from \(-55^\circ C\) to \(225^\circ C\). This system uses several differently doped versions of RuO$_2$. The resistive materials that can be used in the Ferro A6M system include FX87-011, FX87-101, FX87-102, and FX87-103. Each material has a different thermal coefficient of resistance (TCR), resistivity, and short term overload voltage. These values are shown in table 3.1.

Amongst the most relevant material properties for evaluating the performance of a resistor at high temperature is TCR. This value indicates the change in the resistance value of
### Table 3.1: Ferro Thick Film Resistive Materials

<table>
<thead>
<tr>
<th></th>
<th>Resistivity (Ohms/Sq.)</th>
<th>Tolerance</th>
<th>TCR (ppm/°C)</th>
<th>Short Term Overload Voltage (V/mm$^2$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>FX87-101</td>
<td>100</td>
<td>+/- 30%</td>
<td>+/-450</td>
<td>22</td>
</tr>
<tr>
<td>FX87-102</td>
<td>1000</td>
<td>+/- 30%</td>
<td>+/-200</td>
<td>54</td>
</tr>
<tr>
<td>FX87-103</td>
<td>10000</td>
<td>+/- 30%</td>
<td>+/-200</td>
<td>60</td>
</tr>
</tbody>
</table>

The resistor with respect to temperature. The expected room temperature value of a resistor is calculated using Equation (3.1).

$$R(T_0) = \rho \frac{W}{L}$$  \hspace{1cm} (3.1)

where $\rho$ is the resistivity of the material in $\Omega/\square$, $W$ is the width of the resistor, and $L$ is the Length of the resistor. The room temperature value for resistance is used to calculate the temperature dependent value of resistance using Equation (3.2).

$$R(T) = R(T_0)[1 + TCR_1(T - T_0) + TCR_2(T - T_0)^2]$$  \hspace{1cm} (3.2)

where $TCR_1$ is the first thermal coefficient of resistance and $TCR_2$ is the second thermal coefficient of resistance. It is worth noting that the $TCR_2$ for any of the materials in table 3.1 was not available in literature, and as such the resistance with respect to temperature is calculated with just the $TCR_1$. This should not be of any particular concern as $TCR_2$ has a very small or secondary effect on this relationship.
Equations 3.1 and 3.2 are implemented in MATLAB in order to calculate the values of R(T) from $-55^\circ C$ to $225^\circ C$. The resulting values are plotted against temperature. Figure 3.1 shows the relationship between temperature and resistance for the materials listed in table 3.1.
3.2 Screen Printed Capacitors

One of the most useful features of the LTCC system are screen-printed capacitors (SPCs). A simple parallel-plate capacitor is simulated in order to evaluate its operational integrity in high temperature applications. The capacitance of a parallel-plate capacitor is calculated with Equation (3.3).

\[ C = \frac{\epsilon A}{d} \]  

(3.3)

where A is the area of the conductor and d is the thickness of the dielectric. While this equation shows the simplicity of a theoretical parallel-plate capacitor, it does not take a material’s thermal expansion or Thermal Coefficient of Capacitance (TCC) into account. Increases in temperature can result in both the conductive and dielectric layers of a parallel plate capacitor to expand. Changes in the volume of conductive and dielectric layers can cause changes in the capacitance due to change in area and dielectric thickness. A capacitor’s TCC is a useful metric for gauging how capacitance changes with respect to temperature. The value of TCC for the Ferro A6M SPCs could not be found in literature and, therefore, could not be incorporated into the simulations.

COMSOL is used to evaluate Ferro A6M SPC behavior from 25°C to 225°C in order to evaluate the effects of TCE on capacitance. Two parallel-plate capacitors, each using Ferro A6M material for the dielectric material and either silver or gold for the conductor, are created for this purpose. The general model for these capacitors is pictured as figure 3.2. A voltage potential is applied to one plate of the capacitor while the other plate is grounded. A parametric sweep is performed by varying the temperature of the capacitor by +25°C. It is worth noting that these simulations are all performed by assuming uniform temperature distribution throughout an entire capacitor. The simulated capacitance values
are collected and plotted against temperature. The relationship between capacitance and temperature both the Ag and Au SPCs are plotted in Figure 3.3.
3.3 Thermal Vias

The ability to embed a thermal management structure in an LTCC substrate is a promising feature for its use for high temperature micro-electronic packaging. Through-substrate vias, or thermal vias, are able to be organized into massive arrays which decrease the cumulative thermal conductivity of a given area and should, in theory, direct heat away from active components on the LTCC substrate surface. Figure 3.4 is a generic image illustrating a basic thermal via.

While it would be ideal to place a monolithic block of thermally conductive material underneath an active device, such a design practice is prohibited by LTCC fabrication facilities as it breaks many design rules. Specifically, a large monolithic block would cause serious warpage of the chip, likely causing fracture of the LTCC substrate itself. Therefore, in order to fabricate a thermal via array, several common rules must be followed including 1) Pitch, or the distance from via-center to via-center must be 2x via diameter 2) thermal
vias must be spaced at least 150 µm from one another. 3) Thermal vias must have the same diameter of all other vias in the design. 4) 10 µm thick metal layers must be placed above and below the thermal vias. All of these rules are followed when designing the thermal via arrays so that the simulations are accurate.

To study the ability of thermal vias to transport heat, several parametric studies are performed. The first parametric study uses COMSOL Multiphysics to look at thermal via array performance with variation of via diameter and via material. There are six primary vias that were tested in this simulation: Silver conductor 100 µm diameter, Silver conductor 150 µm diameter, Silver conductor 250 µm diameter, Gold conductor 100 µm diameter, Gold conductor 150 µm diameter, and Gold conductor 250 µm diameter.

The first set of simulations uses 4-via arrays to evaluate the performance of the thermal vias. A general diagram of the 4-via arrays is pictured as Figure 3.5.

One important property for determining how effective a material is at dissipating heat is thermal resistance. Thermal resistance is calculated using Equation (3.4).
where $R_\theta$ is the thermal resistance through the length of a material in $\frac{K}{W}$, $l$ is the length of the material in $m$, $A$ is the cross-sectional area of the material orthogonal to the path of thermal transportation in $m^2$, and $k$ is the thermal conductivity of the material in $\frac{W}{m^2}$. Within thermal via arrays, thermal vias are parallel to the substrate. As such, the overall thermal resistance of the via arrays is evaluated as Equation (3.5)

$$R_\theta, total = \frac{R_\theta, via + R_\theta, substrate}{R_\theta, via + R_\theta, substrate}$$

Using Equations (3.4) and (3.5), the expected thermal resistance of each via type is calculated in MATLAB. The resulting values for thermal resistance are pictured in Table 3.2. The length, $l$ for all values in Table 3.2 was calculated using the sintered substrate height of 778 $\mu m$. All of these calculations are performed assuming that all vias in the
4-via array have parallel thermal resistances with each other as well as with the Ferro A6M substrate.

The thermal resistance behavior pictured in Table 3.2 is verified using COMSOL simulation by looking at the change in temperature through the thermal vias. In addition to verifying the thermal resistance behavior, the simulation varies the height of the substrate and thermal vias by an order of 2, in order to see how the change in temperature through the via varies with respect to a change in length, $l$. Figure 3.4 plots the simulated relationship between $l$ and the change in temperature due to thermal resistance $T_R$.

Another worthwhile way of studying the behavior of thermal vias is to look at the performance of larger via arrays. Using Equations (3.4) and (3.5) the theoretical values of thermal resistance for via arrays of varying size are calculated. These calculations are performed using the assumption that all vias have parallel thermal resistances. The calculated values of thermal resistance for each via array is tabulated and presented as table 3.3.

Mass Via Arrays (MVA) is a practical approach to incorporate thermal vias into thermal management structures. An MVA is a distributed array that maximizes the amount of vias.
Figure 3.6: Change in Temperature Through the Substrate as a Function of Varying Substrate Height; Silver-Only Array (top) Gold-only (bottom)

Table 3.3: Expected Values of Thermal Resistance and Conductivity as a function of Increased Number of Vias

<table>
<thead>
<tr>
<th></th>
<th>$R_{\theta, \text{sub.}}$</th>
<th>$R_{\theta, \text{tot.}}$</th>
<th>$R_{\theta, \text{tot.}}$</th>
<th>$R_{\theta, \text{tot.}}$</th>
<th>$R_{\theta, \text{tot.}}$</th>
<th>$R_{\theta, \text{tot.}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>(m²/W)</td>
<td>(m²/W)</td>
<td>(m²/W)</td>
<td>(m²/W)</td>
<td>(m²/W)</td>
<td>(m²/W)</td>
</tr>
<tr>
<td>Au-100</td>
<td>217.8786</td>
<td>108.9393</td>
<td>54.4696</td>
<td>27.2348</td>
<td>13.6174</td>
<td>6.8087</td>
</tr>
<tr>
<td>Au-150</td>
<td>140.5781</td>
<td>70.2890</td>
<td>35.1445</td>
<td>17.5723</td>
<td>8.7861</td>
<td>4.3931</td>
</tr>
<tr>
<td>Au-250</td>
<td>65.8347</td>
<td>32.9173</td>
<td>16.4587</td>
<td>8.2293</td>
<td>4.1147</td>
<td>2.0573</td>
</tr>
<tr>
<td>Ag-100</td>
<td>78.9529</td>
<td>39.4764</td>
<td>19.7382</td>
<td>9.8691</td>
<td>4.9346</td>
<td>2.4673</td>
</tr>
<tr>
<td>Ag-150</td>
<td>39.5497</td>
<td>19.7748</td>
<td>9.8874</td>
<td>4.9437</td>
<td>2.4719</td>
<td>1.2359</td>
</tr>
<tr>
<td>Ag-250</td>
<td>15.2288</td>
<td>7.6144</td>
<td>3.8072</td>
<td>1.9036</td>
<td>0.9518</td>
<td>0.4759</td>
</tr>
</tbody>
</table>
Table 3.4: Simulated MVA Properties and $\Delta T$

<table>
<thead>
<tr>
<th></th>
<th>Via Diameter ($\mu$m)</th>
<th>Via Spacing ($\mu$m)</th>
<th>Via Pitch ($\mu$m)</th>
<th>Via Distance to Edge ($\mu$m)</th>
<th>Number of Vias ($\mu$m)</th>
<th>$T_R$ ($^\circ C$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Au</td>
<td>100</td>
<td>150</td>
<td>250</td>
<td>75</td>
<td>576</td>
<td>3.335</td>
</tr>
<tr>
<td>Au</td>
<td>150</td>
<td>150</td>
<td>300</td>
<td>175</td>
<td>400</td>
<td>0.701</td>
</tr>
<tr>
<td>Au</td>
<td>250</td>
<td>250</td>
<td>500</td>
<td>125</td>
<td>144</td>
<td>2.498</td>
</tr>
<tr>
<td>Ag</td>
<td>100</td>
<td>150</td>
<td>250</td>
<td>75</td>
<td>576</td>
<td>1.130</td>
</tr>
<tr>
<td>Ag</td>
<td>150</td>
<td>150</td>
<td>300</td>
<td>75</td>
<td>400</td>
<td>0.540</td>
</tr>
<tr>
<td>Ag</td>
<td>250</td>
<td>250</td>
<td>500</td>
<td>125</td>
<td>144</td>
<td>1.044</td>
</tr>
</tbody>
</table>

that are placed over a fixed area (while obeying the rules listed on Page 23). This structure is placed directly beneath an active component to dissipate heat.

Ideally an MVA would span the entire surface area of a chip, however, this would severely interfere with the ability to route electrical connections. As such, an MVA should be confined to an area that is equal to or slightly greater than the footprint of the active device in order to maximize heat dissipation. While a variety of sizes could have been used for the MVA, a 6mm x 6mm area is chosen for each simulation, equal to the die size of most micro-controllers. A total of 6 different 6mm x 6mm MVAs are studied in this simulation. Figures 3.7 through 3.9 are the final components for MVAs with each via size. Each MVA was simulated with a 1.8W source on its top boundary. The properties and $T_R$ of each MVA are tabulated in Table 3.3.
Figure 3.7: 100 $\mu$m

Figure 3.8: 150 $\mu$m

Figure 3.9: 250 $\mu$m
CHAPTER IV

LTCC CHIP FABRICATION AND TESTING

This chapter describes the LTCC chip layout, including design considerations, fabrication, and testing. In order to conduct physical testing of LTCC embedded structures, a chip with a variety of resistors, capacitors, and via test-structures is fabricated. The chip is fabricated using 6-layers of Ferro A6M dielectric tape. All conductors (traces, pads, and thermal vias) use an Ag/Au mixed metal system. The screen printed resistors are made using FX87-101, a Ruthenium Oxide (RuO$_2$) thick film.

4.1 Layout Considerations and Fabrication

The pre-processing (punching and sintering) of the LTCC chip is performed by ACAMP in Edmonton, Alberta, Canada. All the final assemblies were performed at the University of Dayton. To design a chip that can be pre-processed using ACAMP facilities, a standard set of rules for processing need to be followed, amongst the most pertinent when designing test structures were, 1) via pitch must be 2x via diameter 2) only one via size can be used for all vias (thermal or electrical interconnect) 3) vias need to be either $100\mu m$, $150\mu m$, $250\mu m$, or $500\mu m$ 4) vias cannot be located in solder pads 5) solid metallization layers can be no greater than 10mm x 10mm in order to be fabricated 6) there can be no dimensions smaller than 100 $\mu m$ 7) resistor minimum dimensions are $750\mu m$. 

32
Two different types of resistors are used in the layout: small area (550 µm x 550 µm) and large area (1000 µm x 1000 µm) SPRs. Two different resistor sizes are used in order to evaluate the performance of SPRs with dimensions greater than minimum specifications and with SPRs that have dimensions less than minimum specification. This information is pertinent because if the small SPRs perform as well as large SPRs, they can be used to create denser layouts. In addition to varied sizes, a variety of SPR configurations are tested to determine the effects of increased spacing, resistor stacking, resistor depth (second- or third-layer SPRs), and trace length on resistance.

All capacitors on the chip use an inter-digitated, parallel-plate capacitor design pictured as shown in Figure 4.1. The depth of the conductive layers in the substrate are varied in order to determine if the amount of dielectric surrounding the SPC has an effect on capacitance. While most of these capacitors have two conductive layers, there is also a 6-layer capacitor in the bottom left corner. The ADS Layout of the test structure chip is shown in Figure 4.2.

All SPRs connect several resistors in series in order to achieve higher values and to increase SPR reliability. Ordinarily, the resistance of an SPR is adjusted by changing the length or width of the resistor, however, due to low firing precision (+/-35%), it is difficult to achieve exact resistance values with precise dimensions.

Our designed chip incorporates a 150µm 5.5mm x 5.6mm MVA. The 150µm MVA was chosen as it demonstrated the highest ability to dissipate heat. While a different size MVA was chosen it should still perform very similarly. The only difference from the simulation that could seriously effect performance is that this MVA uses a mixed metal system meaning it has an Au top conductive layer, Ag vias, and an Ag bottom conductive layer.
The fabrication process is as follows: drying and blanking of the LTCC dielectric layers, cutting and punching cavities and via holes, filling vias and printing conductive traces and passive devices, stacking and laminating the prepared dielectric layers, sintering the LTCC chip at 950°C, wirebonding and soldering components, and hermetically sealing a device with a Kovar\textsuperscript{TM} frame and lid [7]. The fabricated chip dimensions after fabrication are 2.54cm x 2.54cm x .0778cm. The chip received by ACAMP is pictured below as Figure 4.2.

As can be seen in Figure 4.2 the MVA on the test structure chip only has one heat spreader layer. As a result a different chip with the 150µm MVA from chapter IV is used for measurements.
4.2 Passive Device Testing

A number of tests are performed in order to validate the simulated and theoretical results for LTCC passive devices. The fundamental goal of these measurements is to establish baseline values for passive device performance from $-55^\circ C$ to $225^\circ C$.

4.2.1 Screen-Printed Resistor Testing

In order to verify the theoretical SPR calculations described in Chapter III and create new baselines a number of tests are performed on the SPR test-structures. As mentioned in section IV there are two primary types of SPRs that are tested, the small-area SPR and the large area SPR. Most of the SPR tests are performed using an LMS-2709 probing station due to the delicate nature of the passive component contacts (as no brazing pins are added at the current stage) and the ability to raise or lower the temperature of the probing station platform. In order to test an SPR using the probing station the LTCC chip is placed in the platform holder and DC probes are placed in an SPR’s terminals. These probes are then connected to a Keithley Multi-meter to get readings for resistance. The multimeter is set to output 2.1V and 1mA to read values for resistance that are less than or equal to 9.999
$K\Omega$. Figure 4.3 shows the placement of the chip on the probing station platform and the placement of the probes on a set of SPR terminals.

The first test is designed to measure resistance values at room temperature. The purpose of this test is to determine if the resistor values agree with theoretical calculations, as well as to establish a baseline for resistor performance. The experimental setup shown in Figure 4.3 is used for these measurements and each measurement is repeated three times to verify the value for resistance. The results of the measurements are tabulated as Table 4.1 below.

The next test is designed to measure the resistance of the SPRs over a range of temperatures. The purpose of this test is to measure the value of resistance as a function of temperature. This test follows the same primary testing procedure as the first test with the exception that the platform does not remain at a constant temperature but is instead swept
Table 4.1: SPR Probe Measurements (*R*_nP Indicates Large-Area SPR; *r*_nP Indicates Small-Area SPR)

<table>
<thead>
<tr>
<th></th>
<th>Expected Value (Ω)</th>
<th>Chip 1 Value (Ω)</th>
<th>Chip 2 Value (Ω)</th>
<th>Chip 3 Value (Ω)</th>
<th>Average Value (Ω)</th>
<th>% Deviation (<em>R</em>_A / <em>R</em>_E)</th>
</tr>
</thead>
<tbody>
<tr>
<td>R1</td>
<td>200</td>
<td>204.9</td>
<td>197.3</td>
<td>238.7</td>
<td>213.6</td>
<td>6.8</td>
</tr>
<tr>
<td>R2</td>
<td>200</td>
<td>514</td>
<td>380</td>
<td>395.8</td>
<td>429.93</td>
<td>215.0</td>
</tr>
<tr>
<td>R3</td>
<td>100</td>
<td>261.8</td>
<td>161.4</td>
<td>177.0</td>
<td>200.1</td>
<td>0.03</td>
</tr>
<tr>
<td>R4</td>
<td>400</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>R5</td>
<td>200</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>R6</td>
<td>200</td>
<td>254.0</td>
<td>247.4</td>
<td>248.1</td>
<td>249.3</td>
<td>24.9</td>
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<tr>
<td>R7</td>
<td>100</td>
<td>94.2</td>
<td>86</td>
<td>70.6</td>
<td>83.1</td>
<td>16.47</td>
</tr>
<tr>
<td>r1</td>
<td>400</td>
<td>337.4</td>
<td>355.7</td>
<td>515.5</td>
<td>402.2</td>
<td>0.55</td>
</tr>
<tr>
<td>r2</td>
<td>400</td>
<td>562</td>
<td>295.2</td>
<td>315.2</td>
<td>390.8</td>
<td>2.30</td>
</tr>
<tr>
<td>r3</td>
<td>400</td>
<td>237.1</td>
<td>244.8</td>
<td>289.1</td>
<td>257.0</td>
<td>35.8</td>
</tr>
<tr>
<td>r4</td>
<td>400</td>
<td>210.8</td>
<td>245.1</td>
<td>288.2</td>
<td>248.03</td>
<td>38.0</td>
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<tr>
<td>r5</td>
<td>400</td>
<td>X</td>
<td>225.2</td>
<td>335.5</td>
<td>280.35</td>
<td>29.9</td>
</tr>
<tr>
<td>r6</td>
<td>400</td>
<td>268.1</td>
<td>238.1</td>
<td>403.6</td>
<td>303.3</td>
<td>24.2</td>
</tr>
<tr>
<td>r7</td>
<td>400</td>
<td>332.4</td>
<td>234.5</td>
<td>649.25</td>
<td>405.4</td>
<td>1.35</td>
</tr>
<tr>
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<td>400</td>
<td>243.2</td>
<td>230.4</td>
<td>358.1</td>
<td>277.2</td>
<td>30.7</td>
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<tr>
<td>r9</td>
<td>400</td>
<td>612.6</td>
<td>463.2</td>
<td>626.8</td>
<td>567.53</td>
<td>41.88</td>
</tr>
<tr>
<td>r10</td>
<td>400</td>
<td>389.9</td>
<td>229.6</td>
<td>585.6</td>
<td>401.7</td>
<td>0.042</td>
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<tr>
<td>r11</td>
<td>400</td>
<td>473.0</td>
<td>174.7</td>
<td>338.9</td>
<td>328.9</td>
<td>17.8</td>
</tr>
</tbody>
</table>
Table 4.2: SPR Temperature Sweep Values for Resistance ($R_n$ Indicates Large-Area SPR; $r_n$ Indicates Small-Area SPR)

<table>
<thead>
<tr>
<th></th>
<th>25 °C (Ω)</th>
<th>40 °C (Ω)</th>
<th>55 °C (Ω)</th>
<th>70 °C (Ω)</th>
<th>85 °C (Ω)</th>
<th>100 °C (Ω)</th>
</tr>
</thead>
<tbody>
<tr>
<td>R1</td>
<td>238.7</td>
<td>229.8</td>
<td>226.4</td>
<td>225.13</td>
<td>222.9</td>
<td>222.1</td>
</tr>
<tr>
<td>R2</td>
<td>395.8</td>
<td>387.4</td>
<td>384.4</td>
<td>382.6</td>
<td>380.1</td>
<td>379.1</td>
</tr>
<tr>
<td>R3</td>
<td>177.0</td>
<td>169.4</td>
<td>166.8</td>
<td>165.9</td>
<td>164.3</td>
<td>163.8</td>
</tr>
<tr>
<td>R6</td>
<td>248.1</td>
<td>245.5</td>
<td>244.7</td>
<td>243.0</td>
<td>241.1</td>
<td>240.2</td>
</tr>
<tr>
<td>R7</td>
<td>94</td>
<td>83.5</td>
<td>83.3</td>
<td>82.3</td>
<td>80.9</td>
<td>80.7</td>
</tr>
<tr>
<td>r1</td>
<td>515.5</td>
<td>493.0</td>
<td>488.4</td>
<td>487.3</td>
<td>482.6</td>
<td>480.8</td>
</tr>
<tr>
<td>r2</td>
<td>315.2</td>
<td>315.2</td>
<td>292.0</td>
<td>389.1</td>
<td>288.2</td>
<td>284.5</td>
</tr>
<tr>
<td>r3</td>
<td>289.1</td>
<td>276.7</td>
<td>274.2</td>
<td>274.3</td>
<td>270.7</td>
<td>269.8</td>
</tr>
<tr>
<td>r4</td>
<td>288.2</td>
<td>274.5</td>
<td>271.7</td>
<td>274.3</td>
<td>270.7</td>
<td>269.8</td>
</tr>
<tr>
<td>r5</td>
<td>335.5</td>
<td>323.3</td>
<td>319.7</td>
<td>319.3</td>
<td>318.0</td>
<td>314.1</td>
</tr>
<tr>
<td>r6</td>
<td>403.6</td>
<td>395.3</td>
<td>387.5</td>
<td>387.3</td>
<td>384.0</td>
<td>381.3</td>
</tr>
<tr>
<td>r7</td>
<td>649.2</td>
<td>640.2</td>
<td>632.6</td>
<td>631.0</td>
<td>627.2</td>
<td>624.3</td>
</tr>
<tr>
<td>r8</td>
<td>358.1</td>
<td>349.1</td>
<td>341.5</td>
<td>341.9</td>
<td>338.8</td>
<td>337.1</td>
</tr>
<tr>
<td>r9</td>
<td>626.8</td>
<td>617.4</td>
<td>608.5</td>
<td>607.7</td>
<td>604.4</td>
<td>600.4</td>
</tr>
<tr>
<td>r10</td>
<td>585.6</td>
<td>574.2</td>
<td>568.1</td>
<td>567.4</td>
<td>561.8</td>
<td>558.8</td>
</tr>
<tr>
<td>r11</td>
<td>338.9</td>
<td>326.7</td>
<td>322.4</td>
<td>323.2</td>
<td>320.2</td>
<td>318.5</td>
</tr>
</tbody>
</table>

between 25°C and 100°C. The resistance of each SPR is measured every 15°C. The measured values are tabulated in Table 4.2, note that R4 and R5 are excluded from the table since they were open-circuits in every measurement of the first test.
Table 4.3: SPR Temperature Sweep Values for Resistance (\(R_n\) Indicates Large-Area SPR; \(r_n\) Indicates Small-Area SPR)

<table>
<thead>
<tr>
<th></th>
<th>(I_0)</th>
<th>(I_1)</th>
<th>(I_2)</th>
<th>(I_3)</th>
<th>(I_4)</th>
<th>(I_5)</th>
<th>(I_6)</th>
<th>(I_6-I_0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>r1</td>
<td>337.4</td>
<td>335.6</td>
<td>338.3</td>
<td>336.9</td>
<td>335.6</td>
<td>335.6</td>
<td>334.8</td>
<td>-2.6</td>
</tr>
<tr>
<td>r2</td>
<td>562.0</td>
<td>558.6</td>
<td>560.9</td>
<td>559.5</td>
<td>558.1</td>
<td>558.1</td>
<td>557.6</td>
<td>-4.4</td>
</tr>
<tr>
<td>r3</td>
<td>237.1</td>
<td>235.9</td>
<td>236.9</td>
<td>235.6</td>
<td>233.9</td>
<td>234.3</td>
<td>233.4</td>
<td>-3.7</td>
</tr>
<tr>
<td>r4</td>
<td>210.8</td>
<td>209.7</td>
<td>211.0</td>
<td>209.5</td>
<td>207.7</td>
<td>208.1</td>
<td>207.3</td>
<td>-3.5</td>
</tr>
<tr>
<td>r6</td>
<td>268.1</td>
<td>265.8</td>
<td>263.8</td>
<td>262.3</td>
<td>260.6</td>
<td>261.1</td>
<td>260.2</td>
<td>-7.9</td>
</tr>
<tr>
<td>r7</td>
<td>332.4</td>
<td>330.2</td>
<td>330.2</td>
<td>327.0</td>
<td>325.3</td>
<td>325.8</td>
<td>325.0</td>
<td>-7.4</td>
</tr>
<tr>
<td>r8</td>
<td>243.2</td>
<td>239.1</td>
<td>241.2</td>
<td>236.4</td>
<td>234.5</td>
<td>235.0</td>
<td>234.2</td>
<td>-9.0</td>
</tr>
<tr>
<td>r9</td>
<td>612.6</td>
<td>611.0</td>
<td>312.5</td>
<td>608.1</td>
<td>606.4</td>
<td>606.7</td>
<td>606.0</td>
<td>-6.6</td>
</tr>
<tr>
<td>r10</td>
<td>389.9</td>
<td>368.7</td>
<td>360.2</td>
<td>356.1</td>
<td>354.5</td>
<td>354.6</td>
<td>353.9</td>
<td>-36.0</td>
</tr>
<tr>
<td>r11</td>
<td>473.0</td>
<td>471.4</td>
<td>472.5</td>
<td>468.4</td>
<td>467.1</td>
<td>467.3</td>
<td>466.5</td>
<td>-6.5</td>
</tr>
<tr>
<td>R1</td>
<td>204.9</td>
<td>209.0</td>
<td>206.4</td>
<td>205.5</td>
<td>204.3</td>
<td>204.5</td>
<td>207.3</td>
<td>-1.2</td>
</tr>
<tr>
<td>R2</td>
<td>514.0</td>
<td>511.0</td>
<td>508.4</td>
<td>507.1</td>
<td>505.5</td>
<td>505.1</td>
<td>504.1</td>
<td>-9.9</td>
</tr>
<tr>
<td>R3</td>
<td>261.8</td>
<td>263.6</td>
<td>261.9</td>
<td>261.2</td>
<td>259.6</td>
<td>260.0</td>
<td>259.2</td>
<td>-2.6</td>
</tr>
<tr>
<td>R6</td>
<td>254.0</td>
<td>253.8</td>
<td>252.1</td>
<td>251.4</td>
<td>250.0</td>
<td>250.2</td>
<td>249.5</td>
<td>-4.5</td>
</tr>
<tr>
<td>R7</td>
<td>94.0</td>
<td>107.2</td>
<td>105.0</td>
<td>104.0</td>
<td>102.5</td>
<td>103.3</td>
<td>102.1</td>
<td>8.1</td>
</tr>
</tbody>
</table>

Another test is performed evaluates the performance of a resistor after iterative heat exposure. The purpose of this test is to evaluate the performance of the SPRs after being exposed to high temperatures for an extended period of time (225°C). This test is performed by placing a chip on a hot plate set to 225°C for 10 minutes, and then measuring the SPRs after a 15 minute cooling period once the chip has cooled to room temperature (25°C) using the setup pictured in Figure 4.3. The resulting values are tabulated as Table 4.3.
Table 4.4: SPR Multimeter Measurements ($R_n$ Indicates Large-Area SPR; $r_n$ Indicates Small-Area SPR)

<table>
<thead>
<tr>
<th></th>
<th>Expected Capacitance Values (nF)</th>
<th>Chip 1 Capacitance Values (nF)</th>
<th>Chip 2 Capacitance Values (nF)</th>
<th>Chip 3 Capacitance Values (nF)</th>
<th>Average Capacitance Values (nF)</th>
<th>% Deviation ($\frac{C_A}{C_E}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>.0021</td>
<td>0.0030</td>
<td>0.0030</td>
<td>0.0031</td>
<td>0.0030</td>
<td>46.7</td>
</tr>
<tr>
<td>C2</td>
<td>.0041</td>
<td>0.0066</td>
<td>0.0066</td>
<td>0.0068</td>
<td>0.0067</td>
<td>61.2</td>
</tr>
<tr>
<td>C3</td>
<td>.0041</td>
<td>0.0064</td>
<td>0.0063</td>
<td>0.0063</td>
<td>0.0063</td>
<td>53.1</td>
</tr>
<tr>
<td>C4</td>
<td>.0041</td>
<td>0.0042</td>
<td>0.0041</td>
<td>0.0043</td>
<td>0.0042</td>
<td>1.5</td>
</tr>
<tr>
<td>C5</td>
<td>.0041</td>
<td>0.0063</td>
<td>0.0064</td>
<td>0.0062</td>
<td>0.0063</td>
<td>52.3</td>
</tr>
<tr>
<td>C6</td>
<td>.0041</td>
<td>0.0046</td>
<td>0.0044</td>
<td>0.0045</td>
<td>0.0045</td>
<td>8.8</td>
</tr>
<tr>
<td>C7</td>
<td>.0331</td>
<td>0.0286</td>
<td>0.0289</td>
<td>0.0355</td>
<td>0.0310</td>
<td>6.3</td>
</tr>
</tbody>
</table>

4.2.2 Screen-Printed Capacitor Testing

A series of tests are performed in order to validate the simulated and theoretical results of the SPCs. The fundamental purpose of these tests is to help establish a baseline for SPC performance. These tests use a nearly identical setup as the resistor tests except they use an HP 4280A C-Meter to measure a device’s capacitance.

The first set of measurements look at SPC capacitance values at room temperature. The purpose of this test is to determine if the capacitance values agree with the theoretical and simulated values, and to establish a baseline for capacitor performance. The testing uses the experimental setup shown in Figure 4.3. The measured values for capacitance are tabulated in Table 4.4.
Table 4.5: SPC Temperature Swept Measurements ($R_n$ Indicates Large-Area SPR; $r_n$ Indicates Small-Area SPR)

<table>
<thead>
<tr>
<th>Expected Capacitance Values (nF)</th>
<th>Chip 1 Capacitance Values (nF)</th>
<th>Chip 2 Capacitance Values (nF)</th>
<th>Chip 3 Capacitance Values (nF)</th>
<th>Average Capacitance Values (nF)</th>
<th>% Deviation ($\frac{C_{\text{dev}}}{C_{\text{avg}}}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>0.0031</td>
<td>0.0030</td>
<td>0.0031</td>
<td>0.0032</td>
<td>0.0030</td>
</tr>
<tr>
<td>C2</td>
<td>0.0068</td>
<td>0.0067</td>
<td>0.0067</td>
<td>0.0066</td>
<td>0.0067</td>
</tr>
<tr>
<td>C3</td>
<td>0.0063</td>
<td>0.0063</td>
<td>0.0062</td>
<td>0.0063</td>
<td>0.0065</td>
</tr>
<tr>
<td>C4</td>
<td>0.0043</td>
<td>0.0043</td>
<td>0.0044</td>
<td>0.0044</td>
<td>0.0043</td>
</tr>
<tr>
<td>C5</td>
<td>0.0062</td>
<td>0.0064</td>
<td>0.0063</td>
<td>0.0064</td>
<td>0.0065</td>
</tr>
<tr>
<td>C6</td>
<td>0.0045</td>
<td>0.0045</td>
<td>0.0044</td>
<td>0.0045</td>
<td>0.0044</td>
</tr>
<tr>
<td>C7</td>
<td>0.0356</td>
<td>0.0356</td>
<td>0.0355</td>
<td>0.0366</td>
<td>0.0356</td>
</tr>
</tbody>
</table>

The next test is a temperature ramp test. The purpose of this test is to measure the value of capacitance as a function of temperature. This test follows the same primary testing procedure as the previous test, except instead of maintaining the temperature fixed at room temperature, the temperature of the platform is varied between $25^\circ C$ and $100^\circ C$. The values for capacitance is measured and the values are tabulated below in Table 4.5.

An additional test is performed in order to determine the performance of a capacitor after iterative exposure to high-temperatures. This test is performed in order to evaluate any variations in capacitance after being exposed to high heat for an extended period of time. For this test the chip will be placed on a hot plate set to $225^\circ C$ for a ten minutes. After ten minutes the chip will be removed from the hot plate, allowed to cool for 15 minutes back to room temperature ($25^\circ C$), and placed on the probing station platform using the probes to measure capacitance. This process is repeated six times. The resulting values for capacitance are shown below in Table 4.6.
Table 4.6: SPC Values for Capacitance After Iterative heat exposure

<table>
<thead>
<tr>
<th></th>
<th>I0</th>
<th>I1</th>
<th>I2</th>
<th>I3</th>
<th>I4</th>
<th>I5</th>
<th>I6</th>
<th>I6-I0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>(pF)</td>
<td>(pF)</td>
<td>(pF)</td>
<td>(pF)</td>
<td>(pF)</td>
<td>(pF)</td>
<td>(pF)</td>
<td></td>
</tr>
<tr>
<td>C1</td>
<td>3.01</td>
<td>3.61</td>
<td>3.20</td>
<td>3.11</td>
<td>3.10</td>
<td>3.02</td>
<td>3.31</td>
<td>0.30</td>
</tr>
<tr>
<td>C2</td>
<td>6.62</td>
<td>7.06</td>
<td>6.87</td>
<td>6.74</td>
<td>6.74</td>
<td>6.60</td>
<td>6.92</td>
<td>0.30</td>
</tr>
<tr>
<td>C3</td>
<td>6.38</td>
<td>6.77</td>
<td>6.56</td>
<td>6.44</td>
<td>6.44</td>
<td>6.29</td>
<td>6.59</td>
<td>0.21</td>
</tr>
<tr>
<td>C4</td>
<td>4.17</td>
<td>4.78</td>
<td>4.59</td>
<td>4.49</td>
<td>4.45</td>
<td>4.30</td>
<td>4.57</td>
<td>0.40</td>
</tr>
<tr>
<td>C5</td>
<td>6.34</td>
<td>6.77</td>
<td>6.62</td>
<td>6.52</td>
<td>6.47</td>
<td>6.34</td>
<td>6.66</td>
<td>0.32</td>
</tr>
<tr>
<td>C6</td>
<td>4.59</td>
<td>4.76</td>
<td>4.68</td>
<td>4.57</td>
<td>4.51</td>
<td>4.43</td>
<td>4.70</td>
<td>0.11</td>
</tr>
<tr>
<td>C7</td>
<td>28.9</td>
<td>28.8</td>
<td>28.7</td>
<td>28.6</td>
<td>28.5</td>
<td>28.3</td>
<td>28.7</td>
<td>-0.20</td>
</tr>
</tbody>
</table>

4.2.3 Thermal Via Array Testing

The thermal vias are tested in order to determine whether their performance holds true to theoretical calculations and simulated results described in Chapter III. In order to test the thermal vias, the chip is placed on an 8 in. x 8 in. x 1.56 in. aluminum heat spreader that is heated using a UL Type 900 hot plate set to 150°C. The chip is allowed sit for 30 minutes before pictures are taken using a FLIR A655sc Infrared camera and surface temperature measurements are taken using a thermocouple connected to a Fluke 28 II multimeter. A second Fluke 116 multimeter and thermocouple is used to measure the ambient air temperature. The thermocouple connected to the Fluke 28 II multimeter is used to take measurements at four different points both on the chip: the MVA, the ground plane on the substrate, a brazed contact, and the substrate itself. Additional readings are taken of the ambient room temperature and the aluminum heat spreader temperature. The readings are tabulated and cross-referenced with the FLIR temperature readings. An IR image of the MVA being measured is shown in Figure 4.4. This process is repeated 3 times for result verification. The measured values for \( T_R \) are tabulated below as Table 4.7.
Table 4.7: MVA Thermo couple measurements

<table>
<thead>
<tr>
<th></th>
<th>I1 (K)</th>
<th>I2 (K)</th>
<th>I3 (K)</th>
<th>Average (K)</th>
<th>$T_R$ (K)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Heat Spreader</td>
<td>344.0</td>
<td>344.3</td>
<td>345.8</td>
<td>344.7</td>
<td>N/A</td>
</tr>
<tr>
<td>MVA</td>
<td>338.8</td>
<td>339.3</td>
<td>340.4</td>
<td>339.5</td>
<td>5.2</td>
</tr>
<tr>
<td>Ground Plane</td>
<td>335.9</td>
<td>336.8</td>
<td>337.4</td>
<td>336.7</td>
<td>8.0</td>
</tr>
<tr>
<td>Contact</td>
<td>335.2</td>
<td>336.2</td>
<td>337.0</td>
<td>336.1</td>
<td>8.6</td>
</tr>
<tr>
<td>Substrate</td>
<td>334.2</td>
<td>335.2</td>
<td>336.2</td>
<td>335.2</td>
<td>9.5</td>
</tr>
<tr>
<td>Room</td>
<td>296.4</td>
<td>296.5</td>
<td>296.0</td>
<td>296.3</td>
<td>N/A</td>
</tr>
</tbody>
</table>

Figure 4.4: FLIR Camera Capture of MVA Measurement Using Thermocouples
4.2.4 Chip Characterization

The first measurement that is performed in order to characterize a chip is a surface profile study. Using an Ambios XP-7 stylus profilometer, several scans are taken of each side of the test structure chip. Scans are performed by dragging a stylus across the surface of an object, changes surface topography are sensed by changes of the stylus altitude. Each scan creates a dataset that can be used to generate 1-dimensional plots of the chip’s surface topography. A total of 8 scans of the front and 3 scans of the back are taken in order to provide a general overview of chip topography. The scan paths for both the front and the back of the chip are taken going from left to right as shown in figure 4.5. Figures 4.6 and 4.7 are the 1-dimensional topographical plots resulting from scans of the top and bottom of the chip, respectively.
A second test is done to characterize the overall chip using a hydration test. In order to perform this test, an LTCC test chip is heated to 225°C using a hotplate and is then dropped on a block of ice. This process is repeated three times. A fourth heating cycle heats the chip to 300°C before cooling it in order to see if higher temperatures make any difference. The purpose of these tests is to see what happens to a hot chip when it is rapidly cooled using ice. This is a relevant test as aerospace electronics are often exposed to extreme and rapid temperature changes. The entire process is recorded on video. Figure 4.8 is the chip before and after all four heating and cycles.
Figure 4.6: 1-Dimensional Topographical Plots of the Top of the Test Chip: Left-Most Small Area SPRs (top-middle), First Half of Large SPC (top-right), Second Half of Large SPC (center-left), Left-of-Center Large Area SPRs (center-middle), MVA (center-right), Right-of-Center Large Area SPRs (bottom left), Focused Scan of Right-of-Center Large Area SPRs (bottom-middle), Right-Sided SPCs (bottom-right)
Figure 4.7: 1-Dimensional Topographical Plots of the Back of the Test Chip: Backside of the MVA (top), Contacts on the Left Side (middle), Contacts on the Right Side (bottom)

Figure 4.8: Chip After Hydration Test (left) Chip before hydration Test (right)
5.1 Screen-Printed Resistor Results

We will discuss the results presented in Chapter 4 Section 1. One important artifact that we noticed was the mean percent deviation between the measured and designed resistor values was 52.6% for the large area SPRs and 20.26% for small area SPRs. Further, the percent yield was 71.4% for large area SPRs and 97.0% for small area SPRs. Thus, the small area SPRs have both better matching to designed values and good yield. These results come as a surprise due to the fact that the small-area SPRs are below minimum size specifications for an SPR, as such, it should be expected that the small area SPRs should have a lower yield than the large area SPRs. However, after careful consideration the reason for these peculiar results become more understandable. During the sintering process, the Ferro A6M sheets shrink (counter-acting thermal expansion of the conductor layer) in X-, Y-, and Z-direction due to water and other liquids being evaporated. The contraction of the dielectric sheets, along with expansion of the SPR, causes compressive stress on the SPR resulting in serious deformation. While this happens to both large- and small-area SPRs, the effects are more dramatic on the large-area SPR due to a larger bend radius. It is worth pointing out that the two large-area resistor designs that had a 0% yield rate were stacked resistors designs. These almost certainly failed as a result of vias being
severed due to stacked layers exacerbating SPR deformation (similar to how a two-layer metal structure is used to increase actuation distance in thermo-actuators). The difference in deformation also explains why the small-area SPRs had an overall lower percent deviation since the deformation took place on a much smaller scale. Furthermore, we did not notice any difference in the effect of temperature on the resistance of second-layer SPRs and third-layer SPRs.

As was expected from the temperature dependent resistor model, the resistance of all resistors decreased with an increase in temperature. While the change in resistance does not display a perfectly linear relationship with respect to temperature (as it did in the theoretical model), it behaves quadratically. Resistance as a function of temperature for all resistors measured in this test can be seen in figures 5.1 and 5.2.

This implies that there is a secondary value of TCR in these resistors. While the measurement of this value is outside of the scope of this thesis (it requires some specialized equipment), the value of TCR2 is approximated to be $3.5 \frac{ppm}{K}$. Additionally, the datasheet for the Ferro material [7] shows that the TCR1 value should be +/- 450, however, the measurements indicated a value closer to $1000 \frac{ppm}{K}$. Figure 5.3 shows a comparison between the theoretical values for resistance using approximated TCR1 and TCR2 and the measured values for resistance for r6.
Figure 5.1: Small Area SPR; Resistance as a Function of Temperature

Figure 5.2: Large Area SPR; Resistance as a Function of Temperature
Several conclusions about the integrity of SPRs can be drawn from the results of the iterative heating tests. As can be seen from table 4.3, SPR resistance decreased with an increased number of heating cycles. It is apparent that both the large area and small area SPRs respond similarly to iterative heating; decreases in resistance become smaller from first to last iteration. Figures 5.5 and 5.6 show the change in resistance for each heating iteration for large and small area SPRs, respectively.

While the change in resistance does not indicate dramatic degradation, (except in the case of r10) the value of resistance appears to decrease with repeated exposure to high-temperatures. However, there were several iterations in which the resistance appeared to increase. For example, the first iteration appeared to increase the resistance for numerous large area resistors by as much as 13.2 $\Omega$ (in the case of R7). This trend is not indicative of the FX87-101 material degrading, but instead expanding due to CTE. Since an SPR’s
Figure 5.4: Resistance as a Result of Iterative Heating; Large Area SPR

Figure 5.5: Resistance as a Result of Iterative Heating; Small Area SPR
resistance is highly dependent on aspect ratio, a small change in a resistor’s width or length can have a fairly significant effect on resistance value.

5.2 Screen-Printed Capacitor Results

Several conclusions can be drawn from the capacitor tests. As can be seen in Table 4.4 in Chapter 4, every capacitor that was tested was able to be measured within an acceptable margin of error (the average percent deviation from the expected value is 32.8%). While it is desirable for this number to be closer to zero, the percent deviation for SPCs is still lower than large area SPRs. Furthermore, the capacitors had a 100% yield, which is better than both the large and small area SPRs.

The SPCs showed no variation due to change in temperature. This measured behavior agrees with the simulated behavior from shown as Figure 3.3 from Chapter 3, in which thermal expansion of the dielectric and conductor changed capacitance by less than a femto-farad every $10^\circ C$. While there is some random variation in the measured values for capacitance, it likely can be attributed to a variety of factors other than the temperature change. Therefore, as would be expected a best-fit-line is a horizontal line with zero slope. This means that capacitance changed too little to change the best-fit line and that capacitance did not change consistently. This behavior can be seen from Figure 5.5.

The iterative temperature exposure tests were inconclusive. While it appeared that iterative temperature exposure has some effect on the SPCs, there is no logical trend that characterizes the change in capacitance. The only capacitor to have a loss in capacitance is C7, which had an overall decrease of 0.20 pF. Other than C7, all capacitors increased in value from the first to sixth iteration. The behavior of C1 through C6 is shown as Figure 5.8. This plot shows that all capacitors exhibited an increase in capacitance and a similar
behavior with each iteration. While the temperature simulations resulted in decreased capacitance, it is possible that the Temperature Coefficient of Capacitance (TCC) of LTCC SPCs can cause an increase in capacitance (however, the value for TCC is not documented for Ferro A6M capacitors). This could explain why C7 experienced a decrease in capacitance. Since C7 includes significantly more dielectric material, it is possible that the effects of CTE outweighed the effects of TCC in effecting its capacitance.
5.3 Thermal Via Results

Several trends regarding thermal via design can be seen from the simulations. Amongst these are that as area grows (while \( l \) remains the same) in proportion to the number of vias, the thermal resistance changes linearly. Furthermore, as substrate and via height increases \( T - R \) also increases. This indicates that as \( l \) increases, the thermal resistance increases and the thermal conductance decreases, agreeing with the expected theoretical behavior of thermal vias. With this understanding, it can be hypothesized that there are two factors that affect the effectiveness of a thermal via array. The first factor is the total surface area of all vias in the array; more surface area means more heat that can be dissipated resulting in a smaller \( T_R \) and smaller thermal resistance. The second governing factor is parallel resistance; the larger and more numerous channels (vias), the lower the overall thermal resistance.

Following the trends seen in the thermal via simulations, the MVA is able to perform significantly better than a bare substrate. The average temperature differential through the

![Change in Capacitance Per Iteration for SPCs](image)

Figure 5.7: Capacitance as a Result of Iterative Heating
thermal vias is $5.2^\circ C$, $4.3^\circ C$ less than the $\Delta T$ through the substrate. As can be recalled from Chapter 3 Section 3, a lower temperature differential is indicative of a greater ability to dissipate heat from an active source. While the performance of the MVA test structure was not as good as that of the simulated 6mm x 6mm MVA, it still was an improvement over the bare substrate. There are several factors that could have resulted in the difference between the measured and simulation results. The first reason is that the overall size of the measured MVA is smaller than the simulated MVA meaning that there were less channels for heat to travel through. The second reason is that the measured MVA used a mixed metal system. Recalling Chapter 3 Section 3, it was apparent that an Ag only system was superior to an Au only system, therefore, it can be said with some confidence that a system that uses both Au and Ag will not perform as well as a system that uses only Ag.

While the temperature difference between the $T_R$ of the MVA and bare substrate seems like a small change it is rather quite significant. For high temperature electronics, particularly any that are intended to operate above $175^\circ C$, every degree Celsius of dissipated heat helps to increase the operational life of electronics. Therefore, the $4.3^\circ C$ temperature differential between the MVA and the bare substrate is quite a significant difference. This differential is significant enough to protect electronics when they are exposed to short bursts of extreme heat such as in excursions (when a jet applies afterburners). Even when exposed to extreme temperatures in scenarios such as the one mentioned above the thermal vias will continue to dissipate heat from active components. While this may seem counter-intuitive, the junction temperature of micro-electronic devices is approximately $25^\circ C$ higher than ambient temperature, as such the temperature gradient will always result in heat dissipating from the an active component into the surrounding environment.

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Remark ing on the FLIR image, upon first glances it can appear to be very misleading as it makes the MVA appear to be a complete failure. This is because it shows the surface of both the aluminum heat spreader, MVA, and contacts (all metal surfaces) to be the ‘cold’. While this is clearly not the case, since the thermocouple measurements showed these to be the warmest surfaces, this occurs due to metal’s emissivity making it show up as cold on infrared images.

### 5.4 Chip Characterization

The surface profilometry test revealed a significant amount of deformation due to the sintering process. The one dimensional topographical plots reveal that the substrate warped most significantly in and around the MVA and large area SPRs. There are two reasons that this happened: posting and warpage due to stress. Posting is a deformation that occurs when the substrate shrinks around the thermal vias, the result is a tent- or bubble-like structure. Warpage due to stress occurs where there is a conductive sheet that is pinched under compressive stress. As the substrate shinks in the x- and y-direction it pinches and compresses the conductor causing it to ‘bubble’ in the center, resulting in serious, possibly even damaging, deformations. Warpage due to stress is what likely caused 0% yield of R4 and R5 large area screen printed resistors as it likely created enough force to break electrical connections. Furthermore, it is worth noting that the large-scale deformations caused by the large area SPRs and MVAs were significant enough that the profilometer stylus would lift off of the surface of the substrate, resulting in the flat lines in the topographical plots shown in Figures 4.6 and 4.7 from Chapter 4 Section 2.4. These results also showed that the small-area SPRs, particularly those than are printed on the third dielectric layer, caused significantly less surface deformation. While the substrate deformations will not prevent future developments with the LTCC system, it indicates that the size of conductive sheets
and other structures needs to be taken into consideration and optimized to minimize substrate deformation.

As can be seen from Figure 4.8 in Chapter 4 Section 2.4 there is no noticeable change to the chip after heating and cooling. The hydration test proved that an LTCC chip does not absorb moisture and, thus, does not swell or explode when cooled extremely rapidly. In fact the chip cooled so rapidly it barely even left an indent in the block of ice. This is an excellent result since that indicates LTCC has excellent performance in harsh and rapidly-changing operational conditions.

5.5 Summary of Results

A number of conclusions can be made from the research presented in this thesis. First the SPRs exhibited similar behavior to that shown in the theoretical calculations. While the numerical results did not agree, the generalized pattern of behavior did agree. Specifically, the theoretical and experimental results all showed that the value of resistance would decrease with an increase in temperature. While the resistance as a function of temperature differed from what was expected due to different values of TCR, the anticipated behavior was still a useful model for predicting their behavior. Expanding on this, a best fit model was used to approximate the values of TCR1 and TCR2; the resulting values provide a closer fit for approximating resistance as a function of temperature for FX87-101 SPRs. Furthermore, based on the results seen in Chapter 5, it is apparent that the small area SPRs are superior to the large area SPRs in yield and deviation from the expected value. While this comes as a surprise (since the small-area SPRs are in fact smaller than minimum specifications) it is not necessarily counter-intuitive since smaller areas are less-likely to be warped during co-firing. Furthermore, iterative temperature exposure decreased the SPR resistance in almost every case. While this sort of behavior likely indicates that SPRs are
not application ready, some optimization of design could result in resistors that are as environment-robust as some thin-film resistors, but while retaining the larger value range of SPRs.

The SPCs behaved almost exactly as expected. While the real values of the test structures deviated from the expected values, as would be expected as a result of the warpage of conductors, they remained within an acceptable margin of error. More importantly, the capacitors were almost entirely unaffected by changes in temperature, precisely as shown in the simulations. Iterative temperature tests indicated SPCs that are exposed to high temperatures for an extended period of time can be effected by both TCE and TCC even after cooling. These results show that SPCs are environmentally robust and are practically unaffected by temperature. As such, SPC performance is comparable to high-temperature surface mount capacitors while taking up significantly less space. This is ideal for aerospace electronics in which minimization of weight and bulk are critical for aircraft performance.

Simulated and measured thermal via behavior, for the most part, agreed. While the MVA simulations performed better than the measured MVA, it is likely due to smaller dimensions and mixed metal system of the measured MVA. The measured MVA had a lower thermal resistance than the surrounding substrate and, as such, was able to dissipate more heat than a bare Ferro A6M substrate. While the amount of heat dissipated seems nominal, it is a significant number that can extend the life of high-temperature electronics such as those in aerospace systems.

Though deformation of the LTCC substrate is discouraging, as it effected the performance of the screen printed passives, it is not something that would limit future applications
of this system. Further research needs to be done in order to determine the optimal structure of SPCs, SPRs, and MVAs that minimize warpage before the screen printed passives, particularly the SPRs, are application ready.
CHAPTER VI

CONCLUSIONS AND FUTURE WORK

The aerospace industry is desperately seeking new ways to package micro-electronics for harsh environments. While epoxy-based packaging techniques such as PBGAs and QFPs have, historically, been the electronic packaging method of choice they are not reliable enough at high temperatures to be used in aerospace applications. As a result, packaging experts have relied on ceramic packaging. Ceramic packaging, a technique that is as old as electronic packaging itself, comes in two flavors: SMD packaging and embedded packaging. While SMD packaging is a relatively simple method that avoids the CTE and hydration problems associated with epoxy-based packaging it still experiences bulk, weight, and reliability issues associated with exposed solder joints. Embedded packaging techniques on the other-hand, such as the LTCC system, allow passives to be embedded in the substrate and active devices to be placed in hermetically sealed cavities. Embedded packaging techniques are self-contained and modular meaning that they do not need to be soldered to PCBs to complete circuits. As a result, embedded packaging is the most environmentally robust technique.
6.1 Concluding Remarks

The work presented in this thesis is used to establish a baseline for LTCC performance. Theoretical calculations, simulations, and measurements of fabricated SPR, SPC, and thermal vias were performed in order to establish a baseline for the LTCC system. The results of the physical measurements agreed with the theoretical calculations and simulations. All of these results indicated that the LTCC passives are environmentally robust devices that continue to operate within a tolerable range when subjected to high temperatures. Though the fabricated passives had a significant deviation from their intended values, they were within a tolerable range and provide some guidance on future design and implementation. The thermal vias were shown to dissipate heat away from an active device. While this particular structure was not as efficient as an elaborate heatsink, an MVA could easily be optimized to have similar performance or outperform many lightweight heatsinks.

6.2 Future Work

While this research provided a baseline for the performance of screen-printed LTCC structures and thermal vias, it did not extensively look at real-world applications or the use of thin-film passives. The next steps for evaluating the LTCC packaging system is to compare the performance of thin-film passives with screen-printed passives and to fabricate and test a modular device such as a controller or radar system for a real-world application.


MATLAB CODE FOR TEMPERATURE DEPENDENT RESISTOR MODEL

% Calculation of Temp. Depndnt Resistor Model
% Theoretical Calculations for MVA
% Devin A. Smarra
% Masters Thesis: Section 3.3 Simulations
% Temperature Dependent Resistor Model

clear all; close all; clc;
R_01 = 100; % Resistivity 101
R_02 = 1000; % Resistivity 102
R_03 = 10000; % Resistivity 103
W = 1000; % Width (um)
L = 1000; % Length (um)
TC1_1 = -450e-6; % Resistivity 101
TC1_2 = -250e-6; % Resistivity 102
TC1_3 = -250e-6; % Resistivity 103
T = linspace(-55,225,100); % Temperature Matrix (C)
T0 = 25; % Room Temperature (C)
R = zeros(100);

figure
R1 = R_01*(1+TC1_1*(T-T0))
subplot(3,1,1)
plot(T,R1,25,100,'-o')
xlabel('Temperature (C)')
ylabel('Resistance (Ohms)')
title('Relationship Between Temperature...and Resistance (.1k Resistivity)')
R2 = R_02*(1+TC1_2*(T-T0))
% Calculate Temperature Dependent Model
subplot(3,1,2)
plot(T,R2,25,1000,'-o')
xlabel('Temperature (C)')
ylabel('Resistance (Ohms)')
title('Relationship Between Temperature... and Resistance (1k Resistivity)')
axis([-100 250 950 1100])
R3 = R_03*(1+TC1_3*(T-T0))
% Calculate Temperature Dependent Model 3
subplot(3,1,3)
plot(T,R3,25,10000,'-o')
xlabel('Temperature (C)')
ylabel('Resistance (Ohms)')
title('Relationship Between Temperature... and Resistance (10k Resistivity)')
axis([-100 250 9500 11000])
%Calculation of Parallel Thermal Resistances% 
%Theoretical Calculations for MVA %
%Masters Thesis: Section 3.3 Simulations %

k_ag = 250; % Thermal Conductivity Silver 
k_au = 50; % Thermal Conductivity Gold 
k_sub = 2; % Thermal Conductivity A6M

via_r = [50e-6 75e-6 125e-6]; % Via Radii (m)
1 = 778e-6; % Length of Single Via (m)
a1 = 1e-3*1e-3; % Area of Substrate (m)
a2 = pi*(via_r).^2; % Area of Via (m)

% Thermal Reistance (TR) Calcs.
R_sub = l./(k_sub*a1); % TR sub
R_Ag = l./(k_ag.*a2); % TR of 1 Ag Via
R_Au = l./(k_au.*a2); % TR of 1 Au Via

R2(1,:) = (1./R_Ag+1./R_Ag).^(-1); % TR of 2 || Silver Vias
R2(2,:) = (1./R_Au+1./R_Au).^(-1); % TR of 2 || Gold Vias

%Store both calculated values into 2 variable matrix
R4 = (1./R2 + 1./R2).^(-1);
R_tot_4 = (R4.*R_sub)./(R4+R_sub) % TR of 4 Via Array

R8 = (1./R4 + 1./R4).^(-1);
R_sub = 1./(k_sub*2*a1);
R_tot_8 = (R8.*R_sub)./(R8+R_sub) % TR 8 Via Array

R16 = (1./R8 + 1./R8).^(-1);
R_sub = 1./(k_sub*4*a1);
R_tot_16 = (R16.*R_sub)./(R16+R_sub) % TR 16 Via Array
\[ R_{32} = (1./R_{16} + 1./R_{16}).^{\sim 1}; \]
\[ R_{\text{sub}} = 1./ (k_{\text{sub}} \times 8 \times a1); \]
\[ R_{\text{tot} \_32} = (R_{32} \times R_{\text{sub}})/(R_{32} + R_{\text{sub}}) \% \text{ TR 32 Via Array} \]

\[ R_{64} = (1./R_{32} + 1./R_{32}).^{\sim 1}; \]
\[ R_{\text{sub}} = 1./ (k_{\text{sub}} \times 16 \times a1); \]
\[ R_{\text{tot} \_64} = (R_{64} \times R_{\text{sub}})/(R_{64} + R_{\text{sub}}) \% \text{ TR 64 Via Array} \]

\[ R_{128} = (1./R_{64} + 1./R_{64}).^{\sim 1}; \]
\[ R_{\text{sub}} = 1./ (k_{\text{sub}} \times 32 \times a1); \]
\[ R_{\text{tot} \_128} = (R_{128} \times R_{\text{sub}})/(R_{128} + R_{\text{sub}}) \% \text{ TR 128 Via Array} \]
APPENDIX C

ADDITIONAL TEST EQUIPMENT

Figure 6.1: HP 4280A C-Meter
Figure 6.2: Jmicro LMS-2709 Probing Station
Figure 6.3: Elcor MTTC1410 Thermoelectric Temperature Controller

Figure 6.4: FLIR Camera [1]
Figure 6.5: Type 900 Hotplate [2]

Figure 6.6: Fluke 116 Multimeter [3]

Figure 6.7: Ambios XP-7 Profilometer [4]
Figure 6.8: Keithley 2400 Sourcemeter

Figure 6.9: Hot Plate Setup Used for Iterative and Hydration Tests