3-DIMENSIONAL PHOTONIC CIRCUITS FOR QUANTUM INFORMATION PROCESSING

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ABSTRACT

3-DIMENSIONAL PHOTONIC CIRCUITS FOR QUANTUM INFORMATION PROCESSING

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For many years silica fibers have been used for long-distance transfer of quantum information, and in particular within the domain of quantum communications and quantum key distribution. This is in part due to the ability to transmit tens of kilometers with negligible decoherence and loss. Although optical fibers fabricated with transparent materials such as SiO₂ allow for the necessary low-loss transmission, they lack the photon-photon nonlinearity that are necessary for implementation of the other aspect of quantum information, that of quantum computation. The necessary nonlinearity, that is weak in SiO₂, is stronger in material such as silicon nitride. In fact, silicon nitride has proven to be a promising platform for the generation and manipulation of single photons. The strong optical nonlinearity allows for parametric four-wave mixing which can be utilized to generate twin photons, while the transparency of silicon nitride in the near IR allows for low loss wave guides to be fabricated. However, due to silicon nitride’s
dielectric nature and wide bandgap, it cannot be used as a photon counter - a necessary component for any quantum information protocol. In fact, in the visible and near-infrared, the detection of single-photons is possible using silicon avalanche photodiodes (SPADs). Silicon has proven to be a high-efficiency, high-speed, and low-cost single photon detector for wavelengths below 1 µm.

Combining these two materials in a 3-D integrated circuit provides a platform capable of generating, routing, and detecting single photons. This 3-D device provides the transparency and nonlinearity of silicon nitride near IR, with the single-photon detection capability of silicon. These properties are ideal for future development of integrated quantum circuits for scalable quantum information processing applications.

For the stoichiometric silicon nitride to act as a guiding layer it must be deposited using low pressure chemical vapor deposition (LPCVD). LPCVD results in a denser, high quality, sturdy silicon nitride film. If the silicon nitride is deposited using plasma enhanced chemical vapor deposition (PECVD) method the layer could have cracks throughout the film along with other impurities such as high hydrogen or excess silicon which can cause energy loss to the guided waves. Due to the dense and sturdy nature of LPCVD silicon nitride it can also act as a hard mask to protect the silicon photodetectors throughout the necessary thermal oxidation process.

A wet thermal oxidation planarization technique is utilized in the fabrication of this photodector device. By thermally oxidizing the silicon the expensive chemical mechanical planarization technique can be avoided altogether. This also allows us to avoid chemical mechanical planarization (CMP) limitations such as wafer bow,
curvature, and warp. We note here that our technique, due to the stress of the growth of the thermal oxide on the silicon nitride hard mask, shows some unavoidable imperfections, such as a bump known as a “bird’s beak” which forms along the edges of the masked silicon.
This work is dedicated to my wife, son, and entire family. A special feeling of gratitude to my loving wife Caitlin who was always supportive during late nights and frustrations; to Axl who always puts a smile on my face; and to my parents, brothers, sisters, and in-laws who supported and encouraged me throughout the entire program.
I would like to acknowledge the support of the Air Force Office of Scientific Research (AFOSR) (PM: Gernot Pomrenke).

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I would also like to acknowledge David Lombardo for his support in Dr. Sarangan’s lab and for performing etches and assisting with the characterization of the etch rate of LPCVD Si₃N₄ films. Finally, a special thanks to Dr. Jay Mathews for allowing me to characterize the hot phosphoric acid etch in his lab.
TABLE OF CONTENTS

ABSTRACT ................................................................................................................................. iv

DEDICATION ............................................................................................................................... vii

ACKNOWLEDGEMENTS ............................................................................................................. viii

LIST OF FIGURES ................................................................................................................ xi

LIST OF TABLES ....................................................................................................................... xiv

CHAPTER 1: INTRODUCTION ................................................................................................... 1

CHAPTER 2: GUIDED WAVE OPTICS ....................................................................................... 5

2.1 Maxwell’s Equations ........................................................................................................... 5

2.2 Reflection and Refraction ................................................................................................. 11

2.3 Dielectric Waveguides ..................................................................................................... 15

2.4 Coupled Mode Theory ..................................................................................................... 20

CHAPTER 3: NANOFABRICATION THEORY ........................................................................... 24

3.1 Silicon on Insulator .......................................................................................................... 24

3.2 Photolithography ............................................................................................................ 24

3.3 Deposition Processes ...................................................................................................... 30

3.4 Chemical Mechanical Planarization ............................................................................... 36
3.5 Etching Processes .............................................................................................................. 38

CHAPTER 4: DEVICE SIMULATION AND FABRICATION ............................................. 45

4.1 Photodetector Design .................................................................................................... 45

4.2 Lumerical FDTD Simulation ..................................................................................... 47

4.3 Device Fabrication using CMP .................................................................................. 49

4.4 Device Fabrication using Thermal Oxidation ............................................................ 54

CHAPTER 5: FUTURE PLANS ......................................................................................... 66

5.1 Hot Phosphoric Acid Etch .......................................................................................... 66

5.2 Electron Beam Lithography ........................................................................................ 67

5.3 Silicon Nitride Waveguide Etch ................................................................................. 68

5.4 Waveguide on Detector Device Characterization .................................................... 68

5.5 Wafer Flattening .......................................................................................................... 69

5.6 Bird’s Beak Reduction ............................................................................................... 69

CHAPTER 6: CONCLUSIONS ......................................................................................... 71

REFERENCES ....................................................................................................................... 73

APPENDIX: Recipes .............................................................................................................. 78
LIST OF FIGURES

<table>
<thead>
<tr>
<th>Figure</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.1</td>
<td>The design for a silicon nitride waveguide on silicon photodetector for future development of integrated quantum circuits</td>
<td>2</td>
</tr>
<tr>
<td>1.2</td>
<td>Lumerical FDTD design and simulation of a silicon nitride transport layer on a silicon photodetection layer. Left we see the phase matched coupling of the E-field between the nitride and silicon layers. Right we see the setup for the transport and detection layers.</td>
<td>3</td>
</tr>
<tr>
<td>2.1</td>
<td>A wave incident on an interface with angle $\theta$ will reflect and refract.</td>
<td>12</td>
</tr>
<tr>
<td>2.2</td>
<td>Different type of rectangular dielectric waveguides. In a) the top surface is exposed to air, b) shows lateral confinement due to the top ridge, and c) is a waveguide completely encased by the cladding.</td>
<td>19</td>
</tr>
<tr>
<td>2.3</td>
<td>The effective index method is implemented by considering the indices of refraction as if they were two planar slab wave guides.</td>
<td>19</td>
</tr>
<tr>
<td>2.4</td>
<td>A directional coupler consisting of two waveguides silicon nitride waveguides in a silicon dioxide cladding separated by a distance $2a$ and with widths of $2b$</td>
<td>21</td>
</tr>
<tr>
<td>3.1</td>
<td>On the left we see the final thickness of photoresist spun at 2000 RPM over time. The initial thickness is varied, but we see over time the final thickness is limited. The plot on the right shows the final resist thickness as a function of acceleration and spun for 30 seconds. We see that the acceleration of the substrate plays a role in the how quickly the minimum thickness is reached, but again is limited by the resist properties.</td>
<td>27</td>
</tr>
<tr>
<td>3.2</td>
<td>An image of a mask design. The blue areas represent the silicon pads that will be masked during the exposure process. The red represent where the silicon nitride waveguides will be deposited. The crosses are alignment markers that allow alignment for multi-step fabrication.</td>
<td>28</td>
</tr>
<tr>
<td>3.3</td>
<td>Example of Fresnel Zones [15].</td>
<td>29</td>
</tr>
<tr>
<td>3.4</td>
<td>The image on the left is the photoresist pattern for the 10 $\mu$m wide silicon pad. On the right the alignment markers to allow the e-beam lithography step to be aligned.</td>
<td>30</td>
</tr>
</tbody>
</table>
Figure 3. 5: The top image the isotropic CVD coats the vertical and horizontal surfaces of the sample. The bottom image shows the line of sight PVD coats only the horizontal surfaces of the sample.......................................................... 31

Figure 3. 6: A 3 inch silicon wafer with no processing done measured by a Zygo white light interferometer. We see that there is already bow and warp to the wafer before any processes have taken place.......................................................... 37

Figure 3. 7: The Zygo surface profile of one of the pieces of a cleaved silicon wafer. We can see a linear profile on the right that shows the curvature of that slice. ........................................................................................................................... 38

Figure 3. 8: The Zygo surface profile of a second piece of the previously mentioned 3 inch silicon wafer. With this piece we see a different curvature and warp from the first piece. ........................................................................................................................... 38

Figure 3. 9: A typical cross section of a wet chemical etch. Due to the isotropic nature of this etch the removed area is shaped like a bowl.......................................................... 40

Figure 3. 10: Chemical vapor deposition and etching with the volatile and nonvolatile reactions demonstrated.......................................................... 40

Figure 3. 11: The positive ions bombard the substrate and cathode releasing secondary electrons to sustain the plasma and slowly sputter the sample. Neutral free radicals react and chemically etch the substrate.......................................................... 41

Figure 3. 12: An illustration of the expected nearly vertical sidewalls of an RIE process. ...................................................................................................................... 42

Figure 3. 13: Illustration of the rippled sidewalls on vertical etch of silicon during the original Bosch process. ...................................................................................................................... 44

Figure 4. 1: A top view of the silicon photodetectors surrounded by an insulating layer of silicon dioxide...................................................................................................... 46

Figure 4. 2: 400 μm long silicon nitride waveguides are patterned on top of the silicon photo detectors. ...................................................................................................................... 47

Figure 4. 3: Final device design. The fundamental mode is injected into the silicon nitride waveguide which is insulated by silicon dioxide. The guided mode is then vertically coupled into the silicon photo detector ........................................................................... 48

Figure 4. 4: The Lumerical FDTD simulated fundamental TE mode injected into the silicon nitride guiding layer. ...................................................................................................................... 48
Figure 4.5: The Lumerical FDTD electric field simulation of the silicon nitride on silicon waveguide on photo detector device. ................................................................. 49

Figure 4.6: The designed process utilizing CMP polishing to fabricate the waveguide on photo detector devices. .............................................................................. 50

Figure 4.7: The resulting pattern of the photolithography process stated above. Left we see the photoresist pattern for the silicon detector pads are 100 μm apart. Right we see the 10 μm wide silicon detector pattern. .............................................................. 51

Figure 4.8: The pressure, ICP power, RF bias, time, and gas flow parameters of the SDRIE process used to etch silicon. ........................................................................... 52

Figure 4.9: KLA Tencore surface profile of a 10 second SDRIE process done to a patterned silicon wafer. ............................................................................................... 52

Figure 4.10: The Zygo surface profile of a SOITEC 25mm by 25mm SOI piece. We see that without any processing the sample has a curvature of about 1.8 μm. ......... 53

Figure 4.11: The planarization process using thermal oxidation. Left starts with a sturdy LPCVD silicon nitride on silicon. Center is the result of a plasma etch to 44% the original height of the silicon. Right the thermal oxidation process grows to the original height. ........................................................................................................ 54

Figure 4.12: Overview of the thermal oxidation planarization process for the fabrication of waveguide on photo detector devices......................................................... 56

Figure 4.13: The LPCVD silicon nitride on silicon surface profile after 150 second SDRIE etch. The total step height is about 320 nm. ......................................................... 57

Figure 4.14: The OTF-1200X-Series furnace used at the University of Dayton for wet thermal oxidation processes. ...................................................................................... 58

Figure 4.15: Surface profile step height after a 1 hour 20 minute oxidation of 247 nm of silicon. ............................................................................................................. 60

Figure 4.16: Scanning electron microscope (SEM) image of the silicon photo detector encased by silicon dioxide and silicon nitride. The 522 nm feature is the silicon pad while the 133 nm layer above is the silicon nitride mask................................. 61

Figure 4.17: A Lumerical FDTD electric field simulation of the silicon nitride waveguide on silicon photo detector device. The bird’s beak is modeled around the 50 μm point. ........................................................................................................ 62
LIST OF TABLES

Table 1: The etch rates of two pieces of silicon nitride on silicon in a pixel patter in a phosphoric acid bath. Each bath starts with new acid, and a 20 minute silicon nitride seasoning. .............................................................................................................. 64
CHAPTER 1

INTRODUCTION

Silicon has shown promise as a high-speed, high-efficiency, and low-cost single photon detector below 1 \( \mu \)m [1,2]. Silicon has also shown good detection efficiency at 800 nm wavelengths. However, due to the absorptive nature of silicon at these wavelengths, it cannot be equally used as a data/transmission layer. Silicon nitride on the other hand has been shown be an efficient waveguide as well as provide generation and manipulation of single photons [3,4]. Its transparent low-loss, and optical nonlinear attributes allow parametric four-wave mixing to occur. This four-wave mixing allows the generation of twin photons which can be extended to generating entangled states. By utilizing and combining the single-photon detecting capabilities of silicon with the transparency and nonlinearity of silicon nitride future 3-D integrated quantum circuits for quantum information processing applications can be developed [5]. In this project we look to develop an integrated phase matched waveguide on photodetector device shown in figure 1.1.
Figure 1.1: The design for a silicon nitride waveguide on silicon photodetector for future development of integrated quantum circuits.

The ability to transfer photons from the silicon nitride layer to the silicon layer is necessary for single-photon detection. The transfer between the transport layer and photodetection layer must have nearly perfect efficiency with very low latency. The parameters of the nitride and silicon layers are critical due to the large difference in the refractive indices of the two materials. The refractive index difference is great enough that the silicon layer can act like a mirror and reflect the photons rather than having a transfer occur. Because of this it is necessary to phase match the mode of the silicon nitride transport layer to a higher order mode of the silicon photodetection layer. Figure 1.2 below shows a 250 nm Si$_3$N$_4$ layer deposited on a 500 nm Si layer. These numbers were chosen to match the available SOITEC silicon on insulator (SOI) wafers [6]. Once the field couples into the silicon we see that it is absorbed quickly. This design is part of the development of a Single Photon Avalanche Diode (SPAD) integrated in a waveguide fabricated in the silicon layer.
Figure 1.2: Numerical FDTD design and simulation of a silicon nitride transport layer on a silicon photodetection layer. Left we see the phase matched coupling of the E-field between the nitride and silicon layers. Right we see the setup for the transport and detection layers.

The classical approach requires an external detector to be coupled to the optical circuit by an optical fiber. The on-chip design provides advantages in integrability, scalability, coupling efficiency, and improvements in achievable photon detection efficiency and temporal resolution. The state of the art SPAD detectors used today are developed by Politecnico di Milano and are based on “thin” SPAD technology [7]. These detectors have achieved spatial resolution as low as 35 ps or less with about 50% photon detection efficiency (PDE) in the visible range. However, these detectors are not effecting in the near IR due to the limiting thickness of their absorption layer.

One method of overcoming this problem is to increase the thickness of the absorption layer. The researchers at Politecnico di Milano have found that the thicker layer does result in up to 20% more PDE at 900 nm. However, there is a trade-off that causes the temporal jitter of these SPAD devices to jump up to about 90 ps due to the
increased distance the photogenerated carriers have to travel and the PDE is much lower than 100%.

The Single Photon Avalanche Diode (SPAD) integrated in a waveguide fabricated in the silicon layer will overcome the tradeoff between high PDE and low temporal resolution. This is accomplished by forcing the light to propagate orthogonal to the electric field. This increases the absorption efficiency by allowing the detector to have a greater length without increasing the distance travelled by photo-generated carriers. These detectors could reach a PDE as high as 70-80% in the near IR while maintaining a temporal jitter of about 35 ps. Also, the phase-matched coupling allows complete transport, and absorption, into the silicon photodetector layer within a length of 40-50 µm as well as having low noise and low parasitic capacitance.

The process for fabrication of passive structures for testing the vertical coupling between silicon nitride and silicon has been developed throughout this project. Within the course of the project, we found it necessary to planarize our structures as will be discussed later. Processes such as chemical mechanical planarization (CMP) and wet thermal oxidation have been utilized in the microelectronics industry for years. However, these processes remain delicate and have limitations to consider. CMP is limited by wafer bow, warp, and curvature. Each of these characteristics is affected by various wafer processing methods such as thin film depositions or etching [8]. Instead, we develop a recipe based on an interplay between hard masking, partial etching, and thermal oxidation to achieve a CMP-less planarization method.
2.1 Maxwell’s Equations

Maxwell’s equations are essential to understanding the behavior of electromagnetic waves. These equations contain Gauss’s law for electricity, Gauss’ law for magnetism, Faraday’s law of induction, and Ampere’s law. These basic laws are represented in derivative form by the equations

\[ \nabla \cdot \vec{D} = \rho, \quad (2.1) \]
\[ \nabla \cdot \vec{B} = 0, \quad (2.2) \]
\[ \nabla \times \vec{E} = -\frac{\partial \vec{B}}{\partial t}, \quad (2.3) \]
\[ \nabla \times \vec{H} = \vec{J} + \frac{\partial \vec{D}}{\partial t}, \quad (2.4) \]

where \( \vec{D} \) is the electric flux density, \( \rho \) is the charge density, \( \vec{B} \) is the magnetic flux density, \( \vec{E} \) is the electric field amplitude, \( \vec{H} \) is the magnetic field amplitude, and \( \vec{J} \) is the current density. The electric flux density and magnetic flux density are related to the electric field amplitude and magnetic field amplitude in a linear, isotropic media by
where \( \varepsilon \) is the electric permittivity, and \( \mu \) is the magnetic permeability. A linear medium implies that the permittivity, \( \varepsilon \), and the permeability, \( \mu \), are independent of the electric and magnetic field amplitudes.

These equations can be combined to provide a second-order linear partial differential equation that describes the behavior of waves. If we assume that we are operating in a source free, linear, and isotropic medium then \( \rho = 0, J = 0 \), and \( \varepsilon \) and \( \mu \) are independent of \( \vec{E} \) and \( \vec{H} \). Now, Maxwell’s equations become

\[
\nabla \cdot \vec{D} = 0 ,
\]

\[
\nabla \cdot \vec{B} = 0 ,
\]

\[
\nabla \times \vec{E} = \frac{\partial \vec{B}}{\partial t} ,
\]

\[
\nabla \times \vec{H} = \frac{\partial \vec{D}}{\partial t} .
\]

The wave equation is found by taking the curl of Faraday’s law.

\[
\nabla \times \nabla \times \vec{E} = \nabla \times \left( \frac{\partial \vec{B}}{\partial t} \right) = \nabla \times \frac{\partial \vec{B}}{\partial t} .
\]

Substituting equation 6 into equation 11 we get

\[
\nabla \times \nabla \times \vec{E} = -\mu \left( \nabla \times \frac{\partial \vec{H}}{\partial t} \right) .
\]
Due to the continuous property of the functions the time derivative can be moved to the outside of the equation giving

$$\nabla \times \nabla \times \vec{E} = -\mu \frac{\partial}{\partial t} \left( \nabla \times \vec{H} \right).$$

(2.13)

We can now substitute equation 10 into equation 13 to get

$$\nabla \times \nabla \times \vec{E} = -\mu \frac{\partial}{\partial t} \left( \frac{\partial \vec{D}}{\partial t} \right) = -\mu \frac{\partial}{\partial t} \left( \frac{\partial \varepsilon \vec{E}}{\partial t} \right) = -\mu \varepsilon \frac{\partial^2 \vec{E}}{\partial t^2}.$$  

(2.14)

The left side of equation 14 can be simplified using the vector identity

$$\nabla \times \nabla \times \vec{E} = \nabla (\nabla \cdot \vec{E}) - \nabla^2 \vec{E}.$$  

(2.15)

Substituting equation 15 into equation 14 gives us

$$\nabla (\nabla \cdot \vec{E}) - \nabla^2 \vec{E} = -\mu \varepsilon \frac{\partial^2 \vec{E}}{\partial t^2}.$$  

(2.16)

We have stated that we are considering a spatially-uniform medium thus $\nabla \cdot \vec{E} = 0$ and equation 16 becomes the wave equation. The wave equation describes the propagation of electromagnetic waves. We are able to neglect $\nabla \cdot \vec{E}$ as long as the variation of $\varepsilon$ is not too strong, leading to the wave equation.

$$\nabla^2 \vec{E} - \mu \varepsilon \frac{\partial^2 \vec{E}}{\partial t^2} = 0.$$  

(2.17)

There are many solutions to the wave equation. However, we will only discuss the plane wave solution. Plane waves are constant-frequency waves with wavefronts that are infinite in parallel planes and have constant peak-to-peak amplitudes normal to the direction of propagation. Plane waves can be represented as the arbitrary functions
\[ \vec{E} = \hat{x} [f_+(z - vt) + f_-(z + vt)], \]  
(2.18) \[ \vec{H} = \hat{y} \sqrt{\frac{\varepsilon}{\mu}} [f_+(z - vt) + f_-(z + vt)], \]  
(2.19)

where \( \hat{x} \) and \( \hat{y} \) are unit vectors in the x-y directions of the Cartesian coordinate system,  
\( f_+ \) and \( f_- \) are propagating in the \( +\hat{z} \) and \( -\hat{z} \) directions, and \( v = \frac{1}{\sqrt{\varepsilon \mu}} \) is the velocity of the wave in a medium. We know that \( \vec{E} \) and \( \vec{H} \) are perpendicular because \( \nabla \cdot \vec{E} = 0 \) and \( \nabla \cdot \vec{H} = 0 \). To prove that these functions satisfy the wave equation we let \( E = \hat{x} f(z,t) \). 

By substituting this value into equation 17 we see 
\[ \frac{\partial^2 f}{\partial z^2} = \mu \varepsilon \frac{\partial^2 f}{\partial t^2} = \frac{1}{v^2} \frac{\partial^2 f}{\partial t^2}. \]  
(2.20) 

This can now be factored to show that 
\[ \left( \frac{\partial f}{\partial z} - \frac{1}{v} \frac{\partial f}{\partial t} \right) \left( \frac{\partial f}{\partial t} + \frac{1}{v} \frac{\partial f}{\partial t} \right) = 0. \]  
(2.21) 

The left hand side of the product can be solved by any plane wave function \( f_- (z + vt) \) and the right hand side can be solved by \( f_+ (z + vt) \). This can be proved by letting \( \alpha = z - vt \) and using the chain rule. 
\[ \frac{\partial f}{\partial z} = \frac{\partial \alpha}{\partial z} \frac{\partial f}{\partial \alpha} = \frac{\partial f}{\partial \alpha}, \]  
(2.22) \[ \frac{\partial f}{\partial t} = \frac{\partial \alpha}{\partial t} \frac{\partial f}{\partial \alpha} = -v \frac{\partial f}{\partial \alpha}. \]  
(2.23) 

By substituting equations 22 and 23 into equation 21 the right hand side of the product comes to zero. The same method can be used to show that letting \( \alpha = z + vt \) is also a
solution. A combination of forward and backward propagating plane waves satisfies the wave equation. The same procedure can also be used to show that $\vec{H}$ also has a plane wave solution.

The above solution to the wave equation shows how a plane wave propagates. The measure of the power flowing through a surface can be represented by the equation

$$\vec{S} = \vec{E} \times \vec{H}.$$  \hfill (2.24)

This is known as the Poynting vector. The Poynting vector points in the direction of the power flow and describes the instantaneous intensity of the wave. It is also orthogonal to $\vec{E}$ and $\vec{H}$. It is important to remember that electromagnetic waves have both real and imaginary components. The imaginary components must be considered to find the complete description of the wave.

To better describe electromagnetic waves we consider the complex form of Maxwell’s equations.

$$\nabla \cdot \varepsilon \vec{E} = \rho,$$  \hfill (2.25)

$$\nabla \cdot \mu \vec{H} = 0,$$  \hfill (2.26)

$$\nabla \times \vec{E} = -j\omega \mu \vec{H},$$  \hfill (2.27)

$$\nabla \times \vec{H} = j\omega \varepsilon \vec{E} + \vec{J}.$$  \hfill (2.28)

By applying the same method used for the wave equation the Helmholtz wave equation in a spatially uniform medium can be derived.
\[ \nabla^2 \vec{E} + \omega^2 \mu e \vec{E} = 0. \] (2.29)

The Helmholtz equation can handle more complicated wave descriptions because \( \mu \) and \( \varepsilon \) can be functions of frequency \( \omega \). We can now construct plane wave solutions that propagate in the direction \( \vec{k} \), which is the propagation vector, and assume spatial dependence in the form of \( e^{-jk\vec{k} \cdot \vec{r}} \).

The \( \vec{E} \) field and \( \vec{H} \) field can now be described in complex vector notation with \( \vec{E}_+ \) and \( \vec{H}_+ \) representing complex vector amplitudes.

\[ \vec{E} = \vec{E}_+ e^{-jk\vec{k} \cdot \vec{r}} , \] (2.30)
\[ \vec{H} = \vec{H}_+ e^{-jk\vec{k} \cdot \vec{r}} . \] (2.31)

Plane waves must have a constant phase of \( \vec{E} \) and \( \vec{H} \) which means that \( \vec{k} \cdot \vec{r} = \text{constant} \). This will lead to the dispersion relation of a single-frequency plane wave. This relation is derived by replacing \( \nabla \times \) in equations 27 and 28 with \( -jk \times \) and curling both sides of equation 27.

\[ -jk \times (-jk \times \vec{E}_+) = -j\omega \mu (-jk \times \vec{H}_+) , \] (2.32)
\[ -\vec{k} \cdot (\vec{k} \cdot \vec{E}_+) + k^2 E = \omega^2 \mu e \vec{E}_+ . \] (2.33)

Similar to the previous derivations we let \( \vec{k} \cdot \vec{E}_+ = 0 \) and we get the dispersion relation.

\[ k^2 = \omega^2 \mu e . \] (2.34)
2.2 Reflection and Refraction

When two different media come into contact the wave solution must be connected at the boundaries of the interface. If there is a difference in the indices of refraction between the two media Fresnel reflection will occur. These boundary conditions are derived from Maxwell’s equations. Consider two source free, charge free, media. The electric field in medium 1 is \( \mathbf{E}_1 \) and the electric field in medium 2 is \( \mathbf{E}_2 \). The magnetic fields are similar being \( \mathbf{H}_1 \) and \( \mathbf{H}_2 \) for medium 1 and medium 2. For a wave that is crossing through the boundary of 1 and 2, generally, it is both reflected and refracted. Consider a transverse electric (TE) wave where the \( \mathbf{k} \) vector propagates from one medium to another with refractive indices of \( n_1 \) and \( n_2 \). The boundary conditions for a dielectric interface are [9]

\[
\hat{n} \times (\mathbf{E}_2 - \mathbf{E}_1) = 0, \tag{2.35}
\]

\[
\hat{n} \times (\mathbf{H}_2 - \mathbf{H}_1) = 0, \tag{2.36}
\]

\[
\hat{n} \cdot (\mu_2 \mathbf{H}_2 - \mu_1 \mathbf{H}_1) = 0, \tag{2.37}
\]

\[
\hat{n} \cdot (\varepsilon_2 \mathbf{E}_2 - \varepsilon_1 \mathbf{E}_1) = 0. \tag{2.38}
\]
In figure 2.1 $i$ represents the incident ray, $r$ represents the reflected ray, and $t$ represents the transmitted ray. These waves can be described as plane waves in complex notation by writing

$$\vec{E}_i = E_i \hat{x} e^{-jk_i \vec{r}},$$  \hspace{1cm} (2.39)$$

$$\vec{E}_r = E_r \hat{x} e^{-jk_r \vec{r}},$$  \hspace{1cm} (2.40)$$

$$\vec{E}_t = E_t \hat{x} e^{-jk_t \vec{r}}.$$  \hspace{1cm} (2.41)

Now it is useful to break the exponent into its component form.

$$\vec{k}_i \cdot \vec{r} = (z \cos \theta_i - y \sin \theta_i)k_o n_1,$$ \hspace{1cm} (2.42)$$

$$\vec{k}_r \cdot \vec{r} = (-z \cos \theta_r - y \sin \theta_r)k_o n_1,$$ \hspace{1cm} (2.43)$$

$$\vec{k}_t \cdot \vec{r} = (z \cos \theta_t - y \sin \theta_t)k_o n_2.$$ \hspace{1cm} (2.44)
The magnitude of the propagation vector is \(|\vec{k}| = k_{uo}\) with the subscript representing the material. The interaction at the boundary requires the continuity of the tangential electric field for any value of \(y\) at \(z = 0\). This means that the exponents must be equal for any value of \(y\) and thus \(\theta_i = \theta_r\) and Snell’s law is revealed.

\[
n_1 \sin \theta_i = n_2 \sin \theta_2 .
\]  

(2.45)

Figure 2.1 shows that if a ray enters a high index material it is refracted towards the normal. However, if a ray is propagating through a high index material and comes to a low index interface the ray will be refracted away from the normal. For high to low index propagation we know \(n_1 > n_2\) and the critical angle is defined when \(\theta_2 = 90^\circ\) [10]. In this case Snell’s law becomes \(n_1 \sin \theta_i = n_2 \sin 90^\circ\), where \(\theta_i = \theta_c\) and the equation for the critical angle is

\[
\theta_c = \sin^{-1} \left( \frac{n_2}{n_1} \right).
\]  

(2.46)

When investigating guided waves it is important to know the amplitudes being transmitted with the wave. Consider a TE wave. To find the amplitude of the transmitted electric field we consider the ratio of the initial and transmitted fields. This equation is derived knowing that there must be a continuity of magnitude. This means that the entire electric field must be accounted for with transmission and reflection.

\[
E_i + E_r = E_i .
\]  

(2.47)
It is also necessary to consider the magnetic boundary conditions to get $E_t$ in terms of $E_i$.

The continuity of tangential $\vec{H}$ requires that

$$\hat{\vec{z}} \times (\vec{H}_i + \vec{H}_r)|_{z=0} = \hat{\vec{z}} \times \vec{H}_t|_{z=0}. \tag{2.48}$$

By applying the same method as above we find that the cross products of the magnetic fields are

$$\hat{\vec{z}} \times \vec{H}_i = \left(-\hat{x}E_i \cos \theta / n_1\right) e^{-jk_0n_1(-y\sin(\theta))}, \tag{2.49}$$

$$\hat{\vec{z}} \times \vec{H}_r = \left(-\hat{x}E_r \cos \theta / n_2\right) e^{-jk_0n_2(-y\sin(\theta))}, \tag{2.50}$$

$$\hat{\vec{z}} \times \vec{H}_r = \left(+\hat{x}E_r \cos \theta / n_1\right) e^{-jk_0n_1(-y\sin(\theta))}. \tag{2.51}$$

By substituting these equations into equation 2.48 and performing some algebra the transmission and reflection amplitudes are found.

$$r_s = \frac{E_r}{E_i} = \frac{n_1 \cos \theta_i - n_2 \cos \theta}{n_1 \cos \theta_i + n_2 \cos \theta}, \tag{2.52}$$

$$t_s = \frac{E_t}{E_i} = \frac{2n_1 \cos \theta_i}{n_1 \cos \theta_i + n_2 \cos \theta}. \tag{2.53}$$

A similar method is used to find the amplitudes for a TM wave.

The propagation through a waveguide will be represented by the transmitted electric field. When propagating through a medium it is important to know the attenuation coefficient, $\gamma$, in 1/meters and the propagation coefficient, $\beta$, in radians/meter. To find these values consider the transmitted electric field of a TE wave.
\[ E_t = \varepsilon E_i e^{-j k_0 \sin \theta \sin \theta} \cos \theta, \quad (2.54) \]

where \( \tau = \frac{E_t}{E_i} \). We know from Snell’s law that \( \sin \theta_2 = \frac{n_1}{n_2} \sin \theta_1 \), and from Pythagorean identities \( \cos \theta_2 = \sqrt{1 - \frac{n_1^2}{n_2^2} \sin^2 \theta_1} \). If \( \theta_1 \) increases beyond the critical angle then \( \cos \theta_2 \) becomes imaginary which means the description of the transmitted electric field becomes

\[ E_t = \varepsilon E_i e^{-j k_0 \sin \theta \sin \theta} \cos \theta, \quad (2.55) \]

where

\[ \gamma = k_0 n_2 \sqrt{\frac{n_1^2}{n_2^2} \sin^2 \theta_1 - 1} \quad (2.56) \]

\[ \beta = k_0 n_1 \sin \theta_1. \quad (2.57) \]

This tells us that the field in the lower index medium travels parallel to the interface and decays exponentially in the normal direction [9].

2.3 Dielectric Waveguides

A planar slab waveguide consists of a high index dielectric material between two low index materials as shown in figure 2.3 to the right of the arrow. Generally, the bottom material is the substrate and the top material is the cladding. However, both materials can be considered cladding. In the case of a TE wave the electric field is in the \( -\hat{y} \) direction. If a monochromatic wave at frequency \( \omega_0 \), where \( k_0 = \frac{\omega_0}{c} \), is assumed then
the general solution is found by solving the Helmholtz equation, equation 2.29, in each region. Since the slab is infinite in \( \hat{y} \) there can be no dependence of \( E \) on \( \hat{y} \).

Additionally, translation invariance is assumed in the \( z \)-direction. Because of this it can be assumed that propagation in the \( \hat{z} \) direction only adds phase. Assuming a TE mode the wave can be described as

\[
E_y(x, z) = E_y(x)e^{-j\beta z}.
\]  

(2.58)

When this equation is substituted into the wave equation gives a one-dimensional equation.

\[
\frac{\partial^2 E_y}{\partial x^2} + (k_0^2 n_i^2 - \beta^2) E_y = 0.
\]  

(2.59)

The exponential term has been absorbed into \( E_y \). We see that equation 2.59 can result in either a decaying exponential or a sinusoidal term depending on the value of \( \beta \). If \( \beta > k_0 n_i \) then the solution is a decaying exponential. If \( \beta < k_0 n_i \) the solution is a sinusoidal and represents propagation through the material. To see a confined mode in a planar slab waveguide, and to solve a rectangular dielectric waveguide problem using the effective index method, the solution must exponentially decay for \( n_s \) and \( n_c \) while oscillating as a sinusoid for \( n_g \). This leads to an evanescent wave solution in the substrate and cladding with a confined oscillating solution in the guiding layer. The fields are described by the equations

\[
E_y(x) = Ae^{-\gamma x}, \quad x > 0,
\]  

(2.60)
\( E_y(x) = B \cos(\kappa_f x) + C \sin(\kappa_f x) \quad -h < x < 0, \quad (2.61) \)

\( E_y(x) = D e^{\gamma_s (x+h)} \quad x < -h, \quad (2.62) \)

where \( \gamma_c \) and \( \gamma_s \) are the attenuation coefficients in the cladding and substrate, and \( \kappa_f \) is the transverse propagation wavevector in the guiding layer. A, B, C, and D are amplitude constants determined by the boundary conditions. The boundary conditions applied are the continuity of the tangential components of \( \vec{E} \) and \( \vec{H} \). The tangential \( \vec{H} \) is found using the complex representation of Maxwell’s equations. The amplitude constants are found by investigating the structure at the interfaces and substituting the values of \( x = 0 \) and \( x = -h \). Making these substitutions allow equations 2.60, 2.61, 2.62, to be written in terms of the normalizing constant A which depends on the power in the wave.

\( E_y(x) = A e^{-\gamma_c x} \quad x > 0, \quad (2.63) \)

\( E_y(x) = A \left[ \cos(\kappa_f x) - \frac{\gamma_c}{\kappa_f} \sin(\kappa_f x) \right] \quad -h < x < 0, \quad (2.64) \)

\( E_y(x) = A \left[ \cos(\kappa_f h) - \frac{\gamma_c}{\kappa_f} \sin(\kappa_f h) \right] e^{\gamma_s (x+h)} \quad x < -h. \quad (2.65) \)

Finally, applying the remaining boundary condition of the continuity of the derivative of the electric field, \( \frac{\partial E_y}{\partial x} \big|_{x=-h} \), a transcendental equation is revealed. At \( x = -h \) we set the derivatives of equations 2.64 and 2.65 equal to each other and divide both sides by \( \cos(\kappa_f h) \) returning the transcendental equation
\[
\tan(h\kappa_f) = \frac{\gamma_c + \gamma_s}{\kappa_f \left[ 1 - \frac{\gamma_c \gamma_s}{\kappa_f^2} \right]},
\]  (2.66)

Equation 2.66 is solved numerically by plotting one side at a time. The solution is found at the crossing of the two sides of the equation. The solution to this equation is the longitudinal wavevector \( \beta \). A similar equation can be derived for the TM mode.

\[
\tan(h\kappa_f) = \frac{\kappa_f \left[ \frac{n_g^2 \gamma_s}{n_s} + \frac{n_g^2}{n_c^2} \gamma_c \right]}{\kappa_f^2 - \frac{n_g^2}{n_c n_s^2} \gamma_c \gamma_s},
\]  (2.67)

For rectangular dielectric waveguides we must consider both the \( x \) and \( y \) components of the light traveling in the \( z \)-direction. In many cases one of the two components, \( E_x \) or \( E_y \), dominates over the other. If we know which field is dominant we may assume the other to be zero. This semi-vectorial approximation allows for a much simpler equation to describe the rectangular waveguide. As well as using the semi-vectorial approximation we can consider the condition that \( \Delta n \approx 0 \). This allows the condition on the normal electric field to be ignored. This is subject to the condition that the electric field and its derivatives are continuous across all interfaces. This is known as the scalar field approximation and gives very accurate results for \( \beta(\omega) \), and \( n_{\text{eff}}(\omega) \) as long as we operate away from the cut-off frequency.
The effective index method is a very powerful method that yields accurate results for the propagation constants. This is especially true when one of the dimensions of the waveguide is large.

Figure 2.2: Different type of rectangular dielectric waveguides. In a) the top surface is exposed to air, b) shows lateral confinement due to the top ridge, and c) is a waveguide completely encased by the cladding.

The design of the waveguide will have a significant impact on how the wave is guided through the medium. This is because we have to examine the entire layout separately as shown below in figure 2.3.

Figure 2.3: The effective index method is implemented by considering the indices of refraction as if they were two planar slab wave guides.
We first consider the waveguide to be infinitely long. Then the effective index is calculated for one orientation, and then treat the problem as a slab waveguide in the other direction using the effective index. The value of $\beta$ calculated in the first step is the actual value for the mode. The type of mode, TE or TM, must be taken into account when setting up the effective index method. If the mode is an $E_1$ mode then it will look like a TM mode in the first step, and then a TE mode in the second step. This approximation is effective away from the cut-off, but it is not capable of describing the spatial structure of the mode.

2.4 Coupled Mode Theory

There are many structures that can lead to coupled waveguides and coupled modes. We will discuss degenerate mode coupling. Degenerate modes possess equal propagation constants $\beta$ and their polarization states will propagate unchanged. We will consider a structure with two waveguides separated by a distance $2a$ and with widths of $2b$. This is depicted in figure 2.4.
Figure 2.4: A directional coupler consisting of two waveguides silicon nitride waveguides in a silicon dioxide cladding separated by a distance 2a and with widths of 2b.

The distance a must be relatively small because the polarization perturbation in waveguide B is caused by the evanescent field from waveguide A. The energy can tunnel from one waveguide to the other through the evanescent tail in the cladding. We also assume that these are single mode structures. The symmetry of these structures allow the propagating wave to oscillate from waveguide to waveguide freely. We would expect the fields in the guiding layers of ideal waveguides to be

\[
E_A(x, y, z) = A \cos(\kappa_x x + \phi_x) \cos(\kappa_y (y + (a + b))) e^{-j\beta z}, \quad (2.68)
\]

\[
E_B(x, y, z) = B \cos(\kappa_x x + \phi_x) \cos(\kappa_y (y - (a + b))) e^{-j\beta z}, \quad (2.69)
\]

Where the transverse and longitudinal wavevectors \( \kappa_x, \kappa_y \), and \( \beta \) are equal for both waveguides. The perturbation in waveguide B comes from the discontinuity the evanescent field see between the core of waveguide B and the cladding. The polarization perturbation acts as an extra source which excites the mode in waveguide B. This leads to the perturbation being represented as
\[ P(x, y, z) = \varepsilon_0 (n_1^2(x, y) - n_2^2) E_A(x, y) \]

\[ = \varepsilon_0 (n_1^2(x, y) - n_2^2) \left[ \frac{A}{2} e_A(y) e^{-j(\beta z - \omega t)} \right]. \quad (2.70) \]

We are working with directional couplers so there is no need to include a term for backwards propagating waves. It also turns out that phase matching prevents energy from coupling backwards between waveguides. Now it is necessary to find the relationship between the amplitudes \( A \) and \( B \) in equations 2.68 and 2.69. This is done by solving the equation of motion for \( B \).

\[
\frac{\partial B}{\partial z} e^{-j(\beta z - \omega t)} + \text{c.c.} = -\frac{j}{2 \omega} \frac{\partial^2}{\partial t^2} \iint_S e_B(x, y) P_{perp} dS,
\]

\[
\frac{\partial B}{\partial z} e^{-j(\beta z - \omega t)} = jK A e^{-j(\beta z - \omega t)}, \quad (2.71)
\]

where \( K = \frac{\omega}{4} = \iint \varepsilon_0 (n_2(x, y) - n_1^2) e_B(x, y) e_A(x, y) dx dy \). In this case the waveguides are symmetric. Due to this symmetric coupling between waveguides we can write an equivalent coupling equation for the field amplitude transferring from waveguide B to A.

\[
\frac{\partial A}{\partial z} e^{-j(\beta z - \omega t)} = jKB e^{-j(\beta z - \omega t)}.
\]

Again, due to symmetry and identical propagation constants we can drop the exponential terms in equations 2.71 and 2.72. At this point these equations are strongly coupled. In order to uncouple them the derivative of 2.72 is solved and substituted into equation 2.72. This simple calculation leads to an uncoupled second order differential equation [11].

\[
\frac{\partial^2 A}{\partial z^2} = -K^2 A. \quad (2.73)
\]
If we assume the field is located completely within waveguide A initially then the initial conditions become $A(0) = 1$, and $B(0) = 0$. Equation 2.73 then gives us sinusoidal functions for both $A(z)$ and $B(z)$.

$$A(z) = \cos(Kz),$$

$$B(z) = -jsin(Kz).$$

This is an ideal model which shows that 100% transfer efficiency is being achieved. There is also a $90^\circ$ phase difference between the driving and driven field. As it turns out the driven field always lags the initial driving field by $90^\circ$. “When polarization leads the field, the polarization does work on the field, and effectively increases the amplitude of the field. Likewise, when the material polarization lags the field, the field does work on the material, and dissipation of the field occurs” [9].

If waveguide A is the initially excited waveguide then the transfer of the energy from waveguide A to waveguide B will occur until waveguide A is void of all energy. Once all the energy has been transferred from waveguide A to waveguide B the second transfer can occur. All energy will then couple into waveguide A from waveguide B until waveguide B is void of all energy. It is also due to the leading and lagging phase relation that no energy is transferred in the backwards direction.
CHAPTER 3
NANOFABRICATION THEORY

3.1 Silicon on Insulator

The photo detector device is fabricated on a SOITEC silicon on insulator (SOI) substrate [6]. The SOI begins as a standard silicon wafer and is then thermally oxidized. The oxidized wafer has hydrogen atoms implanted on its backside. The implantation allows the wafer bonding of a new silicon wafer on the backside to act as the substrate. The top of the wafer is then cut, to remove the oxide, annealed and polished to the desired parameters.

3.2 Photolithography

Standard fabrication techniques include photolithography, chemical vapor deposition (CVD), physical vapor deposition (PVD), dry etch, and wet chemical etch. For this project plasma enhanced CVD (PECVD), low pressure CVD (LPCVD), and thermal oxidation were used for depositions of thin films. The removal of materials occurred using a reactive ion etch (RIE), wet chemical etch, and chemical mechanical planarization (CMP). The process discussed here are based largely from descriptions provided in [14].
Photoresist is a UV sensitive organic polymer with three components. These components are a solvent, photoactive compound, and resin. The purpose of the solvent is to allow the photoactive compound and resin to be applied in liquid form. This liquid form is necessary due to the main method of application being spin coating. Spin coating plays a critical role in the resolution of capabilities of photolithography. Once the resist is applied it is exposed. The exposure process consists of exposing the resist to UV light. This will activate the photoactive compound and make the resist more soluble to developers. This allows the use of masks to pattern the resist and fabricate devices.

The application of the photoresist is the first of four stages of spin coating. To spin coat a wafer or piece of a sample is place on a chuck and a vacuum holds the sample to the chuck. The photoresist is then applied to the wafer using a pipette. In the second stage the substrate is accelerated. This allows the fluid to flow toward the edges of the substrate and wet the entire surface. This acceleration produces a tangential force in the fluid, and the rotation produces a centrifugal force in the fluid. This produces a spiral pattern toward the edge of the wafer. Stage three is the thin out stage. This stage begins when the velocity comes to its maximum and is held constant. Because there is no acceleration, there is no tangential force. This means that the centrifugal force produces a radial flow of the resist outward. Eventually, the resist will reach its final thickness which is dependent on the viscosity of the resist and final speed of the spin [12,13,14]]. This is shown in equation 3.1 below.

\[
h = \frac{h_0}{\left(1 + \frac{4 \rho \omega^2 h_0^2 t}{3 \eta} \right)^{1/2}}. \tag{3.1}
\]
Here $h_0$ is the initial thickness of the resist, $\rho$ is the density of the resist, $\omega$ is the angular frequency, $t$ is time, and $\eta$ is the viscosity of the resist. For this project we spin the 955 photoresist at 2000 rpm for 45 seconds. This results in about a 1.2 $\mu$m resist thickness. Now, we can consider our photo resist that will have the following parameters. The specific gravity of the photoresist is 1.08, the film thickness after a 30-second spin is 1.3 $\mu$m, and the viscosity is $\eta = 0.05004 \frac{g}{cm \cdot sec}$. This will allow us to investigate the final thickness of the resist relative to the angular frequency or the initial height. These are shown below in figures 3.1 and 3.2. We can see that even around 8000 RPM the thickness is not much smaller than at 6000 RPM. This shows a limit to how thin the resist can be applied by spin coating. The final stage is the evaporation stage. This is where the substrate is put onto a hot plate and the excess solvent is evaporated from the sample. The solvent is only necessary for the application of the resist. Once the resist is applied the excess solvent can be evaporated which results in a slightly thinner resist.

It is sometimes necessary to apply HMDS Organosilane prior to the spin coating of photoresists. The surface energy of the substrate, or of the material the resist is adhering to, largely determines the lateral diffusion of the developer. This surface energy determines the adhesion of the photoresist to the substrate. This adhesion will determine if the photoresist will remain on the substrate during development or potentially be undercut and lifted off by the photoresist developer. The HMDS essentially takes a hydrophilic surface and makes it hydrophobic. This means that aqueous solutions will tend to stay together rather than spread thin across the substrate [14].

26
Figure 3.1: On the left we see the final thickness of photoresist spun at 2000 RPM over time. The initial thickness is varied, but we see over time the final thickness is limited. The plot on the right shows the final resist thickness as a function of acceleration and spun for 30 seconds. We see that the acceleration of the substrate plays a role in the how quickly the minimum thickness is reached, but again is limited by the resist properties.

The resolution of features on the device depend heavily on diffraction through the resist and the exposure time. Contact mask lithography is where you take your sample and press it against a mask that has a pattern on it. The mask used for the photodetector devices is shown below.
The mask has an array of 10 mm chips with 3, 5, 10, and 20 micron wide patterns that are all 100 microns long. This pattern will allow UV light through some portions of the mask but not others. Because of the photoactive compound of the resist the exposed areas of the resist will react differently depending on the tone of the resist. If the tone is positive the exposed areas will become more soluble to developers. If the tone is negative the resist will become less soluble.

In contact mask lithography the sample is pressed against the mask and exposed to UV light. Because the sample can only get as close as the smallest particle, or as close as the mask is thick if the particles are negligible, there will certainly be diffraction. The resolution limit of contact mask lithography is

\[ D_{\min} = 2\sqrt{\frac{z}{\lambda}} , \]  

(3.2)
$D_{\text{min}}$ is the minimum diameter of the aperture [14]. Equation 3.2 is necessary due to the diffraction caused by the edges of the pattern on the mask. Because we are dealing with micron distances we must consider Fresnel (near field) diffraction. The equation above comes from the Fresnel integrals for a circular aperture. This produces a target pattern where $\rho$ is the radius of each zone. Each zone is measured from the center of the target to the edge of the positive part of the pattern. This is shown below.

![Figure 3.3: Example of Fresnel Zones][1]

The radius of the Fresnel zone can be written as $\rho^2 = \lambda z$ where $\lambda$ is the wavelength, and $z$ is the distance between the aperture and the point. We can consider the radius of the zone plate to be the radius of the aperture and get equation 3.2. If the distance between the aperture and sample increases, then the aperture size increases as well. This is due to the diffraction at the edges of the features of the mask. So, as $z$ increases with a thicker photoresist, or a particle on the sample, the resolution becomes worse.
Exposure also plays a role in the resolution of photolithography. This is because light is not a step function. The intensity of the UV rays are not either 1 or 0. They have a diffused profile, and thus have wings. This means that most of the exposure is happening in the areas of the mask that are not covered, but some of the overflow is slowly exposing the area underneath the mask. This means that if a positive resist is over exposed, the features will become smaller. They will also be less sharp due to diffraction.

Figure 3. 4: The image on the left is the photoresist pattern for the 10 μm wide silicon pad. On the right the alignment markers to allow the e-beam lithography step to be aligned.

3.3 Deposition Processes

Chemical vapor deposition (CVD) is a method of depositing solid films from their gas forms [16]. CVD relies on the chemical reaction of gases with each other. The CVD method results in a conformal film whereas a physical vapor deposition (PVD) is line of sight. The conformal nature of CVD means that the side walls will be coated as well as the horizontal surface of the sample. Sputter deposition and electron beam evaporation are two common types of PVD. Sputtering generates a plasma and bombards a target with ions to break away pieces of the desired material to leave a thin film on the
substrate. Electron beam evaporation focuses an electron beam onto the target and heats the target material to its vaporization point. This causes the target material to evaporate and deposit onto the mounted substrate. Neither of these PVD process are used for the fabrication of this photodetector device.

Figure 3. 5: The top image the isotropic CVD coats the vertical and horizontal surfaces of the sample. The bottom image shows the line of sight PVD coats only the horizontal surfaces of the sample.

The isotropic nature of CVD can be desirable for certain applications such as planarization, passivation, and insulation [1]. This isotropic property is due to the diffusion of the gases used in the CVD process. One drawback of CVD is that it requires high temperatures to be applied to the substrate. The higher temperature substrate provides a greater difference between gas phase reactions and reactions on the substrate. If gas phase reactions are occurring they will provide a line of site deposition similar to PVD.

The gas phase and substrate reactions can be controlled by varying the pressure and dilution of the gas within the chamber. There are two limiting rates for CVD. These
limiters are "The diffusion rate of the reaction through the stagnant boundary layer; and the surface reaction rate. The smaller of the two will limit the overall reaction rate" [13]. A stagnant boundary layer can be found on all surfaces. This is a layer where gas will not flow, and any deposition that occurs will occur due to diffusion through the layer. The thickness of the stagnant boundary varies with respect to pressure and flow velocities and is represented by the equation below.

\[ \Delta \propto \frac{1}{\sqrt{vP}}, \]  

(3.3)

where \( \Delta \) is the stagnant boundary thickness, \( v \) is the flow velocity, and \( P \) is the pressure.

The diffusivity \( D \) varies with respect to the temperature \( T \) and pressure as

\[ D \propto \frac{T^{3/2}}{P}. \]  

(3.4)

The diffusion conductance is described as

\[ h_g = \frac{D}{\Delta} = \frac{D_0}{\Delta_0} T^{3/2} \sqrt{\frac{v}{P_g}}. \]  

(3.5)

The surface reaction rate is \( J_s = k_s P_s \) and has the following exponential relationship with temperature.

\[ k_s = A e^{-\left(\frac{E_a}{kT}\right)}, \]  

(3.6)

where \( E_a \) is the activation energy of the reaction.
It is convenient to represent equations 3.5 and 3.6 in their inverse forms. The
diffusion resistance is expressed as $\frac{1}{h_g}$ and similarly the reaction resistance is $\frac{1}{k_s}$. By
considering these resistances we can express three limitations. First is the case that $h_g$ is
greater than $k_s$. This means that the reaction rate is determined only by the diffusion
resistance. Second, if $k_s$ is greater than $h_g$ then the reaction rate is determined by the
reaction resistance. Third, if $k_s = h_g$ we get a transition point from the diffusion-limited
case to the reaction limited case.

Low pressure chemical vapor deposition (LPCVD) is a common CVD technique
that is utilized throughout this process. If we consider the ratio of $\frac{k_s}{h_g}$ and set it equal to 1
Torr we can solve for the substrate temperature necessary for the reactions to occur on
the substrate rather than having gas phase reactions.

\[
\frac{k_s}{h_g} = \frac{Ae^{-\frac{E_a}{kT}}}{D_0 \frac{T^{\gamma/2}}{\Lambda_0 \sqrt{P_g}}}, \quad (3.7)
\]

For silane (SiH$_4$) and oxygen (O$_2$) the necessary substrate temperature would be about
1500° C. If we lower the temperature to accommodate the heat threshold of the substrate
then we decrease $h_g$ and increase $k_s$. This leads to the reaction rate being managed by

\[
J_s \approx k_s P_g = Ae^{-\frac{E_a}{kT}} P_g,
\]

where $J_s$ is the gas flow. 1500° C is too hot for many substrates
and so often the furnace it turned down to around 1000° C. At this temperature the
primary factors affecting the reaction rate are temperature and pressure. For the LPCVD Si$_3$N$_4$ deposition of this project the furnace is set at 850° C.

There are several benefits to using LPCVD methods. It is necessary in our case due to the need for high quality Si$_3$N$_4$. LPCVD results in a high quality and sturdy film. These films aren’t cracked which results in better propagation when used as optical waveguides. The attenuation for these LPCVD nitride films can be on the order of 0.1 dB/cm for zeroth order modes [4]. The films are also denser allowing them to survive longer exposure to high temperatures and gases. For example less of the LPCVD silicon nitride will be converted into oxynitride during the thermal oxidation process than PECVD nitride.

In order to lower the temperature, and to accommodate various materials that have lower temperature thresholds, a plasma can be introduced. This allows for a similar film quality to be deposited at a lower temperature. The parallel plate configuration is the most common PECVD design. An anode and cathode are placed in parallel to each other and the substrate is set on the anode. The pressure is brought down to about 1 Torr. This is similar to the LPCVD process, but the substrate temperature is only raised to about 300° C. By introducing the RF plasma the electron temperature of the gas rises to thousands of degrees C [14]. The plasma decomposes the gas, dislodging electrons, and allowing atoms with unpaired electrons to react with each other. The benefit of lower temperature comes with consequences. The lower temperature allows by products of gases to remain in the chamber and produce deformities. For example silane based reactions contain excess hydrogen, and due to the low temperature the hydrogen won't completely desorb.
The PECVD silicon nitride is a silane based process and thus has excess hydrogen in the deposited film. This hydrogen decreases the quality of the nitride film. Not only is the PECVD film less dense, which can lead to cracking, but the hydrogen leads to higher attenuation due to absorption of the guided waves. Studies have shown that PECVD nitride is hard to use as waveguides and guided modes can struggle to launch into the films [4,17].

Dry thermal oxidation is the process of producing a layer of oxide on a silicon substrate [14,18]. For our purpose we are producing silicon dioxide from single crystal 100 silicon. This is achieved by exposing a silicon substrate to a high temperature, about 1150° C, and introducing oxygen into the furnace in a time-controlled manner. The extreme temperature in the furnace causes the oxygen to diffuse into the top layers of the silicon wafer and react with the silicon. This produces a dense, high quality thermal oxide. However, dry thermal oxidation is a long process. In order to grow 500 nm of oxide from a silicon substrate takes about 9 hours in a furnace at 1150° C. The growth rate is described by the Deal-Grove Model first published by Bruce Deal and Andrew Grove of Fairchild Semiconductor in 1965 [18]. This model assumes that oxygen diffuses from the bulk of the ambient gas to the surface, through the existing oxide layer, and reacts with the substrate. The chemical reaction for dry oxidation is exactly as expected.

\[ \text{Si} + \text{O}_2 \rightarrow \text{SiO}_2 \]

To reduce this time it is possible to expose the silicon substrate to water vapor instead of dry oxygen. This is called wet thermal oxidation and results in a much quicker
growth. This oxidation takes place in the same furnace as a dry oxidation, but there is a beaker of water mounted to it. The beaker has three openings: A gas input, a water input, and a vapor output. First the water is heated to 80° C to produce water vapor. The water is then bubbled with nitrogen gas. The nitrogen gas helps the water vapor exit the beaker and enter into the furnace. The steam increases the reaction between the silicon substrate and wet oxygen. This method reduces the oxidation time from 9 hours to 28 minutes [14].

\[
\text{Si} + 2\text{H}_2\text{O} \rightarrow \text{SiO}_2 + 2\text{H}_2
\]

3.4 Chemical Mechanical Planarization

Chemical mechanical planarization (CMP) polishing is used frequently in the microelectronics industry [19,20]. This process removes features from the surface of a substrate. CMP is a mixture of mechanical polishing and chemical etching. A chemical slurry is applied to the surface while the sample is polished by a polishing pad. In order to achieve planarization both the chemical and mechanical properties must be utilized. Chemical etching is isotropic in nature and can never achieve a planar surface because of this. Mechanical removal of materials can lead to a planar surface. However, there is high surface damage related to surface grinding and polishing. The combination of the CMP process allows for a smooth, planar, and low damage surface. A common CMP process is the damascene process. This process occurs several steps into complementary metal-oxide semiconductor (CMOS) or micro-electro-mechanical system (MEMS) fabrication processes. Due to the many depositions and etches that occur in these processes the surface will accumulate topography over time. Typically copper or aluminum is deposited over the topography and a CMP process is used to planarize the copper or aluminum layer.
There are a few limitations to the CMP process as it is relatively new to the industry. One complication is measuring the amount of material removed. Because planarization is the goal there are no steps to reference. This means that blind polishing based purely on the estimated removal rate is necessary. Another limitation is related to the bow, curvature, and warp of the samples [20]. Every processing step will add some sort of stress or strain to the substrate that will result in some type of bow or curvature.

Figure 3.6: A 3 inch silicon wafer with no processing done measured by a Zygo white light interferometer. We see that there is already bow and warp to the wafer before any processes have taken place.

Figure 3.6 shows a clean silicon wafer measured by a Zygo white light interferometer\(^1\). Due to the short coherence length of white light the surface of the wafer can be analyzed using the interference fringes of the white light. The wafer has been through no processing. We can see that even a pristine clean silicon wafer has some bow and warp [21]. Now if we cleave the wafer we can see that the bow and warp is still apparent in the 25cm by 25cm pieces. Figures 3.7 and 3.8 show two different pieces of the silicon wafers

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\(^1\) Zygo white light interferometer is located at AFRL.
surface profiles. Again we see that there is bow, curvature and warp apparent in these samples.

![Figure 3. 7](image1.png)

**Figure 3. 7:** The Zygo surface profile of one of the pieces of a cleaved silicon wafer. We can see a linear profile on the right that shows the curvature of that slice.

![Figure 3. 8](image2.png)

**Figure 3. 8:** The Zygo surface profile of a second piece of the previously mentioned 3 inch silicon wafer. With this piece we see a different curvature and warp from the first piece.

### 3.5 Etching Processes

The two most common types of etching are wet chemical and plasma etching. Wet chemical etching is a very simple concept. A material is placed in a chemical bath, and the chemical will react with that material. Typically, a wafer is patterned with a photoresist and submerged into a chemical bath. The chemicals are allowed to work their way through the openings in the resist and to react with the underlying material. This is a
convenient method because of the scalability of the bath. Many wafers can be loaded into a carrier and etched simultaneously. However, because the chemicals are fluid they etch equally in all directions. This isotropic etch could be undesirable and lead to undercutting of the photoresist or hard masks. This isotropic etch is shown below in figure 3.9. We see the etch is bowl shaped and lacks sharp vertical side walls that are often desired, especially in wave guide fabrication.

There are three general requirements that result in a good chemical etch. First the chemical must etch the material of interest at a reasonable rate. Second the chemical must not significantly attack the photoresist or masking material. Third the chemical must not etch the underlying substrate or other materials on the substrate. The ratio of the etch rate of the film and the other materials on the sample is known as the selectivity of the etchant.

\[
\text{Selectivity} = \frac{\text{Etch Rate of the Film}}{\text{Etch Rate of other Materials}}. \tag{3.8}
\]

The high selectivity is one of the benefits of wet chemical etching over plasma etching. Another advantage is the low damage to the surface because there are no ions or energetic particles bombarding the wafer [14]. A concern with chemical etching is that mask deterioration can occur. The photoresist or hard mask could have pinholes or cracks throughout the layer that allow the chemical to seep to the underlying material. This can result in unwanted etching due to the isotropic nature of the wet chemical etch.
Figure 3. 9: A typical cross section of a wet chemical etch. Due to the isotropic nature of this etch the removed area is shaped like a bowl.

Figure 3. 10: Chemical vapor deposition and etching with the volatile and nonvolatile reactions demonstrated.

Plasma enhanced chemical vapor processes can lead to deposition or etching. In fact both deposition and etching occur during PECVD and RIE processes. Both processes utilize RF source, gas mixtures, and plasma. It is the balance between the two processes that results in a final deposition or etch. If nonvolatile production rates exceed the volatile production then the process will be considered a deposition.
Within the plasma there will be ions, free radicals, and unexcited feed gas molecules. Only a small fraction of the gas will be ions and free radicals. However, there will be a greater amount of free radicals due to their longer lifetimes and lower dissociative energies. The positive ions are necessary to bombard the cathode and release secondary electrons. These electrons sustain the plasma. The ions bombarding the cathode can result in etching of the substrate. However, due to the small number of ions compared to free radicals they are not the primary source of removal.

Figure 3.11: The positive ions bombard the substrate and cathode releasing secondary electrons to sustain the plasma and slowly sputter the sample. Neutral free radicals react and chemically etch the substrate.

The result of using a heavy, nonreactive gas such as argon is a purely mechanical etch due to the bombardment of the ions into the substrate. Due to argon being nonreactive there will be no chemical etching which will result in an anisotropic etch. It is most common to use a gas that will result in free radicals and ions to sustain the plasma. This means that in most circumstances chemical etching occurs with some slight sputtering due to positive ions.
It turns out the bombardment can affect the chemical reaction between the free radicals and the substrate. The ions can loosen the substrate bonds resulting in a greater reactivity with the free radicals. The consequence of this being a reduction of the activation energy, $E_a$, which significantly increases the chemical etch rate. However, this increased etch rate only occurs on the horizontal surfaces being bombarded by the ions leave the vertical sidewalls unaffected. To increase the bombardment energy a higher DC bias is necessary, which is usually accompanied by an increase in RF discharge.

![Figure 3.12: An illustration of the expected nearly vertical sidewalls of an RIE process.](image)

Another plasma etching method is the inductive coupled plasma (ICP) process. The previously mentioned RIE etching utilized a parallel plate capacitive configuration. This consists of an anode and a cathode put in parallel with the plasma being generated between them. The most common ICP configuration consists of a coil wound around the outside of the vacuum chamber. An RF current is sent through the coil and the plasma is generated and sustained by continuous ionization by the time varying magnetic field. This field holds the positive ions stationary due to the absence of a static electric field in any direction. The electrons will travel a circular path due to the RF source.
The ICP configuration is often combined with the RIE configuration resulting in an ICP-RIE process. When the two designs are combined it is possible to decouple the ion density from the electron density. This is done by taking the ICP design and introducing a separate RF source to the wafer electrode while using the chamber wall as the ground anode. This induces a negative DC bias which attracts the positive ions towards the wafer electrode. This bias can be increased or decreased without much influence on the plasma density. This allows pure isotropic chemical etching to be performed by holding the ions stationary or pure mechanical sputter etching to be utilized. This configuration also allows any percentage of sputtering and chemical etching.

This ICP-RIE configuration allows for more vertical sidewalls to be achieved using the Bosch process. This process was invented for etching silicon by the Robert Bosch Company and is used in the microelectronics industry to etch deep vertical structures in silicon [14,22,23]. The original Bosch process consisted of two steps. The first being a deposition of fluorocarbon polymers. The second step is a RIE etch utilizing heavy argon ions and fluorine radicals from sulfur hexafluoride (SF₆). For the first ICP step the common fluorocarbon polymers used are gases such as CHF₃ or C₄F₂. The ICP step results in an isotropic process that produces a thin fluorocarbon film on the surfaces of the etched material. The second step implements an RIE process. This causes the ions to bombard the horizontal surfaces removing the passivation layer allowing the fluorine radicals to perform a semi-isotropic etch in the cleared area. This two-step process is repeated several times until the desired etch depth is achieved. This process results in more vertical sidewalls due to the fluorocarbon passivation remaining on the sidewalls.
throughout the process. However, without modification the sidewalls tend to have ripples
due to the semi-isotropic etch of the second step.

Figure 3.13: Illustration of the rippled sidewalls on vertical etch of silicon during the original Bosch process.
4.1 Photodetector Design

The design of this device utilizes the nonlinear and optical properties of LPCVD silicon nitride combined with the single-photon detecting capabilities of silicon. The device is a vertically stacked device so it is phase matched for vertical coupling. We start with a SOITEC SOI wafer that consists of a 500 μm silicon substrate, 1 μm silicon dioxide film for insulation, and a 0.5 μm silicon film to pattern the silicon pads for photo detection. Once the silicon pads are patterned to a length of 100 μm, various widths, and surround by silicon dioxide. Figure 4.1 shows the silicon detector design before the LPCVD silicon nitride.
Figure 4.1: A top view of the silicon photodetectors surrounded by an insulating layer of silicon dioxide.

Once the silicon detectors are patterned a 250 nm film of stoichiometric silicon nitride is deposited and patterned into waveguides. These waveguides are 400 μm long and 1 μm wide. This final design is shown from the top down in figure 4.2.
Finally the devices are encapsulated by a layer of silicon dioxide. This creates symmetric rectangular waveguides up to the point of coupling to the detector. This final image is shown below in figure 4.3.

4.2 Lumerical FDTD Simulation

Lumerical Finite-Difference Time-Domain (FDTD)\textsuperscript{2} commercial software was used to determine the mode and simulate the coupling between the guiding silicon nitride layer and the detecting silicon layer. As mentioned in chapter two directional coupling can occur due to evanescent waves in the cladding perturbing a nearby waveguide. In this design we are investigating a vertical coupling instead of a horizontal coupling. The fundamental TE mode is coupled injected into the silicon nitride layer and shown in figure 4.4.

\textsuperscript{2} Lumerical FDTD license registered to AFRL.
Figure 4.3: Final device design. The fundamental mode is injected into the silicon nitride waveguide which is insulated by silicon dioxide. The guided mode is then vertically coupled into the silicon photo detector.

Figure 4.4: The Lumerical FDTD simulated fundamental TE mode injected into the silicon nitride guiding layer.

The injected mode then propagates toward the silicon photo detector. Once the silicon photo detector is directly under the silicon nitride waveguide the matching longitudinal
modes, $\beta_{SiN_4}$ and $\beta_{St}$, will lead to phase matched coupling [11]. Notice that the silicon detector is a higher order mode than the silicon nitride guiding layer which is single mode.

Figure 4.5: The Lumerical FDTD electric field simulation of the silicon nitride on silicon waveguide on photo detector device.

Figure 4.5 also shows that the majority of the electric field is absorbed within 50 microns of coupling with the photo detector. This allows for scalable dimensions for on-chip photo detectors.

4.3 Device Fabrication using CMP

The device fabrication using CMP was initially attempted in the Wright-Patterson Air Force Research Laboratory (AFRL) clean room. Figure 4.6 shows the process implemented to fabricate the waveguide on photo detector devices. The beginning steps of this process proved to be trivial.
as they are regularly performed and well characterized. The first plasma etch step is prepared by spin coating a Shipley 1813 microposit photoresist onto the top silicon layer of the SOI wafer. The resist was applied to the sample using a pipette and spun at 4000 RPM for 30 seconds. After the resist spread across the surface of the wafer it was baked at 100° C for 75 seconds. The sample is then loaded into the MA6 mask aligner with an intensity of 20 mW/cm². Once the exposure is completed the wafer is developed using a 5:1 DI water to 351 developer ratio. The developer was puddled for 15 seconds, spun for 15 seconds, and then straight DI water was applied as a rinse for the final 30 seconds of the spin. This recipe for 1813 photoresist results in a final thickness of about 1.7 μm. This thickness is necessary due to the plasma etch step. However, this thickness can also result in lower resolution as seen in figure 4.7.
Figure 4. 7: The resulting pattern of the photolithography process stated above. Left we see the photoresist pattern for the silicon detector pads are 100 µm apart. Right we see the 10 µm wide silicon detector pattern.

Also notice the right image in figure 4.7 has rounded corners. This rounding could be due to diffraction caused by the thickness of the resist or overexposure in the MA6 mask aligner.

Once the photolithography has been completed a deep silicon RIE\(^3\) (SDRIE) process is used to etch the pattern into the silicon. The gases used for this etch are SF\(_6\), C\(_4\)F\(_8\), and Ar. The fluorine molecules are very reactive with the silicon and perform a chemical etch while the carbon deposits a thin film isometric to the surface topography and the argon sputters the horizontal surfaces including the deposited carbon. In fact, the SF\(_6\) is so reactive with the silicon that it only takes about 10 seconds to etch 350 nm deep resulting in an etch rate of about 2 µm/min. Figure 4.8 shows the parameters used in the SDRIE process [22]. The surface profile is shown in figure 4.9 with the step height measured to be about 2.125 µm, but that is because the resist has not been removed in a solvent rinse. It is important to measure the step height before removing the resist so that

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\(^3\) RIE etching performed by Andrew Browning at the AFRL clean room facility.
if the etch is not deep enough another process can be run. Once the resist is removed it is incredibly difficult to align the mask with the previously etched pattern.

![Figure 4. 8: The pressure, ICP power, RF bias, time, and gas flow parameters of the SDRIE process used to etch silicon.](image)

![Figure 4. 9: KLA Tencore surface profile of a 10 second SDRIE process done to a patterned silicon wafer.](image)

Once the plasma etch is complete the sample looks like the top center image in figure 4.6. Next two times the etch depth of silicon dioxide is deposited using AFRL’s PECVD system. In this case about 2 μm of oxide was deposited. The substrate is put in the PECVD system and heated to 300° C. The RF power is 25 W with silane and nitrous

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4 PECVD performed by Andrew Browning at the AFRL clean room facility.
oxide gas being flown into the chamber. This creates a plasma with nonvolatile chemical reactions and results in a silicon dioxide deposition. Due to the isometric nature of this technique the silicon dioxide also covers the silicon detector pads.

In order to remove this top layer a planarization using CMP was attempted. The samples were sent to Cabot Microelectronics for CMP processing. Unfortunately, the investigation of the curvature of the samples done by Cabot revealed that the CMP could not be done. It was reported that the samples had too much bow for the removal of 3 μm of silicon dioxide to be removed. It was reported that one sample had upwards of 6 μm of curvature by the CMP step. We are starting our processing on a 6 inch SOI wafer. When discussing the bow limits of CMP with Cabot Microelectronics they gave us a workable curvature of 1.2 μm. This curvature was the minimum curvature necessary to remove 3 μm of silicon dioxide from a sample. The surface profile of a piece of diced SOI is shown in figure 4.10.

![Figure 4. 10: The Zygo surface profile of a SOITEC 25mm by 25mm SOI piece. We see that without any processing the sample has a curvature of about 1.8 μm.](image)

On the left of figure 4.10 we see that there is a radius of curvature of about 1.8 μm without any processing. If the cross section of the other diagonal is considered the
curvature is about 2.4 μm. This could be due to the fabrication process of the SOI or the stress of the dicing saw on the SOI sample.

4.4 Device Fabrication using Thermal Oxidation

Due to the difficulty of flattening the SOI pieces a new approach was proposed to bypass the need for CMP and polishing in general. It is beneficial to bypass the polishing process because polishing is hard on the sample. Despite the miniscule surface roughness achieved by the chemical etching of CMP, the mechanical polishing process can cause additional damages below the surface. The general rule of thumb is the damage below the surface is 5 times the coarseness of the polishing pad.

The process replacing CMP is shown in figure 4.11. The thermal oxidation process is a high temperature process that requires a hard mask. Because of this PECVD processes are no longer compatible with the overall process. We start with a LPCVD silicon

![Figure 4. 11: The planarization process using thermal oxidation. Left starts with a sturdy LPCVD silicon nitride on silicon. Center is the result of a plasma etch to 44% the original height of the silicon. Right the thermal oxidation process grows oxide to the original silicon height.](image-url)
nitride deposition\textsuperscript{5}. The density of the LPCVD nitride is necessary to prevent a large amount of silicon oxynitride growing during the thermal oxidation process. The relationship between the volumes of silicon compared to silicon dioxide is 44\%-56\% \cite{14}. Therefore, if we start with 500 nm of silicon and etch it 44\% its original height, 220 nm, then the thermal oxidation reaction will result in an oxide that is 500 nm thick.

The entire process is outlined in figure 4.12. This process utilizes various UD laboratories and Ohio State University (OSU) clean room facilities in addition to AFRL. The LPCVD processes occurred at OSU where they deposit a stoichiometric silicon nitride film. Once 100 nm of LPCVD silicon nitride is deposited on the SOI piece a similar photolithography process was implemented. However, the photo lithography process in Dr. Sarangan’s lab uses the Rohm and Haas SPR-955-CM photoresist.

\textsuperscript{5} LPCVD $\text{Si}_3\text{N}_4$ performed by Paul Steffen at the OSU nanotech facility.
First HMDS organosilane is applied to the surface of the silicon nitride to cause the surface to be hydrophobic. This allows the photoresist to develop better due to the water not spreading along the surface and undercutting the photoresist. Once the HMDS is applied the SOI piece is baked for 90 seconds at 100° C. A 955 photoresist is applied to the sample surface and spread at 2000 RPM for about 30 seconds. The sample is baked for 90 seconds at 100° C to remove excess solvent from the photoresist. The sample is mounted in the MA6 mask aligner where two rows of detector pads are aligned on the SOI. The exposure lasts for 15 seconds with an intensity of 20 mW/cm². The substrate undergoes a post exposure bake for 90 seconds at 100° C and is developed for 1 minute using MF-319 and DI water. This photolithography process results in a 1.2 μm thick photoresist.
For the plasma etching a modified Bosch process is utilized. However, due to the LPCVD silicon nitride on the silicon the time must be altered. This process was done in the Dr. Sarangan’s laboratory using the Unaxis Shuttleline ICP system\textsuperscript{6}. The modified Bosch process, or single-step RIE process for this system etches silicon at a rate of 25 Å/sec, whereas the LPCVD silicon nitride etches at about 18 Å/sec. Figure 4.13 is based on a sample that had about 73 nm of LPCVD silicon nitride on the surface. This requires about 150 seconds in the single-step RIE process. The step height after the process is about 320 nm. We know that about 73 nm of that is LPCVD nitride mask and will be removed. This leaves us with a silicon step of about 247 nm.

The silicon appears to be under etched. However, this is by design. Once the oxidation is completed the LPCVD silicon nitride will need to be removed. Not only will

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{si3n4_on_si_step_height.png}
\caption{The LPCVD silicon nitride on silicon surface profile after 150 second SDRIE etch. The total step height is about 320 nm.}
\end{figure}

\textsuperscript{6} Single-step RIE etches were performed by David Lombardo in Dr. Sarangan’s laboratory.
the nitride need to be etched away, but a layer of silicon oxynitride will form. This is a very stubborn material to remove and it seems the best way to remove it is with a plasma etch. This means we need a small sacrificial layer of oxide. So, we expect the 247 nm of silicon to oxidize to a thickness of about 561 nm. This gives us 61 nm to sacrifice during the removal. This could be excessive and lead a nonplanar surface.

Now that the silicon has been etched to about 44% its original height the thermal oxidation can be done. We modified an OTF-1200X-Series split tube furnace to act as a wet thermal oxidation furnace. The furnace is shown in figure 4.14. The furnace is altered by branching the nitrogen flow to a three input beaker. The nitrogen goes into one opening, bubbles the 80° C water, and the water vapor exits through to the furnace. The third opening is simply to refill the beaker with water. This system was built in Dr. Sarangan’s laboratory and a number of test runs were performed.\(^7\)

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\(^7\) Thermal oxidation processes executed by Dr. Sarangan.
Brigham Young University’s (BYU) thermal oxidation calculator was used to estimate the growth of the oxide [24,25]. The temperature of the furnace is set to 1150° C and takes 2 hours to ramp. One hour into the ramp the beaker heater is powered on and set to heat the water to 80° C. Once the furnace has reached temperature nitrogen is directed through the water to bubble the water vapor into the furnace. This process runs for 30 minutes according to BYU oxide calculator to grow 500 nm of thermal oxide. After the 30 minute run the nitrogen is redirected to the furnace rather than through the water and the furnace ramps down overnight.

According to the Filmetrics reflectometry instrument this process only resulted in about 300 nm of thermal oxide. This instrument estimates the thickness of the film using normal incident interference patterns. The only constant is the time run at the set temperature. It’s very possible the temperature is changing due to the flow of the water vapor through the furnace. This can be controlled be either changing the flow of the nitrogen into the water, or changing the length of the process. Using the oxide calculator the temperature needed to grow 300 nm in 30 minutes is 1037° C. Adjusting the temperature of the calculation to 1037° C results in a oxidation time of 1 hour and 2 minutes. However, the SOI wafer has a natural stop in the 1 μm oxide layer.
under the silicon which allows us to oxidize for 1 hour and 15 minutes without over growing the oxide. Figure 4.15 shows the profile of the sample after an hour and 20 minute oxidation.

The step height in figure 4.15 is about 37 nm. This shows that the oxide has overgrown about 36 nm. This 36 nm will be used as a sacrificial layer in removing the silicon nitride mask. The profile also shows two distinct bumps on either side of the feature. These bumps are known as bird’s beak and are due to the stress of the growth of the oxide on the nitride mask [26]. A scanning electron microscope (SEM)\(^8\) image of this bird’s beak is shown in figure 4.16.

\(^8\) SEM images were recorded by Dr. Shivashankar Vangala in the AFRL clean room facility.
Figure 4.16: Scanning electron microscope (SEM) image of the silicon photo detector encased by silicon dioxide and silicon nitride. The 522 nm feature is the silicon pad while the 133 nm layer above is the silicon nitride mask.

The SEM image shows a cross section of the silicon photo detector pad. The silicon feature is marked by the 522 nm line while the silicon nitride mask is 133 nm. The bird’s beak is on the edge of the mask and goes around the entire device. The isotropic nature of the oxidation is also apparent in this cross section. The waveguides that will be deposited onto the silicon feature will be 1 μm wide which allows for some horizontal loss of the silicon pads without inhibiting the coupling between the guiding and detecting layers.
The Lumerical FDTD simulations were redone inserting the bird’s beak into the design. Although the bump does cause some extra loss, a few percent, the majority of the guided wave is still coupled into the silicon photo detector. This simulation is shown in figure 4.17.

![Lumerical FDTD electric field simulation](image)

**Figure 4.17:** A Lumerical FDTD electric field simulation of the silicon nitride waveguide on silicon photo detector device. The bird’s beak is modeled around the 50 μm point.

With the thermal oxide grown the silicon nitride mask must be removed. A wet chemical etch using phosphoric acid is used for this. The phosphoric acid has a high selectivity of up to 80:1 etching of silicon nitride to silicon and oxide [27]. However, to obtain and maintain this selectivity is a delicate process. The phosphoric acid is 85% by weight, leaving 15% water. The acid must also be heated for the reaction with the silicon nitride to occur. Studies have shown that the most uniform results are achieved when the acid is held at a temperature of 160° C [28,29]. However, the boiling point of the water is 100° C resulting in rapid evaporation from the acid.
The phosphoric acid etch of silicon nitride proven to be fickle. The phosphoric acid must be seasoned with silicon nitride before the samples are etched. The chemical reaction occurring between the silicon nitride and phosphoric acid is

\[ 3\text{Si}_3\text{N}_4 + 27\text{H}_2\text{O} + 4\text{H}_3\text{PO}_4 \rightarrow 4(\text{NH}_2)_3\text{PO}_2 + 9\text{H}_2\text{SiO}_3. \]  \hspace{1cm} (4.1)

The reaction for silicon oxide is

\[ \text{SiO}_2 + 2\text{H}_2\text{O} \rightarrow \text{Si(OH)}_4. \]  \hspace{1cm} (4.2)

The reaction shown in 4.1 shows that the silicon nitride reaction produces an ammonium phosphate and hydrous silica. This hydrous silica reduces the etch rate of both the silicon nitride and silicon oxide. However, these rates on not reduced at the same rate. The selectivity can be improved to 80:1 by seasoning the phosphoric acid bath. The initial silicon nitride to be deposited into the acid is also very volatile. The reaction can cause the sample to move around in the bath as well as producing bubbles along the surface of the sample.

The characterization of this etch has been done without replenishing the evaporating water. This work was done in Dr. Jay Mathew’s laboratory. This has resulted in a non-reproducible etch rate. This is shown in table 4.1. We can see that these etch rates are not consistent with each other or the reported 4.5 nm/min etch from studies [29]. This could be a timing issue due to the evaporation of the water from the acid, a temperature issue if the acid at the bottom of the beaker is hotter it will etch the sample faster, or a stoichiometric issue.
Table 1: The etch rates of two pieces of silicon nitride on silicon in a pixel patter in a phosphoric acid bath. Each bath starts with new acid, and a 20 minute silicon nitride seasoning.

<table>
<thead>
<tr>
<th>etch time (min)</th>
<th>step height (nm)</th>
<th>etch depth (nm)</th>
<th>removal rate (nm/min) (based on total etch depth)</th>
<th>step etch depth (nm)</th>
<th>step removal rate (nm/min)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>356.3</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>5</td>
<td>245.8</td>
<td>110.5</td>
<td>22.1</td>
<td>110.5</td>
<td>22.1</td>
</tr>
<tr>
<td>10</td>
<td>123.4</td>
<td>232.9</td>
<td>23.29</td>
<td>122.4</td>
<td>24.48</td>
</tr>
<tr>
<td>15</td>
<td>119.1</td>
<td>237.2</td>
<td>15.8133333333</td>
<td>4.3</td>
<td>0.86</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>etch time (min)</th>
<th>step height (nm)</th>
<th>etch depth (nm)</th>
<th>removal rate (nm/min) (based on total etch depth)</th>
<th>step etch depth (nm)</th>
<th>step removal rate (nm/min)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>356.3</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>301.5</td>
<td>54.8</td>
<td>27.4</td>
<td>54.8</td>
<td>27.4</td>
</tr>
<tr>
<td>4</td>
<td>224.7</td>
<td>131.6</td>
<td>32.9</td>
<td>76.8</td>
<td>38.4</td>
</tr>
<tr>
<td>6</td>
<td>156.1</td>
<td>200.2</td>
<td>33.366666667</td>
<td>68.6</td>
<td>34.3</td>
</tr>
<tr>
<td>8</td>
<td>138.5</td>
<td>217.8</td>
<td>27.225</td>
<td>17.6</td>
<td>8.8</td>
</tr>
</tbody>
</table>

If the deposited film is hydrogen rich and similar to PECVD quality then studies show the etch to be about 20 nm/min [29]. Between each etch the step height was measured using a profilometer in the cleanroom. However, the hot phosphoric bath was not in the clean room. This required gowning up between each etch leaving up to 10 minutes between each dip. For sample b there was a larger time gap between the 2 and 4 minute etches which could explain why that etch rate is around 38 nm/min when the previous etch was only 22 nm/min.
Using the data from table 4.1 an oxidized sample was etched for 5 minutes in a hot phosphoric acid bath. Due to the oxidation step the etch rate should be slower because of the oxynitride formation on the sample. However, after 5 minutes there was no measureable change in the step height of the sample. This suggests that the oxynitride is much less reactive to the phosphoric acid than anticipated. It could also mean that the layer of oxynitride is thicker than estimated.
5.1 Hot Phosphoric Acid Etch

There is still work to be done for the setup of the hot phosphoric acid etch of LPCVD silicon nitride. First the removal rate of the silicon nitride needs to be reproducible. This should be possible by using a closed heating system instead of an open hot plate. Despite using a thermometer to measure the temperature the acid will have a different temperature relative to the position.

The water replenishment system needs to be installed. An IV drip has been purchased to use as a water refreshment system. As mentioned in the previous chapter water plays a role in the chemical reaction with the acid and nitride. If all of the water is evaporated during the seasoning of the bath this could be having a large effect on the uniformity and consistency of the chemical etch.

A plasma etch process is being developed to handle the oxynitride. This robust film etches very slowly in hot phosphoric acid. It is possible to etch through the oxynitride using a wet chemical etch, but it etch as slowly as silicon or silicon dioxide which has an etch rate of 0.17 nm/min and 0.18 nm/min. However, plasma etching should etch the oxynitride and silicon dioxide at an equal rate. With the extra oxide
thickness it is possible to dry etch the few nanometers of oxynitride and then perform the hot phosphoric acid etch on the opened nitride mask [27,28,29].

5.2 Electron Beam Lithography

Electron beam (E-beam) lithography can be done at AFLR or OSU and is a similar process to photolithography. The main difference being that the resist is exposed using a focused E-beam. This allows for sub-micron features to be exposed. This process will be used to pattern the LPCVD silicon nitride waveguides on the silicon photodetector pads. The resist is applied using the spin method. There are both positive and negative resists available to pattern.

A lift-off process is common for positive resists of e-beam lithography. This is a necessary process because the positive resists for e-beam lithography tend to form a thin layer on the substrate. This strikes dry etching from the process because the sputtering process within RIE etching will destroy the thin resist. However, evaporating a metal like nickel onto the substrate and then removing the resist creates a hard mask. This allows for a plasma etch to be performed and then the nickel is removed using a common, selective nickel etchant.

It is also common to expose trenches around the waveguides if the resist is thick enough to survive dry etching, or if a chemical etch is possible. This is done to reduce the time the e-beam exposure would take. The waveguides need to have vertical sidewalls which rules out a chemical etch and leads to the lift off method being utilized.
5.3 Silicon Nitride Waveguide Etch

A timed SDRIE etch will be used to etch the waveguides. As mentioned above a hard nickel mask is deposited to protect the underlying waveguide. The SDRIE method is ideal because of the multiple steps to insure vertical sidewalls. The LPCVD silicon nitride will be deposited from OSU and has been characterized in chapter 4. The etch rate should remain about 18 Å/sec requiring an etch time of about 139 seconds to etch 2500 Å of nitride.

5.4 Waveguide on Detector Device Characterization

Experiments will be set up to investigate the absorption of the silicon photodetectors. An 800 nm source will be focused and fiber coupled into the silicon nitride waveguides. An IR camera will be used to visually examine the phase matched waves being absorbed into the silicon. To evaluate the quality of silicon nitride waveguides will also be deposited between the silicon pads. This will allow the investigation of the attenuation properties of the waveguides without the absorption of the silicon.

A silicon photodetector will be placed on the output side of the waveguides. By cleaving both sides of the chips the waveguides will have both an input and an output end. This will allow us to record the intensity that propagates through the entirety of the waveguide. Again, some waveguides will couple into the underlying silicon while others will be deposited on the silicon dioxide insulator.
5.5 Wafer Flattening

The CMP process requires a flat wafer. As shown in chapter 3 wafers tend to have some bow and warp out of the package. This was shown again in chapter 4 when the dicing of the SOI wafers already had up to 2 μm of bow. It is possible to deposit films with opposing stress and strain to the measured curvature. The Stoney equation allows you to solve for the ideal thickness to remove the curvature from a sample and is represented as

$$\sigma(f) = \frac{E_s h_s^2 \kappa}{6h_f (1 - v_s)^3},$$

(5.1)

where \(f\) and \(s\) represent the film and substrate, \(E\) and \(v\) are Young’s modulus and Poisson’s ratio, \(h\) is the height of the film, \(\kappa\) is the curvature of the systems, and the stress is denoted by \(\sigma(f)\) [21,30].

Young’s modulus and Poisson ratio for silicon, silicon dioxide, and silicon nitride can be looked up. The curvature is measured, and the initial stress can then be solved. We see that the curvature can’t equal 0 so a small number could be inserted into the equation. If the backside of the wafer is sacrificial, which these waveguide on detector devices are, then the films can be deposited on the backside. This could result in flattened samples and the CMP process could be reconsidered.

5.6 Bird’s Beak Reduction

The bird’s beak is the result of the stress from the growth of the silicon dioxide acting on the silicon nitride mask. Due to the isometric nature of oxidation the oxide grows horizontally as well as vertically. This causes pressure, and the bump, to grow around the silicon features. Again, stress relief methods could be utilized to remove the
bird’s beak. Studies have been done to remove the bird’s beak using various stress relief layer depositions [26]. However, these methods still result in a trench around the features instead of bumps, and require multiple extra steps.
CHAPTER 6
CONCLUSIONS

Phase matching, and coupled mode theory support the design of scalable waveguide on photo detector devices. Models show that fundamental modes injected into a 250 nm thick, 1 μm wide waveguide will couple into a 500 nm thick, 3 μm wide silicon photo detector. However, the 3-D fabrication of this optical circuit relies on new and delicate processes.

Chemical Mechanical Planarization is still in its infancy for semiconductor processing. Although it is used by large semiconductor fabrication facilities it is not readily available. CMP processing has many limitations with respect to the bow, warp, and curvature of the substrates. These limitations must be reached using wafer flattening methods such as deposition of films on the backside of samples.

Planarization using thermal oxidation methods are promising for the fabrication of these devices. Thermal oxide is a high quality oxide and has high quality dielectric properties. However, the SDRIE etch depth through the silicon nitride mask into the silicon is critical and must be reproducible. If the bird’s beak produced by the stress of the oxide growth on the nitride mask causes the guided wave to scatter then addition steps may need to be taken to reduce the size, or completely remove, the bird’s beak.
The selectivity of a hot phosphoric acid bath is ideal for etching silicon nitride. However, there are many complications to consider when preparing and etching samples using this acid. Due to the high temperature, 160° C, the water boils out of the phosphoric acid mixture and must be replenished in order to maintain a constant, uniform etch. In addition to the water being replenished the temperature must be held constant. Finally, it is necessary to season the phosphoric acid. The chemical reaction of the acid with silicon dioxide and silicon nitride is reduced as silicon nitride reacts with the phosphoric acid and water mixture. The reaction rate reduces for the silicon dioxide much quicker than for the silicon nitride leading to a more selective chemical bath.

Once these processes are fully developed waveguide on detector devices will be experimentally tested using fiber coupling, an IR camera, and a silicon detector. This will allow the investigation of the phase matched coupling between the silicon nitride waveguide and silicon photo detector. The nonlinear properties of the silicon nitride also allow further development into scalable quantum information processing through the utilization of four-wave mixing.
REFERENCES


APPENDIX

RECIPES

AFRL Process – CMP based

1. Spin coat Shipley 1813 photoresist
   1.1. 4000 RPM – 30 sec – 200 ramp

2. Pre-exposure bake
   2.1. 110° C – 75 sec

3. Expose using MA6 mask aligner
   3.1. 18 W/cm² – 5.2 sec

4. Develop

5. SDRIE Plasma Etch
   5.1. Flow SF₆, C₄F₈, and Ar. Depth depends on oxide thickness of SOI wafer.

6. PECVD SiO₂
   6.1. SiH₄ + N₂O. Deposition thickness depends on thickness of SOI wafer.

7. CMP
   7.1. Requires a sample curvature of 1.2 µm or less. Sent samples to Cabot Microelectronics.
Drs. Sarangan and Mathews lab processes – Thermal Oxidation based

1. LPCVD 100 nm Si₃N₄ at Ohio State University (OSU)
   1.1. 1:3 Dichlorosilane:Ammonia (DCS:NH₃) at 790° C 0.3 T

2. Spin coat SPR-955 photoresist
   2.1. 2000 RPM – 40 sec – 250 RPM/sec ramp

3. Pre-exposure bake
   3.1. 100° C – 90 sec

4. Expose using MA6 mask aligner
   4.1. 20 W/cm² – 15 sec

5. Post-exposure bake
   5.1. 100° C – 90 sec

6. Develop using UD developer spinner
   6.1. 1 minute MF-319 and DI water

7. SDRIE Plasma Etch
   7.1. Flow SF₆, C₄F₈, and Ar. Etch through the entire Si₃N₄ layer and through 56% of the Si layer.

8. Remove photoresist

9. Wet Thermal Oxidation
   9.1. OTF-1200X-Series set to 1150° C. Growth time depends on depth of Si layer.

10. SDRIE Plasma Etch
    10.1. 40 second etch removes oxidized nitride.

11. Hot phosphoric acid etch
    11.1. 85% phosphoric acid by weight is heated to 160° C.
11.2. A piece of silicon nitride is etched for 20 minutes to season and increase the selectivity of the bath.

11.3. The sample is etched for 10 minutes to remove remaining oxynitride and silicon nitride.

12. LPCVD 250 nm, or desired waveguide thickness, $\text{Si}_3\text{N}_4$ at Ohio State University.

12.1. 1:3 Dichlorosilane:Ammonia (DCS:NH$_3$) at 790° C 0.3 T

13. Electron Beam Lithography to define the waveguides

14. SDRIE Plasma Etch

14.1. Etch through the thickness of the $\text{Si}_3\text{N}_4$

15. PECVD SiO$_2$ thick enough to completely cover the $\text{Si}_3\text{N}_4$