PHYSICAL VAPOR DEPOSITION OF MATERIALS
FOR FLEXIBLE TWO DIMENSIONAL ELECTRONIC DEVICES

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PHYSICAL VAPOR DEPOSITION OF MATERIALS

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ABSTRACT

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Molybdenum Disulfide (MoS$_2$) and Tungsten Disulfide (WS$_2$) are two materials in a larger class of materials known as Transition Metal Dichalcogenides (TMDs) that have begun emerge as semiconducting materials. When their horizontal length scale is reduced from bulk to monolayer they demonstrate surprising combinations of properties including a direct electronic band gap and mechanical flexibility. Two dimensional (2D) materials have the potential to revolutionize performance and tailorability of electro-optical devices fabricated entirely from molecularly thin materials. In a departure from traditional exfoliation or high temperature chemical vapor deposition approaches for 2D materials synthesis, novel plasma-based physical vapor (PVD) techniques were used to fabricate uniform films over large areas. This experimental approach allowed unique studies. For example, vapor phase growth allowed systematically variation of the sulfur vacancy concentration in MoS$_2$ and WS$_2$ and subsequent correlation to electronic properties. This effort leads to controlled bottom-up assembly of 2D devices on flexible and standard substrates to experimentally couple the remarkable intrinsic mechanical and electronic properties of ultrathin materials, which are particularly appealing for molecular sensing. The pursuit of an all physical vapor deposited field effect transistor (FET) is
the main priority for the 2D materials community as definitive demonstration of the feasibility of physical vapor deposition as a scalable technique for consumer electronics. PVD sputtered Titanium Nitride (TiN) and Tungsten (W) were experimentally characterized as potential back gated materials, Plasma Vapor Deposited (PLD) a-BN was electrically characterized as a uniform ultra-thin low temperature dielectric, and sputtered MoS\(_2\) and WS\(_2\) were electrically characterized as a semiconductor material. Tungsten deposition methods were previously researched and mimicked for smooth and conductive back gate material depositions. TiN was parameterized and the best room temperature deposition conditions were 70V applied to the sputtering gun with 25 sccm gas flow of 90% N\(_2\) and 10% Ar for 60 minutes. The best high temperature depositions were done at 500°C, 70V applied to the sputtering gun with 25 sccm gas flow of 90% N\(_2\) and 10% Ar for 30 minutes. Dielectric a-BN electrical characterization began to occur after 6nm which equated to 100 pulses, while 200 pulses equated to 16.5nm thickness. A dielectric constant of 5.90 ± .65 is reported for a-BN for under 20nm thickness. Soft probing techniques by conductively pasted gold wires on the probe tips were required to obtain true electrical measurements of 2D materials in a stacked structure, otherwise scratching would occur and uniformity would cease to exist in the film. Chemical Vapor Deposition (CVD) and mechanical exfoliation have provided the only working TMD semiconductor 2D materials in MOSFET structure to date with lithographic electrical connections. PVD sputtering as a new synthesis method for crystalline TMD with a stoichiometric ratio is achievable over large areas. Though, reduced area depositions are required for doped Silicon and Silicon Oxide (SiO\(_2\)) based FET structures to limit the chance of encountering a pinhole. With reduced area and stoichiometric enhancement control, sputtered TMD films exhibit high sensitivity to oxygen and are electrically conductive even when exposed to a field effect. Increasing the grain size of the
sputtered materials is the next driving force towards a fully recognizable TMD thin film transistor.
Dedicated to the special women in my life: my fiancée Stephanie Riner my pillar of strength and to my puppy Pegasus who keeps me laughing and smiling except for when she's micturating on my roommate’s bed
ACKNOWLEDGEMENTS

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<tr>
<td>2D</td>
<td>Two-Dimensional</td>
</tr>
<tr>
<td>A</td>
<td>Area</td>
</tr>
<tr>
<td>AFM</td>
<td>Atomic Force Microscopy</td>
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<tr>
<td>AFRL</td>
<td>Air Force Research Laboratory (Laboratories)</td>
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<tr>
<td>Al(_2)O(_3)</td>
<td>Aluminum Oxide</td>
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<tr>
<td>Au</td>
<td>Gold</td>
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<tr>
<td>BioFET</td>
<td>Biological Field Effect Transistor</td>
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<tr>
<td>a-BN</td>
<td>Amorphous Boron Nitride</td>
</tr>
<tr>
<td>h-BN</td>
<td>Hexagonal Boron Nitride</td>
</tr>
<tr>
<td>C-AFM</td>
<td>Conductive Atomic Force Microscopy</td>
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<tr>
<td>Cr</td>
<td>Chromium</td>
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<tr>
<td>Cu</td>
<td>Copper</td>
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<tr>
<td>CVD</td>
<td>Chemical Vapor Deposition</td>
</tr>
<tr>
<td>d</td>
<td>Thickness</td>
</tr>
<tr>
<td>DI</td>
<td>De-ionized</td>
</tr>
<tr>
<td>DSM</td>
<td>Death Star Mask</td>
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<tr>
<td>FET</td>
<td>Field Effect Transistor</td>
</tr>
<tr>
<td>HOPG</td>
<td>Highly Ordered Pyrolytic Graphite</td>
</tr>
<tr>
<td>I(_d)</td>
<td>Drain Current</td>
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<tr>
<td>I(_g)</td>
<td>Gate Current (also known as leakage current)</td>
</tr>
<tr>
<td>I(_s)</td>
<td>Source Current</td>
</tr>
<tr>
<td>k</td>
<td>Dielectric Constant</td>
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<tr>
<td>Mo</td>
<td>Molybdenum</td>
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<td>MoS(_2)</td>
<td>Molybdenum Disulfide</td>
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<tr>
<td>Acronym</td>
<td>Definition</td>
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<tr>
<td>MOSFET</td>
<td>Metal Oxide Semiconductor Field Effect Transistor</td>
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<tr>
<td>N₂</td>
<td>Nitrogen</td>
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<tr>
<td>PLD</td>
<td>Pulsed Laser Deposition</td>
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<td>PVD</td>
<td>Physical Vapor Deposition</td>
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<tr>
<td>S</td>
<td>Sulfur</td>
</tr>
<tr>
<td>sccm</td>
<td>Standard Cubic Centimeters Per Minute</td>
</tr>
<tr>
<td>SOTA</td>
<td>State of the Art</td>
</tr>
<tr>
<td>SS</td>
<td>Subthreshold Swing</td>
</tr>
<tr>
<td>TMD</td>
<td>Transition Metal Dichalcogenide</td>
</tr>
<tr>
<td>TOX</td>
<td>Thermally Grown Oxide, Note: for this work SiO₂</td>
</tr>
<tr>
<td>Ti</td>
<td>Titanium</td>
</tr>
<tr>
<td>TiN</td>
<td>Titanium Nitride</td>
</tr>
<tr>
<td>UHV</td>
<td>Ultra-high Vacuum</td>
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<tr>
<td>V</td>
<td>Volts</td>
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<tr>
<td>Vₐ</td>
<td>Drain Voltage</td>
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<td>V₉</td>
<td>Gate Voltage</td>
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<tr>
<td>Vₛ</td>
<td>Source Voltage</td>
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<td>W</td>
<td>Tungsten (when used in sentence)</td>
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<tr>
<td>W</td>
<td>Watts (after a number for power)</td>
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<tr>
<td>WS₂</td>
<td>Tungsten Sulfide</td>
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<tr>
<td>XPS</td>
<td>X-ray Photoelectron Spectroscopy</td>
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CHAPTER I

INTRODUCTION

1.1. Electronic Devices

Electronic devices began to emerge in the 1800s by harnessing the power of electromagnets and eventually led to the production of the first transistor which was built by Lilienfeld in 1925. Lilienfeld’s invention went unnoticed until later Bell Laboratories with W.S. Gorton invented the first operational transistor intended for commercial applications. A transistor is an electrical switch. A series of transistors can be used to store information by correlating a pattern of OFF and ON states to correspond to a digital piece of information. Larger numbers of integrated transistors allow storage of more information. With the first transistor came the birth of modern electronics and the rise of many devices with diverse functionality including switching, sensing, optoelectronics, and batteries. The focus for this body of work is specifically on fundamental transistor behavior—primarily, discovering a path to overcome physical size limitations potentially inhibiting continuation of Moore’s Law for transistor density. Moore’s Law states that the number of transistors per unit area should double every two years. Overcoming the theoretical limitations associated with transistor miniaturization requires a search for new semiconducting materials other than silicon for integrated Field Effect Transistor (FET) circuits. The metal oxide semiconductor field effect transistor, MOSFET, is the type of transistor studied in this work. A MOSFET is a sandwich structure which consists of four main components including the source/drain contacts, semiconductor material, the dielectric...
insulator, and the gate contact arranged in a particular architecture. There are three main electrical testing connections within the MOSFET which are the gate, source, and drain. There are two different architectures for MOSFETs; a bottom gated structure and a top gated (Figure 1). The channel length is the distance between the source and the drain. This distance dictates the size, or more specifically, the ‘footprint’ of the transistor in an integrated circuit.

Figure 1: (a) Bottom and (b) Top Gated MOSFET Heterostructures

For a top gated device channel lengths are also the distance between the source and the drain. Geometrically, top and bottom gated devices have different layouts slightly deviating from the above images but will remain consistent with an electrically isolated gate and a source/drain pair separated by the semiconducting material.

Commercially, Intel scientists are able to produce sub 14nm channel length silicon based technologies\(^7\). The channel length refers to the distance between the source and the drain which has a major impact on device density driving Moore’s Law, but also on transistor device performance. The thickness of the active semiconductor in the device limits the minimum channel length permissible before the source and drain begin to interact and compromise transistor performance. The characteristic length of short channel transistors with planar structures is shown in the following equation, where \( \lambda \) is the characteristic length, \( \varepsilon_s \) and \( \varepsilon_{ox} \) are the permittivity of semiconductor and gate oxide, and \( t_s \) and \( t_{ox} \) are the thickness of semiconductor channel and gate oxide.
\[ \lambda = \sqrt{\frac{\varepsilon_s}{\varepsilon_{ox}} t_s t_{ox}} \]

The characteristic length for a 5nm thick Molybdenum Disulfide, MoS\textsubscript{2}, transistor on 300nm Silicon Oxide, SiO\textsubscript{2}, is 35.6nm. If the 300nm SiO\textsubscript{2} gate oxide is replaced by 6nm Hafnium Oxide, HfO\textsubscript{2}, with an equivalent oxide thickness, EOT, of roughly 1nm, the characteristic length is 2nm. Intel’s current roadmap indicates 14nm transistors are the current state of the art, SOTA. Many predict 5nm transistors to be the threshold for Moore’s Law. Alternatives to silicon, or at least silicon in a planar geometry, will have to be considered if the doubling trend is to be extended.

There are two main types of transistors which are the bipolar junction and the metal oxide semiconductor field effect transistor, MOSFET. Typically in a device involving a semiconductor and a metal connection, there is an interfacial energy barrier for electron transport called the Schottky barrier which limits current flow due to the mismatch in electronic energy levels dictating transport across the interface. This barrier necessitates more electron injection than is necessary for device operation; therefore, reducing the Schottky barrier improves device performance. A metal-semiconductor interface with a low Schottky barrier is referred to as an Ohmic contact. The source and drain are metallic materials that operate as the terminals of the transistor switch, where current flows from one connection to another when the switch is activated, otherwise known as the ON state. Semiconducting materials have two modes (ON and OFF) which are selected by application of a bias to a dielectric gate via the field effect.

Referred to as Field Effect Transistors (FETs) the semiconductor is either conducting or insulating depending upon the controlled and applied gate voltage. The metallic gate material connection is used to apply a bias via the gate dielectric in order to switch the MOSFET from depletion mode into enhancement mode between the source and drain contacts. Depletion mode is when the polarity of the gate voltage depletes the semiconducting channel eliminating
charge carriers. Conduction is inhibited between the semiconducting material source and drain from having any majority carriers and remains in the OFF state. Enhancement mode is when the gate voltage applied enables the semiconducting channel to pass current via majority carriers from the source to the drain and move into the ON state\(^8\). Depending on the majority carriers whether holes referred to as ‘p-type’ transport or electrons as ‘n-type’ transport, the MOSFET can either switch from the depletion mode to enhancement mode (OFF to ON) or enhancement mode to depletion mode (ON to OFF). Traditional MOSFETs operate from OFF to ON with a n-type active layer, with electrons as the majority carrier. Figure 2 shows typical transistor behavior for a swept gate voltage as the abscissa, \(V_{\text{gs}}\), with the drain current (current flow between source and the drain) as the ordinate, \(I_d\), and different curves for varying drain source voltages, \(V_{\text{ds}}\).

\[\text{Figure 2: The Drain Current Versus Swept Gate Voltage with an Applied Drain Bias for a Working Transistor}^{10}\]

The higher current plateau is representative of the ON state and the lower current corresponds to the OFF state. Extrapolating values from the curve characteristics, the subthreshold swing (SS) is the derivative of the steepest portion of the slope between the ON and OFF state, sometimes referred to as the switching regime. The switching regime is a particularly useful metric for evaluating the utility of semiconductor material in sensing applications, where the measured resistance from a small change in the surface potential from
adsorbed molecules is maximized. Mobility calculations for the semiconducting material and ease of manufacturing determines if n-type or p-type MOSFET semiconductor material would work better.

Semiconducting materials such as Molybdenum Disulfide, MoS$_2$, shows great promise as an extremely thin material (<10nm). Mechanical exfoliation and Chemical Vapor Deposition (CVD) synthesized devices are currently being researched for MoS$_2$ transistor performance$^{10-11}$. In departure of previous and ongoing literature, analysis of MoS$_2$ transistor performance using Physical Vapor Deposition (PVD) as a deposition technique is investigated.

1.1.1. Mechanical Exfoliation and the Birth of 2D Electronics

Mechanical exfoliation was the beginning of 2D materials and it is hard to tell the story of advanced synthesis techniques without referencing the discovery of the scotch tape method for graphene$^{12}$. Mechanical exfoliation is the easiest way to obtain the best results for FET and electrical characterization of materials. The synthesis is done by taking a piece of tape and removing a flake of material from bulk graphite, MoS$_2$, or another Van der Waals bonded material. Another new piece of tape is used to remove another layer from the first piece of tape with material. This process is repeated until a monolayer is achieved. A diagram for the process flow is show in Figure 3.
While mechanical exfoliation is a great procedure for investigations of fundamental monolayer material properties, the scalability is clearly limited. Moreover, the technique is marked by thickness non-uniformity and contamination from interactions with the tape and the solvents to remove the desired material. Thus, other techniques began to produce crystalline 2D materials.

1.1.2. Beyond Graphene - Two Dimensional Materials Discovery

Two dimensional (2D) materials began with experimental synthesis of monolayer graphene. In the form of a single atomic carbon layer on SiO$_2$, graphene was produced by repeated peeling of highly ordered pyrolytic graphite, HOPG, with scotch tape$^{12}$. Graphene was presumed to be an extraordinary material with unique electronic conduction behavior and mechanical strength and flexibility beyond any other, which seemed like a combination of properties for leading the world into the next generation of technologies and electronics. As an allotrope of carbon, graphite is a material with a hexagonal lattice, with each atomically flat basal plane held together by strong covalent bonds between carbon atoms. The individual, covalently bound layers are held together (out of plane) by Van der Waals forces. Research into carbon has found many ways to make FET devices and other optoelectronic devices with
ON/OFF ratios of up to $10^3$, which is a low value compared to most conventional semiconducting materials\textsuperscript{13}. The problem arises as pristine graphene is a zero band gap material and there is great difficulty in tuning the band gap to a regime with an OFF depletion mode\textsuperscript{14}. Research to dope and manipulate the band gap has yet to manifest results in graphene with a usable semiconductor band gap that can be optimally used in a 2D device. The maximum bandgap observed in highly doped graphene is 0.14eV which is not within the 1-2 eV band gap range required for high ON/OFF ratios\textsuperscript{15,16}. As a 2D material, graphene didn’t directly lead the world into the next generation of electronics. Indirectly, however, graphene motivated discovery and development of techniques and theory of subsequent generations of new 2D materials. The emergence of graphene spawned research into other 2D materials including: hexagonal Boron Nitride (h-BN), Molybdenum Disulfide (MoS$_2$), Tungsten Disulfide (WS$_2$), and other materials all of which can be isolated into two dimensional forms with very limited defects from bulk material. The first synthesis method began with mechanical exfoliation research as described earlier\textsuperscript{17,18,19}. A long list of 2D materials were found to have the capability to be synthesized by continuously peeling material with scotch tape from bulk material until a monolayer is achieved\textsuperscript{20}. This technique of mechanical exfoliation proved these 2D materials are useful in the opto-electronics field, and other synthesis methods providing uniform large area material growth for 2D materials followed. While mechanical exfoliation has provided the best results for 2D materials as a defect free material and nano-micro scale electronic devices, a feasible industrially scalable synthesis technique is currently unidentified\textsuperscript{14}.

\subsection*{1.2 Nanoelectronics with 2D Materials}

The microelectronic generation is rapidly coming closer to fundamental performance limitations and nanoelectronics are potentially the path forward to future generation electronics\textsuperscript{21}. While electronic devices are scaled down from microelectronics to
nanoelectronics, unique characteristics begin to dictate performance on a quantum level. MOSFET structures based on Silicon in the past decade have not changed the vertical thickness of the devices significantly to increase the ability of FET devices to handle the smallest channel lengths. Thus, the channel length scaling is coming to an end for microelectronics due to fundamental laws and manufacturing costs\textsuperscript{22}. Therefore, new generation electronics including Carbon Nanotube FETs, Graphene nanoribbon transistors, and new semiconductor material FETs are areas of active research\textsuperscript{14,22-23}. Growth methods to create thin film semiconductors and thin film dielectrics dating back to the 1970s is available; however, fully integrated 2D devices are just beginning to emerge\textsuperscript{24}. 2D materials have inherently large surface to volume ratios which create a new class of materials with unique properties not currently well understood. The unique properties open the door to even smaller integrated circuits with FETs as well as hybrid electrical and biomolecular devices\textsuperscript{25}. Also, the thin nature of nanomaterials increases mechanical flexibility and potentially paves the way for flexible electronic devices such as personal sensors, ultra-thin and flexible cell phones, or an e-newspaper\textsuperscript{26}. Before the e-newspapers and cell phones integrated into clothing can exist, all 2D material FET devices need to be created upon flexible substrates\textsuperscript{27}. New materials will need to be investigated to build all 2D generated devices as well as new techniques to deposit the materials.

First, for this work boron nitride, a known electrical insulator, was shown to have promising dielectric properties as a 2D material and enhance carrier mobility of adjacent semiconducting materials. Advanced synthesis methods for wafer-scale applications (> 5 cm\textsuperscript{2}) are pursued\textsuperscript{28}. Secondly, MoS\textsubscript{2} and WS\textsubscript{2} are members of the class of TMD materials that have been produced with significant coverage area constraints. A method of production other than mechanical exfoliation for new electronic devices over large areas is required for the next generation of 2D materials devices\textsuperscript{20}. Thus for continued research beyond 2D mechanically
exfoliated materials, other methods of synthesizing 2D materials for industrial applications are explored in this work.

1.2.1. 2D Transition Metal Dichalcogenide Semiconductor Materials

Discovery of exfoliated graphene in 2004 has prompted research into atomically thin materials due to unique structure and properties at the monolayer level. A semiconductor material with a true bandgap, unlike graphene, is needed in order to make a FET device at the nanoscale level. TMDs can be used as the semiconducting material in electronic devices. TMD materials have a layered trigonal prismatic structure that is shown in Figure 4 for MoS$_2$.

![Figure 4: MoS$_2$ Atomic Structure](image)

This unique atomic structure can be Molybdenum or Sulfur terminated on the plane edges, depending on the dangling bonds. For semiconductors a band gap is required; the band gap refers to the energy level difference between the electronic valence and the conduction band which is important when trying to switch the semiconductor from the OFF to ON state. Monolayer MoS$_2$ devices demonstrate an indirect band gap of 1.2eV in bulk and a direct band gap of 1.9eV when shrunk down to monolayer$^{29}$. Also, MoS$_2$ exhibits an ON/OFF ratio of $10^8$, a low threshold swing of 74 mV/dec, and a mobility of $17 cm^2/Vs$ $^{30}$. WS$_2$ is another material in the TMD family that has an indirect band gap in bulk and a direct band gap of 1~1.3eV in monolayer form$^{31}$. WS$_2$, exhibits an ON/OFF ratio of $10^6$ and an electron mobility of $34 cm^2/Vs$. Both MoS$_2$
and WS$_2$ exhibit properties that are useful for nanoelectronic FET devices. Reported synthesis for MoS$_2$ and WS$_2$ semiconductor material include: mechanical exfoliation, chemical vapor deposition (CVD), and physical vapor deposition (PVD)$^{32,33,34}$. While achieving large area semiconducting materials is important to the next generation of FET devices, the other layers in the MOSFET structure are just as important.

1.2.2. 2D Dielectrics

Electrically insulating dielectrics don’t conduct electricity and can be polarized to create a field. The most commonly used dielectric is SiO$_2$ and is considered the standard dielectric material in terms of usability and performance$^{35}$. Dielectrics can be solids, liquids, or gases. The purpose of the dielectric in a FET device is to apply the field effect to the semiconductor material and alter the device into the enhancement mode or the depletion mode depending on the voltage applied. Dielectrics are measured in terms of their ability to store the electrical energy when a voltage is applied$^{36}$. Dielectrics are quantified in terms of their permittivity, $k$, also known as their dielectric constant. The dielectric constant, $k$, is taken from the following expression:

$$k = C \times d/A$$

The dielectric constant equation uses $C$ as the capacitance, $d$ as the thickness, and $A$ as the cross sectional area. High $k$ dielectrics are better than the lower $k$ dielectrics in terms of performance as an insulator and applying a field effect. If the dielectric underlying an electrically active layer has pinholes or other discontinuities there will be current that is able to effectively penetrate the dielectric with a low resistance and the dielectric will be ineffective for application of the field effect to turn the transistor ON and OFF. One promising 2D layered dielectric material is Boron Nitride, BN, which can be achieved via mechanical exfoliation or Chemical Vapor Deposition. Another technique used to make dielectrics is Pulsed Laser
Deposition (PLD) of thin films which has been used and characterized since the 1970s and is still in use today. In deviation from the traditional and previously characterized PLD techniques, amorphous Boron Nitride, a-BN, depositions are analyzed for 2D materials characteristics. Investigation of the thinnest dielectrically viable PLD a-BN for 2D materials is conducted. Hexagonal Boron Nitride has shown to be an atomically smooth surface that is free of dangling bonds with a lattice constant similar to graphene and MoS$_2$, both properties which enhance device performance and mobility. Therefore, new processing conditions involving PLD and characterization of the dielectric feasibility over areas of 1 inch diameter for a-BN with all 2D material components is of high interest and will be investigated. To realize molecularly thin circuitry in MOSFET and other devices, semiconductor and dielectric materials are needed, but so are connection metals as conductors.

1.2.3. 2D Conductors

Conductors are materials that pass electricity freely from one location to another with a very low resistance. Typically conductors are metals but conductors can also be doped materials or metallic ceramics and some TMD compounds are also good electrical conductors. Easy flow of electrons is needed for the source/drain contacts and the back or top gate material for a FET device shown in Figure 1. Most commonly used source/drain contacts are layered Titanium, Ti, and Gold, Au, depositions. This combination of contact materials is ideal in many cases due to the reactive, and adhesive nature of Titanium due to the many unpaired d-electrons that form intimate contact with many surfaces. The titanium reacts with the surface it is deposited upon, but also reacts with the atmosphere if exposed. Therefore, Gold is layered on top to passivate the connecting Titanium, blocking its surface from atmospheric exposure.

The back gate connection also needs to be a conductor of electricity. Silicon, Si, can be heavily doped to 0.001-0.005 Ohm-cm resistivity levels either with Boron, B, or Arsenic, As, to be
p-type or n-type, respectively. A thermal oxide, TOX, also known as \( \text{SiO}_2 \) on Silicon can be grown commercially quite easily for the dielectric layer as well. Traditionally a Silicon wafer with a TOX on top is used because these wafers are commercially available from various suppliers and offer the first few layers of effective MOSFET device architectures.

Another way to generate a back gate is to deposit conductive Titanium Nitride, TiN, via reactive sputtering which has advantages as it is a chemically inert material with substantial electronic conductivity, unlike most metals. Tungsten, W, is another common electrode material with reasonable stability in ambient environments and can be deposited as a contact via Physical Vapor Deposition\(^1\). The ability to locally deposit the back gate material in desired locations offers control over the area and shape of the device. From a combination of the semiconductor, dielectric, and conductor layers, MOSFET devices can be built and analyzed from different thin film synthesis techniques.

### 1.3. Ultra Thin Material Synthesis Methods

Various methods of creating 2D materials are available, and each method has its unique advantages and disadvantages. The major synthesis methods include Chemical Vapor Deposition, Magnetron Sputtering, and Pulsed Laser Deposition.

#### 1.3.1. Chemical Vapor Deposition Synthesis

Chemical Vapor Deposition (CVD) is a technique used for generating high quality materials. CVD processes are often used in the semiconductor industry and can be used to synthesize 2D materials. A wafer or substrate is inserted into a furnace with precursor materials and a background gas flow through the chamber. The substrate is heated to sufficient and optimal conditions (often very high temperatures >700°C for TMD synthesis) for a reaction to occur between the precursor materials and the surface. The reacted species then diffuses or
reacts on the substrate surface to effectively deposit the material on the surface. A MoS$_2$ CVD chamber setup is shown in Figure 5$^{43}$.

![CVD Chamber Diagram for MoS$_2$ Deposition Growth](image)

**Figure 5: CVD Chamber Diagram for MoS$_2$ Deposition Growth$^{43}$**

The specific reaction in Figure 5 setup uses Sulfur, S, to react with and convert Molybdenum Trioxide, MoO$_3$, into MoS$_2$. CVD reaction mechanisms and types are not the focus of this work, but the ability to produce crystalline MoS$_2$ over large areas for industrially scalable techniques is a priority. There are many different types of CVD reactions that have been proven to make crystalline semiconducting MoS$_2$ and WS$_2$ devices$^{11,41}$. CVD techniques require high temperatures, above 700°C, and growth on specific substrates, most commonly SiO$_2$ substrates. Deviating from SiO$_2$ growth 2D materials grown on Cu foil have shown to have better nucleation and growth for graphene and MoS$_2$.$^{43-44}$ Growth on Cu foil works very well and provides triangular crystal domains of up to 5µm for MoS$_2$, but the material needs to be transferred via peel and lift off techniques$^{45}$. There are direct methods for growing MoS$_2$ on SiO$_2$ for device making, but the discontinuous islands of material that typically form are limited in terms of large area coverage$^{43}$. Figure 6 shows the structure of MoS$_2$ grown on Cu foil and transferred to SiO$_2$.

![MoS$_2$ Triangular Grain Growth on Cu Foil and Transferred to SiO$_2$](image)

**Figure 6: MoS$_2$ Triangular Grain Growth on Cu Foil and Transferred to SiO$_2$$^{43,46}$**
Comparatively to 2D MoS$_2$ CVD deposition results, BN can also be deposited via CVD. The same structure and of discontinuous triangles and small grain sizes, 1µm, also plague h-BN from industrially scalable growth techniques. Additionally, h-BN requires a transfer process which is not conducive to current industrial applications$^{47}$. MoS$_2$ semiconductor based devices can still be made from these techniques and have shown promise in the FET, sensing, and optoelectronic regimes, but different growth mechanisms and techniques are paramount to finding ways to build full scale processing technology for continuous films at low temperatures for flexible devices. Therefore, MoS$_2$ and WS$_2$ Physical Vapor Deposition is pursued in this work as a method for growing crystalline 2D TMD materials.

1.3.2. Physical Vapor Deposition Synthesis

Physical Vapor Deposition, PVD, techniques are another way that 2D materials can be synthesized. There are diverse PVD approaches but all share the common theme of intense energy input into a pure solid material to physically form a vapor that can condense on a surface in ultra-high vacuum (UHV) or in a background ultra-high purity gas$^{48}$. Ultra-high vacuum pressures are on the order of $1 \times 10^{-8}$ Torr or less. Two PVD techniques that are commonly researched in semiconductor materials research are magnetron sputtering and Pulsed Laser Deposition, PLD. In this work magnetron sputtering is used to create crystalline MoS$_2$ and PLD is used to explore generation of BN on various substrates.

1.3.2.1. Magnetron Sputtering Synthesis

Magnetron sputtering is often referred to as simply sputtering and uses a background gas introduced into an ultra clean and UHV environment. The background gas is typically Argon, at low pressures (2-50mTorr) with a target material of ultra-high purity attached to a magnetron gun. A plasma is ignited by the background gas according to Paschen’s Law when a sufficiently
high potential is applied to the target surface. The positively charged argon ions generated in the background gas breakdown are accelerated into the negatively charged target, and the solid material comprising the target is ejected and then condenses on the surfaces within the vacuum chamber, including the substrate\textsuperscript{48}. The magnetron gun uses high power magnets and a power source to generate a confined plume to charge the background gas and attract the charged particles needed to bombard the target and eject material directed towards the substrate. Growth of crystalline, few-layer MoS\textsubscript{2} at low temperatures has been demonstrated with this technique. Figure 7 shows the setup for the depositions\textsuperscript{34}.

![Figure 7: Magnetron Sputtering Deposition of MoS\textsubscript{2}](image)

Magnetron sputtering is one way to generate 2D films over large areas typical of those encountered in industrial semiconductor device fabrication processes. The technique is commonly used for insulators, conductors, and semiconducting materials for devices. Sputtering techniques are explored for the next generation of nanoelectronics of TMDs to be electrically characterized. Also, 2D dielectric large area depositions are explored in conjunction with the sputtering semiconductor depositions.

### 1.3.2.2. Pulsed Laser Deposition Synthesis

Pulsed Laser Deposition, PLD, is a type of PVD involving the use of a high power laser to ablate materials from a solid target material in the form of a plume in UHV or the presence of a low pressure background gas. The laser is pulsed to avoid unwanted heating of the target
material. Pulsed Laser Depositions have been used to generate thin films for decades and depositions for BN as a 2D dielectric are explored in this work\textsuperscript{37, 49}. Shown in Figure 8 is the setup for a PLD system\textsuperscript{28}.

![Figure 8: Pulsed Laser Deposition System Setup with BN Target\textsuperscript{28}](image)

A laser strikes the target material and heats the surface such that a plume of evaporated material moving at supersonic speed is generated. This plume is directed at the substrate material to facilitate deposition on the surface. This synthesis method has been proven to generate many different thin film dielectrics; however, BN as a 2D material has only recently been explored using PLD techniques. Analysis of the material as a dielectric has shown that it is a useful material for development of scalable 2D flexible devices.
CHAPTER II

RESEARCH OBJECTIVES

The objectives of the research were the following:

1. To correlate composition and structure to electronic and optical properties of large area two-dimensional materials synthesized via novel methods.

2. To construct FET devices from 2D semiconducting TMD materials synthesized via novel physical vapor deposition techniques. An example of the heterostructure is shown in Figure 9.

![Figure 9: FET Structure (a) Isometric View (b) Cross-section](image)

Each layer requires a different functional material as a semiconductor, dielectric, and conductor built from shadow masking techniques which will be investigated in this work.
CHAPTER III
EXPERIMENTAL METHODOLOGY

3.1. Sample Preparation

All substrates were prepared by cleaning in solvent solution prior to any material growth. The cleaning procedure used includes: ultrasonicating samples in semiconductor grade acetone for 15 minutes, rinsing in semiconductor grade methanol, sonicate in methanol for 5 minutes, rinsing in DI water then drying the samples with blown N₂. The main substrates used include highly doped p-type and n-type silicon wafers with a resistance of 0.001-0.005Ω-cm, with a 300nm of thermal oxide (TOX) on top of the wafer; sapphire wafers with <0001> orientation are also used for MoS₂ depositions. Both substrate types were purchased from Virginia Semiconductor and University Wafer. Samples were then loaded into a UHV chamber pumped to pressure of less than 1 x 10⁻⁸ Torr, using 2.5cm diameter ‘blanks’ as holders for the samples via a vacuum load-lock and mounted on an electrically grounded, heated, and rotatable fixture. Samples were not cleaned according to the rinsing procedure defined if a previous material was already deposited, as this surface, freshly coated with high purity metals in a UHV environment, could not be much cleaner. The background gas was selected based on the requirements for the material characteristics desired. For all the different depositions the adjustable processing parameters were: substrate temperature, deposition time, annealing time, pre-loading the chamber with additional sulfur, and background gas pressure. Pre-loading conditions describe a process where the substrate holder with WS₂ to add additional sulfur into
the UHV chamber prior to annealing the substrate. The time for each sample spent out of UHV was limited between growth techniques in order to limit oxidation effects and dust accumulation on the surface. A typical time spent out of vacuum from layer to layer is roughly 10 minutes. This amount of time was required for application or removal of shadow masks for subsequent layers in the device architecture.

3.2. Materials and Architecture for Back Gated Transistor Devices

Certain devices were created by application of a metal for a back-gated electrode which was deposited on 1 inch diameter substrates of silicon oxide or sapphire. The back gated shadow mask design is shown in Figure 10.

![Figure 10: Shadow Mask Design for Back Gated Material Deposition](image)

3.2.1. Tungsten Back Gate Deposition

Room temperature Tungsten depositions were done with a background gas flow rate of 30 sccm, pressure of 2.5 mTorr, and 40 Watts power to the sputtering gun for a total of 10 minutes. These processing conditions resulted in a roughly 30nm thick Tungsten metal film. To

Titanium Nitride, TiN, or Tungsten, W, were deposited inside a UHV chamber with base pressures less than $1 \times 10^{-8}$ Torr using magnetron sputtering. A 1inch target of 99.999% pure metals were used for the deposition.
ignite the target the pressure was initially set to 15mTorr and brought down to 2.5mTorr within the first few seconds of the Tungsten deposition. This process was developed in the course of previous work done at AFRL by Amber Reed because of the exceptionally smooth nature and a-BN affinity to grow on Tungsten.

3.2.2. Titanium Nitride Back Gate Deposition

For the Titanium Nitride deposition a similar process was used for the depositions that occurred in UHV with pressures of less than $1 \times 10^{-8}$ Torr. A 1 inch magnetron sputtering target of 99.999% pure Titanium was used. The background gas was a mixture of N$_2$ and Ti which was varied until optimum results on a reactive sputtering hysteresis curve, where the maximum reactive gas flow rate was identified by watching for a pressure increase due to saturation of the reactive Ti metal applied inside the system. A total gas flow of 25 sccm (inert and reactive) and power of 70 Watts were selected for all depositions. Temperature was varied from room temperature to 500°C, pressure was varied from 2-5mTorr, and the time was varied from 30 minutes to 120 minutes to identify the conditions yielding the desired thickness. Table 1 shows the sample progression until the desired results were achieved.

<table>
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<tr>
<th>Sample</th>
<th>Power (W)</th>
<th>Total Gas Flow (sccm)</th>
<th>N$_2$ (%)</th>
<th>Ar (%)</th>
<th>Pressure (mTorr)</th>
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To achieve the lower pressures the background gas was initially set to 15mTorr to ignite the target and then the pressure was brought to the lower sputtering pressure. The depositions were optimized and the heterostructures that used Titanium Nitride as a back gate were always grown with the optimum conditions. A Fluke 87V meter was used to test the electrical conductivity of the films and atomic force microscopy, AFM, was used to evaluate the roughness of the materials. The main parameters being optimized were the conductivity and the smoothness of the films. After the back gated layer was grown the second dielectric layer of a-BN could be grown.

3.2.3. Dielectric a-BN Deposition

PLD can be used to deposit various materials and for this study a stoichiometric, 99.9999% pure BN target was used to deposit a-BN onto many different substrates. The laser used for depositions is a Lambda Physik LPX300 248nm KrF excimer laser with a pulse energy of 900 mJ/pulse, 30ns duration, and 1 Hz frequency. The spot size of the laser is 2.66mm x 1.50mm. Samples were all heated to 200°C by a joule heated tungsten filament for all depositions controlled by a thermocouple. A N₂ background gas flowing at 30sccm was used at 50mTorr to optimize the film composition. The number of pulses was varied in order to obtain the thickness dependence on dielectric properties. Low temperature growth at substrate temperatures, <200°C, was investigated to allow a-BN growth on flexible substrates. This film recipe was known to yield continuous BN films, however the electrical properties were unknown. To measure dielectric properties, a layered stack architecture had to be synthesized. The stack consisted from top to bottom of Tungsten, a-BN, Titanium, and Gold deposited on a 1inch diameter SiO₂ wafer. Portions of the shadow mask layers were used as shown in Figure 11.
Figure 11: Drawing of the Dielectric Measurement Stack for a-BN Without Titanium and Gold Contacts

Figure 11 shows the stack before the contacts are placed. The W on the bottom of the layer allows access with electrical probes without poking through the dielectric a-BN during testing. The top contacts of Titanium and Gold were deposited after the a-BN deposition. The a-BN layer is the second layer in the analysis of the AFRL dual gated device architecture and the contacts were the third step towards fabrication of the dielectric test devices. A photograph of an a-BN dielectric heterostructure, as tested in dielectric property measurements, is shown in Figure 12.

Figure 12: Image of a Heterostructured W, a-BN, and TEM Mesh Ti/Au Contacts on SiO$_2$ Device
The Gold circular pads are the areas where the top contacts are connected and the silver colored Tungsten is the area where the back gate connection is achieved in order to test the device.

3.2.4. TMD Depositions Including MoS$_2$ and WS$_2$

Magnetron sputtering is the specific type of PVD technique employed for growth of MoS$_2$ and WS$_2$. One inch pure MoS$_2$ and WS$_2$ targets are used in a UHV growth system with \textit{in situ} XPS analysis. A 3.3cm diameter magnetron sputtering target of 99.95% pure MoS$_2$ or 99.5% pure WS$_2$ is used. All MoS$_2$ depositions were done with pulsed sputtering at 30W, 65Hz, and 0.4$\mu$s reverse time while all WS$_2$ depositions were done with pulsed sputtering at 35W, 60Hz, and 0.4$\mu$s reverse time. A background gas of flowing Argon at 25sccm was introduced during deposition at a pressure of 15mTorr for MoS$_2$ and a pressure of 20mTorr for stable plasma generation with a WS$_2$ cathode. In contrast to typical sputtering of TMDs, a magnetic field was used to steer high energy ions away from the growing film surface. The steering mechanism allows primarily neutral species to deposit on the surface, and reduces damage to the ultra-thin films (>3 nm) from energetic particles. Thus, wafer-scale, semiconducting MoS$_2$ and WS$_2$ films are achievable when the materials are able to crystallize.

An additional variable in the study included sulfurization of the chamber surfaces prior to growth (5-20 minutes), growth temperature (200-600$^o$C), annealing time (30-60 minutes), annealing temperature (200-600$^o$C) and the deposition time (12-60 seconds) which gave different results for electrical characterization of the materials. The main criteria used to identify optimized growth parameters was stoichiometry of the films measured via XPS analysis, and the degree to which the films crystallized as determined by Raman spectroscopy. After those parameters were identified, electrical contacts of a thin titanium layer followed by a passivating gold layer were applied by sputtering.
The sulfurization enhancing process used was: deposit semiconductor materials at room temperature from sputtering techniques, move the sample into the load-lock, coat the substrate can for 20 minutes with either TMD and then bring the sample back to the substrate holder and anneal the sample at 600°C for 1 hour.

3.2.5. Electrical Contact Depositions, Specifically Titanium and Gold Depositions

Electrical connection to the semiconductor material via conductive contacts are needed in order to create a MOSFET device. For field effect transistors, the electrical contacts are commonly referred to as the source and drain of the device as described earlier in Figure 1. The source and drain must be separated by some distance referred to as the channel length also seen in Figure 1. To create a series of multiple source-drain contacts, TEM meshes (used for sample preparation in the transmission electron microscope) of various dimensions were used in order to create a grid structure shown in Figure 13.

![Figure 13: Gilder 400 Mesh Electrical Contact Pads of Titanium and Gold](image)

Metal in the vapor state in a physical vapor deposition process passes through the openings and is blocked by the mesh. Diverse ‘coarseness’ of TEM meshes were obtained to vary the channel length from 5µm to 45µm. The copper meshes were taped with vacuum compatible Kapton tape in order to create a flush surface with little to no space between the mesh and the top of the substrate surface. Shadowing effects occurred when contact was non-flush with the surface.
areas. Other, less-effective, masking techniques resulted in bridging across source to drain, shorting out the circuit and resulting in untestable devices.

Sample TEM mesh masks were taped on top of the MoS\textsubscript{2}. Titanium and Gold contact materials were deposited using magnetron sputtering techniques with the TEM mesh as the source and drain contact mask. Both layers were applied in the same pump down cycle in the UHV chamber to maintain a pristine, unoxidized Ti surface. The depositions had the same conditions, but were run at different lengths in a UHV chamber consistent with that illustrated in Figure 13. Conditions for depositing were as follows: 25 sccm of Argon background gas, 15mTorr pressure, 1inch magnetron target, and 40W power supply. The titanium deposition was done for 3 minutes in duration and gold deposition was performed immediately after for 20 minutes. The samples were then taken for testing to the Keithley Semiconductor Analyzer.

3.2.5.1. Electron Beam Evaporator Depositions

To investigate the effects of the contact application method on semiconducting properties, electrical contacts were also deposited in a Denton UHV evaporator chamber at pressures <1 x 10\textsuperscript{-8} Torr. For the evaporated contacts, chromium and gold were used instead of titanium and gold. Both metals (Cr and Ti) are reported to yield identical characteristics on MoS\textsubscript{2} devices\textsuperscript{51}. Before applying contacts, the same TEM meshes were taped onto the samples as a shadow mask. The chromium contacts were deposited using an electron beam evaporator to a thickness of 30nm. Gold contacts were deposited to a thickness of 60nm. Afterwards, the samples were tested electrically in the Keithley Semiconductor Analyzer to avoid contamination effects from exposure to the ambient environment.
3.3. AFRL Dual Gated Device Deposition

The dual gated device was created using two or more of the techniques in the previous experimental methodology procedures. A typical heterostructure consisted of Tungsten as the back gate, a-BN as the dielectric second layer, MoS$_2$ as the semiconductor, and electric contacts on top of the device. From this the dual gated device was then tested in the Keithley 4200 Semiconductor Analyzer. Figure 14 shows the full layout of the dual gated device without the electrical contacts on top.

![AFRL Dual Gated Device without Electrical Contacts](image)

**Figure 14: AFRL Dual Gated Device without Electrical Contacts**

3.4. Electrical Measurements and Apparatus

A Keithley Semiconductor Analyzer 4200, shown in Figure 15, was used to test the samples for FET properties.
The Keithley analyzes the electrical signals from the probing stations and graphically shows the data as well as stores the information in an Excel file. Abbreviations include: $V_d$ and $I_d$ as the drain voltage and current, $V_g$ and $I_g$ as the gate voltage and current, along with $V_s$ and $I_s$ as the source voltage and current measurements. Beryllium Copper soft probe tips, part number 7H from Micromanipulator, were used for the probing stations with some of them having gold wires silver pasted onto them for an even gentler probing mechanism to avoid puncturing the ultra thin materials from which the devices were comprised. Two probing stations were used for testing in air or vacuum ($1 \times 10^{-5}$ Torr) as shown in Figure 16.
Two different types of measurements were made. The first was the resistance test which consisted of 2 points of connection, purely testing the amount of resistance through that path of the device. Voltage was swept from -1V to 1V and the resistance was extrapolated from the average of the resistances based on Ohms law given in the following equation.

\[ \frac{V}{I} = R \]

Sometimes the range of the voltage sweep was increased to get more data points and test the breakdown voltages of the materials. In addition to the 2 point measurement, a 3 point measurement sweeping gate voltage standard test was done. The three different connections included the source, drain, and gate connections. Source and drain connections were established by contact with the electrical titanium and gold layer on the top of the device. Gate connection was established by using a diamond scribe to eliminate the TOX layer and establish connection to the bare highly doped silicon. The 3 point measurement was for examining the semiconducting nature of the PVD grown MoS\textsubscript{2} material.
3.4.1. Gold Wire Measurement Requirements

Any measurement made with a probing station on thin sample material used a gold wire to connect the probe to the sample surface. Otherwise, the probe would effectively scratch the material or poke through the layer to the under layer. Silver conductive paste was used to attach the gold wire to the probe upon drying. Figure 17 shows the gold wire attached to a probe station holder.

![Figure 17: (a) Gold Wire Silver Pasted to Probing Station and Microscope Images of (b) the Gold Wire Attached to the Probe Tips and (c) the Dangling Gold Wire](image)

The gold wire pasted to the probe was therefore necessary due to the fragile nature of the materials. Soft and thin gold contact pads and MoS$_2$ would become scratched even if a soft copper beryllium probe was used. As also with the dielectric measurements, the a-BN results wouldn’t be obtained due to the extreme thinness of the material without the use of gentle, dangling gold wires attached to the probe tips.

3.4.1.1. Dielectric Permittivity Measurements

A Novocontrol Alpha Analyzer was used to determine the dielectric constant. The scans were done by sweeping 10Hz to 1MHz with an AC driving voltage of 100mV. A standard probe was used for the apparatus for the back gate connection and a gold wire filament was used to connect with the other contact pad on top of the dielectric.
3.5. Surface Analysis

Surface Analysis is required in order to optimize all the layers of the FET device heterostructure. Requirements for surface analysis measurements are a result of the material goal of the specific layer being analyzed.

3.5.1. X-Ray Photoelectron Spectroscopy

X-Ray Photoelectron Spectroscopy, XPS, was performed using SSI and Kratos Ultra DLD spectrometers with monochromatic Al Ka radiation of 1486.6eV operated at pressures below 1 x 10^-9 Torr UHV pressure. The Kratos Ultra DLD typically has less background noise than the SSI instrument and has better resolution. Typically all XPS experiments were done in situ with the semiconductor growths and the SSI is the instrument connected to the UHV deposition chamber. The Kratos Ultra DLD was used for various experiments that were exposed to air, required line scanning, or required more fine focus on a smaller area. Survey and high resolution scans were created in the analyzer program. A large spot size of 700x400 µm$^2$ was used for the samples unless the area was reduced by the presence of mask (referred to as the ‘Death Star Mask’ due to its geometry which is reminiscent of the science fiction icon) for device fabrication, in which case, the spot size was reduced to 150x100 µm$^2$. A fixed analyzer passed energies of 160eV for the survey scans and 20eV for the high resolution scans while the x-rays irradiated the sample surface. Spectra were then analyzed using CasaXPS software with individual peaks fitted to a Gaussian-Lorentzian function to a Shirley background subtraction. CasaXPS includes the sensitivity and photoelectron escape depth variations for the periodic table. Since the XPS was done in situ, the calibration was done according the Sulfur peak positions for MoS$_2$ and WS$_2$ of 162.07eV and 162.63eV, respectively. Sulfur peak positions of the XPS data was shifted to fit the binding energy consistent with the National Institute of
Standards and Technology (NIST) value. XPS provided the exact percentage analysis (to 1 atomic %) via pre-programmed sensitivity factors and curve fitting parameters. Specifically, XPS was used as the analysis technique in order to determine stoichiometric ratios of the samples to try to allow systematic variation which had not been examined previously, but was a parameter of great interest.

3.5.2. Raman Spectroscopy

Raman Spectroscopy was performed with a Renishaw InVia Raman Microscope. Determining the crystallinity of the MoS$_2$ is important because the unique properties of 2D semiconductors are strongly dependent upon the crystalline structure. For all experiments, a 514 nm excitation laser with a power of 5mW was used. The laser power was adjusted in the system in order to ensure the composition and structure of deposited material was not altered by laser heating. Wavelength-resolved elastically scattered light intensity was detected upon radiation of each sample with the excitation laser to measure Raman shift in terms of wavenumber (cm$^{-1}$) on multiple locations for each sample.

3.5.3. Atomic Force Microscopy

Atomic Force Microscopy, AFM, was done with a Bruker Icon AFM. The AFM uses a closed-loop performance to reduce noise and allow for distortion free images. The AFM was used to precisely determine the smoothness of material surfaces (with <1 nm spatial resolution in the z direction) and the surface morphology. AFM images were made using the cantilever with a sharp probe tip at the end which scans the surface analyzing the surface mapping. The sharpness of the tip dictates the minimum size of features that can be resolved with the instrument. When brought into proximity of a sample surface, forces between the tip and sample leading to slight bending of the cantilever. A laser spot that is reflected from the top
surface of the cantilever is focused into an array of photodiodes. Changes in the position of the spot when the cantilever is moved slightly by the surface are detected and translated into a topographical map of the analyzed surface.

3.5.3.1 Conductive Atomic Force Microscopy

Conductive Atomic Force Microscopy, C-AFM, was also done with the Bruker Icon AFM machine. C-AFM mode uses a voltage applied to the tip of the cantilever while the tip is in contact with the surface. Conductive diamond-coated silicon tips are used because of their conductivity and the diamond coating is wear resistant. A current image is made from the magnitude of the measured current along the surface which can be compared to the traditional AFM map of the same sample area. The identification of areas demonstrating higher or lower conductance can be compared to the topography of the sample to determine feature characteristics of the material or layer in question. The spatial resolution of the C-AFM and the electrical mapping of the sample surface offer unique insight on the effective continuity of a layer based on its electrical conductivity. The C-AFM is also gentler than probing the surface which is beneficial for delicate surfaces.

3.5.4. Scanning Electron Microscopy

At times a Scanning Electron Microscope (SEM) was used to image the surface of a material or device. A table top SEM Hitachi TM3030 Plus was used to take most images. The table top SEM was used to measure channel length distances and other surface images. Additionally, a FEI Sirion SEM was used to image the cross section of certain samples in order to extrapolate a thickness of certain layers. This microscope is well-suited for high resolution investigations of surface morphology or layer architectures, where features on the order of 1
nm are expected. The table top SEM is a much simpler device suitable for imaging of features on the order of 1 μm.
CHAPTER IV
RESULTS AND DISCUSSIONS

4.1. AFRL Dual Gated Device

Creation of nanoelectronic devices requires material depositions in the correct areas and in the right order to direct electrical currents only to intended destinations. One technique available for precise placement of materials is shadow masking with physical masks that cover portions of the substrate. In an effort to have a fully PVD grown 2D device, the AFRL dual gated mask layout was made with stainless steel of a thickness of approximately 100 µm in 4 parts to produce a device: 1. the back contact mask for the back gated transistor 2. the mask for dielectric layer deposition 3. the mask for semiconductor layer deposition 4. the mask for top contacts deposition which was either star mask (shown) or a Copper grid (not shown) in Figure 9. An example of the copper grids on a device sample can be seen in Figure 12. Figure 9 shows where the material is deposited and how the layer stacks into a fully integrated device. The masks are the negative images on stainless steel shim. From the AFRL dual gated device architecture each layer was individually optimized for the best parameters. First, the back contact layer was required to withstand higher temperatures without evaporating, maintain electrical conductivity, and remain smooth.
4.1.1. Back Gated Layer - Titanium Nitride Results

A Tungsten recipe was previously known for depositing a back contact, but Titanium Nitride a metallic ceramic was also optimized in order to generate a smooth conductive film, stable at high temperature and with much higher strength than metal contact materials, which is useful for a back contact. Smooth conductive films are needed because the roughness will limit the large area capability of the films to perform correctly when layered. For molecularly thin materials, even small values of surface roughness can compromise the structure. Subsequent layers deposited on the back contact will emulate the morphology of the first layer, therefore it is critical for a 2D device that all layers are smooth. All results for different material growth conditions were ranked with heavier weighting on roughness than on the electrical resistance. The lowest roughness measured by AFM was determined to be the best material provided the resistance was low enough to be considered a conductor. First, the background gas mixture was analyzed and the best films were grown at a 90% Nitrogen and 10% Argon with a pressure of 3 mTorr. At pressures of 2.5 mTorr the magnetron would extinguish and stop depositing material, thus, 3mTorr pressure was required to run the full deposition. All of the resulting films have that background gas for different deposition times and temperatures as the remaining tested variable with 70W power to the magnetron. Table 2 shows the results for the best grown films at 90% N₂ to 10% Ar background gas for TiN.
Table 2: Best TiN Deposited Sample Matrix for Deposition Time and Temperature Variables

<table>
<thead>
<tr>
<th>Sample</th>
<th>Deposition Time (min)</th>
<th>Roughness/R_{rms} (nm)</th>
<th>Temperature (°C)</th>
<th>Resistance (Ω)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TiN – 1</td>
<td>30</td>
<td>-</td>
<td>25</td>
<td>1000</td>
</tr>
<tr>
<td>TiN – 2</td>
<td>30</td>
<td>0.88</td>
<td>500</td>
<td>200</td>
</tr>
<tr>
<td>TiN – 3</td>
<td>60</td>
<td>1.4</td>
<td>25</td>
<td>100</td>
</tr>
<tr>
<td>TiN - 4</td>
<td>60</td>
<td>1.2</td>
<td>500</td>
<td>50</td>
</tr>
</tbody>
</table>

The optimum parameters were found to be TiN grown at 500°C for 30 minutes at 70W magnetron power in a 90%/22.5sccm N2 to 10%/2.5sccm Argon background gas flow at as low as pressure as possible (~3mTorr). Sample 2 was deemed best since the resistance was low enough with a value of 200 Ω, which was suitable for a back gate conductor. This sample was the smoothest TiN. Room temperature depositions at 30 minutes did not produce sufficient conductivity to be used as a back gate. Moreover, the depositions done at 60 minutes were more conductive but had rougher surfaces. Thus, the thinner the TiN, the smoother the material was due to the ability for thin materials to maintain similar smoothness of the substrates at small thickness. Figure 18 shows the AFM of the smoothest deposited film parameters from above. Compared to the melting temperature of titanium nitride of 2930°C, 500°C is a moderate value. This comparison is often referred to as the homologous temperature, which is equivalent to T/T_{m}. In this case, T/T_{m} = 0.24. At this temperature, it is anticipated that nucleation would be enhanced, facilitating nearly homogeneous nucleation, which is of benefit to ultra thin continuous films if island growth, a primary source of roughness, is to be avoided.
Figure 18: AFM Image of Smoothest TiN Deposited Film Grown at 500°C for 30 minutes and 3mTorr of 90% N₂ and 10% Ar

Smooth back gated materials that are extremely thin are available at room temperature and high temperature. The TiN best results are at higher temperatures of 500°C, but TiN can also be used as a back gate when deposited at room temperature for 60 minutes, although surface roughness will be slightly larger for the room temperature growth. Roughness can become larger from layer to layer heterostructure growth. Moreover, the Tungsten recipe can be used for low temperature deposition and the TiN material with the best results can also be used as a high temperature deposition. The next step is to determine a 2D dielectric material that can be integrated to the AFRL device architecture.

4.1.2. Dielectric Layer Results

Effective dielectrics are a top priority when characterizing FET devices, since a leaky dielectric will yield erroneous results during electrical property characterization. Before testing
any devices for semiconductor transistor behavior, a recipe for a leak-free dielectrics was required.

4.1.2.1. a-BN as a 2D Dielectric

A Tungsten back contact, then PLD a-BN, and Ti/Au sputtered contacts were created on top of Si/SiO$_2$ wafers according to each deposition’s individual section which is visually shown previously in Figure 9. These samples were not fully integrated FET devices, but a layered structure with a-BN sandwiched between the two deposited metal layers. The aim of these samples was to allow measurement of the electrical properties of the material. Tungsten was chosen via the previous work of growing PLD a-BN on W due to the strong growth potential for a-BN on W. These wafers were tested with the Keithley Semiconductor Analyzer with the gold wire enhanced probe station out of vacuum in order to prevent poking through the material and mechanically enabling leakage. For a-BN there was no need to test in vacuum due to the inert nature of a-BN. All samples were grown at 200°C, 50mTorr pressure, 30 sccm N$_2$, and laser power of 900mJ/pulse on the W back gate. Different thicknesses of the a-BN gave different results for the resistivity of the films. Table 3 introduces the sample variables and the experimentally determined values for the corresponding samples.

Table 3: a-BN Dielectric Study Parameters List

<table>
<thead>
<tr>
<th>PLD Number of Pulses</th>
<th>a-BN Thickness (nm)</th>
<th>Resistivity ($\Omega$-cm)</th>
<th>Dielectric Constant (k)</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>2.17</td>
<td>$6.86 \times 10^5$</td>
<td>-</td>
</tr>
<tr>
<td>50</td>
<td>3.11</td>
<td>$6.85 \times 10^7$</td>
<td>-</td>
</tr>
<tr>
<td>100</td>
<td>6.00</td>
<td>$7.22 \times 10^{11}$</td>
<td>5.2</td>
</tr>
<tr>
<td>200</td>
<td>16.5</td>
<td>$2.98 \times 10^{12}$</td>
<td>6.5</td>
</tr>
</tbody>
</table>
Table 3 shows the experimentally determined values for the different pulse length depositions.

Figure 19 shows resistivity, in Ohm-cm, versus the thickness, in nanometers, for the 600mesh TEM masked contact pads of 40µm (1600µm²) size squares.

![Figure 19: a-BN Resistivity (Ohm-cm) Versus Thickness (nm)](image)

The resistivity varied logarithmically with thickness which was measured from high-resolution cross sectional SEM images. Number of pulses was used to initially calibrate thickness with 30, 50, 100, 200 pulses of the 900mJ/pulse laser. The Sirion SEM image used to characterize the thickness for the 100 pulse sample is shown in Figure 20.

![Figure 20: Cross Section SEM Image of 100 Pulse W, a-BN, Ti/Au Deposited Sample](image)

From the acquired thicknesses for the a-BN along with a masked metal pattern from a TEM 600 mesh pad area of material coverage (1600µm²), the dielectric constants were experimentally
obtained by setting the area and thickness values into the Novocontrol Alpha Analyzer. Figure 21 shows the dielectric permittivity for the non-leakage bearing samples of a-BN 100 pulses (6nm thick) and 200 pulses (16.5nm thick) graphed versus frequency.

![Figure 21: Dielectric Permittivity Versus Frequency for 100 Pulse and 200 Pulse a-BN](image)

The 100 pulse (6.0nm) and 200 pulse (16.5nm) a-BN deposited films had a dielectric permittivity, \( k \), of 5.2 and 6.5 respectively with an average and estimated error of 5.90 ± 0.65. a-BN can be used as a dielectric material for 2D devices in such a way that is even comparable to the CVD h-BN dielectric constant measurements of 3 ± 1\(^ {47} \).

100 and 200 pulse samples had visible layers in the SEM and experimentally viable dielectric constants. The 30 and 50 pulse samples did not have visible thicknesses in the SEM and their thicknesses were calculated using an extrapolated average value from a regression analysis between the quadratic and linear fit. Additionally the 30 and 50 pulse samples showed leakage through the dielectric. Coalescence and uniform coverage can be achieved by 30 pulses and prove the 30 and 50 pulse samples useful as a dielectric; however, processing the samples without a clean room leads to defects from dust particle accumulation. While the a-BN and the
back gated electrode material have shown promise to be effective as FET layers for 2D materials, the semiconductor properties are the next step to generating a device.

4.2. MoS$_2$ and WS$_2$ Deposited on SiO$_2$ Results

MoS$_2$ and WS$_2$ require stringent structure and compositional tolerances for demonstration of semiconducting properties which can be achieved by PVD sputtering techniques. The materials are insulating when amorphous$^{52}$; thus, Raman spectroscopy was employed as a simple tool to evaluate for crystallinity. Characteristic $E^{12g}$ (in plane) and $A_{1g}$ (out of plane) Raman peaks are observed. Both materials show Raman signals characterized by relatively broad peaks, indicating a film comprised of nanocrystalline domains. MoS$_2$ was grown for 18s at room temperature and annealed at 600$^\circ$C for 1 hour using the pre-loading of the chamber with WS$_2$ technique for the Raman experiments. WS$_2$ was grown for 18s and annealed at 600$^\circ$C for 1 hour using the same pre-loading technique. Once again pre-loading was the process of applying a thick layer of TMD material inside the processing system (with the substrate out of the system) prior to annealing samples at high temperatures (600$^\circ$C). The purpose of this step is to create a sulfur rich environment during the annealing step since sulfur has a high vapor pressure at the annealing temperatures. Characteristic Raman spectra for both PVD grown materials are shown in Figure 22.
Both MoS$_2$ and WS$_2$ have Raman signals which is the first step in determining whether or not a material is semiconducting. MoS$_2$ $E_{2g}^1$ and $A_{1g}$ peaks at 382.56 cm$^{-1}$ and 406.40 cm$^{-1}$, respectively are characteristic of high quality crystalline MoS$_2$. WS$_2$ also had characteristic crystalline peaks at 354.79 cm$^{-1}$ and 417.94 cm$^{-1}$, while the silicon peak is the 521.24 cm$^{-1}$ peak due to the substrate on which the material was grown.

All materials integration into devices were analyzed with the *in situ* XPS immediately after depositing MoS$_2$ or WS$_2$. Early experimentation found the *in situ* XPS results for MoS$_2$ and WS$_2$ deposited at room temperature and annealed at high temperature (600°C) produced sub-stoichiometric films with a S:Mo ratio less than 2 (films without pre-loading). The XPS characterization graphs are shown in Figure 23 and Figure 24 for MoS$_2$ and WS$_2$, respectively.
High resolution XPS scans of Mo are useful for determining the stoichiometry of MoS$_2$. The high resolution scans provide better insight into the electronic orbitals of MoS$_2$, specifically how the Mo and S are bonded. Figure 23(b), has three peaks which include the Mo 3d +4 as the first two and the S 2s peak as the third peak from left to right. Using a sensitivity factor of 9.5 for the Mo and 1.43 provided by Casa XPS for the S peaks, the full width half max areas determine the percentage analysis for the film. The MoS$_2$ film is 44.52% by atomic weight Molybdenum and 55.48% by atomic weight Sulfur according to the high resolution scan fit data which yields a sub-stoichiometric film of a S:Mo equal to 1.25:1. Likewise, WS$_2$ had similar sub-stoichiometric ratios without pre-loading which is shown in Figure 24.
The WS$_2$ film is 29.18\% Tungsten and 39.58\% Sulfur according to survey scan fit data which yields a sub stoichiometric film of a S:W equal to 1.36:1. The sub-stoichiometric films are doped by the sulfur vacancies and demonstrate metallic film behavior. Sulfur vacancies in both TMDs dope the semiconductor and don’t allow the band gap to exist which consequentially doesn’t allow switching behavior. More specifically, the semiconductor won’t turn off with a surplus of vacancies which is shown in Figure 25.

Figure 24: XPS Survey Scan of WS$_2$ Deposited at Room Temperature and Annealed at 600°C

Figure 25: (a) MoS$_2$ Sulfur Vacancy $^{53}$ and (b) Equivalent Band Gap Diagram $^{54}$
The Sulfur vacancies effectively dope the material and the equivalent band gap diagram is shown in Figure 25(b) where both the valence and conduction band are extremely close, effectively making the material conductive. Sulfur deficient films are generated due to the high vapor pressure of sulfur relative to stable MoS$_2$ and Mo. There is significant desorption of sulfur from the substrate and growing films surfaces at processing temperatures above 500°C. Table 4 shows the vapor pressures for Sulfur between 39°C and 644°C.
Table 4: Elemental Sulfur Vapor Pressure\textsuperscript{55}

<table>
<thead>
<tr>
<th>Temperature (°C)</th>
<th>Pressure (Torr)</th>
</tr>
</thead>
<tbody>
<tr>
<td>39</td>
<td>1.0 x 10\textsuperscript{-5}</td>
</tr>
<tr>
<td>59</td>
<td>1.0 x 10\textsuperscript{-4}</td>
</tr>
<tr>
<td>81</td>
<td>1.0 x 10\textsuperscript{-3}</td>
</tr>
<tr>
<td>107</td>
<td>1.0 x 10\textsuperscript{-2}</td>
</tr>
<tr>
<td>141</td>
<td>1.0 x 10\textsuperscript{-1}</td>
</tr>
<tr>
<td>186</td>
<td>1.0</td>
</tr>
<tr>
<td>245</td>
<td>10</td>
</tr>
<tr>
<td>328</td>
<td>100</td>
</tr>
<tr>
<td>445</td>
<td>760</td>
</tr>
<tr>
<td>495</td>
<td>1520</td>
</tr>
<tr>
<td>574</td>
<td>3800</td>
</tr>
<tr>
<td>644</td>
<td>7600</td>
</tr>
</tbody>
</table>

Thus, techniques to improve the sulfur concentration were investigated because of the metallic doping that the sulfur vacancies can introduce.

4.2.1. Sulfur Enhancement of MoS\textsubscript{2} and WS\textsubscript{2} via Pre-Loading

A feasible and workable technique to introduce more sulfur into the system showed an increase in the sulfur concentration of the TMD samples grown on SiO\textsubscript{2}. Figure 26 and 27 show the increased stoichiometric films for MoS\textsubscript{2} and WS\textsubscript{2}.
Figure 26: (a) Survey and (b) High Resolution XPS Scans with Data Analysis for MoS$_2$

Enhancement of the MoS$_2$ film by the sulfur pre-loading process yields 37.81% Molybdenum and 62.19% Sulfur according to the high resolution scan fit data which yields a more stoichiometric film of a S:Mo equal to 1.64:1. The more stoichiometric the film, the better potential for creating a device by eliminating the sulfur doping vacancies. While the MoS$_2$ can coated deposition technique requires more optimization, the WS$_2$ films showed a more sensitive response to the 20 minutes of TMD can coating. Figure 27 shows the XPS survey scan and quantification for the exact sample processing conditions done with WS$_2$ instead of MoS$_2$. 
The WS\textsubscript{2} sulfur enhanced films had a Tungsten atomic percentage of 29.31% and a Sulfur atomic percentage of 63.53% which yielded a S:W of 2.17:1. The ability to control the sulfur concentration is important to generating semiconducting FET devices. As Raman crystallinity is the first step towards making a FET device, the stoichiometry of Sulfur to Metal of 2:1 is just as important for 2D TMD semiconducting materials. The Sulfur concentrations can be controlled and the devices were tested for electrical properties after being sulfur enhanced.

Afterwards, both TMDC showed better stoichiometry in XPS. By coating the can along with the chamber with sulfur, the low vapor pressures of sulfur in vacuum allows the surplus of heated species at 600\degree C in vacuum to diffuse and react on the substrate surface. A higher concentration of Sulfur in the XPS analysis is shown from deposited TMDs with the exact same conditions except for pre-loading and without pre-loading the can. The specific peaks of Mo 2d +4 and S 2s peaks in the high resolution scan also prove that the Sulfur species is bonded to the Mo and not conformably coating the substrate. For PVD of TMDs the stoichiometric control
needs to be enhanced for development of semiconducting devices. Thus, once a process was known to control the stoichiometry of the films, the electrical testing could begin.

4.2.2. Silicon Oxide, SiO$_2$, on Doped Silicon Wafers as Dielectric Structure

While growing different conductor and dielectric layers on various substrates occurred, MoS$_2$ and WS$_2$ semiconductor information could be extracted from depositing PVD semiconductor material on silicon wafers with 300nm (thick) SiO$_2$ dielectric coverage. MoS$_2$ was deposited using various growth times, temperatures, and annealing procedures. Initially, any method growing semiconductor on SiO$_2$ yielded extreme leakage concerns with a 3-point MOSFET measurement which is shown in Figure 26.

![Graph showing Drain Current (Blue) and Gate Current Leakage (Red) Versus Gate Voltage](image)

**Figure 28: Drain Current (Blue) and Gate Current Leakage (Red) Versus Gate Voltage**

The gate current is often referred to as the leakage current for MOSFETs and the drain current is the desired transistor curve portion. Graphically the drain current inverses, but only when the gate current inverses as well which proves that the dielectric is not working and the gate current is allowed a free path to the source and drain. In order to be useful as FET data, the drain current must be one hundred times larger than the gate current and one thousand.
times for industrial applications. This was a major concern since the TOX is very thick at 300 nm and should have whole area coverage. Scribing and grinding the edges where material overlap occurs to the gate was investigated but significant leakage current remained. A schematic of the scribing is shown in Figure 29.

**Figure 29: Elimination of Potential Edge Defects by Scribing**

Since even scribing around the device didn’t yield leakage free devices, C-AFM was done in order to determine a topographical electrical resistivity map alongside the AFM image to determine potential sources of leakage. Figure 28 shows the C-AFM and AFM image of a commercially bought p-type (0.001-0.005 Ohm-cm) 300 nm SiO₂ wafer.

**Figure 30: (a) AFM Image of 10×10μm² Spot Size with (b) C-AFM on the Same Location**
The C-AFM image shows clear spots of higher and lower resistance on the SiO$_2$. This causes concern for pin-hole leakage through the films. Though the AFM image shows the resistance go only as high as femto-amp, the type of spots on the image show a multitude of pin-hole type leakage areas. Finding the source of large area leakage is difficult, but the C-AFM map provides clear reasoning to potential leakage. To further investigate the leakage problems MoS$_2$ was grown in a confined rectangular area of 0.3in x 0.1in in at the center of a 1inch 300nm SiO$_2$ wafer. A test of resistance was done with a Fluke voltmeter before and after MoS$_2$ growth at the location of the deposition by contacting the highly doped silicon to the positive terminal and the SiO$_2$ (before growth) and MoS$_2$ (after growth). The results are shown in Figure 31.

Figure 31: (a) Post MoS$_2$ Deposition on SiO$_2$ (b) Electrical Resistance from SiO$_2$ to Conductive Wafer Before MoS$_2$ Deposition (c) Electrical Resistance After Deposition from MoS$_2$ to Conductive Wafer

From the generated images clear leakage concerns are shown for the wafers after the MoS$_2$ deposition. Generating large area MoS$_2$ has been developed, but manufacturing large area insulating material was a device architecture concern. Large area devices require quality insulating materials with no defects over the whole surface. Unlike semiconductor materials, if an insulator has one defect the entire dielectric fails and is unusable. Experimentally, an additional layer of a-BN coverage over the SiO$_2$ did not show a decrease in leakage current. Devices made from SiO$_2$ and a-BN heterostructured did not yield working dielectric performance over large areas >1600$\mu$m$^2$. Pinholes found in the SiO$_2$ were not fully covered by the additional
a-BN layer. This makes finding and using large area 2D dielectrics difficult for the future of nanoelectronics. Despite the leakage problems over large areas, certain procedures were implemented to reduce the area of the MoS$_2$ and WS$_2$ depositions. The Death Star Mask, DSM, was created in order to reduce the area of the semiconductor deposition and increase the likelihood of a useful dielectric free of pinholes. Figure 30 shows the dimensions in inches for the DSM along with the 1 inch substrate holder with the DSM attached.

![Figure 32: Death Star Mask (a) Dimensions in Inches (b) Holder and (c) MoS$_2$ Deposited Sample](image)

The DSM is an additional shadow mask that overlays the initial substrate to limit the area of semiconductor grown. The results of the DSM show that the reduced area is pivotal to creating a leakage free device when working with SiO$_2$ back gated wafers. From the DSM the unique properties of PVD semiconductors could be analyzed when having a field effect applied. Not all of the generated spots from the DSM deposition are useful for testing devices. Some of the MoS$_2$ pads generated from the DSM were overlaid on a significant point of leakage and no device data could be gleaned from those samples. However, roughly two thirds of the pads were on top of quality SiO$_2$ that can be used as an insulator and device data was generated from those sample spots.
4.3. Electrical Characterization Results for MoS$_2$ and WS$_2$ on SiO$_2$

Back gated devices were made with the Death Star Mask overlay from highly conductive silicon wafers with 300nm of SiO$_2$ on top. After the semiconductor was deposited, Titanium and Gold contacts were created using 100 Mesh TEM grids which had a channel length of about 45µm. Similar TEM mesh contact pads with smaller channel lengths were difficult to electrically probe due to the proximity of the electrical test connections. Often the attached gold wires would touch and create an artificial source drain conducting connection. The entire processing deposition is described in the experimental methodology. Figure 33 shows a tested sample.

![Figure 33: MoS$_2$ FET Device Back Gated from Doped Si Wafer with 300nm SiO$_2$](image)

The devices were tested for FET switching behavior with the doped Si wafers with 300nm TOX. Only TEM mesh Titanium and Gold deposited contacts that were placed over the DSM deposited MoS$_2$ and WS$_2$ exhibited a working dielectric. The DSM deposited semiconductor yielded a successful dielectric 66% of the time while the TEM pads yielded a testable success rate of 40%. The XPS characterized MoS$_2$ with sulfur enhancement showed interesting electrical properties out of vacuum for a swept gate voltage from -25V to 25V that are shown in Figure 34.
Figure 34: MoS$_2$ Drain Current Versus Gate Voltage for S:Mo of 1.64:1 (Sulfur Enhanced)

The device has a working dielectric which can be seen by the extremely low gate current ($\sim 1 \times 10^{-8}$) leakage. Gate current leakage has one spike which is not repeatable and could be due to the building vibration and not a true dielectric current measurement. However, the main concern is being able to turn the device OFF into the depletion mode for the majority carriers. The other observation includes that the resistance of the device seems to be increasing over time and accounts for the wing shaped drain current data. The MoS$_2$ material not being able to be turned off was partially due to the Sulfur vacancies which lead to the creation of the over stoichiometric WS$_2$ device of a 2.17:1, S:W ratio. Sulfur vacancies effectively act as dopants increasing the metallic characteristics of the semiconductor. Due to the extremely high surface to volume ratio the Sulfur has an exponential effect as a dopant. The WS$_2$ with an extra pre-coat
processing condition had a surplus ratio which eliminates any Sulfur metallic vacancies. The Sulfur enhanced electrical properties for the device are shown in Figure 35.

\[ \text{Figure 35: Sulfur Enhanced WS}_2 \text{ Drain Current Versus Gate Voltage for S:W of 2.17:1} \]

The over stoichiometric WS\(_2\) devices also had a working dielectric which is consistent with the low gate current values. However, the devices also did not turn OFF. The current stays in a very tight window and shows movement, but not enough to process any signal or be considered a FET device. Once again the second observation was that the resistance of the source drain channel length seems to increase over time. Electrical testing in vacuum will eliminate some oxidation effects. Moreover, alluded to previously, even the best shadow masks will show some type of edge smearing. Figure 36 shows the size and potential of the contacts to smear and be rendered useless.
Despite the large channel lengths and the smearing, there were a number of contact pads that were isolated and usable for electrical characterization data. However, using lithography techniques is extremely important for a path forward for PVD deposited materials in order to get smaller channel lengths and better electrical characterization. Shadow masking has the ability to characterize certain aspects of the TMD devices out of vacuum though limited in scope. The second observation for the drain current becoming more resistive can be a result of environmental degradation and a reduction reaction with Oxygen.

4.3.1. Environmental Degradation of TMDs

The unique 2D properties yield materials with a high surface to volume ratio which are extremely reactive and sensitive to the environment. To investigate a gate voltage of 20V was held and the drain source of 1V was also held constant and graphed versus time. Figure 37 shows the results of the held gate and drain voltage over time.
Figure 37: Drain Current and Gate Current Versus Time with Held Gate Voltage and Held Drain Voltage

The gate current looks like a capacitor charging which is in accordance to the structure of the device which does not affect the drain current. However, the drain current is decreasing with what appears to be a constant rate overtime. Once again the unique 2D surface to volume ratio being extraordinarily high allows oxygen to react with the device channel and become increasingly resistive overtime. Moving forward from the obtained results, the next step is to test the devices in vacuum to eliminate the effects of oxygen. The vacuum probing system was set up for the 3 point measurement with the source, drain, and gate connections. Figure 38 shows the results of sweeping the gate voltage of a MoS$_2$ device in vacuum.
The gate is swept to a much larger range from -100V to 100V, but the inability to turn the device to the OFF state remains. An ambipolar drain current graph is seen, but the response is extremely minimal and cannot be considered an ambipolar FET device. The response is 9.55E-6 OFF vs 9.66e-6 ON and is a percent difference of 1.14% which is negligible at the current operating regime. The effects of Oxygen appear to be eliminated, but a further investigation is required in order to make that conclusion. Two tests were done over a 30 minute period (1800s). An out of vacuum test was performed when the pump was off and compared to the results of an in vacuum test for a held gate voltage of 30V and a source drain voltage of 1V. The out of vacuum and in vacuum results are shown in Figure 39.
Figure 39: Amount of Amps Decrease Versus Time for In and Out of Vacuum MoS$_2$ Devices

The device that was tested used the same source and drain locations for both the in and out of vacuum tests. First the device was tested in vacuum which is the green curve, then the device was subjected to out of vacuum testing which is the purple curve. A clear difference can be seen in the amount of decrease in current which is directly correlated to increase in resistance of the device over 30 minutes (1800s). Once a certain resistance was tested a lower resistance was not recorded, this is why an amount of electrical decrease in current is used and not the actual resistances. This ensures that the pattern of current decrease is obtained and not an arbitrary percentage. Out of vacuum the device becomes more resistive faster than when in vacuum. Cycling testing in vacuum and out of vacuum yield completely different results for the same spot size for a traditional swept gate voltage versus drain current which are the drain current versus gate voltage. Out of vacuum tests produce signals similar to Figure 34 and 35 while the in vacuum tests produce the ambipolar response shown in Figure 38. The device wing
shape of the drain current will continuously decrease over the swept gate voltage (with time) and when in vacuum a miniscule ambipolar response will occur. While generating working devices may not require testing 2D materials in vacuum, testing in vacuum is ideal to get the best electrical responses. Thus, unreactive traditional materials in bulk become more sensitive to oxygen at the monolayer thickness. A unique interest for passivation layers is of high importance in the 2D materials world. a-BN is useful as a dielectric and can be used as a passivation layer for 2D MoS₂ to prevent Oxygen from increasing the channel resistance.

### 4.3.1.1. a-BN as a Passivation Layer

In response to the oxidation effects, a conformal coating of a-BN was explored to decrease the oxidation over time. Since a-BN is highly unreactive and atomically smooth, the a-BN doesn’t allow Oxygen diffusion through the surface to a reactive MoS₂ Sulfur vacancy. To explore a-BN as a passivation layer, MoS₂ was grown at room temperature and annealed at 600°C on sapphire wafers with Ti/Au contacts deposited on top with 100 TEM mesh grids. Samples then had a-BN deposited by PLD with 5, 10, and 20 pulses with a control sample with no a-BN deposited. Since there is no conductive back gate or dielectric layer a simple two point resistance measurement test was done on four different locations for each sample totaling 16 data points. The average percent increase in resistance was tracked and shown in Table 5.

#### Table 5: Percentage Increase in Resistance After 24 Hours for a-BN Deposited Samples

<table>
<thead>
<tr>
<th>Sample</th>
<th>0 Pulses</th>
<th>5 Pulses</th>
<th>10 Pulses</th>
<th>20 Pulses</th>
</tr>
</thead>
<tbody>
<tr>
<td>After 24 Hours</td>
<td>234000%</td>
<td>93000%</td>
<td>259%</td>
<td>284%</td>
</tr>
</tbody>
</table>

a-BN has an application as a dielectric and also as a passivation layer. The samples took an appreciable thickness past 10 pulses in order for the samples to have appreciable coverage to
prevent Oxygen from diffusing though the pinholes. 2D materials are highly sensitive to Oxygen and there are ways to mitigate the effects to produce better devices.

4.4. AFRL Dual Gated Device FET Results

In hopes that the SiO₂ was not the best material for depositing 2D PVD MoS₂, a successful dual gated device was created. A fully integrated AFRL device was created using the masking layers for the W back gate, 300 pulse a-BN, 45 second MoS₂ DSM deposition with 100 Mesh TEM grid contacts of Ti/Au. Figure 40 shows the 3 terminal electrical test for the device.

Figure 40: AFRL Generated Device 3-Terminal Measurement for a Swept Gate Voltage

The device once again did not show the switching behavior typically accompanying operation of a FET. The device did however, show a fully working W and a-BN shadow masking technique that can be used for 2D materials on various substrates at low temperatures. While there are many avenues to generate higher quality MoS₂, fully adaptable techniques are
available to deposit nanoelectronic devices on many different substrates. Physical Vapor Deposition could be the next revolutionary breakthrough for semiconducting thin film materials.
The research objectives stated previously were the following:

1. To correlate composition and structure to electronic and optical properties of large area two-dimensional materials synthesized via novel methods.

2. To construct FET devices from 2D semiconducting TMD materials synthesized via novel physical vapor deposition techniques. An example of the heterostructure is shown in Figure 9.

While a working FET device from 2D semiconducting TMD material device was not created, Physical Vapor Deposition Techniques are highly adaptable techniques that can be used for semiconducting 2D materials with slightly more optimization. The advantages of 2D material device processing using physical vapor deposition were demonstrated to include:

1. Low temperature (<200°C) growth of all components of a semiconducting device
2. Large area growth
3. Simple fabrication methods to create devices (using physical masks only)
4. No contamination during processing due to UHV environment

The current 2D materials field has working TMD transistors created from Chemical Vapor Deposition and Mechanical Exfoliation. In this work the challenges associated with fabrication of fully integrated Physical Vapor Deposition nanoelectronic devices have been identified. PVD has a number of attributes suggesting that it may become a leading technique for 2D electronic
device fabrications, but currently there are no 2D PVD nanoelectronic devices that have been created.

All materials (conductors, insulators, semiconductors) were synthesized using PVD techniques. First, very smooth (<1 nm roughness), electrically conductive materials can be grown as back gated materials fully buildable into FET devices. Tungsten and TiN are two examples showing great promise as electrode materials suitable for underlying contacts in devices based on 2D materials that maintain structure and continuity. Their smoothness also allows layered heterostructures for dielectrics to be deposited uniformly and perform correctly.

Second, a-BN is a high performance dielectric that works within devices comprised of 2D materials. Between 6-16nm, a-BN is able to maintain a field effect and remain leakage free. a-BN is also very smooth in nature and allows for Transition Metal Dichalcogenides to be deposited on top. Also, low temperature Pulsed Laser Depositions allow a-BN to conformably coat a wide range of flexible materials while maintaining dielectric performance.

Third, crystalline and stoichiometric MoS$_2$ and WS$_2$ PVD deposited materials are achievable. However, transistor FET performance is not yet achieved by Physical Vapor Deposition methods. Conduction through the channel is the experimentally identified problem. The two largest issues that will need to be addressed are the sulfur vacancies and the grain size. Sulfur vacancies will always cause the MoS$_2$ to be conductive, and creating a stoichiometric crystalline film is pivotal for semiconductor behavior. Also, larger channel lengths than crystalline semiconductor links are introduced between crystalline locations. The links between the grain boundaries acting as effective conduction pathways will need to be investigated for further insight into 2D semiconducting materials. Additionally, techniques to increase the grain size will also need to be conducted for PVD MoS$_2$.
A majority of the future work will look into better controlling the stoichiometric ratio for the TMD films to improve switching performance. Current methods are now known to anneal the films and increase the Sulfur ratio after deposition occurs by processing the materials in a sulfur rich environment. New methods to control the stoichiometric ratio while depositing are highly desirable even more so than an annealing procedure and are currently under review for generating a new path forward for 2D PVD devices.

Other than being able to control the Sulfur ratio, the ability to generate lithography deposited contacts with sub-micron channel lengths is of high importance to have the contacts along a single crystalline domain. For lithography to be possible, a new contact deposition method will need to be created and the TEM mesh contacts will need to be avoided.

Environmental sensitivity is a major factor in 2D materials. Once again, the surface to volume ratio is extremely high and the environmental influence will need to be mitigated to make useful applications from 2D materials or the devices will always become insulating from the oxidation reaction. Lastly, 2D materials also have potential for electronic sensing applications. The sensing properties arise from the ability to functionalize the MoS$_2$, and upon being functionalized, the surface to volume ratio allows drastic changes in electrical properties from miniscule surface potential changes brought by adsorbed molecules.
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