AN AREA EFFICIENT 10-BIT TIME MODE HYBRID DIGITAL-TO- ANALOG CONVERTER WITH CURRENT SETTLING ERROR COMPENSATION

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AN AREA EFFICIENT 10-BIT TIME MODE HYBRID DIGITAL-TO-ANALOG CONVERTER WITH CURRENT SETTLING ERROR COMPENSATION

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ABSTRACT

This work describes an area efficient 10-bit time mode hybrid DAC with current settling error compensation. The proposed 10-bit hybrid DAC is realized using a current steering DAC for the lower bits conversion and a time mode DAC for the upper bits conversion. The time mode DAC consist of a single capacitor, amplifier, current mirror and several control switches which occupies less area than other DAC architectures. The time mode DAC current settling error occurs because of the capacitor current not immediately responding to the control pulse, which further decreases the DAC output voltage. A compensation pulse corresponding to the DAC error voltage is generated and is added to the control pulse to compensate the DAC output voltage error caused by improper current settling. In addition, the time mode DAC current settling error compensation does not critically increase the area. The proposed DAC is realized using 0.35µm CMOS technology with estimated core area of 0.00463mm², which is less than most of the existing 10-bit DACs published in the literature. The maximum DNL and INL with error compensation showed 0.5LSB and -0.6LSB, respectively.
DEDICATION

I would like to dedicate this thesis to my family and friends. This thesis would not have been possible without their support, encouragement and love.
ACKNOWLEDGEMENTS

I would like to acknowledge my thesis advisory committee, Dr. Kye-Shin Lee, Dr. S.I Hariharan and Dr. Yilmaz Sozer, for their technical input and support throughout the conception, realization and culmination of this thesis project.

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CHAPTER I
INTRODUCTION

1.1. Motivation

With the rapid progress in digital multimedia technologies, there is an increasing demand for high quality displays such as the ultra-high definition (UHD) and the 3D TVs. In order to realize high quality displays with larger screen size, liquid crystal display (LCD) drivers require higher resolution and data depth which is challenging for low cost designs. For LCD driver modules, the column driver is the most critical component that determines the cost and quality of the overall display driver system [1], [2].

A typical column driver includes shift registers, data latches, level shifters, digital-to-analog converters (DACs), and output buffers. Among these components, the DAC occupies the largest area, since hundreds of channels should be built into the driver module. Therefore, it is highly preferred to reduce the area of the DAC in order to reduce the cost whereas maintaining the display quality of LCD drivers. So far, the resistor string DAC has been widely used for LCD drivers, due to stringent requirement on uniformity but generally they result in larger area and low speed. The increase in color depth for LCD further discloses the limitation of the RDAC. Although other area efficient DAC
architectures including the cyclic and the segmented DACs are proposed, the conversion speed and the performance significantly degrades as the resolution of the DAC increases [3] – [5].

In this thesis, an area efficient 10-bit time mode hybrid DAC is proposed, where the area is significantly reduced by combining a 5-bit time mode DAC for upper bit conversion with a 5-bit current steering DAC for lower bit conversion. The time mode DAC consist of a single capacitor, amplifier, current mirror and several control switches which occupies less area than other DAC architectures.

The current mode DAC is realized using the cascode current mirrors for better current matching. The current mode DAC uses MOS transistors and only one resistor which does not occupy large area. Furthermore, a current settling error compensation scheme for the time mode DAC is included without significantly increasing the overall DAC area. Therefore the proposed DAC combining the lower and upper bit voltages to generate the final DAC output voltage significantly minimizes the routing area. This area efficient DAC will have its application in liquid crystal display drivers and multichannel readout electronics systems designed for high energy physics experiments like ILC (International Linear Collider). Often a large number of precise DACs is required to be used in a single ASIC to control various parameters. For this reason a general purpose moderate resolution low power small area DAC is one of the key components in such systems [8].
1.2. Goal of thesis

The goal of this thesis is to design an area efficient 10 bit time mode hybrid DAC which will occupy minimum area compared to most of the existing DACs. Various DAC circuits were investigated and the time mode hybrid DAC architecture is selected, since this enables the least area among other DACs.

The circuit level DAC is realized and the operation is verified through circuit level simulations. In order to evaluate the DAC performance INL and DNL plots were obtained. Further an additional compensation technique to compensate the current settling error is adopted. The proposed compensation technique used does not critically impact the area of time mode hybrid DAC. The proposed 10-bit DAC with current settling error compensation scheme was realized in 0.35µm CMOS technology. The estimated core area of the DAC is around 0.00463mm$^2$ which is small compared to most of the other DACs. The maximum INL and DNL of 10-bit DAC with error compensation is -0.6LSB and 0.5LSB, respectively. The conversion speed is 3.4 MS/s with the power consumption of 50µW.

1.3. Organization of this thesis

The remaining part of the thesis is divided into four chapters.

Chapter II presents the overview of LCD drivers and various DAC architectures used for LCD driver applications. The various DAC architecture area and performance are compared using a table.
Chapter III describes the architecture of the proposed hybrid DAC and operation timing of the hybrid DAC.

Chapter IV addresses the current settling error and the error compensation technique implemented in the 10 bit DAC.

Chapter V shows the simulation results of INL and DNL plots before and after the compensation, presents the estimated core area of the proposed DAC and also includes the performance comparison table.

Chapter VI presents the conclusion and future work.
CHAPTER II
LITERATURE REVIEW

This chapter describes the overview of LCD drivers, and DAC architectures generally used for LCD drivers - RDAC, RRDAC, a small area 10-bit linear gamma DAC with voltage adder, resistor - capacitor hybrid DAC (RCDAC), a piecewise linear 10-bit DAC architecture with drain current modulation. In addition, the various DAC architectures area and performance are compared.

2.1. Overview of LCD driver

With a rapid evolution of liquid crystal display (LCD) television (TV), there is a large demand for developing high resolution, high color depth driver IC [1]-[3]. The block diagram of LCD column driver is shown in Figure 2.1. An LCD driver generally consist of column driver, row drivers, a timing controller, and a reference source. The column drivers are especially critical for achieving a high quality display.

A column drivers generally includes shift registers, data latches, level shifters, DACs and output buffers, where the DAC occupies the most area and consumes the most power. Since hundreds of channels are build into a single chip, it is desirable to reduce the area of the DAC, especially for color depth displays [8].
In LCD applications, for high resolution the column driver requires a 10-bit DAC. Therefore an area efficient 10-bit DAC is necessary.

![Block diagram of LCD driver](image)

Figure 2.1 Block diagram of LCD driver

2.2. Basic concept of DAC

There are several DAC architectures, the suitability of a DAC for a particular application is determined by six main parameters physical size, power consumption, resolution, speed, accuracy and cost.

Integral non linearity (INL) and differential nonlinearity (DNL) measurements are generally performed on Digital to Analog converters to verify their performance.
characteristics. Together with gain and offset errors, INL and DNL measurements define the device static error specifications.

DNL error is defined as the difference between an actual step width and the ideal value of 1LSB as shown in Figure 2.2. For an ideal ADC, in which the differential nonlinearity coincides with DNL=0LSB, each analog step equals 1LSB \(1\text{LSB} = \frac{V_{\text{FSR}}}{2^{N}}\), where \(V_{\text{FSR}}\) is the full-scale range and \(N\) is the resolution of the ADC and the transition values are spaced exactly 1LSB apart [11]. A DNL error specification of less than or equal to 1LSB guarantees a monotonic transfer function with no missing codes. An ADC's monotonicity is guaranteed when its digital output increases (or remains constant) with an increasing input signal, thereby avoiding sign changes in the slope of the transfer curve. DNL is specified after the static gain error has been removed. It is defined as follows:

\[
\text{DNL} = \left| \frac{V_{D+1} - V_{D}}{V_{\text{LSB-Ideal}}} - 1 \right|, \text{ where } 0 < D < 2^{N} - 2.\quad (2.1)
\]

\(V_{D}\) is the physical value corresponding to the digital output code \(D\), \(N\) is the ADC resolution, and \(V_{\text{LSB-Ideal}}\) is the ideal spacing for two adjacent digital codes. By adding noise and spurious components beyond the effects of quantization, higher values of DNL usually limit the ADC's performance in terms of signal-to-noise ratio (SNR) and spurious-free dynamic range (SFDR).
INL error is described as the deviation, in LSB or percent of full-scale range (FSR), of an actual transfer function from a straight line. The INL-error magnitude then depends directly on the position chosen for this straight line. At least two definitions are common: "best straight-line INL" and "end-point INL" as shown in Figure 2.3.

2.2.1. Best straight-line INL

It provides information about offset (intercept) and gain (slope) error, plus the position of the transfer function (discussed below). It determines, in the form of a straight line, the closest approximation to the ADC's actual transfer function [11]. The exact position of the line is not clearly defined, but this approach yields the best repeatability, and it serves as a true representation of linearity.
2.2.2. End-point INL

End point INL passes the straight line through end points of the converter's transfer function, thereby defining a precise position for the line [11]. Thus, the straight line for an N-bit ADC is defined by its zero (all zeros) and its full-scale (all ones) outputs. The best straight-line approach is generally preferred, because it produces better results.

The INL specification is measured after both static offset and gain errors have been nullified, and can be described as follows:

\[
\text{INL} = | \frac{(V_D - V_{ZERO})}{V_{LSB-Ideal}} - D |, \quad 0 < D < 2^{N-1}. \quad [11] \tag{2.2}
\]

\(V_D\) is the analog value represented by the digital output code \(D\), \(N\) is the ADC's resolution, \(V_{ZERO}\) is the minimum analog input corresponding to an all-zero output code, and \(V_{LSB-Ideal}\) is the ideal spacing for two adjacent output codes.

Figure 2.3  INL measurement for digital to analog converter [11]
2.3. Resistor string DAC (RDAC) and Resistor-resistor string DAC (RRDAC)

The general block diagram of resistor string DAC (RDAC) is shown in Figure 2.4. The RDAC consist of resistor string reference voltage generator, N-bit decoder and a unity gain buffer. An N-bit resistor string DAC uses $2^N$ resistors. The switches connecting the resistor to N-bit decoder is controlled by the DACs digital input, which selects the appropriate reference voltage for the output. This is given to the unity gain buffer to generate the final DAC output voltage. To achieve high color depth for LCD drivers requires a high DAC resolution and a large circuit die area. The resistor string DAC has been widely used for LCD drivers, due to stringent requirement on uniformity but generally they result in larger area and low speed for higher resolution. Hence the RDAC are generally used for low resolution (6b<) and small size panels.
Generally the resistor-resistor string DAC (RRDAC) consist of two resistor string DACs, and two intermediate unity gain buffers which reduces the chip area. The intermediate buffers isolate the two RDACs. There will be an offset errors associated with the buffers which is further spread to the LCD driver output. As a result, obtaining output uniformity for high color depth column driver is rather difficult [9]. Each output channel demands two additional buffers which further increases the power consumption. To reduce the area, researchers have used RRDAC without unity gain buffers [9]. Figure 2.5 shows the block diagram of RRDAC without the unity gain buffers which is realized with $2^6+2^4$ resistors but with complicate decoding logic. To obtain this, the parallel channel resistor strings are directly connected to the global resistor string, this in fact affects the reference voltage of the global resistor string.

Based on the digital input bits given to the 6-bit decoder, the corresponding voltage range that is upper bound range ($V_{H}$), and the lower bound range ($V_{L}$) is selected and given as the input to the 4-bit decoder which further selects the appropriate voltage corresponding to the 4 lower input digital bits.

![Figure 2.5 Block diagram of RRDAC](image)
2.4. A small area 10-bit linear gamma DAC with voltage adder

The active matrix flat panel displays (AMFPDs) have been mainly used for most display applications. In particular the liquid crystal display has dominated most display (LCD) markets of electronic products. In order to realize the AMFPDs, it is required for the source driver to convert the input digital code to the analog output voltage and transfer this voltage to the panel[2]. However the chip area of the source driver IC is increasing because of large size and high resolution AMFPDs requires many column drivers and high resolution DACs [7]. Therefore, an area efficient and high resolution DAC is necessary.

One of the area efficient 10-bit DAC architecture is splitting the upper DAC into two 7-bit RDACs, which is used for selecting two adjacent voltages $V_H$ (upper voltage) and $V_L$ (lower voltage) and lower 3-bit DAC with unity gain buffer. The Figure 2.6 shows the conventional DAC with 128 resistors($2^7$) forming 7-bit upper data resistor string DAC. Generally in a resistor string reference voltage generator, $2^N$ resistors and switches are required for N-bit DAC. Both the 7-bit upper data DAC has the same digital input but slightly different reference voltage.

Based on the digital input bits the resistors are switched which in turn used for selecting two adjacent voltages $V_H$ and $V_L$. The unity gain buffer divides the voltage range between $V_H$ and $V_L$ into eight voltage levels according to the 3-bit lower inputs. The 3-bit DAC generates the DAC output voltage by combining the 7-bit upper voltage levels $V_H$ and $V_L$, depending on the lower 3-bit input data. Table 2.1 shows the DAC
output voltage as a function of 3-bit lower input data. Thus this conventional DAC can be used to achieve 10-bit DAC using two 7-bit upper data.

Table 2.1 DAC output voltage as function of 3-bit lower input data

<table>
<thead>
<tr>
<th>b₂</th>
<th>b₁</th>
<th>b₀</th>
<th>V_{out}</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>V_L</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>(V_H+V_L)/8</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>V_L/4</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>(V_H+V_L)/8</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>V_H/2</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>5/4[(V_H+V_L)²]</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>3/8V_H</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>7/36[(V_H+V_L)²]</td>
</tr>
</tbody>
</table>

Figure 2.6 Structure of conventional 10 bit DAC [7]
The architecture of small area 10-bit linear gamma correction DAC with voltage adder is shown in Figure 2.7, where one of the upper 7 bit DAC that selects $V_H$ from the output voltage of the resistor string is replaced with the voltage adder. The architecture mainly consist of one upper 7 bit DAC, voltage adder, and lower 3-bit DAC with unity gain buffer.

The voltage adder is a general switched capacitor adder, which includes one OPAMP, two capacitors, and six switches. The upper 7 bit DAC selects $V_L$ from the output voltage of the resistor strings according to input data. The voltage adder generates $V_H$ by adding $V_L$ and the difference between two adjacent voltages of resistor string. The unity gain buffer divides the voltage range between $V_H$ and $V_L$ into eight voltage levels according to the lower 3-bit input data. As a result, the output of the proposed 10 bit DAC becomes equivalent to that of a conventional 10-bit DAC using two upper 7-bit DACs.

![Figure 2.7 Structure of 10-bit DAC with voltage adder [7]](image-url)
The area of the upper 7 bit DAC is high compared to the voltage adder. Hence the small area 10-bit gamma DAC with voltage adder is realized with smaller area of 0.02871 mm$^2$ compared to the area of 10-bit conventional DAC with 2 upper 7-bit DACs which is 0.0396 mm$^2$. The 10 bit linear gamma DAC with voltage adder is designed in 0.18µm CMOS technology with maximum DAC INL and DNL of 0.98LSB and 0.69 LSB respectively.

In conventional column driver ICs, the resistor string DAC has been generally used due to its uniform characteristic, because each R-DAC in channel shares a common resistor string for gamma reference voltage generation. Furthermore, the nonlinear gamma correction can be easily implemented using a non linear resistor string that has a inverse transverse curve to liquid crystal (LC) response [8]. However, the conversion speed and the performance of the resistor string DAC significantly degrades with the increase in the resolution of the DACs. Even though the 10-bit linear gamma DAC uses only one 7-bit RDAC, the resistor string divides the voltage and generates 256 voltage segments which in turn result in larger area and low speed.

2.5. Resistor-Capacitor hybrid DAC (RCDAC)

The piecewise linear digital to analog converters is used to reduce the die area and to increase the color depth. The data conversion is carried out by a resistor string type DAC (R-DAC) and a charge sharing DAC (C-DAC) which are used for the most significant and least significant bit data converters respectively. The 10-bit DAC contains
a 7-bit R-DAC and 3-bit C-DAC to reduce the die area and data conversion time. The data conversion is implemented by R-DAC and C-DAC. The decoder of the R-DAC is based on the upper input bits that selects the two adjacent voltages \( V_i \) and \( V_{i+1} \), and sends them to the C-DAC. Then the C-DAC uses the two adjacent voltages to do voltage division, and generates the final output voltage.

![Schematic of resistor-capacitor hybrid DAC (RCDAC)](image)

**Figure 2.8 Schematic of resistor-capacitor hybrid DAC (RCDAC)**

Figure 2.8 shows the RCDAC architecture. The voltage division in the C-DAC is based on precharging and charge redistribution [1]. The C-DAC basically consist of three binary weighted capacitors, an additional unit capacitor and a set of switches that connect the capacitor to the input voltage. Two operation phases are required to perform voltage division in this circuit. In the precharge phase (\( \Phi_1=0 \)), the weighted capacitors are connected to \( V_{i+1} \) or \( V_i \) depending on 3-bit lower inputs (\( b_2~b_0 \)). In the evaluation phase (\( \Phi_1=1 \)), all the capacitors are disconnected from the input and connected to the output
The charge redistribution occurs, and finally the reconstructed analog value appears at the output. The output voltage can be given as:

\[
V_{\text{out}} = \frac{4b_2 + 2b_1 + b_0}{8} (V_{i+1} - V_i) + V_i
\]  

(2.3)

The experimental results of this DAC shows that the settling time is within 3 µs with average die area of 0.063 mm². The measured maximum DNL and INL are 3.83 and 3.84 LSB respectively. The area of this 10-bit LCD column driver with piecewise linear digital to analog converters is smaller than that of full R-DAC based column drivers.

2.6. A piecewise linear 10-bit DAC architecture with drain current modulation

The conceptual diagram of the operation of drain current modulation is shown in Figure 2.9. The upper DAC with N-M (N=9, M=3) resolution is implemented with an R-DAC that produces two neighbor voltages upper bound voltage (V_{Hi}) and lower bound voltage (V_{Lo}). The lower DAC with M bit resolution is implemented using the drain current modulation that uses these two voltages. The V-I converter converts the voltage difference (V_{Hi} - V_{Lo}) to a current ΔI.

The current flows through the valve which controls the current with M-bit resolution. Then the current is further injected into the interpolation block which is again converted to voltage and added to the V_{Lo} to generate the final DAC output V_{OUT}. The interpolation block has a unity gain buffer with negative feedback where the V_{OUT} follows the V_{Lo} when no current is injected into the interpolation block. When there is a
current injection, $V_{\text{OUT}}$ will be sum of $V_{\text{LO}}$ and the voltage converted from the injected current.

![Conceptual Diagram](image.png)

Figure 2.9 Conceptual diagram for the operation of current modulation [4]

Figure 2.10 shows the circuit diagram of drain current modulation DAC. The overall 10-bit DAC is realized with 6-bit R-DAC and 4-bit sub-DAC with interpolation scheme. It is assumed that the input differential pairs are identically designed and negative feedback is present in the interpolation block. The amount of current flowing through the interpolation block is controlled by the 4-bit current DAC. The DAC output current $I_{\text{DAC}}$ is transformed to certain amount of voltage in the interpolation block. The output voltage $V_{\text{OUT}}$ is given as
$V_{OUT} = V_{LO} + \frac{I_{DAC}}{g_{m1}}.$

(2.4)

Figure 2.10 Interpolating scheme with drain current modulation [4]

A piecewise linear 10-bit DAC architecture with drain current modulation was realized in 0.1 µm technology with maximum DNL and INL to be 0.37 LSB and 1.71 LSB. The 10-bit R-DAC with the interpolation scheme occupies an area of 0.0046mm$^2$. Although the area of piecewise linear DAC architecture with drain current modulation has comparatively less area, this is realized using a scaled semiconductor technology (0.1µm).
2.7. Performance comparison

The below Table 2.2 shows the performance comparison of various DAC architecture used in LCD driver applications. Among the various DAC architecture the RRDAC occupies the largest area and the drain-current modulation DAC occupies less area.

<table>
<thead>
<tr>
<th>DAC Architecture</th>
<th>Technology</th>
<th>Resolution</th>
<th>Area</th>
</tr>
</thead>
<tbody>
<tr>
<td>RRDAC</td>
<td>0.35 µm</td>
<td>10-bit</td>
<td>0.069 mm²</td>
</tr>
<tr>
<td>Linear gamma DAC</td>
<td>0.18 µm</td>
<td>10-bit</td>
<td>0.028 mm²</td>
</tr>
<tr>
<td>C+R DAC</td>
<td>0.35 µm</td>
<td>10-bit</td>
<td>0.063 mm²</td>
</tr>
<tr>
<td>Drain-Current Modulation DAC</td>
<td>0.1 µm</td>
<td>10-bit</td>
<td>0.004 mm²</td>
</tr>
</tbody>
</table>
CHAPTER III

PROPOSED DAC

Figure 3.1 shows the proposed 10-bit hybrid DAC which consists of the 5-bit time-mode DAC (converts the upper bits \(b_9\) to \(b_5\)) and the 5-bit current steering DAC (converts the lower bits \(b_4\) to \(b_0\)). The final DAC output voltage is generated by combining the upper and lower bit conversion results.

Figure 3.1 Proposed DAC architecture
The time mode DAC includes the reference current source $I_{REF}$, simple current mirror $M_1$ and $M_2$, feedback amplifier, capacitor $C$, and several control switches. Figure 3.2 shows the simplified circuit of the time mode DAC, where $I_C$ connected to the inverting input of the amplifier represents the current mirror by $M_1$ and $M_2$ through the control switch $S_1$. Assuming the inverting input of the feedback amplifier is a fixed voltage, if $S_1$ is on, the current $I_C$ which is equal to $I_{REF}$ will discharge $C$, and increase the output amplifier voltage, whereas if $S_1$ is off, the amplifier output level will remain constant. Based on this principle, the output voltage of the time mode DAC is determined by the width of the switch $S_1$ control pulse $T_{CTRL}$. That is

$$V_{out} = I_C \cdot \frac{T_{CTRL}}{C} + V_{CM}. \quad (3.1)$$

since $I_C$ and $C$ are constant, the capacitor charge is proportional to the pulse width $T_{CTRL}$. As a result, the DAC output voltage corresponding to the upper bits $b_9$ to $b_5$ is generated
by sequentially applying the control pulses with binary weighted pulse widths to switch $S_1$. The pulse width corresponding to each DAC upper input bit $b_i$, $i=5$ to 9 can be written as

$$T_{i-4} = 2^{i-5} \cdot T$$

(3.2)

where $T$ is the unit pulse width. Therefore, in order to make a DAC, the bits of the input code are processed one by one in a sequence. When there is a binary bit 1 as the first input, the capacitor is charged with a control pulse whose pulse width is proportional to the weight of the input binary bit and when the input is 0, the control pulse remains low and no charge is added to the capacitor. Then the next bit is applied. If it is 1, another control pulse is applied to $S_1$ whose pulse width is proportional to the weight of second bit in the input binary code. Therefore the capacitor charge is the summation of the charge corresponding to all the 5 MSB bits which each of them are either zero or certain voltage which is proportional to corresponding bit weight in the input binary code. Furthermore, the DAC output voltage for the upper bits $b_0$ to $b_5$ is given as

$$V_{up} = \frac{I_c \cdot T}{C} \left[ \sum_{i=5}^{9} 2^{(i-5)} \cdot b_i \right] + V_{CM}$$

(3.3)

where $b_i$ is 1 for High and 0 for Low input level. Each time when $b_i$ is 1, a voltage proportional to the weight of input bit is added to voltage stored in the capacitor and if the $b_i$ is 0, the capacitor voltage does not change. When the last bit is processed, the
capacitor voltage is the analog equivalent of the input binary code. Since \( b_5 \) is the 6\(^{th} \) bit of the 10-bit DAC, it corresponds to analog output level of \( 32V_{\text{LSB}} \), where \( V_{\text{LSB}} \) is the LSB voltage of the DAC. Therefore, the unit pulse width \( T \) is given as

\[
T = \frac{32 \cdot V_{\text{LSB}} \cdot C}{I_c}.
\]  

(3.4)

the values of \( C \) and \( I_c \) are selected in a way that the obtained value for \( T \) is convenient to implement. The value of \( V_{\text{CM}} \) is calculated based on the proper operation of the operational amplifier and current mirror. Maintaining the drain voltage of the current mirror transistor \( M_2 \) at the constant voltage \( V_{\text{CM}} \) minimizes the channel length modulation effect. Furthermore, the parasitic at the inverting input of the amplifier is always charged to \( V_{\text{CM}} \), which prevents charge sharing errors caused by large parasitic at this node [6]. Since the drain terminal of \( M_2 \) is fixed to \( V_{\text{CM}} \), there is no need of using a high output resistance current mirror (a simple current mirror will work). An additional switch \( S_2 \) is used to turn the current mirror off quickly, which will minimize transient current errors.

The 5-bit current mode DAC is realized using cascode current mirrors to improve the current matching. As shown in Figure 3.1, cascode current mirrors generate the binary weighted currents which are added together and flow through resistor to generate 5LSBs analog voltage. Bits \( b_4 \) to \( b_0 \) control the switches \( S_5 \) to \( S_0 \). The basic idea of the current mode DAC is to switch the current sources to the output, depending on the value of the digital input bits \( (b_{N-1} \sim b_0) \) [10]. The reference current \( I_{\text{REF}} \) is mirrored to current
sources and the output voltage $V_{\text{Low}}$ is being generated. The DAC output voltage for the lower bits conversion is given as

$$V_{\text{Low}} = I_{\text{REF}} \cdot R \left[ \sum_{i=0}^{4} \frac{b_i}{2^{3-i}} \right]$$  \hspace{1cm} (3.5)

where the value of resistance $R$ should be scaled to

$$R = \frac{32 \cdot V_{\text{LSB}}}{I_{\text{REF}}}.$$ \hspace{1cm} (3.6)

The final DAC output voltage is given as

$$V_{\text{out}} = V_{\text{up}} + V_{\text{Low}}$$  \hspace{1cm} (3.7)

Where $V_{\text{up}}$ is the analog voltage corresponding to 5 MSBs of input code and $V_{\text{Low}}$ is the analog voltage corresponding to 5 LSBs of input code combined and stored in the capacitor.

In the proposed 10-bit DAC, the time mode DAC is responsible for converting 5 most significant bits ($b_9$-$b_5$). The conversion sequence of MSB bits $b_9$, $b_8$, $b_7$, $b_6$, $b_5$ to its equivalent analog voltage is as follows. The input bits $b_9$ to $b_5$ are set in D-flip flops and are available at the one of the input of AND gates of Figure 3.3. The sequence of control pulses $T_1$ to $T_5$ which correspond to $b_9$ to $b_5$ are applied to the other input of the AND gate where all the outputs of AND gate are added using OR gate and control pulse $T_{\text{CTRL}}$
is generated. This $T_{CTRL}$ pulse is given as the input to the switch $S_1$. The conversion starts from $b_9$ and if $b_9=1$, $T_5$ is transferred to $T_{CTRL}$ through AND1 and OR gate (Figure 3.3) and the capacitor is charged with $I_C$ to voltage $(I_C*16T)/C$. However if $b_9=0$, the $T_{CTRL}$ remains low and capacitor is not charged. The capacitor stores this charge until the next bit conversion. When $T_5$ goes low, $T_4$ goes high which corresponds to $b_8$ and if $b_8=1$, the voltage $(I_C*8T)/C$ is added to previous charge of the capacitor and if $b_8=0$, no voltage is added to the previous capacitor voltage. Similarly this process is repeated for all $T_3$ to $T_1$ pulses and their corresponding bits $b_7$ to $b_5$.

![Figure 3.3 Logic for $T_{CTRL}$ generation](image)

The operation timing of the proposed DAC is shown in Figure 3.4, where the conversion starts with a RESET signal that discharges $C$, in order to erase the voltage from previous conversion result, followed by the upper bits and lower bits conversion. For the upper bits conversion, a sequence of control pulses $T_1$ to $T_5$ corresponding to the weight of each bit $b_5$ to $b_9$ are applied to $S_1$. Once the time mode DAC finishes conversion, the analog
voltage corresponding to 5 MSBs is stored in the capacitor, MSBC becomes Low and opens the switch $S_3$ to disconnect the time mode DAC from the Opamp. Then LSBC becomes High which activates the current mode DAC that generates the analog voltage corresponding to 5 LSBs and give it to the non-inverting input of Opamp through the switch $S_4$. The DAC output corresponding to the upper and lower bits are combined in capacitor $C$ to generate the final DAC output. Therefore the final Opamp result is the summation of LSB voltage and MSB voltage. The LSBC signal is long enough to let the voltage of current mode DAC settle at its final value. Furthermore to reduce the power consumption, when MSBs are converted, the current mode DAC is not active and all the switches $S_5$ to $S_9$ are open.

![Figure 3.4 Operation timing of the hybrid DAC](image)

Figure 3.4 Operation timing of the hybrid DAC
The proposed area efficient 10-bit hybrid time mode DAC can be realized with small area, since the time mode DAC only requires a single capacitor, current mirror, amplifier and several switches, whereas the 5-bit current DAC using only MOS transistors and one resistor which does not occupy large area. Furthermore the proposed DAC combining the lower and upper bit voltages to generate the final DAC output significantly reduces the routing area.
CHAPTER IV
ERROR COMPENSATION

4.1. Current settling error

The improper current settling is a critical error source for time mode circuits. Noticing the capacitor current \( I_C \) is determined by node voltage \( V_X \), if \( V_X \) does not immediately respond to the control pulse \( T_{CTRL} \), an error will be induced at the output of the time mode DAC. This delay in the capacitor current to reach its steady state degrades the output voltage of the DAC. This decrease in the current during the initial time decreases the output voltage which further affects the INL and DNL. This current settling error can be due to the switch \( S_1 \) on resistance \( R_{on1} \) and the gate to source capacitance of \( M_2 \), \( C_{gs2} \) which cause a delay for \( V_X \) to reach its steady state value, once \( S_1 \) is on. Figure 4.1 is the equivalent circuit model of the proposed time mode DAC current mirror \( M_1 \) and \( M_2 \) when \( S_1 \) is on, where the initial voltage across the capacitor \( C_{gs2} \) is assumed as 0. In addition, \( V_{gs1} \) represents the steady state gate to source voltage of \( M_1 \). The output current which is being passed through the capacitor depending on the digital input bits reaches steady state after the \( V_X \) reaches steady state. Figure 4.2 shows the behavior of \( V_X \) with respect to switch control pulse \( T_{CTRL} \) where \( V_X \) and \( I_C \) almost reach their steady state values after the time delay \( T_X \).
Figure 4.1 Equivalent circuit model of the time mode DAC current mirror

Figure 4.2 Settling behavior of $V_X$ and $I_C$ with respect to $T_{CTRL}$

Where $V_X(T_X)$ is steady state voltage of node voltage $V_X(t)$ and $I_C(T_X)$ is the steady state value of capacitor current of $I_C(t)$ in Figure 4.2. Both the node voltage and capacitor current reaches its steady state after a delay of $T_X$. Since this is a first order RC network, the node voltage $V_X$ can be written as
\[ V_x = V_{gs1} \left( 1 - e^{-\frac{-t}{R_{on1}C_{gs2}}} \right) \] (4.1)

Where \( V_{gs1} = V_X(T_X) \).

Generally, the node voltage \( V_X \) will reach the steady state value within \( 3\tau \), where \( \tau = R_{on1}C_{gs2} \). The output voltage of the time mode DAC is determined by the control pulse width \( T_{CTRL} \), \( I_C \) and \( C \). When \( V_X \) immediately responds to \( T_{CTRL} \), the DAC output voltage is given as \( (I_c(T_X) \cdot T_X)/C \). However, improper settling of \( V_X \) will cause a current settling error for \( I_C \), which will add an error voltage to the DAC output. Assuming the capacitor current \( I_C \) follows \( V_X \) the error voltage can be written as,

\[ V_{error} = \frac{I_c(T_X) \cdot T_X}{C} - \int_0^{T_X} \frac{I_c(t) \cdot dt}{C} \] (4.2)

where \( I_c(T_X) \) is the steady state capacitor current.

The capacitor current \( I_C(t) \) can be written as,

\[ I_c(t) = I_c(T_X) \cdot \left( 1 - e^{-\frac{-t}{\tau}} \right) \] (4.3)

On substituting equation (4.3) in equation (4.2) the error voltage is given as

\[ V_{error} = \frac{I_c(T_X) \cdot T_X}{C} - \frac{I_c(T_X)}{C} \int_0^{T_X} \left( 1 - e^{-\frac{-t}{\tau}} \right) dt \] (4.4)
where the first term is the ideal DAC output voltage and the second term is the actual output voltage due to improper settling of $V_X$. Integrating the second term from 0 to $T_X$ will lead to the final expression for the error voltage as

$$V_{error} = \frac{I_c(T_X)}{C}(-\tau e^{-3\tau} + \tau)$$  \hspace{1cm} (4.5)

4.2. Compensation scheme

In order to overcome the time mode DAC current settling error, a compensation technique is adopted. Due to the improper settling of $V_X$, that reaches the steady state after a delay of $T_X$, the DAC output voltage will be always less than the ideal voltage. As a result, the control pulse width of $T_{CTRL}$ (which is applied to switch $S_1$ shown in Figure 4.3) has to be extended to compensate the error. The proposed compensation scheme is generating an extended control pulse width that can compensate the DAC output voltage reduction due to improper $V_X$ settling, and adding it to the control pulse $T_{CTRL}$. In order to estimate the duration of the compensation pulse width $T_{comp}$, the error voltage can be rewritten as

$$V_{error} = \frac{I_c(T_X)T_{comp}}{C}$$  \hspace{1cm} (4.6)
Figure 4.3 Time mode DAC circuit

Figure 4.4 Compensation circuit
Furthermore, assuming $e^{-3} \approx 0$ and combining the above eq.(4.5) with eq.(4.6), the compensation pulse width can be obtained as

$$T_{\text{comp}} = \tau = \frac{T_X}{3}$$

(4.7)

where the compensation pulse width is equal to $\tau$ which is $1/3$ of $T_X$.

Figure 4.4 shows the proposed compensation circuit which includes an additional current mirror and a comparator. The basic concept of the proposed calibration technique is to extend the pulse width of $T_{\text{CTRL}}$ by $T_{\text{comp}}$ to compensate the improper settling of $V_X$ and $I_C$. A duplicate of the original time mode DAC current mirror block is designed where $T_{\text{CTRL}}$ pulse is given to switch $S_{11}$ and $T_{\text{CTRLB}}$ is applied to the switch $S_{10}$. According to eq. (4.7), in order to build an RC network with time constant of $\tau$, the $C_{gs}$ of transistor $M_4$ is reduced by $1/3$ of the original current mirror $M_2$. This can be achieved by decreasing the width $W$ of $M_4$ to $W/3$ such that time constant is $1/3$ of the
original circuit. The threshold voltage $V_{TH}$ is identical to the steady state voltage $V_X$ of the original current mirror $M_1$ and $M_2$.

The node voltage $V_X'$ is given to the negative input of the comparator and $V_{TH}$ is given to the positive input of the comparator. When $T_{CTRL}$ becomes High $V_X'$ will be 0, and starts reaching steady state when $T_{CTRLB}$ is being applied. The output of the comparator will be High when $T_{CTRL}$ pulse is High and remains High until $V_X'$ reaches the threshold level $V_{TH}$. The output of the comparator adds the compensation pulse $T_{comp}$ to the control pulse $T_{CTRL}$. The operation concept of the proposed compensation scheme is shown in Figure 4.5. Therefore the performance degradation due to error in the output current reaching the steady state is calibrated by adding the compensation pulse $T_{comp}$ corresponding to the error to the control pulse $T_{CTRL}$. Furthermore proposed compensation circuit includes an additional current mirror and a comparator which does not critically increase the area of the DAC.
CHAPTER V
SIMULATION RESULT

The operation of the transistor level 10-bit DAC was verified through circuit level simulations with \( C = 1.25\text{pF} \), \( I_{\text{REF}} = 5\text{µA} \), and current mode DAC resistor \( R = 6.25\text{kΩ} \). A folded-cascode amplifier circuit can be used to reduce the area and a 2 stage amplifier with high slew rate can be used for the comparator. The conversion speed of the proposed DAC is 3.4 MS/s with the time mode DAC unit pulse width \( T \) of 8ns and power consumption of 50µW. The INL and DNL plots of the DAC before and after the compensation is shown in Figure 5.1 and Figure 5.2, respectively. Without the compensation, both the DNL and INL of the proposed DAC are degraded – maximum INL and DNL of -5LSB and 4.5LSB due to the current settling error. This is mainly caused by the delay in the capacitor current \( I_C \) to reach the steady state. The maximum INL and DNL with error compensation shows -0.6LSB and 0.5LSB, respectively. This verifies the effectiveness of the proposed current settling error compensation scheme.
Figure 5.1 DNL and INL plot before error compensation

Figure 5.2 DNL and INL plot after error compensation
5.1. Current mismatch error in current steering DAC

The current mode DAC uses cascode Current mirrors for better current matching. The INL and DNL values for various percentage of current mismatch is obtained by changing the width $W$ of the transistors corresponding to the current steering DAC in Figure 5.3. The $\epsilon_1 I_1$, $\epsilon_2 I_2$, $\epsilon_3 I_3$, $\epsilon_4 I_4$, $\epsilon_5 I_5$ corresponds to the mismatch current. The allowable mismatch that is ±1LSB is obtained when the current mismatch is less than 0.1% as shown in Figure 5.4.

![Figure 5.3 Current steering DAC architecture](image-url)
Table 5.1 shows the estimated area of the proposed DAC, where the capacitor C, current steering DAC, and the amplifier occupy the major area. The other components do not critically affect the area. Table 5.2 summarizes the performance comparison of recently published 9 to 10-bit DACs. The results demonstrate that the proposed DAC has smallest area and comparable DNL and INL compared to other DACs. Although the area of Ref [4] is similar to the proposed DAC, this is realized using a scaled semiconductor technology (0.1µm).
Table 5.1 Estimated area of the proposed DAC

<table>
<thead>
<tr>
<th>Circuit Blocks</th>
<th>Area [mm$^2$]</th>
<th>Percentage [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Capacitor</td>
<td>$36 \times 10^{-4}$</td>
<td>77.62</td>
</tr>
<tr>
<td>Amplifier</td>
<td>$4.225 \times 10^{-4}$</td>
<td>9.11</td>
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<tr>
<td>Comparator</td>
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<td>0.21</td>
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<td>Current mirrors</td>
<td>$0.142 \times 10^{-4}$</td>
<td>0.30</td>
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<tr>
<td>Switches</td>
<td>$0.028 \times 10^{-4}$</td>
<td>4.48</td>
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<tr>
<td>Digital logic</td>
<td>$0.448 \times 10^{-4}$</td>
<td>0.96</td>
</tr>
<tr>
<td>Current mode DAC</td>
<td>$5.390 \times 10^{-4}$</td>
<td>11.62</td>
</tr>
<tr>
<td>Total</td>
<td>$46.373 \times 10^{-4}$</td>
<td>100</td>
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Table 5.2 Performance comparison with other DACs

<table>
<thead>
<tr>
<th>Architecture</th>
<th>C+RDAC</th>
<th>Resistor string DAC with gamma correction</th>
<th>Multiplexed RDAC with current interpolation gamma correction</th>
<th>Drain current modulation DAC</th>
<th>RDAC+DAC embedded OPAMP with 1.6-bit current mode interpolation cells</th>
<th>Time mode hybrid DAC with current settling error compensation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>0.35µm CMOS</td>
<td>0.5µm CMOS</td>
<td>0.35µm CMOS</td>
<td>0.1µm CMOS</td>
<td>0.35µm CMOS</td>
<td>0.35µm CMOS</td>
</tr>
<tr>
<td>Resolution</td>
<td>10 bit</td>
<td>9 bit</td>
<td>10 bit</td>
<td>10 bit</td>
<td>10 bit</td>
<td>10 bit</td>
</tr>
<tr>
<td>DNL[LSB]</td>
<td>3.83</td>
<td>0.5</td>
<td>1.30</td>
<td>0.37</td>
<td>0.45</td>
<td>-0.6</td>
</tr>
<tr>
<td>INL[LSB]</td>
<td>3.84</td>
<td>1</td>
<td>2.13</td>
<td>1.71</td>
<td>0.93</td>
<td>0.4</td>
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<tr>
<td>Area[mm²]</td>
<td>0.063</td>
<td>0.042</td>
<td>0.052</td>
<td>0.00466</td>
<td>0.016</td>
<td>0.00463</td>
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</table>
CHAPTER VI
CONCLUSION

6.1. Summary

This thesis proposes an area efficient 10-bit time mode hybrid DAC with current settling error compensation. The 10-bit hybrid DAC is composed of current mode DAC for lower 5-bit conversion and time mode DAC for upper 5-bit conversion. The time mode DAC effectively reduces the area by using a single capacitor, amplifier, current mirror and several control switches. The current mode DAC is realized using the cascode current mirrors for better current matching. The current mode DAC uses MOS transistors and only one resistor which does not occupy large area. Furthermore, the performance degradation due to the current settling error is compensated by extending the control pulse width with a compensation circuit that does not significantly increase the area. The proposed 10 bit DAC was realized using 0.35µm technology with estimated core area of 0.00463mm$^2$. The maximum INL and DNL of 10-bit DAC with error compensation is -0.6LSB and 0.5LSB, respectively.
6.2. Future work

In future the performance of the current mode DAC could be improved by adopting some compensation scheme to overcome the error due to current mismatch.

The 10-bit hybrid time mode DAC has to be laid out and sent to the foundry for IC fabrication and can be tested for performance evaluation. This will help to evaluate the performance of the proposed design under an actual process condition.

Finally, to be updated with the technology, the proposed design can be implemented with a more advanced CMOS process.
BIBLIOGRAPHY


