A COMPACT LOW POWER BIO-SIGNAL AMPLIFIER WITH EXTENDED LINEAR OPERATION RANGE

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A COMPACT LOW POWER BIO-SIGNAL AMPLIFIER WITH EXTENDED LINEAR OPERATION RANGE

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ABSTRACT

This work presents a low power, small size bio-signal amplifier with an extended linear operation range. The proposed scheme consists of an open loop rail-to-rail differential amplifier in the first stage and a closed loop amplifier in the second stage that minimizes the gain reduction with output voltage level variation. Furthermore, an additional gain control feature compensates the gain degradation as the amplifier output level moves toward the supply rails. Voltage buffers are used in the first and second stages in a way that enables using smaller sized feedback resistors in the second stage. The amplifier performance is relatively insensitive to feedback resistor mismatch. In addition to providing an extended linear operation range, this approach reduces the area and power which are required for portable medical devices. The proposed amplifier is implemented using CMOS 0.35 μm technology with a supply voltage of 3.3 V. The measurement results show a constant gain of 46 dB with a linear operation range from 0.3 V to 3.08 V. The total harmonic distortion (THD) is 0.04% with power consumption of 18.5 μW and a core area of 0.063 mm².
DEDICATION

I would like to dedicate this thesis to my parents, Md. Fazlul Haque and Chemon Afroz. This thesis would not have been possible without their support, encouragement, and love.
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I would like to acknowledge my thesis advisory committee, Dr. Kye-Shin Lee, Dr. Robert Veillette and Dr. Joan Carletta, for their support throughout the conception, realization and analysis of this thesis project. I want to thank Mr. Joe Davis for his advice during some part of the PCB design. I also like to thank MOSIS for fabricating the IC in TSMC 0.35 \(\mu\)m process. I wish to also express my most sincere gratitude to the Electrical and Computer Engineering Department of the University of Akron for supporting my studies through a research assistantship.
# TABLE OF CONTENTS

<table>
<thead>
<tr>
<th>LIST OF TABLES</th>
<th>viii</th>
</tr>
</thead>
<tbody>
<tr>
<td>LIST OF FIGURES</td>
<td>ix</td>
</tr>
<tr>
<td>CHAPTER</td>
<td></td>
</tr>
<tr>
<td>I.  INTRODUCTION</td>
<td>1</td>
</tr>
<tr>
<td>1.1 Motivation</td>
<td>1</td>
</tr>
<tr>
<td>1.2 Goal of the thesis</td>
<td>4</td>
</tr>
<tr>
<td>1.3 Thesis organization</td>
<td>5</td>
</tr>
<tr>
<td>II. PREVIOUS WORK</td>
<td>6</td>
</tr>
<tr>
<td>2.1 Three op-amp instrumentation amplifier</td>
<td>6</td>
</tr>
<tr>
<td>2.2 Current feedback IA</td>
<td>8</td>
</tr>
<tr>
<td>2.3 Chopper amplifier</td>
<td>11</td>
</tr>
<tr>
<td>III. PROPOSED BIO-SIGNAL AMPLIFIER</td>
<td>14</td>
</tr>
<tr>
<td>3.1 Amplifier architecture</td>
<td>14</td>
</tr>
<tr>
<td>3.2 Operation of the proposed amplifier</td>
<td>15</td>
</tr>
<tr>
<td>3.3 Proposed amplifier circuit description</td>
<td>19</td>
</tr>
<tr>
<td>3.4 Frequency compensation</td>
<td>25</td>
</tr>
</tbody>
</table>
### LIST OF TABLES

<table>
<thead>
<tr>
<th>Table</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.1</td>
<td>13</td>
</tr>
<tr>
<td>3.1</td>
<td>24</td>
</tr>
<tr>
<td>4.1</td>
<td>29</td>
</tr>
<tr>
<td>5.1</td>
<td>50</td>
</tr>
</tbody>
</table>
### LIST OF FIGURES

<table>
<thead>
<tr>
<th>Figure</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.1</td>
<td>Block diagram of a bio-signal sensing system</td>
<td>2</td>
</tr>
<tr>
<td>1.2</td>
<td>Transfer characteristic (a) Wide linear operation range (b) Narrow linear operation range</td>
<td>3</td>
</tr>
<tr>
<td>1.3</td>
<td>Typical op-amp’s gain variation with output voltage [13]</td>
<td>3</td>
</tr>
<tr>
<td>2.1</td>
<td>Structure of a three op-amp IA [24]</td>
<td>7</td>
</tr>
<tr>
<td>2.2</td>
<td>Current feedback IA [20]</td>
<td>8</td>
</tr>
<tr>
<td>2.3</td>
<td>Chopper amplifier [33]</td>
<td>10</td>
</tr>
<tr>
<td>2.4</td>
<td>Chopping principle in frequency and time domain [33]</td>
<td>10</td>
</tr>
<tr>
<td>2.5</td>
<td>Noise power spectrum of chopper amplifier [33]</td>
<td>11</td>
</tr>
<tr>
<td>3.1</td>
<td>Block diagram of the proposed amplifier</td>
<td>16</td>
</tr>
<tr>
<td>3.2</td>
<td>Circuit diagram of the proposed amplifier</td>
<td>17</td>
</tr>
<tr>
<td>3.3</td>
<td>Rail-to-rail voltage buffer</td>
<td>19</td>
</tr>
<tr>
<td>3.4</td>
<td>Resistance of $M_9$ and $M_{10}$ with $V_{out}$</td>
<td>21</td>
</tr>
<tr>
<td>3.5</td>
<td>Second stage gain variation with $V_{out}$</td>
<td>21</td>
</tr>
<tr>
<td>3.6</td>
<td>Calculated overall gain as a function of $A_2$</td>
<td>24</td>
</tr>
</tbody>
</table>
5.18 Amplified ECG signal (usual) ........................................ 47
5.19 Input ECG signal (abnormal) ........................................ 48
5.20 Amplified ECG signal (abnormal) .................................... 48
CHAPTER I

INTRODUCTION

1.1 Motivation

Recently, due to the advancement in integrated circuits and wireless technology, portable wireless body sensors that can periodically monitor a patient’s bio-potentials such as the Electroencephalogram (ECG), Electrocardiogram (EEG), and Electromyogram (EMG) are becoming prevalent [1–7]. Fig. 1.1 shows the example of an ECG acquisition system, which includes the sensor electrodes, bio-signal amplifier, filter, analog to digital converter (ADC) and the signal processing unit. The ECG signal is captured from the human body through the electrodes, amplified, and filtered for further signal processing. The key element of the body sensor system is the bio-signal amplifier which determines the quality of the acquired signal. In order to amplify the weak and noisy bio-potential signals without distortion, bio-signal amplifiers require constant voltage gain and low noise and must consume extremely low power. Furthermore, to eliminate the effect of uneven sensor electrode offset, high common mode rejection ratio (CMRR) and high input impedance are both required.

In addition to the above mentioned requirements, the linear operation range of the amplifier needs to be wide to increase the input range of the ADC. The high
Figure 1.1: Block diagram of a bio-signal sensing system

input range of ADC increases the dynamic range of the sensing system as the noise level is kept constant. The linear operation range of an amplifier is defined as the output voltage range with constant DC gain. Fig. 1.2 shows the transfer characteristics of amplifiers with wide and narrow linear operation ranges. The wide linear operation range increases the output swing of the amplifier. However, the linear operation range of amplifiers are limited by the DC gain variation with output voltage level [8–13]. Moreover, as the transistor sizes continue to scale down and the supply voltage further reduces, this will be one of the major non-ideality that critically affects the performance of the bio-signal amplifiers. DC gain degradation is primarily due to output resistance variation of the transistors with the drain to source voltage change. The gain degradation is shown in Fig. 1.3 for a common source output stage. The linear operation range is more limited for a cascode output stage as the output resistance of four transistors change with output voltage level.
Figure 1.2: Transfer characteristic (a) Wide linear operation range (b) Narrow linear operation range

Figure 1.3: Typical op-amp’s gain variation with output voltage [13]
The bio-signal amplifiers need to suppress DC electrode offset (DEO) generated from skin-electrode interface to improve the performance of the sensing system [14–21]. A conventional technique to remove the DEO is the use of a high pass filter. The cut-off frequency of a high pass filter needs to be very low in order to preserve the fidelity of the signal as the bandwidth of the bio-signals are very low (0.1 Hz - 150 Hz) [21]. However, a low cut-off frequency is obtained with a high input capacitor and a large resistor [22]. Due to process mismatch and inaccuracy of capacitors and resistors, it is difficult to control or predict the high pass cut-off frequency. Another way to remove the offset is to use a $G_mC$ filter. However, the cut-off frequency of $G_mC$ filters may vary as much as ±50% [23]. Even with the above mentioned techniques, the DC offset cannot be completely removed. High DC electrode offset voltage changes the common mode level of the output voltage. Therefore, extending the linear range of bio-signal amplifiers is necessary in order to acquire less distorted bio-signals even with large electrode offset which will move the output level toward the supply rails. However, none of the previous research work focuses on extending the linear operation range of bio-signal amplifiers.

1.2 Goal of the thesis

To overcome the previously mentioned drawbacks of bio-signal amplifiers, we propose a new amplifier architecture to extend the linear operation range. The proposed amplifier consists of two stages, where the first stage is open-loop and the second stage is closed-loop with gain enhancement feature which compensates DC gain degradation.
with output voltage variation. In order to verify our concept, we design, simulate, fabricate and test the proposed amplifier. The amplifier is simulated and the prototype IC is fabricated in CMOS 0.35 \( \mu \text{m} \) process. According to test results, this architecture enables low power and small area while maintaining low noise, high CMRR and high input impedance, which makes it suitable for portable medical devices.

1.3 Thesis organization

In Chapter II, the characteristics of previous ECG amplifiers are described. The proposed amplifier architecture and circuit design are described in Chapter III. The noise, CMRR, and PSRR performance of the proposed amplifier are addressed in Chapter IV. Chapter V shows the experimental results, and the conclusions are given in Chapter VI.
CHAPTER II
PREVIOUS WORK

In this chapter, previously designed bio-signal amplifiers are described based on gain, CMRR, linear operation range, power and area. This chapter concludes with a brief summary of the proposed amplifier and a comparison between other amplifiers.

2.1 Three op-amp instrumentation amplifier

Most of the previous amplifier designs used instrumentation amplifier (IA) for bio-signal sensing system. It is the most critical building block that determines the quality of the entire sensing system. The most common architecture for instrumentation amplifier is the three op-amp IA [7, 25–28]. The circuit diagram of IA is shown in Fig. 2.1. The overall differential voltage gain of the amplifier is given by

\[ A_d \equiv \frac{v_o}{v_{id}} = \frac{R_4}{R_3}(1 + \frac{R_2}{R_1}), \quad v_{id} = v_{i1} - v_{i2} \quad (2.1) \]

Although the architecture is simple, conventional three op-amp IAs are not suitable when low power, small size and high CMRR are simultaneously needed. Small value of the feedback resistors are needed to reduce the overall area of the instrumentation amplifier. As a result, the operational amplifiers \( A_1, A_2 \) and \( A_3 \) in Fig. 2.1) must have low output impedance in order to drive the feedback resistors. The
low output impedance of the amplifier increases the current, as the output resistance of a transistor varies inversely with the drain current. As a result, this amplifier leads to high power dissipation [20]. The CMRR of the three op-amp IA depends on the precise matching of the resistors. Without proper matching of the resistors, a spurious signal appears between the two outputs of the first stage op-amps. This signal is amplified by the difference amplifier in the second stage, which causes error at the output. In addition, the electrode offset generated from skin-electrode interface can create a differential error voltage at the amplifier output. Due to the use of three op-amps, the area of this IA is large and the input referred noise is also high.

Most of the three op-amp IAs use a common source amplifier in the output stage [26]. However, the gain of the amplifier is degraded with output voltage level even if a common source output stage is used, as mentioned in chapter I. As a result, the linear operation range of this amplifier is not wide.

Figure 2.1: Structure of a three op-amp IA [24]
2.2 Current feedback IA

Another topology for implementing IA is the current feedback or current balancing IA [14,29,30]. The current feedback IA is shown in Fig. 2.2. The gain of this amplifier is defined by the ratio of two resistors. There is no need for low output impedance amplifiers as there is no global feedback from output to the input. In Fig. 2.2, a high input impedance is guaranteed by two unity gain buffers. The current in resistor $R_g$ is given by

$$i_g = \frac{1}{R_g} (v_1 - v_2). \quad (2.2)$$

The output voltage is given by

$$v_{out} = R_s i_s + v_{ref}. \quad (2.3)$$

The input and output circuits behave as a transconductance amplifier and a transresistance amplifier, respectively [20]. Current mirrors are used to copy the currents.
from the input branch to the output branch \((i_g = i_1 = i_2 = i_s)\). The output voltage is expressed as

\[ v_{out} = \frac{R_s}{R_g}(v_1 - v_2) + v_{ref} \]  

which is quite similar to that of a conventional instrumentation amplifier.

One of the major advantages of this topology is that the CMRR does not depend on the resistor matching [20]. The CMRR mainly depends on the accuracy of the current copying from the input to the output branch. It is possible to copy the currents more accurately by using current mirrors than by means of resistor matching in three op-amp IA. Due to reduced resistor count, the chip area is also reduced. The area is smaller and the input referred noise is also less compared to three op-amp IA. However, the power dissipation of this IA increases with increased number of parallel current branches used in monolithic instrumentation amplifier [31]. The monolithic amplifier uses matched differential current sources to couple input and output circuits. The linear operation region of this amplifier depends on the output stage architecture. The folded cascode structure used in the output stage [32] degrades the linear operation region of this amplifier severely as there are four transistors in the output stage with less headroom. The input referred noise of this topology is low compared to three op-amp IA due to reduced number of components [20].
Figure 2.3: Chopper amplifier [33]

Figure 2.4: Chopping principle in frequency and time domain [33]
2.3 Chopper amplifier

The most common technique used in the bio-signal sensing system to filter the amplifier offset and flicker noise is chopping [33,34]. The chopper amplifiers modulate the offset and flicker noise to a higher frequency. The block diagram of a general chopping amplifier is shown in Fig. 2.3.

![Diagram of chopper amplifier](image)

Figure 2.5: Noise power spectrum of chopper amplifier [33]

The principle of chopping in frequency and time domain is shown in Fig. 2.4 [33]. The input signal $V_{in}$ is modulated to the chopping frequency ($f_{chop}$), amplified and modulated back to the baseband. The offset voltage $V_{os}$, as well as the flicker noise, is modulated once and appears at the chopping frequency and its odd harmonics. The low pass filter removes the high frequency components at chopping frequency and its odd harmonics. In the time domain, the input signal $V_{in}$ is periodically inverted by the first chopper. After amplification, the inverted signal is inverted again, resulting in a DC signal. The offset is modulated only once by the
second chopper and therefore appears as a square wave at the output. Since the flicker noise is removed, the baseband noise of chopper amplifier is almost equal to the wideband thermal noise, considering the chopping frequency is higher than the flicker noise corner frequency as shown in the noise power spectrum in Fig. 2.5. As a result, the input referred noise of this amplifier is very low. However, the major disadvantages of this topology are high power, increased area due to the addition of switches and filter and complicated control due to synchronization between input and output chopper [35]. The CMRR of chopping amplifiers is not affected by chopping. High CMRR can be obtained as this topology does not require resistors [33].

Similar to the current feedback topology, the linear operation region of the chopper amplifier also depends on the design of the output stage. The folded cascode structure used in the output stage [36] degrades the linear operation region. The common source output stage [33] also degrades the gain with the output voltage.

Table 2.1 gives a comparative summary of the characteristics of different bio-signal amplifier architectures as discussed above. The gain of all three topologies is high, as two or more stages are used in all the amplifiers. In the next chapter, a new amplifier architecture is presented. The proposed amplifier consists of an open-loop first stage and a closed-loop second stage. Two gain control switches are used in the second stage to compensate the gain degradation when the output voltage moves to the rails. The linear operation region of this amplifier is high compared to other architectures. Due to low bias current, the power consumption is also low. The input referred noise is comparatively high due to increased number of components. The
Table 2.1: Characteristics of previous bio-signal amplifiers

<table>
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<tr>
<th>Ref.</th>
<th>Methodology</th>
<th>Gain</th>
<th>CMRR</th>
<th>Linear range</th>
<th>Input referred noise</th>
<th>Power</th>
<th>Area</th>
</tr>
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<tbody>
<tr>
<td>[20]</td>
<td>Three op-amp IA</td>
<td>High</td>
<td>Low</td>
<td>Low</td>
<td>High</td>
<td>High</td>
<td>Large</td>
</tr>
<tr>
<td>[33]</td>
<td>Current Feedback IA</td>
<td>High</td>
<td>High</td>
<td>Moderate</td>
<td>Low</td>
<td>High</td>
<td>Small</td>
</tr>
<tr>
<td>[34]</td>
<td>Chopper amplifier</td>
<td>High</td>
<td>High</td>
<td>Moderate</td>
<td>Low</td>
<td>Low</td>
<td>Large</td>
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area of the amplifier is the smallest among all the other bio-signal amplifiers. The total harmonic distortion (THD) is also very low.
CHAPTER III
PROPOSED BIO-SIGNAL AMPLIFIER

In this chapter, the proposed amplifier architecture, detailed circuit configuration, and major characteristics are addressed.

3.1 Amplifier architecture

Figure 3.1 shows the block diagram of the proposed amplifier architecture, which includes two stages. The first stage is an open-loop and the second stage is a closed-loop configuration. The first stage includes two differential voltage amplifiers with two voltage buffers. The second stage consists of a closed-loop class A amplifier ($M_{11}$ and $M_{12}$), output voltage buffer and the gain enhancement switches ($M_9$ and $M_{10}$). Due to the open-loop configuration of the first stage, the input impedance of the amplifier is high. The second stage is made closed-loop so as to minimize the overall amplifier gain degradation.

Due to the closed-loop configuration of the second stage, the input resistance of second stage is not high. The low input resistance of the second stage would reduce the effective gain of the first stage if the two stages were connected without buffering. To prevent this gain degradation voltage buffers are included in the first stage after the differential voltage amplifiers. An output buffer is also included in the
second stage to alleviate the loading effect, which enables the use of a lower feedback resistance as the output resistance of the buffer is small.

3.2 Operation of the proposed amplifier

The operation of the proposed amplifier can be divided into three regions depending on the differential input voltage between $V_{in+}$ and $V_{in-}$. The input voltages $V_{in+}$ and $V_{in-}$ consist of a common mode DC voltage of 1.65 V and small signal voltages $v_{in+}$ and $v_{in-}$, respectively. In the first region, the input voltage difference between $V_{in+}$ and $V_{in-}$ is small. In the second region $V_{in+} \gg V_{in-}$, and $V_{in+} \ll V_{in-}$ in the third region. We will describe the operation of the amplifier in three different regions separately.

If the input voltage difference is small, the output levels of both differential voltage amplifiers lie in the mid supply range, which will enable both second stage transistors $M_{11}$ and $M_{12}$ to operate. Both gain control switches $M_9$ and $M_{10}$ are off in this region. Fig. 3.2 shows the detailed circuit description of the proposed amplifier. The rail-to-rail differential pair in first stage consists of one NMOS and one PMOS input pair. The rail-to-rail input stage helps extend the linear operation range of the proposed amplifier. The small signal output voltage of NMOS-input differential pair $v_1$ and PMOS-input differential pair $v_3$ can be expressed as

$$v_1 = -A_{1n}(v_{in+} - v_{in-}) = -g_{m1,2}(r_{o2}||r_{o4})(v_{in+} - v_{in-})$$  \hspace{1cm} (3.1)  

15
Figure 3.1: Block diagram of the proposed amplifier

\[ v_3 = -A_{1p}(v_{in+} - v_{in-}) = -g_{m5,6}(r_{o6} || r_{o8})(v_{in+} - v_{in-}) \]  \hspace{1cm} (3.2)

where \( g_{m1,2} \) is the transconductance of \( M_1 \) and \( M_2 \) and \( g_{m5,6} \) is the transconductance of \( M_5 \) and \( M_6 \). \( r_{o2}, r_{o4}, r_{o5}, \) and \( r_{o6} \) are the output resistances of \( M_2, M_4, M_5 \) and \( M_6 \), respectively. \( A_{1n} \) and \( A_{1p} \) are the gains of NMOS-input and PMOS-input differential pairs, respectively. Applying KCL at node \( V_2 \) of Fig. 3.2,

\[ \frac{v_1 - v_2}{R_1} = \frac{v_2 - v_{out}}{R_2}. \]  \hspace{1cm} (3.3)

In a similar way applying KCL at node \( V_4 \),

\[ \frac{v_3 - v_4}{R_3} = \frac{v_4 - v_{out}}{R_4}. \]  \hspace{1cm} (3.4)
Writing a small signal node equation at node $V_p$ yields

$$g_{m11}v_2 + g_{m12}v_4 + \frac{v_p}{r_{o11}} + \frac{v_p}{r_{o12}} = 0 \quad (3.5)$$

where $g_{m11}$ and $g_{m12}$ are the transconductances of $M_{11}$ and $M_{12}$, respectively. $r_{o11}$ and $r_{o12}$ are the output resistances of $M_{11}$ and $M_{12}$, respectively. Writing a small signal node equation at node $V_{out}$ gives

$$\frac{v_{out} - v_2}{R_2} + \frac{v_{out} - v_4}{R_4} + \frac{v_{out} - v_p}{R_{buff}} = 0. \quad (3.6)$$

Assuming $R_2, R_4 \gg R_{buff}$, (3.6) gives that $v_{out} = v_p$, and (3.5) then gives

$$v_{out} = -g_{m11}(r_{o11}\|r_{o12})v_2 - g_{m12}(r_{o11}\|r_{o12})v_4. \quad (3.7)$$
We can combine eqs. (3.1)-(3.7) to obtain the overall voltage gain of the proposed amplifier. The overall voltage gain is given by

\[ A_{ov} = \left( g_{m1,2}(r_{o2}\|r_{o4})g_{m11}R_2 \right) + \frac{g_{m5,6}(r_{o6}\|r_{o8})g_{m12}R_4}{R_3+R_4} \left( r_{o11}\|r_{o12} \right). \]  

(3.8)

Due to the symmetrical design of the differential voltage amplifiers in the first stage, the node voltages \( V_1 \) and \( V_3 \) are assumed to be the same. By designing the transconductances in the second-stage equal, \( g_{m11} = g_{m12} \), the node voltages \( V_2 \) and \( V_4 \) will also be the same. Based on these assumptions, the second-stage open loop gain \( A_2 \) is defined as

\[ A_2 = \frac{v_{out}}{v_2} = \frac{v_{out}}{v_4} = -g_{m11,12} \times (r_{o11}\|r_{o12}). \]  

(3.9)

Substituting the expression of \( A_2 \) in (3.8), the overall gain of the amplifier is written as

\[ A_{ov} = - \frac{A_1R_2}{R_1+R_2} + \frac{A_1R_4}{R_3+R_4} - \frac{1}{A_2}. \]  

(3.10)

where \( A_1 = -g_{m1,2}(r_{o2}\|r_{o4}) = -g_{m5,6}(r_{o6}\|r_{o8}). \)

In the second region, where \( V_{in+} \gg V_{in-} \), the small signal voltages at node \( V_1 \) and \( V_3 \) move down, which lowers the voltages \( V_2 \) and \( V_4 \). As a result, the output voltage \( V_{out} \) will move towards \( V_{DD} \), and eventually put \( M_{11} \) into the linear region by decreasing the drain to source voltage. This will cause \( r_{o11} \) reduction, since the linear region output resistance is much lower than the saturation region output resistance. Therefore, the second-stage open loop gain is degraded by \( r_{o11} \) reduction, which decreases the second-stage closed-loop gain. But, the first-stage gain remains

18
constant. Therefore, to compensate the gain degradation, the high amplifier output voltage level activates $M_9$ and reduces the effective resistance of $R_1$. This reduction tends to increase the gain of the second stage, thereby compensating the reduction of $A_2$.

In the third region, where $V_{in+} \ll V_{in-}$, the low output voltage activates $M_{10}$ and reduces the effective resistance of $R_3$. This reduction tends to increase the gain of the second stage, thereby compensating the reduction of $A_2$.

3.3 Proposed amplifier circuit description

In this section, we will describe the detailed circuit design of different parts of the proposed amplifier. The sizes of all the NMOS and PMOS transistors in the first-
stage differential voltage amplifiers are chosen to make the $g_m$ of the NMOS input pair same as that of the PMOS input pair. The bias currents in the first-stage differential voltage amplifiers are set to 0.4 $\mu$A. The output common mode level of NMOS and PMOS input pairs are set to 1.65 V. The gains of both the differential voltage amplifiers are set to 31 dB. We will describe the second-stage after the buffer.

The proposed amplifier includes three rail-to-rail voltage buffers, all of the same design. Fig. 3.3 shows the rail-to-rail voltage buffer which includes a rail-to-rail differential pair combined with the output stage transistors $M_{9b}$ and $M_{10b}$ in a negative feedback configuration [37]. Sensing the voltage difference, the amplifier drives the gates of the output transistors to make the difference as small as possible. Large size transistors are used in the first stage to reduce the flicker noise. The major advantages of this buffer are the high output swing and low output resistance.

The gain of the buffer amplifier assuming no load is expressed as

$$|A_{\text{buff}}| = \frac{1}{1 + \frac{1}{(A_{nb}g_{m9b} + A_{pb}g_{m10b})(r_{o9b}||r_{o10b})}}$$

and the output resistance is

$$R_{\text{buff}} = \frac{(r_{o9b}||r_{o10b})}{1 + (A_{nb}g_{m9b} + A_{pb}g_{m10b})(r_{o9b}||r_{o10b})}$$

where $A_{pb} = g_{m_{5b,6b}}(r_{o6b}||r_{o8b})$ and $A_{nb} = g_{m_{1b,2b}}(r_{o2b}||r_{o4b})$.

The second-stage of the proposed amplifier includes closed-loop class-A amplifier, output voltage buffer and the gain control switches. The second-stage bias current is set to 1 $\mu$A and the size of transistors ($M_{11}$, $M_{12}$) are chosen in such a way
Figure 3.4: Resistance of $M_9$ and $M_{10}$ with $V_{\text{out}}$.

Figure 3.5: Second stage gain variation with $V_{\text{out}}$. 
that $g_{m11}$ equals $g_{m12}$. In addition, the values of $R_1$, $R_3$ and $R_2$, $R_4$ are set as 1 kΩ and 10 kΩ, respectively.

To control the closed-loop gain of the second-stage amplifiers, two transistors ($M_9$ and $M_{10}$) are used. The sizes of these two transistors are chosen in such a way that the effective resistance of $R_1\parallel R_{\text{on},M_9}$ or $R_3\parallel R_{\text{on},M_{10}}$ is changed properly when the output voltage moves to one of the rails. In this design, $(\frac{W}{L})_{M_9}=1 \mu\text{m}/0.7 \mu\text{m}$ and $(\frac{W}{L})_{M_{10}}=2.9 \mu\text{m}/0.7 \mu\text{m}$. The values of $R_1$ and $R_3$ are both set as 1 kΩ. Fig. 3.4 shows the on resistance of both $M_9$ and $M_{10}$ with amplifier output voltage variation obtained from circuit simulation.

The effective resistance $R_3\parallel R_{\text{on},M_{10}}$ varies from 1 kΩ for mid-range output voltages to 470.42 Ω as the output voltage approaches 0.3 V. The effective resistance $R_1\parallel R_{\text{on},M_9}$ varies similarly as the output voltage varies from mid-range to 3.08 V.

Fig. 3.5 shows the second stage open loop gain $A_2$ with output voltage level, which is obtained from the circuit simulation. The second-stage gain degradation is due to the output resistance variation with output voltage as mentioned in the introduction. In order to obtain $A_2$ with different amplifier output levels, the node voltages $V_2$, $V_4$ and $V_{\text{out}}$ are plotted by changing the input voltages ($V_{\text{in}+}$ and $V_{\text{in}-}$) from 0 V to 3.3 V, and observing $V_2 = V_4$, the ratio between $V_{\text{out}}$ and $V_2$ or $V_4$ is taken. The ratio between $V_{\text{out}}$ and $V_2$ or $V_4$ will be the same since the feedback in the second stage makes the node voltages $V_2$ and $V_4$ equal. Next, the x-axis is changed from $V_{\text{in}}$ to $V_{\text{out}}$ in the circuit simulator.
Fig. 3.6 shows the calculated overall voltage gain of the amplifier as a function of the second-stage open loop gain $A_2$. The range of $A_2$, from 16 dB to 25.1 dB corresponds to the amplifier output voltage range of 3.08 V to 1.65 V. The overall voltage gain without the contribution of the gain control switches ($M_9$ and $M_{10}$) is obtained by using equation (3.10). However, in order to find the overall gain with the contribution of the gain control switches, the on resistance of $M_9$ ($R_{\text{on},M_9}$) and $M_{10}$ ($R_{\text{on},M_{10}}$) with different $V_{\text{out}}$ levels were obtained from Fig. 3.4, and the effective resistance values $R_1||R_{\text{on},M_9}$ and $R_3||R_{\text{on},M_{10}}$ were calculated. In addition, the second stage gain $A_2$ with different $V_{\text{out}}$ levels were found from Fig. 3.5. From this information, we can figure out the effective resistance values corresponding to specific $A_2$ levels. Finally, the overall gain was obtained by replacing the actual values of the effective resistance $R_1||R_{\text{on},M_9}$, $R_3||R_{\text{on},M_{10}}$ and $A_2$ in the modified version of equation (3.10) which is given as

$$A_{\text{ov}} = -\frac{A_1R_2}{R_1'+R_2} + \frac{A_1R_4}{R_3'+R_4} - \frac{1}{A_2}.$$  

(3.13)

where $R_1' = R_1||R_{\text{on},M_9}$ and $R_3' = R_3||R_{\text{on},M_{10}}$. When $V_{\text{out}}$ is near ground, $M_9$ is off ($R_{\text{on},M_9} = \infty$) and when $V_{\text{out}}$ is near 3.3 V, $M_{10}$ is off ($R_{\text{on},M_{10}} = \infty$). As shown, the overall gain changes about 3 dB without the gain control switches and only 1.7 dB with the gain control switches, as the output voltage changes from 1.65 V to 3.08 V. This is due to the effective resistance reduction of $R_1'$ or $R_3'$ that compensates the $A_2$ reduction. Assuming the resistance variation (Fig. 3.4) and $A_2$ variation (Fig. 3.5) are symmetric with respect to 1.65 V, the overall voltage gain change will
be the same as the output voltage changes from 0.3 V to 1.65 V. The conventional case refers to a two stage amplifier [38]. In this case the overall gain is assumed
as $A_{ov} = A_1 \times A_2$, where $A_1$ is the first stage open loop gain. The overall gain degrades with $A_2$ variation for the conventional case whereas it is almost constant for the proposed case. The overall gain degradation is 8.8 dB for the conventional case as the output voltage changes from 1.65 V to 3.08 V. The detailed overall gain variation with output voltage is shown in Chapter V. The transistor sizes and bias current values are shown in Table 3.1.

3.4 Frequency compensation

Frequency compensation is required for stable feedback operation when the amplifier has more than two poles inside the unity gain bandwidth. To improve the phase margin of the amplifier two Miller compensation capacitors $C_{c1}$ and $C_{c2}$ can be used between the first-stage differential pairs and second stage as shown in Fig. 3.7. The compensation capacitors are placed at the output node of the first-stage differential pairs instead of the output node of the first-stage buffers. Capacitors of 0.5 pF were used in the remainder of the thesis. Much larger compensation capacitors would be required if they were connected to the outputs of the first-stage buffers, because the output resistance of the buffers is low. In addition, assuming $C_{c1}$ and $C_{c2}$ are identical, the poles from the NMOS-input and PMOS-input differential pairs in the first-stage will move to the lower frequency in a similar manner, since the NMOS-input and PMOS-input pairs are symmetric. The detailed frequency response analysis of this amplifier is a future work of this thesis.
Figure 3.7: Proposed amplifier with compensation capacitors

Figure 3.8: AC simulation test bench
Fig. 3.8 shows the AC simulation test bench. A $1 \text{ V}_{\text{pp}}$ sinusoidal signal is applied as an input and the frequency is swept from 1 kHz to 100 MHz. A 5 pF capacitor is used as the load, which accounts for the pad and the probe capacitance.

The frequency response of the amplifier after compensation is shown in Fig. 3.9. The simulation result shows a $76.48^\circ$ phase margin. Although two external compensation capacitors are used, these can be placed on chip by increasing the amplifier core area of 10%.
CHAPTER IV
NON-IDEALITIES ANALYSIS

Noise, common mode spur, and finite power line interference are the major non-idealities that critically limit the performance of bio-signal amplifiers. Therefore, bio-signal amplifiers require high CMRR and high PSRR while maintaining low noise. In this chapter, we will analyse the noise, CMRR and PSRR performance of the proposed amplifier.

4.1 Noise analysis

An ECG signal differs in magnitude from patient to patient and can typically be in the range of 80-2000 $\mu$V [39]. With such small magnitude, the quality of the bio-potential signals can be easily corrupted with noise. The flicker noise dominates due to the low frequency nature of bio-potential signals.

The total input referred noise of the proposed amplifier is expressed as

$$
\overline{V_{ni}^2} = \overline{V_{n1}^2} + \overline{V_{p1}^2} + 2 \times \frac{V_{b1}^2}{A_1^2} + 4 \times \frac{V_{R2}^2}{A_1^2} + \frac{V_{b2}^2}{A_1^2} \times \left( 1 + \frac{R_1 \parallel R_3}{R_2 \parallel R_4} \right)^2 + \left( \frac{R_1 \parallel R_3}{R_2 \parallel R_4} \right)^2 \frac{V_{b2}^2}{A_1^2} \tag{4.1}
$$

where

$\overline{V_{n1}^2}$ = Noise power of the first stage NMOS input differential pair

$\overline{V_{p1}^2}$ = Noise power of the first stage PMOS input differential pair
\( V_{b1}^2 = \) Noise power of the first stage buffer

\( V_R^2 = \) Noise power of resistor

\( V_2^2 = \) Noise power of second stage

\( V_{b2}^2 = \) Noise power of second stage buffer.

Table 4.1: Noise contribution from each block

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<thead>
<tr>
<th>Block name</th>
<th>Input referred noise power</th>
<th>Percentage</th>
</tr>
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<tbody>
<tr>
<td></td>
<td>([V^2])</td>
<td>(%)</td>
</tr>
<tr>
<td>PMOS diff pair (1st stage)</td>
<td>(2.3 \times 10^{-12})</td>
<td>54.3</td>
</tr>
<tr>
<td>NMOS diff pair (1st stage)</td>
<td>(1.87 \times 10^{-12})</td>
<td>44.2</td>
</tr>
<tr>
<td>Buffer (1st stage)</td>
<td>(2 \times 10^{-14})</td>
<td>0.47</td>
</tr>
<tr>
<td>2nd stage</td>
<td>(2.12 \times 10^{-15})</td>
<td>0.05</td>
</tr>
<tr>
<td>10k resistance</td>
<td>(6.68 \times 10^{-23})</td>
<td>0</td>
</tr>
<tr>
<td>1k resistance</td>
<td>(4 \times 10^{-22})</td>
<td>0</td>
</tr>
<tr>
<td>Total noise power</td>
<td>(4.24 \times 10^{-12})</td>
<td>100%</td>
</tr>
</tbody>
</table>

Table 4.1 shows the noise contribution of each circuit block obtained from noise simulation where the input referred noise power is obtained by integrating the noise spectrum within the amplifier bandwidth of 0.2 Hz to 12.1 kHz. The main
noise contributor are the NMOS-input and PMOS-input differential pairs in the first stage. The inter-stage buffers in the first stage have also some noise contribution. In comparison, the class-A amplifier and the resistors in second stage have negligible noise contribution to the total input-referred noise. Total input referred noise is $V_n^2 = 4.24 \times 10^{-12} \, \text{V}^2$ and the rms noise voltage is $V_n = 2.06 \, \mu\text{V}$.

The difference between the proposed amplifier and the conventional two-stage amplifier is the additional buffer noise, $V_{b1}^2$, $V_{b2}^2$ and resistor noise, $V_R^2$ due to the second-stage closed-loop configuration. However, the additional buffer, feedback resistor, and the second-stage amplifier noise is negligible. Furthermore, in order to reduce the flicker noise, the length of each transistor is increased from 350 nm to 700 nm.

4.2 Common mode rejection ratio (CMRR)

The CMRR of IA based bio-signal amplifiers are primarily affected by impedance mismatch at the amplifier input node, feedback resistor mismatches and finite CMRR of individual amplifiers consisting the IA [7]. CMRR degradation leads to increased offset voltage at the amplifier output. The output voltages due to a common mode input signal $V_{in,cm}$ of NMOS-input and PMOS-input differential pairs (Fig. 3.2) are given by [40]
\[ v_1 = -\frac{g_{m1,2}}{(1 + 2g_{m1,2}R_{ss1})g_{m3,4}}v_{in,cm} \] 

\[ v_3 = -\frac{g_{m5,6}}{(1 + 2g_{m5,6}R_{ss2})g_{m7,8}}v_{in,cm} \]

where \( R_{ss1} \) and \( R_{ss2} \) are the output resistance of NMOS-input and PMOS-input differential pair tail current sources. Furthermore, the overall common mode gain can be obtained by combining the first-stage common mode gain with the second-stage gain. That is

\[ A_{cm,ov} = \frac{g_{m1,2}R_2}{(1+2g_{m1,2}R_{ss1})g_{m3,4}(R_1+R_2)} + \frac{g_{m5,6}R_4}{(1+2g_{m5,6}R_{ss2})g_{m7,8}(R_3+R_4)} \cdot (4.3) \]

As a result, using (3.7) and (4.3) the CMRR of the proposed amplifier is expressed as

\[ CMRR = \left| \frac{A_{ov}}{A_{cm,ov}} \right| = \frac{\frac{g_{m1,2}R_2}{(1+2g_{m1,2}R_{ss1})g_{m3,4}(R_1+R_2)} + \frac{g_{m5,6}R_4}{(1+2g_{m5,6}R_{ss2})g_{m7,8}(R_3+R_4)}}{\frac{A_1R_2}{R_1+R_2} + \frac{A_3R_4}{R_3+R_4}}. \] 

(4.4)

From (4.4), we see that CMRR can be increased by increasing the output resistance of the tail current source (\( R_{ss1} \) and \( R_{ss2} \)). In addition, the CMRR can also be increased by increasing the size of \( M_3, M_4 \) and \( M_7, M_8 \), which increases the \( g_m \). The calculated CMRR of the proposed amplifier is 81.24 dB.

4.3 Power supply rejection ratio (PSRR)

Bio-signals such as the ECG and EEG are often contaminated with 60 Hz power line interference. For ECG, due to unbalanced electrode-skin impedances a common
mode voltage induced from 60 Hz power line can be transformed into a differential error voltage [41]. Therefore, to suppress the power line interference high PSRR is required. However, the positive rail PSRR+ is more critical than the ground line PSRR-. As a result, we will only consider the PSRR+ for the proposed amplifier.

The circuit diagram for calculating the power gain is shown in Fig. 4.1. There are three paths that connects the power rail $V_{\text{DD}}$ to the amplifier output, $V_{\text{out}}$. The power gain of the proposed amplifier is obtained by combining the power gain of each path, which is expressed as

$$A_{pG} = \left(1 + \frac{R_2}{R_1}\right) - \left(1 + \frac{1}{A_2}\left(\frac{R_2}{R_1}\right)\right) - \left(1 + \frac{1}{A_2}\left(\frac{R_4}{R_3}\right)\right)$$

Figure 4.1: Model for PSRR analysis
where, $g_{mp}$ denotes the transconductance of the PMOS-input pair tail current source $M_p$. As shown, the power gain of path(i) is positive and the power gains of path(ii) and path(iii) are negative. The power gain of the proposed amplifier can be made nearly zero by setting $\frac{g_{mp}}{2g_{m7}} = \frac{R_3}{R_4}$, which will significantly improve the PSRR+. The buffers can also affect the power gain, however due to the negative feedback operation in the buffers, simulation results show buffer power gain of -66 dB, which is negligible. The overall power gain of the proposed amplifier is -39.5 dB and considering the differential gain of 48 dB, PSRR+ of 87.5 dB can be obtained.

In this chapter we describe noise, CMRR and PSRR of the proposed amplifier. The input referred noise of the amplifier is not high. The amplifier exhibits high CMRR and PSRR. In the next chapter, we will describe about the test set-up and measurement results of different parameters of the proposed amplifier.
CHAPTER V
EXPERIMENTAL RESULTS

In the previous chapters, we analysed the operation of the proposed amplifier and the effect of non-idealities on the amplifier performance. In this chapter, we will present the simulation and measurement results for different parameters. The chapter concludes by comparing the proposed amplifier with other bio-signal amplifiers for DC gain, CMRR, PSRR, THD, input-referred noise, bandwidth and area.

The proposed amplifier is implemented in 0.35\(\mu\)m two-poly four-metal analog CMOS technology with supply voltage of 3.3 V. The resistors \(R_1 \sim R_4\) are realized using n-well diffusion type resistors to reduce the area. A die photograph of the proposed amplifier is shown in Fig. 5.1. The die area of the proposed amplifier is 0.063 mm\(^2\). The second stage buffer is divided into two parts.

A two layer PCB as shown in Fig. 5.2 is designed to test the proposed amplifier. The test bench set-up is shown in Fig. 5.3. The test chip is shown with dotted lines. The bias circuit consists of a differential amplifier, a resistor (2 M\(\Omega\)) and the current mirror. A DC power supply of 1.65 V with a 110 k\(\Omega\) resistor is used to generate the 15 \(\mu\)A current to bias the differential amplifier. Due to the negative feedback operation in the bias circuit, the node voltage \(V_x\) is equal to the differential amplifier input 1.4 V. A 2 M\(\Omega\) resistor is used to generate the 0.7 \(\mu\)A bias current for
the proposed amplifier. In addition, differential inputs with common mode voltage level of 1.65 V are applied to the proposed amplifier. The output waveform of the proposed amplifier is observed using an oscilloscope.

The test set-up to measure the transfer characteristic of the amplifier is shown in Fig. 5.4. The amplifier is put into the unity gain buffer configuration where the input $V_{in}$ is varied from -1.65 V to 1.65 V. Fig. 5.5 shows the transfer characteristic of the proposed amplifier. The linear operation range of the amplifier is from 0.1 V to 3.09 V for the simulation and from 0.3 V to 3.08 V for the measurement. The wide linear operation range is achieved by the second-stage closed-loop configuration with the gain control feature.

Fig. 5.6 shows the DC simulation test bench. Two voltage controlled voltage sources with opposite gain are used to generate the differential inputs of the amplifier.
Figure 5.2: Two layer PCB test board
Figure 5.3: Experimental set-up of the amplifier

Figure 5.4: Test bench for transfer characteristic
The DC voltage $V_{\text{in}}$ is varied from -1 V to 1 V. The gain is measured from the slope of the transfer characteristic. Fig. 5.7 shows the DC gain as a function of the output voltage where simulation results with and without the gain control switches are given as a reference. The measurement result shows the overall DC gain remains at 46 dB or higher for output range from 0.3 V to 3.08 V. The slight increase of the DC gain near the supply rails is due to the gain enhancement feature, which extends the linear operation range of the amplifier.

A test set-up for common mode gain measurement is shown in Fig. 5.8. A 1 V$_{\text{pp}}$ sinusoidal input signal is applied to both input terminals of the amplifier. The differential gain (3.8) is divided by the common mode gain (4.3) to obtain the CMRR.
Figure 5.6: DC simulation test bench

Figure 5.7: DC gain as a function of amplifier output voltage
of the amplifier. Fig. 5.9 shows the measured and simulation (with and without resistor mismatch) CMRR versus frequency. As shown, with 20% resistor mismatch for all the resistors $R_1 \sim R_4$, the CMRR degradation is only 2 dB. This shows the CMRR of the proposed amplifier is not sensitive to resistor mismatch which is an advantage compared to IA based bio-signal amplifiers. Furthermore, according to (4.4), process induced mismatches of the transistors reduces the CMRR. Therefore, the common-centroid layout technique is used for $M_1, M_2$ and $M_5, M_6$ to reduce the device mismatch.

Fig. 5.10 shows the test set-up for power gain measurement. A 1 V$_{pp}$ sinusoidal input signal is applied at the supply rail $V_{DD}$ where both inputs are tied to the common mode voltage 1.65 V. The differential gain (3.8) is divided by the power gain (4.5) to obtain the PSRR+ of the amplifier. Fig. 5.11 shows the simulated and
measured PSRR+ versus frequency, where the simulation and measurement results show 87.55 dB and 84 dB, respectively. The difference between the simulation and measurement results can be due to feedback resistor mismatch and process variation that increases the power gain of the amplifier as given in (4.5).

Fig. 5.12 shows the amplifier output spectrum with a 100 Hz sinusoidal input. The test bench shown in Fig. 5.3 is used to obtain the output spectrum of the amplifier where the output waveform is captured by the data acquisition unit (DAQ), and the output spectrum is generated by LABVIEW. In the output spectrum, the power tone is observed at 60 Hz, and the third and fifth harmonics are at 300 Hz and 500 Hz. However, the harmonic tones are small compared to the fundamental tone.
Figure 5.10: Test bench for measuring the power gain

Figure 5.11: PSRR+ of the amplifier
Figure 5.12: Measured output spectrum of the amplifier with a 100 Hz sinusoidal input.

Figure 5.13: THD of the amplifier as a function of frequency.
The total harmonic distortion (THD) of the amplifier is 0.04% for a 20 mV_{pp} input, and is constant up to 1 kHz (Fig. 5.13). The noise floor is around -75 dB.

Fig. 5.14 shows the measured time domain input referred noise waveform. Without providing any input to the amplifier, the output of the amplifier is observed in LABVIEW. Fig. 5.15 shows the measured input-referred voltage noise spectrum, which is obtained by taking the fast Fourier transform of the time domain waveform shown in Fig. 5.14. The thermal noise level is around 48.98 nV/√Hz, with 1/f noise corner at 100 Hz. Integrate this waveform from 0.2 Hz to 12.1 kHz yields an rms noise voltage of 2.06 µV_{rms}. The power tone is visible at 60 Hz, which is the primary source of noise that increases the input-referred noise power of bio-signal amplifiers.
Figure 5.15: Input-referred voltage noise spectrum. Integration under this spectrum yields an rms noise voltage of $2.06 \mu V_{\text{rms}}$

The set-up shown in Fig. 5.4 is used to obtain the step response where the input is replaced with a step input. Fig. 5.16 shows the step response of the amplifier with a $1.8 \, V_{p-p}$ square wave input and a 5 pF load capacitor. The settling behavior of the proposed amplifier indicates the proper operation of the frequency compensation with sufficient phase margin.

Actual ECG signals obtained from the MIT-BIH database [42] are applied to the proposed amplifier with the data acquisition board. The database contains 8 half-hour excerpts of two-channel ambulatory ECG recordings, obtained from 47 subjects. An example input ECG signal (normal) is shown in Fig. 5.17. The amplified output is captured with an oscilloscope which is shown in Fig. 5.18. Fig. 5.19 and Fig. 5.20
Figure 5.16: Measured output signal with a square input signal of 1.8V\textsubscript{p-p}

show the input and amplified output waveforms for another ECG signal from the database (abnormal). The proposed amplifier showed proper amplification for both ECG signals.

The amplifier consumes 5.6 \mu A current from a 3.3 V supply. As a result, total power consumption of the amplifier is 18.5 \mu W. The input referred noise is 2.06 \mu V_{rms}. The power consumption is 18.5 \mu W and the core area of the amplifier is 0.063 mm\textsuperscript{2}. In addition, the wide bandwidth (0.2 Hz - 12.1 kHz) of the proposed amplifier makes it suitable to amplify a variety of bio-signals.

A detailed performance summary of other bio-signal amplifiers are shown in Table 5.1. The proposed amplifier is much simple compared to current feedback IAs [14, 29, 30] or chopping amplifiers [43]. The power consumption is relatively
Figure 5.17: Input ECG signal (usual)

Figure 5.18: Amplified ECG signal (usual)
Figure 5.19: Input ECG signal (abnormal)

Figure 5.20: Amplified ECG signal (abnormal)
low, and the voltage gain and CMRR are comparable to other amplifiers. The core area of the proposed amplifier is much small compared to other bio-signal amplifiers. In addition, a very low THD is achieved due to the wide linear operation range. Therefore, the proposed amplifier can amplify small amplitude bio-signals without distortion.
<table>
<thead>
<tr>
<th>Ref.</th>
<th>Technology</th>
<th>Supply voltage (V)</th>
<th>Voltage gain (dB)</th>
<th>CMRR (dB)</th>
<th>PSRR (dB)</th>
<th>THD (%)</th>
<th>Input ref. noise (µV rms)</th>
<th>Power (µW)</th>
<th>Area (mm²)</th>
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<tr>
<td>[22]</td>
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<td>83</td>
<td>85</td>
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CHAPTER VI
CONCLUSION

A compact and low power bio-signal amplifier with extended linear operation range is proposed. A first-stage open-loop and second-stage closed-loop configuration with gain control feature is applied to extend the linear operation range of the amplifier. This approach enables low power and small size while maintaining sufficient CMRR and PSRR. A very low THD is achieved due to the wide linear operation range. Therefore, the proposed amplifier is suitable for portable bio-signal sensing devices.

The wide bandwidth of the amplifier makes it suitable to amplify any type of bio-signals, such as ECG, EEG and EMG. The performance of the amplifier is verified with ECG signals. In the future, the amplifier will be tested for EEG and EMG signals. The amplifier can be used in wireless body sensor networks. The primary focus of designing this amplifier is to reduce power, noise and area, so that it can be implantable on a human body. Another option is to combine the proposed amplifier with an energy harvesting device. In that case, the supply voltage and power consumption of the amplifier should be further reduced.
BIBLIOGRAPHY


